THE UNIVERSITY OF CALGARY

HARMONIC TUNING FOR HIGH EFFICIENCY IN POWER AMPLIFIERS

BY

ANDREW FRAENKEL GIBSON

A THESIS
SUBMITTED TO THE FACULTY OF GRADUATE STUDIES
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE
DEGREE OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL ENGINEERING

CALGARY, ALBERTA

SEPTEMBER, 1992

ISBN 0-315-83150-2

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  - Anatomie 0287
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  - Botanique 0309
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  - Écologie 0329
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  - Génétique 0369
  - Limnologie 0793
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  - Genéralités 0485
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ABSTRACT

This investigation is concerned with power amplifiers operating at high frequencies with maximized power added efficiency.

The approaches traditionally employed to raise amplifier efficiency are reviewed, followed by the waveforms and harmonic combinations required for harmonic tuning. Significant performance gains may be achieved by the correct use of the second and/or third harmonic voltages on the transistor collector (drain). Next, descriptions of the measurement system, the circuit and the simulation system are presented.

Measured and simulated performance of an unmodified amplifier and the same circuit with second harmonic tuning is given. The theoretical performance gains are proven in both the physical and simulated measurements. Finally, some measured effects of third harmonic tuning and the effects of tuning on amplifier linearity are summarized.

A significant part in this work is that conclusions are drawn from measurement and simulation of an actual amplifier circuit rather than from a set of idealized assumptions.

ACKNOWLEDGMENTS

The author wishes to express his appreciation for the supervision, guidance and support of Dr. R.H. Johnston.

Thanks are offered to friends and colleagues for their interest in this work. This is specially true for my parents and the members of the 746 Calgary Communication Squadron.

The author is indebted to the University of Calgary and Telecommunications Research Laboratories for both financial and material support.

TABLE OF CONTENTS

List of Tables

List of Figures

CHAPTER ONE
INTRODUCTION

1.1 Object of Investigation

This thesis is concerned with practical means of increasing the efficiency of radio frequency amplifiers. While there have been many theoretical investigations of high efficiency amplifiers most have involved idealized and assumed waveforms. Experimental testing has generally been done at fairly low frequencies, where rapid transistor switching is more easily achieved.

The present work involves both experimentation at 400 MHz and theoretical development. One standard amplifier is used to allow the direct comparison of different methods of achieving high efficiency.

1.2 Background

In a transmitter the final stage or stages of power amplification use most of the total supply power. Even in a transceiver the power amplifier uses a large share of the input power. This may be seen in transceiver battery specifications given in terms of an n:1 listen to talk ratio, where n may be 8 or even higher. Long periods of transmission can rapidly drain the batteries. An improvement in power amplifier efficiency will therefore have a considerable influence on the efficiency of an entire radio set. In a battery operated set this would allow the use of smaller batteries or longer operation. Even when almost unlimited supply power is available, high efficiency power amplifiers are desirable. In very high power transmitters, for instance commercial broadcast stations, the cost of utility power is considerable. The removal of heat from a power amplifier can also be a design problem. Large transmitters may need forced water cooling, while the heat released from portable or vehicle mounted sets may lead to operator discomfort and premature equipment failure. In higher efficiency power amplifiers heat sink requirements are reduced or eliminated. The final result is smaller, lighter and more reliable equipment.

Because most early amplifier design was empirical it is difficult to place an exact time when specific forms of high efficiency amplifier were first used. Raab *(1)* suspects that harmonically tuned class F amplifiers may have been the earliest high efficiency designs. This class of amplifier evolved from the conventional class A, B and C approaches in the quest for lower power loss. Class A amplifiers have a low efficiency because they have collector current and voltage on the collector at all times. Class B and C improve this by progressively reducing the interval of collector current flow and using resonant circuits to maintain a sinusoidal collector voltage. Short current pulses lead to a reduced average voltage-current product at the collector and thereby lower power dissipation in the transistor. The only drawback is that in the limit as collector efficiency approaches 100% output power approaches zero. A 100% efficient class C amplifier is thus a virtually useless circuit with no output.

Class F amplification is one solution to this problem. In the form of interest here harmonic components of the amplified output of a transistor are reflected back to the collector from the load with the proper phase to create a square edged collector voltage with a relatively flat minimum during the current pulse. The sharp edges of the voltage waveform cause a reduced collector voltage during the pulse, reducing the voltage-current product and raising efficiency.

This result may be found at lower frequencies by operating the transistor as a switch. At higher frequencies, though, switching time limits the sharpness of transition edges. Harmonic tuning demands rather less performance of an active device, extending the range of usefulness. Some improvement is possible by reflecting back either the second or third harmonic, while a larger improvement is theoretically possible by reflecting all the odd harmonics back to the collector of the transistor(*1*, *2*). The upper harmonics are less likely to be generated or to escape the transistor, so the analysis in this thesis focuses on the lower harmonics only.

Efficiency is always desired in a circuit. Unfortunately there are many ways of reporting measured efficiency. Usually,

$$\text{efficiency} = \frac{\text{Useful Output Power}}{\text{Total Input Power}}$$

Collector efficiency, though, does not follow this broad approach. Instead,

$$\text{collector efficiency} = \eta_c = \frac{\text{Output Power}}{\text{DC Input Power}}$$

This last definition neglects the RF input power. While justifiable in high gain circuits, in low gain circuits this may lead to considerable overestimation of efficiency and could result in damage to the active device. As an example, consider an amplifier using a one Watt device with 50% collector efficiency, 500 mW output and 3 dB gain. Such a circuit seems at first glance to have a safety factor of 2; recall, though, that an amplifier with 3 dB gain also has half its output power dissipated in its input. The total power dissipated in the device is thus 500 + 250 mW = 750 mW, lowering the safety factor to 1/.75 = 1.33. Lower collector efficiency will exacerbate this condition, as will any transistor performance drop at higher temperatures. A design based on collector efficiency where gain is not high would tend to allow the device to overheat and suffer premature failure.

Efficiency is conventionally defined as the percentage of total input power that is transformed into useful output. This includes the input signal power. Conventional efficiency is more useful than collector efficiency when applied to power amplifiers.

$$\text{efficiency} = \eta = \frac{\text{RF Output Power}}{\text{DC Power + RF Input Power}}$$

recalling that $P_{out} = \eta_c * P_{dc}$

$$\text{then } \eta = \frac{G*\eta_c}{G + \eta_c}$$

where G = power gain as a ratio

For high gain operation, collector efficiency is approximately the same as true efficiency. For lower gain this is increasingly untrue, as shown in table 1.2.1

Table 1.2.1 Comparison of Collector Efficiency and True Efficiency

Gain (dB)	Collector Efficiency	True Efficiency
20	0.8	0.794
10	0.8	0.741
6	0.8	0.667
3	0.8	0.571
0	0.8	0.444

Except when used as an isolation buffer a unity gain amplifier is not normally useful. Systems can be made better and smaller if all amplifier/buffers still have some reasonable level of gain.

While a unity gain circuit with 100% collector efficiency has a real efficiency of 44% this is deceptive. It still seems useful, when really such a stage is wasting DC power and space while contributing no additional signal strength. A better way of reporting amplifier performance is through power added efficiency, PAE.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}$$

In the case of the unity gain amplifier the input power equals the output power and the power added efficiency is zero. This is a much better representation of the effectiveness of low gain amplifiers and also accounts for input power dissipation. Neglecting any power consumed to set the transistor bias,

$$PAE = \frac{P_{out} - \frac{P_{out}}{G}}{\frac{P_{out}}{\eta_c}} = \eta_c * \frac{G-1}{G}$$

This leads to the example values of PAE given in table 1.2.2. For unity or higher gain conventional efficiency has a limited numeric range of 50 to 100%. Over the same range PAE goes from 0 to 100%. In a circuit requiring reasonable amounts of gain and not demanding a large number of low gain stages (to achieve stability, for instance) the circuit size is minimized and overall efficiency increased by the use of higher gain stages. Power Added Efficiency acts as a figure of merit partly based on gain, and will be used in this work whenever possible.

Table 1.2.2 Comparison of Collector Efficiency and Power Added Efficiency

Gain (dB)	Collector Efficiency	PAE
20	0.8	0.792
10	0.8	0.72
6	0.8	0.6
3	0.8	0.4
0	0.8	0.0

1.3 Classical Amplifiers

As mentioned before, class A amplifiers have low efficiency. Their advantages are high linearity and ease of design and construction. Class A linearity is gained by biasing the transistor so that there is always some collector current. Small signal and low noise amplifiers are an extreme example, where the current flow due to the signal of interest is a negligible part of the total collector current. While the efficiency of such a stage is very low the impact on overall system efficiency is slight if the amplifier still consumes little power. The degree to which this is true varies; very different levels of waste power are negligible in comparison between a commercial radio transmitter and a hand held telephone.

The least efficient class A amplifier is resistively loaded. For a quiescent collector current Icq the load resistor R_l dissipates Icq^2*R_l. The transistor collector voltage will also sit near some rest level V_{cq} while drawing I_{cq} and will itself dissipate roughly $V_{cq}*I_{cq}$. An example of such an amplifier is shown in fig 1.3.1.

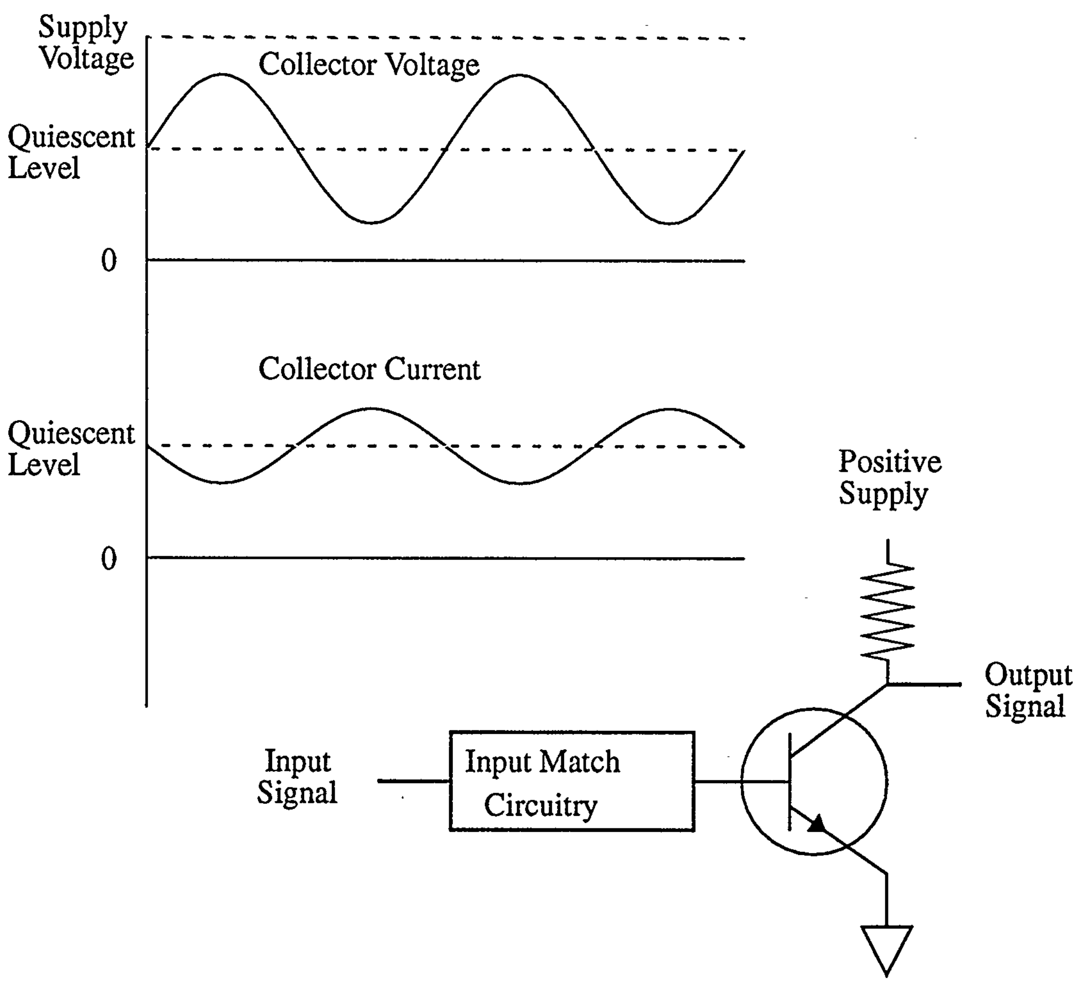


Figure 1.3.1 Resistive Load

The first step to higher efficiency is to replace the load resistor by an inductor. A properly chosen inductor will have a high quality factor (Q) around the frequency of use. It should have virtually no resistance to the collector bias current while presenting a very high impedance to the output RF signal. This has the effect of making the collector bias voltage equal the supply level, and removes the $Icq^2 * R_l$ loss.

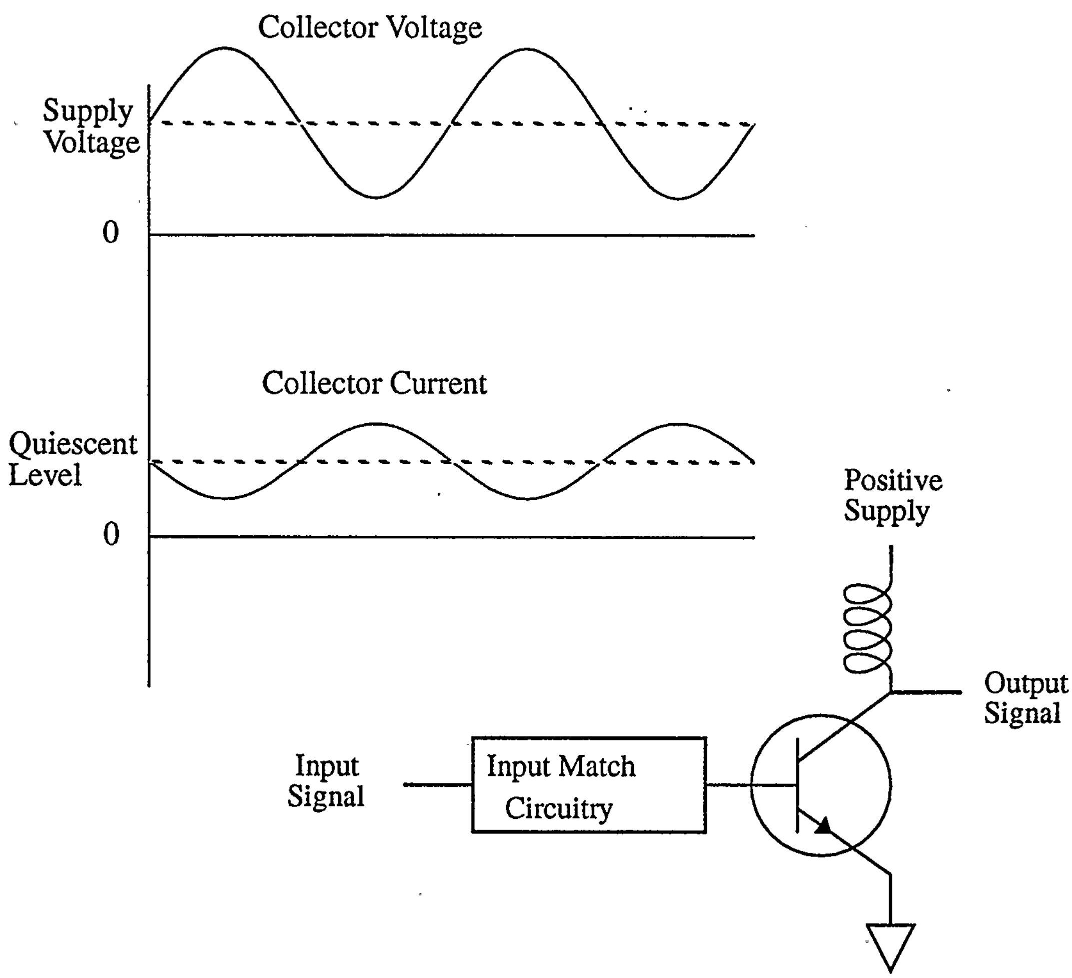


Figure 1.3.2 Inductive Load

Once this is done there is still inefficiency through collector power dissipation. The average value of the instantaneous voltage-current product is the power lost in the transistor. Even when large voltage and current variations occur in class A operation some non zero voltage-current product always exists.

Class B amplifiers reduce power loss by allowing transistor conduction through only half of each cycle. For narrowband applications the missing half cycle can be filled in by a resonant circuit, while for broadband use two transistors operating on alternate half cycles are employed. These transistor pair class B circuits are called push-pull amplifiers, indicating the alternating amplification. One device amplifies the positive half of the input waveform while the other amplifies the negative half.

For these class B circuits the collector voltage-current product is now zero for half of each cycle, lowering the average dissipation. Maximum theoretical efficiency and output power are achieved if the output voltage swings down to zero and up to two times the supply voltage. In real amplifiers with saturation voltages, the maximum realizable swing is from the transistor collector-emitter saturation voltage up to double the supply voltage minus the saturation voltage.

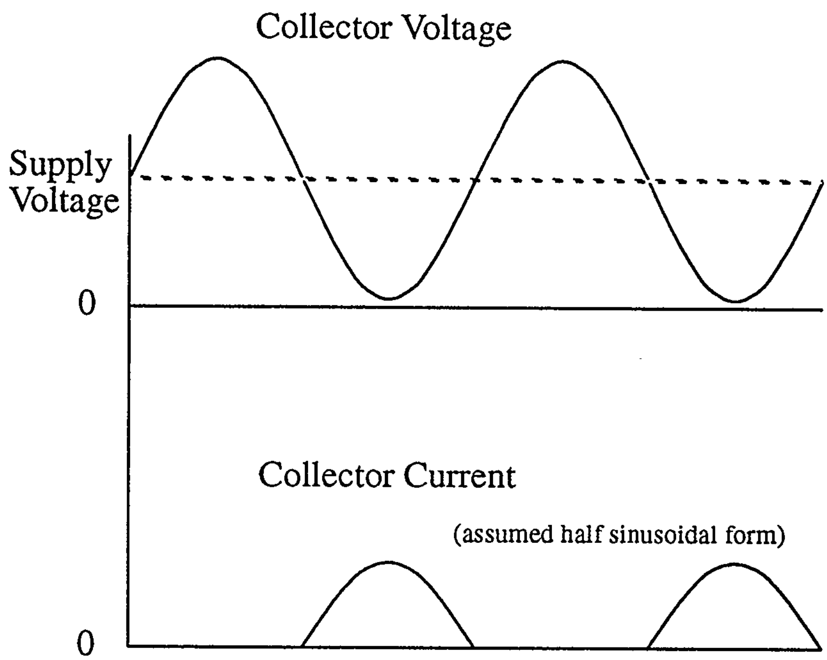


Figure 1.3.3 Class B Waveforms

Class C amplifiers use this idea to further reduce the collector dissipation; the interval of current flow in the amplifying device is reduced below 180 degrees. While a class B amplifier could be made linear by using two push-pull transistors, class C amplifiers are very nonlinear and must rely on tuned resonant circuits to remove the harmonics from the output waveforms. Collector efficiency, the fraction of DC supply power converted to useful output, rises as the current flow duration is reduced. Unfortunately, the maximum possible output power also drops. A class C amplifier with a collector current-voltage product of zero can be designed but it would also have zero output power (16). There is a definite tradeoff between efficiency and output power which must be addressed in such a design.

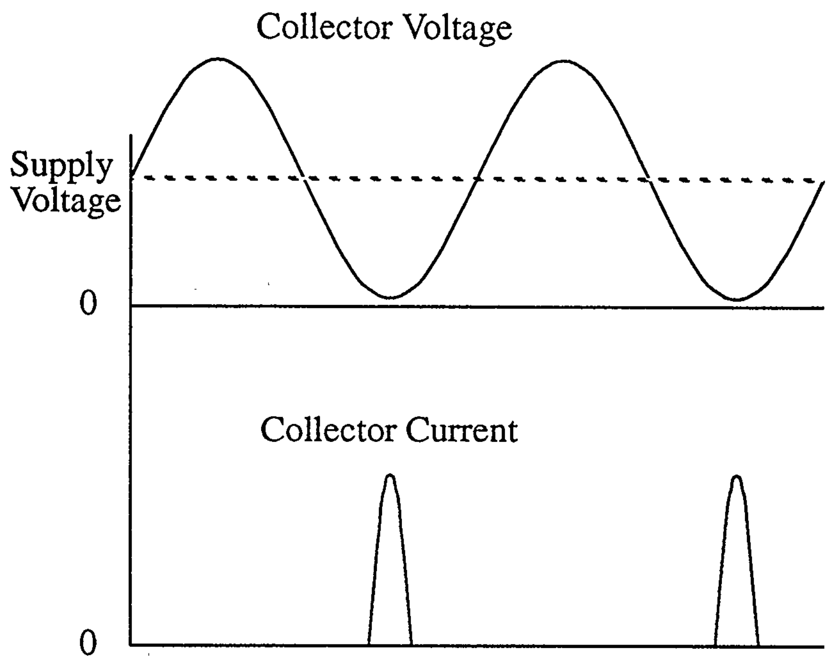


Figure 1.3.4 Class C Waveforms

These are the classical types of power amplifier, along with several combinations of biasing such as class AB, where the conduction interval is between 180 and 360 degrees. Harmonic tuning is one of several higher efficiency operating modes which should boost amplifier performance without decreasing the useful output power.

1.4 High Efficiency Harmonic Tuning

As mentioned, higher efficiency can be achieved by reducing the time in which both voltage and current exist at the collector. This cannot be done by reducing the interval of current flow without encountering the low output power difficulties of class C operation. Raab (*1*) has coined the name class F operation for one very different approach. In class F, rather than reducing the current-voltage product by decreasing the duration of current or voltage pulses, circuitry is used which gives one waveform or the other a new shape. In the class B amp a roughly half sinusoidal current and fully sinusoidal voltage is established (fig 1.3.3). The product of these is zero when no current flows, but is positive through the conduction interval except where the voltage approaches zero. Because of the collector-emitter saturation voltage the collector does not reach zero. For minimum power dissipation these waveforms are not ideal.

When the frequency of operation is much lower than the reciprocal of the transistor switching times the transistor may be operated as a switch rather than an amplifier. Instead of a sinusoidal voltage the collector voltage will then resemble a rectangular wave, as shown in fig 1.4.1. The collector voltage is now close to zero when the current is high and the current is zero whenever the voltage is high. The power dissipated in the transistor is considerably reduced, directly raising the efficiency.

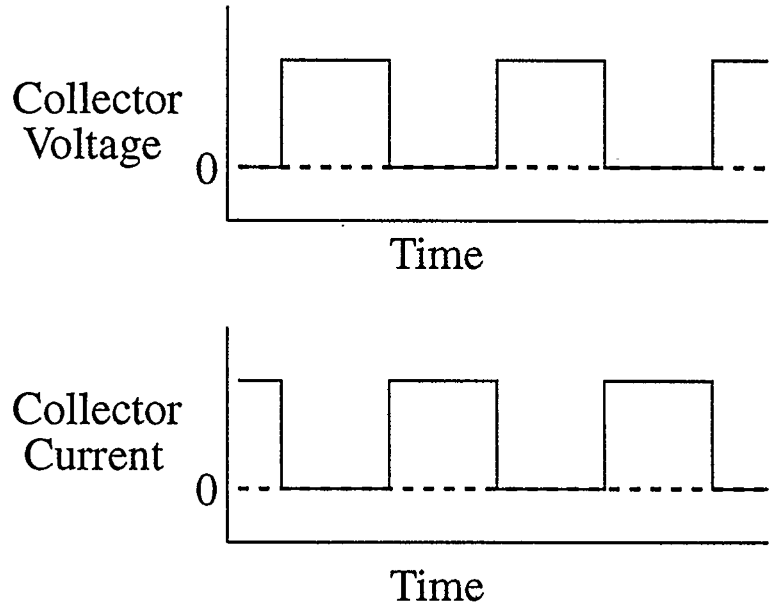


Figure 1.4.1 Ideal Switching Waveforms

Unfortunately, this mode of operation is not easy to achieve at higher frequencies due to transistor switching speed limits; a transistor with unnecessarily high frequency performance and cost would be called for. Also, since both voltage and current are present in the square wave, harmonic output power is generated. In most applications this harmonic power is not desired and it must be removed, reducing the overall efficiency and requiring filters.

Class F amplification changes the collector waveforms without requiring extremely short switching times. It does this by terminating the different output harmonics in different impedances. As a result some of the output harmonics are reflected back into the collector by the harmonic impedance mismatches. If reflected with the correct phase, these harmonics will change the net collector voltage and current shapes. Raab built a circuit of this type for testing at 25 MHz (4) while Kazimierczuk (2) designs and evaluates a conjugate circuit. Glazman et al. (5) investigated the effect of using the second or third harmonic separately.

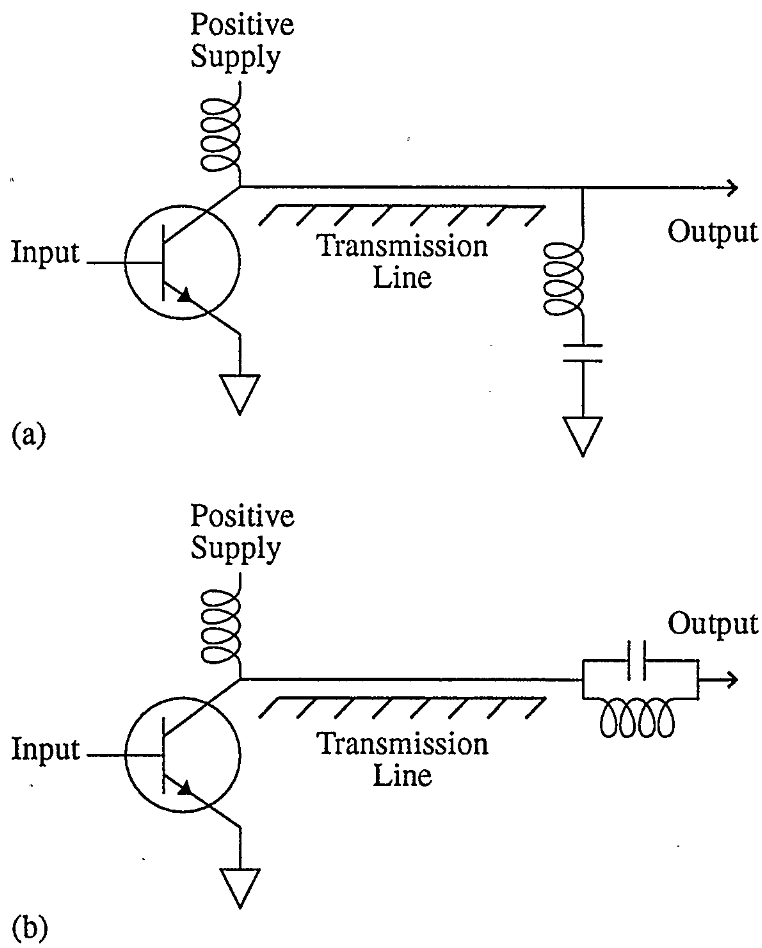
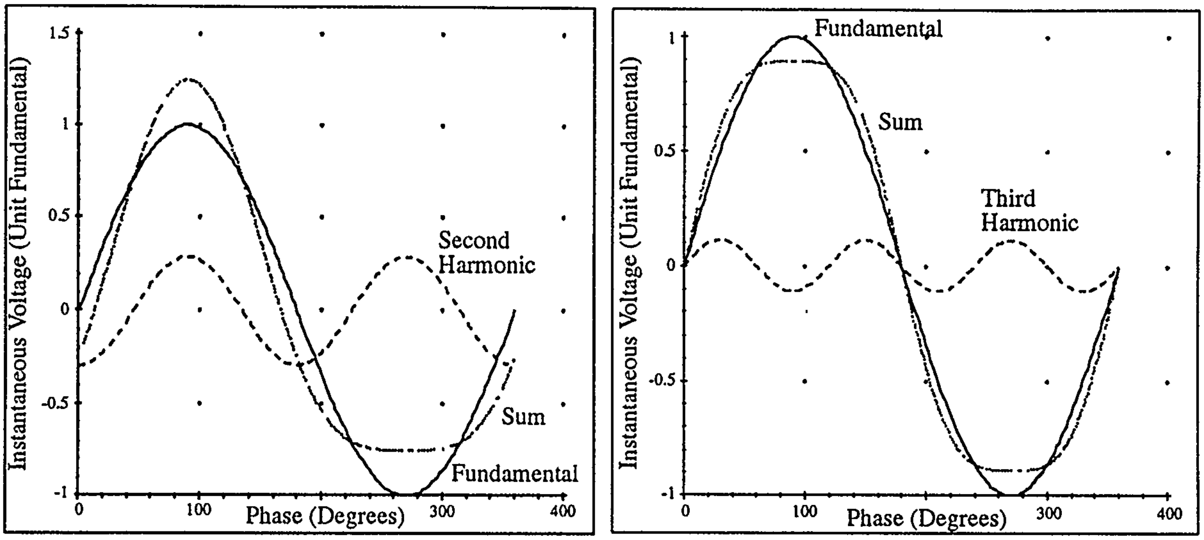


Figure 1.4.2 General Class F Amplifiers

As shown in fig 1.4.2 a generalized class F amplifier consists of an active amplifying device, a length of transmission line and a harmonic filter element. The filter may be relatively low Q, as it is required to work with octave frequency separations; a low Q will allow more broadband operation of the tuned amplifier.

All class F modes of operation can be viewed in two ways. As seen in fig 1.4.2a, the fundamental signal passes across the filter without effect while the filter acts as a short circuit to ground for one of the harmonic distortion signals. In that case the harmonic voltage and current will be reflected back towards the active device. The length of the transmission line between the transistor and the filter controls the phase with which the harmonic is reflected back to the collector. In fig 1.4.2b the parallel tuned filter will reflect one harmonic, while passing the remaining signal components. With proper frequency selection series resonant filters may be substituted for parallel, and vice versa, to tune a single harmonic. Fig 1.4.3 shows the waveforms in Glazman's (5) ideal use of the second or the third harmonic based on such a system.

The second approach is less intuitive and is based on the magnitude and phase of the reflection coefficient presented to the harmonics at the collector by the transmission line and filter, while the fundamental should see a low reflection coefficient. While these views are equivalent, the first may allow for better understanding of the circuit operation.



(A) Second Harmonic Tuned

(B) Third Harmonic Tuned

Figure 1.4.3 Glazman (5) Collector Waveforms

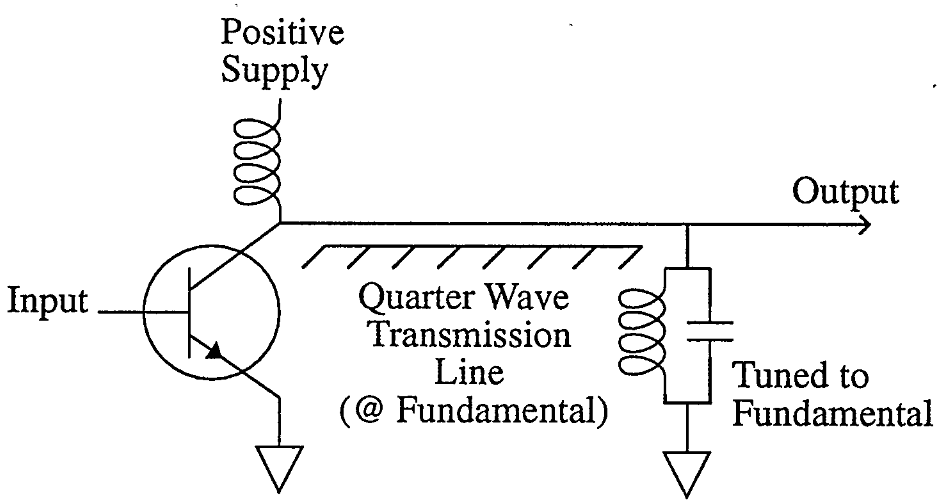


Figure 1.4.4 Raab's Class F Amplifier (1, 4)

Raab's method of harmonic tuning is an extension of this basic idea (fig 1.4.4). Because the Fourier decomposition of a square wave consists of a fundamental signal and all the odd harmonics, it uses a combination of a transmission line and a filter to recompose a square wave voltage at the collector, assuming that suitable harmonic levels are present in the output at the collector. This recomposition requires that the collector be presented with a high impedance for all the odd harmonics, and a low impedance to ground all the even harmonics. While there will be significant odd harmonic voltage levels, if the odd harmonic impedance is high enough there will be little odd harmonic current and low power loss. Similarly, if the even harmonics are grounded well there will be little even harmonic voltage. The only frequency at which both current and voltage coexist on the collector is the fundamental output. While such a circuit could be built using a large number of filters, one for each harmonic, this would likely be lossy, large and expensive. Raab's elegant solution was to connect the collector to a filter by a line one quarter of a fundamental wavelength long. The filter was a parallel inductor capacitor pair shunting the signal path to ground; it was tuned to the fundamental frequency. As the shunt filter is a parallel LC combination, the fundamental signal sees it as a very high impedance shunt, and passes over it with little loss. For a filter of reasonable Q all the harmonics are shunted to ground at the filter. The quarter wave line is what allows this system to work; for the second and all even harmonics the line is a whole multiple of one half wavelength, so that all even harmonics are directly grounded at the collector. All the odd harmonics see the line as an odd multiple of one quarter wavelength, an effective open circuit at the collector.

While this system seems promising, some problems with it are expected. These are discussed in Chapter 2.

CHAPTER TWO

PRACTICAL WAVEFORMS

2.1 Practical Waveforms Introduction

There are many collector waveform combinations which theoretically ensure higher collector efficiency. One of the most appealing, Raab's quarter wave line-tuned circuit, should even yield 100% theoretical efficiency. In practice, rather less is expected because at higher frequencies an economically selected transistor will not have sufficient harmonic output to allow recomposition of a square wave collector voltage. To ensure that switching is rapid, Raab recommends that the amplified frequency should not exceed one tenth of the transistor gain bandwidth, thereby requiring more expensive devices. Either the transistor will not be fast enough to generate the harmonics or they may be trapped within it by the case and lead parasitic reactances. Whatever the reason, the higher the harmonic the less likely it is to be present in useful quantities in the output. Also, the harmonics need to be recombined with the correct phase. If they are not launched from the transistor in phase or travel along a dispersive transmission line they will not recombine correctly. While a very neat system, it has little flexibility in tuning the harmonic phases separately.

A simpler technique with somewhat lower ideal performance using only the second or third harmonic has been described by Glazman and others (2, 5, 14). Either harmonic can flatten the collector voltage during current pulses, but not for more than 90 or 60 degrees, respectively. As both of these signals are more likely to escape a transistor than the higher harmonics (13), the beneficial effects of an optimal combination of the fundamental, second and third harmonic is investigated.

2.2 Combining the Second and Third Harmonics

Since efficiency can be raised by both the odd second harmonic and the even third (even and odd with respect to symmetry), it seemed likely that the two could be combined for even greater performance. The chief problem was how to find the best amplitude and phase of the harmonics relative to a unit amplitude zero phase sinusoidal fundamental collector voltage . It is assumed that the voltage waveform should be symmetric about the collector current peak at 270 degrees. Neglecting the DC supply voltage and normalizing the fundamental to unity, this yields a collector voltage

$$v_C(t) = \sin(\omega t) + k \sin(2\omega t + 2\phi) + m \sin(3\omega t)$$
$$= \sin(\omega t) + k \cos(2\omega t) + m \sin(3\omega t)$$

where k = second harmonic amplitude

m = third harmonic amplitude

ϕ = phase of second harmonic, $-\pi/4$

The difficulties faced in solving for the best harmonic amplitudes, k and m, are that both the largest possible interval of collector voltage flatness and the most negative point of the flattened waveform are not known. As the best flat voltage level is not known, it is not possible to adjust k and m to flatten the waveform to some specific level.

To resolve these unknowns it was decided to flatten the waveform by minimizing the mean square of its slope over as wide an interval as possible. It was expected that the flat interval would be less than one half cycle or 180 degrees. The harmonic amplitudes were to be optimized such that the slope outside the flat region is as steep as possible. The interface between the steep and shallow region was taken to be where the steep mean square slope was ten times that of the flat region. This was followed by a trial and error routine which was allowed a limited number of attempts, followed by a return to the slope interface routine. After a reasonably flat waveform was achieved the trial and error code was replaced by a Newton-Raphson iteration solution for best flatness. During this work it was found that the flattened region could be a full 180 degrees wide. This leads to both high efficiency and easier solution, as the iterations for maximum slope interfered with the shallow region optimization. To ensure reliable convergence double precision values were required. This was necessary because the iteration was used to find a zero (root) in the first derivative of the slope function with respect to the harmonic amplitudes. Both the first and second derivatives were approximated numerically and thus sensitive to precision limits.

This tuning method is expected to outperform that of Glazman et al. which only uses one of the harmonics. At higher frequencies it should also exceed Raab's odd harmonic tuning for the reasons already given.

In their paper, Glazman et al. do not consider actual realizable efficiency. Instead, they compare efficiencies assuming an absolutely flat, rectangular current pulse. Under that condition collector efficiency is dependent only on the voltage waveform shape; the higher the fundamental output for a given supply voltage the higher the relative efficiency.

$$\text{relative efficiency} = \frac{\eta_{tuned}}{\eta_{untuned}} = \frac{V_{1tuned}/V_{cctuned}}{V_{1untuned}/V_{ccuntuned}}$$

For equivalent (or normalized) fundamental output levels,

$$\text{relative efficiency} = \frac{V_{ccuntuned}}{V_{cctuned}}.$$

If the untuned amplifier has output peaks of the same amplitude as the supply,

$$\text{relative efficiency} = \frac{V_{1tuned}}{V_{cc}}$$

Table 2.2.1 is generated using this last relationship; the untuned amplifier efficiency is that of an ideal class B circuit.

Table 2.2.1 Relative Harmonic Amplitudes for High Efficiency Modes

Tuning Method	Relative Efficiency (Glazman)	Second Harmonic Amplitude, k	Third Harmonic Amplitude, m
Untuned	1.000	0.	0.
Glazman 3rd Harmonic	1.13	0.	0.11
Glazman 2nd Harmonic	1.390	0.293	0.
Maximally Flat 2nd & 3rd Harmonic	1.609	0.573053	-0.194569
Maximally Efficient 2nd & 3rd Harmonic	1.580	0.473011	-0.106140

By their approach, Glazman et al. overestimate relative efficiency. In waveforms with two negative peaks rather that one rounded minimum at the current pulse peak (fig 1.3.3) they consider the required supply voltage to be the negative excursion at the current midpoint rather that at the actual negative extreme. A relative efficiency of 1.41 is claimed for conditions which really yield 1.39, for example. The difference is more significant in realistic efficiency calculations where a constant current pulse may not be assumed, as described below.

While useful as a simple means of comparing circuit efficiency the assumed flat current pulse does not occur in real devices. A more probable current pulse is a half sinusoidal one (18) or, alternately, a raised cosine (sine squared) pulse. While the flat current pulse will be most efficient with an equiripple, maximally flat voltage during the current flow, this is not the general case. The half sinusoid (or similar) pulse will be more efficient with a voltage customized to it for best performance. In more direct terms, the current pulse starts and ends at a low value, rising to and falling from some peak level. For best performance the collector voltage can be a higher level at the start and stop times if this will allow a flatter voltage around the higher current points.

To allow comparison of actual realizable efficiencies an expression was derived for actual collector efficiency based on a half sinusoidal current pulse (18). A raised cosine pulse should give similar results. If the harmonic load impedances are large relative to that of the fundamental the harmonics will not affect the current shape or detract from efficiency. If this is not true the use of harmonics will reduce efficiency from optimum; for reasonable design there will still be improved performance.

Neglecting saturation voltages, for a 180 degree duty cycle,

$$\eta_c = \frac{\frac{\pi}{4} - \frac{k(1 + R_{112})}{3} + \frac{3mk(R_{112} + R_{113})}{5} + \frac{\pi(k^2R_{112} + m^2R_{113})}{4}}{V_{cc}(1 + \frac{mR_{113}}{3})}$$

$$\text{where } V_{cc} = \begin{array}{c}\text{greater}\\ \text{of}\end{array}\begin{cases} 1 - k - m \\ -a + k\cos(2\arcsin(a)) - m\sin(3\arcsin(a)) \end{cases}$$

$$\text{and} \qquad a = \frac{k - \sqrt{k^2 + 9m^2 + 3m}}{6m}$$

$$R_{112} = \frac{\text{fundamental load resistance}}{\text{second harmonic load resistance}}$$

$$R_{113} = \frac{\text{fundamental load resistance}}{\text{third harmonic load resistance}}$$

This equation was used to generate table 2.2.2, comparing different harmonic levels in tuned amplifier operation.

Using Newton's method to maximize efficiency in two dimensions, the harmonic amplitudes, is effective only if the initial approximations are close to the best solution. Newton's method based on the original maximal flatness coefficients leads toward a best operating point of 97.3% collector efficiency. While this was a substantial improvement over any other mode of operation, an even better operating condition was hidden. It was found through simulated annealing, another numerical optimization method (6). A simulated annealing program using the efficiency equation as an error function found second and third harmonic coefficients yielding an efficiency of 99.14%. These coefficients were revised using the Newton's approach to provide up to 99.15% collector efficiency over a broad range of harmonic load impedance levels. The harmonic power levels needed are also lower than those for the 97.3% point, making successful implementation even more practical. The resulting waveforms are shown in fig 2.2.1.

Table 2.2.2 Collector Efficiency & Supply Voltage for Several High Efficiency Modes

Tuning Method	Collector Efficiency	Supply Voltage for Unity Peak Output	Relative Efficiency (Glazman)
Untuned	.785	1.000	1.000
Glazman 3rd Harmonic	.8914	0.8897	1.124
Glazman 2nd Harmonic	.9557	0.7194	1.390
Maximally Flat	.9563	0.6215	1.609
Maximum Efficiency	.9915	0.6329	1.580

The actual collector current pulse is not likely to be an exact half sinusoid as assumed for this efficiency maximization. Nevertheless, the harmonic levels suggested as yielding the highest efficiency should still result in high efficiency; for an economical transistor the rise times are not expected to be sharp enough to result in unreasonable power loss at the non flat edges of the voltage waveform. If a radically different current pulse shape was expected a new collector efficiency equation should be derived for it and optimal harmonic levels selected accordingly.

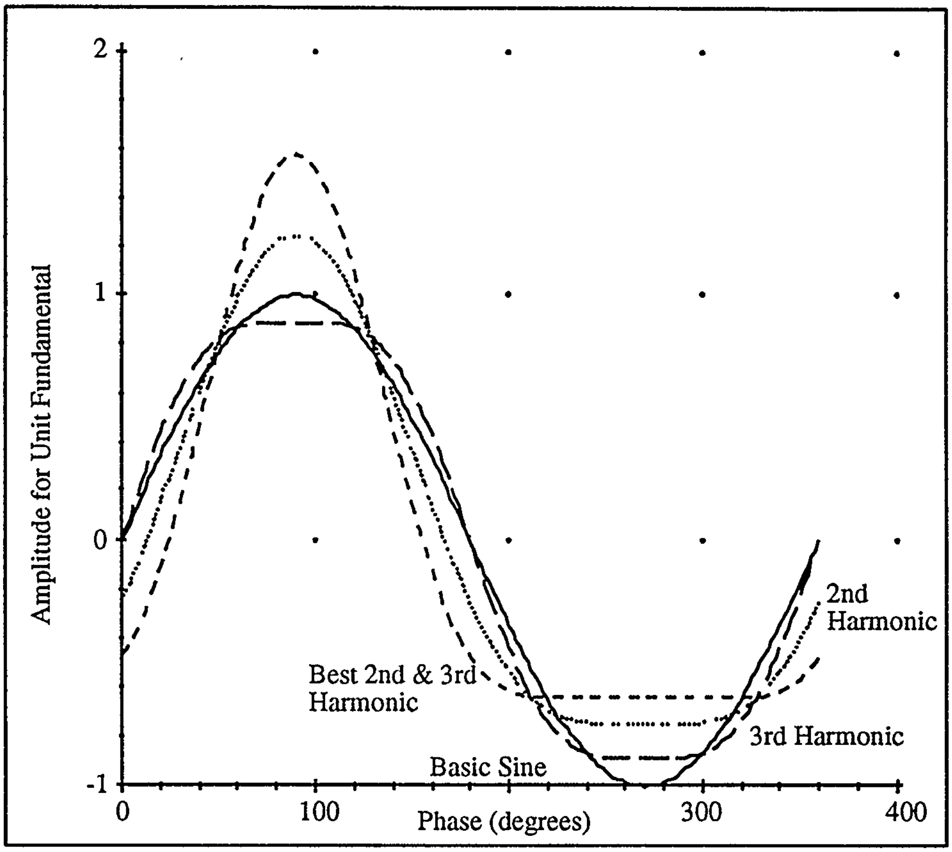


Figure 2.2.1 High Efficiency Collector Waveforms

2.3 Effect of Harmonic Tuning on Supply Requirements

As well as raising amplifier efficiency, harmonic tuning will allow lower voltage supplies to provide higher output power. This may be seen in consideration of the waveforms in fig 2.2.1. The supply voltage required for unity peak output voltage is the voltage between the zero line and the most negative excursion of a given waveform, neglecting saturation voltages and device resistance. This information is given in table 2.2.2. While an untuned amplifier would require a 1 volt dc supply to drive a 1 volt peak output, using the second harmonic for enhanced efficiency lowers this to 0.72 volts. The highest efficiency combination of the second and third harmonics would require only 0.63 volts for the same output level. This allows the use of lower voltage supplies, higher output power levels or the option of raising the effective output impedance of the transistor, reducing the need for matching circuitry. While the maximally flat harmonic combination has an even lower dc supply requirement this is not expected to be useful. The actual difference is slight, under 2%, and the flat waveform requires considerably higher harmonic levels. Most important, it has a significantly lower collector efficiency.

Reducing the supply voltage requirement promises to be of value at both extremes of power amplifier use. Cellular hand held sets could use smaller or simpler batteries, while large, high power transmitters would also need lower voltage supplies.

CHAPTER THREE

EQUIPMENT

3.1 Amplifier Circuits

Early experimental work was done using a two stage 35 Watt amplifier. While this amplifier worked fairly well it was not the best unit for the desired research. First, it required relatively expensive transistors which had a frequent habit of failure due to overheating in spite of massive heat sinks, fuses, overcurrent sensing bias removal circuits and manual current metering. A fairly simple design, it also had many approximate value straight line inductors which were tuned by variable capacitors for peak operation. While this allowed operation over a reasonable band with retuning, the capacitor-inductor combinations resulted in narrow band operation. The transistor employed was also ill suited to the research. Not only was it expensive, it was only characterized from 400 to 525 MHz in the manufacturer's data (8). It is quite likely that its output of harmonics of 400 MHz would be reduced by parasitics and may easily have been at an impedance very poorly matched to the output connection by the narrowband match circuitry employed. When a parallel output port tuned for the harmonics failed to allow easy and effective harmonic tuning, a replacement circuit to overcome these problems was needed. A schematic of the first amplifier in its final form is presented in fig 3.1.1.

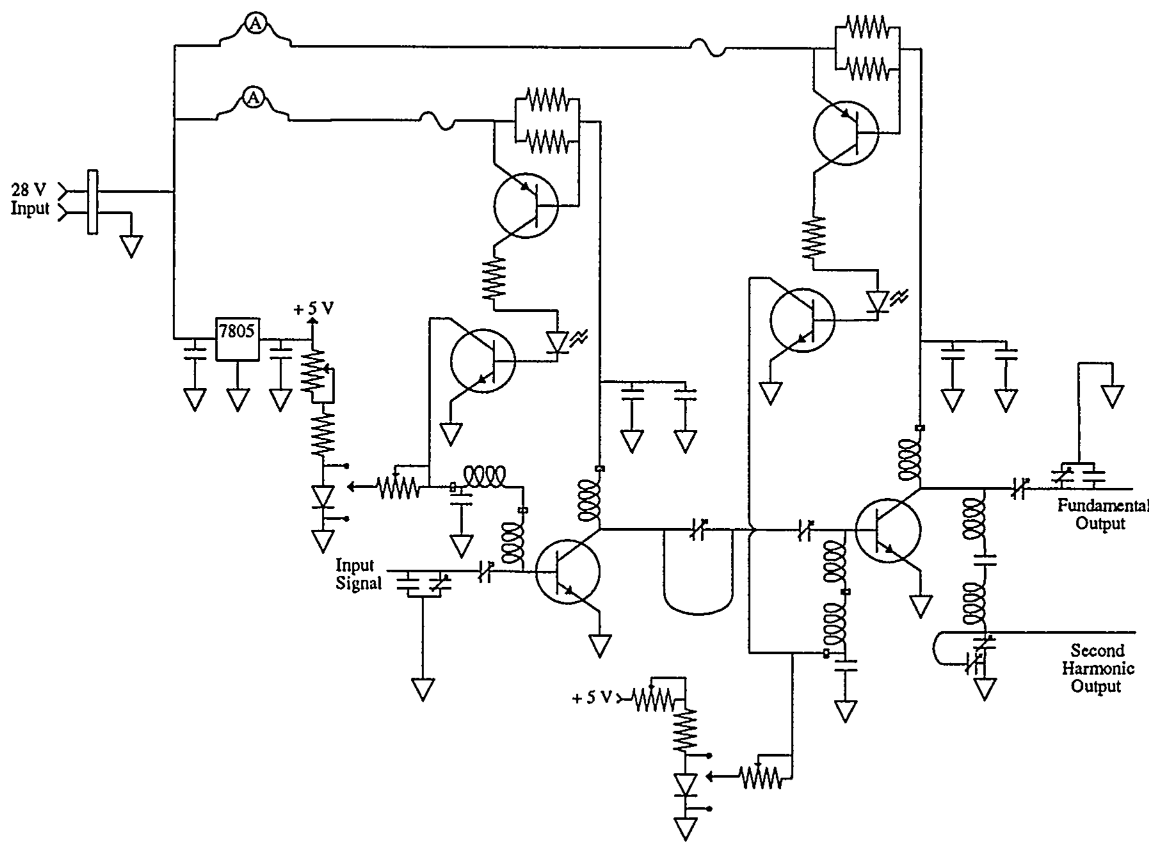
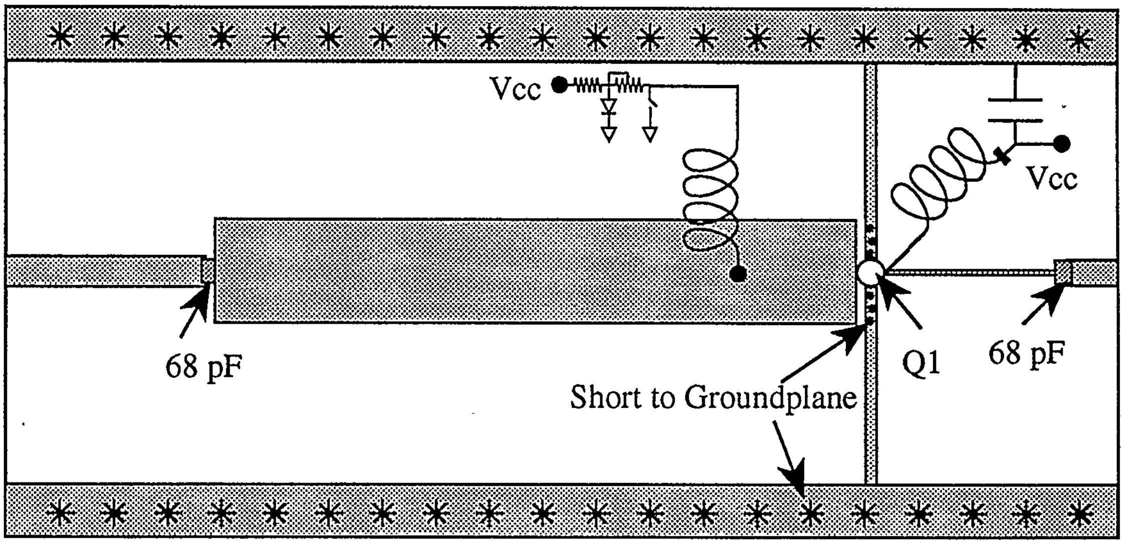


Figure 3.1.1 The First Amplifier

The problems described above were removed by the design and construction of a new power amplifier (8, 10-12). The output power requirement was lowered to 500 mW both for convenience and so as to follow the needs of hand held transceivers. This allowed the use of much lower cost devices which were readily available. A simple, rough amplifier design was optimized using Touchstone RF for very broadband performance with no retuning; this was made easier by the reported device specifications which covered both the 400-500 MHz and the 800-900 MHz ranges. Conveniently, the transistors were specified to have a large signal output impedance fairly close to 50 Ohms, reducing the need for matching circuitry (8).

This simplified the design, as matching circuits which work well for both the fundamental and the harmonics are not necessarily easy to design or build. This amplifier is shown in detail in fig 3.1.2.



G-10 board 1/16 inch thick Microstrip (reduced scale)

Figure 3.1.2 Broadband Amplifier

3.2 <u>Harmonic Tuning Circuits</u>

A simple and intuitive system of harmonic separation and reflection was tried first. This centered on a five port filter built by Dr. R. H. Johnston. The filter was a four frequency multiplexer with one common port and four helical resonator outputs, tuned for 400, 800, 1200 and 1600 MHz.

As shown in fig 3.2.1 the transistor output was to be fed into the common port. The fundamental output was to be extracted at the 400 MHz port, and variable length short circuit stubs provide independent control of the phase at which the harmonics would be returned to the collector.

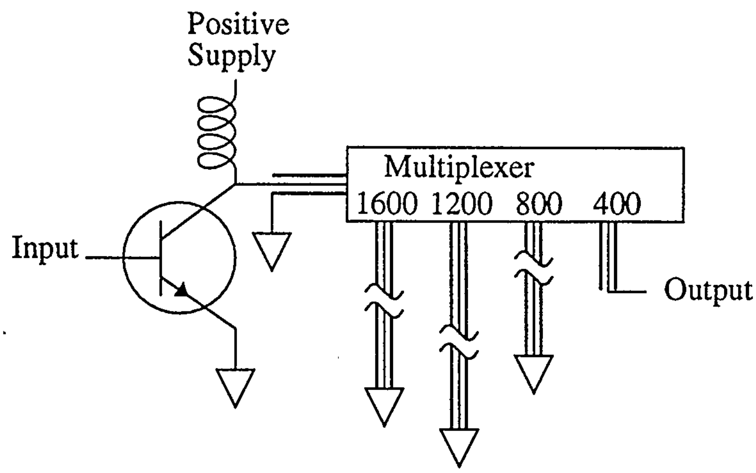


Figure 3.2.1 Multiplexer Harmonic Tuning

For more flexibility at least one more multiplexer was desired. While another resonator filter could have been built it was desirable to avoid the time and metal machining required. Several microstrip and microstrip-inductor-capacitor multiplexers were designed and optimized with Touchstone RF. Both of the four frequency designs attempted optimized slowly but had a good predicted performance that failed completely in the physical units that were constructed. Losses were extremely high, though frequency selectivity was adequate.

A two frequency multiplexer was optimized much more quickly and had quite acceptable performance. It is shown in fig 3.2.2, while its measured performance is given in table 3.2.1. Harmonic tuning was achieved through adjustable short circuit stubs as in fig 3.2.1.

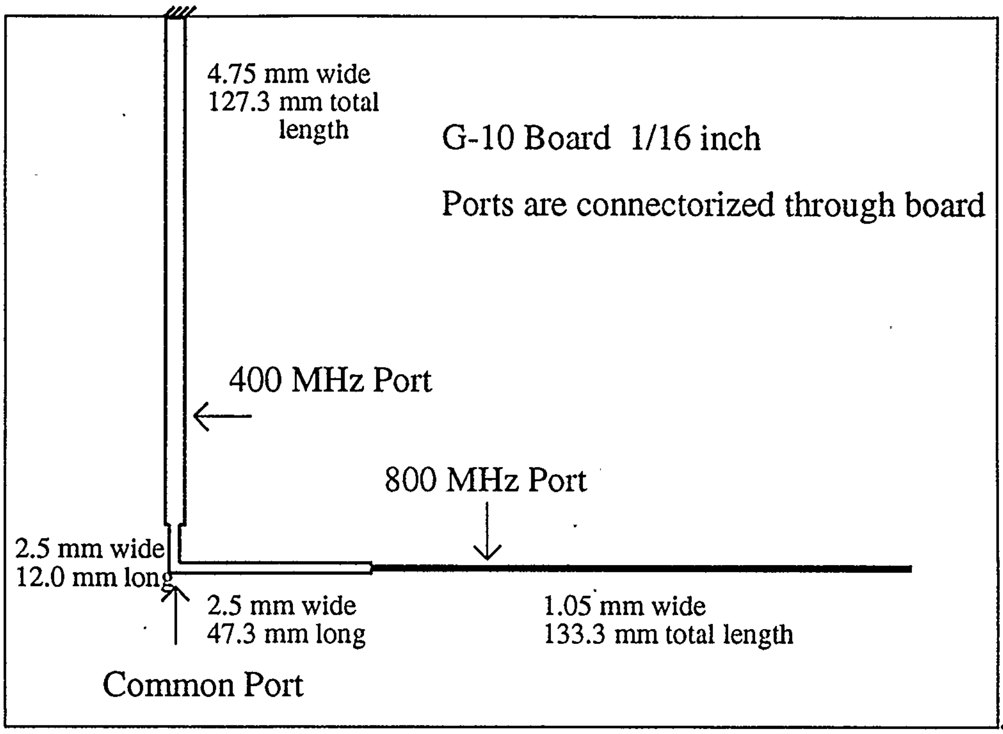


Figure 3.2.2 Microstrip Multiplexer

Table 3.2.1 Three Port Multiplexer Measured Performance

Port Frequency (MHz)	Test Frequency (MHz)	Loss with 50 Ohm termination (dB)	Loss with unused port open circuit (dB)
400	400	0.3	0.2
	800	29.5	27.0
800	400	27.5	24.0
	800	0.6	0.6

Glazman, Raab and others used a combination of transmission lines and inductor-capacitor filters in their work. To assess the operation of their designs several adjustable second order filters and transmission lines were built. While at lower frequencies an LC filter can easily be built and connected to a transmission line this ease does not exist at 400 MHz. To avoid building oversized tubing coaxial lines and inserting filters into them, series and parallel tuned LC resonant circuits were made by cutting off the side connector of BNC Tee connectors, leaving the center pin of the side tap in place. This allowed series or parallel tuned filters between the center conductor and shield with minimal lead length and parasitics. A variable air dielectric capacitor and a small single wire loop comprised adequate series resonant filters at 800 and 1200 MHz and parallel resonant filters at 400 MHz. Higher frequencies could not be accommodated without some change in approach as the required inductor size would become too small. Using the variable capacitor these filters were easily retuned over a broad frequency range. An inline LC filter was not required, as circuits using these (eg Kazimierczuk, 2) are conjugate cases of the shunt style circuits and are not expected to perform as well in the present experiments; fundamental signal loss is expected to be higher in harmonic rejection filters that the fundamental signal passes through. When the fundamental travels along a transmission line shunted by a harmonic filter it will experience less of an impedance mismatch than when passing through a readily built series filter. With industrial quality filters this should be less of a problem.

Variable length transmission lines are also required for use with the filters. Such lines are difficult to build in microstrip, and an unbalanced line was desired. While a variable length trombone line was available it was far too long for use at 400 MHz, and the time and expense required to find and buy a line stretcher suggested that copper pipe was found to exhibit usable performance three excellent lines were made from thin brass tubing. This tubing is available in a range of sizes that all nest snugly, allowing straightforward construction of telescoping coaxial segments. The tubing is thin enough that the coaxial radii in overlapping and non-overlapping regions are both close to those required for a 50 Ohm characteristic impedance. As these lines use air as the dielectric they have better adjustment resolution than a higher dielectric line would. They should not contribute to phase dispersion between the fundamental and harmonics, though the microstrip segments in the amplifier may.

3.3 Measurement System

Early in the work the only measurements taken were the input and output signal strength, measured with directional couplers and Hewlett Packard RF power meters. To protect the transistors and allow efficiency calculations the collector current was measured, using analog Avometers. Such a system worked well for measuring gain, input power and output power but was rather limited in tuning for maximum efficiency. When harmonic tuning was added to the basic amplifier it was easy to tune the circuit for maximum output, minimum input power or minimum collector current. Unfortunately, it was rapidly found that the highest efficiency operating point was not at one of these extremes. Tuning the harmonic circuits normally involved adjusting both the length of an adjustable coaxial line and the position of a variable capacitor. It was extremely difficult to do this for peak efficiency or PAE when each slight adjustment required at least four measurements, a string of calculations (programmed), recording the results of the calculations and only then deciding whether or not the slight adjustment had a positive or negative effect. No simple way of directly measuring efficiency was available. Two possible solutions were seen.

First, an analog processing solution was considered; the RF power meters both have a proportional DC output that can be used to drive a plotter. Given several logarithmic converters and subtraction analog building blocks an analog efficiency or PAE output could have been generated. Several problems with this approach resulted in its rejection; the power meters changed output levels for each sensitivity range and the required signal processing blocks were not available. The analog system would also be less flexible for other kinds of measurement or calculation.

The second solution seemed possible when it was noted that one of the power meters had an IEEE 488 bus port. The IEEE 488 bus is also known as the GPIB, general purpose interface bus, or the HPIB, Hewlett Packard interface bus; it is a fast parallel bus scheme used on some modern test equipment. GPIB voltmeters were readily available, and an expedient current shunt converted one into an ammeter for measuring collector current. The only additional expense encountered was in upgrading the other RF power meter which lacked the GPIB option (now an included feature on new meters). With one power meter and ammeter the collector efficiency measurement was automated for fixed levels of supply voltage. With both power meters and a voltmeter properly interfaced the system power dissipated in the transistor. Having an on-line report of power dissipation has prevented further transistor burnout since the measurement system was implemented. This is a significant saving in both time and cost and a relief during data acquisition, removing the concern as to device condition.

Soon after the system described above was assembled, it was decided to add a supply voltage measurement capability. This removed a slight source of error in that the current shunt used by the ammeter fractionally reduced the actual supply voltage to the collector terminal. This also allowed the supply voltage to be varied while the circuit measurements were reported accurately. Harmonic tuning can only yield reasonable efficiency if the collector voltage swing is an appreciable percentage of the supply voltage. As the transistor in use was a fairly low power device, the output swing could not be raised by increasing the input power without limit; the solution was to lower the supply voltage. Another advantage was that the voltage measurement was both easier, more rapid and more repeatable than the input power adjustment. The complete system is diagrammed in fig 3.3.1.

An IBM PC was considered and rejected as the controller for the GPIB equipment described above. Such a machine would have needed an additional IEEE 488 controller card; there was also no excess of such computers available. An excellent machine for the job turned out to be a somewhat dated Commodore business computer which used the GPIB as its primary input/output system. Communicating with the voltmeters and power meters was therefore faster than the power meters, which must wait for up to ten seconds for low power measurements to stabilize. Such computers are very economical, and may be considered when a dedicated GPIB controller is required.

In its final form the measurement system reports gain in dB, input and output power in both dBm and milliWatts and actual supply voltage. Collector efficiency, power added efficiency and total transistor power dissipation are given both numerically and as horizontal bar charts. While the power meter response time limits the usefulness of the bar charts as an aid to tuning, the visual power dissipation warning has proven quite useful.

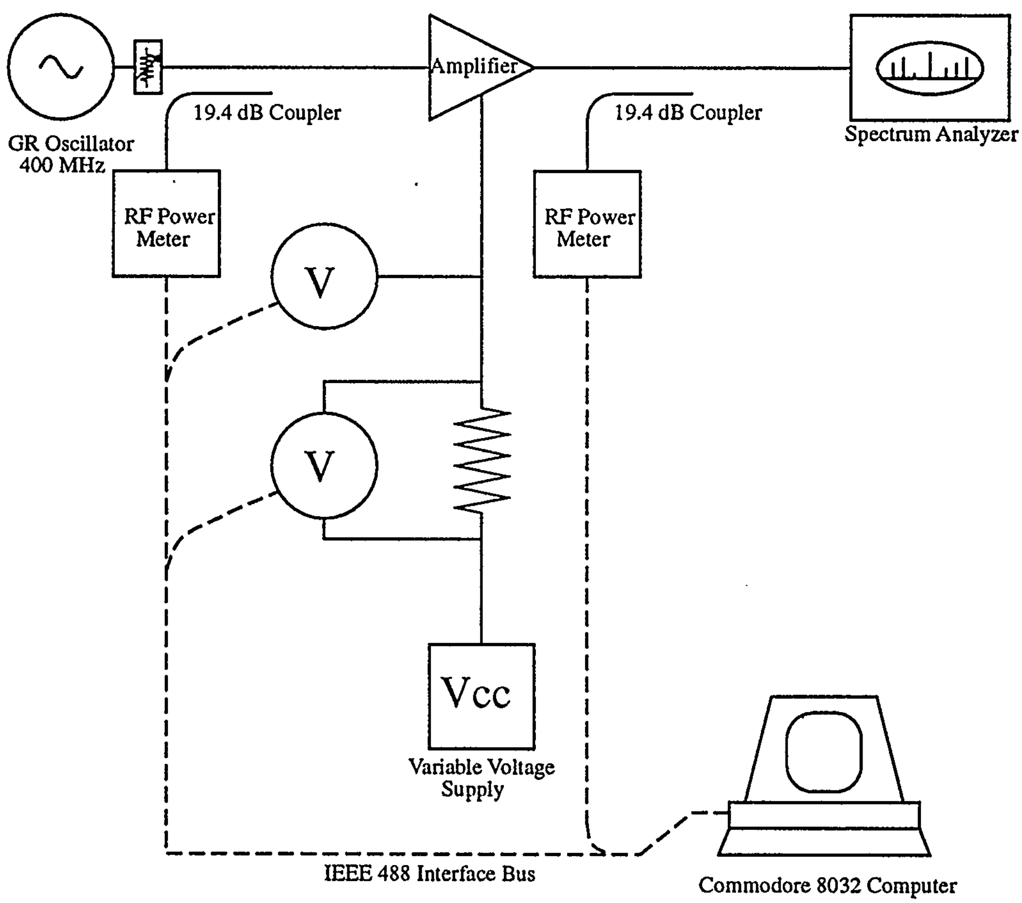


Figure 3.3.1 Automated Measurement System

It was found that an attenuator was required following the General Radio oscillator. Without this attenuation high harmonic levels existed along the circuit between the oscillator and the transistor base junction; this was due to the signal generator's non ideal match to the 50 Ohm line and the harmonic power generated in the base-emitter junction. High attenuation levels were compensated for by higher oscillator output signals, limited only by the generator's peak output.

Table 3.3.1 Input Line Suppression of Undesired Harmonics

Approximate Attenuation (dB)	Supply Voltage	Forward Power (dBm)		Reverse Power (dBm)	
		400 MHz	800 MHz	400 MHz	800 MHz
0	5.00	18.7	11.2	13.4	12.9
0	7.00	18.4	11.2	12.4	11.9
3.7	5.00	18.7	-0.8	14.4	7.4
3.7	7.00	18.7	-1.3	13.9	7.4
8.2	5.00	18.2	-9.8	13.9	7.4
8.2	7.00	18.7	-9.8	14.4	7.4
8.2	9.00	18.7	-10.3	14.4	7.4

While the data taken without the attenuator are valid they are limited to a system with similar input conditions; the system using the attenuator is much more easily reproduced. Table 3.3.1 indicates the significance of the attenuation. It may be seen that the attenuator allowed considerable suppression of the second harmonic power directed towards the base and that further suppression (the 8.2 dB level as opposed to the 3.7 dB) did not further affect the reverse harmonic power from the base, indicating that the reduction was sufficient.

3.4 Simulation With PSpice

Much of the electrical action in an RF circuit is difficult or impossible to measure. This is especially true when measurements of interest would have to be taken inside an operating component such as a transistor. For instance, while it is not impossible to open a transistor case and apply probes directly to the chip junctions inside it is somewhat difficult. Even such intricate measurements as these would not reveal what was happening inside the intrinsic device. At high frequencies the results of such measurements may also be unreliable, due to low impedance probes and dispersion along any transmission lines employed. Computer simulation may be used to good effect, in that any waveform anywhere in the simulated circuit may be measured and manipulated easily. For useful results the only requirement is that the simulated circuit reflect the real one fairly closely.

For this research the student version of PSpice (MicroSim) has proven useful (9). While SPICE itself could have been run rapidly on available SUN systems the PC or Macintosh based PSpice was superior because of its extensive graphical post processor, PROBE. Using PROBE on a set of simulation results allowed the easy examination, measurement and manipulation of most current or algebraically manipulated, Fourier transformed and averaged. This allowed an appreciation of actual amplifier operation that could not have been obtained otherwise.

Student PSpice is somewhat less powerful than the industrial versions. Its chief limitations are in speed and the maximum number of active devices allowed. The speed limitation was tedious but workable; long simulations could take ten minutes to run on the fastest platform available. Whenever possible fewer complete cycles were simulated, decreasing the time required. Because the present work required that a simple single transistor be simulated with great accuracy, the ten device limitation caused no problem at all. Student PSpice is a remarkably powerful public domain program.

In order to obtain reasonable data from a simulation program like SPICE a large number of transistor model parameters had to be approximated. The transistor chosen, the Motorola MRF559 was selected partly because of the detailed information made available by Motorola. Unfortunately this data was with regard to small signal scattering parameters and large signal impedance levels, rather than as direct equivalent circuit values. While the SPICE default parameters may work well for modeling a transistor at low frequencies, this was not the case in the present work at 400 MHz. Whenever practical the parameters of several typical transistors were actually measured. This was achieved for dc beta (forward current gain), junction capacitance, emitter and collector resistance and the junction diode parameters of the Shockley equation (7, 8). The remaining parameters were approximated through the use of

Touchstone RF, a microwave simulation program made by EESOF. Touchstone can be used to model linear (small signal) transistors and has a powerful optimization capability. The optimizer was used to fit a hybrid pi model to the Motorola S parameters over a broad range of frequency and current levels. Whenever a standard model current dependency was expected the optimized model was checked as to whether it fit the trend. Several other possible parameter trends with current were also investigated to check for possible interactions. All the model parameters and how they were approximated are summarized in Appendix 1.

The base, emitter and collector inductances are not part of the PSpice model. They are included outside the device because they affect the transistor model significantly at 400 MHz and above.

The transistor model used initially is shown in fig. 3.4.1. The Touchstone optimizer was given freedom to vary all of the parameters shown in the figure. Optimization was performed targeting S parameters at 250, 500, 1000 and 1500 MHz for a single current level. After random and gradient optimizations settled to a minimum error the equivalent circuit values were recorded and a new optimization started for the S parameters at a different current level, from 10 to 150 mA.

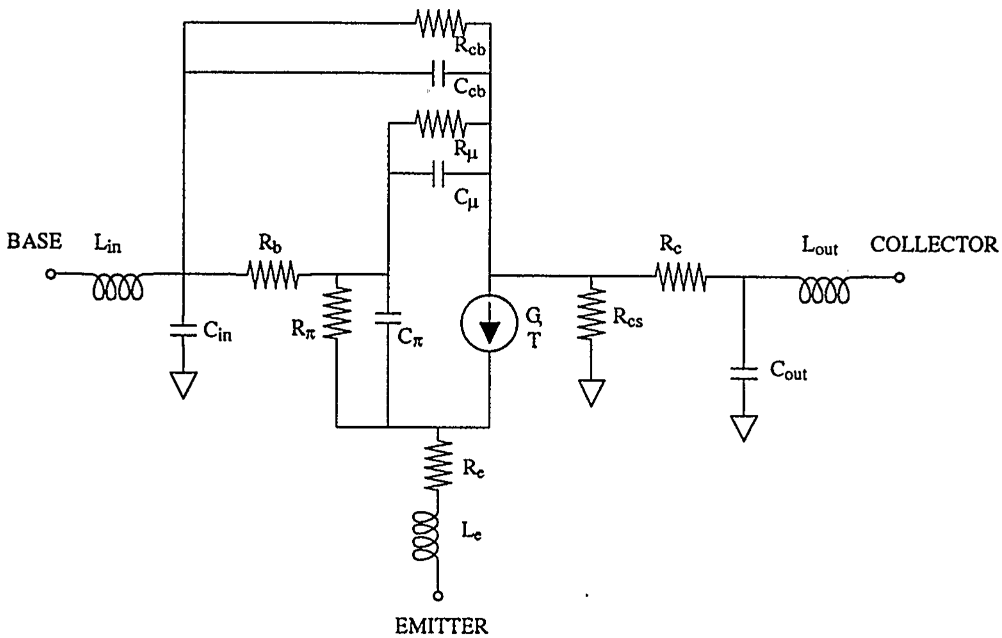


Figure 3.4.1 Complex Transistor Model

While this approach did yield transistor models that fit the scattering parameter data there were several problems, all stemming from the excessive flexibility of the model. The model allows some aspects of transistor performance to be accounted for in several ways. As an example, one of the most obvious is the possible relationship between the collector to base feedback resistance and capacitance inside and outside the base spreading resistance R_b. If R_b is small and the shunt reactances and resistances are large then the optimization algorithm will not be able to select unique, correct values for the shunt capacitances and resistances as these are effectively connected in parallel. In the same way, transit time can be ascribed to base-emitter capacitance C_π, which includes diffusion capacitance, or to a separate forward transit time parameter. Less obvious interactions between other elements caused successive optimization runs with the same start points and goals to converge to radically different equivalent circuit values. Some of the values did not change significantly between runs and were recorded directly as being reliable. Referring to the figure, these included L_{in}, R_e, L_e and to a lesser extent L_{out}, R_{cs}, R_μ and C_π. The remainder had some extreme differences between runs, often several orders of magnitude. These included C_{in}, R_b, R_π, R_{cb}, R_c and C_{out}. It was these unstable results that caused difficulty in interpreting the model values and trends.

Some of the uncertainty was reduced by combining the results from different runs. This was straightforward for obvious combinations such as the collector-base feedback capacitances mentioned earlier. If the proper combination of two or more elements yielded a significantly lower statistical spread then the combination was taken as correct. If the elements were required separately they were split from the combination according to their average contribution. This was used primarily to find better starting approximations for subsequent attempts.

A better way to resolve the ambiguities was to simplify the circuit model. This may only be applied within limits so as to maintain the accuracy of the model; nevertheless, some overlap was removed without loss. The model shown in fig 3.4.2 was optimized along this line. The following have been eliminated: R_{cb}, C_{cb}, C_{in} and the transit time associated with the current source. This reduced the uncertainty and optimization time required, with negligible effect on not required separately from the internal. The input capacitance C_{in} had a very high reactance and, for a low base resistance, will work well lumped into the base-emitter capacitance C_π. The forward transit time was accounted for in the current dependency of C_π.

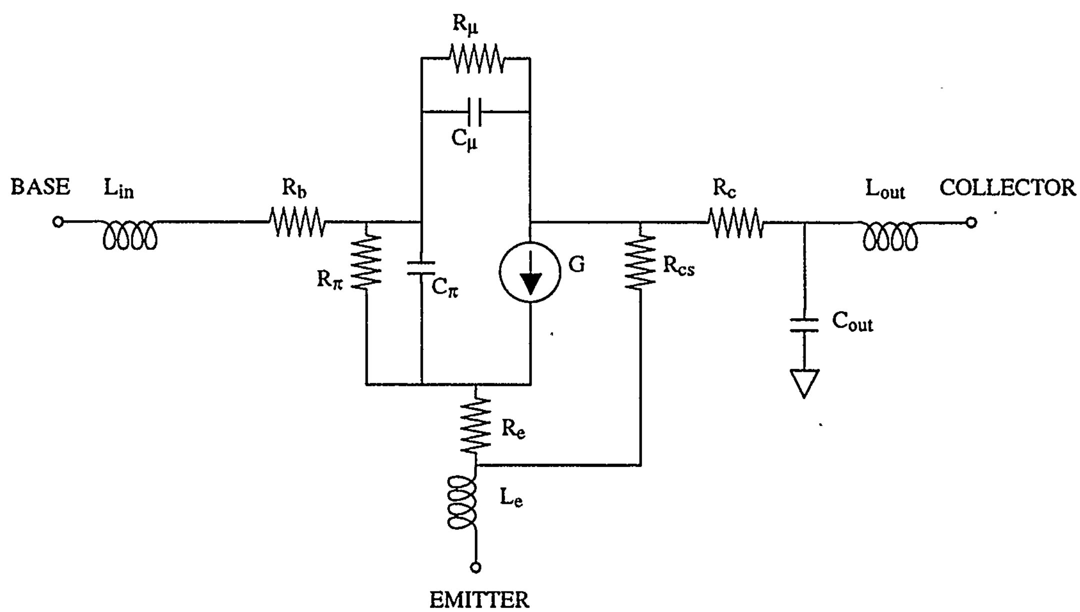


Figure 3.4.2 Simplified Transistor Model

While there are still noticeable performance differences between measured and simulated performance, the simulated circuit has enough real parameters given plausible values that it does model a realistic transistor. As the present work focuses on the transistor itself, losses in the passive circuitry (the filters and transmission lines) were ignored; simulated efficiency and gain results are therefore overestimated.

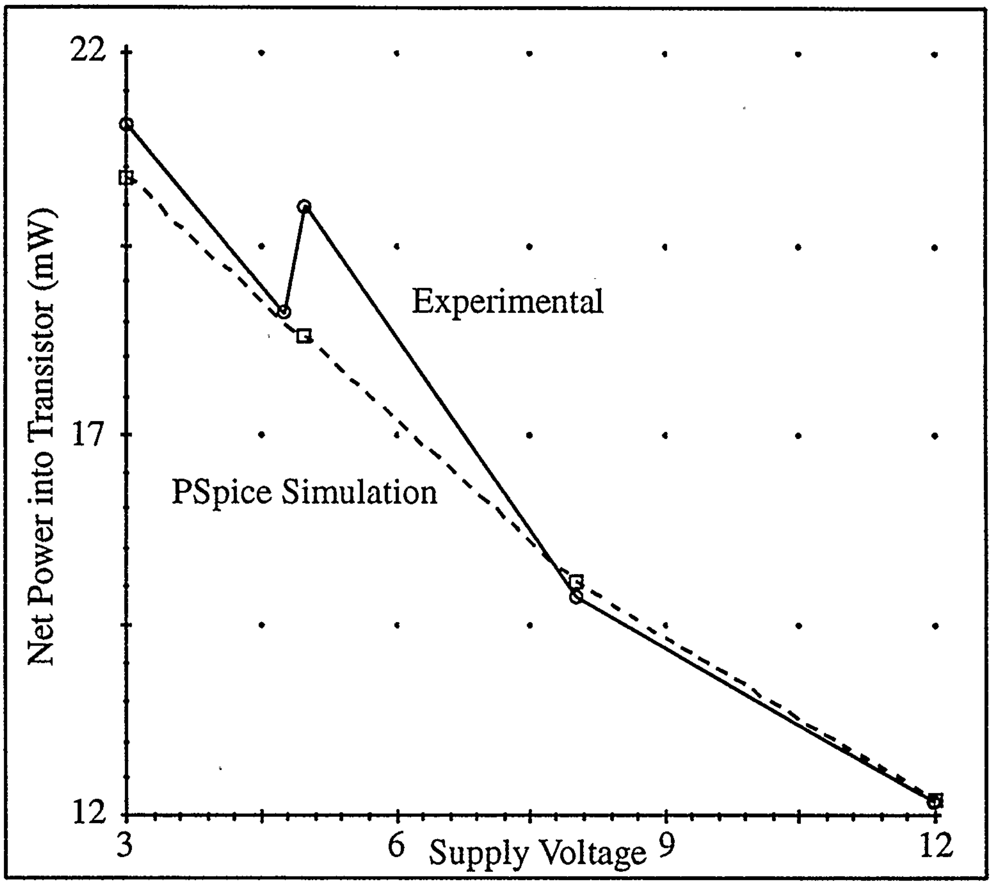


Figure 3.4.3 Comparison of Real & Simulated Net Input Power

Figure 3.4.3 compares the net input power of the transistor in both the measured and simulated circuit over a four to one range of supply voltage for one input power level. The similarity between the two is encouraging. An even closer match could have been achieved by fine tuning the simulated amplifiers input power; this was not done, as the two traces are more than close enough to show the same general characteristic.

CHAPTER FOUR

UNTUNED AMPLIFIER PERFORMANCE

The basic amplifier, without any harmonic tuning, has been measured and simulated under different conditions. Most of the basic amplifier data appear to misrepresent the efficiency of this amplifier because no fundamental frequency filter was included in the collector circuit. This differs from standard class B and C operation in which a filter at the fundamental frequency removes the signal distortion caused by the half cycle or less collector current pulses. Some simulation was performed using such a filter to allow comparison.

4.1 Amplifier Performance Without a Fundamental Filter

Measured data were obtained under two input conditions. A number of readings were taken with the amplifier input connected directly to the output of the General Radio signal generator. As described in 3.3 this was a valid operating condition but one which could be difficult to duplicate. For easier repetition and to allow comparison, circuit operation with the input harmonics suppressed was also measured. PSpice simulation results are also used so as to assess the accuracy of the basic PSpice circuit.

In simulation the actual net input power supplied to the amplifier was calculated and recorded. This was more involved for the real amplifier, in which the frequency content of the forward and reverse power had to be measured. Nevertheless, as the transistor input impedance changes with operating conditions the actual net power into the base was more accurate and useful than a reading of the power ideally available to the input. The real amplifier measurements (with the suppressed harmonics) are corrected with respect to the fundamental input reflection coefficient. This raises the gain level and PAE above that apparent from a direct measurement of power flowing towards the base and the final load so as to better agree with the simulation. When this input reflection coefficient correction has been applied it will be indicated by the description "corrected for reflection loss".

Fig 4.1.1 shows the agreement between measured and simulated collector efficiency for two input power levels over a broad range of supply voltage, while fig 4.1.2 shows gain figures in much the same way. Both figures show data corrected for input reflection loss. Collector efficiency and gain were separated rather than combined as power added efficiency so as to show the separation of error in each. It may be seen that the higher input power operation achieves a better agreement between the two sets of results, and that the low power gain of fig 4.1.2 is by far the worst behaved, especially for the higher supply levels. This is in part a measurement error; at the 12 volt supply level the measured forward (low) power was only 1.8 dB higher than the reflected. In comparison, the high power reflection was at least 3.8 dB less than the forward at all points. The closer the reflected power is to the forward the more sensitive the entire reading is to error and loss in the reflected signal. This is the same effect as when line losses appear to be a low SWR. Again as in transmission line work, there will be additional power loss due to the high SWR along a lossy line. Because this is an unbiased transistor it is very non-linear and will not amplify signals below a certain level. As the supply voltage was raised, the actual input power dropped from 21 mW to 12 mW. This will also account for some of the performance drop at higher supply levels.

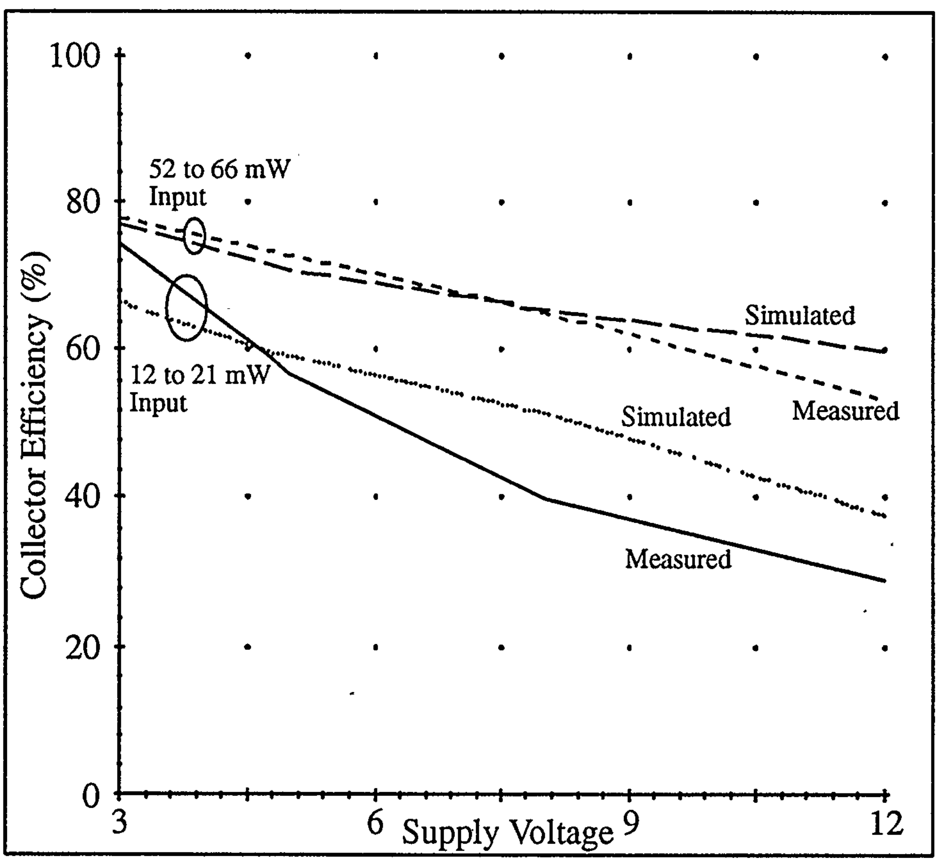


Figure 4.1.1 Typical Measured & Simulated Collector Efficiency

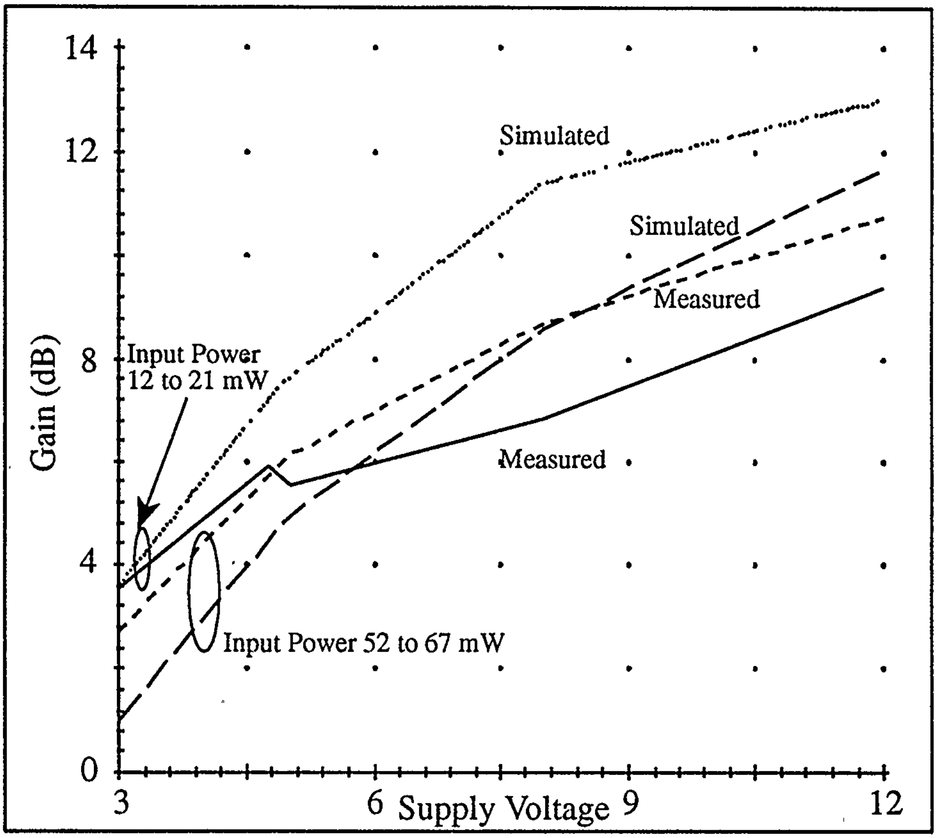


Figure 4.1.2 Typical Measured & Simulated Gain

Actual measured PAE is shown in fig 4.1.3 for three input power ranges averaging 17.3 mW, 64.5 mW and 89.3 mW. The actual net input power at the extremes of each trace are shown on the figure. The higher power level efficiencies behave as expected, rising to a peak with increasing supply voltage then dropping off gradually. Recalling that

$$PAE = \frac{P_{out} - \frac{P_{out}}{G}}{\frac{P_{out}}{\eta_c}} = \eta_c * \frac{G-1}{G},$$

the peak occurs because as the supply voltage rises the gain increases; the collector voltage can easily experience a wider swing. Also, collector dissipation rises due to the increased collector voltage-current product. The low voltage PAE drop is due to low gain, while the high voltage drop is due to poor collector efficiency. It is clear from fig 4.1.3 that the drop with high supply levels is much less steep than with low; this is even more clear in fig 4.2.1, in which a tighter sample spacing was used. The characteristic slope of PAE occurs whether or not the base harmonic terms are suppressed.

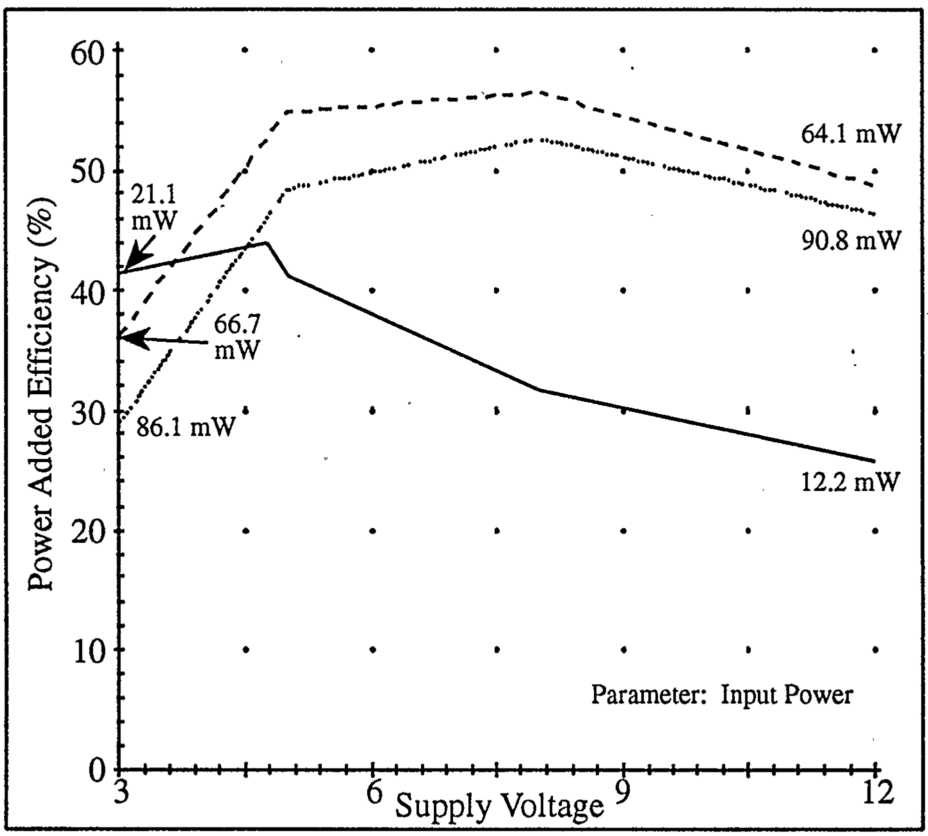


Figure 4.1.3 Measured PAE @ Three Power Levels

The low power PAE was less predictable. As shown in figs 4.1.1 and 4.1.2 the device collector efficiency begins a sharp decline at a supply level of 5 volts, and gain fails to rise as sharply as expected. It is likely that the input power is insufficient to fully activate the device and achieve the full collector voltage swing necessary for reasonable efficiency. This is plausible because the base is biased to ground potential and is accepting very low input power. This is supported by the simulation which begins to show higher minimum collector-emitter voltage levels than saturation for the same range of input power for the eight volt level. For twelve volts the separation from a saturation voltage is definite. With higher input power levels this did not occur.

Transistor conduction time is one of the aspects of circuit performance which was impractical to measure. Even with PSpice the measurement was not direct; the duration of collector current flow is not a good indication in that it has a long, gradual turnoff. The time for which collector current exceeded zero was fairly constant over a broad range of operating conditions. The external base voltage was also virtually useless; parasitic base and emitter inductance severely distorted the wave shape. Using the simulator it was practical to examine the base-emitter voltage inside the lead inductances. This voltage has a more definite shape than the external one, rising and falling fairly steeply, with a wide, relatively flat plateau of one volt, typically. An example is presented in fig . 4.1.4. Collector current began to flow when the internal base voltage reached the plateau, indicating the suitability of the plateau width as a measure of conduction time and the duty cycle. Unfortunately, the trailing edge of the plateau was somewhat less sharp than its start. To measure the conduction time it was decided that rather than establishing a threshold voltage level to judge the plateau width, the time between the voltage zero crossings could be used instead. In that the rising and falling edges are quite sharp this was a valid assumption, borne out by the correspondence between the approximate plateau widths and the more precise zero crossing timings. The latter duration was somewhat longer but conformed to the same pattern of behavior with respect to input power and supply voltage levels.

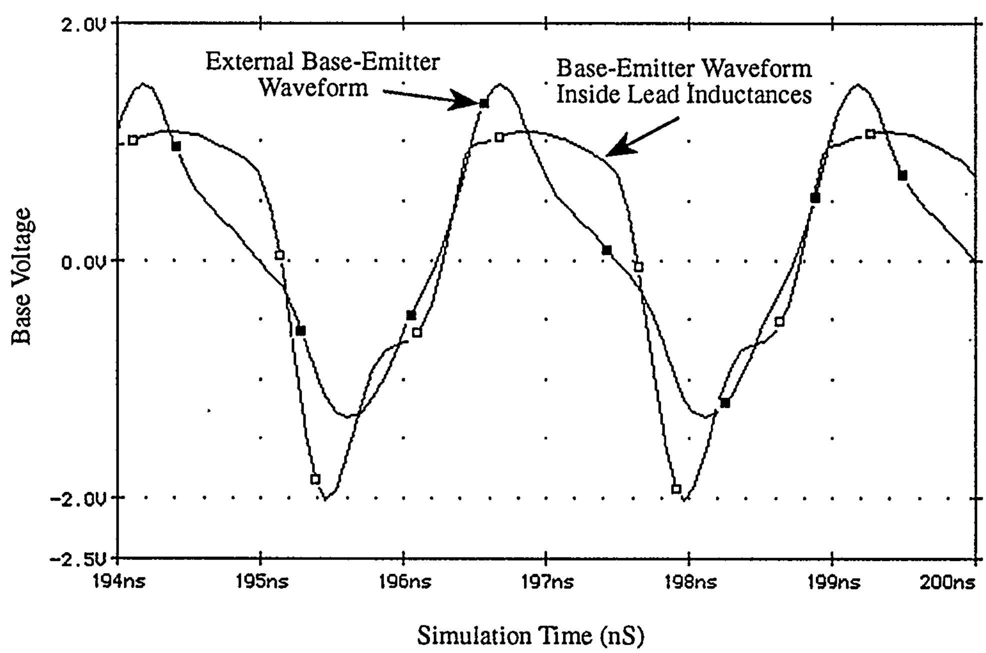


Figure 4.1.4 Effect of Lead Inductance on Base Voltage

Several plots of the dependence of conduction time on the input power level are given in fig 4.1.5, in which the supply voltage is a variable parameter. Three, eight and twelve volt levels are shown based upon only three power level data points, while the five volt data has eight; this was tolerated because of the general agreement between the simple traces and the five volt detailed trace. As with fig 4.1.3, for power levels beyond a certain point (18 mW with a five volt supply) the slope of each trace in fig 4.1.5 is remarkably consistent.

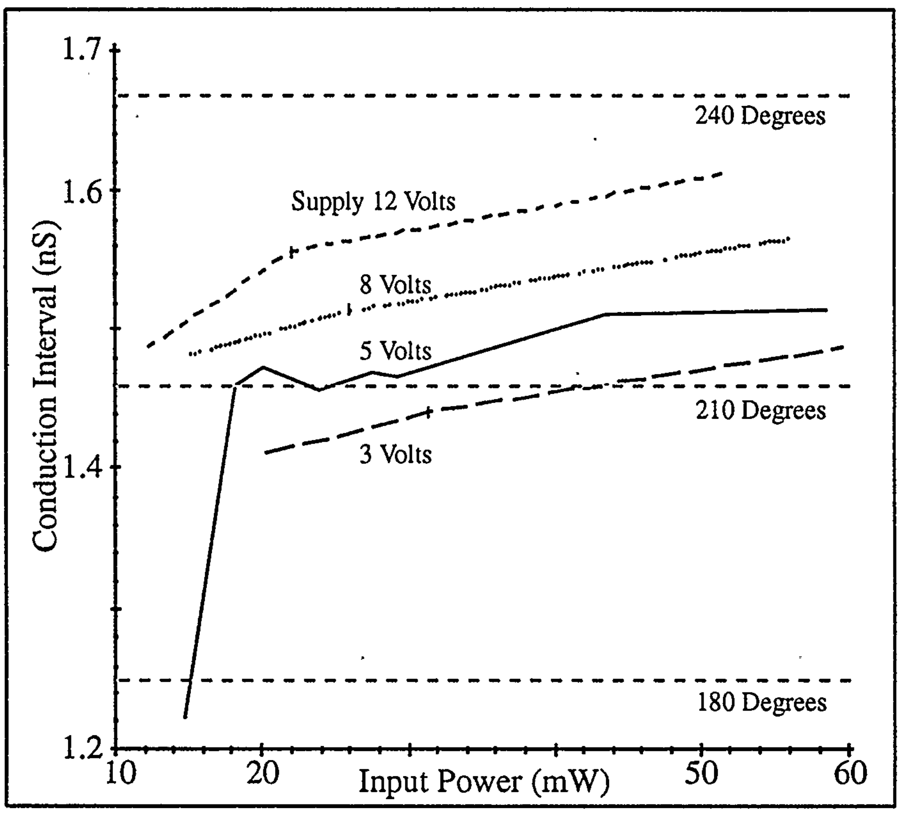


Figure 4.1.5 Conduction Interval & Input Power (Simulation)

In simulation the power accepted by the transistor was a function of supply voltage (fig 3.4.3). The model parameter used to set the input power was the level of a fifty ohm voltage source. While the voltage required to set an input power for a given supply level could have been found this would have required an extreme number of simulation runs and an unreasonable amount of time. Accordingly, the signal source open circuit amplitude was taken to be constant and the input power level allowed to drift. Given the consistent slopes of fig 4.1.5, however, it was practical to generate figures approximating the conduction intervals for a constant input power, subjected to a varying supply. A least mean squares linear best fit equation was found for each of the traces in the figure. Because of the droop at low power levels the data used were those with input power exceeding 22 to 31 mW. The line equations are given in table 4.1.1, where input power is in milliWatts.

Table 4.1.1 Linear Best Fit to Figure 4.1.4

Supply Voltage	Conduction Interval Linear Best Fit (nS)
3.00	$t_c = 1.390 + 0.001631(P_{in})$
5.00	$t_c = 1.425 + 0.001634(P_{in})$
8.00	$t_c = 1.469 + 0.001715(P_{in})$
12.0	$t_c = 1.516 + 0.001839(P_{in})$

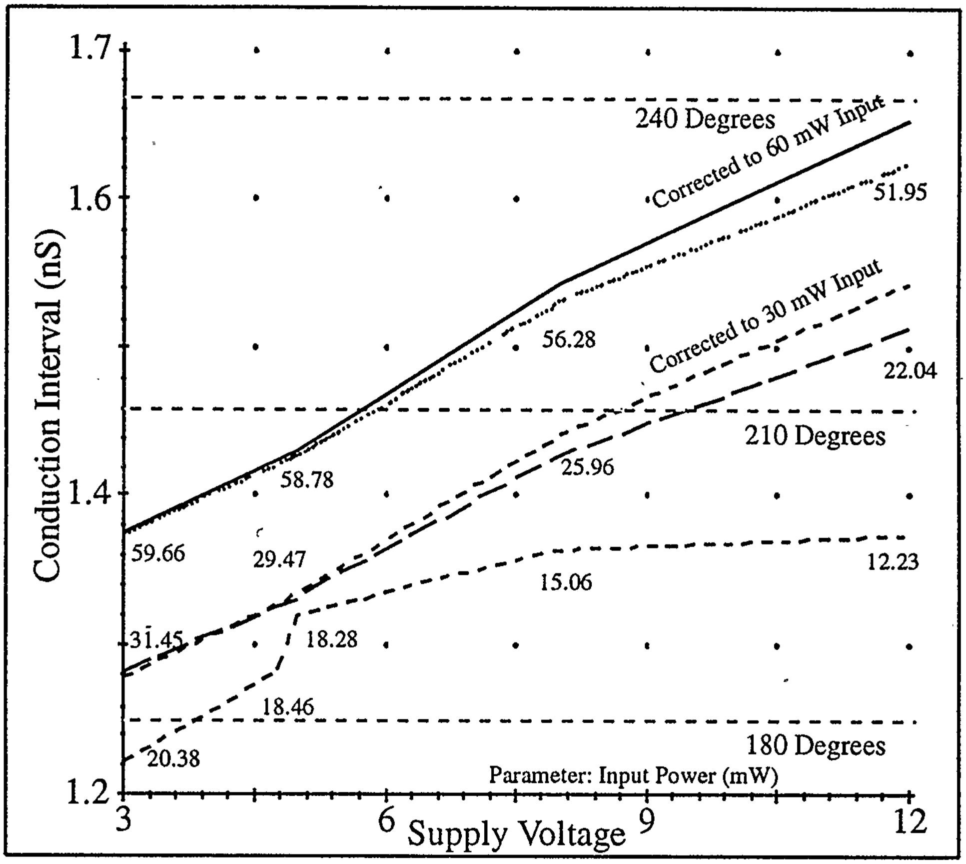


Figure 4.1.6 Conduction Interval & Supply Voltage (Simulation)

The basic and corrected, constant power conduction times are shown in fig 4.1.6. This correction could not be performed for the lowest power data; as may be seen in fig 4.1.4 the conduction time drops sharply for power below a definite cutoff level and may not be easily predicted.

4.2 Measured Performance With Harmonic Rich Input

As mentioned earlier the output impedance of the General Radio signal generator was not a good termination for harmonic power generated in the base of the transistor in the amplifier (section 3.3). When attenuation was not applied to these signals they set up harmonic standing waves along the transmission lines connecting the transistor to the oscillator; these lines included microstrip matching circuits in the amplifier and one or more unmeasured lengths of RG-58 coaxial cable. Any readings taken in this environment have an unintended form of harmonic tuning applied to the input; as this tuning was not adjusted at all, it is quite possibly detrimental for at least some of the readings. Power added efficiency dependence on supply level in this mode is compared with the results given earlier, with input harmonics suppressed, in fig 4.2.1. It should be noted that these results have not been corrected to compensate for input reflection loss. The actual PAE and gain performance would be higher were a better input match used. As expected, the PAE rises rapidly to a peak then declines gradually as the supply level is raised.

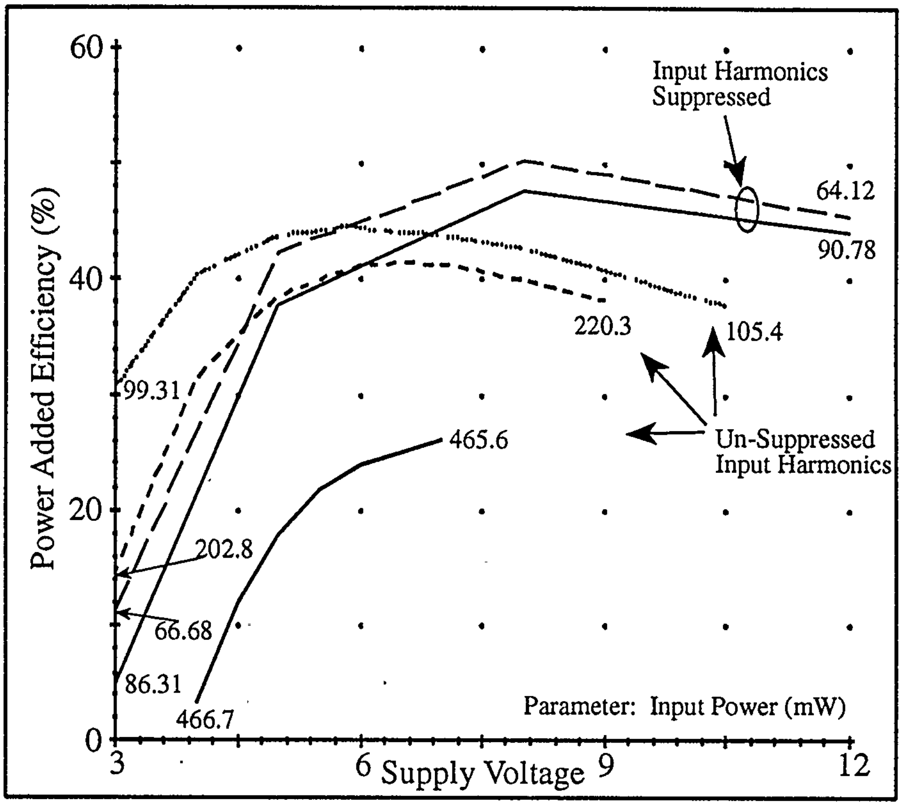


Figure 4.2.1 PAE Dependence on Supply & Input Harmonics

For an unchanged circuit the peak PAE for a higher input level will occur at a higher voltage, as described earlier. This is best seen in the un-suppressed input harmonic curves of the figure. The 466 mW input trace was not completed, as the transistor would have been damaged by excess power dissipation. The suppressed input harmonic circuits exhibit higher PAE at a greater supply level even though they use less input power. The reason why is not apparent from the figure but may be seen if PAE is broken up and plotted separately as collector efficiency and gain, figs 4.2.2 and 4.2.3, respectively. The random coaxial cable length in the un-suppressed harmonic circuit is allowing harmonic tuning that raises the circuit gain but results in lower collector efficiency. Comparing the 88 mW suppressed trace to the 103 mW un-suppressed, the difference is roughly 1.76 dB and 9%. Because gain rises while efficiency drops with supply voltage, this lower gain and higher collector efficiency yields a maximum PAE for a higher supply.

While the supply level for maximum PAE varies with the input circuit termination the actual peak efficiency seems more consistent. Data measured with the unknown termination is used in Chapter Six.

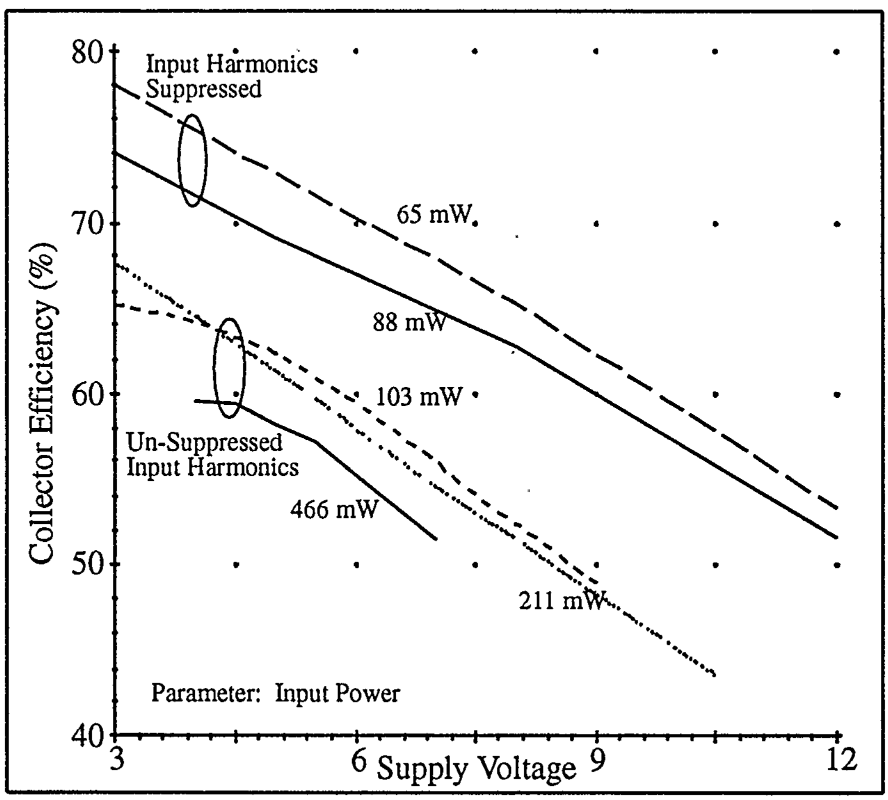


Figure 4.2.2 Collector Efficiency Dependence on Supply & Input Harmonic Suppression

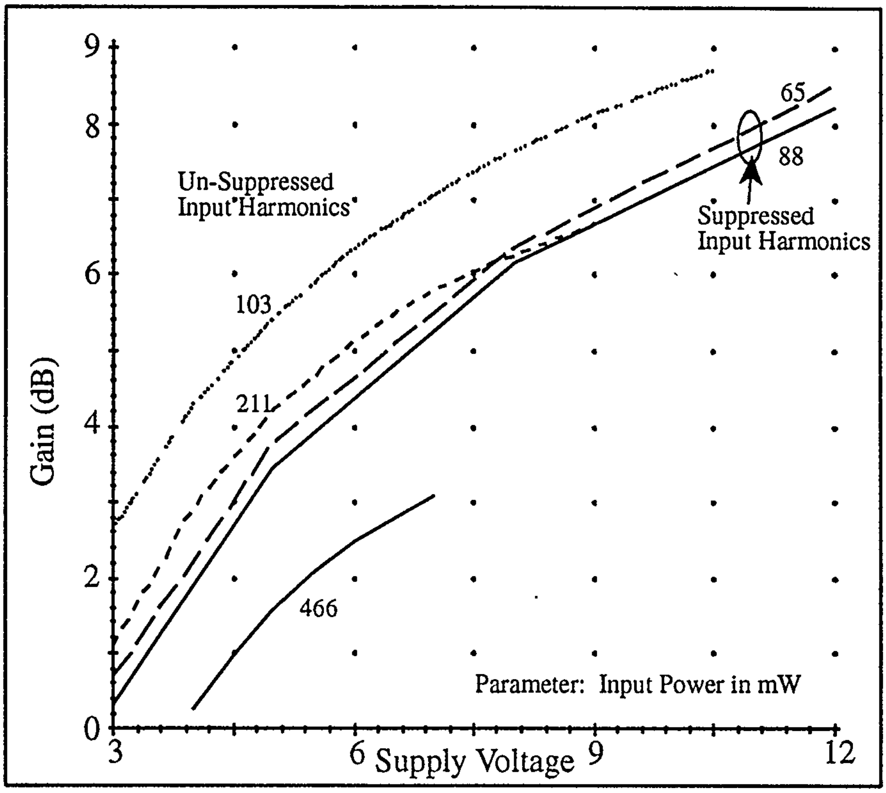


Figure 4.2.3 Gain Dependence on Supply & Input Harmonic Suppression

4.3 Untuned Operation With & Without Collector Filter

All of the untuned amplifier data mentioned previously were obtained without any fundamental filter in the collector circuit. This was how the actual amplifier was operated for untuned measurements and in a number of simulations. As shown in fig 4.3.1, for higher power levels the second harmonic output component was low, though it rose with increased supply voltage. This pattern was also shown by the simulations, and suggests that for this zero bias voltage configuration a large collector voltage swing corresponds to reduced relative second harmonic output. As the figure also shows, the simulated circuit had considerably higher second harmonic output; this may be because it does not allow for transmission line and impedance match losses. Because of the high second harmonic content in simulation and in the real circuit at lower power levels a set of simulations was run in which a parallel inductor-capacitor filter tuned to the fundamental was substituted for the collector choke. This addition raised the power added efficiency directly by amplifying only the desired fundamental signal, short circuiting harmonic voltages to ground such that less harmonic power is generated. The filter used had a quality factor of one, based on the fifty Ohm load. As shown, even this filter reduced the second harmonic output power by at least 10 dB.

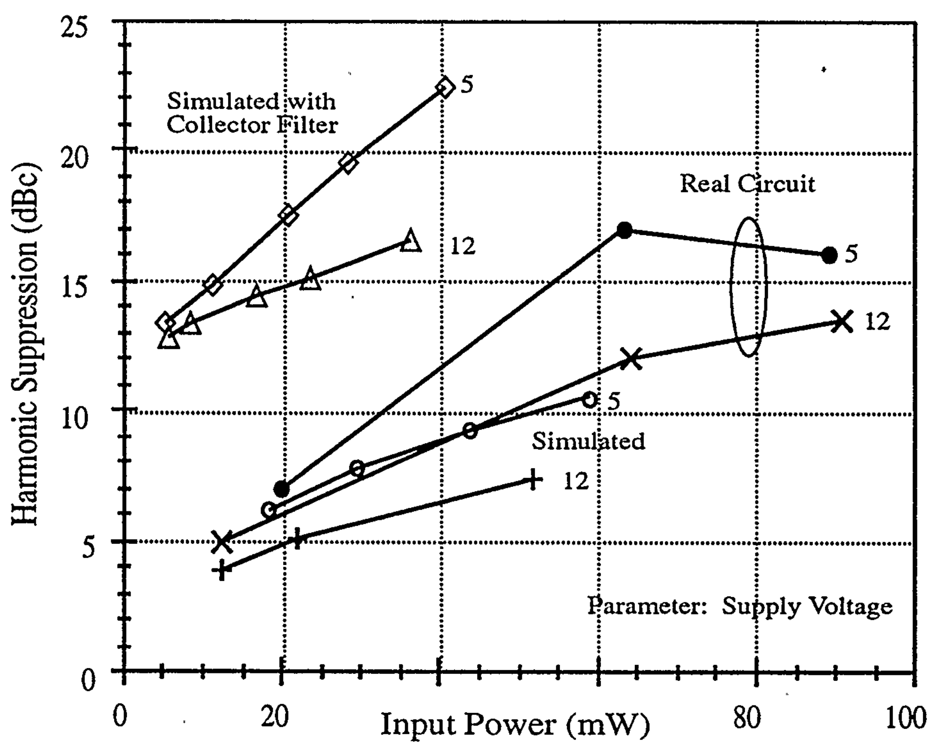


Figure 4.3.1 Second Harmonic Suppression Dependance On Supply, Input Power & Circuit

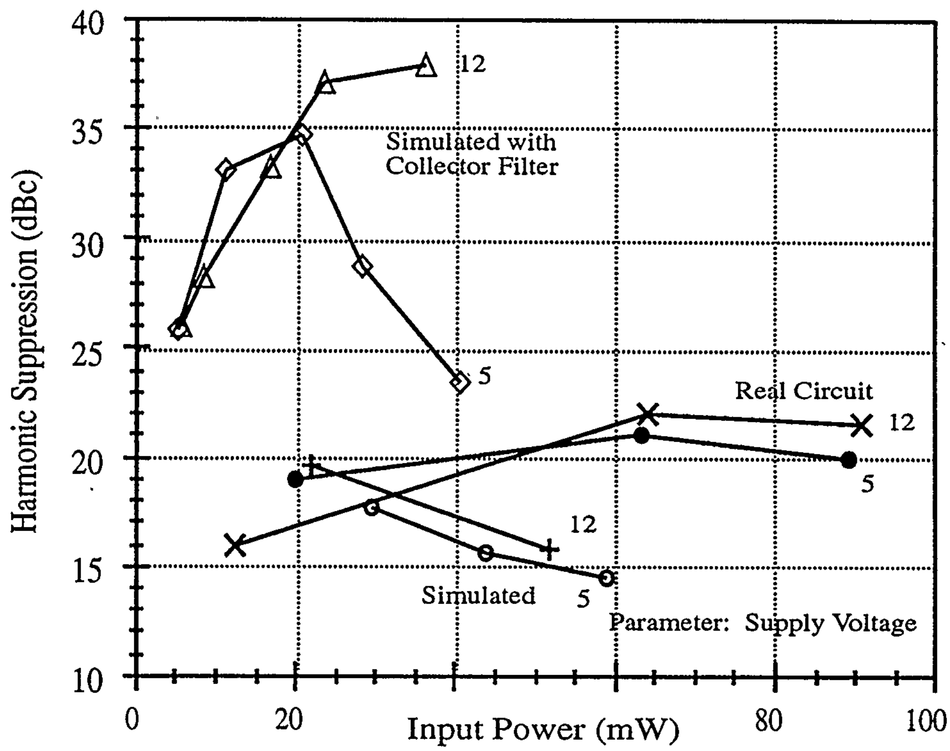


Figure 4.3.2 Third Harmonic Suppression Dependance On Supply, Input Power & Circuit

Similar measurements for third harmonic distortion are presented in fig 4.3.2, in which there is less interaction between supply level and third harmonic content for the real circuit. As expected, the third harmonic levels are considerably lower than the second. The use of a fundamental filter instead of the RF choke reduced the third harmonic output, though for low supply and high input levels the third harmonic output was rising sharply.

In simulation, using the fundamental filter in the collector supply raised power added efficiency considerably, as shown in fig 4.3.3. Both gain and collector efficiency were raised. In that output harmonics were better suppressed in the real circuit the collector filter would not cause quite so much improvement. It should be noted that in a practical circuit the filter is more likely to be series tuned at the fundamental frequency. This differs from classical class C operation but is more practical for reasonable filter Q and impedance at higher frequencies.

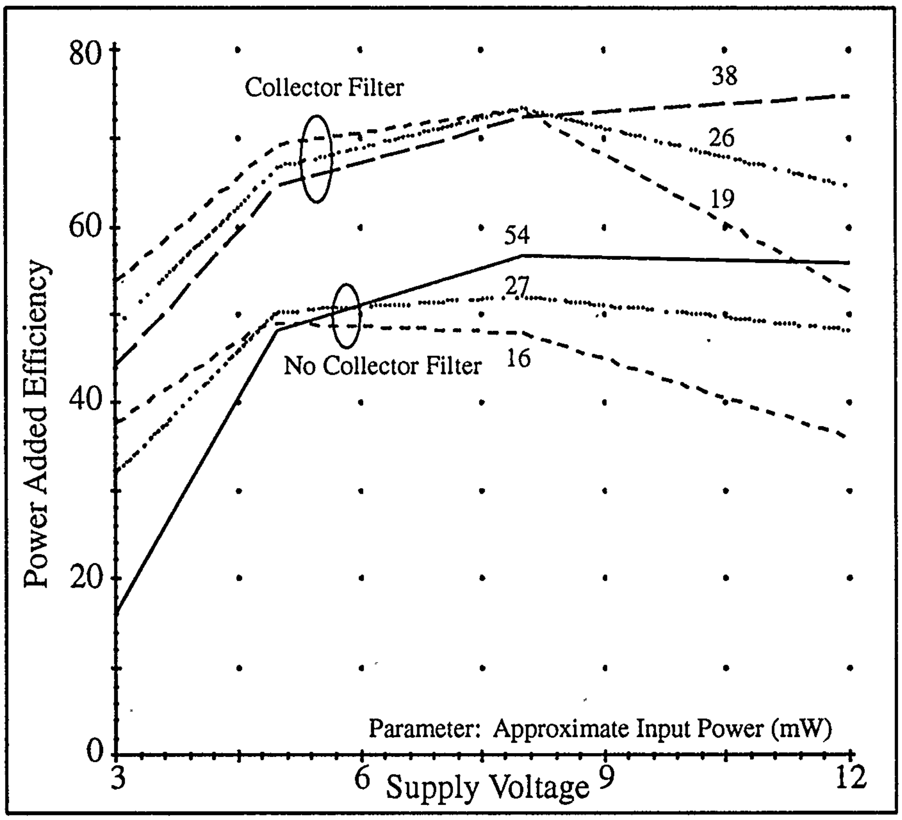


Figure 4.3.3 PAE Dependence on Supply & Collector Filter (Simulation)

The filter improves performance in part by reducing the amount of DC supply power converted into undesired output components; it does this by reducing the collector supply impedance for frequencies other than the fundamental. This turned out to affect the internal operation of the transistor more than expected. Fig 4.3.4 shows a comparison between transistor conduction periods with and without the filter. With the filter the conduction intervals are significantly shorter, and are more consistent for lower input power levels than, for instance, the five volt basic trace.

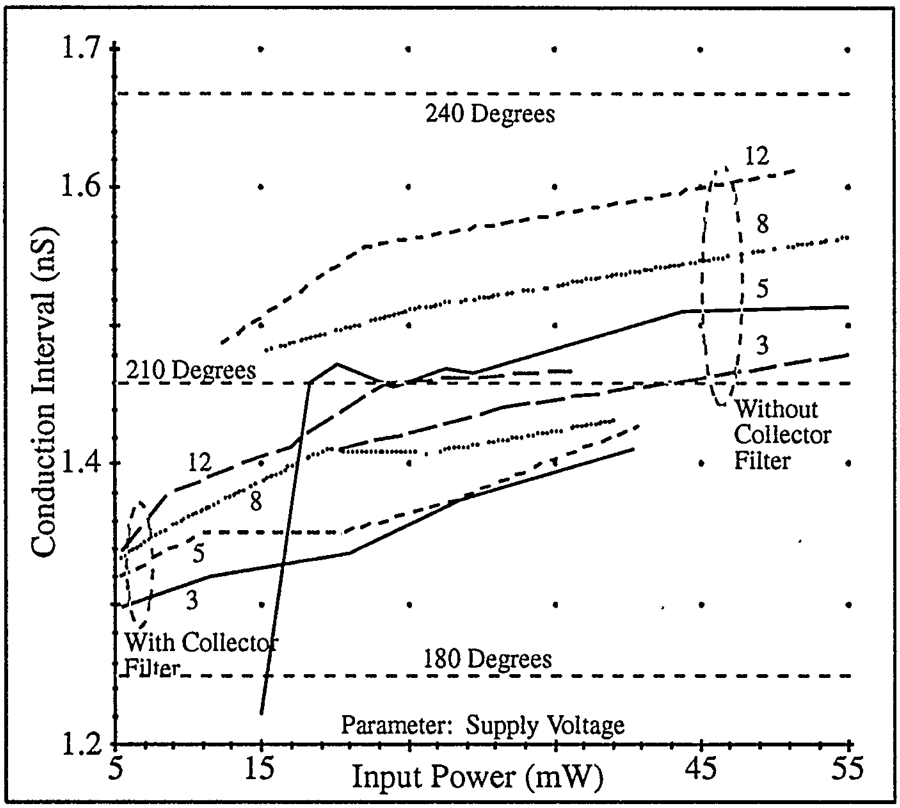


Figure 4.3.4 Conduction Interval Dependence on Collector Filter (Simulation)

That the filter should have this effect is interesting; for the present work, conduction time has been determined as the interval in which the intrinsic base-emitter voltage exceeds zero. This is, therefore, an example of the bi-directional nature of the bipolar transistor, in that a change in collector circuit conditions should have such an influence over the input. The transistor input impedance, both real and reactive, was slightly lower in the filtered circuit under equivalent conditions. The differences were small relative to those imposed by supply variation.

As mentioned, a fundamental filter at the collector prevents waste power generation at undesired harmonics. In order to see if this was a sufficient explanation of the performance differences in fig 4.3.3 the results of a series of simulations with and without the filter were used to create fig 4.3.5. This figure compares power added efficiency based on total power output from both an unfiltered and filtered amplifier under similar operating conditions.

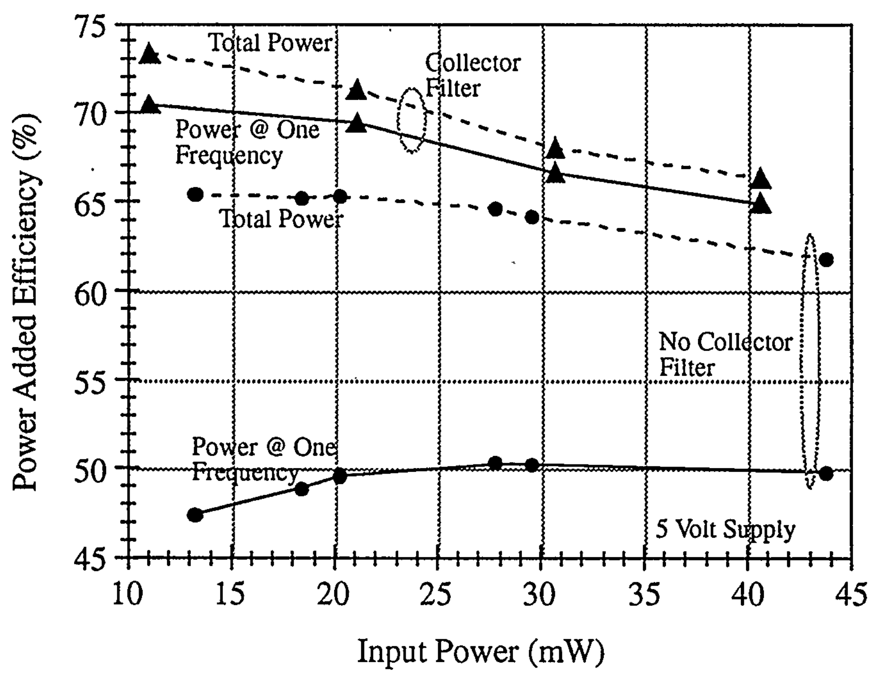


Figure 4.3.5 PAE From Fundamental & Total Output Power (Simulation)

It should be noted that on the basis of total power output the amplifier without a collector filter operates much better than described earlier, based on single frequency performance. This is due to the reduction in transistor and circuit performance at higher frequencies. The PAE improvement in the filtered circuit was considerably smaller, indicating the filter reduction of undesired signal content in the output.

CHAPTER FIVE

SECOND HARMONIC TUNING

As discussed earlier, lower order harmonics are more available than higher orders for an economical transistor (13, 14). The second harmonic also has greater potential for efficiency improvement than the third harmonic. For these reasons considerable attention was given to operation of the amplifier under second harmonic tuning. The tuning circuitry may be applied to the amplifier at the output, input or both.

5.1 Measured Performance

The measured results here are for a single sinusoid input; reflections of base junction harmonic power back from the signal generator are attenuated by at least 27 dB.

Tuning the second harmonic at the input only did not yield good performance. For the other tuning combinations performance was optimized for the highest PAE. After adjusting the series tuned filter to ground as much of the second harmonic as possible the filter was connected to the amplifier by a variable length coaxial segment. The length of the coaxial link was then adjusted for peak power added efficiency at one or more supply voltages. Where the input and output were both tuned this required several iterations, tuning the output and then the input for best performance. The line lengths for the suppressed input harmonic data are given in table 5.1.1, accompanied by the input power levels and the supply voltages at which the circuit was tuned (designated by an asterisk). The different conditions tested may be referred to by their average input power levels. These had the standard deviations given in brackets.

Table 5.1.1 Second Harmonic Tuning

Tuning	Input Line Length (cm)	Output Line Length (cm)	Supply Voltage	Input Power (mW)	Average Input (Deviation)
Output		10.9	3 *	69.66	70.80
		12.5	5 *	71.78	(0.773)
		12.4	8 *	70.63	
		12.4	12 *	71.12	
Output		3.5	3	62.81	67.05
		3.5	5 *	64.27	(3.56)
		3.5	8 *	70.96	
		3.5	12 *	70.15	
Input & Output	8.4	12.	3	34.43	40.10
	8.4	12.	5	39.08	(5.09)
	8.4	12.	8 *	46.77	
	8.4	12.	12	44.67	
Input & Output	9.2	12.6	3 *	25.12	31.31
	9.2	12.6	5	29.44	(4.55)
	9.2	12.6	8	33.27	
	9.2	12.6	12	37.41	

* denotes operating points at which harmonic tuning circuit was adjusted

Circuit measurements of gain, collector efficiency and power added efficiency for the tabled combinations are shown in figs 5.1.1, 5.1.2 and 5.1.3, respectively. The corresponding untuned amplifier measurements from the highest PAE test are included for comparison.

Several patterns may be seen directly from fig 5.1.1. In spite of tuning line length and input power level differences, both double tuned circuit measurement sets have almost exactly the same gain characteristic. Also, the output tuned and untuned data follow the same general trend as the double tuned ones, with lower gain. Finally, the untuned amplifier gain is very similar to one of the output tuned traces.

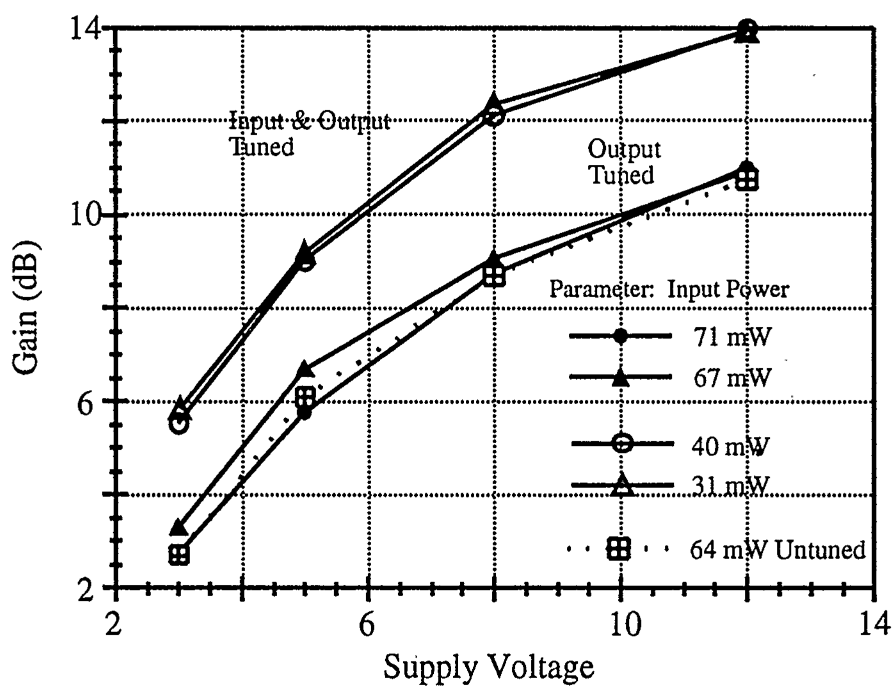


Figure 5.1.1 Gain Variation with Tuning Method & Supply (Measured)

Comparing collector efficiency, fig 5.1.2, there is less agreement between the measurement sets, though all the traces have a similar general trend. The collector efficiency of the untuned amplifier is very close to the lower power double tuned result, whereas they were the least similar in gain. In both gain and collector efficiency the untuned amplifier had close to the worst measured performance.

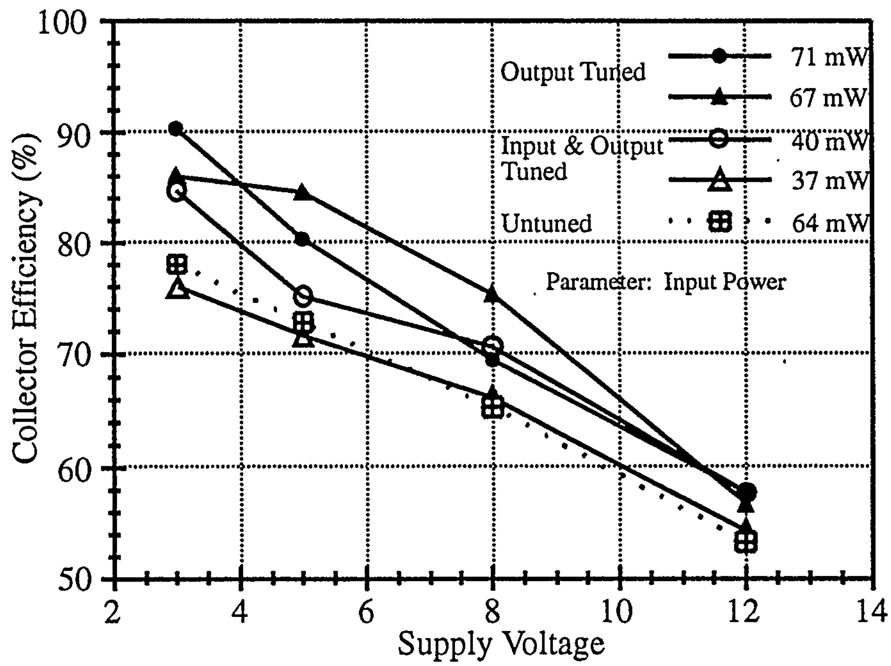


Figure 5.1.2 Collector Efficiency Variation with Tuning Method & Supply (Measured)

Because PAE is based on both collector efficiency and gain, the final PAE of the basic amplifier is lower than any of the tuned measurements, as shown in fig 5.1.3. While the best output tuned PAE matches the best results with input and output tuning it does not do so over as wide a range of supply voltage. This suggests that both the input and output should be tuned for operation in low regulation or collector modulation environments. The wider zone of high efficiency operation under input & output tuning is due to its higher gain at all measured points.

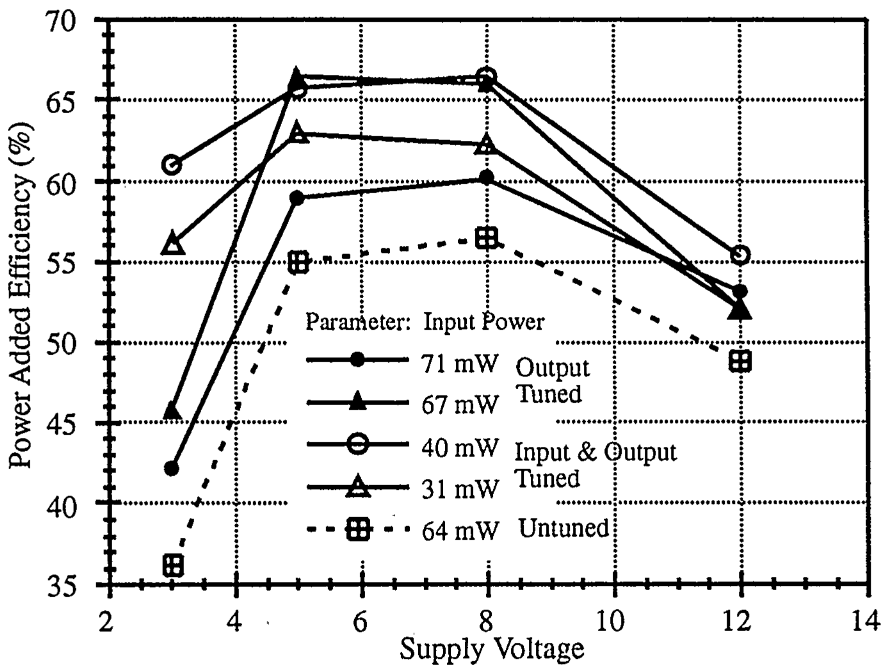


Figure 5.1.3 PAE Variation with Tuning Method & Supply (Measured)

Comparing the average double tuned gain to the average output tuned gain at each supply level, the double tuned operation had 5.90 dB more gain, with a standard deviation of only 0.46 dB. When variable envelope (eg AM) operation is expected, output tuning may be more practical; the double tuned amplifier was more prone to parametric oscillation in response to excessive input levels. The additional loss caused by the input variable length line and harmonic filter was not measured; with better components even higher double tuned performance could be practical. In spite of their additional losses, both output and double tuned amplifiers surpassed the untuned amplifier PAE by 10% at its best point, and by considerably more at lower supply levels.

5.2 Simulation

Simulating a simple second harmonic tuned amplifier with PSpice confirms the real experimental results. PSpice was not an ideal package for this purpose for several reasons. Input power levels could not be specified accurately and thus required a degree of trial and error. For this reason input power was used as the independent variable in the following figures. Considerable effort was also required to optimize the transmission line length between the amplifying device and the harmonic filter. The best circuit corresponds to the general class F amplifier modified to use the second harmonic only. A typical PSpice file is reproduced in Appendix 2.

The simulated amplifier used in this section employs a fundamental frequency filter at the collector of the transistor. This is, therefore, a proper comparison of a standard amplifier and an enhanced performance harmonic tuned one.

An unexpected improvement in gain may be seen in figs 5.2.1 and 5.2.2 for lower and higher supply levels, respectively. The figures describe gain indirectly, showing output power as a function of input power. The output tuned amplifier has much higher gain for lower input levels. It also saturates more sharply, tending to an almost constant output power influenced only by the supply level.

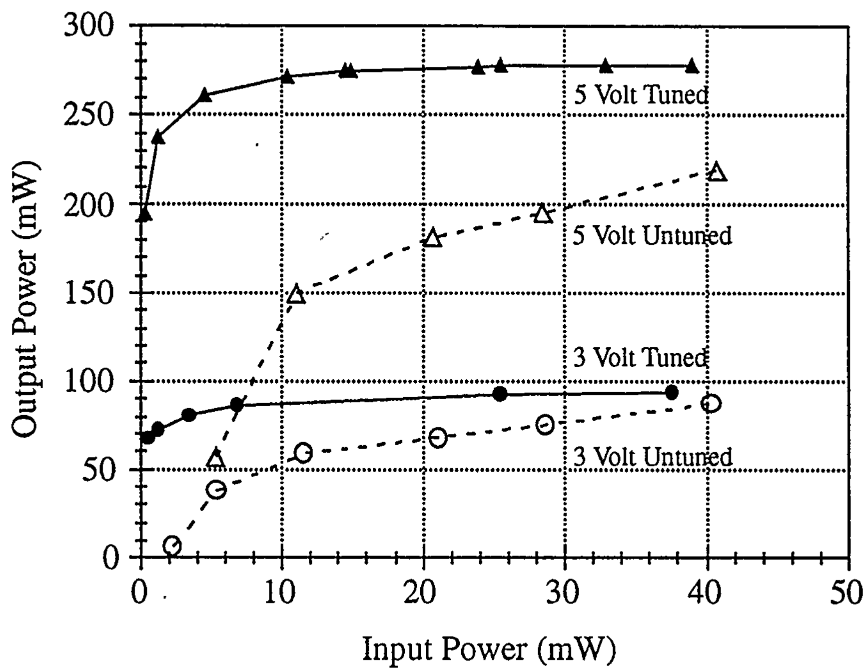


Figure 5.2.1 Simulated Gain Improvement With Second Harmonic Tuning

Collector efficiency measurements from the simulator are shown in figs 5.2.3 and 5.2.4. At lower input levels the harmonic tuned amplifier performance is due to improved gain characteristics as well as the modified collector waveform. At higher power levels the untuned amplifier collector efficiency roughly parallels the tuned efficiency; even there, it is lower, with a difference of roughly 6% for all traces except for the 12 Volt supply.

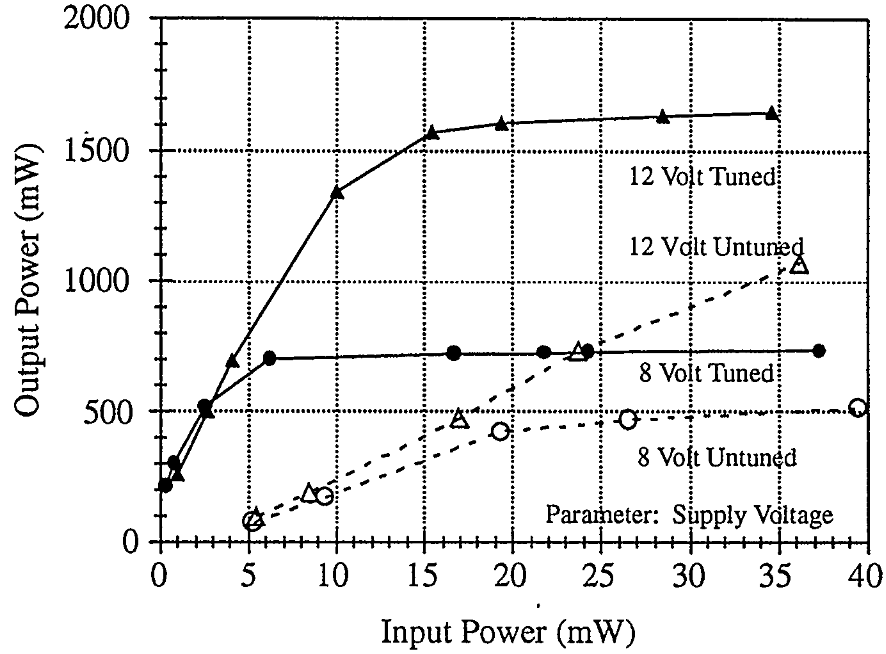


Figure 5.2.2 Simulated Gain Improvement With Second Harmonic Tuning

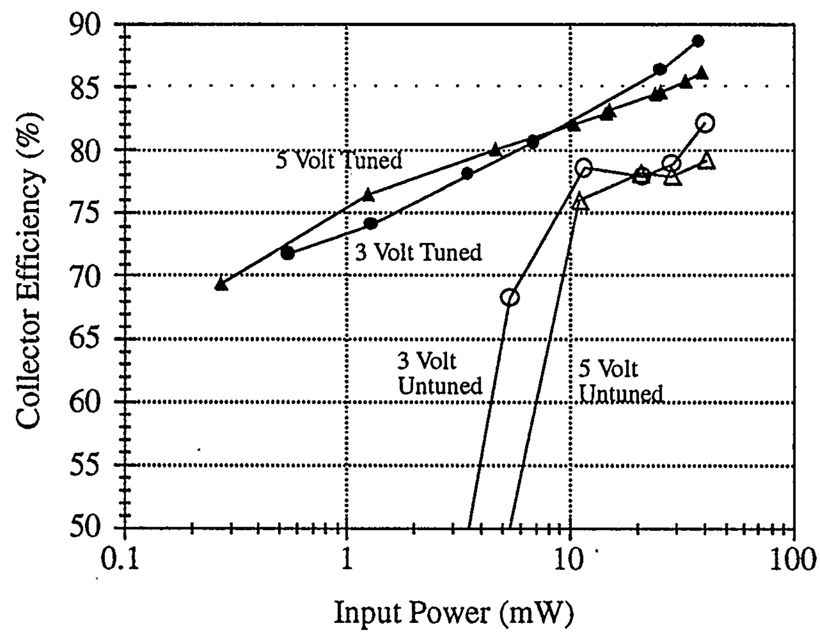


Figure 5.2.3 Simulated Collector Efficiency Improvement With Second Harmonic Tuning

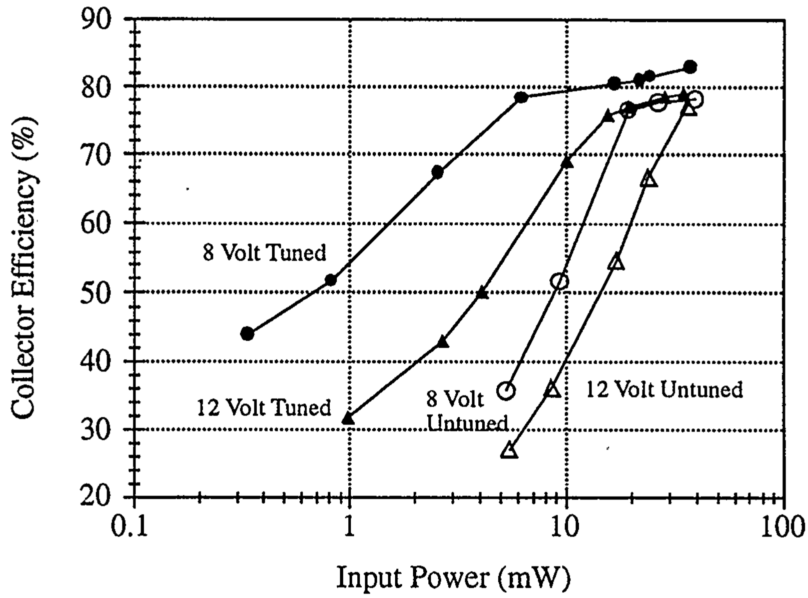


Figure 5.2.4 Simulated Collector Efficiency Improvement With Second Harmonic Tuning

Power added efficiency performance with and without second harmonic tuning is as shown in figs 5.2.5 and 5.2.6. As could be predicted from the gain and collector efficiency curves harmonic tuning results in higher PAE. For low input power levels the superior tuned gain allowed 50% or greater improvements. At higher input levels, where the traces become more parallel, the tuned amplifier has a PAE at least 6% to 8% higher than the basic unit, tending to be even better at the highest power levels. This result is not seen so clearly for the 12 Volt supply in that the curves do not become parallel within the power range simulated; nevertheless the tuned amplifier performs better at all the measured points. It is assumed that the lines would become parallel for simulations at higher power levels.

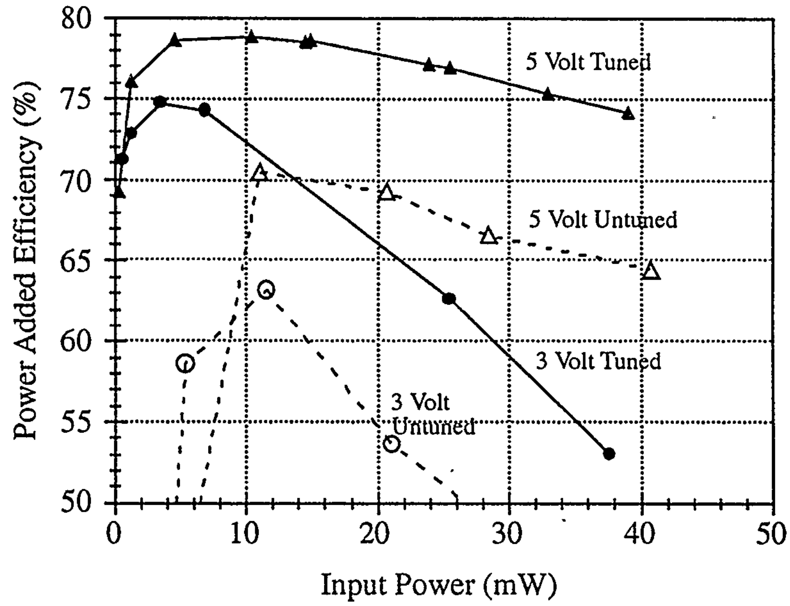


Figure 5.2.5 Simulated Power Added Efficency Variation With Input Power

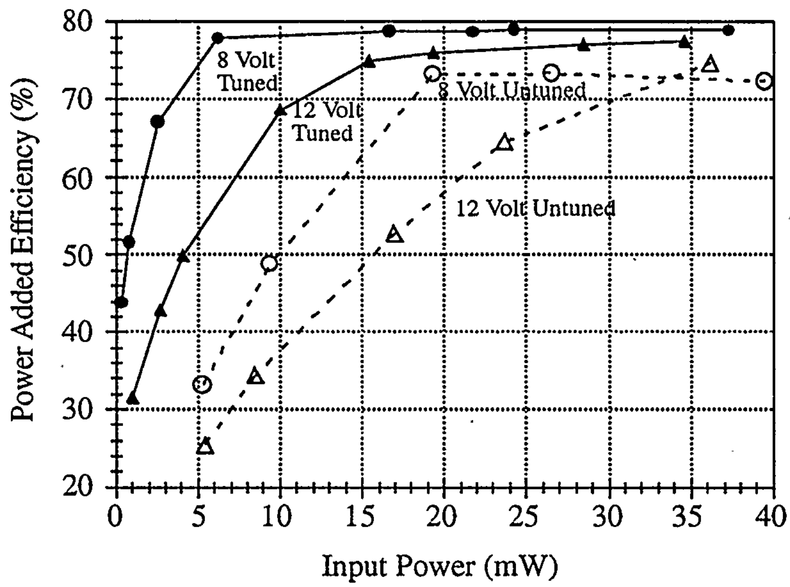


Figure 5.2.6 Simulated Power Added Efficency Variation With Input Power

CHAPTER SIX
EFFECTS OF DIFFERENT TUNING METHODS ON LINEARITY & EFFICIENCY

6.1 Introduction

The measurements described in this chapter were taken with the signal generator connected directly to the amplifier input. As described in section 4.1 this resulted in high, unmeasured harmonic content at the transistor input, due to standing waves generated by the nonlinear transistor junction and the mismatched impedance. These results are included in spite of the arbitrary harmonic input levels, in that they compare several harmonic tuning methods. The qualitative results should be of use.

6.2 Intermodulation Distortion

As intermodulation distortion (IMD) performance is a useful measure of amplifier linearity for single sideband and multi-carrier applications, the IMD characteristics of the basic amplifier (with no collector filter), second harmonic, third harmonic and Raab's method of tuning were measured (8, 15). A two tone test was used, with tones at 400 and 410 MHz, combined in a hybrid ring to provide isolation between the signal generators. Frequency separations of less than 10 MHz allowed undesired interaction between the signal generators in spite of the hybrid ring. Unless noted otherwise, the harmonic tuning circuits were all adjusted for peak PAE at a supply voltage of 7.00 Volts; the supply voltage was then raised and lowered in order to explore the IMD characteristic under various operating conditions.

Table 6.2.1 Input Power Balance for IMD Tests

Input Signal(s)	Input Power (dBm)	Difference From Combined Input	Output Power (dBm)	Sum of Output Powers (dBm)
Combined	20.54		26.91	
400 MHz	17.43	3.11 dB	24.61	26.92
410 MHz	17.46	3.08 dB	23.08	26.92

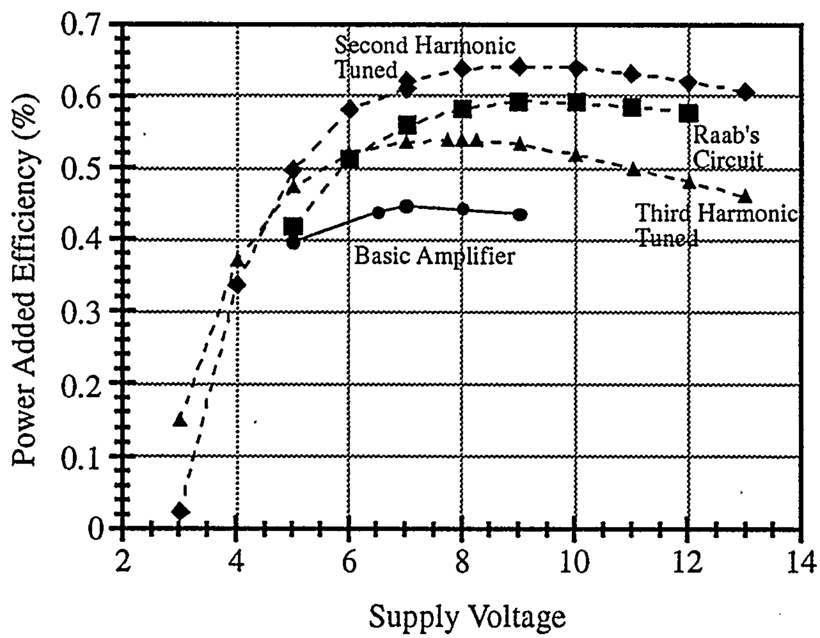


Figure 6.2.1 Two Tone PAE Variation (17 dBm Input)

For brevity only the average of the upper and lower third order IMD terms are presented here; more detailed information is presented in Appendix 3. Figs 6.2.1 to 6.2.3 show the variation of power added efficiency with supply voltage for two tone input signals. The indicated power is as indicated by a power meter measuring the combined signal. This input reading is shown to correspond to the total input power by the measurements presented in table 6.2.1.

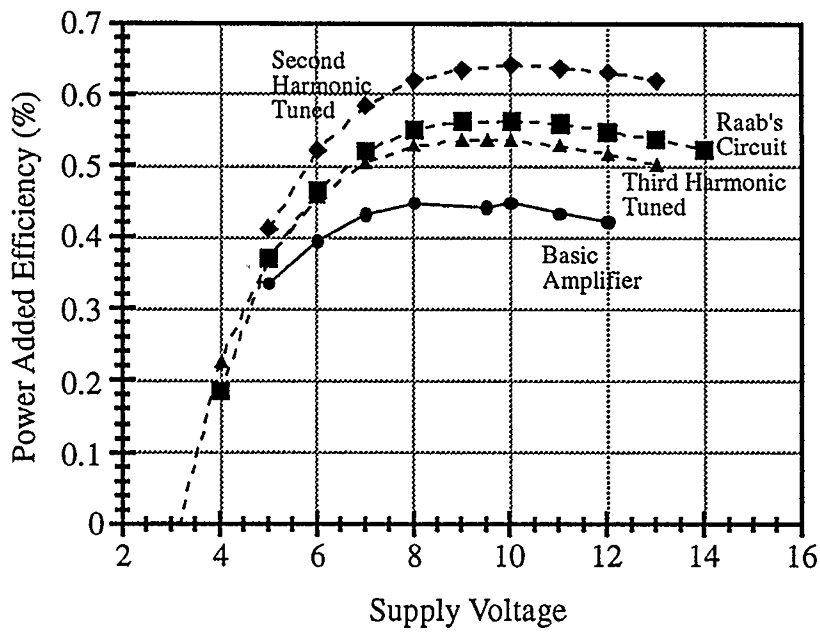


Figure 6.2.2 Two Tone PAE Variation (20 dBm Input)

From the figures it is apparent that there is a repeatable performance agreement between the various harmonic tuning methods over a considerable range of power and efficiency. For the lower power levels second harmonic tuning has the highest PAE. This may be seen in figs 6.2.1 and 6.2.2, for input power levels of 17 dBm and 20 dBm, respectively. As the power level increases, third harmonic tuning becomes more effective until, at the 23 dBm level (fig 6.2.3) it exceeds all the other modes. This is because at a given supply level, under higher power operation the collector waveform is more prone to saturation. Symmetrical saturation at the voltage extremes will result in greater odd harmonic signal content, allowing third harmonic tuning to operate better than at lower levels.

This saturation characteristic may be seen very clearly in figs 4.3.1 and 4.3.2, in which second harmonic suppression increases with an increase in input power, while third harmonic suppression decreases. It is most evident for the simulation data, but is present to a degree in the actual measured data. The second and third harmonic tuning measurements in fig 6.2.3 have not reached a peak level; power dissipation limits prevented tests of higher supply levels.

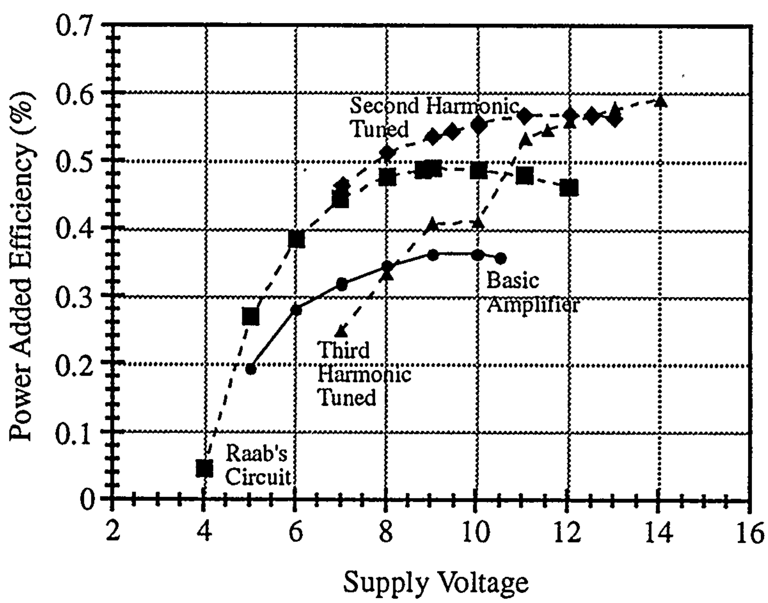


Figure 6.2.3 Two Tone PAE Variation (23 dBm Input)

Comparing figs 6.2.4, 6.2.5 and 6.2.6 it may be seen that the basic amplifier consistently has the best linearity but the lowest peak PAE. Third harmonic tuning tends to have the best IMD performance of all the harmonically tuned circuits, but is surpassed in efficiency by Raab's circuit and second harmonic tuning. For the 23 dBm power input level the third harmonic circuit exceeds the other tuned modes and approaches the linearity of the basic amplifier. Second harmonic tuning outperforms Raab's circuit in both peak PAE and the attendant linearity.

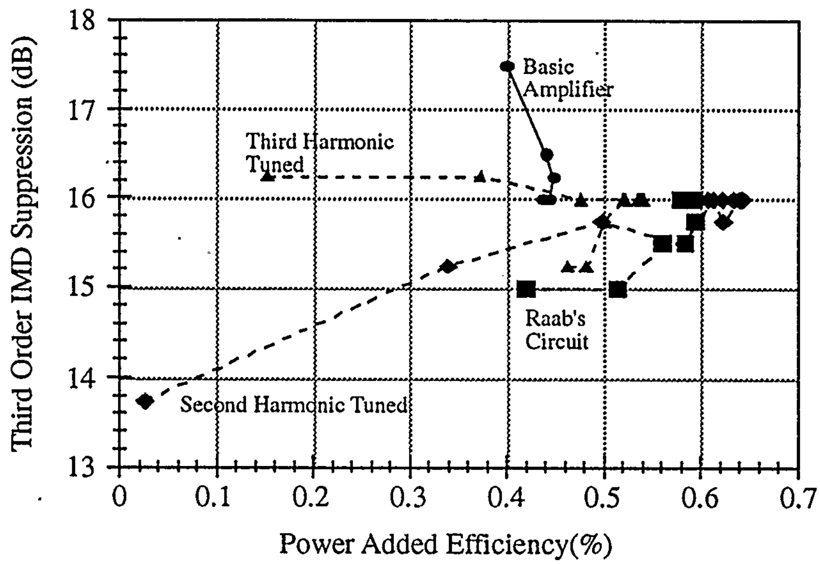


Figure 6.2.4 Third Order Intermodulation Variation For 17 dBm Input

To achieve good linearity and PAE, second harmonic tuning appears to be the best circuit configuration. For the best performance at high power levels third harmonic tuning may also be of value. Raab's circuit does not outperform either of the single harmonic tuned circuits.

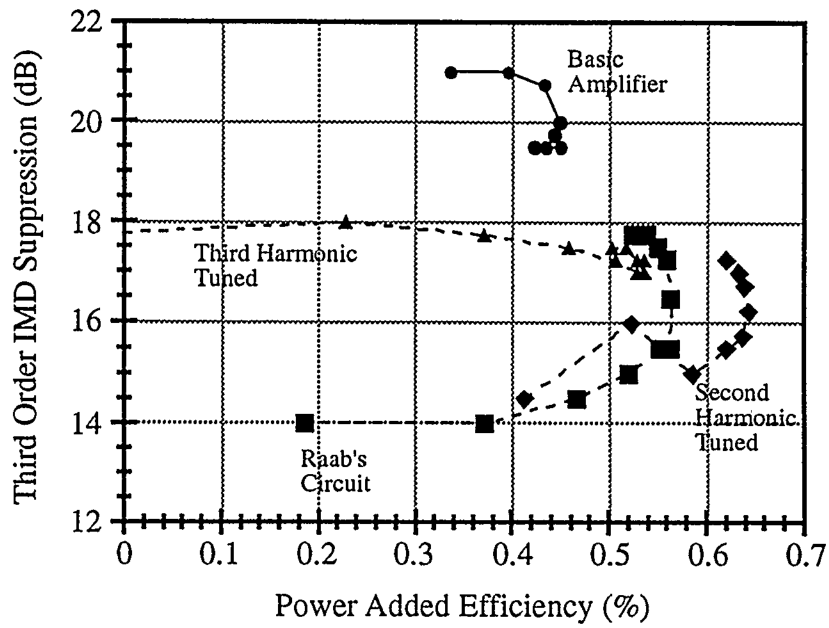


Figure 6.2.5 Third Order Intermodulation Variation For 20 dBm Input

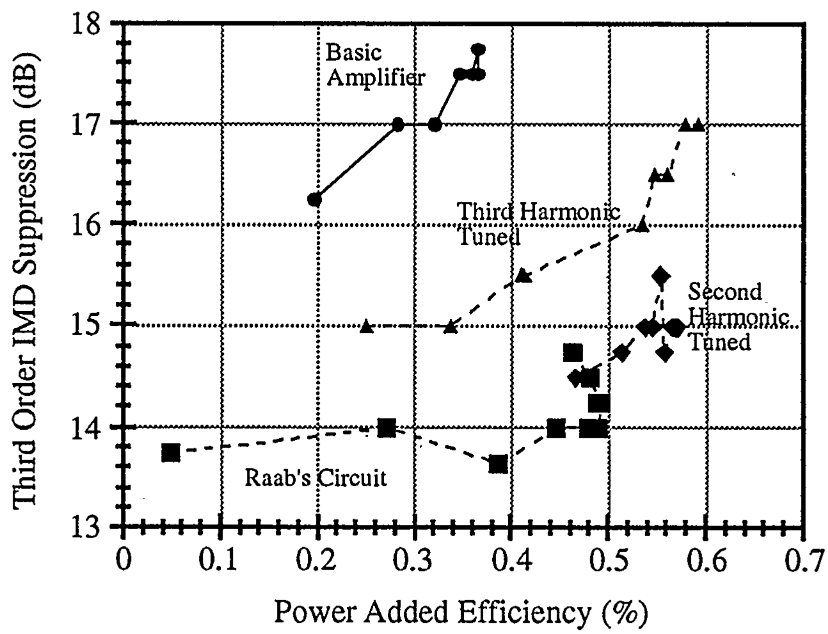


Figure 6.2.6 Third Order Intermodulation Variation For 23 dBm Input

6.3 Comparison of Three Approaches to Harmonic Tuning

The measurements presented here are not as accurate as those of chapter 5 for the following reasons. As described earlier the impedance mismatch between the signal generator and the amplifier input resulted in high, uncharacterisable harmonic input levels. Also, the measurements do not allow for loss in the variable length transmission line and harmonic filter. Gain and efficiency would be even more attractive in comparison to the basic amplifier if more efficient lines and filters are used. Finally, output power due to harmonic components is not subtracted from the total; gain and PAE are therefore overestimated.

Measurements of the untuned amplifier are taken without a fundamental frequency filter at the active device. This omission resulted in increased harmonic output and decreased the useful fundamental output. As shown in Chapter Four this decrease is not as severe as it could be, in that PAE and gain are measured with regard to total output power. The decrease in performance was not measured with the real circuit but may be inferred from simulation results comparing the PAE between untuned circuits operating with and without a fundamental filter at the collector. Fig 4.3.5 presents simulated data for such circuit operations at 5 Volts. PAE is presented based on the desired fundamental output alone and also based on the total power output. Ideally, the elimination of the collector filter should not reduce the PAE considering total power output. In the figure, the unfiltered basic amplifier performance is much closer to that of the filtered circuit when total power is considered. It is still less efficient, because the transistor and circuit performance is reduced at the harmonic frequencies.

While it is not accounted for, the effects of waste harmonic power are indicated by table 6.3.1, which presents the weakest suppression (highest harmonic levels) of the second and third harmonics, relative to the desired output. In many cases the average level of suppression was much greater than in these worst cases. Harmonic levels more than 13 dB below the fundamental may be neglected for the most part; with this threshold it may be seen that for all of the amplifier circuits and power levels the untuned amplifier has the weakest second harmonic suppression, while third harmonic suppression exceeds 13 dB in all the circuits except the one using the second harmonic. Calculation of gain, collector efficiency or PAE using only the fundamental output power will tend to favor the class F circuits even more highly.

Subject to these qualifications, a detailed comparison of untuned and harmonic tuned amplifiers is presented in fig 6.3.1. The tuned circuits measured used the second harmonic, third harmonic and Raab's approach; all were tuned for best PAE at a 5 Volt supply and three power levels; the supply voltage was then varied without other adjustment.

Table 6.3.1 Harmonic Suppression Comparison

Amplifier Tuning Circuit	Input Power (dBm)	Worst Second Harmonic Suppression (dB)	Worst Third Harmonic Suppression (dB)
Basic Amplifier	20	9.5	23.5
	23	6	17.5
	26	6	16
Third Harmonic	20	11.5	24
	23	7	28.5
	26	6	16.5
Raab's Circuit	20	25	23
	23	25	15
	26	29.5	13.5
Second Harmonic	20	36	18
	23	19	11
	26	14.5	9

Inspection of the figure reveals several consistent traits. It may be seen that the untuned amplifier is significantly less efficient than any of the tuned circuits. As expected, second harmonic tuning is the best over the input powers considered, while third harmonic tuning is increasingly good at higher power levels. This is in accordance with the discussion in 6.2.

Raab's circuit outperforms the untuned amplifier, but is the least effective of the high efficiency circuits. It is possible that the actual tuning of Raab's circuit is more critical than the others, in that its relative performance is much better at the supply voltage for which the tuning adjustments were performed than elsewhere. This is clearest at higher power levels because Raab's circuit will also benefit from the higher odd harmonic levels associated with amplifier saturation.

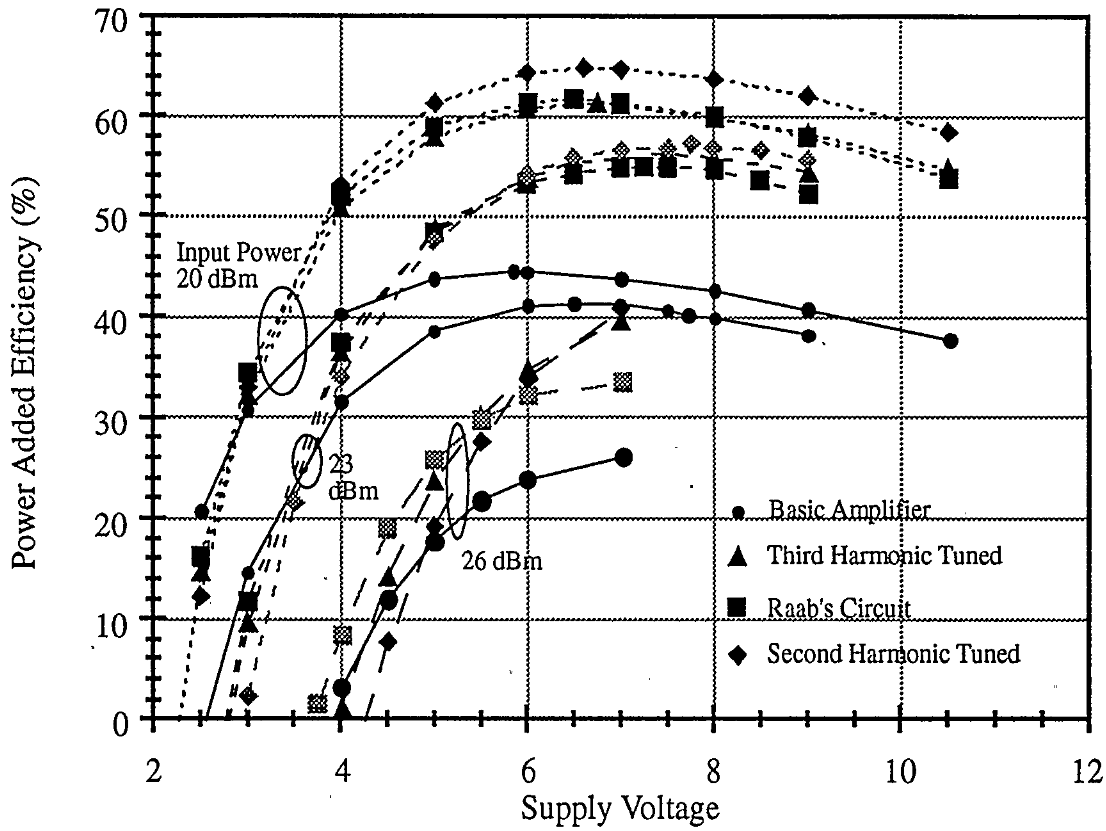


Figure 6.3.1 PAE Variation With Tuning Method and Supply at Three Power Levels

CHAPTER SEVEN

CONCLUSIONS

This work has shown experimentally that class F operation (harmonic tuning) may be used to increase the efficiency of radio power amplifiers. In that a large part of the power supplied to a transceiver is used in the power amplifier stages, this approach could be used to raise the efficiency of radio communication systems as a whole.

Chapter One introduces some basic concepts, including the desirability of high efficiency operation, the traditional classes of amplification and a brief history of class F amplification. An argument is presented in favor of the use of power added efficiency (PAE) instead of collector efficiency, η_C, as a means of describing amplifier performance.

Chapter Two compares Raab's fundamental class F circuit (1, 4) and the more usual approaches involving only the second or third harmonic. While Raab's circuit is attractive, it requires higher order harmonics than either of the others and is therefore expected to require a more costly transistor than approaches based on low harmonics. Inspired by the limitations of second or third harmonic class F operation there follows a description of how an optimal combination of second and third harmonics may be used to achieve collector efficiencies exceeding 99%. This result assumes a half sinusoidal collector current pulse but should allow comparable performance for similar pulse shapes such as a raised cosine. The harmonic levels may be recalculated if a radically different current pulse is to be used.

As well as raising efficiency it is shown that class F operation also reduces supply voltage requirements. While a basic amplifier requires a 1 Volt supply to produce a 1 Volt peak output (neglecting saturation effects) a second harmonic class F circuit generates the same output with a 0.72 Volt supply. By using the best combination of the second and third harmonics the supply requirement for the same output is reduced to 0.63 Volts. A method is given to calculate collector efficiency for any combination of fundamental, second and third harmonic voltages and a half sinusoid current pulse.

Chapter Three describes the experimental equipment built for this work. It includes a narrowband 35 Watt amplifier, a low power broadband amplifier, a transmission line multiplexer and several LC filters and variable length transmission lines. Test instruments connected through the IEEE 488 interface bus to a GPIB computer were used to report transistor power dissipation, PAE and other circuit parameters.

Measurements of fundamental and harmonic inputs to the transistor revealed that high standing waves at the harmonics existed between the signal generator and the transistor. This reduced a number of data readings that would have appeared throughout the work to solely qualitative value; some of these are reported in chapter six. The undesired harmonics were reduced through the insertion of an attenuator. It was found that relatively small attenuation levels could significantly reduce the harmonic standing waves. While higher attenuation levels further reduce the harmonics it is shown that this is not required.

Because it is difficult to measure waveforms directly in a radio frequency circuit, simulation was employed to gain information about circuit waveforms and operation. PSpice transistor parameters were measured when practical, while the remainder were approximated through a linear simulation program which contained both a random and a gradient based optimizer. The optimizer tendency to converge to different solutions from similar start approximations was reduced by combining the results of many sequences of optimization. A much better approach would have been to apply a large signal, non-linear simulator and optimizer to the problem.

Chapter Four details the performance of the experimental, unmodified, class B amplifier. To account for imperfect match conditions PAE and gain are reported with regard to the actual power accepted through the amplifier input. Comparing operation with and without the input harmonic standing voltages, slightly better performance is seen with the harmonic levels attenuated. The harmonics seem to have achieved a form of uncontrolled class F operation in that the circuit gain was higher with the harmonics, while the collector efficiency was lower; the net effect was reduced PAE.

Measurement and simulation results of a second harmonic tuned class F amplifier are given in Chapter Five. Adjusting the second harmonic termination at the input (input tuning) is found to be ineffective. The adjustment procedure for tuning the output or for both input and output tuning is given, and measured values of gain, collector efficiency and PAE are compared. Tuning the input and output yields higher gain than tuning only the output but it also yields lower collector efficiency. This is similar to the comparison in Chapter Four between untuned amplifier operation with and without suppression of input harmonics due to the signal generator mismatch. Similar maximum values of PAE are found in both double tuned and output tuned circuits, though tuning on both sides is less sensitive to input power and supply levels. Simulation results compare second harmonic tuning at the output to an unmodified amplifier with a collector fundamental filter. This is in contrast to the physical measurements, in which the amplifier has no collector filter. Positive results here confirm that class F operation does outperform a similar class B circuit in gain, collector efficiency and PAE.

Chapter Six contains measurements which may be influenced by undesired harmonic input levels. These results are included for their qualitative value. The class F amplifiers under comparison use the second harmonic, third harmonic and Raab's quarter wave transmission line circuit (1, 4). The untuned reference amplifier has no fundamental collector filter. Using a two tone IMD test, at low power levels second harmonic tuning had the highest PAE; for higher levels third harmonic tuning improved but was still less effective than either the second harmonic or Raab's circuit. Comparing average third order IMD terms, third harmonic tuning is slightly more linear than second at peak PAE. Raab's circuit did not exceed either of the others in PAE or linearity. The basic amplifier is more linear than any of the tuned circuits. For operation at a single frequency, detailed comparison of the three class F circuits and the untuned amplifier operating at three power levels shows that second harmonic tuning outperforms the other tuned modes and the basic amplifier, though third harmonic tuning is increasingly effective as input power rises. Raab's circuit exceeds the basic amplifier but is not as effective as the other tuned circuits.

Future work could pursue two lines, physical and simulated. Physical measurements could be taken with greater characterization of loss in transmission lines and filters so as to indicate more truly the efficiency of class F operation. Actual measurements of an untuned amplifier with a collector filter would also ensure fair comparison. Under simulation, a more powerful nonlinear simulator with an optimization routine could be used to find the length of transmission line required between the amplifier and harmonic filter. Finding this length manually was time taking; based upon a limited number of trials the best operating point may not have been found herein. In addition, an RF simulator based on the harmonic balance method would be much faster than the present version of PSpice employed, especially for IMD simulation.

To summarize, second harmonic tuning and to a lesser extent third harmonic tuning and Raab's circuit have been shown to exhibit superior gain, collector efficiency and PAE in comparison with a standard class B amplifier. These techniques may be researched further, but are ready for use in practical RF circuits now.

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Appendix 1

PSPICE Transistor Model Parameters

Table A1.1 SPICE Parameter Values

Parameter Symbol	Description	Default	Value	Source of Value
IS	p-n saturation current	1e-16 A	1.045e-15 A	best fit Shockley equation to measured data
BF	forward Beta	100	89.6	best fit to measured data
NF	fwd current emission coefficient	1	1.057	best fit Shockley equation to measured data
VAF	fwd Early voltage	infinite V	29.55 V	average over beta measurements
IKF	fwd Beta high current rolloff	infinite A	infinite A	default - hard to distinguish from temperature effects
ISE	B-E leakage saturation current	0 A	6.5e-13 A	best fit to measured data
NE	B-E leakage emission coefficient	1.5	2.140	best fit to measured data
BR	reverse Beta	1	13.	measured on curve tracer
NR	rvs current emission coefficient	1	1	default
VAR	rvs Early voltage	infinite V	4.256 V	from curve tracer measurements
IKR	rvs Beta high current rolloff	infinite A	98.20 mA	from curve tracer measurements
ISC	B-C leakage saturation current	0 A	7.350e-16 A	best fit Shockley equation to measurements
NC	B-C leakage emission coefficient	2.0	1.036	best fit Shockley equation to measurements
RB	max base resistance	0 Ohm	1.0 Ohm	optimizer results fit to linear current relationship
RBM	min base resistance	RB	0.0857 Ohm	optimizer results fit to linear current relationship
IRB	current at which base resistance is the avg of RB & RBM	infinite A	21.17 mA	optimizer results fit to linear current relationship
RE	emitter ohmic resistance	0 Ohm	0.7990 Ohm	curve tracer measurement
RC	collector ohmic resistance	0 Ohm	0.2164 Ohm	curve tracer measurement
CJE	B-E zero bias junction capacitance	0 F	8.6 pF	measured

VJE	B-E built in potential	0.75 V	1.438 V	calculated from measurements
MJE	B-E p-n grading factor	0.33	0.3473	calculated from measurements
CJC	B-C zero bias junction capacitance	0 F	3.6 pF	interpolated from Motorola data
VJC	B-C built in potential	0.75 V	0.830 V	calculated from Motorola data
MJC	B-C p-n grading factor	0.33	0.358	calculated from Motorola data
XCJC	fraction of Cbc internal to Rb	1	1	default and simplified model
CJS	collector-substrate zero bias junction capacitance	0 F	0.2306 pF	average of optimizer best fit results
VJS	collector-substrate built in potential	0.75 V	0.75 V	default
MJS	collector-substrate p-n grading factor	0	0	default
FC	fwd bias depletion capacitor coefficient	0.5	0.5	default
TF	ideal forward transit time	0 S	13.21 pS	best fit of diffusion capacitance from optimizer
XTF	transit time bias dependence coeff.	0	0	default
VTF	transit time dependency on Vbc	infinite V	infinite V	default
ITF	transit time dependency on Ic	0 A	0 A	default
PTF	excess phase	0 degree	0 degree	default
TR	ideal reverse transit time	0 S	0 S	default
EG	bandgap voltage	1.11 eV	1.11 eV	default
XTB	Beta temperature coefficient	0	0	default
XTI	Is temperature effect exponent	3	3	default
KF	flicker noise coefficient	0	0	default
AF	flicker noise exponent	1	1	default

Appendix 2

Second Harmonic Tuned PSPICE Circuit Model

```
Second Harmonic tuning circuit model - large signal
* nodes: (10) Vin
*         (60) base
*         (70) collector
*          (100) harmonic filter, load
*         (110) DC Supply

vin 5 0 0 sin(0 5.3 4e8)
rin 5 10 50
Txlnin1 10 0 20 0 zo=50 td=306.67e-12
Txlnin2 20 0 30 0 zo=32 td=238.4e-12
cinblk 30 40 68e-12
Txlnin3 40 0 50 0 zo=12 td=586.5e-12
lbias 50 0 150e-9
Txlnin4 50 0 60 0 zo=12 td=170.3e-12
lb 60 65 1.2213e-9
q1 67 65 69 transistor
le 69 0 .96803e-9
lc 70 67 .51168e-9
Ll 110 70 250e-9
* ll & cl make up a fundamental filter at the collector
*ll 110 70 19.89437e-9
*cl 110 70 7.957747e-12
Txlnout1 70 0 80 0 zo=88.08 td=190.5e-12
Cblk 80 90 68e-12
Txlnout2 90 0 100 0 zo=50 td=330.e-12
* lf & cf make up a series tuned filter to ground at the second
harmonic
lf 100 105  9.947184e-9
cf 105 0    3.978874e-12
rl 100 0 50
Vcc 110 0 5.00
.OPTION ITL5=500000
.TRAN 100ps 200ns 100ns
.FOUR 4e8 V(60) I(LB) V(100) V(70)
.PROBE v(10) i(vin) i(lbias) v(50) v(60) v(65) v(70) v(69) v(67) i(ll)
    + v(110) v(100) i(rl) i(lb) i(lc) v(5) v(30) v(40) i(le) i(vcc)
```

```
.MODEL TRANSISTOR NPN IS=1.045E-15 BF=89.6 NF=1.05714
    + VAF=29.550 ISE=6.5E-13 NE=2.14 BR=13. VAR=4.256
    + IKR=.0982 ISC=7.3504E-16 NC=1.03586
    + RB=1. RBM=.085699 IRB=.02117 RE=.7990 RC=.2164
    + CJE=8.6pF VJE=1.438 MJE=.3473
    + CJC=3.6pF VJC=.830 MJC=.358 XCJC=1. CJS=.23057pF
    + TF=13.21pS
.WIDTH OUT=80
.END
```

Appendix 3

Intermodulation Characteristics of Several Harmonic Tuned Circuits

In Section 6.2 only the averaged third order intermodulation terms were presented. Third, fifth and seventh order terms were measured and are presented here in full. As was also noted earlier, these measurements were taken with a high, unmeasured level of harmonic signal content at the amplifier input due to an impedance mismatch between the signal generator and the input. The upper and lower IMD terms are as identified in fig A3.1

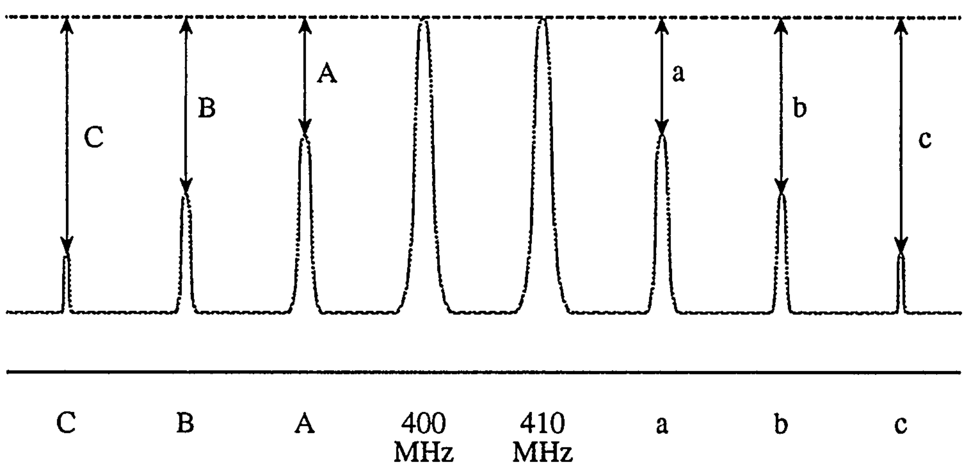

Figure A3.1 Intermodulation Suppression

Table A3.1 Untuned Amplifier IMD Characteristics

Supply Voltage	Input Power (dBm)	Gain (dB)	Collector Efficiency (%)	PAE (%)	C	B	A	a	b	c
5.003	17.24	3.78	68.3	39.8	22.5	20	18	17	22.5	31.5
6.500	17.19	5.13	63.3	43.9	24	20	16.5	16.5	23.5	33.5
7.001	17.22	5.49	62.2	44.7	24	20	16	16.5	23.5	34
8.000	17.23	6.08	58.7	44.3	24.5	20	16	16	24	35
9.000	17.24	6.59	55.6	43.6	25	20.5	16	16	24	35
4.999	20.31	2.95	67.7	33.6	23.5	22	22	20	26	31
6.001	20.36	3.99	65.8	39.5	24	22	22	20	26	31.5
7.001	20.32	4.85	64.2	43.2	24	21.5	21.5	20	26	32
8.001	20.32	5.58	61.9	44.8	24	21	20	20	26	32.5
9.501	20.56	6.36	57.4	44.2	24.5	21.5	21	18.5	25	31
10.003	20.39	6.79	57.2	44.9	25	20.5	19.5	19.5	24	33
10.998	20.53	7.05	54.1	43.4	25	21.5	20.5	18.5	25	31
12.001	20.51	7.44	51.6	42.2	25.5	21.5	20	19	25	31
5.001	23.64	1.79	60.2	19.5	20.5	37	17	15.5	28	25.5
6.003	23.69	2.81	59.1	28.2	21	32	18	16	29	26.5
6.999	23.77	3.59	56.8	32.0	22	33	18	16	27	26
8.004	23.75	4.39	55.1	34.6	22.5	30	18	17	27.5	26.5
9.004	23.35	5.07	52.8	36.4	24	30	18	17	26.5	26
10.000	23.35	5.53	50.5	36.4	24	29	18	17.5	27	26
10.501	23.36	5.71	49.1	35.9	24	28	18	17	27	26.5

Table A3.2 Third Harmonic Tuned Amplifier IMD Characteristics

Supply Voltage	Input Power (dBm)	Gain (dB)	Collector Efficiency (%)	PAE (%)	C	B	A	a	b	c
3.001	17.29	0.87	84.1	15.1	20	19.5	16.5	16	21	28.5
4.006	17.29	2.67	80.5	37.1	20.5	19	16.5	16	21	28
5.000	17.27	4.07	77.8	47.4	21.5	18.5	16	16	20.5	28
6.000	17.25	5.17	74.6	52.1	22	19	16	16	20.5	28.5
7.003	17.15	6.06	71.3	53.6	23.5	19	16	16	20.5	30
7.753	17.22	6.59	69.2	54.0	24	19	16	16	20.5	31
8.002	17.17	6.75	68.4	54	24	19	16	16	20.5	32
8.254	17.21	6.88	67.7	53.8	24	19.5	16	16	20.5	32
9.009	17.19	7.32	65.3	53.3	24.5	19.5	16	16	21.5	33
10.000	17.18	7.79	62.2	51.9	26	20	16	16	21.5	34
11.001	17.2	8.17	59.0	50.0	26	20	15.5	16	22	34.5
12.005	17.19	8.59	56.0	48.1	26	20	15	15.5	22	35
13.003	17.17	8.77	53.2	46.1	26.5	21	15	15.5	22.5	34.5
3.000	20.08	-0.22	77.9	-3.9	22.5	26	18	17.5	25	26
4.001	20.08	1.56	75.5	22.8	22.5	24.5	18	18	25.5	27
5.001	20.08	2.97	74.9	37.1	22.5	23.5	17.5	18	24.5	27.5
6.008	20.04	4.13	74.3	45.7	22.5	22	17	18	24.5	27.5
7.003	19.98	5.09	73.1	50.5	22.5	22	16.5	18	24	28
8.000	19.99	5.87	71.1	52.8	23	21.5	16.5	17.5	24.5	28
9.005	19.99	6.54	68.8	53.6	23.5	21	16.5	18	24	28
9.500	19.99	6.83	67.6	53.6	23.5	21	16.5	17.5	24	28
10.002	19.97	7.13	66.5	53.6	24	20.5	16	17.5	24	28
11.000	19.94	7.63	63.9	52.8	24	20.5	17	18	24	29
12.000	19.92	8.06	61.2	51.7	24.5	20.5	17	18	24	29
13.001	19.94	8.43	58.7	50.2	24.5	20.5	17	18	24	29
7.001	23.21	1.94	69.7	25.0	26	22	14	16	24	32
8.002	23.15	2.91	69.1	33.6	26	22	14	16	24	32
9.000	23.14	3.82	69.7	40.9	27	22	15	16	25	32
10:00	23.16	4.62	70.8	46.2	27	22	15	16	26	32

11.04	23.05	5.52	74.1	53.4	28	22	15	17	26	32
11.51	23.01	5.89	73.8	54.7	28	22	16	17	26	31
12.00	23.07	6.19	74.1	56.0	28	22	16	17	26	33
13.00	23.06	6.63	74.0	57.8	29	22	16	18	27	34
14.00	23.08	7.09	73.6	59.2	30	22	16	18	28	34

Table A3.3 Raab's Circuit IMD Characteristics

Supply Voltage	Input Power (dBm)	Gain (dB)	Collector Efficiency (%)	PAE (%)	C	B	A	a	b	c
5.002	17.46	2.96	84.9	41.8	22	19	14	16	23.5	28
6.002	17.42	4.29	81.7	51.3	22	18.5	14	16	22.5	29
7.011	17.41	5.38	78.9	56.0	22	18	15	16	22	30
8.003	17.36	6.32	76.1	58.3	22	18	15	16	22	30.5
9.001	17.38	7.09	73.6	59.3	22	18	15.5	16	22	31.5
10.00	17.41	7.74	71.2	59.2	22	18	16	16	22	32
11.00	17.35	8.33	68.8	58.6	22	18	16	16	21.5	32.5
12.00	17.35	8.84	66.4	57.8	22	18	16	16	22	34
4.006	20.31	1.05	86.7	18.6	32	24	13	15	28	24.5
5.001	20.31	2.61	81.7	37.1	28	28	12.5	15.5	29	24
6.001	20.32	3.88	78.6	46.5	27	28	13	16	30	25
7.000	20.29	4.96	76.4	52.0	26	26	14	16	31	25
8.000	20.38	5.85	74.4	55.1	26	26	14	17	31	26
8.999	20.35	6.56	72.1	56.2	26	25.5	14	17	31	26
10.001	20.35	7.17	69.7	56.3	26	25.5	15	18	30.5	26.5
11.001	20.37	7.69	67.4	55.9	26	25	16	18.5	30	27
12.000	20.31	8.15	64.8	54.9	26	24.5	16	19	29	18
13.001	20.39	8.56	62.4	53.8	26	24.5	16	19.5	29	28
14.002	20.28	8.92	60.0	52.4	26	24	16	19.5	29	29
3.999	23.27	0.27	82.8	4.81	29.5	25	13.5	14	21	24
5.000	23.2	1.89	77.2	27.1	28	28	14	14	22	22
5.995	23.14	3.21	73.8	38.6	26	28	13.8	13.5	23	22
6.967	23.09	4.24	71.5	44.6	26	28	14	14	25	24
8.00	23.05	5.13	69.1	47.9	26	27.5	14	14	26	26
8.795	23.08	5.67	67.1	48.9	26	27	14	14	27.5	26
9.00	23.06	5.81	66.5	49.1	26	27	14	14.5	28	27
10.004	23.07	6.36	63.6	48.9	26	26	14	14.5	29	28
11.003	23.05	6.85	60.4	48.0	26	25.5	14	15	30	28
12.001	23.02	7.21	57.3	46.3	26.5	25	14	15.5	30	28

Table A3.4 Second Harmonic Tuned Amplifier IMD Characteristics

Supply Voltage	Input Power (dBm)	Gain (dB)	Collector Efficiency (%)	PAE (%)	C	B	A	a	b	c
3.001	17.23	0.17	97.3	2.44	20	19.5	13.5	14	20.5	29
4.000	17.22	1.98	91.8	33.8	19	19	16	14.5	20.5	28
5.003	17.16	3.69	88.6	49.7	19	18	16	15.5	20	28
6.004	17.09	4.92	85.7	58.2	19	18	15	16	20	28
7.015	17.05	6.03	82.9	62.2	19.5	18	15.5	16	20	28
8.002	17.01	6.93	80.2	63.9	19.5	18	16	16	20	28
9.002	17.00	7.69	77.5	64.2	20	18	16	16	20	28
10.002	17	8.33	75.1	64.1	20	18	16	16	19.5	28.5
10.998	16.98	8.90	72.7	63.2	20	17.5	16	16	19	28
12.000	16.97	9.49	70.2	62.1	21	18	16	16	19.5	29
13.003	16.96	9.82	67.8	60.7	21.5	17.5	16	16	19.5	29.5
5.000	20.04	2.69	88.9	41.2	24	22.5	13.5	15.5	23.5	27
6.000	20.02	4.01	86.8	52.2	24	23	16	16	24	28
7.006	20.01	5.19	84.6	58.5	23.5	22.5	14	16	24.5	28.5
8.001	20	6.01	82.7	62.0	23.5	22	14.5	16.5	25	29
9.003	19.94	6.81	80.4	63.6	23	21.5	14.5	17	25	29.5
10.002	19.93	7.48	78.2	64.3	23	21	15	17.5	25.5	30
11.004	19.95	8.05	75.8	63.8	23	21	15.5	18	26	30.5
12.010	19.92	8.56	73.4	63.2	23	20.5	16	18	26	31
13.001	19.93	8.99	71.0	62.0	23	20.5	16	18.5	26	31.5
7.016	22.99	4.02	77.0	46.5	26.5	24	14	15	24	26
8.000	22.99	4.90	75.8	51.3	26.5	23	14	15.5	26	27.5
9.003	23.13	5.58	74.1	53.7	27	23	14.5	15.5	25	26.5
9.428	23.12	5.86	73.6	54.5	26.5	22.5	14.5	15.5	25.5	26.5
10.009	23.06	6.08	73.9	55.7	26	22	14	15.5	26	30
11.000	23.07	6.65	72.4	56.8	26	22	14	16	26.5	31
12.006	23.04	7.19	70.6	57.0	26	22	14	16	28	32
12.501	23.02	7.41	69.5	56.9	26	22	14	16	28	32
13.004	23.01	7.64	68.3	56.5	26	21.5	14	16	28	32