

THE UNIVERSITY OF CALGARY

A Novel Four-Quadrant CMOS Analog Multiplier/Divider

by

Gang Li

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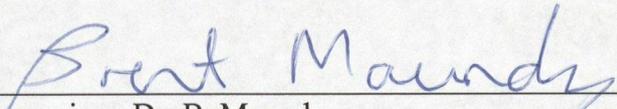
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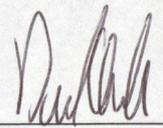
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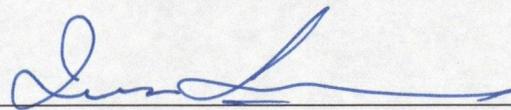
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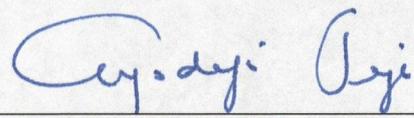
Supervisor, Dr. B. Maundy,
Dept. of Electrical and Computer Engineering.



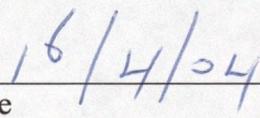
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Dept. of Electrical and Computer Engineering.



Dr. I. Finvers,
Dept. of Electrical and Computer Engineering.



Dr. A. Jeje,
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Date

Abstract

Recently, a number of analog multipliers based on the square-law model of the metal-oxide-silicon (MOS) transistor operating in the saturation region have been presented.

This thesis presents a novel four-quadrant complementary metal-oxide-silicon (CMOS) analog multiplier/divider circuit using the 3.3V, 0.18 μ m CMOS process of Taiwan Semiconductor Manufacturing Company Ltd (TSMC) based on the square-law model of the MOS transistor. The proposed analog multiplier/divider uses two newly-proposed analog multipliers, a negative feedback path and a common-mode feedback (CMFB) circuit to realize the following transfer function: $W=(K_2-K_1)*(X_2-X_1)/(Z_2-Z_1)+Y_1$, where W is the output, $K_{1,2}$, $X_{1,2}$ and $Z_{1,2}$ are differential inputs and Y_1 is a DC bias voltage. Spectre(S) simulation results from a chip design show that the 3dB bandwidth of the analog divider is proportional to the magnitude of input signal (Z_2-Z_1) , and a 3dB bandwidth of 11 MHz is achievable.

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To my wife, Qian.

Contents

Abstract	iii
Acknowledgments	iv
Dedication	v
Contents	vi
List of Tables	ix
List of Figures	x
List of Symbols	xii
CHAPTER 1 INTRODUCTION	1
1.1 Analog Multipliers	1
1.2 Analog Dividers	7
1.2.1 Feedback Technique	8
1.2.2 Conventional Log-Antilog Technique	10
1.2.3 Voltage Variable Resistance (VVR) Technique	11
1.2.4 Pool Circuit Technique	12
1.3 The Proposed Analog Multiplier/Divider	15
CHAPTER 2 A NEW MULTIPLIER/DIVIDER	18
2.1 MOS Transistor Static Modelling	18
2.2 Analog Adder	20
2.3 Analog Multiplier	22
2.4 Analog Divider	23

2.5 Operational Amplifier	25
2.6 Common Mode Feedback Circuit	30
2.7 Threshold Voltage Referenced Self-Biasing	32
2.8 The Complete Analog Multiplier/Divider	35
CHAPTER 3 CIRCUIT ANALYSIS	39
3.1 The Range of Input Signals	39
3.2 Small Signal Analysis	40
3.3 Noise Analysis	41
3.4 High frequency Characteristics of The Analog Divider	42
CHAPTER 4 SECOND ORDER EFFECTS	45
4.1 Basic Idea of Second Order Effects	45
4.2 Threshold Voltage Variation	46
4.3 Bulk Effects	46
4.4 Channel-Length Modulation	47
4.5 Mobility Degradation	48
4.6 Mismatch Effects	49
CHAPTER 5 SIMULATION AND EXPERIMENTAL RESULTS	52
5.1 Simulation Results	52
5.1.1 DC Sweep	52
5.1.2 AC Sweeps	53
5.1.3 Transient Analysis	54
5.2 Experimental Results	57
5.2.1 Differential Signals Generator	57
5.2.2 Chip Test Bench	59
5.2.3 Experimental Data Analysis	60

5.2.4 The Correction to CMFB Circuit	63
CHAPTER 6 CONCLUSION AND FUTURE WORK	69
6.1 Summary	69
6.2 Contribution	70
6.3 Future Work	70
REFERENCES	72

List of Tables

Table 2.1 Transistor sizes used in Fig. 2.6	28
Table 2.2 Transistor sizes used in Fig. 2.10	35

List of Figures

1.1 Basic idea of multiplier	4
1.2 Divider circuit (A) using a multiplier in the feedback path of an op-amp	9
1.3 Divider circuit (B) using a multiplier in the feedback path of an op-amp	9
1.4 Divider using log-ratio and anti-log circuits	10
1.5 The basic scheme of a divider circuit using the VVR property of a MOSFET	11
1.6 The pool circuit proposed by Tsay and Newcomb in [33]	13
1.7 The proposed CMOS divider in [32]	13
2.1 The adder circuit proposed in [10]	20
2.2 An all PMOS transistor adder circuit	21
2.3 (a) The proposed analog multiplier	22
2.3 (b) The equivalent block diagram	23
2.4 The simplified block diagram of the multiplier/divider	24
2.5 Block diagram of a basic two-stage CMOS op-amp	26
2.6 Two-stage CMOS operational amplifier with class-AB output stage	28
2.7 Circuit used to measure open-loop gain and frequency response	29
2.8 The simulated AC magnitude and phase response of the designed op-amp	30
2.9 Voltage divider implementations in CMOS	32
2.10 Threshold reference self-biasing circuit with startup circuit	33
2.11 Two possible operating points of self-biased circuit	34
2.12 The complete schematic of the analog multiplier/divider (without biasing circuitry)	36
2.13 Using two complementary transistors to replace a resistor	37

3.1 Small signal equivalent of adder circuit	40
3.2 Noise equivalent of the adder circuit	42
5.1 Simulation result of DC sweep over Y_1 for W	53
5.2 Simulation result of AC sweep over X_2-X_1 for $Z_2-Z_1=0.1V$	53
5.3 Simulation result of AC sweep over X_2-X_1 for $Z_2-Z_1=0.05V$	54
5.4 Simulated output waveform for multiplication	55
5.5 FFT results of the multiplication output waveform W	55
5.6 Simulated transient response for the divider function	56
5.7 Matlab simulation results of the division operation	56
5.8 The layout of the new multiplier/divider	57
5.9 Differential signals generator	58
5.10 The chip test bench	59
5.11 The designed PCB for testing ICFCYDIV	60
5.12 (a) The measured waveform of output node W	61
5.12 (b) The measured waveform of internal node V_{cm}	61
5.13 The simulated waveforms of W and internal node V_{cm} under stability test (old CMFB circuit)	62
5.14 The circuit used to test loop gain response of the original CMFB circuit	63
5.15 The loop gain response of the original CMFB circuit	64
5.16 The corrected CMFB circuit	65
5.17 The simulated AC magnitude and phase response of the single stage op-amp	65
5.18 The simulated waveforms of W and internal node V_{cm} under stability test (using the new CMFB circuit)	67
5.19 The loop gain response of the corrected CMFB circuit	68

List of Symbols

f_T	Transistor cutoff frequency
f	Transistor operating frequency
W	Transistor channel width
L	Transistor channel length
β_F	Forward current gain of BJT transistors
g	Transconductance of transistors
g_m	Transconductance of MOS transistors
$V_{i(t)}$	Multiplier input voltage
X, Y, Z, K	DC or common mode component
x, y, z, k	AC signal component
K_n	NMOS transconductance parameter
μ	NMOS transistor carrier mobility
C_{ox}	Gate oxide capacitance per unit area
V_t	MOS transistor threshold voltage
V_{tn}	NMOS transistor threshold voltage
V_{tp}	PMOS transistor threshold voltage
A	Operational amplifier DC gain
r_o	Small signal output resistance
V_p	The pinch-off voltage of FET
I_{dss}	The drain saturation current of FET for zero gate bias

λ	Channel length modulation factor
V_{i0}	Zero-bias threshold voltage
γ	Body effect coefficient
I_D	Drain current
V_T	Thermal voltage
n	Subthreshold slope factor
Φ_F	Surface potential
Op Amp	Operational amplifier
CMFB	Common-mode feedback
R_n	NMOS transistor on-resistance
R_p	PMOS transistor on-resistance
V_{ref}	Common-mode reference voltage
k_B	Boltzmann constant
T	Temperature
GBP	Op Amp gain-bandwidth-product
ω_a	Op Amp dominant pole frequency
α	Scaling factor
μ_0	NMOS transistor zero field carrier mobility
t_{OX}	Oxide thickness
E_{CR}	Critical field
θ	Transistor mobility parameter
V_{out}	Output voltage

CHAPTER 1

INTRODUCTION

1.1 Analog Multipliers

A multiplier generates an output i_o proportional to the product of two input signals x and y ,

$$i_o = Kxy \quad (1.1)$$

where K is a multiplication constant with suitable dimension, x and y represent AC or small signals.

Multiplier performance is specified in terms of accuracy and nonlinearity. Accuracy represents the maximum error of the actual output compared with the ideal value predicted by equation (1.1). Nonlinearity represents the maximum output deviation from the best straight line when one input is swept from end to end while the other input is fixed at a constant. A four-quadrant multiplier is a multiplier that accepts bipolar inputs and keeps the correct polarity relationship at the output. By contrast, a single-quadrant multiplier requires that both x and y are unipolar, a two-quadrant multiplier requires that either x or y be unipolar [1].

Analog multipliers are widely applied in analog computation, signal modulation/demodulation, a variety of voltage-controlled functions, and systems such as filters and neural networks as programmable elements [1-2].

Since analog multipliers are very important analog integrated circuits, they have been proposed in a variety of implementations by bipolar junction transistor (BJT) technology, with the popular Gilbert cell as the core in this technology. Gilbert proposed the first high performance four-quadrant multiplier based on the Gilbert cell [3], and achieved an accuracy of 0.1% in a useful frequency range from DC to about 500 MHz. Then Gilbert first used translinear (TL) and the translinear principle (TLP) to analyze large-signal behavior in a class of nonlinear-circuits. The key to TLP is to convert a linear constraint on the base-emitter voltages in a circuit (i.e., Kirchhoff's voltage law) into a product-of-power-law constraint on collector currents flowing in the circuit, through the exponential I_c (collector current) - V_{be} (base-emitter voltage) characteristic of the BJT. From another point of view, this convention is realized through the characteristic that the BJT's transconductance is linear in its collector current [4-7].

Since the late 1970s, the metal-oxide-silicon field-effect transistor (MOSFET) has been widely applied in digital circuits. Although we find that MOSFET is not suitable for analog design in terms of its cutoff Frequency (f_T), DC range of operation and noise performance when comparing with BJT [8], MOS transistors occupy a much smaller silicon area on the IC chip because of their comparatively smaller dimensions, and operate at a much lower supply voltage. A more important factor is that, with today's trends of large-volume technology and the demand for low-voltage and low-power systems [9], MOS is a reasonable choice for the technology of availability. Now the complementary MOS (CMOS) process is the dominant technology in the world, and it has also been applied extensively in the design of analog integrated circuits and mixed-signal circuits.

To date, it is a development trend to integrate entire systems on a single chip. This means that analog circuits will have to coexist on the same substrate along with dominant digital systems. Since CMOS technologies are primarily developed and optimized for digital systems at present, it is not easy to design quality analog circuits through standard CMOS processes for low-cost fabrication, and the key BJT Gilbert cell cannot be implemented by a standard CMOS process. Hence, although high performance BJT multipliers have been available for a long time, the implementation of CMOS multipliers is still necessary and challenging, especially for low-voltage and low-power circuit design.

Implementation of the analog multiplier has successfully been achieved in both bipolar and CMOS technologies, but in this thesis we focus on CMOS implementation. An excellent summary on CMOS multipliers that operate in a multitude of modes such as saturation, triode, and subthreshold region can be found in [1].

It should be mentioned that translinear structures are feasible in principle with CMOS technology by using MOS transistors working in the subthreshold region. From equation (2.5), we note the exponential current-voltage characteristic of the MOS transistor when it operates in the subthreshold region. However, the dynamic range and speed of such circuits would be too low to be practical for general applications.

Therefore, CMOS multiplier structures can be roughly grouped into triode or saturation, according to their MOS operating region, but they all have the same circuit topology as illustrated in Fig. 1.1 [1].

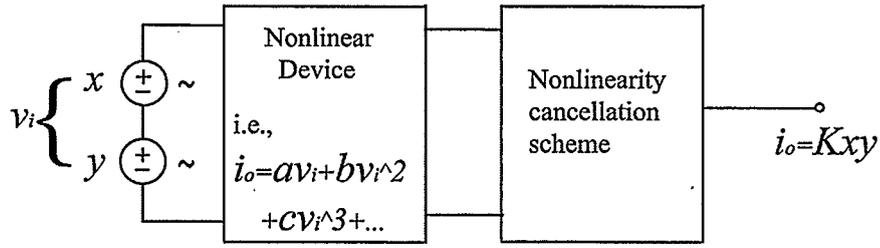


Fig. 1.1. Basic idea of multiplier.

The addition or subtraction of two voltage signals, x and y , are applied as inputs to a nonlinear device (e.g., a MOS transistor). This nonlinear device can be represented by a high-order polynomial function, therefore generating terms like xy , x^2 , y^2 and other higher order items. We know that the item xy is the desired output, and those undesired terms are required to be cancelled. This is usually implemented by a nonlinearity cancellation scheme so as to yield the final output $i_o = Kxy$.

A fully differential input configuration is usually preferred in a multiplier topology so as to achieve a better cancellation of nonlinearities. The differential multiplier has two inputs, x and y , therefore four combinations are derived from these two differential signals, i.e., (x, y) , $(-x, y)$, $(-x, -y)$, and $(x, -y)$.

If MOS transistors are operating in triode region in the multiplier topology, the realization of four-quadrant multiplication and simultaneous cancellation of all the higher order and common-mode components is based on the following equation [1],

$$\begin{aligned} & [(X+x)(Y+y) + (X-x)(Y-y)] \\ & - [(X-x)(Y+y) + (X+x)(Y-y)] = 4xy \end{aligned} \quad (1.2)$$

Here, upper case letters, i.e., X and Y , represent DC or common mode components of the input signals. As we will see later in section 2.1, from the Shichman-

Hodges MOS transistor model, the term $V_{GS}V_{DS}$ in (2.2) can be used to realize equation (1.2).

In [1] more than a dozen of references are mentioned on the subject of triode region multipliers. However, we find that using passive resistors or MOS transistors biased in the triode region will limit the high-frequency operation and accuracy of the multiplier. Moreover, it will also increase the cost, power consumption, and chip area of the multiplier produced. In [1] more than seventy references are cited on the subject of CMOS multipliers operating in saturation region, so operation in saturation mode seems to be preferable to the triode mode to date primarily because there are more options for multiplier topologies that are practical.

If MOS transistors are operating in saturation region in the multiplier topology, the realization of four-quadrant multiplication and simultaneous cancellation of all the higher order and common-mode components is based on the following two equations [1, 10],

$$\begin{aligned} & \{[(X+x)+(Y+y)]^2 + [(X-x)+(Y-y)]^2\} - \\ & \{[(X-x)+(Y+y)]^2 + [(X+x)+(Y-y)]^2\} = 8xy \end{aligned} \quad (1.3)$$

and

$$\begin{aligned} & \{[(X+x)-(Y+y)+V_{bias}]^2 + [(X-x)-(Y-y)+V_{bias}]^2\} - \\ & \{[(X-x)-(Y+y)+V_{bias}]^2 + [(X+x)-(Y-y)+V_{bias}]^2\} = -8xy \end{aligned} \quad (1.4)$$

Here again, upper case letters, i.e., X and Y, represent DC or common mode components of the input signals, and V_{bias} is a DC bias voltage introduced to ensure that all the transistors remain in saturation. As we will see later in section 2.1, from the

Shichman-Hodges MOS transistor model, the term V_{GS}^2 in (2.1) can be used to realize equations (1.3) and (1.4).

In [11-12] two multiplier circuits were proposed with all transistors operating in saturation region. The unique configurations in these circuits also make them possible for low voltage operation. In [11] the method of connecting only two transistors between the power supply and ground allowed low voltage operation. In [12] cross-coupled transistor pairs and floating voltage sources also allowed low voltage operation. In [13-14] sum and difference voltage squaring circuits were used, the multiplication operation was simply realized by the difference of their outputs. Voltage adders and squaring circuits (V_{GS}^2) were also used to realize multiplication with current as the output signal. In these types of multiplier, capacitive adders, resistive adders and active adders were reported as voltage adders [10, 15-17, 18-19], and the performance of the voltage adder directly affects the performance of the multiplier.

One may have noticed that the inputs of the CMOS multipliers are voltage signals based on equations (1.2), (1.3) and (1.4). Yet there is another way to implement CMOS multipliers using current as input signals, and the output is still current signal, e.g., so-called current-mode multipliers [5]. Evert Seevinck further applied the TL concept to the MOS transistor, and developed a systematic technique for the design of CMOS current-mode nonlinear signal processing circuits [20]. When implementing the translinear loop in this case, the main limitation is accuracy because the performance of the resulting circuits is very sensitive to deviations from the simple square-law model of the transistors in saturation, caused by channel-length modulation, mobility degradation and mismatching.

It is usually stated in the technical literature [5, 21-22] that current-mode circuits have wider signal bandwidths, larger dynamic ranges and lower power consumption when they are compared with their voltage-mode counterparts. Since there are no fundamental differences between them from the viewpoint of circuit theory, the only explanation of performance differences between published voltage-mode and current-mode circuits is that they are implemented by different design techniques. Voltage-mode circuits often use higher loop gains than current-mode circuits, and current-mode circuits are often made less complex than the voltage-mode circuits they are compared to at the cost of higher distortion and gain variation [23]. Here we can think about the example of designing an analog multiplier. If one needs to use analog adders or subtractors in the circuit, it is easier to realize in current-mode circuits than voltage-mode circuits. The reason is all that is required in a current-mode circuit is to put signal currents into the same node for addition or subtraction, while we have to design analog adder or subtractor blocks in a voltage-mode circuit.

In this thesis we use voltage signals as inputs. Based on equation (1.3), a modified voltage adder in [10] and the square law drain current, versus gate-source voltage characteristic of the MOSFET in the saturation region is used for the development of a multiplier realization in CMOS technology.

1.2 Analog Dividers

A divider performs analog division. Divider performance is specified in terms of accuracy.

Analog dividers are also important building blocks with wide application in analog computation, fuzzy control, and signal conditioning and processing, particularly in instrumentation areas [2, 24-25]. A typical application of a divider is for linearizing the behavior of certain transducers [26].

Although many sampled-data and switched-capacitor (SC) systems had been used in designing dividers [27-28], they do not yield a directly realizable continuous-time divider circuit and will not be discussed here.

Compared with analog multipliers, analog dividers require more complex circuitry, and there are much less references can be cited on the subject of analog divider realizations. Several research developments on this area are described below. They include the use of the feedback technique [27], the log-antilog technique [29], the voltage variable resistance (VVR) technique [26, 30-31], and the pool circuit technique [32]. The increased complexity and advantages/disadvantages of these realizations are also briefly discussed.

1.2.1 Feedback Technique

A divider can be realized by the feedback technique. Usually the divider consists of a multiplier and an operational-amplifier (op-amp) with or without resistors, as shown in Figs. 1.2 and 1.3. The multiplier circuit is connected between the output and the inverting terminal of the op-amp [27]. Here, K_1 and K_2 are the closed loop gains of each circuit.

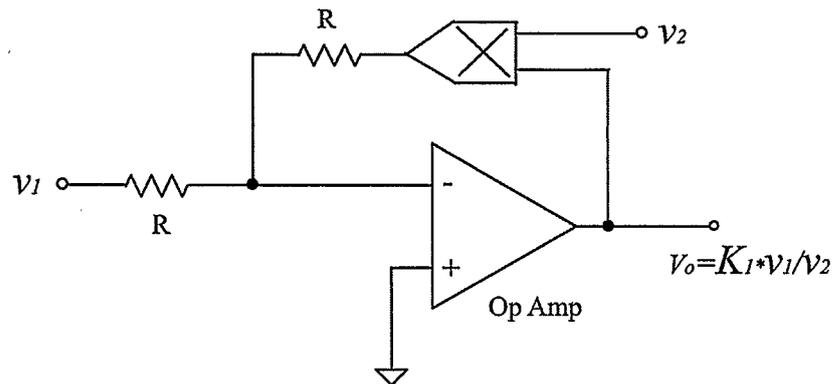


Fig. 1.2. Divider circuit (A) using a multiplier in the feedback path of an op-amp.

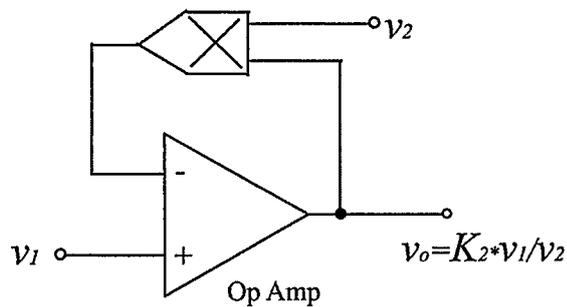


Fig. 1.3. Divider circuit (B) using a multiplier in the feedback path of an op-amp.

Straightforward analysis shows that in both cases $v_o = K_1 \cdot v_1 / v_2$ or $v_o = K_2 \cdot v_1 / v_2$.

The divider circuitry is simple. The performance of these multiplier/dividers depends primarily on the performances of the multiplier and operational amplifier employed. Accuracy is mainly limited by offsets associated with the input and output variables. Using operational amplifiers as building blocks to synthesize the division function will limit the high-frequency operation, as well as the accuracy of the divider.

1.2.2 Conventional Log-Antilog Technique

A divider can be also realized by a conventional log-antilog technique, as shown schematically in Fig. 1.4 [29]. The divider consists of two log circuits, an antilog circuit, an op-amp and four identical resistors, R . Straightforward analysis shows that $v_o = K_3 \cdot v_1 / v_2$, here K_3 is the overall gain of the circuit.

Thus this way of thinking is to transform the division operation of two variables into the subtraction operation of their log function with the help of two log circuits, then to apply an antilog operation with the help of an antilog circuit. Log, log ratio, and antilog circuits are suitable for realization in BJT technology, and they have been implemented into several integrated circuit forms [29].

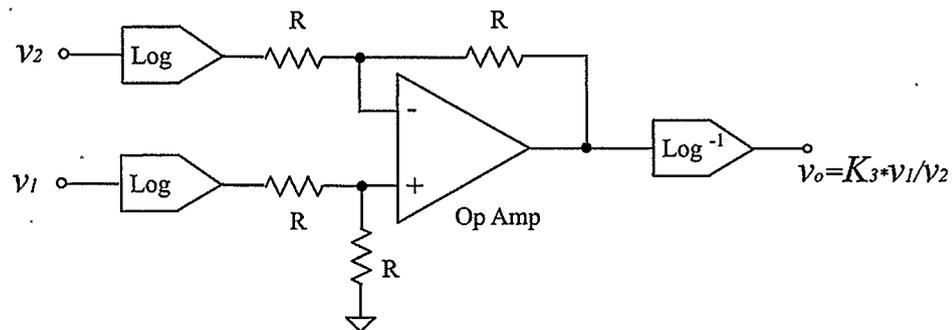


Fig. 1.4. Divider using log-ratio and anti-log circuits.

This technique is relatively complicated to be realized, because it has to use a log ratio network and an antilog circuit. Moreover, it is not suitable to be realized in CMOS technology.

1.2.3 Voltage Variable Resistance (VVR) Technique

Other implementations utilize the voltage variable resistance (VVR) property of a MOS transistor [26, 30-31]. A straightforward realization of the divider by this technique was presented in [26]. The simplest divider scheme with only one op-amp is shown in Fig. 1.5. In this circuit the drain-source conductance g_{ds} of an NMOS transistor (Q1) was used.

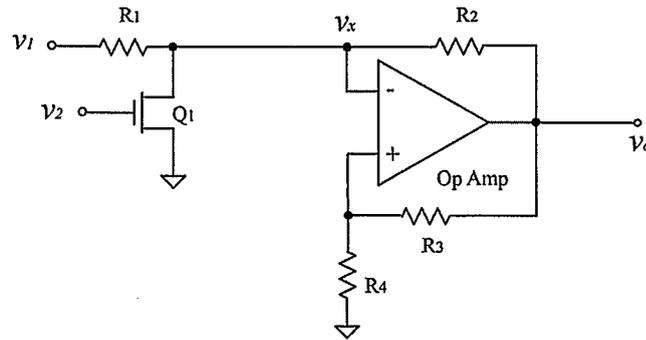


Fig. 1.5. The basic scheme of a divider circuit using the VVR property of a MOSFET.

Here the VVR property of a MOS transistor is that the conductance of Q1 is linear with its gate-source voltage, v_2 [26],

$$g_{ds} = K_1 + K_2 v_2 \quad (1.5)$$

where K_1 and K_2 are two positive constants related to the pinch-off voltage and the drain saturation current of Q1.

If we get further insight into the circuit, a negative resistor, $-R_2 R_4 / R_3$, is implemented from node v_x to ground by the help of the op-amp and resistors R_2 , R_3 , and R_4 . So we utilize this negative resistor to cancel the constant item K_1 in equation (1.5), by making

$$\frac{1}{R_1} + K_1 - \frac{R_3}{R_2 R_4} = 0 \quad (1.6)$$

which is usually met by adjusting R_4 .

Therefore straightforward analysis of the circuit yields the following output voltages,

$$v_x = \frac{1}{K_2 R_1} \cdot \frac{v_1}{v_2} \quad (1.7)$$

and

$$v_o = \frac{1}{K_2 R_1} \left(1 + \frac{R_3}{R_4} \right) \frac{v_1}{v_2} \quad (1.8)$$

which represents the division operation.

The disadvantage of this technique is obvious, because it is not very suitable for implementation in integrated circuit form. The reason is that equation (1.6) is required to be met in order to realize the division operation, and it is difficult to realize accurate resistances (<1%) in the form of integrated circuits.

1.2.4 Pool Circuit Technique

A recently proposed circuit used pool circuits [33] as function blocks to realize the division operation [32].

Fig. 1.6 shows the pool circuit [33], it consists of two standard operational transconductance amplifiers (OTAs). The operation principle of this circuit is explained as following. Assume that all the NMOS transistors in Fig. 1.6 are biased in the saturation region with individual bulks connected to their sources to eliminate the bulk effects, and the transconductance of M_1 - M_4 is equal to g_m . Here I_B is a DC current source.

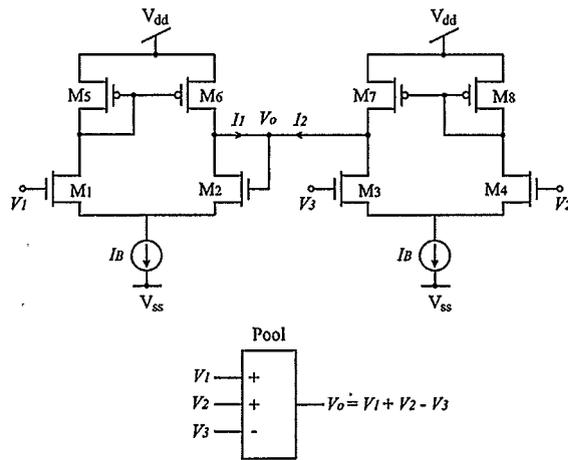


Fig. 1.6. The pool circuit proposed by Tsay and Newcomb in [33].

Then at the output node V_o , the sum of total currents is zero, that is,

$$g_m(V_1 - V_o) + g_m(V_2 - V_3) = 0 \quad (1.9)$$

Therefore,

$$V_o = V_1 + V_2 - V_3 \quad (1.10)$$

So the pool circuit can realize addition and subtraction operations simultaneously.

The proposed CMOS divider is shown in Fig. 1.7 [32].

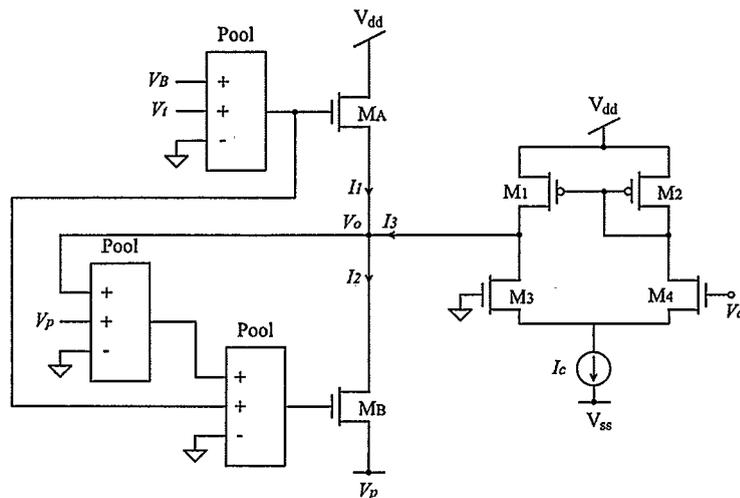


Fig. 1.7. The proposed CMOS divider in [32].

Applying the previous conclusions, the gate-to-source voltages of M_A and M_B are,

$$V_{GSA} = V_B - V_O + V_t \quad (1.11)$$

and

$$V_{GSB} = V_B + V_O + V_t \quad (1.12)$$

therefore, the difference of drain currents of M_A and M_B is,

$$I_1 - I_2 = K(V_B - V_O)^2 - K(V_B + V_O)^2 = -4KV_B V_O \quad (1.13)$$

Note that the output current I_3 of the OTA is approximately proportional to its input signal V_C ,

$$I_3 \cong g_{mc} V_C \quad \text{if} \quad \frac{2I_C}{K_C} \gg V_C^2 \quad (1.14)$$

Because the total current at node V_O is zero, finally,

$$V_O = \frac{g_{mc} V_C}{4KV_B} \quad (1.15)$$

which represents a division operation.

Here, V_O is the output signal, V_B is an input signal acting as the denominator, V_C is another input signal acting as the numerator, V_t is the threshold voltage of M_A and M_B , K is the transconductance parameter of M_A and M_B , g_{mc} is the transconductance of M_3 and M_4 , K_C is the transconductance parameter of M_3 and M_4 , and I_C is a DC current source.

The advantage of this technique is that it does not use any resistors and op-amps in the circuit, so the performance of its high-frequency operation is excellent. The disadvantage is that it is not very suitable for modern deep submicron process technology for the simple reason that it requires an accurate threshold voltage V_t , which is not a fixed value, and this situation becomes more serious for N-well process by considering bulk

effects. The divider circuit was simulated with 2- μm P-well process parameters in [32].

From simulation results reported, the total harmonic distortion was less than 1% with an input range up to ± 1 V, and its 3dB bandwidth was about 7 MHz.

1.3 The Proposed Analog Multiplier/Divider

From the previous discussions, we consider it is necessary and beneficial to develop a new CMOS analog multiplier/divider operating in low voltages and achieving a higher accuracy and bandwidth.

In this thesis a new CMOS four-quadrant multiplier/divider is proposed. The idea is based on the work of [1, 10, 15]. As we mentioned before, voltage adders and squaring circuits (V_{GS}^2) can be used to realize multiplication with current as the output signal. The new multiplier is derived from equation (1.3), which is more obvious by modifying it to the following form:

$$\begin{aligned} & K_n \{ [(X+x) + (Y+y) - V_t]^2 + [(X-x) + (Y-y) - V_t]^2 \} - \\ & K_n \{ [(X-x) + (Y+y) - V_t]^2 + [(X+x) + (Y-y) - V_t]^2 \} = 8K_n xy \end{aligned} \quad (1.16)$$

where K_n is a constant equal to $\mu C_{ox} W/2L$, μ is the mobility of charge carriers, C_{ox} is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio, and V_t is MOS transistor threshold voltage. The DC component is needed to ensure that all of the transistors are biased in saturation region. Note the introduction of V_t in the LHS of (1.16) does not affect the final result, and it is also worthy noting that the equation (1.16) is valid under the conditions of K_n and V_t are perfectly matched across the four items in the LHS of (1.16).

Therefore four voltage adders are required to generate multiplication using (1.16). To generate the squared terms and hence an output current, four NMOS transistors can be used and their respective drain currents are added and subtracted from each other. In this thesis we present a modified version of the multiplier circuit in [10].

For the divider realization, we consider using a voltage feedback technique with two feedback loops, which is easy to design and analyze. One feedback loop is used to realize analog division. The other feedback loop is a common-mode feedback loop which will be introduced in more detail in chapter 2.

Assume two multipliers are used and their current difference is converted into voltage by small signal output resistance r_o , then amplified by a very large gain A . Let the inputs to one multiplier be $K_{1,2}$ and $X_{1,2}$. The second multiplier can be driven with inputs $Y_{1,2}$ and $Z_{1,2}$. Here $K_{1,2}$ represent two differential inputs as K_1 and K_2 , and $K_2=K+k$, $K_1=K-k$, upper case letter K , represent DC or common mode component, lower case letter k , represent AC or small signal component. Other symbols $X_{1,2}$, $Y_{1,2}$, and $Z_{1,2}$ have the similar meaning. Therefore the following voltage equation can be written:

$$2K_n A r_o [(K_2 - K_1)(X_2 - X_1) - (Y_2 - Y_1)(Z_2 - Z_1)] = W \quad (1.17)$$

where W is the voltage output.

An analog divider can be realized with Y_2 directly connected to W by feedback. That means, there is no input connected to Y_2 . Therefore,

$$W = \frac{(K_2 - K_1)(X_2 - X_1)}{\left((Z_2 - Z_1) + \frac{1}{2K_n A r_o} \right)} + \frac{Y_1(Z_2 - Z_1)}{\left((Z_2 - Z_1) + \frac{1}{2K_n A r_o} \right)} \quad (1.18)$$

If $|Z_2 - Z_1| \gg 1/(2K_n A r_o)$, then equation (1.18) can be simplified to

$$W = \frac{(K_2 - K_1)(X_2 - X_1)}{(Z_2 - Z_1)} + Y_1 \quad (1.19)$$

which represents the multiplication/division operation plus a DC offset Y_1 .

The remainder of this thesis is devoted to a description of the proposed sub-circuits that perform addition, multiplication and division, circuit analysis, a discussion of second order effects, a presentation of our simulation and experimental results, and corresponding correction and improvement in our analog multiplier/divider.

CHAPTER 2

A NEW MULTIPLIER/DIVIDER

2.1 MOS Transistor Static Modelling

The simplest model that analytically describes the drain current in heavy inversion when the gate-source voltage exceeds the threshold voltage ($V_{GS} > V_t$) of a MOS transistor is the Shichman-Hodges model [34], first described in 1968. The model for NMOS transistors can be written mathematically as follows:

$$I_D = K_n (V_{GS} - V_t)^2 (1 + \lambda V_{DS}) \quad V_{DS} \geq V_{GS} - V_t \quad (2.1)$$

$$I_D = K_n \left\{ 2V_{DS}(V_{GS} - V_t) - V_{DS}^2 \right\} (1 + \lambda V_{DS}) \quad V_{DS} < V_{GS} - V_t \quad (2.2)$$

$$V_t = V_{t0} + \gamma (\sqrt{V_{SB} + 0.6} - \sqrt{0.6}) \quad (2.3)$$

In this model, the K_n parameter is fabrication process related, as is the parameter γ , which is the bulk effect coefficient. The parameter λ is the channel-length modulation factor, used to model the finite output conductance in the saturation region, i.e. it models the increase in drain current with increasing drain-source voltage in saturation. It should be noted that non-zero V_{SB} results in an increase in threshold voltage. This phenomenon causes problems in analog IC design as we shall see later.

Although these equations provide a quite accurate representation of the drain current of a MOSFET, they are too complicated to incorporate in a circuit synthesis procedure. Usually a simpler expression for (2.1) is used:

$$I_D = K_n (V_{GS} - V_t)^2 \quad V_{DS} \geq V_{GS} - V_t \quad (2.4)$$

Omitting the channel-length modulation factor is justified by the fact that, in the synthesis procedure usually all devices are operated well into the saturation region. The assumption of no channel-length modulation however, is a serious one since, λ adversely depends on channel length L , and short channel length causes I_D to be dependent on V_{DS} . Designers use the terms V_{GS}^2 in (2.1), $V_{GS}V_{DS}$ in (2.2), or V_{DS}^2 in (2.2) to implement the multiplication equations.

The Shichman-Hodges model is a reasonable representation for long-channel devices fabricated in larger feature size processes, (for channel lengths and widths greater than, say 10 micrometers). It predicts a square-law behaviour in saturation. Modern small-geometry device behaviour deviates significantly from this model, and newer more sophisticated models have been developed [35]. Nevertheless, the model described here has great value in predicting the functional behaviour of circuits, and it is still used extensively in this context.

When $V_{GS} < V_t$ the transistor is not turned off completely. It is said to be operating in the subthreshold or weak inversion region of operation in this mode. In the subthreshold region, the drain current is mainly diffusion current, and the transistor behaves somewhat like a bipolar transistor with drain current given by,

$$I_D \cong I_o \frac{W}{L} e^{\frac{(V_{GS} - V_{on})}{nV_T}} \left(1 - e^{\frac{-V_{DS}}{nV_T}} \right) (1 + \lambda V_{DS}) \quad (2.5)$$

where $I_o = \frac{\mu C_{ox} \mathcal{W}_T^2}{(2\sqrt{2}\Phi_F + V_{SB})}$.

In this model, I_o is a process parameter, n is the subthreshold slope factor, and V_T is the thermal voltage, Φ_F is a constant relevant to temperature and MOS transistor doping concentration.

2.2 Analog Adder

As we discussed in chapter one, adder circuits are needed to implement the novel CMOS analog multiplier/divider circuit. In [10], two kinds of adder circuit are proposed to perform addition on the two input signals in accordance with equation (1.16). One of these two adder circuits is redrawn in Fig. 2.1.

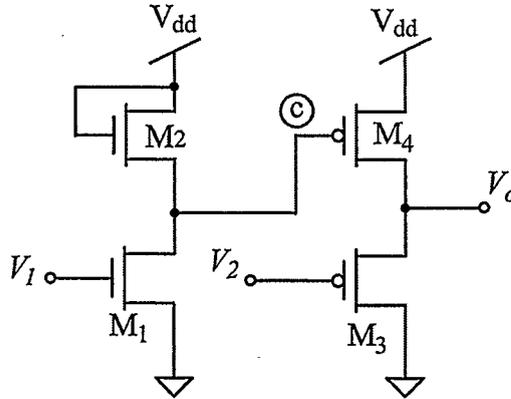


Fig. 2.1. The adder circuit proposed in [10].

In order to understand the principle of operation of this circuit, we assume that all the transconductance parameters of these four transistors are the same, threshold voltages of each pair of series connected transistors are perfectly matched, and output resistances of these four transistors are neglected. Under these conditions, the gate to source voltage

of each pair of series connected transistors must be the same. This means that the voltage at node c is $V_{dd}-V_1$. Since M3 and M4 are PMOS transistors, the source to gate voltage of M4 is $V_{dd}-(V_{dd}-V_1)$, or V_1 . Therefore V_o is equal to (V_1+V_2) .

As shown in Fig. 2.1, the analog adder consists of two transistors between the supply rails and operates off a single supply. However, this adder circuit suffers from bulk effects in a N-well process. That is, because the substrates of M1 and M2 are both connected to analog ground, the threshold voltages of M1 and M2 will be different. In fact the threshold voltage of M2 will be greater than that of M1.

Here a new version of adder circuit is proposed in order to eliminate the bulk effects in a N-well process. The new all PMOS transistor adder circuit is shown in Fig. 2.2.

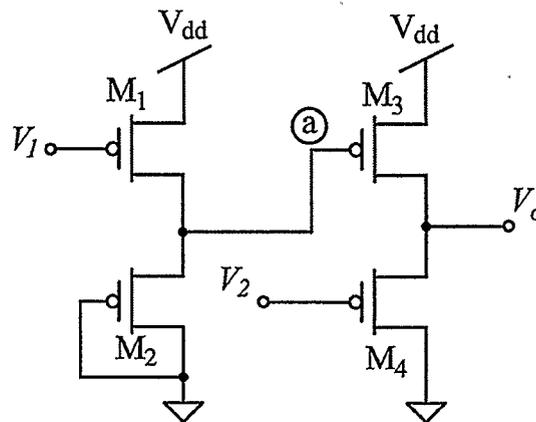


Fig. 2.2. An all PMOS transistor adder circuit.

The operation of this adder is conceptually the same as that in Fig. 2.1. By assuming that all the transconductance parameters of these four transistors are the same, and threshold voltages of each pair of series connected transistors are the same, the output voltage V_o is equal to (V_1+V_2) . All aspect ratios of PMOS transistors in our final

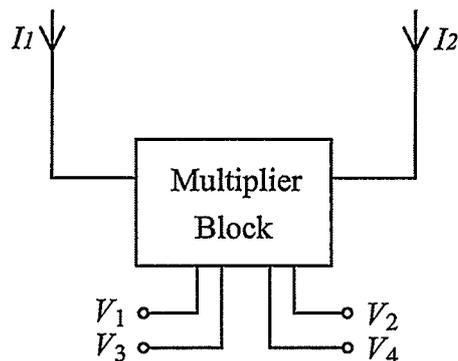


Figure 2.3 (b). The equivalent block diagram.

Here transistors M1-M12 make up the four adders, with the two middle transistors (M1/2 and M7/8) simultaneously feeding two adders. Let input voltages V_1 and V_3 be $Y \pm y$, and input voltages V_2 and V_4 be $Z \pm z$, respectively. Transistors M13-16 are used to convert the output voltage of each adder sub-circuit into a current, which is where the square law characteristic of the MOS transistors operating in saturation comes in. The aspect ratios of these four transistors are designed to be $20/2 \mu\text{m}$, one consideration is to compensate the short channel effects, the other consideration is to reduce the total power consumption by limiting the currents of I_1 and I_2 . For example, if common-mode components of Y and Z are chosen to be 1.4 V and 0.3V respectively, the drain currents of M13-16 are close to 0.68 mA, therefore the currents of I_1 and I_2 are close to 1.36 mA. Referring to equation (1.16), the subtraction of the currents ($I_2 - I_1$) yields the correct output current of $8K_n yz$. Note that two multipliers are required to make up the divider.

2.4 Analog Divider

Fig. 2.4 is a simplified block diagram of the complete multiplier/divider.

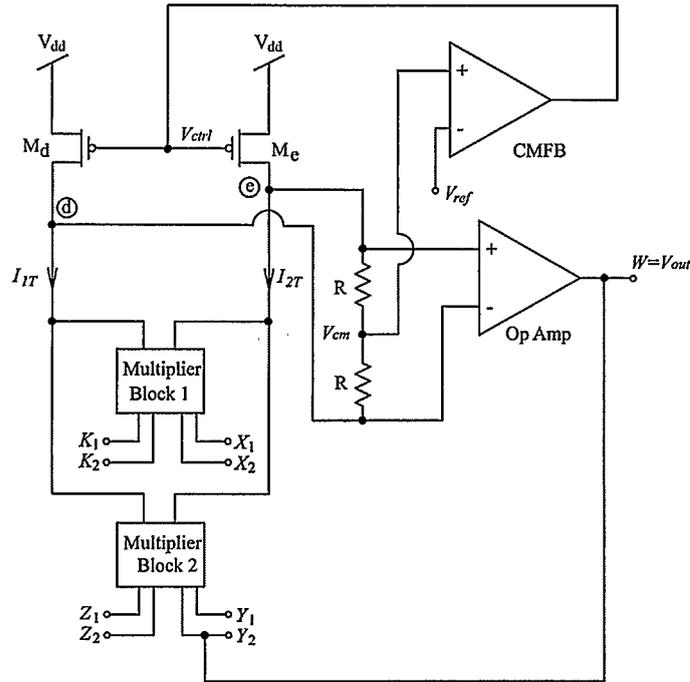


Figure 2.4. The simplified block diagram of the multiplier/divider.

Internal signals are actually in the form of currents, but the function of the multiplier/divider can be understood by using voltages throughout, as shown in this figure.

The multiplier/divider responds to the difference signals $2k=K_2-K_1=(K+k)-(K-k)$, $2x=X_2-X_1=(X+x)-(X-x)$ and $2z=Z_2-Z_1=(Z+z)-(Z-z)$, and rejects common-mode voltages on these inputs under the condition of perfect matching. The high-gain op-amp nulls the difference between the inverting terminal and the non-inverting terminal, according to equations (1.17), (1.18), and (1.19) to generate the final output $W=V_{out}$.

To implement the divider, the sub-circuits are arranged according to equation (1.17) except that two multiplier output currents are cross-connected in order to simplify the circuitry. Two multiplier output currents are converted into voltages at each input terminal of the high gain operational amplifier. That way equation (1.19) can be realized.

The realization of the division operation requires two analog multipliers, so current source transistors M_d and M_e must supply DC currents I_{1T} and I_{2T} , close to two times of the currents of I_1 and I_2 , respectively. The values of I_{1T} and I_{2T} are roughly the same, 2.74 mA. Therefore aspect ratios of M_d and M_e are designed to be $3 \times 90/1 \mu\text{m}$, where 3 as the multiplier, means effectively there are three transistors parallel connected.

It is difficult to keep the drain voltages of these two current source transistors the same for the following two reasons. First, the drain voltages of these two transistors depend on the common-mode and small-signal components of the input signals, and this is the dominant reason. Second, a mismatch effect occurs in transistors M_d and M_e , with this being the minor reason. Both effects cause a DC biasing problem of the high gain operational amplifier. In order to stabilize the drain voltages of current source transistors M_d and M_e , and to let the high gain operational amplifier work properly, a common-mode feedback (CMFB) circuit is introduced in the circuit. The CMFB circuit fixes the common-mode level of the drain voltages of M_d and M_e to V_{ref} .

To supply the DC biasing voltages for the op-amp and V_{ref} , a self-biased reference with a start-up circuit is also introduced in the whole circuit, as we will explain later.

2.5 Operational Amplifier

By avoiding the cascode scheme of the transistors, a two-stage operational amplifier (op-amp) was chosen for achieving larger output ranges with a single +3.3V power supply voltage. The op-amp is the most useful building block in analog integrated circuit design [36-38]. A block diagram of a basic two-stage CMOS op-amp is shown in Fig. 2.5.

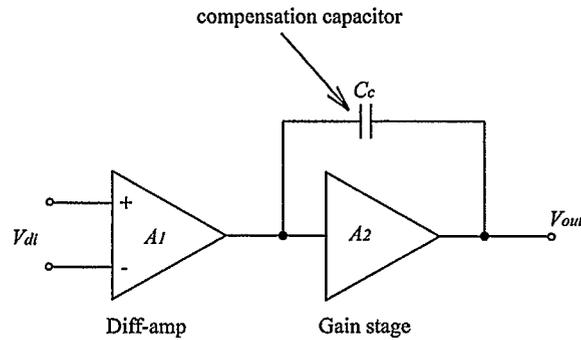


Figure 2.5. Block diagram of a basic two-stage CMOS op-amp.

The first stage of the op-amp is a differential amplifier, which is composed of a differential pair terminated in an active load and biased by a simple DC current source. The output of this stage is connected to another CMOS gain stage, a common source stage. The op-amp is frequency compensated by a compensation capacitor C_c connected around the common source gain stage in order to prevent oscillation when the op-amp is applied in a feedback loop. Since the op-amp is used to drive a purely capacitive load, which is the case in the design of the analog multiplier/divider, the output buffer is not needed [39].

The design goals of this operational amplifier are a DC gain not less than 100dB and gain bandwidth product (GBP) not less than 40MHz. Fig. 2.6 shows the circuit schematic diagram of the operational amplifier used in the design of the multiplier/divider circuit. Two points that are different from the basic concept of the two-stage op-amp can be recognized in this schematic. First, the circuit is frequency compensated by a series R-C network (M_c - C_1) connected around the gain stage, and transistor M_c operates with no dc drain current. The reason is that, in the basic two-stage CMOS op-amp including Miller compensation, a right-half-plane (RHP) zero exists in

the circuit which value is not far from the origin, and this zero considerably degrades the stability of the circuit by yielding more phase shift [35]. One technique to deal with the RHP zero is to insert a resistor in series with the compensation capacitor, and in practice, the resistor is usually implemented using a MOS transistor biased in the triode region, as shown in Fig. 2.6. Second, in order to reduce the standby current of the output stage, a class-AB output stage is used, and two additional NMOS transistors Mp6 and Mp7 implement this.

In this compensation approach, the dominant pole is set by compensation capacitor C1, and the first non-dominant pole is inversely proportional to C2. Usually the compensation capacitor should be selected to give an acceptable phase margin for the largest C2. In the circuit, since the total load capacitance varies for each amplifier, a maximum load capacitance of value 8 pF was chosen to ensure operation stability, and C1 is chosen as 20pF accordingly. These two capacitors will set the dominant pole and the first non-dominant pole. We can try to move the RHP zero into the left-half-plane (LHP) so as to cancel the first non-dominant pole and increase the GBP, and this occurs if $R \cong (C1+C2)/g_{mp8}C1$ [35, 40-41]. Substituting the PMOS model parameters of $\mu_p C_{ox}$ to $33 \mu A/V^2$ and V_{tp} of -0.68 V, we note that W/L of Mp8 is $8 \times 25 \mu m / 1 \mu m$. By hand calculation, we get the transconductance of transistor Mp8 to be around 2.3 mA/V, therefore $R \cong 609 \Omega$. From simulation results we found that the optimum value of R is around 300Ω , and here Mc acts as a resistor close to 300Ω whose value is controlled by its aspect ratio.

Table 2.1 shows all the sizes of the transistors used in this operational amplifier. Here again a multiplier of “5” means effectively there are five transistors parallel

connected. The reason is that in TSMC's CMOS P18 process, the maximum width for one transistor is limited to $100\ \mu\text{m}$.

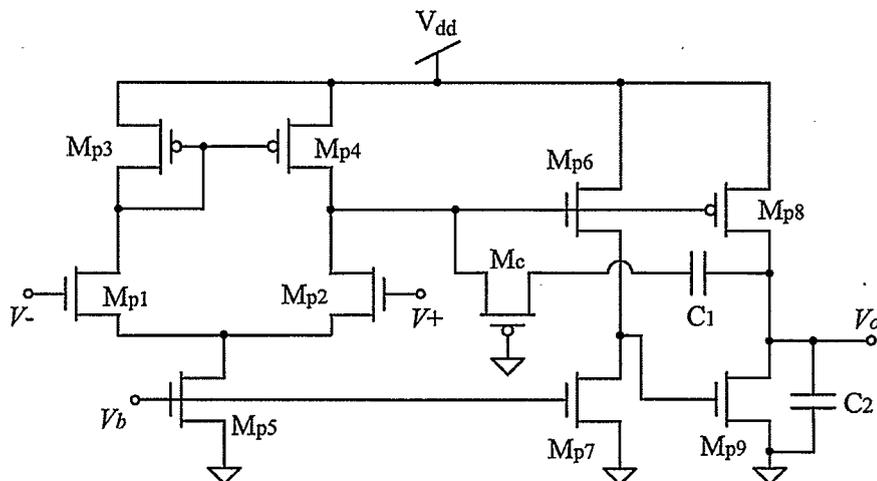


Figure 2.6. Two-stage CMOS operational amplifier with class-AB output stage.

Table 2.1. Transistor sizes used in Fig. 2.6.

Transistor's number	Width (μm)	Length (μm)	Multiplier
Mp1-Mp2	50	1	5
Mp3-Mp4	25	1	5
Mp5	100	1	1
Mp6	100	1	1
Mp7	50	3	1
Mp8	25	1	8
Mp9	100	1	1
Mc	80	1	1

A circuit useful in simulating the open-loop gain of an op-amp with or without compensation is shown in Fig. 2.7 [39]. The resistive feedback ensures a DC biasing condition, while the capacitor/resistor combination eliminates AC signals fed back from the output to the inverting terminal of the op-amp.

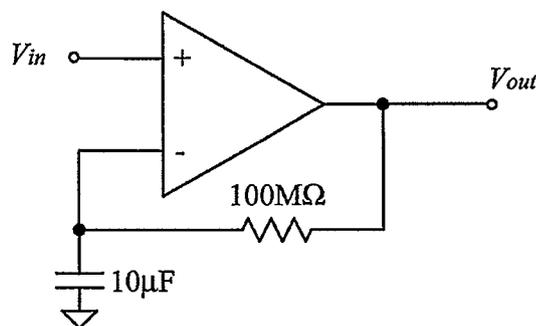


Figure 2.7. Circuit used to measure open-loop gain and frequency response.

To simulate the circuit, Cadence Spectre(S) with level 28 models was used. If the feedback factor β does not depend on the frequency, the worst-case stability corresponds to unity-gain feedback, that is, $\beta=1$. For this reason, we analyze the magnitude and phase response without considering the feedback factor β . The simulated AC magnitude and phase response of the designed op-amp are shown in Fig. 2.8. We note that the DC gain was 107 dB, and the op-amp's gain bandwidth product (GBP) was 42 MHz, which implies the transconductance of transistor Mp1 or Mp2 to be around 5.3 mA/V. To verify the validity of the GBP value, we substitute the NMOS model parameters of μC_{ox} as 140 $\mu A/V^2$ and V_t as 0.72 V, and note that W/L of Mp1 or Mp2 is $5 \times 50 \mu m / 1 \mu m$. By hand calculation, we get the transconductance of transistor Mp1 or Mp2 to be around 5.7 mA/V, which is very close to the simulation result.

Normally we desire no less than a 45° phase margin when compensating an op-amp. Here the point at which the open-loop gain is unity (0 dB) corresponds to a phase shift of -120° , or a 60° phase margin, so the designed op-amp is stable by itself. Since the high-frequency (larger than 1MHz) gain of this op-amp is not very high, the operational bandwidth of the analog divider is limited by this op-amp. Because we just wanted to prove a new design concept to realize an analog divider, we used this op-amp in the circuit. However, the performance of the analog multiplier/divider can be improved by improving the op-amp design.

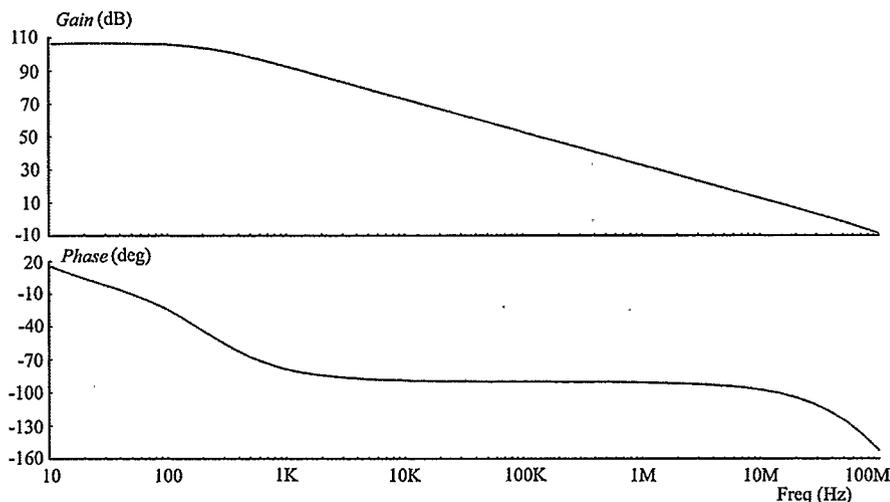


Figure 2.8. The simulated AC magnitude and phase response of the designed op-amp.

2.6 Common Mode Feedback Circuit

Feedback loops are necessary to hold the common-mode voltage, at nodes operating fully differentially, at a constant value. As a general rule, if the output CM level cannot be determined by “visual inspection” of the circuit and requires calculations based on device properties, then it is poorly defined [35]. This is the case in Fig. 2.4, so a common mode feedback circuit is necessary to hold the node voltages at d and e .

In Fig. 2.4 the simplest common mode detector, which consists of two equal resistors R , senses the average voltage at the midway of the two resistors to a value of $(V_d+V_e)/2$. The common mode detector, along with common mode reference voltage V_{ref} and another servo op-amp (the same as the op-amp we discussed above), consist of the common mode feedback (CMFB) circuit. Of course one can use a more advanced CMFB circuit here, but again the objective was just to use this circuit to verify the behaviour of the analog multiplier/divider. Thus we chose this CMFB circuit as a functional block to realize the multiplier/divider.

The circuit functions as follows: The output common mode level is measured by the common-mode detector and compared to the desired common-mode reference voltage V_{ref} at the inputs of a high gain servo amplifier. The negative feedback loop is completed through M_d and M_e . If V_d and V_e were at different potentials, the common mode detector result $(V_d+V_e)/2 \neq V_{ref}$. This in turn would generate a correction, V_{ctrl} , dependent on the error. Since V_{ctrl} is tied to both gates of M_d and M_e via negative feedback, it forces $V_d = V_e$ to center the signals around V_{ref} if the loop was designed properly. In order that the common-mode level be as close to V_{ref} as possible, the servo amplifier should be designed to have a large DC gain. This means that its bandwidth cannot be expected to be very high [42]. The gain of the designed op-amp in this case was sufficient so that it could serve as a servo amplifier also.

2.7 Threshold Voltage Referenced Self-Biasing

Voltage and current references are extensively used in analog CMOS integrated circuit design. A good voltage or current reference means that it is independent of power supply voltage and process. We can design voltage reference from the power supplies using resistors and/or the MOSFET transistors in a straightforward manner, as shown in Fig. 2.9 [39].

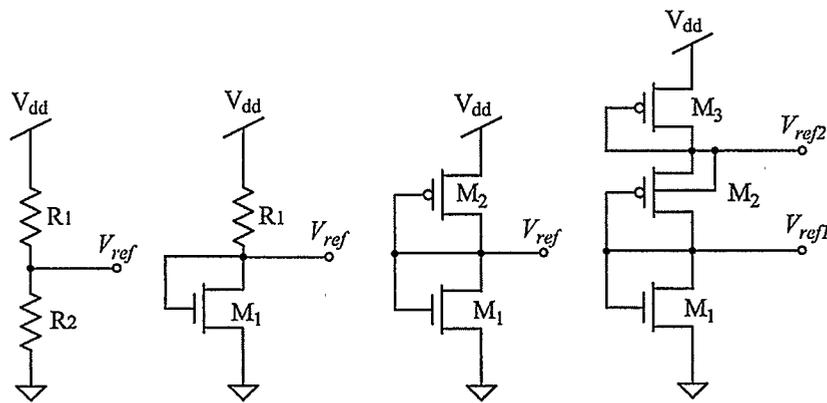


Fig. 2.9. Voltage divider implementations in CMOS.

The common disadvantage of these voltage reference implementations is that, variations in V_{dd} directly affect the currents in the circuit, thus V_{ref} depends on power supply voltage V_{dd} . A DC biasing circuit that can reduce the effect of power supply variations on currents is shown in Fig. 2.10 [37, 39].

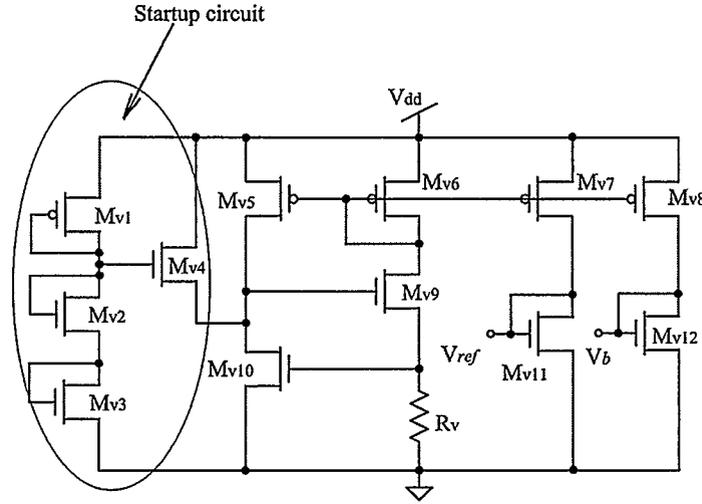


Figure 2.10. Threshold reference self-biasing circuit with startup circuit.

The circuit operates as follows. Neglecting the output resistances and body effects of the transistors, suppose the current I flows through the resistor R_v , we can apply Kirchoff's voltage law and the Shichman-Hodges model, such that the voltage drop across R_v is then given by [39],

$$IR_v = V_{GS10} = V_{tn} + \sqrt{\frac{2I}{\mu C_{ox}(W/L)_{10}}} \quad (2.6)$$

This equation indicates that the current I can be obtained through resistance R_v , as well as transconductance parameter and threshold voltage of transistor $Mv10$. The accuracy of the current I is only affected by the accuracy of the threshold voltage and the resistance R_v . Thus the current I does not depend on the power supply voltage V_{dd} .

MOSFETs $Mv5$ - $Mv8$ are designed to have the same aspect ratios, forcing the same current I to flow through $Mv9$ and $Mv10$. MOSFETs $Mv7$ and $Mv8$ mirror the same current I that flows through $Mv9$ and $Mv10$, and generate reference voltages V_{ref} and V_b on the two diode-connected transistors $Mv11$ and $Mv12$.

A startup circuit is necessary for this self-biased circuit because two results of I are expected from equation (2.6). This is clearly illustrated by Fig. 2.11 [39], where point A in this figure corresponds to the desired I , while point B corresponds to $I=0$.

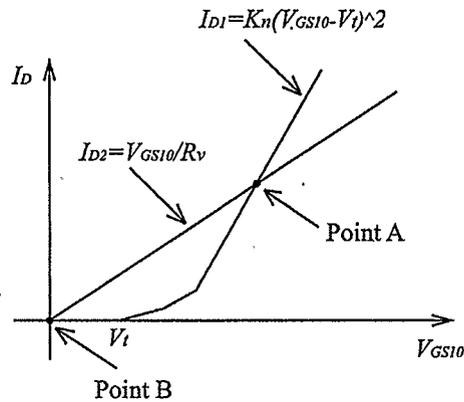


Fig. 2.11. Two possible operating points of self-biased circuit.

The startup circuit is used to avoid operation at point B . The principle of this startup circuit is as follows. If the gate voltage of Mv9 is at or near zero, Mv4 turns on because the gate voltage of Mv4 is $2V_{GS}$, then the gate voltage of Mv9 eventually goes up until it reaches $2V_{GS}$, this causes Mv4 to be turned off and the startup circuit is disconnected from the threshold reference self-biasing circuit. That is, once the self-biasing circuit is operating at point A , the startup circuit does not affect its operation anymore.

In Fig. 2.10, R_v is chosen as $1\text{k}\Omega$. Table 2.2 shows all the sizes of the transistors in the circuit. From the circuit, we can obtain $V_{ref}=1.75\text{V}$ and $V_b=1.1\text{V}$.

Table 2.2. Transistor sizes used in Fig. 2.10.

Transistor's number	Width (μm)	Length (μm)	Multiplier
Mv1	40	1	1
Mv2	1	1	1
Mv3	1	1	1
Mv4	20	1	1
Mv5-Mv8	100	1	1
Mv9	100	1	3
Mv10	100	1	2
Mv11	14.6	1	1
Mv12	54.5	1	2

2.8 The Complete Analog Multiplier/Divider

Fig. 2.12 shows the complete schematic of the novel four-quadrant CMOS analog multiplier/divider without the biasing circuits.

resistance that decreases as the input voltage becomes more positive. It is then possible to employ “complementary” switches so as to achieve a relatively constant on-resistance, but usually the allowable range of signal swing across the transistors is required to be small, this is the case when it is used as common-mode sampling resistor. Fig. 2.13 shows the idea behind using two complementary transistors to replace a resistor.

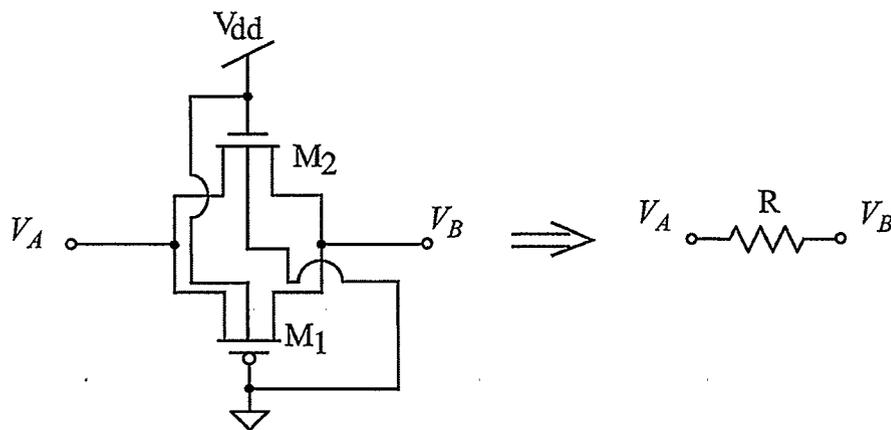


Fig. 2.13. Using two complementary transistors to replace a resistor.

In the analog multiplier/divider, common-mode sampling resistors R 's are optimized to be $4.5 \text{ k}\Omega$, $V_{A, \text{ or } B}$ was set to be 1.75 V , around the middle of the power voltage supply. It can be shown that, such a combination produces an equivalent resistance $R_{on,eq}$ given by,

$$R_{on,eq} = R_n // R_p \quad (2.7)$$

where,

$$R_n \equiv \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N (V_{dd} - V_{A,orB} - V_{tn})} \quad (2.8)$$

$$R_p \cong \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_P (V_{A,orB} - |V_{tp}|)} \quad (2.9)$$

which further simplifies to,

$$R_{on,eq} \cong \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N (V_{dd} - V_{tn}) - \left[\mu_n C_{ox} \left(\frac{W}{L}\right)_N - \mu_p C_{ox} \left(\frac{W}{L}\right)_P \right] V_{A,orB} - \mu_p C_{ox} \left(\frac{W}{L}\right)_P |V_{tp}|} \quad (2.10)$$

It should be noted that both the NMOS and PMOS transistors are required to operate in deep triode region. In the final design, the aspect ratios for the NMOS and PMOS transistor were the same, $5.5 \mu\text{m} / 1 \mu\text{m}$, which yielded an on resistance of approximately $4.5 \text{ k}\Omega$.

CHAPTER 3

CIRCUIT ANALYSIS

3.1 The Range of Input Signals

As we stated earlier, in order for these multipliers to work properly, we must set all the transistors operating in saturation region. These requirements place restrictions on the range of input values of the adders and NMOS current generators, e.g., M13-M16 in Fig. 2.3 (a), and are given by [10],

$$\frac{V_{dd} - |V_{tp}|}{2} \leq V_1 \leq V_{dd} - |V_{tp}| \quad (3.1)$$

$$-|V_{tp}| \leq V_2 \leq V_{dd} + |V_{tp}| - 2V_1 \quad (3.2)$$

$$V_{tn} < V_1 + V_2 \quad (3.3)$$

$$V_1 + V_2 - V_{tn} \leq V_e \quad (3.4)$$

Referring to Fig. 2.3 (a) and Fig. 2.4, V_{tn} is the threshold voltage of M13-M16, V_{tp} is the threshold voltage of M1-M12, and V_e is the drain voltage of M15, M16 and Me, at node e .

From these ranges, the common mode voltage $\{Y, Z, W \text{ and } X\}$ that allows for maximum input swing can be found in a straightforward manner. Since the bulk of a PMOS transistor can be connected to either V_{dd} or source for an N-well process, bulk effects are eliminated.

From equations (3.1) and (3.2), if $V_{dd}=3.3\text{V}$, $|V_{tp}|\cong 0.7\text{V}$, then $1.3\text{V} \leq V_1 \leq 2.6\text{V}$, and $-0.7\text{V} \leq V_2 \leq 4 - 2V_1$ can be derived. In our simulation results, in order to avoid large overdrive voltages and limit currents of M13-M16, Md and Me, we choose DC biasing voltages close to the lower limits of (3.1) and (3.2). When considering the limits set by (3.3) and (3.4), and a range of signal swing, we choose the common-mode level of V_1 to be 1.4 V, and the common-mode level of V_2 to be 0.3 V, to simulate the operation of the analog multiplier/divider.

3.2 Small Signal Analysis

Small signal and noise analysis were also performed on the analog adder in order to determine the performance of the multiplier/divider. The small signal equivalent of the analog adder is shown in Fig. 3.1.

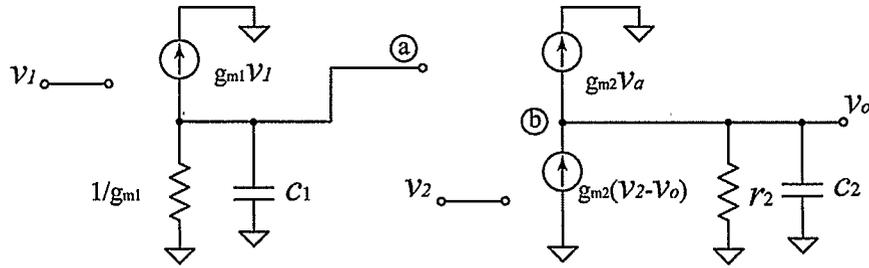


Fig. 3.1. Small signal equivalent of adder circuit.

Here, r_2 is the reciprocal of the total conductance at node b , c_1 and c_2 represent the total parasitic capacitance seen at nodes a and b , respectively. The output v_o of this sub-circuit as a function of v_1 and v_2 is given by,

$$v_o = \frac{g_{m2}r_2}{(1 + sr_2c_2 + g_{m2}r_2)} \left[\frac{g_{m1}}{(g_{m1} + sc_1)} v_1 + v_2 \right] \quad (3.5)$$

When determining this function, it was assumed that since all of the aspect ratios of the transistors were the same, and the drain current of each series connected transistor pair was the same, therefore their small signal parameters would also approximately be equal. The output v_o thus has two poles and for the reason of stability, one must ensure they are adequately separated.

3.3 Noise Analysis

One of the main noise sources in a MOS transistor is thermal channel noise, and it is dependent on the transconductance of the transistor. In [43], a noise current source placed from source to drain models the thermal channel noise, and the drain noise current spectral density is expressed as,

$$\overline{I_n^2} = 4k_B T \gamma g_m \quad (3.6)$$

where $k_B = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, T is temperature, the coefficient γ is 2/3 for long-channel transistors, but it will become larger for short-channel transistors [44].

Another main source of noise is flicker noise, also called 1/f noise. Unlike thermal noise, the average power of flicker noise cannot be predicted easily. A noise voltage source that is series connected to the gate models the flicker noise, and the gate noise voltage spectral density is roughly expressed as [35],

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \quad (3.7)$$

where K is a process-dependent constant, and f is operating frequency. Since flicker noise voltage is inversely proportional to the transistor area, WL , then it is possible to decrease flicker noise by increasing the transistor area.

In our simple noise analysis we just consider the transistor channel thermal noise. The noise equivalent circuit of the adder is shown in Fig. 3.2.

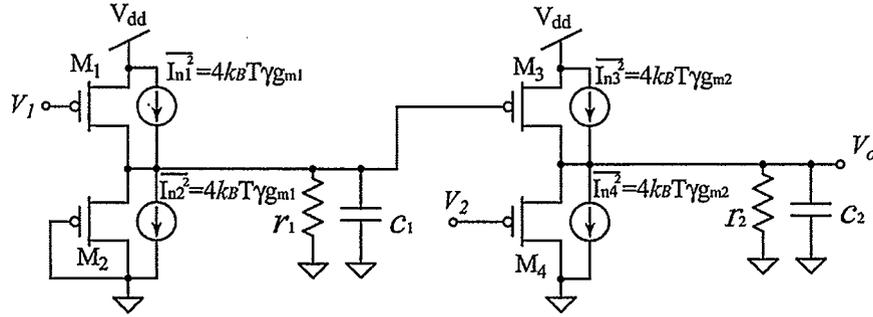


Figure 3.2. Noise equivalent of the adder circuit.

From Fig. 3.2, it can also be shown that the output noise voltage can be expressed as,

$$\bar{V}_{on}^2 = 8k_B T \gamma \frac{r_2^2}{(1 + \omega^2 c_2^2 r_2^2)} \left[g_{m2} + \frac{g_{m1} g_{m2}^2}{(g_{m1}^2 + \omega^2 c_1^2)} \right] \quad (3.8)$$

where the symbols have their usual meaning. The implication of this equation is that we can decrease the noise voltage by decreasing g_{m2} .

3.4 High Frequency Characteristics of The Analog Divider

From AC sweep results, the 3-dB bandwidth of the analog multiplier is close to 200 MHz. For the op-amp, since we know that the DC gain was 107 dB, and the op-amp's GBP was 42 MHz, the estimation value of the 3-dB bandwidth is close to 188 Hz. We can also get the op-amp's 3-dB bandwidth from its AC magnitude response as 207 Hz, which is close to the estimation value. We note that the 3-dB bandwidth of the analog

multiplier is much larger than that of the op-amp. Therefore the bandwidth of the analog divider is mainly limited by the op-amp's bandwidth, and we can simplify the high frequency analysis of the analog divider by neglecting the frequency dependence of the analog multiplier.

If the op-amp's open loop gain is characterized by $A(s) = GBP/(s + \omega_a) \cong GBP/s$, where the assumption $\omega_o \gg \omega_a$ (where ω_a is the op-amp dominant pole) is made to allow simplification, we arrive at the following equations:

$$W = \frac{GBP}{s} \times \frac{r_o}{(1 + sr_o c_o)} \times (I_{2T} - I_{1T}) \quad (3.9)$$

$$I_{2T} = 2K_n(K_2 - K_1) \times (X_2 - X_1) \quad (3.10)$$

$$I_{1T} = 2K_n(Z_2 - Z_1) \times (W - Y_1) \quad (3.11)$$

where r_o is the reciprocal of the total conductance at node d and e , and c_o is the total parasitic capacitance at nodes d and e . Since the circuit is designed to be symmetrical, the value of r_o and c_o are the same at nodes d and e . Currents I_{1T} and I_{2T} are the total currents flowing out of nodes d and e , respectively (see Fig. 2.4).

From DC biasing currents of all transistors connected to node d and e , if we choose $\lambda \cong 0.1 \text{ V}^{-1}$, we can calculate r_o to be 1.82 k Ω . The circuit test value is 1.89 k Ω at low frequencies (lower than 21 MHz), and if the frequency goes higher, the test value of r_o will be smaller.

In TSMC's 3.3V, CMOS18 technology, $C_{ox} = \epsilon_{ox}/t_{ox} \cong 5.15 \times 10^{-3} \text{ pF}/\mu\text{m}^2$. Considering all transistors connected to node d or e , c_o lies in the range of 1 pF. If the operating frequency is lower than 21 MHz, the total impedance is close to r_o at node d or e .

Therefore equation (3.9) can be simplified to,

$$W = \frac{GBP}{s} \times r_o \times (I_{2T} - I_{1T}) \quad (3.12)$$

Solving these equations, the transfer function of Fig. 2.4 can be written as:

$$W = \frac{\frac{(K_2 - K_1)(X_2 - X_1)}{(Z_2 - Z_1)} + Y_1}{1 + \frac{s}{2K_n \cdot (Z_2 - Z_1) \cdot GBP \cdot r_o}} \quad (3.13)$$

We can observe that there is a difference between equations (3.13) and (1.19) when frequency is taken into account. Here if $|s/(2K_n \cdot (Z_2 - Z_1) \cdot GBP \cdot r_o)| \ll 1$, equation (3.13) becomes (1.19).

Here we can define the 3dB frequency of the analog divider under the condition of $|s/(2K_n \cdot (Z_2 - Z_1) \cdot GBP \cdot r_o)| = 1$. First we substitute r_o by 1.89 k Ω , $(Z_2 - Z_1)$ by 0.1 V, μC_{ox} by 140 $\mu\text{A}/\text{V}^2$, and GBP by 42 MHz, then the 3dB frequency is close to 11 MHz. If instead, we substitute $(Z_2 - Z_1)$ by 0.05 V while keeping other parameters unchanged, the 3dB frequency is close to 5.6 MHz. We can also note that the 3dB bandwidth of the analog divider is proportional to the magnitude of input signal $(Z_2 - Z_1)$. These predictions roughly matched with simulation results, as we will see in section 5.1.2.

CHAPTER 4

SECOND ORDER EFFECTS

4.1 Basic Idea of Second Order Effects

The Shichman-Hodges model [34] shows an approximate square-law relationship between drain currents and overdrive voltages of MOSFETs, and it is only accurate for long-channel transistors with feature size larger than $4\ \mu\text{m}$ [35]. Since we use $0.18\ \mu\text{m}$ feature size technology in designing the analog multiplier/divider, the simple square-law model should be adjusted to incorporate higher order effects in order to get enough accuracy in simulation results.

Here we provide a basic understanding of short-channel effects and their effects on our analog multiplier/divider. The basic operation of the multiplier has been described by neglecting second-order effects such as threshold voltage variation, bulk effect, channel-length modulation, mobility degradation, and component mismatch. The operation of this type of multiplier depends directly on the inherent square-law of the MOS transistor so that the mobility degradation due to large gate input voltages and component mismatches are the significant error sources. In the subsection that follows, we briefly discuss each source of error and possible solutions.

4.2 Threshold Voltage Variation

The threshold voltage varies with different process technology, and it cannot be scaled down accordingly with the development of the CMOS technology [9].

As we mentioned in equation (1.16), one requirement of the realization of multiplication is perfectly matched threshold voltage, V_m . Also, one requirement of the analog adder is perfectly matched threshold voltage, V_p . But in TSMC's CMOSP18 3.3V process technology, V_m varies from 0.62 to 0.82 V, and V_p varies from -0.78 to -0.58 V. Therefore the operation of the analog multiplier/divider is affected by these threshold voltage variations.

Here we note that the effect of threshold voltage variation emerges as a kind of effect on parameter mismatch. Since threshold voltage mismatch is inversely proportional to the transistor size, which means, bigger devices have better matching performance, so we can choose larger devices in the design of the analog multiplier/divider.

4.3 Bulk Effects

Theoretically, V_t increases when the source-bulk potential difference increases. This is the bulk effect.

When considering the bulk effects, V_t is given by equation (2.3) and repeated here for convenience as,

$$V_t = V_{t0} + \gamma(\sqrt{V_{SB} + 0.6} - \sqrt{0.6}) \quad (4.1)$$

where V_{SB} is the source-bulk potential difference. The value of γ typically lies in the range of 0.3 to 0.4 $V^{1/2}$ [35]. In the simple small signal model it can be modeled by a CCCS (g_{mb}) in parallel with g_m .

To understand this effect we concentrate on Fig. 2.2, where we momentarily assume that transistors M2 and M4 are affected by bulk effects. A general expression for the output of this adder circuit that includes the body effect in terms of g_{mb} is then given by:

$$v_o = \frac{1}{(1 + g_{mb2}/g_{m2})} \left(\frac{v_1}{(1 + g_{mb1}/g_{m1})} + v_2 \right) \quad (4.2)$$

An alternative way of thinking about bulk effects is in terms of threshold voltages since V_{SB} is directly related to V_t . In that case, if the PMOS transistors are matched in terms of their transconductance parameters, it is straightforward to show that ΔV_o , the error in V_o , is given by:

$$\Delta V_o = |V_{tp,2}| + |V_{tp,3}| - |V_{tp,1}| - |V_{tp,4}| \quad (4.3)$$

In our design, using a N-well process where the bulk can be connected to source will reduce bulk effects as g_{mb} in (4.2) goes to zero.

4.4 Channel-Length Modulation

The channel-length modulation effect can be simply explained as effective channel length decreases when V_{DS} increases. This means that the drain current varies with V_{DS} and deviates from the simple square-law model, thus generates a nonideal current source in saturation.

In equations (2.1) and (2.2), λ is the channel-length modulation coefficient, it becomes smaller for longer channel transistors. In order to minimize the effect of channel-length modulation, transistors with large channel lengths of 1 μm to 2 μm are used in our design, but this reduces the operation bandwidth significantly.

4.5 Mobility Degradation

Mobility degradation as low carrier mobility occurs when large gate-source voltages are used. This effect becomes more significant for short-channel transistors. An empirical equation can be used to model this effect [45],

$$\mu = \frac{\mu_o}{1 + \theta(V_{GS} - V_t)} \quad (4.4)$$

where μ_o is the zero field mobility, $\theta = 1/(t_{OX}E_{CR})$ with t_{OX} is the oxide thickness, and E_{CR} is the critical field. The mobility parameter θ is process dependent and may have values ranging from 0.01 to 0.25 V⁻¹. This means a deviation from the nominal value of μ ranging from 1% to 20% for a 1V change in $(V_{GS} - V_t)$ [45].

Using Taylor series expansion, (4.4) can be rewritten as,

$$\mu = \mu_o \left\{ 1 - \theta(V_{GS} - V_t) + \theta^2(V_{GS} - V_t)^2 - \theta^3(V_{GS} - V_t)^3 + \dots \right\} \quad (4.5)$$

Assuming that $\theta(V_{GS} - V_t) \ll 1$, (4.5) can be rewritten as:

$$\mu \approx \mu_o \{ 1 - \theta(V_{GS} - V_t) \} \quad (4.6)$$

So the drain current equation including the mobility degradation can be modeled as,

$$I_{DS} \approx \frac{1}{2} \mu_o C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_t)^2 [1 - \theta(V_{GS} - V_t)] \quad (4.7)$$

That is,

$$I_{DS} \approx \frac{1}{2} \mu_o C_{ox} \left(\frac{W}{L} \right) [(V_{GS} - V_t)^2 - \theta(V_{GS} - V_t)^3] \quad (4.8)$$

From equation (4.8), we note that the drain current is decreased for the reason of mobility degradation, and the square-law behavior of the drain current is significantly affected by mobility degradation. Moreover, for the harmonic analysis, both even harmonics and odd harmonics will be generated in drain current according to equation (4.8).

However, substituting (4.8) into the analog multiplier realization equation (1.16), it can be shown that,

$$\begin{aligned}
& K_n \left\{ [(X+x)+(Y+y)-V_t]^2 - \theta [(X+x)+(Y+y)-V_t]^3 \right\} + \\
& K_n \left\{ [(X-x)+(Y-y)-V_t]^2 - \theta [(X-x)+(Y-y)-V_t]^3 \right\} - \\
& K_n \left\{ [(X-x)+(Y+y)-V_t]^2 - \theta [(X-x)+(Y+y)-V_t]^3 \right\} - \\
& K_n \left\{ [(X+x)+(Y-y)-V_t]^2 - \theta [(X+x)+(Y-y)-V_t]^3 \right\} = 8K_n xy [1 - 3\theta(X+Y-V_t)]
\end{aligned} \tag{4.9}$$

From the above equation, it is obvious that the output current of each multiplier is modified to the form of $8K_n yz [1 - 3\theta(Y+Z-V_t)]$ with perfect matching, so both even harmonics and odd harmonics are cancelled at the output current of each multiplier. This is an advantage of our analog multiplier.

4.6 Mismatch Effects

Mismatch effects in these circuits show up as a mismatch between the aspect ratios of the PMOS transistors (M1-M4) in the adder circuit of Fig. 2.2, and a mismatch between the aspect ratios of the NMOS transistors (M13-M16) in the multiplier circuit of Fig. 2.3 (a).

First, we consider the mismatch effect in the adder circuit. As shown in Fig. 2.2, assuming that the series connected transistor pair is mismatched uniformly, that is, the transconductance parameters of M1 and M3 are the same, $K_p + \Delta K_p / 2$, and the

transconductance parameters of M2 and M4 are the same, $K_p - \Delta K_p/2$. Then we can write the following equations,

$$\left(K_p + \frac{\Delta K_p}{2}\right) (V_{dd} - V_1 - |V_{tp}|)^2 = \left(K_p - \frac{\Delta K_p}{2}\right) (V_a - |V_{tp}|)^2 \quad (4.10)$$

$$\left(K_p + \frac{\Delta K_p}{2}\right) (V_{dd} - V_a - |V_{tp}|)^2 = \left(K_p - \frac{\Delta K_p}{2}\right) (V_o - V_2 - |V_{tp}|)^2 \quad (4.11)$$

Because usually $\Delta K_p/K_p$ is very small (less than 5%), and $|V_{tp}|$ is around 0.68 V, then we can simplify the above equations to the following,

$$\left(K_p + \frac{\Delta K_p}{2}\right) (V_{dd} - V_1)^2 = \left(K_p - \frac{\Delta K_p}{2}\right) V_a^2 \quad (4.12)$$

$$\left(K_p + \frac{\Delta K_p}{2}\right) (V_{dd} - V_a)^2 = \left(K_p - \frac{\Delta K_p}{2}\right) (V_o - V_2)^2 \quad (4.13)$$

If we set $\alpha = \sqrt{\left(K_p - \frac{\Delta K_p}{2}\right) / \left(K_p + \frac{\Delta K_p}{2}\right)} = \sqrt{\left(1 - \frac{\Delta K_p}{2K_p}\right) / \left(1 + \frac{\Delta K_p}{2K_p}\right)}$, then

the output V_o of the adder can be rewritten as,

$$V_o = \frac{V_{dd}}{\alpha} - \frac{V_{dd}}{\alpha^2} + \frac{V_1}{\alpha^2} + V_2 \quad (4.14)$$

The conclusion drawn from equation (4.14) is that output V_o of the adder is distorted somewhat when considering the mismatch effect in the adder circuit. If we do not consider the mismatch effect between the aspect ratios of the NMOS transistors (M13-M16) in the multiplier circuit of Fig. 2.3 (a) now, applying the conclusion of equation (4.14) into equation (1.16), the output current of the multiplier becomes

$\delta K_n yz/\alpha^2$. So the error appears, to a first-order approximation, as a scaling factor in the output current.

If we consider the mismatch effect between the aspect ratios of the NMOS transistors (M13-M16) in the multiplier circuit, the situation becomes more complicated. Except for the desired output item of $\delta K_n yz/\alpha^2$, there are many undesired items that also include signal components y or z . However, these errors can be significantly reduced in most cases by using symmetrical layout methods.

CHAPTER 5

SIMULATION AND EXPERIMENTAL RESULTS

5.1 Simulation Results

To verify the theoretical analyses, the design was built and simulated in a $0.18\mu\text{m}$ N-well CMOS process with Spectre using a level 28 model. The supply voltage was set at 3.3V , and V_{ref} at 1.75V . Fig. 2.3 was set up as multiplier, with aspect ratios of transistors M1-M12 set at $100\mu\text{m}/1\mu\text{m}$. The transistors used to generate the currents (e.g. M13-16 in Fig. 2.3) had aspect ratios of $20\mu\text{m}/2\mu\text{m}$. The common mode inputs used were $Y=X=1.4\text{V}$, $Z=K=0.3\text{V}$. DC, AC and transient analyses were performed on the multiplier/divider to verify its operation.

5.1.1 DC Sweep

Usually a DC sweep is made by changing the value of a source. Under the condition of $K_2-K_1=0.1\text{V}$, $X_2-X_1=0.1\text{V}$, $Z_2-Z_1=0.2\text{V}$, a DC sweep over Y_1 for the $W=V_{out}$ was performed, and the simulation result is shown in Fig. 5.1. Theoretically, the slope of output signal W equals to that of signal Y_1 with a 50 mV DC offset.

From this simulation result, we note that the slope of output signal W is very close to that of signal Y_1 , and DC offset is close to 50 mV within the simulated range.

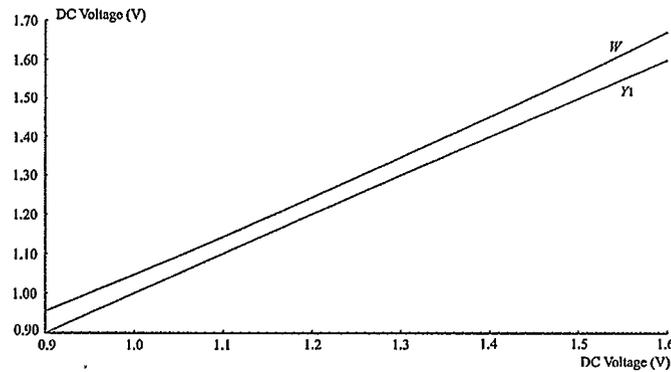


Figure 5.1. Simulation result of DC sweep over Y_1 for W .

5.1.2 AC Sweeps

Under the condition of $K_2-K_1=0.1\text{V}$, $Z_2-Z_1=0.1\text{V}$, $X_2-X_1=0.1\sin(2\pi ft)$ V, the AC response of the multiplier/divider was also examined to determine its high frequency performance. The simulation result is shown in Fig. 5.2. The 3dB bandwidth is located between 1.24 MHz and 20 MHz. It shows that W begins to change from 1.24 MHz, and it is not a simple one-pole response perhaps due to the pole created by parasitic capacitor c_o cannot be ignored at higher frequencies. It also indicates that the “ideal” bandwidth of the analog divider is close to 1.24 MHz, and this value matches with the “ideal” bandwidth of 1.1 MHz as we predicted in section 3.4.

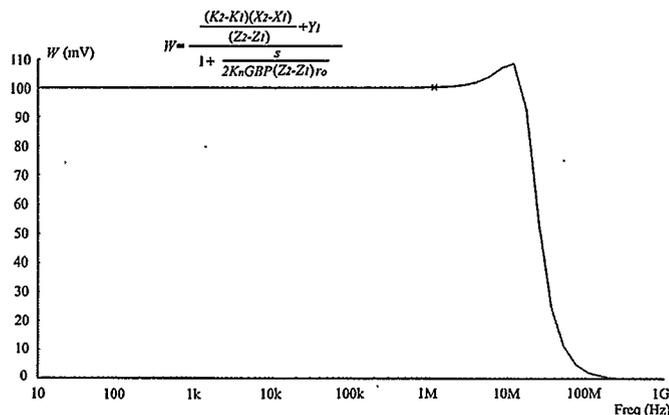


Figure 5.2. Simulation result of AC sweep over X_2-X_1 for $Z_2-Z_1=0.1\text{V}$.

As we stated earlier in section 3.4, the bandwidth of the analog divider is proportional to the magnitude of input signal (Z_2-Z_1) . The AC response was also examined to verify it under the condition of $Z_2-Z_1=0.05V$, with other input parameters the same as in previous test. The simulation result is shown in Fig. 5.3. The 3dB bandwidth is located between 0.5 MHz and 9.4 MHz. It shows that W begins to change from 0.5 MHz, which indicates that the “ideal” bandwidth of the analog divider decreases to 0.5 MHz, and this value matches with the “ideal” bandwidth of 0.56 MHz as we predicted in section 3.4.

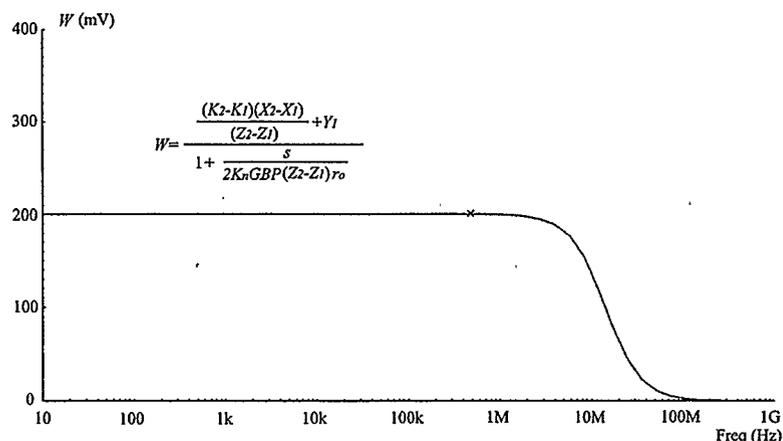


Figure 5.3. Simulation result of AC sweep over X_2-X_1 for $Z_2-Z_1=0.05V$.

5.1.3 Transient Analysis

For a transient analysis simulation, two sine waves were used as the inputs in order to verify operation. Under the condition of $K_2-K_1=0.1\sin(2\pi 1000t)V$, $X_2-X_1=0.1\sin(2\pi 30000t)V$, $Z_2-Z_1=0.1V$, Fig. 5.4 shows the output waveform of the multiplier/divider acting as a modulator, using two sinusoidal modulating waveforms. Fig. 5.5 shows FFT results of the multiplication output waveform W . We can find some

distortion products exist except the two desired output components with frequency of 29 kHz and 31 kHz, respectively. These distortion products perhaps come from threshold voltage mismatching, non-linearity in the CMFB loop introduced by using MOSFETs to sense the CM voltage, mobility degradation due to overdrive voltage, and so on.

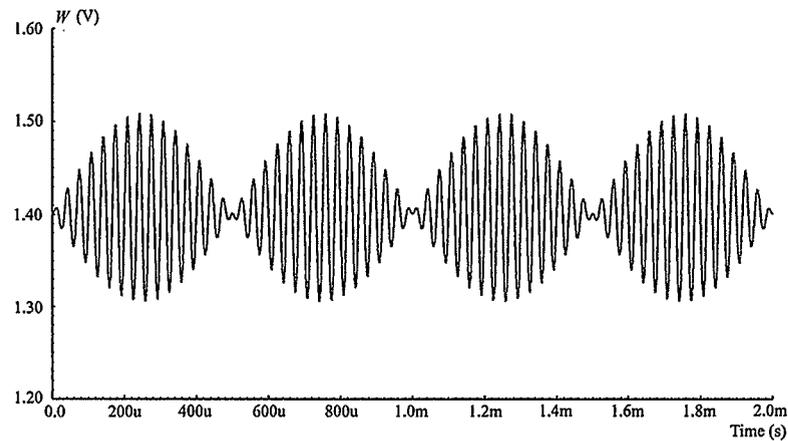


Figure 5.4. Simulated output waveform for multiplication.

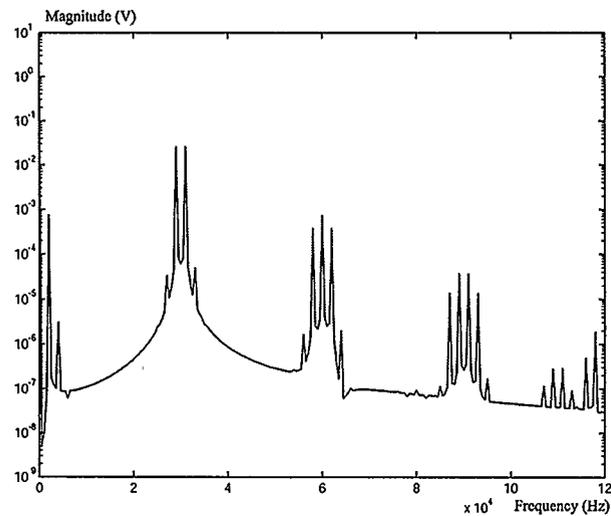


Figure 5.5. FFT results of the multiplication output waveform W .

Fig. 5.6 shows the simulated transient response of the circuit when functioning as a divider. In this case, the output voltage $W=V_{out}$ was an inverting function of a triangular

wave signal. The simulation conditions were $K_2-K_1=0.1V$, $X_2-X_1=0.1V$. Here Z_2-Z_1 was the triangular waveform with $T=10\mu s$, maximum magnitude $0.2V$, minimum magnitude $0.05V$. Compared with Matlab simulation results as shown in Fig. 5.7, the simulated values achieved 2% accuracy.

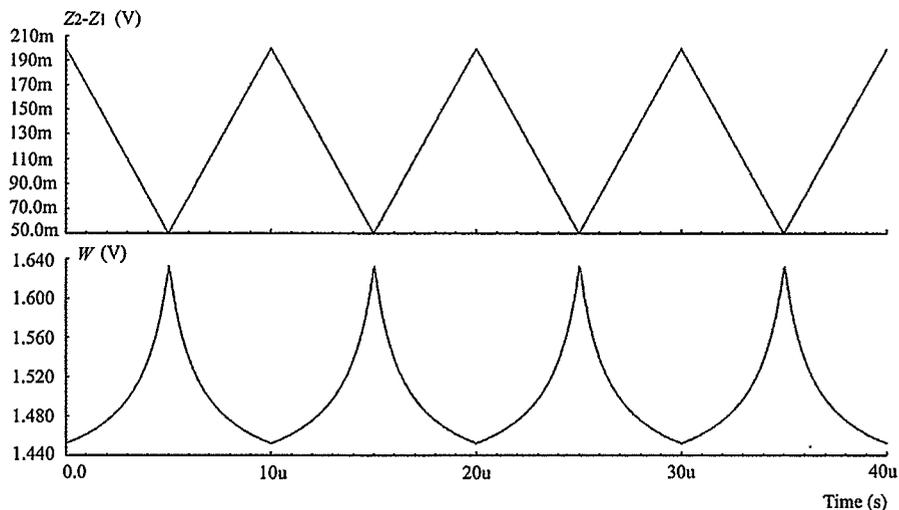


Figure 5.6. Simulated transient response for the divider function.

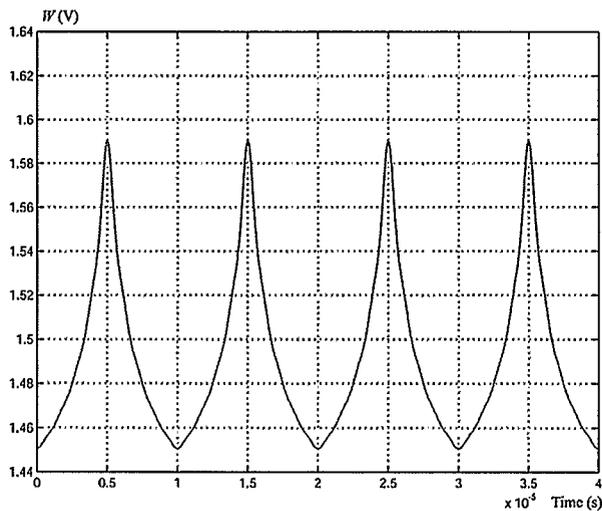


Figure 5.7. Matlab simulation results of the division operation.

The total harmonic distortion (THD) of the circuit was also checked, from the simulated results, this value was less than 2% under the condition of $K_2-K_1=0.1V$, $Z_2-Z_1=0.1V$, $X_2-X_1=0.1\sin(2\pi \times 10^6 t)$ V.

5.2 Experimental Results

A multiplier/divider based on this approach was fabricated via The Canadian Microelectronics Corporation (CMC) in a 40 pin-DIP package using TSMC CMOS 3.3V, 0.18 μ m process. The overall chip size (bonding pad inclusive) is 1200 μ m x 500 μ m equivalent to an area of 0.6 mm². Sixteen circuit nodes (I/O and power supplies) were bonded for testing purposes. The chip layout is shown in Fig. 5.8.

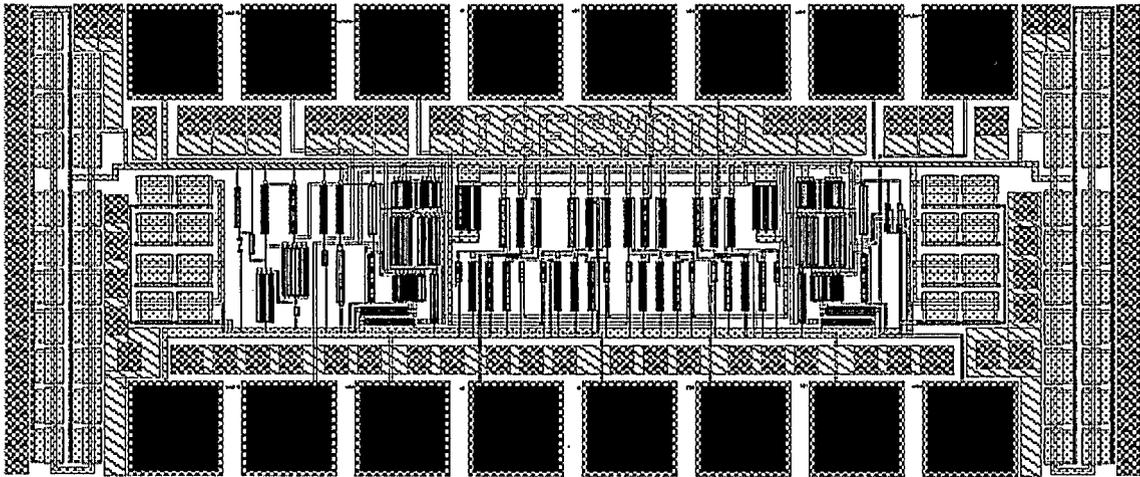


Figure 5.8. The layout of the new multiplier/divider.

5.2.1 Differential Signal Generator

In order to test the designed chip, we need to generate the appropriate input differential signals.

One circuit to generate differential signals is shown in Fig. 5.9. In this figure, V_{DC} represents DC common mode voltage, and V_{AC} represents AC small signal.

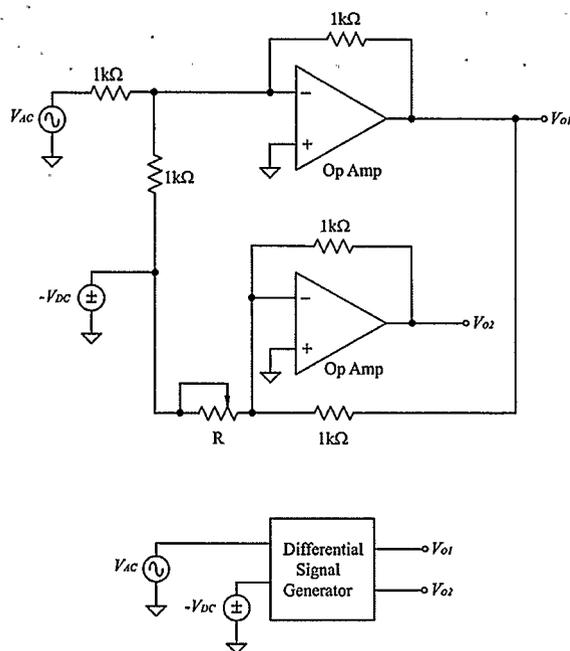


Figure 5.9. Differential signal generator.

Based on the op-amp's characteristic and superposition theory, straightforward analysis shows that,

$$V_{o2} = \left(\frac{1k\Omega}{Rk\Omega} - 1 \right) V_{DC} + V_{AC} \quad (5.1)$$

$$V_{o1} = V_{DC} - V_{AC} \quad (5.2)$$

We consider two cases as follows.

First, if we choose $R=0.5 \text{ k}\Omega$, then equation (5.1) becomes,

$$V_{o2} = V_{DC} + V_{AC} \quad (5.3)$$

So in this way we can generate two differential signals, and $V_{o2} - V_{o1} = 2V_{AC}$.

Second, if we set $V_{AC}=0$, and adjust the resistance of potentiometer R at the same time, $V_{o2}-V_{o1}$ becomes $(1k\Omega/Rk\Omega-2)V_{DC}$, in this way we can generate a DC offset voltage.

5.2.2 Chip Test Bench

The chip test bench is as shown in Fig. 5.10. Here ICFCYDIV is the designed analog multiplier/divider chip, X_{AC} , K_{AC} and Z_{AC} represent AC small signals, $X_{1,2}$, $K_{1,2}$ and $Z_{1,2}$ represent three differential input signals, and W represents the output signal.

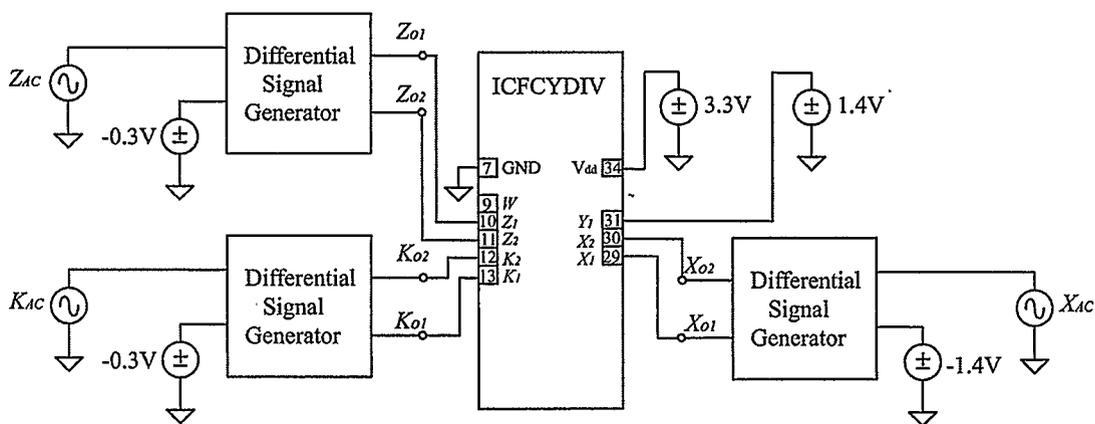


Figure 5.10. The chip test bench.

Three high-speed, wide bandwidth op-amp chips (LT1364CN8) were used for three differential signal generators. Two decoupling capacitors of $0.1\mu\text{F}$ and $10\mu\text{F}$ were connected between each power rail and ground.

The printed circuit board (PCB) used for testing ICFCYDIV is shown in Fig. 5.11.

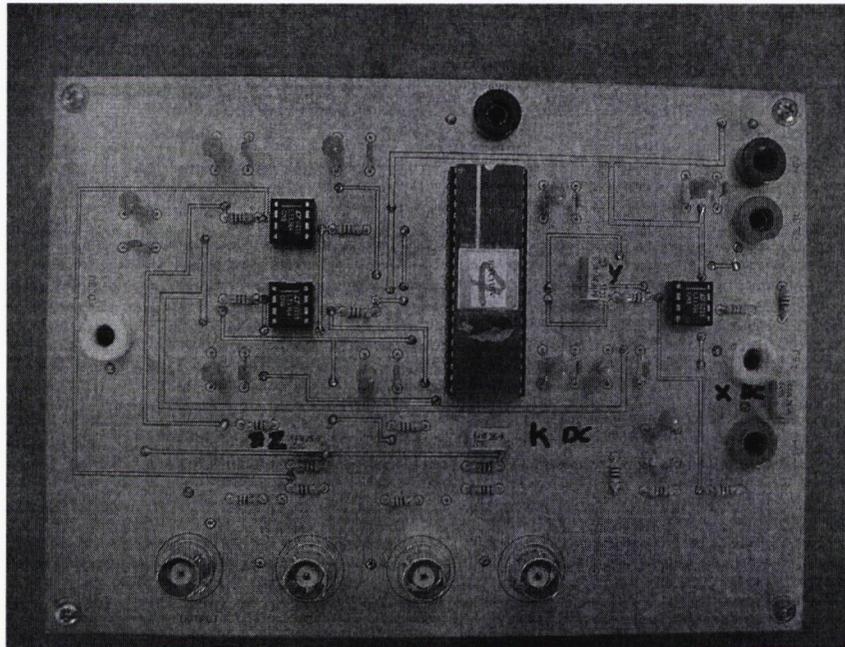


Figure 5.11. The designed PCB for testing ICFCYDIV.

5.2.3 Experimental Data Analysis

In order to analyze which subcircuit in the chip might be a problem in the case of chip cannot work properly, we bonded six internal nodes for this purpose. Please refer to Fig. 2.4, they include nodes V_{cm} , V_{ctrl} , V_d and V_e .

First we conducted a transient test. Two sine waves were used as the inputs in order to verify the chip's operation. Under the condition of $K_2-K_1=0.1\sin(2\pi 1000t)V$, $X_2-X_1=0.1\sin(2\pi 30000t)V$, $Z_2-Z_1=0.1V$, Fig. 5.12 (a) shows the measured waveform of output node W , and Fig. 5.12 (b) shows the measured waveform of internal node V_{cm} .

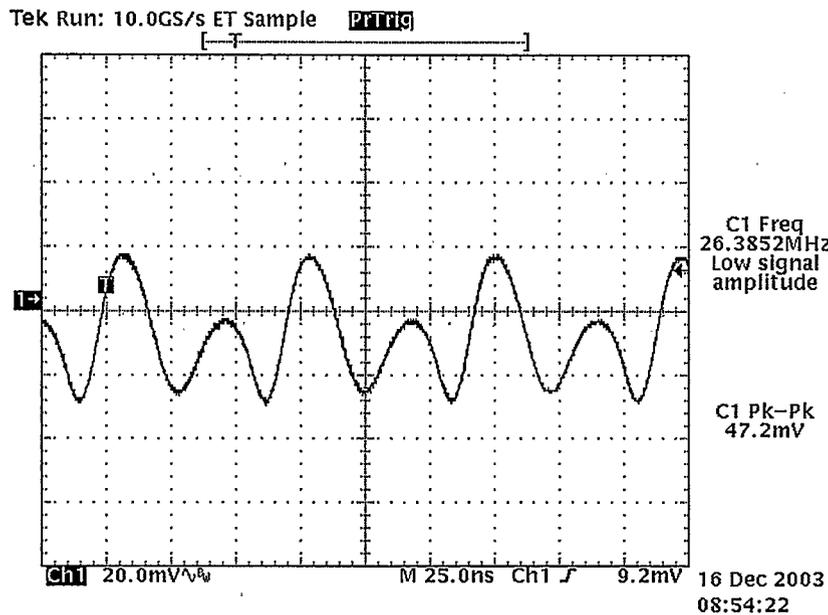


Figure 5.12 (a). The measured waveform of output node W .

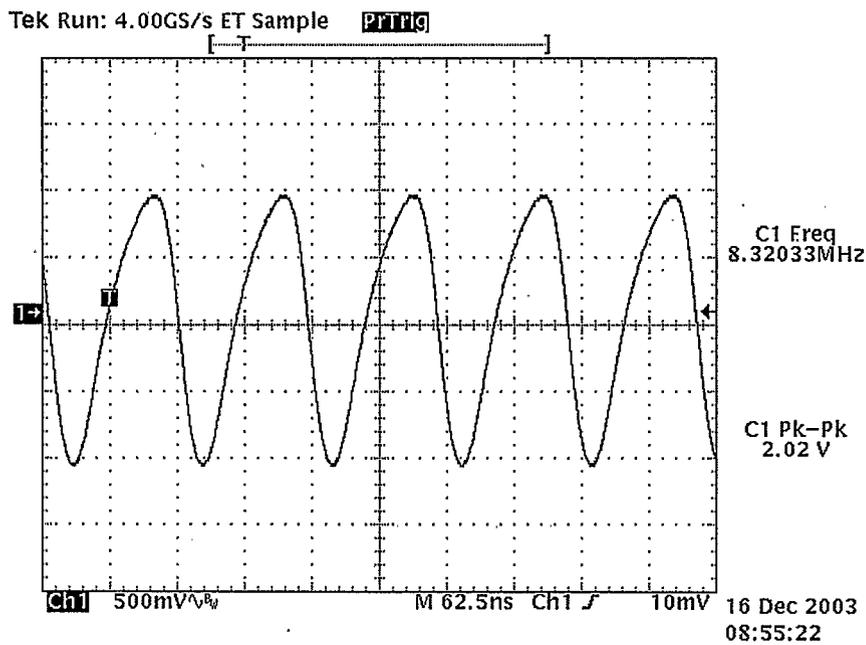


Figure 5.12 (b). The measured waveform of internal node V_{cm} .

The DC level of W is around to 3.2V, which is close to the chip voltage supply 3.3V. Fig. 5.12 (a) also showed that the output W was oscillating, and the CMFB circuit could not hold node voltages of V_{cm} , V_d and V_e at common mode reference voltage V_{ref} . Even as we set AC input signals to zero, the output W still kept oscillating.

From the above observation, we can draw the conclusion that there was a design error in the CMFB circuit that causes the problem of oscillation. In order to verify this conclusion (refer to Fig. 2.4), we series connected a very small pulse voltage source, of 10mV, to the reference voltage V_{ref} in the CMFB circuit, and did a stability test. The simulated waveforms of output W and internal node V_{cm} under stability test is shown in Fig. 5.13.

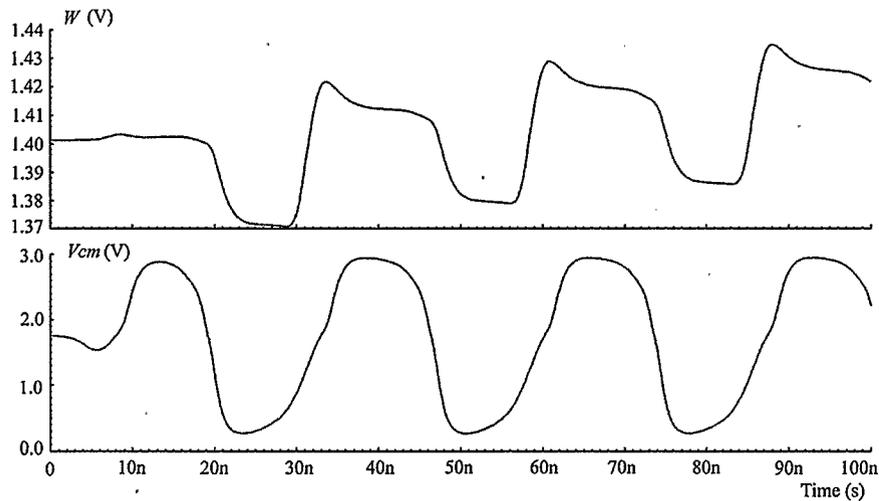


Figure 5.13. The simulated waveforms of W and internal node V_{cm} under stability test (old CMFB circuit).

From the above simulation results, we found that the values of W and V_{cm} were correct at the very beginning, and they began to oscillate after several nanoseconds. Eventually output W will go up to the upper limit of the chip voltage supply, which is 3.3V. These simulation results match the experimental results.

The loop gain response of the original CMFB circuit is shown in Fig. 5.15.

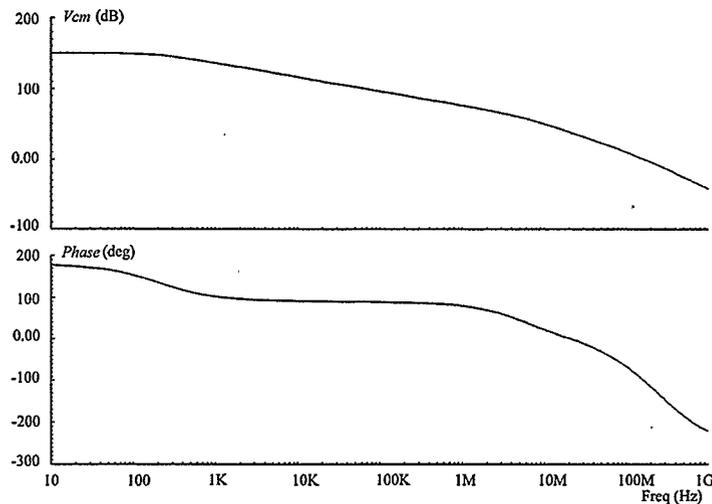


Figure 5.15. The loop gain response of the original CMFB circuit.

We find that at a frequency close to 21 MHz, the total phase shift of a signal proceeds from the input terminal, through the op-amp and feedback network, and back again to the input, is zero. At this frequency, the magnitude of the loop gain is close to 38.6 dB. We can conclude that the original CMFB circuit was unstable according to the Barkhausen criterion.

Now that we have identified the problem in the chip, we can correct the CMFB circuit design to ensure it is stable. Under this consideration, we adjust the op-amp design to a single stage differential amplifier without using any compensating capacitors in the op-amp, in other words, we just keep the first stage of our designed op-amp in section 2.5. This would significantly decrease phase shift at very high frequencies and benefit the stability in the common-mode loop. Also, a “crossover network” formed by R_c and C_c is used to effectively remove the amplifier from the feedback loop at high frequencies [42]. With this scheme, we can maintain loop stability. The correction to CMFB circuit is shown in Fig. 5.16.

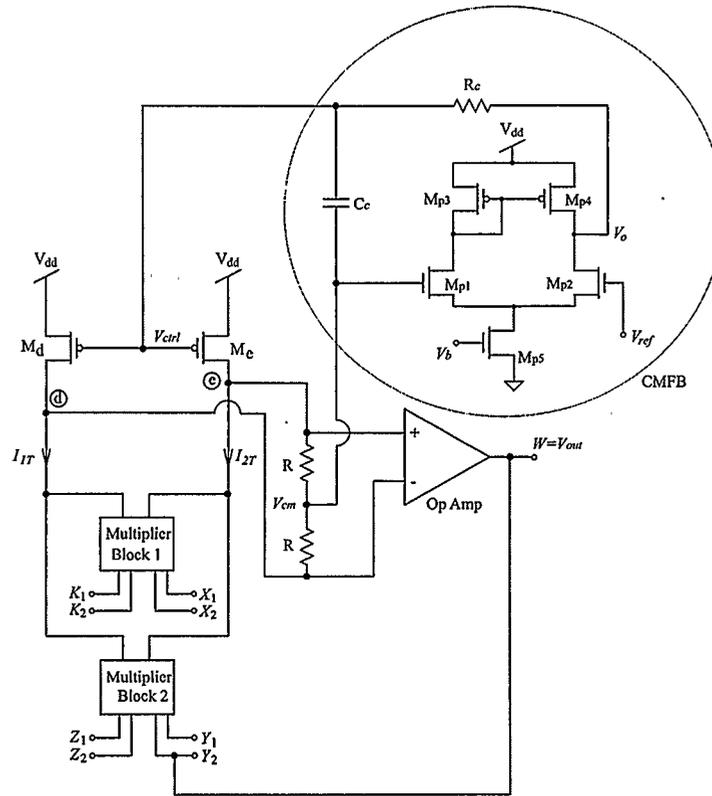


Figure 5.16. The corrected CMFB circuit.

The simulated AC magnitude and phase response of the single stage op-amp is shown in Fig. 5.17.

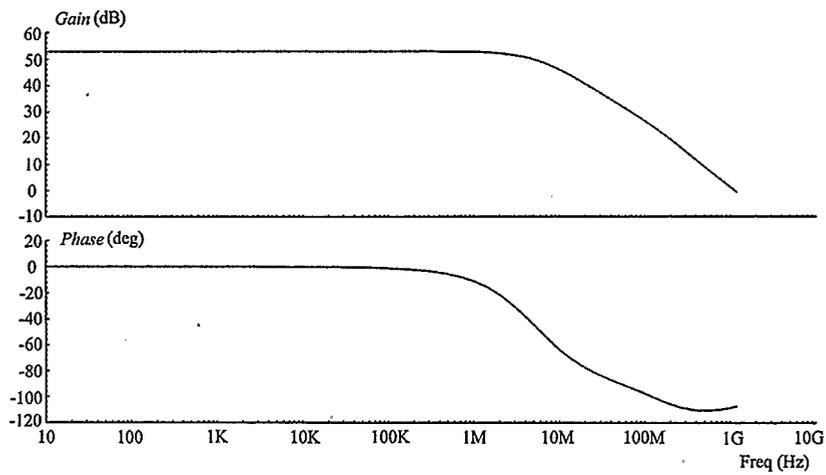


Figure 5.17. The simulated AC magnitude and phase response of the single stage op-amp.

We note that the DC gain was 53 dB, dominant pole frequency was 5 MHz, and the op-amp's gain bandwidth product (GBP) was 1.14 GHz. Here the point at which the open-loop gain is unity (0 dB) corresponds to a phase shift of -108° , or a 72° phase margin, so the designed op-amp is stable.

In order to decide the values of R_c and C_c to ensure stability of the common-mode loop (see Fig. 5.16), if the op-amp's open loop gain is $A(s)$, we can break the CMFB loop and write the following equations:

$$V_{ref} = 0 \quad (5.4)$$

$$V_o = A(s) \times (V_{cm} - V_{ref}) \quad (5.5)$$

$$(V_{cm} - V_{ctrl}) \cdot sC_c + \frac{(V_o - V_{ctrl})}{R_c} = 0 \quad (5.6)$$

Solving for V_{ctrl}/V_{cm} , yields the equation (5.7) as follows:

$$\frac{V_{ctrl}}{V_{cm}} = \frac{A(s) + sR_cC_c}{1 + sR_cC_c} \quad (5.7)$$

If the op-amp's open loop gain is characterized by $A(s) \cong GBP/s = A_0\omega_a/s$, where ω_a is the op-amp dominant pole, and A_0 is the op-amp DC gain, then we arrive at one pole at the origin, and another pole at $-1/R_cC_c$ from equation (5.7). This means that the transfer function of the common-mode loop is unstable. It implies that the designed op-amp dominant pole frequency cannot be small.

However, if the op-amp's open loop gain is characterized by $A(s) = GBP/(s + \omega_a) = A_0\omega_a/(s + \omega_a)$, then equation (5.7) becomes,

$$\frac{V_{ctrl}}{V_{cm}} = \frac{A_0 \omega_a + sR_c C_c (s + \omega_a)}{(1 + sR_c C_c)(s + \omega_a)} \quad (5.8)$$

From equation (5.8), we note that it is a two-pole system, and we can choose $1/R_c C_c \ll \omega_a$ to let the CMFB circuit stable. As we mentioned above, the op-amp's dominant pole frequency was 5 MHz, so we chose $R_c = 5 \text{ k}\Omega$ and $C_c = 100 \text{ pF}$ (off-chip capacitor) to meet the requirement.

In order to verify this conclusion, refer to Fig. 5.16, we conducted the stability test again. The simulated waveforms of output W and internal node V_{cm} under the stability test is shown in Fig. 5.18. We note that these signals become stable now.

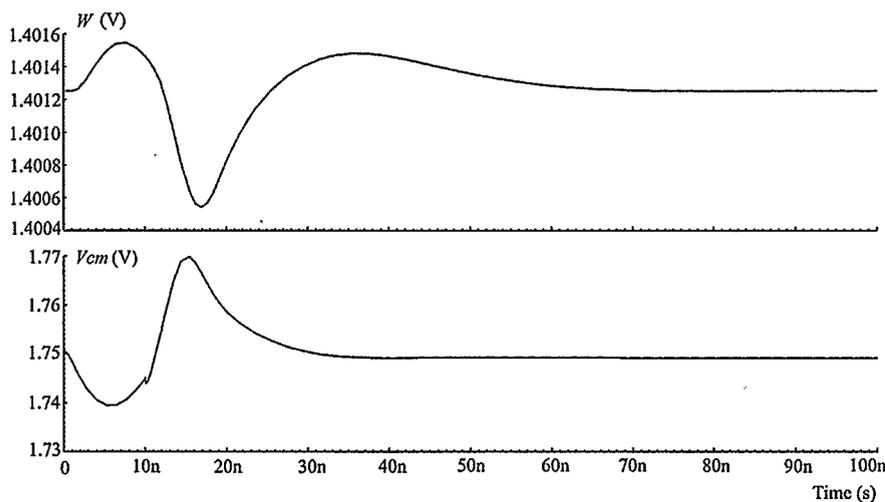


Figure 5.18. The simulated waveforms of W and internal node V_{cm} under stability test (using the new CMFB circuit).

Similarly, we can test loop gain response of the corrected CMFB circuit. The loop gain response of the corrected CMFB circuit is shown in Fig. 5.19.

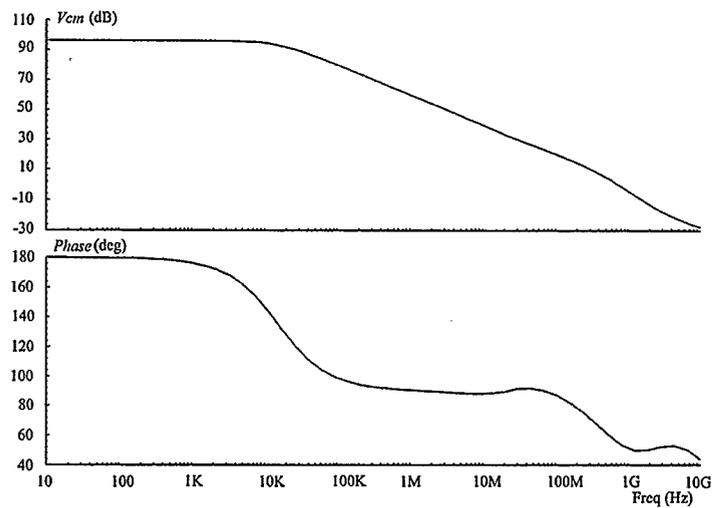


Figure 5.19. The loop gain response of the corrected CMFB circuit.

We find that the total phase shift of a signal proceeding from the input terminal, through the op-amp and feedback network, and back again to the input, never crosses zero. We can conclude that the corrected CMFB circuit is stable according to the Barkhausen criterion.

DC, AC and transient analyses were performed again on the corrected multiplier/divider to verify its operation. The simulation results were exactly the same as in section 5.1.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Summary

Presented in this thesis, is a novel four-quadrant CMOS analog multiplier/divider. Circuit principle and description, analysis, and a discussion of second order effects from an analog perspective, as well as simulation and experimental results were presented in the preceding chapters.

A novel four-quadrant CMOS analog multiplier/divider circuit based on the square-law model of the MOS transistor has been proposed. The proposed multiplier applies a new adder circuit suited for CMOS N-well process, and uses differential inputs to reduce common-mode signals and noise. The proposed divider uses two newly-proposed analog multipliers, a divider feedback path and a common-mode feedback (CMFB) circuit, which are easy to design and analyze, to realize the following transfer function: $W=(K_2-K_1)*(X_2-X_1)/(Z_2-Z_1)+Y_1$, where W is the output, $K_{1,2}$; $X_{1,2}$ and $Z_{1,2}$ are differential inputs and Y_1 is a DC bias voltage. Spectre(S) simulation results from a chip design using a 3.3V, 0.18 μ m CMOS process show that the 3dB bandwidth of the analog divider is proportional to the magnitude of input signal (Z_2-Z_1), and a 3dB bandwidth of 11 MHz is achievable.

Experimental results from chips show that there was a design error within the CMFB circuit that caused the output signal to oscillate. The reason has been identified

and a corresponding correction to the chip design has been analyzed and verified in simulation.

6.2 Contribution

The main work in this thesis was written in a paper entitled “A Novel Four-Quadrant CMOS Analog Multiplier/Divider”, which was accepted by IEEE International Symposium on Circuits and Systems (ISCAS) 2004. Some of the contributions of this work include:

- Development a new adder circuit suited for N-well process.
- Development a fully differential analog multiplier.
- Development a new voltage-mode analog divider architecture.
- Detailed analysis of R-C network design to eliminate oscillation within a common-mode loop.

6.3 Future Work

This thesis represents new research work on the development and implementation of a CMOS analog multiplier/divider.

The proposed analog multiplier/divider in this thesis was based on a 3.3V single-ended, voltage-mode circuit implementation, just to serve as a proof of concept. It is of further interest to develop, design and fabricate a fully differential circuit implementation. Application of two power supply rails will let the analog multiplier become fully four-quadrant.

Also, foreseeable future work would be to correct the CMFB circuit in the chip, and further experimental tests on the chips can be implemented.

Finally, an improved op-amp design within the divider feedback loop to realize the analog divider will improve the performance of the analog multiplier/divider.

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