THE UNIVERSITY OF CALGARY

A New Analysis of Charge Injection Error in Analog MOS Switches

by

Saeed Aghtar

A DISSERTATION

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE

DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

CALGARY, ALBERTA

APRIL, 1998

© Saeed Aghtar 1998

National Library of Canada
Acquisitions and Bibliographic Services
395 Wellington Street
Ottawa ON K1A 0N4
Canada

Bibliothèque nationale du Canada
Acquisitions et services bibliographiques
395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence

Our file Notre référence

The author has granted a non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of this thesis in microform, paper or electronic formats.

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de cette thèse sous la forme de microfiche/film, de reproduction sur papier ou sur format électronique.

The author retains ownership of the copyright in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

L'auteur conserve la propriété du droit d'auteur qui protège cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

0-612-31011-6

Canada

Abstract

A new charge injection error analysis of MOS analog switches is developed in this work. Second order effects are included in the new analysis in order to obtain a more accurate prediction of the final charge injection error. The second order effects to be discussed in this work are the subthreshold current, gate-source capacitance variation and drain current in the moderate inversion regionn. Also, a comprehensive study of the importance of each effect with regard to the most important electrical and process parameters involved with switch charge injection error is performed. The results show that the second order effects studied in this work can have a significant impact on the final charge injection error calculation and therefore, they need to be considered in the simulation of switching circuits.

An analytical model is also developed for the simple case where input source resistance and capacitance are ignored. This model provides excellent physical insight into switch charge injection with regard to the subthreshold current and gate-source capacitance variation effects.

In addition, a new dc model for MOS transistors which provides excellent results for the drain current calculation in all regions of operation including the moderate inversion region is proposed. The new model is simple and provides a smooth transition in the moderate inversion region between the subthreshold and strong inversion regions of operation. This model is used to improve the accuracy of the new charge injection model discussed in this work.

Finally, the comprehensive model developed for the general case of switch charge injection can be used for accurate prediction of the final error voltage

for various combinations of electrical and process parameters.

Acknowledgments

The success achieved as a result of the four-year work that went into the completion of this dissertation could not have been accomplished without the support and interest of a number of people.

I thank my supervisor Dr. J. W. Haslett for giving me freedom to pursue my own ideas, to make mistakes, and to learn. He must be especially acknowledged for his scholarly advice, sacrifice of time and thoughtful editing of this thesis. Also, his generous financial support ensured that I could devote all of my time to my studies.

Dr. F. N. Trofimenkoff was an invaluable resource. Without his help and insight into the physics of semiconductors, completion of this thesis would have been more difficult.

I am deeply grateful to all my teachers and friends who helped me in many ways.

Pursuing my studies abroad would have been difficult without the financial support of The Iranian Ministry of Culture and Higher Education for which I am very grateful. Partial financial support of the Department of Electrical and Computer Engineering of The University of Calgary is acknowledged as well.

My parents have always supported and encouraged my pursuit of learning. I feel eternal gratitude for the sacrifices they have made for me.

I was also fortunate enough to have met my wife, Leila, during this period. Her support, patience and encouragement made the completion of this dissertation much easier.

To My Parents,

Fatemeh and Gholamreza

and

My Wife,
Leila

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 MOS Analog Switches

One of the most important elements in analog MOS switching circuits is the MOS switch. This element is particularly important in widely used applications such as sample and hold (S/H) stages, analog to digital (A/D) and digital to analog (D/A) converters, switched capacitor filters and switched current circuits. In these applications, the performance of the analog switches can have a significant impact on the overall circuit accuracy.

MOS technology is well known for its capability of implementing high performance analog switches. In this technology, a single transistor can be used as an analog switch with its gate voltage controlling the resistance between its source and drain. In addition to simplicity, an MOS switch can provide high impedance between the input and output when off, and zero offset voltage when on. However, an MOS analog switch is not an ideal switch. The injection of parasitic charges from the channel and gate-source/gate-drain overlap capacitances into the source and drain terminals degrades the circuit performance. This is one of the major limiting factors in high precision and fast analog switching circuits. Because of its importance,

an accurate analysis of this effect is critical in the simulation of switching circuits and the development of error cancellation techniques.

1.2 Switch Operation

The operation of an analog switch can be demonstrated by the simple sample and hold circuit shown in Fig. 1.1. This arrangement is also encountered in switched capacitor and switched current circuits. In this circuit, the MOS transistor performs as an analog switch between the input source (V_{in}) and capacitive load (C_L).

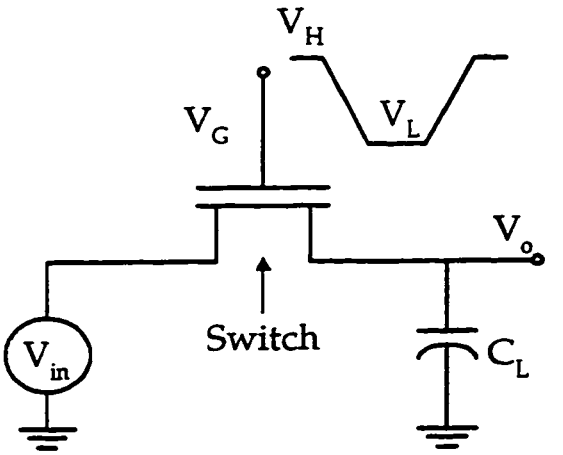

Figure 1.1: A simple sample and hold circuit.

At high gate voltage ($V_G = V_H$), the transistor is ON and behaves as a resistor provided that $V_G > V_{in} + V_T$. The on-resistance can be expressed as

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}, \tag{1.1}$$

where μ_n is the electron mobility in the channel, C_{ox} is the gate-oxide capacitance per unit area, W and L are the effective width and length of the transistor, respectively, V_{GS} is the gate-source voltage and V_T is the threshold

voltage. Provided that the gate voltage stays at V_H long enough, the load capacitance is charged completely and the output voltage (V_o) reaches the input voltage. This is referred to as the *sampling state* in sample and hold circuits.

R_{on} and C_L determine the acquisition time and as a result the maximum sampling rate in sample and hold circuits. They also limit the speed and accuracy of switched capacitor and switched current circuits. Therefore, high speed and high precision applications require large transistor sizes and small load capacitances in order to minimize the circuit time constant ($R_{on}C_L$) and maximize the speed for a given accuracy. R_{on} can also be decreased by increasing V_{GS}. However, this voltage is limited by the power supply voltage that is small in modern standard processes.

At low gate voltage ($V_G = V_L$), the transistor turns off provided that $V_L < V_{in} + V_T$. When the transistor is OFF, a large resistance is introduced between the input source (V_{in}) and the load capacitance (C_L) which isolates the output node from the input node. Therefore, the output voltage is held by the load capacitance (C_L). This phase of operation is referred to as the *holding state*. Any error caused during the switch turn-off transient can change the sample signal at the output and degrade the overall circuit performance.

1.3 Clock Feedthrough and Channel Charge Injection

In the sampling circuit of Fig. 1.1, the transistor carries a certain amount of charge in its channel that can be expressed as

$$Q_{ch} = WLC_{ox}(V_{GS} - V_T). \tag{1.2}$$

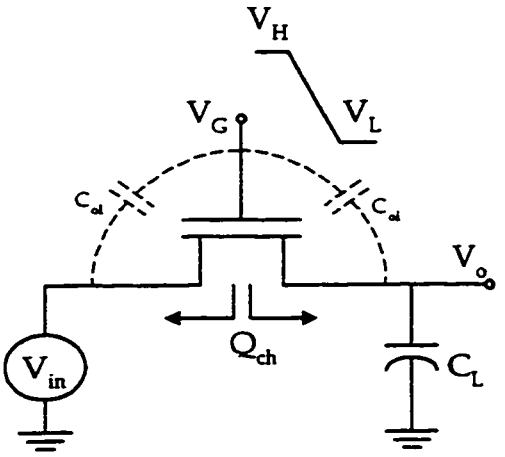

Figure 1.2: MOS switch charge injection.

When the transistor turns off, this charge leaves the channel through the source and drain terminals (Channel Charge Injection) and substrate (Charge Pumping Effect). The charge pumping effect is negligible in most practical cases [1]. The injected charge changes the total charge stored on the sampling capacitor and introduces an output error voltage. The amount of charge transferred to the holding node depends on the gate voltage falling rate from high (V_H) to low (V_L). At low gate voltage falling rates, most of the channel charge returns to the source (V_{in}) so that the output error voltage due to the channel charge is negligible. At high falling rates, however, almost half of the channel charge is directed into the holding node. This causes an error voltage ($Q_{ch}/2C_L$) at the output.

Another source of error in MOS switches is clock feedthrough, caused by the finite overlap capacitance between the gate and source or drain terminals. As shown in Fig. 1.2, when the gate control voltage (V_G) changes state from V_H to V_L to turn off the switch, the overlap capacitance (C_{ol}) changes the

voltage stored on C_L by an amount equal to

$$\Delta V_o = \frac{C_{ol}}{C_{ol} + C_L}.(V_H - V_L). \tag{1.3}$$

This error is independent of the input signal and appears as an offset error at the output.

In the literature, the term *Charge Injection* often refers to both channel charge injection and clock feedthrough.

1.4 Charge Injection Error Analysis

Because of the importance of the charge injection error in MOS analog switching circuits, many attempts have been made to cancel or decrease this error in different circuit configurations. Some of the most widely used cancellation techniques are the fully differential circuit approach [2], the dummy switch compensation technique [3] and replacing single transistor switches with transmission gates. These techniques cancel switch charge injection only to first order.

Comprehensive understanding and detailed analysis of switch charge injection are required for the development of cancellation techniques and design of the appropriate circuits to improve the accuracy of MOS switching circuits.

Most of the analyses proposed in the literature take into account only first order effects. Therefore, they are capable of characterizing the charge injection error to the first order which is sufficient in some applications. To design high performance integrated circuits, however, a precise model for charge injection error which also includes second order effects is required. For instance, in high precision A/D converters [4, 5] and sample and hold circuits where absolute error is of prime interest, using an accurate model for charge injection error can help determine the optimized switch sizes in

the presence of other error sources. In addition, this model can be used to examine the efficiency of charge injection cancellation techniques. The accuracy of the model is particularly important in simulation and analysis of new generation of IC designs where low power supply voltages and smaller holding capacitances are used.

1.5 Literature Review

The charge injection error problem was identified in the very first publications on switched-capacitor circuits [3]. Attempts have been made to model switch charge injection error using the simplified circuit of Fig. 1.1, to which most practical charge injection problems can be reduced. A qualitative observation regarding a simplified case assuming infinite source capacitance, C_S, was made by MacQuigg [6]. Sheu and Hu proposed an analytical model for this simple case which takes into account the strong inversion characteristics and gate-source overlap capacitance of the MOS transistor switch [7]. Equations for the general case of Fig. 1.3 were derived and solved numerically by J.H. Shieh et al. [8,9]. This model was also validated with experimental evi-

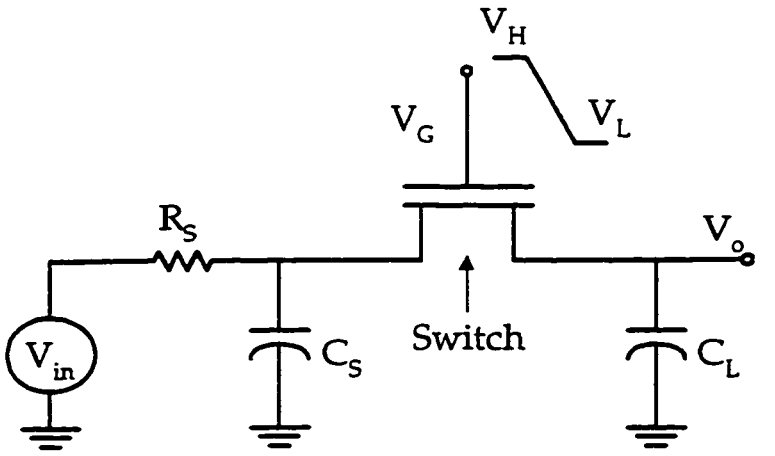

Figure 1.3: The general case for the charge injection error problem.

dence and its limitations were delineated by G. Wegmann et al. [1]. By using the continuity equation, this study also showed that an equivalent lumped model for the transistor provides satisfactory results for practical situations. The negligible influence of substrate current, which simplifies the model to a unidimentional model, was also shown. The charge injection problem in transmission gates was studied by Eichenberger et al [10]. This analysis is based on the analytical model presented by Sheu and Hu [7].

All aforementioned analyses take into account first order effects such as the channel current and gate-source capacitance in the strong inversion region. Second order effects such as the subthreshold current and gate-source capacitance variations in the MOS transistor switch are ignored. Also, the drain current model used for these analyses is not accurate enough particularly in the moderate inversion region where the gate-source voltage is near threshold. Different charge conserving non-quasi-static (NQS) models have also been proposed for the transient analysis of a transistor and used for the charge injection error calculation [11, 12]. Although these models guarantee node charge conservation [12] and the results are found to be in very good agreement with the experimental results, they are very complicated and computationally inefficient.

Second order effects such as the subthreshold current and weak inversion channel charge have recently been observed and studied [13–16]. It has been shown that the contribution of these effects to the final charge injection error can be comparable to those of the channel charge in strong inversion and gate-source overlap capacitance. Y. Gu et al. [15] recently derived an expression to take into account the weak inversion channel charge effect. This model can only predict the final error and therefore it cannot be used for transient time analysis. Also, an analytical expression cannot be derived due to an integral function evaluation in the model. This makes the model inappropriate for use in circuit simulators. In addition, the subthreshold current and gate-source

capacitance variations are ignored in this analysis. The model also cannot be applied to the general case where the source resistance and capacitance are finite.

1.6 Research Objective

The importance of charge injection error analysis and accurate modelling of this effect were discussed previously. The lack of a charge injection error model which takes into account the second order effects was also explained in Section 1.5.

The objective of this work is to develop a comprehensive switch charge injection model which can accurately predict the error due to this effect in MOS analog switching circuits. The following issues need to be considered in the development of the new model.

Subthreshold Current The drain current below the MOS transistor threshold voltage needs to be included in the model. This current has not been considered in previous work.

Weak Inversion Channel Charges The inversion layer charge of the switch transistor fades as the gate-source voltage drops below the threshold voltage. However, in most of the charge injection error analyses this variation is ignored and the weak inversion channel charge is assumed to be zero.

Gate-Source Capacitance Variations in Strong Inversion In all the charge injection error analyses reported in the literature, the MOSFET gate-source capacitance is assumed constant in the strong inversion region. However, as accurate MOSFET models show, this capacitance varies with respect to the gate-source voltage. This variation needs to be taken into account in a precise switch charge injection model.

Modelling of the MOSFET Drain Current The drain current of the switch transistor compensates part of the charge injected from the transistor channel and the gate-source overlap capacitance. Therefore, accurate modelling of this current in all regions of operation is of great importance to the switch charge injection error analysis.

Applicable to the General Case Although most of the charge injection problems can be reduced to the simple case of Fig. 1.1, the switch charge injection model should be capable of modelling this effect in the general case where the switch is connected to an input with non-zero capacitance and resistance.

Computation Time To use the model for the simulation of large switching circuits, the proposed charge injection model should be computationally efficient.

Compatibility with Circuit Simulators To avoid the need for developing a new circuit simulator, the model should be compatible with one of the widely used programs such as SPICE.

Analytical Expression for the Final Error An analytical equation for estimating the final error can provide physical insight into the switching errors and possible compensation techniques. This analytical expression can be very useful even if it can only be derived for the simple switch arrangements.

The proposed analyses in this work cover all of these requirements.

1.7 Overview

To prepare a background on switch charge injection error analysis, the simple model proposed by Sheu and Hu [7] is explained in Chapter 2. The shortcomings of this model are also discussed.

Chapter 3 is devoted to the analysis of the subthreshold effects in analog switches. A new analytical model is developed based on Sheu and Hu's model which also takes into account the subthreshold current and weak inversion channel charges as well as the gate-source capacitance variations in strong inversion.

To improve the accuracy of the drain current calculation in the proposed model in Chapter 3, a new MOSFET dc model is developed in Chapter 4 which provides excellent results in all regions of operation including the moderate inversion region. Due to modelling difficulties, most MOSFET models fail to provide accurate drain current predictions in this region. The new model is compared with other models and experimental data.

Utilizing the proposed dc MOSFET model in Chapter 4, the model in Chapter 3 is modified in Chapter 5. This modified model is used to study the effect of switch transistor drain current on the charge injection error prediction. This effect is discussed especially with regard to the moderate inversion current. The validity of this model is also confirmed with experimental data.

In Chapter 6, the comprehensive model explained in Chapter 5 is used to study the general case of switching problems where the input source has a finite capacitance and resistance.

Finally, in Chapter 7 a summary and conclusion of this work is presented.

Chapter 2

Analysis of Charge Injection Error

An overview of the charge injection error analysis in different switch arrangements is given in this chapter in order to prepare a background for developing the new charge injection model in Chapter 3.

Various cases of switch charge injection are explained in Section 2.1. The charge injection model proposed by Sheu and Hu for the simple case where the source resistance and capacitance are ignored is discussed in Section 2.2. The results and shortcomings of this model are also reviewed. In Section 2.4, Sheu and Hu's model is applied to the special case where finite source resistance is assumed. The case with finite source capacitance and large source resistance is discussed in Section 2.5. A set of differential equations is also derived in Section 2.6 for the charge injection error prediction in the general case where both the source resistance and capacitance are taken into account. A summary is given in Section 2.7.

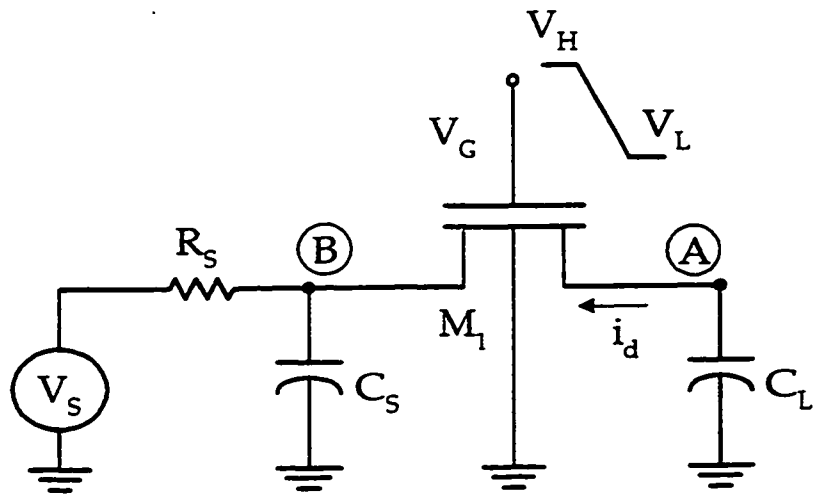

Figure 2.1: Circuit schematic in the general case of switch charge injection.

2.1 Various Cases of Switch Charge Injection

2.1.1 General Case

The circuit schematic corresponding to the general case of switch charge injection is shown in Fig. 2.1. In this figure, C_L is the load capacitance at the holding node, R_S and C_S are the input source resistance and capacitance, respectively, V_S is the input source and M_1 is the switch transistor. R_S and C_S could be the resistance and capacitance associated with the output of an operational amplifier.

When the transistor turns off, the channel charge and the charge on the gate-source/gate-drain overlap capacitances is divided between the drain and source nodes (A and B) depending on the values of R_S, C_S, C_L and the gate voltage falling rate (U). The charge injected into the output, node A, causes an error in the sampled voltage on C_L.

2.1.2 Special Cases

Figure 2.2 illustrates the special cases of switch charge injection. The case where the switch transistor is connected to the input source, V_S, with no resistance or capacitance is shown in Figure 2.2(a). In spite of its simplicity, most practical charge injection problems can be modelled in this way. An analytical expression for the final charge injection error at the output can be found in this case.

Figure 2.2(b) demonstrates the case where only the effect of input source resistance is taken into account. This case is not usually encountered in practice because when the source resistance is important the capacitance between node B and ground, which holds the voltage at node B, should also be considered. This capacitance is at least equal to the parasitic capacitance at node B.

Another special case where the input source resistance, R_S, is large enough so that the time constant $R_S C_S$ is much larger than the switch turn-off time, is shown in Fig. 2.2(c). In this case the channel charge is shared between C_S and C_L. For instance, when $C_S = C_L$ and the switch transistor is assumed symmetrical, half of the channel charge will be deposited to each capacitor. Otherwise, the amount of charge deposited into C_L depends on the ratio of C_S to C_L.

2.2 Sheu and Hu's Model

2.2.1 Analytical Charge Injection Model

This model was developed based on Fig. 2.2(a), assuming zero source resistance so that the switch transistor is connected directly to the ideal voltage source V_S [7]. The model is simple and provides analytical results for the output error voltage during the switch turn-off transient. It can also be modified

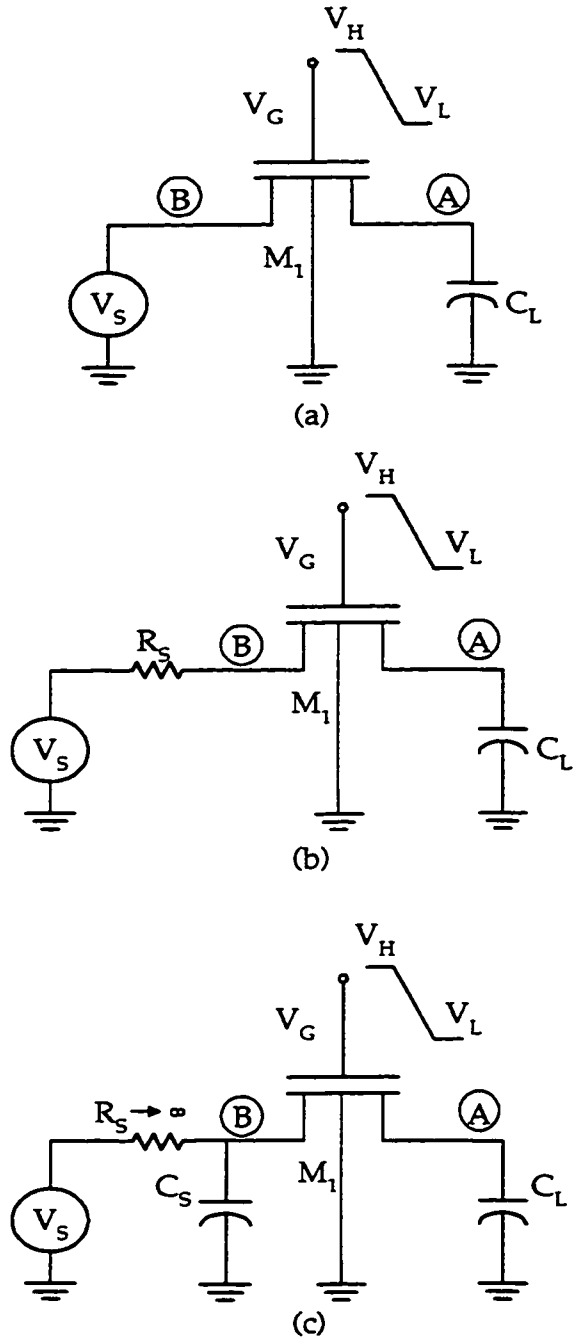

Figure 2.2: Special cases of charge injection. (a) No source resistance and capacitance. (b) No source capacitance. (c) Infinitely large source resistance.

to analyze the general case of switch charge injection (Fig. 2.1).

The fraction of the channel charge that escapes to the substrate (charge pumping effect [17]) is neglected in Sheu and Hu's model. This charge is due to trapping at the gate-channel interface and to recombination in the channel and in the substrate. In the practical case of switch transistors where short devices are usually used, this charge can be neglected. More specifically, the charge pumping effect is negligible when the channel transit time, T_0, is smaller than the gate voltage fall time [18, 19], where

$$T_0 = \frac{nL^2}{\mu (V_{GS} - V_T)}. \tag{2.1}$$

L is the transistor channel length, n is the subthreshold slope factor, μ is the carrier mobility and V_T is the threshold voltage. As equation (2.1) shows, the channel transit time is small in short channel devices and therefore the gate voltage fall time can be easily larger than T_0. For example, for the typical values of $n = 1.5$, $L = 5\mu m$, $\mu = 500 cm^2/V.s$, and $V_{GS} - V_T = 2.5V$, $T_0 = 3 \times 10^{-10} s$. However, the gate voltage fall time (V_H/U) even for $U = 10^9 V/s$ is $3.3 \times 10^{-9} s$ for $V_H = 3.3V$.

In Sheu and Hu's model, two phases of operation are considered during the turn-off transient as the gate voltage decreases. The two phases of operation correspond to the time periods $(0 - t_0)$ and $(t_0 - t_f)$ where t_0 is the time at which the switch enters cutoff. Also, a ramp function is assumed for the gate voltage as shown in Fig. 2.3.

In the first phase, the transistor is ON $(V_G \geqslant V_S + V_T)$ and the channel current i_d contributes to the cancellation of the charge injected by the gate-oxide capacitance (C_{ox}) and gate overlap capacitance (C_{ol}). The circuit schematic to be analyzed in this phase is shown in Fig. 2.4(a). It should be noted that the gate-source and gate-drain capacitances are modelled by two constant capacitors $\frac{C_{ox}}{2}$ and C_{ol}. In other words, the clock feedthrough and

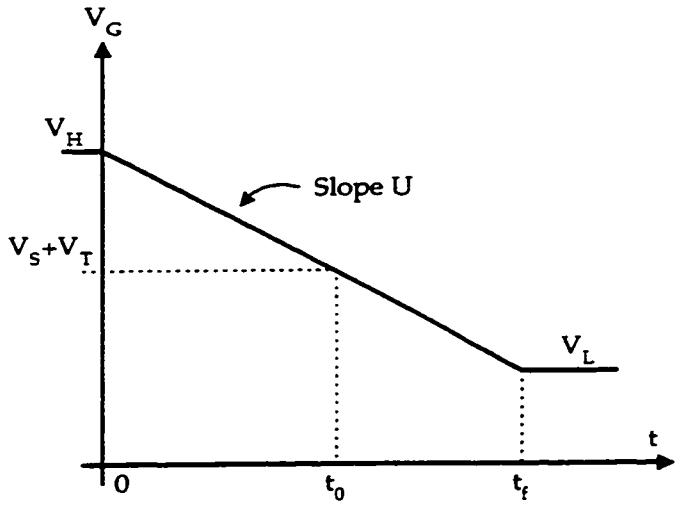

Figure 2.3: Definition of the applied gate voltage.

channel charge injection are modelled by C_{ol} and $\frac{C_{ox}}{2}$, respectively.

In phase 1, Kirchoff's current law (KCL) at the output node requires

$$C_L \frac{dv_d}{dt} = -i_d + \left(C_{ol} + \frac{C_{ox}}{2} \right) \frac{d\left(V_G - v_d\right)}{dt}, \tag{2.2}$$

where v_d is the error voltage at the drain end (output node) at time t. The gate voltage, V_G, can be written as

$$V_G = V_H - Ut, \tag{2.3}$$

where U is the gate voltage falling rate and V_H is the gate high voltage. Equation (2.3) is valid until V_G reaches the gate low voltage V_L (see Fig. 2.3).

In the switching problems encountered in practice, it can be assumed that $|dV_G/dt| \gg |dv_d/dt|$. This simplifies (2.2) to

$$C_L \frac{dv_d}{dt} = -i_d - \left(C_{ol} + \frac{C_{ox}}{2} \right) U. \tag{2.4}$$

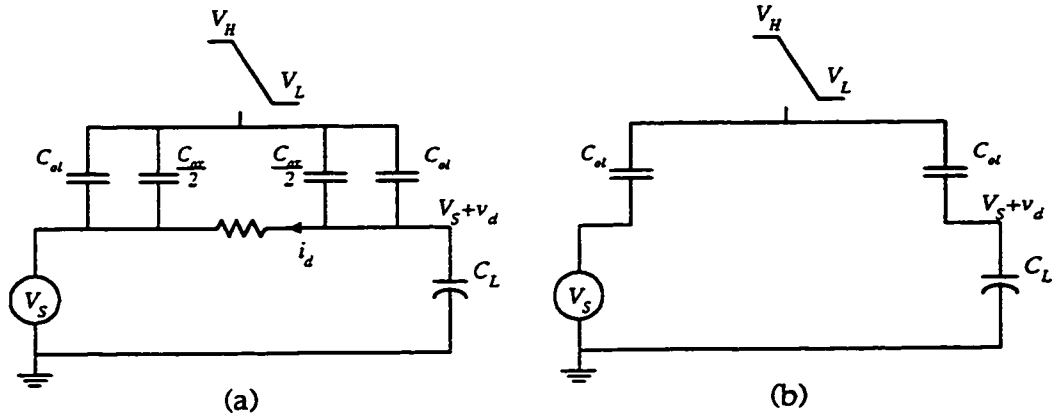

Figure 2.4: Equivalent model for the analog switch. (a) Transistor is ON. (b) Transistor is OFF.

When the switch transistor operates in the strong inversion region ($V_S+V_T \leqslant V_G \leqslant V_H$), i_d can be written as

$$i_d = \beta\,(V_{HT} - Ut)\,v_d, \tag{2.5}$$

assuming v_d is small so that the transistor operates in the linear region. In equation (2.5),

$$\beta = \mu C'_{ox}\frac{W}{L}, \tag{2.6}$$

$$V_{HT} = V_H - V_S - V_T, \tag{2.7}$$

and

$$V_T = V_{T0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \tag{2.8}$$

where C'_{ox} is the gate-oxide capacitance per unit area, ϕ_F is the Fermi potential, V_{SB} is the source-bulk voltage, V_{T0} is the threshold voltage at zero source-bulk voltage, and γ is the body effect coefficient.

Substituting equations (2.5) to (2.7) into (2.4) and solving for v_d gives

$$v_d(t) = -\sqrt{\frac{\pi U C_L}{2\beta}}\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_L}\right)\exp\left\{\frac{\beta U}{2C_L}\left(t-\frac{V_{HT}}{U}\right)^2\right\} \cdot\left\{\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}V_{HT}\right]-\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}(V_{HT}-Ut)\right]\right\}. \quad (2.9)$$

where "erf" is the error function defined by

$$\operatorname{erf}(x)=\frac{2}{\sqrt{\pi}}\int_0^x e^{-y^2}dy. \quad (2.10)$$

At the end of phase 1 ($t_0 = V_{HT}/U$), when the threshold condition is reached ($V_G = V_S + V_T$), the error voltage can be written as

$$v_d(t_0) = -\sqrt{\frac{\pi U C_L}{2\beta}}\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_L}\right)\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}V_{HT}\right]. \quad (2.11)$$

In phase 2 ($V_L \leqslant V_G \leqslant V_S + V_T$), if subthreshold effects are ignored, only the gate overlap capacitor (C_{ol}) continues to contribute to the error voltage (see Fig. 2.4(b)). Therefore, the differential equation describing this phase is given by

$$C_L\frac{dv_d}{dt} = -C_{ol}U. \quad (2.12)$$

This equation is valid for the time period when $t_0 < t < t_f$ where $t_0 = \frac{V_{HT}}{U}$ and $t_f = \frac{V_H - V_L}{U}$. Using (2.11) and (2.12), it can be easily shown that when the gate voltage reaches its final value V_L, the total amount of switch charge injection error voltage on the load capacitance C_L becomes

$$v_{df} = -\sqrt{\frac{\pi U C_L}{2\beta}}\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_L}\right)\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}V_{HT}\right]-\frac{C_{ol}}{C_L}(V_S+V_T-V_L). \quad (2.13)$$

The second term in (2.13) is due to the charge injection in phase 2.

Equation (2.13) can be simplified under two extreme cases of fast and

slow gate voltage falling rate by using the well known approximation for the "erf" function as follows [20]

$$\text{erf}(x) \approx \begin{cases} 1 & if \quad x \gg 1 \\ \frac{2x}{\sqrt{\pi}}\left(1 - \frac{x^3}{3}\right) & if \quad x \ll 1. \end{cases} \tag{2.14}$$

At slow gate voltage falling rates when $\frac{\beta V_{HT}^2}{2C_L} \gg U$,

$$v_{df} = -\sqrt{\frac{\pi U C_L}{2\beta}}\left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_L}\right) - \frac{C_{ol}}{C_L}(V_S + V_T - V_L) \tag{2.15}$$

and at fast falling rates when $\frac{\beta V_{HT}^2}{2C_L} \ll U$,

$$v_{df} = -\left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_L}\right)\left(V_{HT} - \frac{\beta V_{HT}^3}{6UC_L}\right) - \frac{C_{ol}}{C_L}(V_S + V_T - V_L). \tag{2.16}$$

2.2.2 Dependence on Process and Electrical Parameters

Equation (2.13) verifies that the switch charge injection error depends on various process and electrical parameters such as the gate voltage falling rate, input voltage level, substrate doping, oxide thickness and switch transistor size. The simulation results of Sheu and Hu's model showing the effects of these parameters are presented in this section. The model parameters of a commercial CMOS $1.5\mu m$ process were chosen as the simulation parameters unless otherwise specified. In this process $N_A = 1.405 \times 10^{16} cm^{-3}$, $T_{ox} = 26.17nm$, $V_{T0} = 0.8486V$, $\mu = 526.7 cm^2/V.s$ and the gate overlap capacitance is 2.771×10^{-12} farads per transistor width (cm).

Dependence on Gate Voltage Falling Rate

At low gate voltage falling rates, most of the channel charges return to the

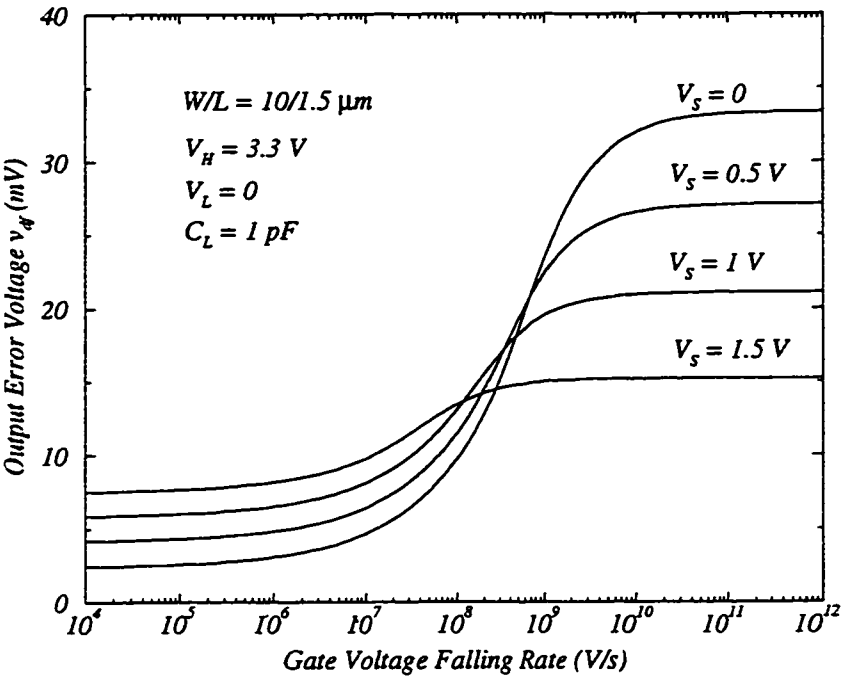

Figure 2.5: The output error voltage variation with respect to the gate voltage falling rate for different input signal voltage levels.

input source and the channel current compensates the charge injected from the overlap capacitance during the time the transistor is ON. Therefore, the final charge injection is primarily due to the clock feedthrough of the overlap capacitance (C_{ol}) after the switch is turned off. This error saturates at $(V_S + V_T - V_L)\, C_{ol}/C_L$ for very low falling rates.

At high falling rates, almost half of the channel charge is deposited on the load capacitance C_L. Therefore, the output error voltage can be written as

$$v_{df} \approx -V_{HT} \left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_L} \right) - \frac{C_{ol}}{C_L} (V_S + V_T - V_L)\,. \tag{2.17}$$

Figure 2.5 shows the variation of the absolute value of the output error voltage as a function of the gate voltage falling rate for different input

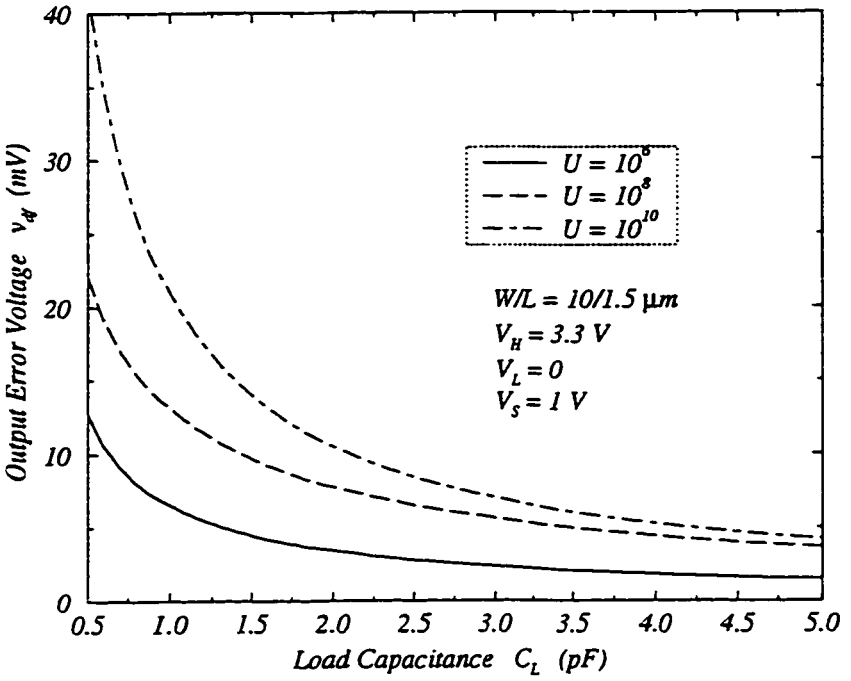

Figure 2.6: The output error voltage as a function of the load capacitance with gate voltage falling rate as a parameter.

voltages.

Dependence on Load Capacitance

Figure 2.6 shows the output error voltage variation with respect to the load capacitance for different gate voltage falling rates. As can be seen, the error voltage increases significantly at lower load capacitances. This confirms that the charge injection error of analog switches is an important issue in modern integrated switching circuits where small capacitor sizes are used.

Dependence on Input Voltage Level

Figures 2.7 and 2.8 illustrate the variation of the output voltage with

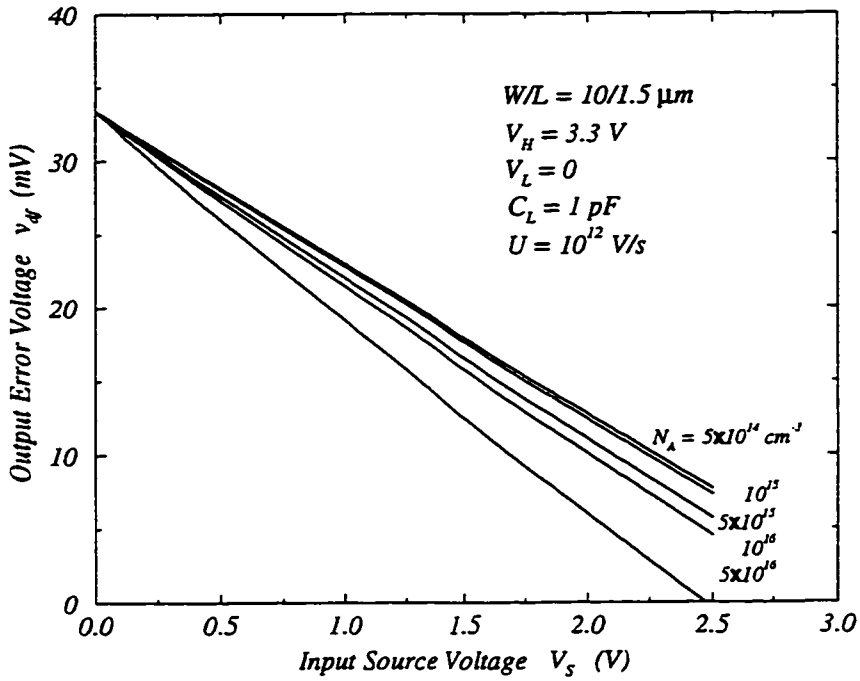

Figure 2.7: The variation of the output error voltage with respect to the input voltage level for different substrate doping levels at high gate voltage falling rates.

respect to the input voltage level for various substrate dopings. As can be seen from 2.7, the final error is a strong function of the input voltage particularly at higher substrate doping levels when the gate voltage falling rate is high. However, Fig. 2.8 shows that this variation is quite nonlinear at moderate gate voltage falling rates where the output error voltage varies significantly with the gate voltage falling rate (see Fig. 2.5). As the substrate doping increases, the variation of the threshold voltage due to body effect also increases which in turn makes the final error more sensitive to V_S.

In addition, equation (2.13) confirms that the switch charge injection error consists of two components, one signal dependent and the other signal independent. The signal independent component can be treated as an offset

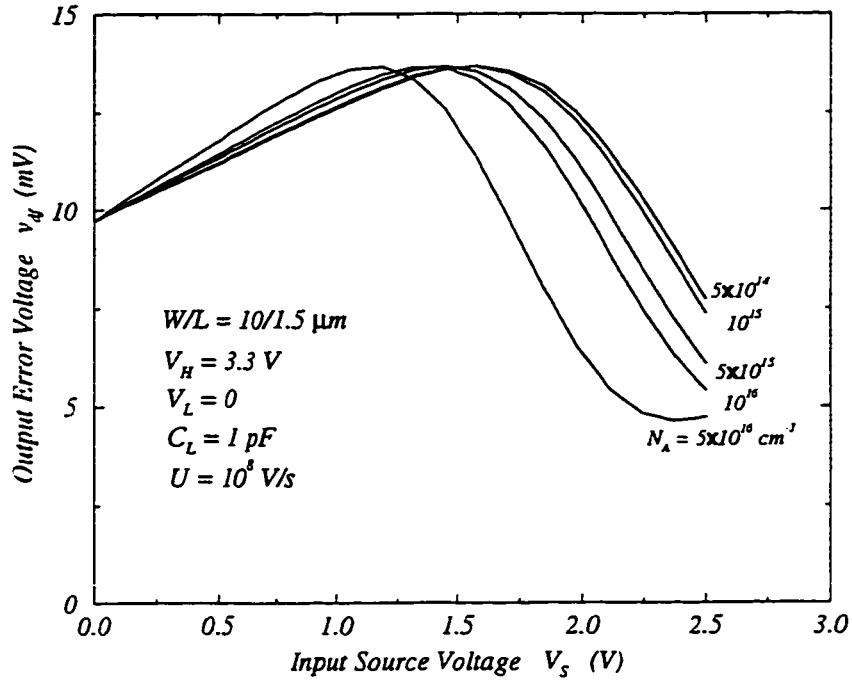

Figure 2.8: The variation of the output error voltage with respect to the input voltage level for different substrate doping levels at moderate gate voltage falling rates.

and it is not important in many applications. However, the signal dependent component causes distortion in applications such as sample and hold and A/D converters.

Dependence on Oxide Thickness

In modern MOS processes as the process feature size decreases, the oxide thickness is also reduced. As a result, the relationships between some of the parameters and capacitances in charge injection error analysis remain constant. For instance, if the oxide thickness of the load capacitor and the oxide thickness of the gate are reduced by the same factor, $(C_{ol} + C_{ox}/2)/C_L$ and $\frac{\beta}{C_L}$ remain constant. Therefore, v_{df} calculated from (2.13) does not

change as oxide thickness changes. Otherwise, the variation of oxide thickness changes the final charge injection error.

Dependence on Channel Width and Length

Figure 2.9 shows the final error voltage variation with respect to the channel length for different channel widths. This figure confirms that the larger the switch transistor is, the higher the output error voltage will be for a fixed load capacitance. This may conflict with the requirement of low on-resistance which requires a large W/L ratio in the switch transistor. Therefore, in applications where charge injection is a concern, optimizing the size of the switches by considering other factors such as the switch on-resistance can improve the circuit performance.

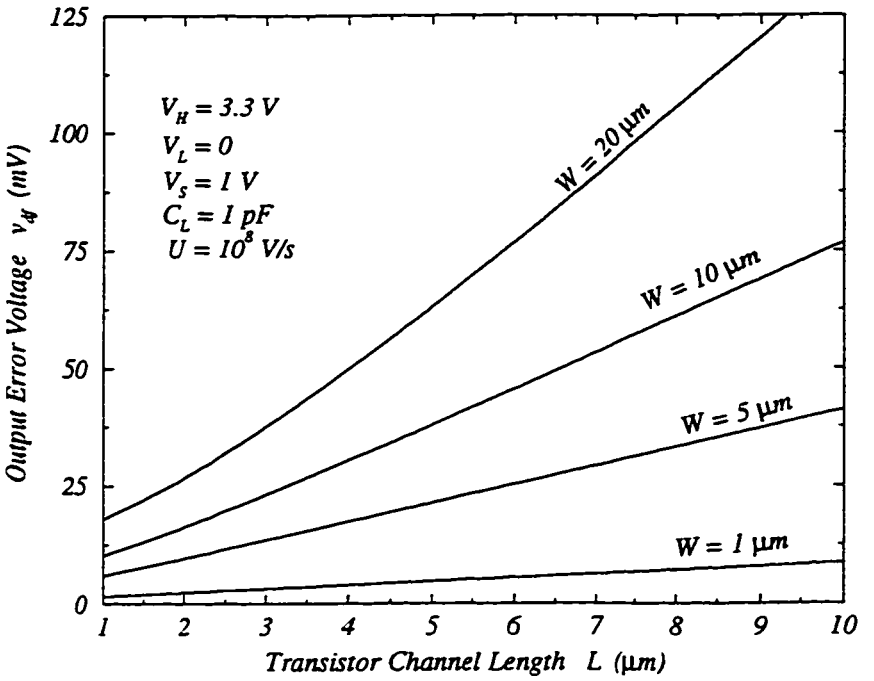

Figure 2.9: The final error voltage variation with respect to the transistor channel length for different channel widths.

2.3 Shortcomings of Sheu and Hu's Model

Sheu and Hu's model discussed in previous sections takes into account first order effects in switch charge injection. These effects are the channel charge injection when the transistor is in the strong inversion region, the charge on the overlap capacitances and the channel current in strong inversion. The model is simple and provides excellent insight into the switching problem. However, it does not take into account second order effects whose importance was discussed in Chapter 1. One of the most important second order effects is the channel subthreshold current. In Sheu and Hu's model no channel current is assumed below threshold. However, it is well known that this current fades exponentially in the subthreshold region. Their model also ignores the

injection of channel charge in the weak inversion region by assuming zero gate-source/gate-drain capacitance in this region. However, in a practical device, the inversion layer does not disappear spontaneously at the threshold voltage. Another important effect which has been ignored in Sheu and Hu's model is the variation of the gate-source capacitance in strong inversion. This capacitance is modelled by a constant value of $\frac{C_{ox}}{2}$ above threshold, but accurate MOSFET models [12] predict a variable behavior for this capacitance particularly around the threshold voltage. In addition, a very simple and inaccurate model has been used for the MOSFET drain current calculation in Sheu and Hu's model. As discussed in Chapter 1, error in the drain current calculation can cause significant error in the final charge injection error prediction. Therefore, Sheu and Hu's model is not appropriate for precise prediction of switch charge injection where second order effects are also important.

2.4 Analysis in the Presence of Source Resistance

Sheu and Hu's model can be used to analyze the charge injection problem of Fig. 2.2(b) where the input resistance is taken into account. KCL at nodes A and B in Fig. 2.2(b) requires

$$C_L\frac{dv_d}{dt} = -i_d + \left(C_{ol} + \frac{C_{ox}}{2}\right)\frac{d\left(V_G - v_d\right)}{dt} \tag{2.18}$$

$$\frac{v_s}{R_S} = i_d + \left(C_{ol} + \frac{C_{ox}}{2}\right)\frac{d\left(V_G - v_s\right)}{dt}. \tag{2.19}$$

Assuming $|dV_G/dt| \gg |dv_d/dt|$, (2.18) and (2.19) can be simplified to

$$C_L\frac{dv_d}{dt} = -\beta\left(V_{HT} - Ut\right)\left(v_d - v_s\right) - \left(C_{ol} + \frac{C_{ox}}{2}\right)U \tag{2.20}$$

$$\frac{v_s}{R_S} = \beta\left(V_{HT} - Ut\right)\left(v_d - v_s\right) - \left(C_{ol} + \frac{C_{ox}}{2}\right)U. \qquad (2.21)$$

It should be noted that v_d and v_s are the voltage variation from V_S at node B and node A, respectively.

A first order differential equation can be derived by eliminating v_s from (2.20) using (2.21) as follows

$$\begin{aligned} C_L\frac{dv_d}{dt} &= -\frac{\beta\left(V_{HT} - Ut\right)}{1 + \beta R_S\left(V_{HT} - Ut\right)}v_d \\ &\quad - \left(C_{ol} + \frac{C_{ox}}{2}\right).\left[2 - \frac{1}{1 + \beta R_S\left(V_{HT} - Ut\right)}\right]U. \end{aligned} \qquad (2.22)$$

The output error voltage can be calculated by solving this differential equation and adding the clock feedthrough due to the gate-drain overlap capacitance when the switch transistor is OFF. The final answer is given by

$$\begin{aligned} v_{df} &= -\frac{C_{ol}}{C_L}\left(V_S + V_T - V_L\right) - U\left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_L}\right).\exp\left[-\frac{V_{HT}}{UC_LR_S}\right] \\ &\quad .\int_0^{V_{HT}/U}\left[1 + \beta R_S\left(V_{HT} - Ut\right)\right]^{1/C_L\beta U R_S^2} \\ &\quad .\exp\left(\frac{t}{C_LR_S}\right)\left(2 - \frac{1}{1 + \beta R_S\left(V_{HT} - Ut\right)}\right)dt. \end{aligned} \qquad (2.23)$$

Since the integral function in (2.23) requires numerical evaluation, a closed-form expression for the final error voltage cannot be obtained.

Figure 2.10 shows the variation of the output error voltage as a function of the input source resistance R_S for different load capacitances.

This figure also confirms that most of the channel charge returns to the input source at low source resistances (R_S) which reduces the output error voltage.

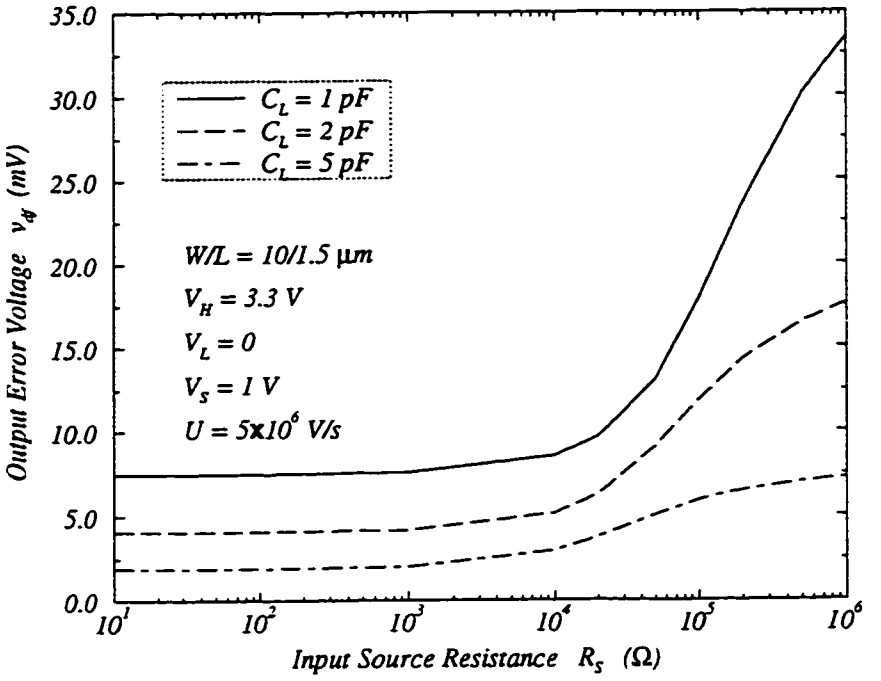

Figure 2.10: The output error voltage variation as a function of the input source resistance for different load capacitances.

2.5 Analysis in the Presence of Source Capacitance

In the case where R_S is large so that the time constant $R_S C_S$ is much larger than the switch turn-off time (Fig. 2.2(c)), KCL at node A and node B requires

$$C_L \frac{dv_d}{dt} = -i_d + \left(C_{ol} + \frac{C_{ox}}{2}\right) \frac{d(V_G - v_d)}{dt} \tag{2.24}$$

$$C_S \frac{dv_s}{dt} = i_d + \left(C_{ol} + \frac{C_{ox}}{2}\right) \frac{d(V_G - v_s)}{dt}. \tag{2.25}$$

Under the practical conditions where $|dV_G/dt| \gg |dv_d/dt|$ and $|dv_s/dt|$, equations (2.24) and (2.25) can be written as

$$C_L\frac{dv_d}{dt} = -\beta\left(V_{HT}-Ut\right)\left(v_d-v_s\right)-\left(C_{ol}+\frac{C_{ox}}{2}\right)U \qquad (2.26)$$

$$C_S\frac{dv_s}{dt} = \beta\left(V_{HT}-Ut\right)\left(v_d-v_s\right)-\left(C_{ol}+\frac{C_{ox}}{2}\right)U. \qquad (2.27)$$

Combining (2.26) and (2.27), the following differential equation for $(v_d - v_s)$ can be obtained

$$C_L\frac{d\left(v_d-v_s\right)}{dt} = -\beta\left(V_{HT}-Ut\right)\left(1+\frac{C_L}{C_S}\right)\left(v_d-v_s\right) - \left(C_{ol}+\frac{C_{ox}}{2}\right)\left(1-\frac{C_L}{C_S}\right)U. \qquad (2.28)$$

The solution to this equation when the gate voltage reaches the threshold condition ($t = V_{HT}/U$), is given by

$$v_d-v_s = -\sqrt{\frac{\pi U C_L}{2\beta\left(1+C_L/C_S\right)}}\cdot\left[\left(C_{ol}+\frac{C_{ox}}{2}\right).\frac{1-C_L/C_S}{2C_L}\right] .\operatorname{erf}\left(\sqrt{\frac{\beta\left(1+C_L/C_S\right)}{2UC_L}}V_{HT}\right). \qquad (2.29)$$

If the subthreshold region is ignored, the transistor channel between the drain and source disappears below threshold so that the charges at nodes A and B cannot communicate. Therefore, the charges injected to the drain and source sides due to the overlap capacitances are equal below the threshold condition. These charges correspond to $(V_S + V_T - V_L)\frac{C_{ol}}{C_L}$ and $(V_S + V_T - V_L)\frac{C_{ol}}{C_S}$ error voltages at the output and input nodes, respectively.

At low gate voltage falling rates, the right side of equation (2.29) approaches zero and as a result $v_d = v_s$. This indicates that at slow falling rates, the communication between the charge at the input source side and

the charge at the output is so strong when the transistor is in strong inversion that it makes the final error voltage at both sides equal. This shows that the majority of the channel charges move to the node with larger capacitance. At fast falling rates, however, there is not enough time for the charges at the source and drain to communicate. Therefore, almost half of the channel charge is deposited to each side.

Figure 2.11 shows the percentage of the channel charge injected into the output node for various C_L/C_S ratios. The dimensionless quantity $(V_H - V_T)\sqrt{\frac{\beta}{UC_L}}$ has been used as the variable in this simulation. As can be seen, at high gate voltage falling rates, this percentage approaches 50 whereas at low falling rates, it depends on the C_L/C_S ratio.

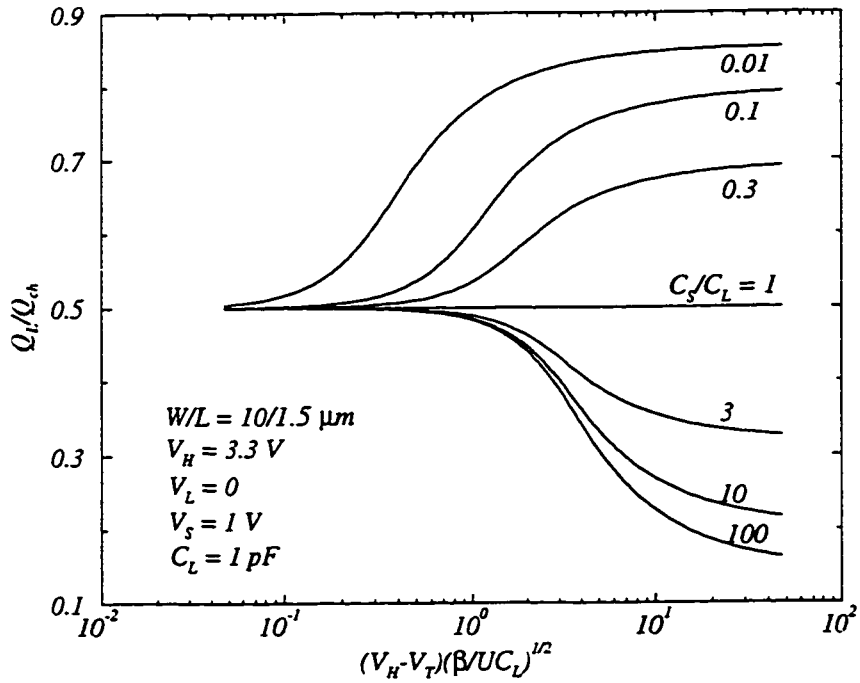

Figure 2.11: The percentage of the channel charge injected to the output node for various C_L/C_S ratios.

2.6 Analysis in the General Case

Referring to Fig. 2.1, KCL at node A and node B requires

$$C_L\frac{dv_d}{dt} = -i_d + \left(C_{ol} + \frac{C_{ox}}{2}\right)\frac{d(V_G - v_d)}{dt} \tag{2.30}$$

$$\frac{v_s}{R_S} + C_S\frac{dv_s}{dt} = i_d + \left(C_{ol} + \frac{C_{ox}}{2}\right)\frac{d(V_G - v_s)}{dt}, \tag{2.31}$$

where

$$i_d = \beta\,(V_{HT} - Ut)\,(v_d - v_s)\,. \tag{2.32}$$

Under the conditions $|dV_G/dt| \gg |dv_d/dt|$ and $|dv_s/dt|$, equations (2.30) and (2.31) can be simplified to

$$C_L\frac{dv_d}{dt} = -\beta\,(V_{HT} - Ut)\,(v_d - v_s) - \left(C_{ol} + \frac{C_{ox}}{2}\right)U \tag{2.33}$$

$$\frac{v_s}{R_S} + C_S\frac{dv_s}{dt} = \beta\,(V_{HT} - Ut)\,(v_d - v_s) - \left(C_{ol} + \frac{C_{ox}}{2}\right)U. \tag{2.34}$$

Equations (2.33) and (2.34) can only be solved numerically. Figures 2.12 and 2.13 show the percentage of the channel charge injected to the load capacitance (Q_L/Q_{ch}), for various C_L/C_S ratios. Since the relative magnitude of the falling rate compared with the signal time constant R_SC_S is an important factor in switch charge injection, two cases where $V_{HT}/UR_SC_S = 1$ and 5 have been plotted in Fig. 2.12 and Fig. 2.13, respectively. Therefore, the source resistance at each point in Fig. 2.13 is five times smaller than the one at the similar point in Fig. 2.12. It can be seen from these figures that a small source resistance can reduce the output error voltage significantly. This case will be discussed further in Chapter 5.

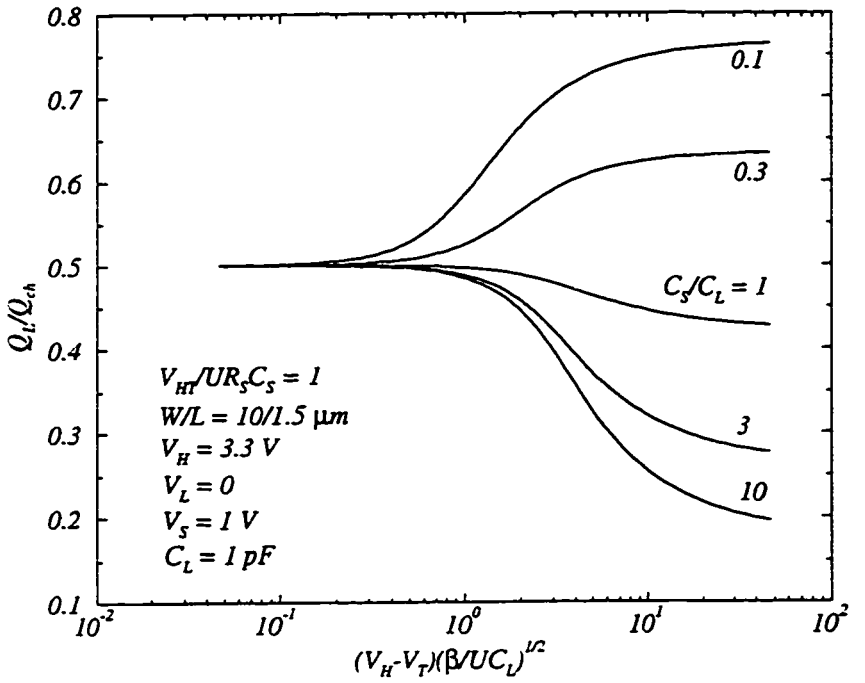

Figure 2.12: The percentage of the channel charge injected to the load capacitance for various C_L/C_L ratios where $V_{HT}/UR_SC_S = 1$.

2.7 Summary

Different cases of switch charge injection were introduced and discussed in this chapter. Sheu and Hu's model for the charge injection error analysis and its shortcomings were also explained in detail. Based on this model. a different equation was derived in each special case of switch charge injection as well as the general case. Also, the dependences on various electrical and process parameters were illustrated to obtain a good understanding of the switch charge injection problem for developing the modified model in the following chapters.

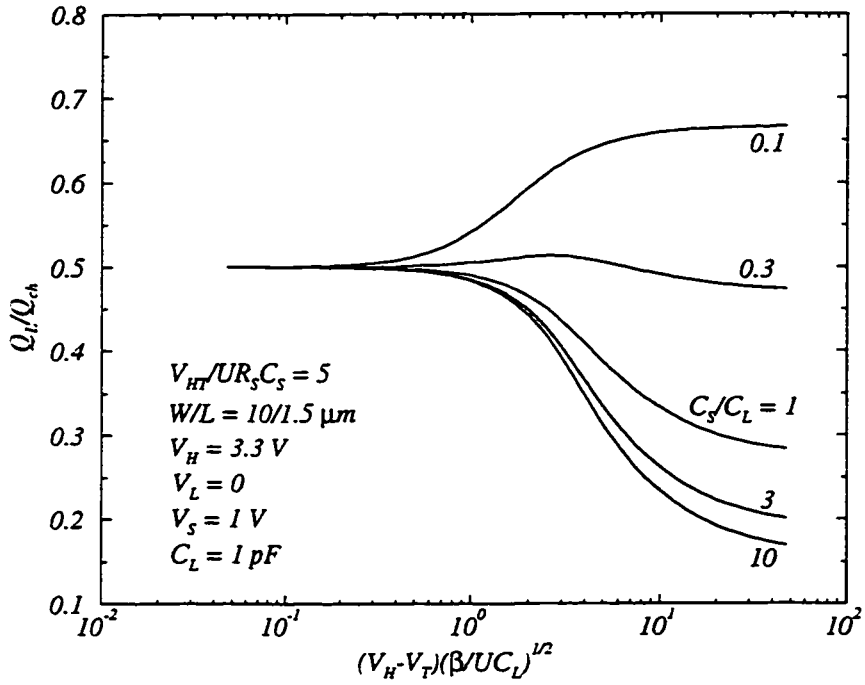

Figure 2.13: The percentage of the channel charge injected to the load capacitance for various C_L/C_L ratios where $V_{HT}/UR_SC_S = 5$.

Chapter 3

Subthreshold Analysis of an MOS Analog Switch

Second order effects such as the subthreshold current and weak inversion channel charges have not been considered in the simple Sheu and Hu's model for the charge injection error analysis described in Section 2.2.

In this chapter, the subthreshold current and weak inversion channel charges are added to this model in order to study subthreshold effects. An approximation is used to find an analytical solution for the final charge injection error. The modified model is simple, computationally efficient and provides physical insight into the switching errors in the weak inversion region.

3.1 Introduction

Sheu and Hu's analysis [7] described in Section 2.2 shows that a smaller gate voltage falling rate and transistor size produce a lower output error voltage if the load capacitance is fixed. However, lower on-resistance requires a larger transistor size. In high accuracy applications where low on-resistance is essential, a slow gate voltage falling rate can decrease the error. It will be

shown that second order effects which are not considered in Sheu and Hu's analysis play a significant role at low gate voltage falling rates.

The modified model to be described in this section takes into account the subthreshold current and inversion layer charge variation effect in the weak inversion region. The variation of the gate-source capacitance above the threshold voltage is also taken into account. An exponential equation is used to model the subthreshold current. A new model using two exponential equations is developed to include the gate-source capacitance variations.

The modified model is explained in Section 3.2. The analytical model for the final error is derived in Section 3.3. The dependence on process and electrical parameters is considered in Section 3.4. Section 3.5 is devoted to a brief explanation of a charge conserving non-quasi-static (NQS) model [12] which will be referred to as the NQS-model throughout this chapter. This accurate but complicated model is used to verify the validity of the proposed model. The simulation results comparing the modified model with the NQS and SPICE models are presented in Section 3.6. The effect of source capacitance is discussed in Section 3.7. A summary is given in Section 3.8.

3.2 Modified Sheu and Hu's Model

As described in Section 2.2, the fundamental equations for the output error voltage calculation in the simple Sheu and Hu's model are given by (3.1) and (3.3). In phase 1, when the transistor gate-source voltage is above the threshold voltage

$$C_L \frac{dv_d}{dt} = -i_d - \left(C_{ol} + \frac{C_{ox}}{2} \right) U \tag{3.1}$$

where

$$i_d = \beta (V_{HT} - Ut) v_d. \tag{3.2}$$

and in phase 2, when the transistor gate-source voltage is below the threshold voltage

$$C_L \frac{dv_d}{dt} = -C_{ol}U. \tag{3.3}$$

In the modified model, the gate-source capacitance variation is added to the analysis in phase 1 by substituting $\frac{C_{ox}}{2}$ with C_{gs} in (3.1). C_{gs} is an exponential function of the gate-source voltage. In Phase 2, however, both the subthreshold current and variation of the gate-source capacitance need to be added to (3.3). To accurately include these effects into the model, appropriate models are required for the subthreshold current and the gate-source capacitance variation.

3.2.1 The Subthreshold Current Model

The diffusion current in a MOS transistor is significant compared to the total drain current when the gate-source voltage is below the threshold voltage. When $V_{GS} \ll V_T$, the drain current can be modelled accurately with an exponential function. We assume that the I-V characteristics of a MOS transistor in the subthreshold region can be described by [21]

$$I_{SUB} = I_0 \exp\left(\frac{V_{GS} - V_{on}}{nV_t}\right) \tag{3.4}$$

where V_{on} is the modified threshold voltage, given by

$$V_{on} = V_T + nV_t, \tag{3.5}$$

and n is the subthreshold slope factor,

$$n = 1 + \frac{qN_{FS}}{C'_{ox}} + \frac{\gamma}{2\sqrt{\phi_B + V_{SB}}}, \tag{3.6}$$

where C'_{ox} is the oxide capacitance per unit gate area and V_t is the thermal voltage, kT/q. N_{FS} is the fast surface state density, V_{SB} is the source to substrate voltage and

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_a}}{C'_{ox}}. \tag{3.7}$$

I_0 is the current in the strong inversion region for $V_{GS} = V_{on}$ [21], given by

$$I_0 = \beta(V_{on} - V_T)V_{ds} = n\beta V_t V_{ds}. \tag{3.8}$$

Equation (3.8) is derived from the simple transistor drain current equation in the triode region by ignoring the V_{DS}^2 term. I_0 depends on process parameters and transistor size.

3.2.2 The Gate-Source Capacitance Variation Model

In Sheu and Hu's simple model, the gate-source capacitance is considered to be $\frac{C_{ox}}{2}$ above threshold and zero below threshold, respectively. The variation of C_{gs} around threshold is therefore ignored and inversion layer charge is assumed to be negligible. In the modified model, two exponential functions are used to model the C_{gs} variation above and below the threshold voltage as follows (see Appendix A),

$$C_{gs} = \begin{cases} C_{gsm} \exp\left(\frac{V_{GS}-V_{on}}{nV_t}\right) & V_{GS} < V_{on} \\ \frac{C_{ox}}{2} - \left(\frac{C_{ox}}{2} - C_{gsm}\right) . \exp\left(-\frac{V_{GS}-V_{on}}{kV_t}\right) & V_{GS} \geq V_{on}\ , \end{cases} \tag{3.9}$$

where C_{gsm} is the gate-source capacitance when $V_{GS} = V_{on}$.

Fig. 3.1 shows that (3.9) is a better approximation to the C_{gs} variation than what has been used in Sheu and Hu's model.

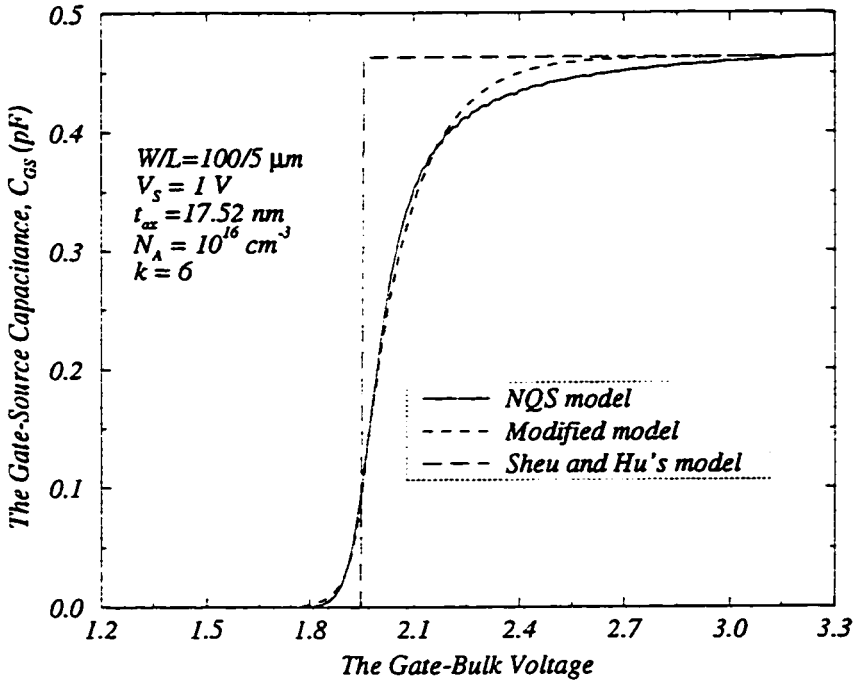

Figure 3.1: The gate-source capacitance approximation.

3.2.3 The Analytical Models above and below Threshold

As in the analysis in Section 2.2, two phases of operation are considered during the turnoff transient. The new C_{gs} variation model (Equation (3.9)) is used in both phases. In phase two, the subthreshold current effect is also added to this analysis.

Substituting C_{gs} from (3.9) for $\frac{C_{ox}}{2}$ in equation (3.1) will lead to the following differential equation in phase 1 ($V_{GS} \geq V_{on}$)

$$C_L \frac{dv_d}{dt} = -i_d - (C_{ol} + C_{gs})\, U \tag{3.10}$$

where

$$C_{gs} = \frac{C_{ox}}{2} - \left(\frac{C_{ox}}{2} - C_{gsm}\right).\exp\left(-\frac{V_{GS} - V_{on}}{kV_t}\right). \tag{3.11}$$

It can be easily shown that the analytical solution to this equation after some simplifications is given by

$$\begin{aligned} v_d(t) \;=\; & -\sqrt{\frac{\pi UC_L}{2\beta}}\left(\frac{\frac{C_{ox}}{2}+C_{ol}}{C_L}\right)\exp\left[\frac{\beta U}{2C_L}\left(t-\frac{V_{HT}}{U}\right)^2\right] \\ & .\left\{\mathrm{erf}\left[\sqrt{\frac{\beta}{2UC_L}}V_{HT}\right]-\mathrm{erf}\left[\sqrt{\frac{\beta}{2UC_L}}(V_{HT}-Ut)\right]\right\} \\ & +\sqrt{\frac{\pi UC_L}{2\beta}}\left(\frac{\frac{C_{ox}}{2}-C_{gsm}}{C_L}\right)\exp\left[\frac{\beta U}{2C_L}\left(t-\frac{V_{HT}}{U}\right)^2\right] \\ & .\left\{\mathrm{erf}\left[\sqrt{\frac{\beta}{2UC_L}}\left(\frac{UC_L}{kV_t\beta}+V_{HT}\right)\right]\right. \\ & \left.-\mathrm{erf}\left[\sqrt{\frac{\beta}{2UC_L}}\left(\frac{UC_L}{kV_t\beta}+V_{HT}-Ut\right)\right]\right\}. \end{aligned} \tag{3.12}$$

Comparing (3.12) with (2.9) shows that including the C_{gs} variations in the modified model adds an extra term (the second term in (3.12)) to the final error voltage at the end of phase 1. This term is less significant at smaller $\frac{UC_L}{kV_t\beta}$.

In the second phase ($V_{GS} \leq V_{on}$), the circuit to be analyzed is shown in Fig. 3.2.

Using (3.4), (3.8) and (3.9), the differential equation describing the circuit can be derived as

$$\frac{dv_d}{dt} = -\left(\frac{C_{ol}}{C_L}+\frac{C_{gsm}}{C_L}\exp\left(\frac{V_{GS}-V_{on}}{nV_t}\right)\right)U - \frac{\beta nV_t}{C_L}\exp\left(\frac{V_{GS}-V_{on}}{nV_t}\right)v_d. \tag{3.13}$$

The gate-source voltage is given by

$$V_{GS} = V_H - V_S - Ut. \tag{3.14}$$

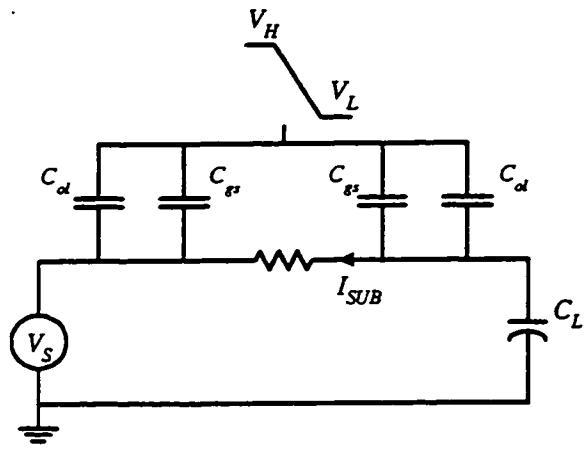

Figure 3.2: Circuit model in the subthreshold region.

Substituting (3.14) into (3.13), the error voltage can be found from the solution of the differential equation

$$\frac{dv_d}{dt} = -\frac{C_{ol}}{C_L}U - \left(\frac{C_{gsm}}{C_L}U + \frac{\beta n V_t}{C_L}v_d\right).\exp\left(\frac{V_{HT} - nV_t}{nV_t}\right)\exp\left(-\frac{Ut}{nV_t}\right) \tag{3.15}$$

where

$$V_{HT} = V_H - V_S - V_T. \tag{3.16}$$

Equation (3.15) has an exact solution of the form

$$\begin{aligned} v_d(t) &= \frac{nV_t C_{ol}}{C_L}e^Z\left[\mathrm{Ei}(Z_0) - \mathrm{Ei}(Z)\right] \\ &\quad -\frac{C_{gsm}U}{\beta n V_t}\left[1 - e^{Z-Z_0}\right] + e^{Z-Z_0}v_d(t_0) \end{aligned} \tag{3.17}$$

where

$$Z = \frac{\beta(nV_t)^2}{UC_L}\exp\left(-\frac{U}{nV_t}(t - t_0)\right), \tag{3.18}$$

$$Z_0 = \frac{\beta(nV_t)^2}{UC_L}, \tag{3.19}$$

and $v_d(t_0)$ is found from equation (3.12). Equation (3.17) is valid in the

subthreshold region ($t \geq t_0$) until the gate voltage reaches V_L ($t = t_f$), where

$$t_0 = \frac{V_{HT} - nV_t}{U}, \tag{3.20}$$

and

$$t_f = \frac{V_H - V_L}{U}. \tag{3.21}$$

Ei is the exponential integral function defined by [20]

$$\mathrm{Ei}(Z) = \int_Z^\infty \frac{e^{-y}}{y} dy, \tag{3.22}$$

where y is a dummy variable.

Evaluating the exponential integral at the point associated with time t ($t \geq t_0$) gives the output error voltage caused by the transistor in this region of operation. The final output error voltage can be calculated by substituting t_f into (3.17) and (3.18).

3.3 Approximate Analytical Model

An exact solution using the exponential integral requires numerical calculations. To obtain a simple analytical equation for the final output error voltage, an approximation is developed for [Ei(Z)-Ei(Z_0)].

From (3.22), it can be seen that

$$[\mathrm{Ei}(Z_0) - \mathrm{Ei}(Z)] = \int_{Z_0}^{Z} \frac{e^{-y}}{y} dy. \tag{3.23}$$

It turns out that approximating $\frac{e^{-y}}{y}$ with e^{-y} and $\frac{1}{y}$ for y greater than and less than unity, respectively, gives an excellent approximation to the exact solution of (3.23) for $Z \ll 1$. Making these approximations results in the

following limits

$$\begin{aligned} [\mathrm{Ei}(Z_0) - \mathrm{Ei}(Z)] &\approx \ln(Z) + (\mathrm{e}^{-Z_0} - \mathrm{e}^{-1}) \quad Z_0 \gg 1 \\ [\mathrm{Ei}(Z_0) - \mathrm{Ei}(Z)] &\approx \ln\left(\tfrac{Z}{Z_0}\right) \qquad\qquad\quad Z_0 \ll 1 \end{aligned} \tag{3.24}$$

which are valid provided $Z \ll 1$.

A smooth transition between the two solutions given in equation (3.24) can be made by using the following form to express the integral of (3.23)

$$[\mathrm{Ei}(Z_0) - \mathrm{Ei}(Z)] \approx \ln\left[\left(1 + \frac{1}{Z_0}\right) Z\right] + \mathrm{e}^{-\mathrm{e}^{-Z_0}} - \mathrm{e}^{-1}. \tag{3.25}$$

For our region of operation, Z_0 can be greater or less than unity, depending on the value of U. However, the value of Z at t_f (Z_f) is always much less than Z_0 and unity since

$$\frac{Z_f}{Z_0} = \exp\left(-\frac{V_S + V_T + nV_t - V_L}{nV_t}\right). \tag{3.26}$$

Fig. 3.3 shows the numerical evaluation of the exponential integral function along with (3.25) for the required values of Z_0 and Z_f when Z_f is obtained using (3.26). It is seen that (3.25) is a very close approximation to the exponential integral function over the range of Z_0 usually encountered in practice.

Substituting (3.25) into (3.17) and evaluating the time it takes for the gate voltage to reach V_L ($t = t_f$), the final output error voltage is determined to be

$$\begin{aligned} v_{df} &= \frac{nV_tC_{ol}}{C_L}\left\{\ln\left[\left(1 + \frac{1}{Z_0}\right) Z_f\right] + \mathrm{e}^{-\mathrm{e}^{-Z_0}} - \mathrm{e}^{-1}\right\} \\ &\quad -\frac{C_{gsm}U}{\beta nV_t}\left[1 - \mathrm{e}^{-Z_0}\right] + \mathrm{e}^{-Z_0}v_d(t_0). \end{aligned} \tag{3.27}$$

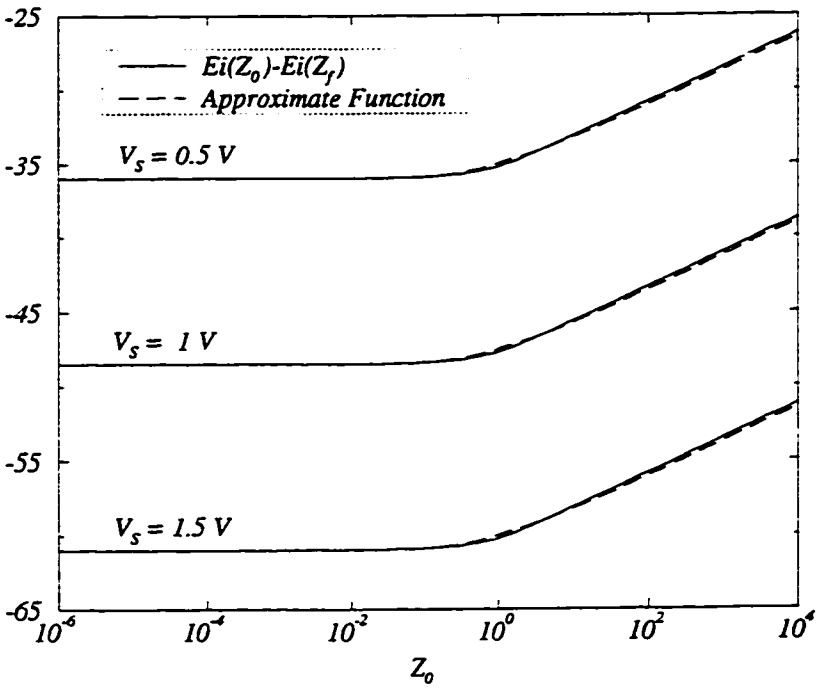

Figure 3.3: [Ei(Z_0)-Ei(Z_f)] and its approximate function.

Substituting all the parameters, equation (3.27) can be written as

$$\begin{aligned} v_{df} &= e^{-(nV_t)^2\beta/2UC_L} v_d(t_0) \\ &\quad -\frac{C_{ol}}{C_L}(V_S + V_T + nV_t - V_L) \\ &\quad +\frac{C_{ol}}{C_L} nV_t \left\{ \ln\left[1 + \frac{\beta(nV_t)^2}{UC_L}\right] \right. \\ &\quad \left. + \exp\left(-e^{-(nV_t)^2\beta/UC_L}\right) - e^{-1} \right\} \\ &\quad -\frac{C_{gsm}U}{\beta nV_t}\left(1 - e^{-(nV_t)^2\beta/UC_L}\right), \end{aligned} \tag{3.28}$$

where $v_d(t_0)$ can be calculated from (3.12).

The first and second terms in (3.28) correspond to the errors caused by the gate-oxide overlap capacitances and channel charges when the transistor is in

strong and weak inversion, respectively. The third term is the contribution of the subthreshold current to the cancellation of the error caused by the overlap capacitance in weak inversion. The last term is the error due to the inversion layer charge injection in the weak inversion region which decreases at the lower gate voltage falling rates. At high voltage falling rates, since the channel charge is divided equally between the source and drain, this term saturates at $\frac{C_{gsm}nV_t}{C_L}$. Equation (3.28) then provides a simple and quite accurate analytical model for switch induced error voltage. The model is useful in describing the functional dependence of the error voltage on circuit and process parameters.

Equation (3.28) can be further simplified at high and low gate voltage falling rates. At high falling rates ($V_{HT}^2\beta/2C_L \ll U$):

$$\begin{aligned} v_{df} \simeq & -V_{HT}\left(\frac{C_{ox}/2+C_{ol}}{C_L}\right)\left(1-\frac{\beta V_{HT}^2}{6UC_L}\right) \\ & +V_{HT}\left(\frac{C_{ox}/2-C_{gsm}}{C_L}\right)\left(1-\frac{\beta}{6UC_L}\right. \\ & \left.\cdot\left[3\left(\frac{UC_L}{kV_t\beta}\right)^2+3V_{HT}\left(\frac{UC_L}{kV_t\beta}\right)+V_{HT}^2\right]\right) \\ & -\frac{C_{ol}}{C_L}(V_S+V_T+nV_t-V_L) \\ & -\frac{C_{gsm}nV_t}{C_L}, \end{aligned} \tag{3.29}$$

and at low falling rates ($V_{HT}^2\beta/2C_L \gg U$):

$$\begin{aligned} v_{df} \simeq & -\frac{C_{ol}}{C_L}(V_S+V_T+nV_t-V_L) \\ & +\frac{C_{ol}}{C_L}nV_t\left\{\ln\left[\frac{\beta(nV_t)^2}{UC_L}\right]\right\}. \end{aligned} \tag{3.30}$$

A comparison of (3.30) with Sheu and Hu's results at low falling rates [7] shows that the first term of (3.28) corresponding to the error caused by the injected charge above the threshold voltage has disappeared. In addition, the

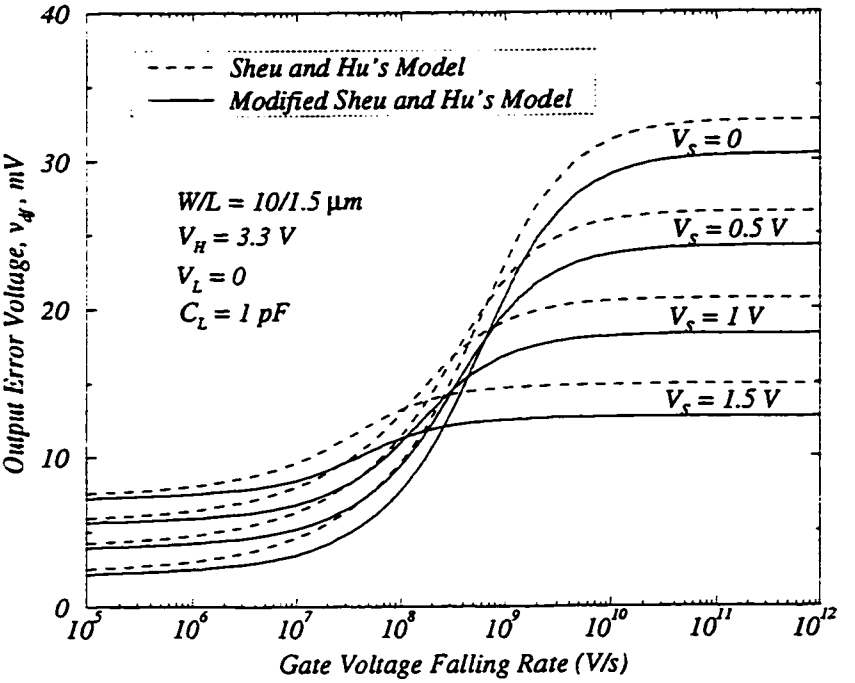

Figure 3.4: A comparison between the simple and modified Sheu and Hu's models.

second term of (3.30), which is also due to the subthreshold current, decreases the final error voltage. At high falling rates, the subthreshold current effect is negligible and the contribution of the channel charges in the subthreshold region to the final error saturates at $\frac{C_{gsm} n V_t}{C_L}$.

Figure 3.4 shows a comparison between the simple Sheu and Hu's model results with those of the modified Sheu and Hu's model (equation 3.28).

3.4 Dependence on Process and Electrical Parameters

In the weak inversion region, the effects of the subthreshold current and inversion layer charges on the charge-induced error depend on the circuit and process parameters. In (3.28), the third term, which represents the subthreshold current effect, is independent of the input voltage signal level. As a result, at higher input voltage signal levels, as the total charge-induced error decreases, the subthreshold effect becomes more important. The last term in (3.28) indicates that the effect of the inversion layer charge in the weak inversion region is more significant at moderate gate voltage falling rates. In general, the exponential terms in (3.28) show that the lower the gate voltage falling rate, the more significant are the effects of the weak-inversion characteristics of the transistor.

Fig. 3.5 shows the contribution of the last two terms of (3.28) to the final charge induced error as a function of gate voltage falling rate. As can be seen, at all substrate dopings, the subthreshold current effect and the weak inversion channel charge effect cancel each other partially. However, as the falling rate decreases, ignoring the subthreshold effects can cause a higher error in the output voltage than that calculated using Sheu and Hu's model. The subthreshold effects for various gate oxide thickness values are shown in Fig. 3.6.

The importance of the subthreshold effects with respect to the load capacitance is depicted in Fig. 3.7.

As can be seen in Figs. 3.5 and 3.6 , the subthreshold effect in an analog switch is important when larger transistor sizes, lower load capacitances, lower substrate dopings, smaller gate oxide thickness values and lower gate voltage falling rates are used.

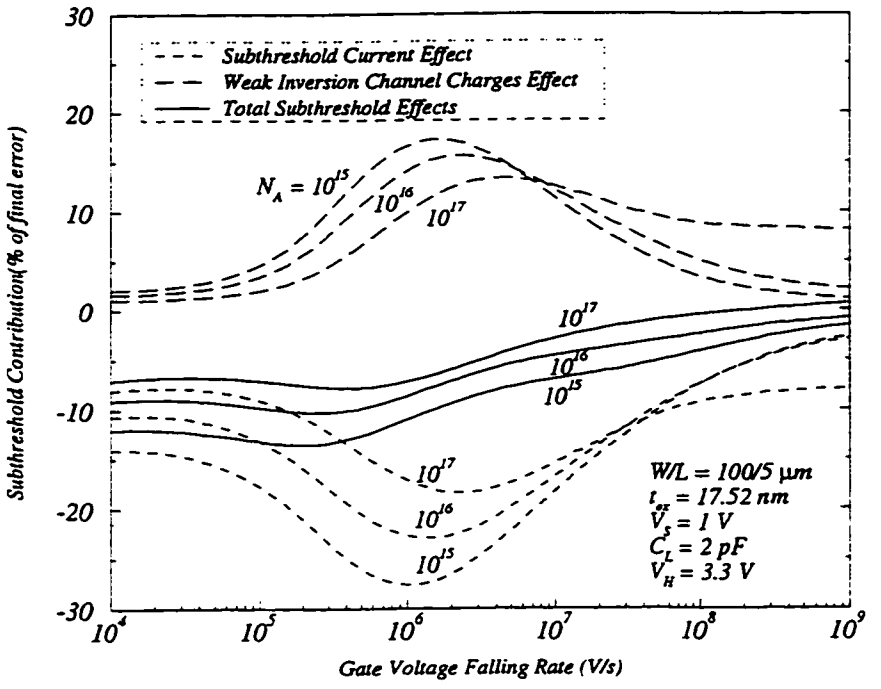

Figure 3.5: Normalized subthreshold effects with respect to the gate voltage falling rate for different substrate dopings.

3.5 A Non-Quasi-Static(NQS) Model

It has been shown in [11] and [12] that a non-quasi-static model can accurately predict the channel charge injection error. To check the approximate method proposed in the previous section, an NQS model based on [12] was used. All models were evaluated numerically using MATLAB. This model is not used in circuit simulators due to its complexity. The implementation of this method required a lot of effort and took a substantial amount of time.

In the NQS model, the transistor current continuity equation is solved approximately and analytical equations are derived for the node charges using the charge-sheet formulation. All the voltages and currents can be derived from these charges. This model includes the subthreshold current since the

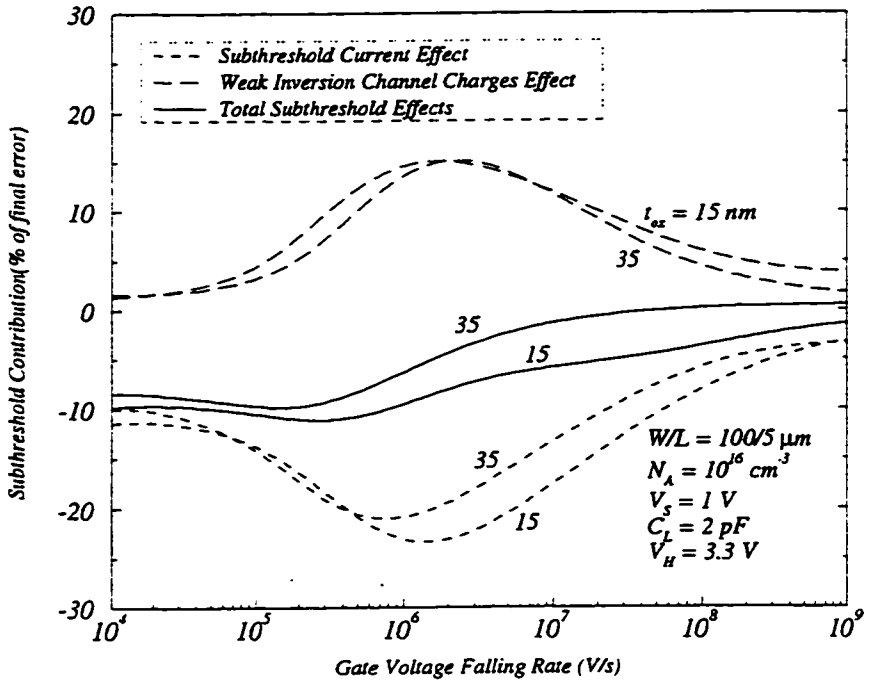

Figure 3.6: Normalized subthreshold effects with respect to the gate voltage falling rate for different gate oxide thickness values.

general partial differential equation for the channel inversion charge layer is solved. Excellent agreement has been reported between this model and various numerical simulators [12].

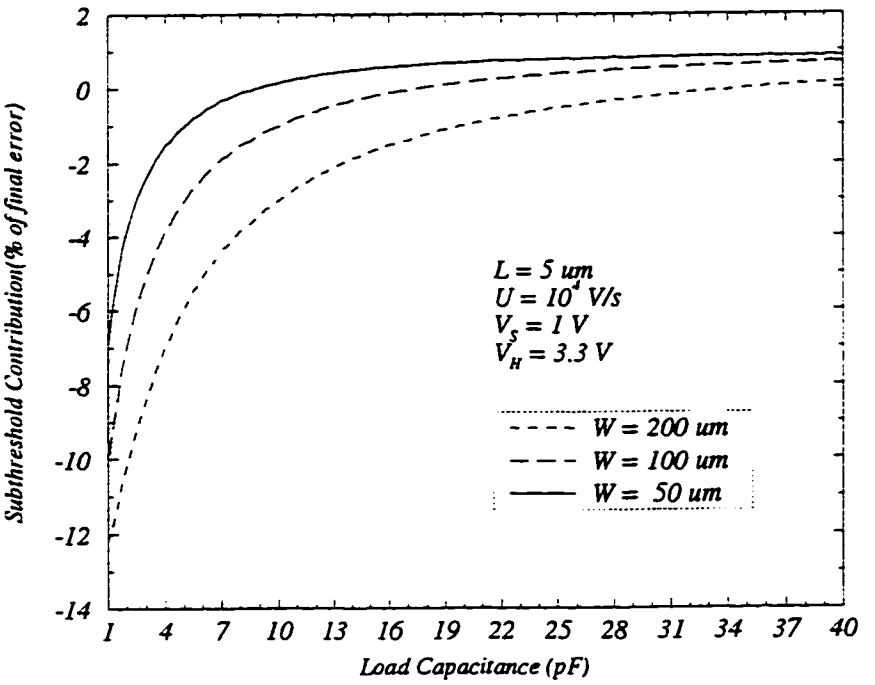

Figure 3.7: Normalized subthreshold effect with respect to the load capacitance for different transistor widths.

3.6 Simulation Results

Fig. 3.8 shows the transient analysis of an analog switch with $W = 100\mu m$ and $L = 5\mu m$. The model parameters of a commercial BiCMOS $0.8\mu m$ process were chosen as the simulation parameters where $N_A = 3.23 \times 10^{16} cm^{-3}$, $T_{ox} = 17.5nm$, $N_{FS} = 820 \times 10^9 cm^{-2}V^{-1}$, $V_{FB} = -0.425V$ and the gate overlap capacitance is 2.74×10^{-12} farads per transistor width (in cm). The SPICE and simple model suggested by Sheu and Hu begin to deviate from the modified and NQS models in the subthreshold region ($t \geq 0.5\mu s$). Figure 3.9 illustrates a similar transient analysis which compares the BSIM3v3 model [22] with the NQS and modified models. In this simulation a different set of parameters that was available for BSIM3v3 has been used.

As can be seen, even the most recent SPICE models such as BSIM3v3 do not provide accurate results in terms of the charge injection error voltage. The final output error voltage for the different gate voltage falling rates is shown in Fig. 3.10. The modified and NQS models are in very good agreement at low and high gate voltage falling rates. At moderate falling rates, there is some discrepancy between the modified model and NQS model results. This is due to the inaccuracy of the MOS transistor model in the moderate inversion region. Chapter 5 has been devoted to the details of this effect. As will be seen in this chapter, this discrepancy can be even more significant under some conditions. In addition to the inaccurate modeling in moderate inversion, the SPICE model (Level-3) considers only subthreshold current and ignores the inversion layer charge in the weak inversion region. Therefore,

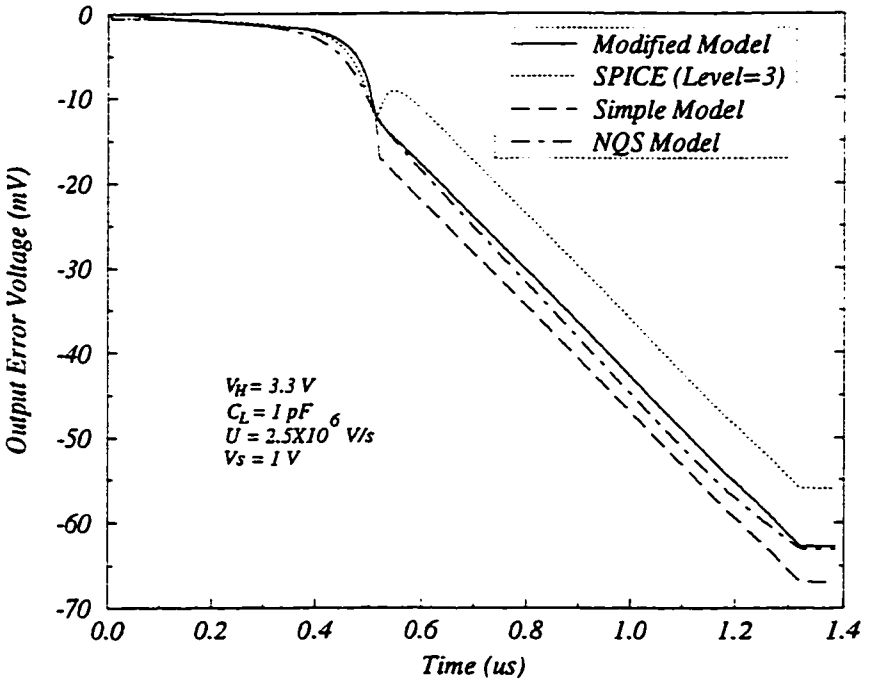

Figure 3.8: Comparison of the output error voltage using different models.

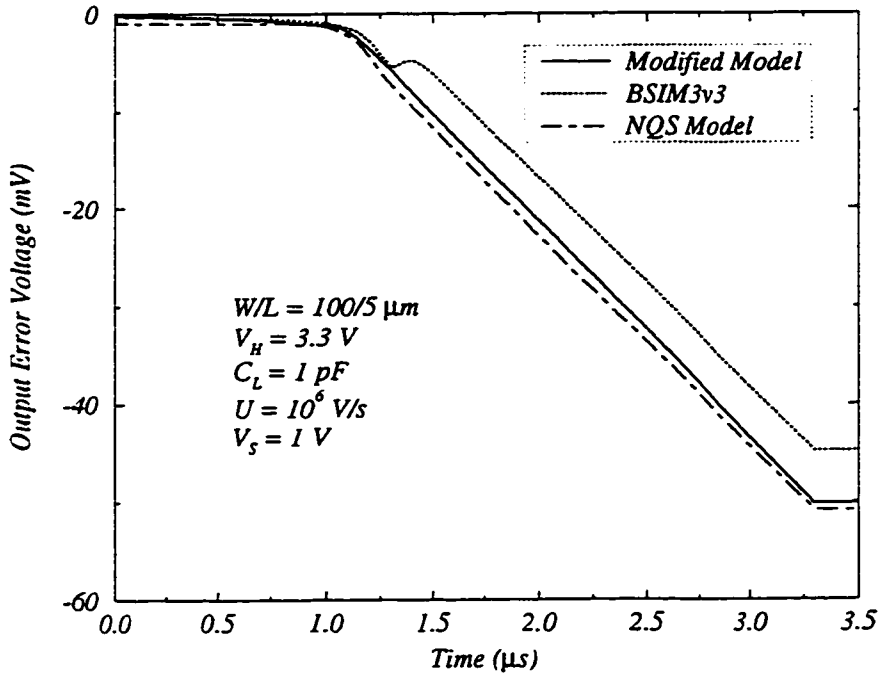

Figure 3.9: Comparison of the output error voltage using different models including BSIM3v3.

it fails to correctly predict the final output error voltage at moderate gate voltage falling rates.

Figs. 3.11 and 3.12 compare the experimental and simulated results published in [13] with the modified model presented in this paper, and show the capability of this model to predict the charge induced output error voltage. The 2D simulation results have been obtained using the program MEDICI [23] which is a two dimentional device simulator.The model parameters used were those presented in [13]. Since N_{FS} and V_{FB} were not specified, the abovementioned process values were chosen for these parameters. Since the results are not particularly sensitive to the values chosen. The sharp drop in the drain current in Fig. 3.12 occurs when the gate voltage reaches

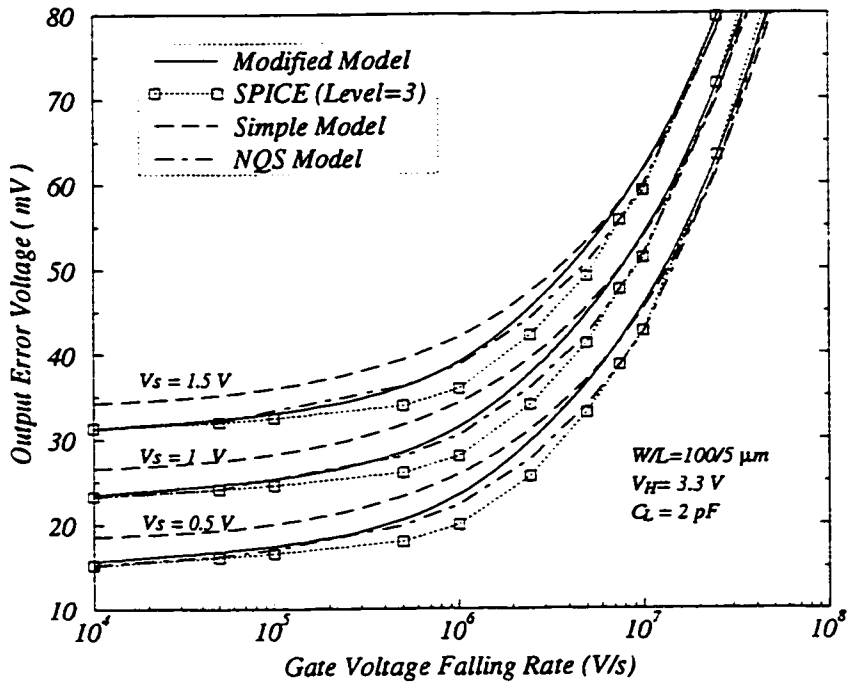

Figure 3.10: Comparison of the different model results of the output error voltage as a function of the gate voltage falling rate.

the low voltage V_L. At this time charge injection of the gate-source overlap capacitance disappears and as a result the output current drops to zero.

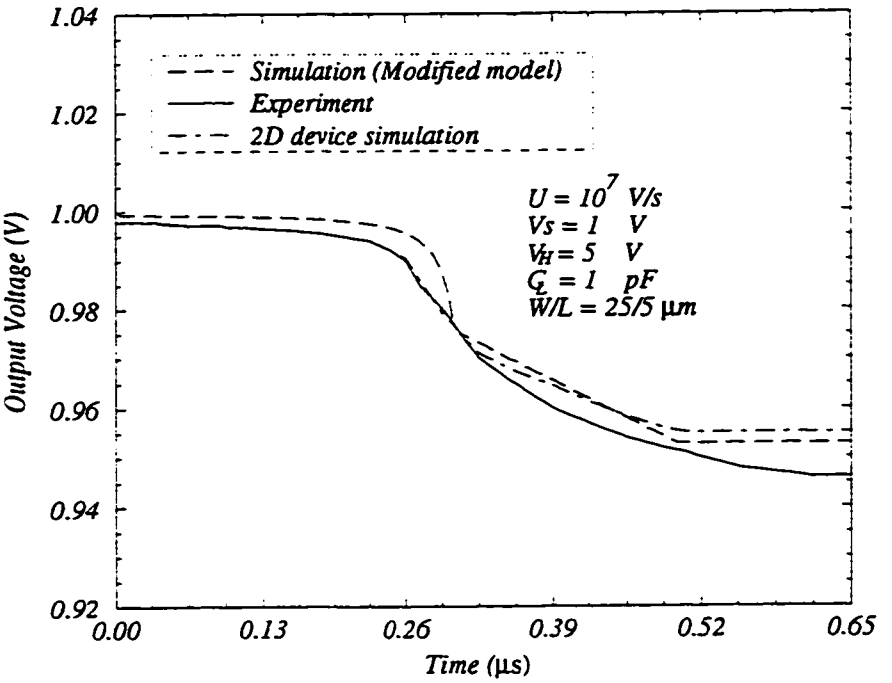

Figure 3.11: Comparison of simulated and experimental results [13] (Output voltage).

3.7 Effect of Source Capacitance

The general equations for the output error voltage in the presence of finite source capacitance have been derived in [7], [8] and [9]. By following the derivation described in Section 3.2, the subthreshold effects can be added to these equations. However, the final differential equations can only be solved numerically. Fig. 3.13 shows the contribution of the subthreshold effects to the final error for various C_S/C_L ratios. The source resistance, R_S is assumed to be infinitely large. As can be seen, the subthreshold effects are more significant for higher C_S/C_L ratios where a relatively higher voltage is developed between the source and drain of the transistor.

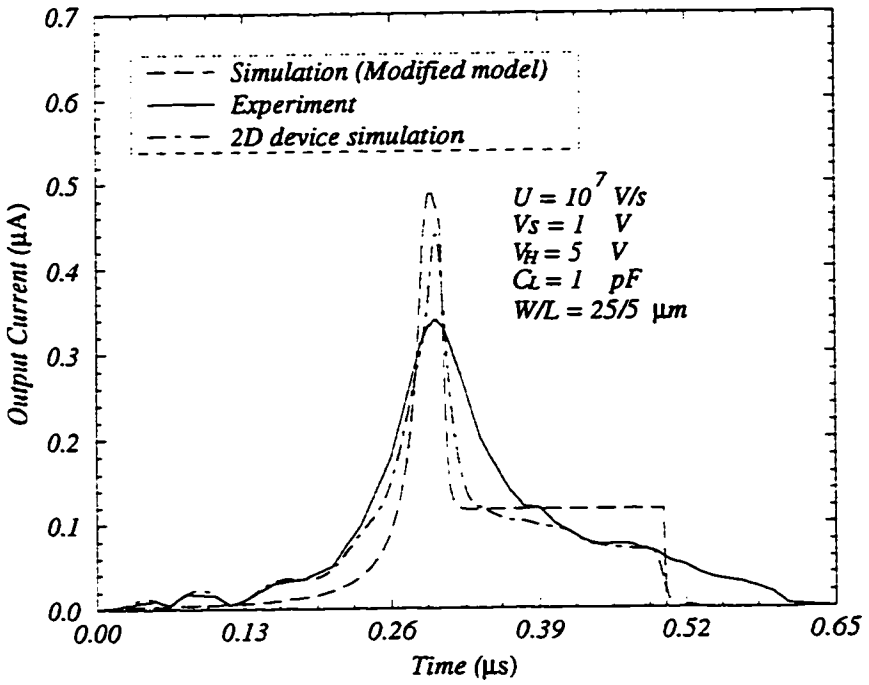

Figure 3.12: Comparison of simulated and experimental results [13] (for the output current).

3.8 Summary

A simple model based on Sheu and Hu's model for analysis of the charge injection error which takes into account subthreshold effects has been described. An approximation has also been proposed to simplify the final error voltage calculation. The model was compared to SPICE and NQS models as well as recently published experimental results. Excellent agreement was achieved in most cases. The modified model provides physical insight into the effects of varying parameters in switching circuits in the weak inversion region.

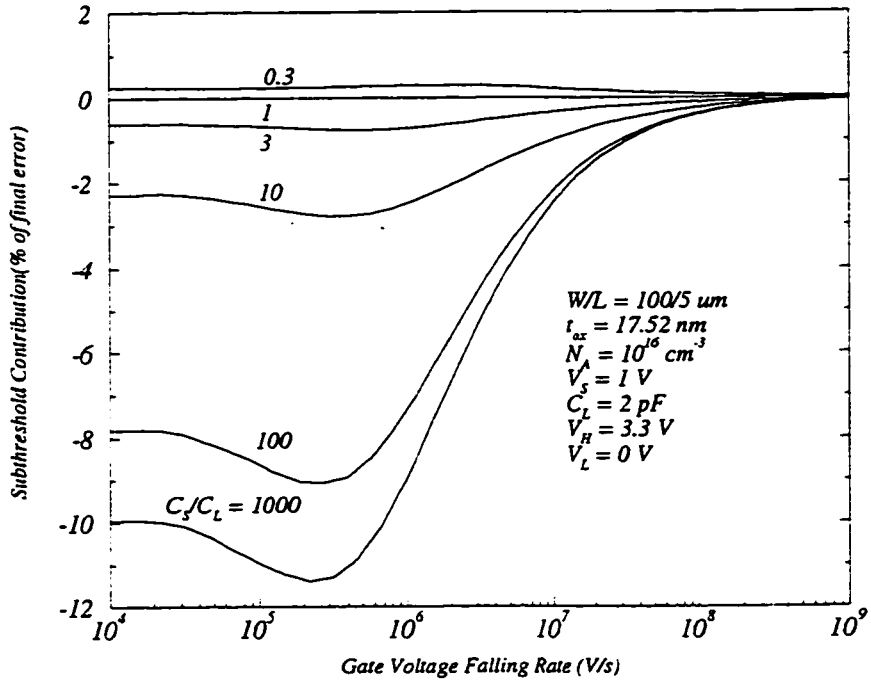

Figure 3.13: Normalized subthreshold effect with respect to the gate voltage falling rate for different source-load capacitance ratios.

Chapter 4

A New DC Model for MOS Transistors

As discussed in Chapter 1, error in the drain current calculation of the switch transistor can lead to significant error in the final charge injection error prediction. Therefore, an accurate MOS transistor model is required for the charge injection error analysis. In the literature, the computationally efficient charge injection error analyses [7–9, 13, 16] are based on a simple quadratic equation for the MOS transistor [24] which introduces large errors into the drain current calculation in the moderate inversion region [24, 25].

In this chapter, a new dc model for MOS transistors is proposed which provides accurate results in the moderate inversion region as well as other regions of operation. This model is computationally efficient and can be used in the charge injection error analysis (see Chapter 5). The motivation for this work came from the fact that at the time of developing the new charge injection model, the only available set of parameters for a commercial process was the one for the SPICE level 3 model. As discussed in the previous chapters, the SPICE level 3 model is not accurate, particularly in the moderate inversion region. Therefore, the developement of this model was required to

improve the accuracy of the new charge injection model. The main advantages of the proposed model are simplicity and the small number of required model parameters.

4.1 Introduction

The MOSFET model required for circuit simulation consists of a steady-state or dc model and a dynamic or ac model. The dc model is used to calculate the quiescent operating points of the circuit. The accuracy of the dc model is therefore critical in simulating transient and ac responses in applications such as evaluating charge injection error in analog switches [4,16], etc. The classical long-channel model proposed by Pao and Sah [26] is device physics based but requires a double integration and is computationally too inefficient for use in circuit simulators. The charge-sheet based models established by Brews [27], Pierret and Shields [28] and Boothryod et al [29] avoid double integration, reduce computation time substantially, and are a good aproximation to the Pao-Sah model. They do, however, still require two surface potential calculations and are therefore not commonly used in SPICE simulators [30]. The most commonly-used models in circuit simulation programs are piece-wise multisection models which have low computation times. Various assumptions for producing a smooth join between the subthreshold and strong inversion regions are used as, for example, in the SPICE level 3 model [21]. Although continuous transitions can be achieved in this model, there are relatively large errors in the moderate inversion region [24]. Several continuous MOSFET models have been reported [22,31,32]. These models are generally more complicated than the simple SPICE level 3 model, but good agreement between their predictions and experiment results have been reported. BSIM models provide more accurate results in the moderate inversion region by increasing the number of model parameters and the com-

putation time. BSIM3v3 is the most recent and popular MOSFET model which was published in early 1997 [22]. In this model, continuity is obtained by introducing a new function which results in continuous channel charge characteristics from subthreshold to strong inversion [22]. The accuracy of the BSIM3v3 model is obtained at the expense of increasing the complexity and the number of parameters. Our variable threshold technique can also be incorporated into BSIM3v3 as an alternative to the proposed function introduced in this model. In summary, the proposed model in this chapter may not be as sophisticated as the BSIM3v3 model in all aspects of circuit simulation, but it is an effective, simple and accurate enough model to be used for charge injection error modelling and therefore, in this application it is prefered to more complicated models such as the BSIM models. Perhaps most importantly, the BSIM3v3 model still fails to accurately predict injection error as indicated in Fig. 3.9.

The new model is based on a simple piece-wise model with exponential and quadratic equations in the subthreshold and strong inversion regions, respectively. Also, a variable threshold voltage method is used to provide more accurate results in the moderate inversion region. In this model, the surface potential calculation is not required in the subthreshold region. In the strong inversion region, only one approximate boundary surface potential calculation is required and this can be obtained using a small number of iterations. The model produces accurate results in the moderate inversion region, is compatible with SPICE models and can be easily incorporated into these programs. The dc results are in very good agreement with those of the Pao-Sah [26], MISNAN [29] and BSIM3v3 [22] models in all regions of operation.

The simple piece-wise model is described in Section 4.2. The variable threshold voltage method for the strong inversion region is derived in Section 4.3. The compatibility of this model with the SPICE models is discussed in

Section 4.4. The details of the implementation of this model are discussed in Section 4.5. The simulation results comparing the new model with the Pao-Sah model, MISNAN model, BSIM3v3 model and experiment are presented in Section 4.6. A summary is given in Section 4.7.

4.2 Simple Piece-Wise Model

An approximate piece-wise model for a MOS transistor is described in this section in order to prepare the basis for developing the variable threshold voltage method in the next section. This simple model is suitable for hand calculations as well as for fast computer simulation of large circuits [24].

4.2.1 Strong Inversion Region Model

The current in a MOS transistor channel involves both drift and diffusion. The diffusion component is due to the concentration gradient of the inversion layer charges. The movement of electrons and holes in the channel as a result of the applied potential between the drain and source terminals characterizes the drift component of the current. In the strong inversion region, the current is mostly due to drift [24], while in the weak inversion region, the current is mostly due to diffusion.

Using the general charge sheet model and ignoring the diffusion component, the drain current in the strong inversion region due to drift is given by

$$I_D = \frac{W}{L} \int_{\psi_{S0}}^{\psi_{SL}} \mu \left(-Q_I'\right) \cdot d\psi_S \tag{4.1}$$

where W, L and μ are the channel width, channel length and surface carrier mobility, respectively. In equation (4.1), Q_I' is the channel inversion layer charge per unit area and ψ_S is the surface potential at a particular point along the channel. The surface potentials corresponding to the source and

drain are represented by ψ_{S0} and ψ_{SL}, respectively.

Using a charge balance equation for the gate charge, it can be shown that

$$Q'_I = -C'_{ox}\left(V_{GB} - V_{FB} - \psi_S + \frac{Q'_I}{C'_{ox}}\right), \tag{4.2}$$

where C'_{ox}, V_{GB} and V_{FB} are the gate-oxide capacitance per unit area, gate-to-bulk voltage and flat band voltage, respectively. The depletion region charge per unit area, Q'_B, is given by

$$Q'_B = -\gamma C'_{ox}\sqrt{\psi_S}, \tag{4.3}$$

where

$$\gamma = \frac{\sqrt{2q\epsilon_S N_A}}{C'_{ox}}.$$

To calculate the drain current in terms of the terminal voltages, the relation between ψ_S and the terminal voltages must be known.

Assuming sufficiently high gate-source and gate-drain voltages, both channel ends can be considered in the strong inversion region. With both channel ends strongly inverted, it is usually assumed [24, 26, 33] that the surface potential, ψ_S, varies linearly along the channel from source to drain. Therefore, it is reasonable to define a quantity $V_{CB}(x)$ such that

$$\psi_S(x) = \phi_B + V_{CB}(x), \tag{4.4}$$

where

$$\begin{aligned} V_{CB}(x=0) &= V_{SB} \\ V_{CB}(x=L) &= V_{DB} \end{aligned}$$

are the values of V_{CB} at the source and drain, respectively. V_{CB} represents the channel to bulk voltage. ϕ_B is the channel surface potential at the source

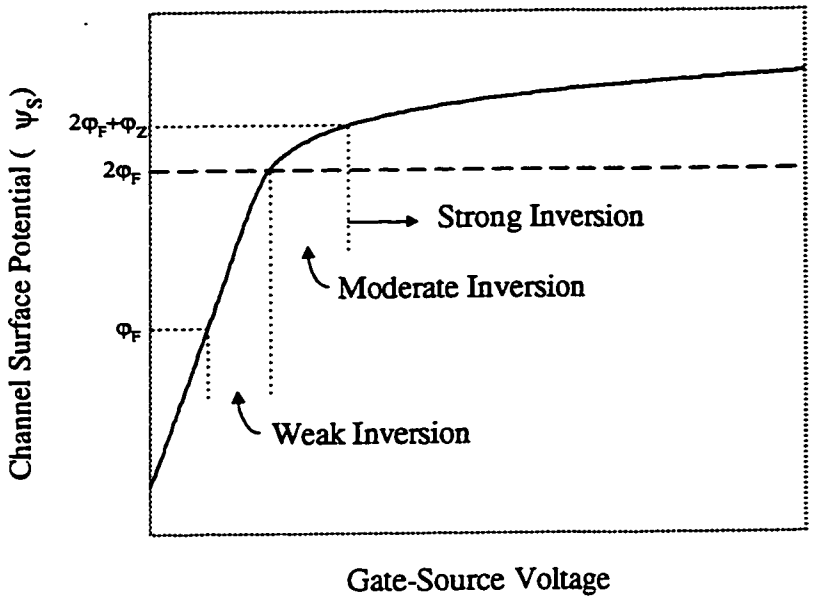

Figure 4.1: The channel surface potential variations with respect to the gate-source voltage in different regions of operation.

when the source-bulk voltage is zero. At the onset of strong inversion, ϕ_B is assumed to be $2\phi_F + \phi_Z$ [24] where ϕ_F is the Fermi potential and ϕ_Z is several ϕ_t ($\phi_t = kT/q$). As the gate-source voltage increases, the value of ϕ_B increases from $2\phi_F + \phi_Z$. Fig. 4.1 shows the typical variations of the surface potential with respect to the gate-source voltage in different regions of operation [24]. For an approximate analysis, often a constant value between $2\phi_F$ and $2\phi_F + \phi_Z$ is chosen for ϕ_B as a compromise [24]. However, this assumption cannot provide accurate results for all gate-source voltages in both moderate and strong inversion regions.

Assuming a constant ϕ_B and substituting (4.4) into (4.2) and (4.3), Q'_B and Q'_I are given by

$$Q'_B = -\gamma C'_{ox}\sqrt{\phi_B + V_{CB}} \tag{4.5}$$

and

$$Q'_I = -C'_{ox}\left(V_{GB} - V_{FB} - \phi_B - V_{CB} + \frac{Q'_B}{C'_{ox}}\right). \tag{4.6}$$

Since $\frac{d\psi_S}{dx} = \frac{dV_{CB}}{dx}$, it can be shown from (4.1) that

$$I_D = \frac{W}{L} \int_{V_{SB}}^{V_{DB}} \mu \left(-Q_I'\right) \cdot dV_{CB}. \tag{4.7}$$

Using (4.5) and (4.6) in (4.7) and calculating the integral by assuming constant μ, the drain current is given by

$$\begin{aligned} I_D &= \frac{W}{L} \mu C_{ox}' \left\{ \left(V_{GS} - V_{FB} - \phi_B\right) V_{DS} - \frac{1}{2} V_{DS}^2 \right. \\ &\left. - \frac{2}{3} \gamma \left[\left(\phi_B + V_{SB} + V_{DS}\right)^{3/2} - \left(\phi_B + V_{SB}\right)^{3/2} \right] \right\}. \end{aligned} \tag{4.8}$$

In the derivation of (4.8) the following relationships have been used:

$$\begin{aligned} V_{GB} &= V_{GS} + V_{SB} \\ V_{DB} &= V_{DS} + V_{SB}. \end{aligned}$$

Although the model developed so far provides fairly good results, it is still complicated due to the $\frac{3}{2}$ powers involved [24]. These powers originate from the square-root term in (4.5).

Figure 4.2 shows the variations of the quantity $-\frac{Q_B'}{C_{ox}'}$ with respect to V_{CB}. As can be seen, this quantity does not change significantly with V_{CB} [24]. Therefore, as a further simplification, it is reasonable to approximate $-\frac{Q_B'}{C_{ox}'}$ by the first two terms of its Taylor expansion around the point $V_{CB} = V_{SB}$. Thus,

$$-\frac{Q_B'}{C_{ox}'} \simeq \gamma \sqrt{\phi_B + V_{SB}} + \delta \left(V_{CB} - V_{SB}\right) \tag{4.9}$$

where δ is the slope of $-\frac{Q_B'}{C_{ox}'}$ vs. V_{CB} evaluated at $V_{CB} = V_{SB}$. The value of δ is given by

$$\delta = \frac{\gamma}{2\sqrt{\phi_B + V_{SB}}}. \tag{4.10}$$

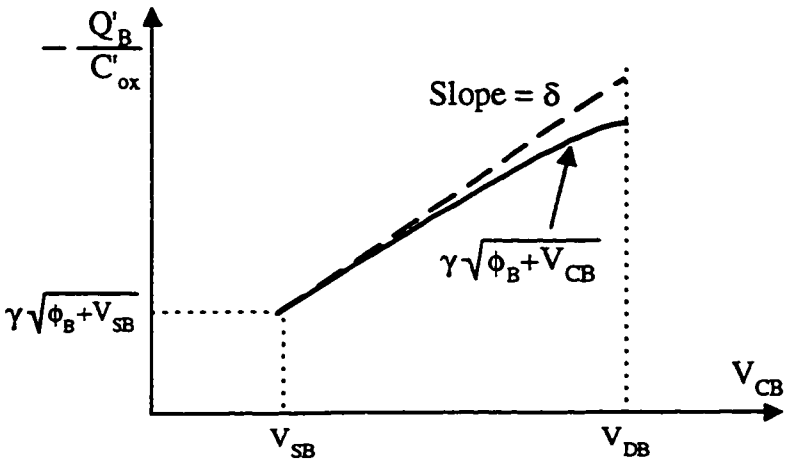

Figure 4.2: The variations of $-\frac{Q'_B}{C'_{ox}}$ in the strong inversion region. The solid line is the accurate calculation and the broken line is the approximation using a Taylor expansion at $V_{CB} = V_{SB}$.

Using Q'_B from (4.9) in (4.6), it can be shown that

$$\begin{aligned} Q'_I(V_{CB}) &= -C'_{ox}V_{GB} - V_{SB} - V_{FB} - \phi_B - \gamma\sqrt{\phi_B + V_{SB}} \\ &\quad - (1+\delta)(V_{CB} - V_{SB}). \end{aligned} \tag{4.11}$$

A simplified drain current equation can be derived by using (4.11) in (4.7) as follows

$$I_D = \frac{W}{L}\mu C'_{ox}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}(1+\delta)V_{DS}^2\right] \tag{4.12}$$

where

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B + V_{SB}} \tag{4.13}$$

is the threshold voltage. It is important to note that in the derivation of (4.12), all the approximations have been made at the source, therefore, the threshold voltage defined in (4.13) is taken at the source and this cannot be an accurate representation for the threshold voltage at every point in the channel or for different gate-source voltages.

The drain current for large values of V_{DS} is assumed to be independent of V_{DS} and can be found by calculating the maximum value of I_D in (4.12). This maximum occurs at $V_{DS} = V'_{DS}$ where

$$V'_{DS} = \frac{V_{GS} - V_T}{1 + \delta}, \tag{4.14}$$

and the corresponding value of the drain current is given by

$$I_D = \frac{W}{L}\mu C'_{ox}\frac{(V_{GS} - V_T)^2}{2(1 + \delta)}. \tag{4.15}$$

Thus, the complete model for the strong inversion region becomes

$$I_D = \begin{cases} \frac{W}{L}\mu C'_{ox}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}(1 + \delta)V_{DS}^2\right] & V_{DS} \leq V'_{DS} \\ \frac{W}{L}\mu C'_{ox}\frac{(V_{GS} - V_T)^2}{2(1 + \delta)} & V_{DS} > V'_{DS} \end{cases} \tag{4.16}$$

Channel length modulation effects have not been taken into account in equation (4.16).

Figure 4.3 shows the $I_D - V_{DS}$ characteristics obtained from this approximate model [24].

4.2.2 Weak-Inversion Region Model

In the weak inversion region, the drain current is mostly due to diffusion. Ignoring the drift component, the drain current in this region was described by Barron [33] and can be written as follows:

$$I_D = \frac{\beta\gamma V_t^{3/2}}{2\sqrt{U_S - 1}}\left(1 - e^{-\frac{V_{DS}}{V_t}}\right)e^{-2U_F - \xi_S}.e^{U_S}. \tag{4.17}$$

In (4.17), β is the transistor conductance coefficient ($\mu C'_{ox}\frac{W}{L}$), V_t is the thermal voltage (kT/q), U_F is the normalized Fermi potential (ϕ_F/V_t), and U_S

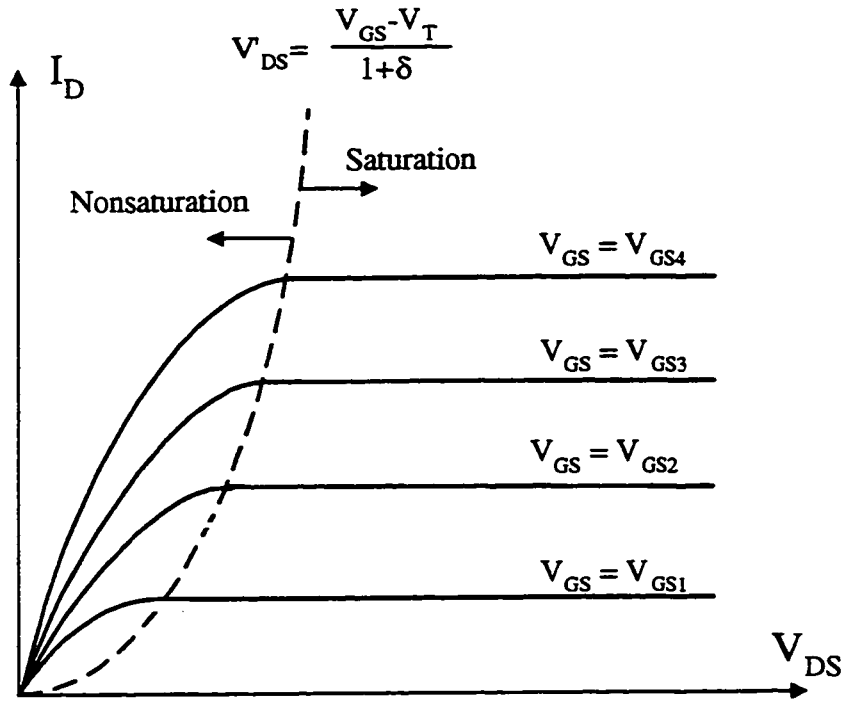

Figure 4.3: $I_D - V_{DS}$ characteristics as obtained from (4.16).

is the normalized surface potential at the source and $\xi_S = \frac{V_{SB}}{V_t}$. The surface potential can be calculated by using [24]

$$U_G = U_S + \gamma' \left(e^{U_S - 2U_F - \xi_S} + U_S - 1\right)^{1/2} \tag{4.18}$$

where

$$\gamma' = \frac{\gamma}{\sqrt{V_t}} \tag{4.19}$$

and

$$U_G = \frac{V_{GB} - V_{FB}}{V_t}. \tag{4.20}$$

To find the drain current in terms of the terminal voltages, U_S in (4.17) can be replaced by its value from (4.18) which results in a complicated expression for I_D. To derive an approximate but simple expression for the drain current, a Taylor expansion of U_S around an appropriate point (U_S^*) can be

used. The Taylor expansion of U_S is given by

$$U_S = U_S^* + \left.\frac{dU_S}{dU_G}\right|_{U_S^*} . (U_G - U_G^*) \tag{4.21}$$

where

$$U_G^* = U_S^* + \gamma' \left(e^{U_S^* - 2U_F - \xi_S} + U_S^* - 1\right)^{1/2}. \tag{4.22}$$

The slope of U_S vs U_G, $\frac{1}{n}$, can be found from (4.18) as

$$\left.\frac{dU_S}{dU_G}\right|_{U_S^*} = \frac{1}{1 + \frac{\gamma'\left(e^{U_S^* - 2U_F - \xi_S + 1}\right)}{2\sqrt{e^{U_S^* - 2U_F - \xi_S} + U_S^* - 1}}} = \frac{1}{n}. \tag{4.23}$$

Substituting (4.21) and (4.23) into the exponential term of (4.17), the drain current is given by

$$I_D = \frac{\beta\gamma V_t^{3/2}}{2\sqrt{U_S - 1}} \left(1 - e^{-\frac{V_{DS}}{V_t}}\right) e^{-2U_F - \xi_S} . e^{U_S^* + \frac{U_G - U_G^*}{n}}. \tag{4.24}$$

The channel surface potential at the source and at the beginning of the weak inversion region ($U_S^* = 2U_F + \xi_S$) can be chosen as an appropriate value for U_S^* which simplifies (4.24) as follows:

$$I_D = \frac{\beta\gamma V_t^{3/2}}{2\sqrt{U_S - 1}} \left(1 - e^{-\frac{V_{DS}}{V_t}}\right) e^{\frac{U_G - U_G^*}{n}}. \tag{4.25}$$

Using (4.20) and (4.22) in (4.25), the drain current can be written in the following simple form:

$$I_D = \frac{\beta\gamma V_t^{3/2}}{2\sqrt{U_S - 1}} \left(1 - e^{-\frac{V_{DS}}{V_t}}\right) e^{\frac{V_{GS} - V_T}{nV_t}} \tag{4.26}$$

where

$$V_T = V_{FB} + 2U_F V_t + \gamma\sqrt{2U_F V_t + V_{SB}} \tag{4.27}$$

and

$$n = 1 + \frac{\gamma}{\sqrt{2U_F V_t + V_{SB}}}. \tag{4.28}$$

Since the exponential term in (4.26) ($e^{\frac{V_{GS}-V_T}{nV_t}}$) is the dominant term, the variation of U_S in the square-root term in (4.26) can be ignored without affecting the accuracy significantly. Using $U_S = U_S^*$ in the square-root term and considering the fact that for practical U_F values $2U_F \gg 1$, the drain current in subthreshold is given by

$$I_D = \frac{\beta\gamma V_t^2}{2\sqrt{2U_F V_t + V_{SB}}}\left(1 - e^{-\frac{V_{DS}}{V_t}}\right) e^{\frac{V_{GS}-V_T}{nV_t}} \tag{4.29}$$

where V_T and n are calculated from (4.27) and (4.28), respectively. Equation (4.29) is valid for $V_{GS} \leq V_T$ when $V_{GS} = V_T$ is the switching point from the strong inversion equation to the weak inversion equation. Equation (4.27) is the same as the derived equation for V_T in the strong inversion region (equation (4.13)) when ϕ_B is chosen to be $2U_F V_t$.

In choosing different joining techniques between the strong and weak inversion regions, a slightly different switching point may be used. For a general switching point between the strong inversion and subthreshold regions when $V_{GS} = V_{on}$, equation (4.29) can be written as follows:

$$I_D = \frac{\beta\gamma V_t^2}{2\sqrt{2U_F V_t + V_{SB}}}\left(1 - e^{-\frac{V_{DS}}{V_t}}\right) e^{\frac{V_{GS}-V_{on}}{nV_t}}. \tag{4.30}$$

For instance, in the SPICE level 3 model $V_{on} = V_T + nV_t$ is chosen as the joining point and the drain current at the beginning of the weak inversion region is matched with the current at the end of the strong inversion region to maintain current continuity [21]. Thus,

$$I_D = I_0 e^{\frac{V_{GS}-V_{on}}{nV_t}}, \quad V_{GS} \leq V_{on} \tag{4.31}$$

where I_0 is calculated from (4.16) at $V_{GS} = V_{on}$. In this model, equation (4.16) is used to calculate the drain current for $V_{GS} > V_{on}$.

4.3 Variable Threshold Voltage Method

Although the model presented in Section 4.2 is very simple and computationally efficient, it generates large errors especially around the joining point. Figure 4.4 shows the comparison between the Pao-Sah model [26] and the SPICE level 3 model which is based on equations (4.16) and (4.31). The Pao-Sah model was chosen because it utilizes the original equations derived from device physics, and therefore, it is very accurate in terms of the drain current calculation. The NQS model explained in Chapter 3 which is derived from the original device equations after some simplifications can also be used as the reference model. As can be seen, large errors occur in the drain current calculation around the transition point. These errors originate from the approximations made in the derivation of (4.16). The most inaccurate approximation is the approximation of a constant ϕ_B in (4.4) that resulted in a constant threshold voltage. As discussed previously, ϕ_B varies with gate-source voltage and thus for more accurate results the value of ϕ_B corresponding to each value of V_{GS} should be used in (4.4). However, for each value of V_{GS}, the derivation procedure of (4.16) is valid and (4.16) can be used for the drain current calculation. In the final form, the effect of (4.4) appears in the values of δ and V_T (Equations (4.10) and (4.13)).

In the new variable threshold voltage method, an appropriate ϕ_B is calculated for each value of V_{GS} and the corresponding values of δ and V_T are found from (4.10) and (4.13). The resulting values of δ and V_T can be used for the drain current calculation in (4.16). In other words, the surface potential is used to shape the threshold voltage function in the strong inversion region to achieve more accurate results.

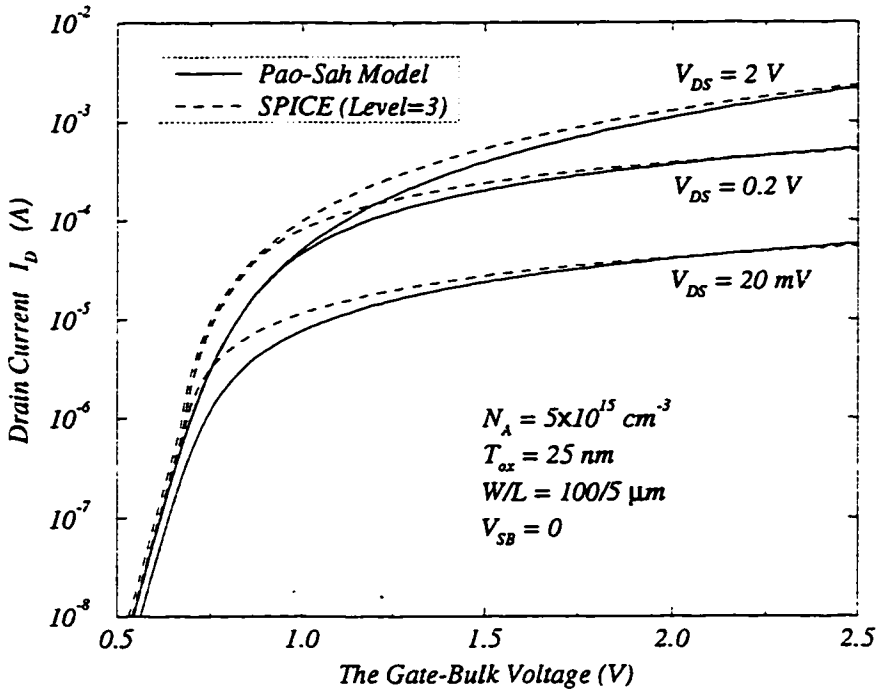

Figure 4.4: Comparison between the Pao-Sah and SPICE level 3 models.

In the new model the drain current in the weak inversion region is calculated from (4.30). It is important to note that (4.30) is more accurate than (4.31) since it results directly from the exact Barron equation [33]. However, in (4.31) the accuracy of the current in the weak inversion region depends on the accuracy of the model in the strong inversion region.

As will be shown in Section 4.6, the result of this newly proposed model is in excellent agreement with very accurate models.

4.3.1 Finding The Appropriate Value of ϕ_B

Assuming a linear variation for the surface potential in the linear region of operation ($V_{DS} < V'_{DS}$) [24, 33] and evaluating (4.4) at the source, it can be

shown that

$$\phi_B = \psi_S - V_{SB} = (U_S - \xi_S)V_t, \tag{4.32}$$

where U_S and ξ_S are the normalized values of ψ_S and V_{SB}, respectively. Using (4.32) in the threshold voltage equation, (4.13), $\overline{V_T}$ can be calculated from

$$\overline{V_T} = V_{FB} + (U_S - \xi_S)V_t + \gamma\sqrt{U_S V_t}. \tag{4.33}$$

$\overline{V_T}$ is the modified threshold voltage. For each value of the gate voltage, U_S can be found from the solution of the exact equation for U_S [24], given by

$$U_G = U_S + \gamma' \left(e^{U_S - 2U_F - \xi_S} + U_S - 1\right)^{1/2} \tag{4.34}$$

where $\gamma' = \gamma/\sqrt{V_t}$, U_F is the normalized Fermi potential and

$$U_G = \frac{V_{GB} - V_{FB}}{V_t}. \tag{4.35}$$

Making an appropriate initial guess along with the second order Newton-Raphson procedure, the surface potential from (4.34) can be calculated fairly quickly [29] (Appendix B). The simulation results in Section 4.6 show that only one iteration can provide sufficient accuracy for most purposes. If the fast surface state charge density is not zero, it can be considered in equation (4.35) by adding $\frac{qN_{FS}}{C_{ox}}$.

In this model, $\overline{V_{on}}$ which is the switching point (joining point) between the subthreshold and strong inversion regions, is chosen to be

$$\overline{V_{on}} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F + V_{SB}}. \tag{4.36}$$

This value of $\overline{V_{on}}$ is equal to the gate-source voltage corresponding to the value of $U_S = 2U_F + \xi_S$ in equation (4.34).

The drain current can be calculated from (4.16) and (4.26) by substituting

$\overline{V_T}$ and $\overline{V_{on}}$ for V_T and V_{on}. From (4.16) for $V_{GS} \geq \overline{V_{on}}$

$$I_D = \begin{cases} \beta\left[\left(V_{GS} - \overline{V_T}\right) V_{DS} - \frac{(1+\delta)}{2} V_{DS}^2\right] & V_{DS} \leq V'_{DS} \\ \beta\frac{\left(V_{GS} - \overline{V_T}\right)^2}{2(1+\delta)} & V_{DS} > V'_{DS} \end{cases} \tag{4.37}$$

and from (4.26) for $V_{GS} < \overline{V_{on}}$

$$I_D = \frac{\beta\gamma V_t^2}{2\sqrt{\phi_B + V_{SB}}}\left(1 - e^{-V_{DS}/V_t}\right) e^{\frac{V_{GS} - \overline{V_{on}}}{nV_t}}. \tag{4.38}$$

In the derivation of (4.38), U_S in (4.26) has been replaced by its value from (4.32) ($U_S = (\phi_B + V_{SB})/V_t$).

The threshold voltage corresponding to the value of U_S calculated from (4.34) does not necessarily guarantee the continuity of the drain currents calculated from (4.38) and (4.37) in the subthreshold and strong inversion regions, respectively. To maintain current continuity, $\overline{V_T}$ can be adjusted by adding a parameter $V_{T(Shift)}$ to (4.33). The threshold voltage is then given by

$$\overline{V_T} = V_{FB} + (U_S - \xi_S)V_t + \gamma\sqrt{U_S V_t} + V_{T(Shift)}. \tag{4.39}$$

$V_{T(Shift)}$ is determined so that $\overline{V_T}$ provides continuity for the drain current when substituted in (4.37) and (4.38). In other words, $V_{T(Shift)}$ adjusts the threshold voltage so that at the joining point the drain current calculated from (4.37) is equal to the drain current calculated from (4.38).

In order to obtain more accurate results, the continuity of the derivative of the drain current with respect to V_{GB} can be achieved by adding another degree of freedom to the equations. To accomplish this, ξ_S in (4.34) and (4.39) can be replaced by ξ where ξ is treated as a fitting parameter. Thus, (4.34) and (4.39) can be written as

$$U_G = U_S + \gamma'\left(e^{U_S - 2U_F - \xi} + U_S - 1\right)^{1/2}, \tag{4.40}$$

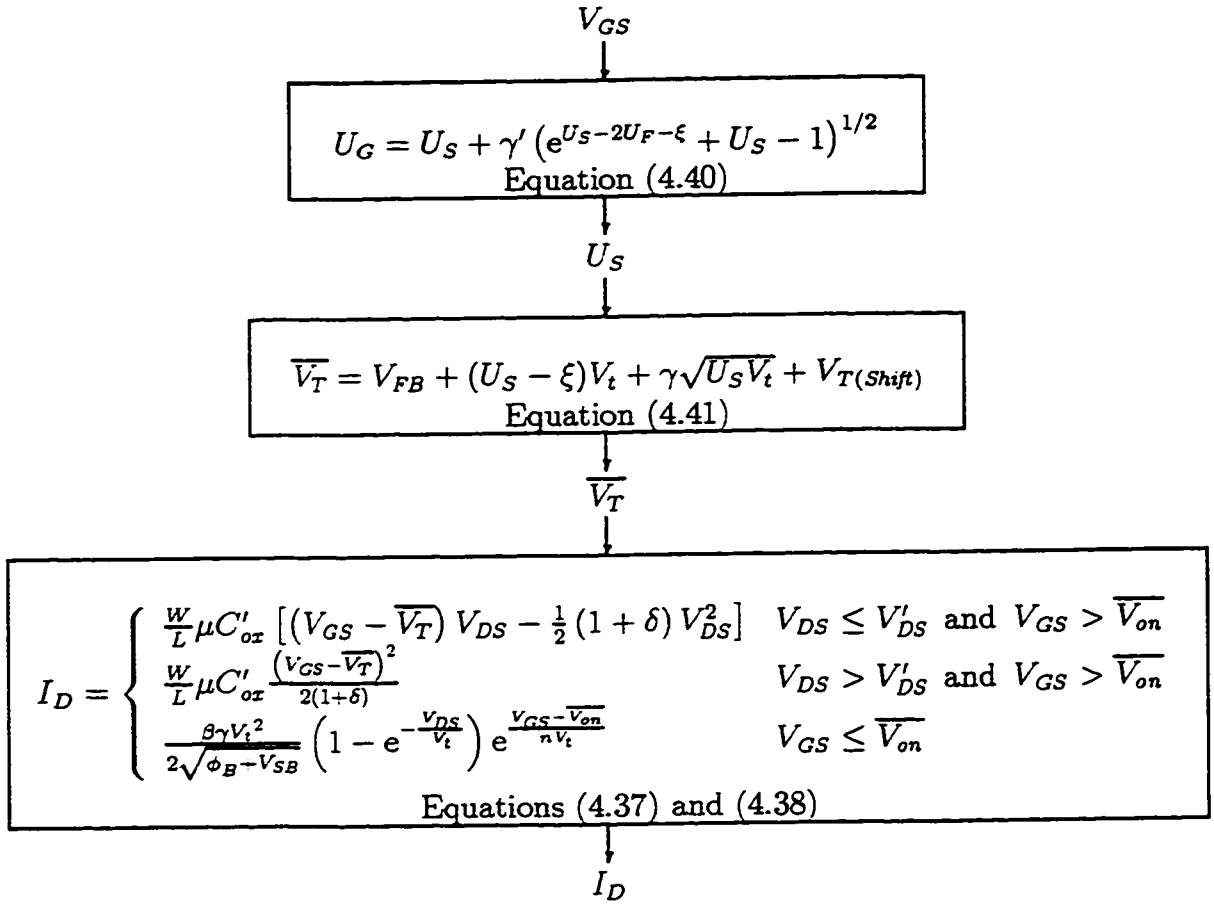

Figure 4.5: The variable threshold voltage method procedure.

$$\overline{V_T} = V_{FB} + (U_S - \xi)V_t + \gamma\sqrt{U_S V_t} + V_{T(Shift)}. \tag{4.41}$$

Physically this means that instead of calculating the threshold voltage at the source in the conventional method, it is calculated at a point corresponding to ξ in the new model. The method for finding ξ and $V_{T(Shift)}$ is shown in Section 4.3.2.

Once the values of ξ and $V_{T(Shift)}$ are determined, the procedure for calculating the drain current using the variable threshold voltage method can be summarized as shown in Fig. 4.5.

4.3.2 Calculation of $V_{T(Shift)}$ and ξ

Calculation of $V_{T(Shift)}$

As discussed previously, the drain current continuity at the joining point ($V_{GS} = \overline{V_{on}}$) can be preserved by adjusting the value of $V_{T(Shift)}$ so that (4.41) provides an appropriate threshold voltage ($\overline{V_T} = \overline{V_{T(on)}}$) when $V_{GS} = \overline{V_{on}}$ ($U_S = U_{S(on)}$). V_{on} is the threshold voltage that results in the same I_D values in the evaluation of (4.37) and (4.38) when it is substituted for $\overline{V_T}$ in (4.37). Using (4.37) and (4.38) and solving for $\overline{V_{T(on)}}$

$$\overline{V_{T(on)}} = \begin{cases} \overline{V_{on}} - \dfrac{1}{V_{DS}}\left[\dfrac{I_{D(on)}}{\beta} + \dfrac{(1+\delta)\,V_{DS}^2}{2}\right] & V_{DS} \le \sqrt{\dfrac{2I_{D(on)}}{(1+\delta)\,\beta}} \\ \overline{V_{on}} - \sqrt{\dfrac{2\,(1+\delta)\,I_{D(on)}}{\beta}} & V_{DS} > \sqrt{\dfrac{2I_{D(on)}}{(1+\delta)\,\beta}} \end{cases} \tag{4.42}$$

where

$$I_{D(on)} = \frac{\beta\gamma V_t^2}{2\sqrt{\phi_B + V_{SB}}}\left(1 - e^{-\frac{V_{DS}}{V_t}}\right).$$

Once the value of $\overline{V_{T(on)}}$ is known, $V_{T(Shift)}$ can be calculated by evaluating (4.41) at the joining point. Thus,

$$V_{T(Shift)} = \overline{V_{T(on)}} - V_{FB} - (U_{S(on)} - \xi)\,V_t - \gamma\sqrt{U_{S(on)}V_t}. \tag{4.43}$$

Calculation of ξ

The value of ξ is found so that the drain current slope continuity is maintained at the joining point. The drain current slope can be calculated from the derivatives of (4.37) and (4.38). From (4.38) for $V_{GS} \le \overline{V_{on}}$

$$\frac{dI_D}{dV_{GS}} = \frac{\beta\gamma V_t}{2n\sqrt{\phi_B + V_{SB}}}\left(1 - e^{-\frac{V_{DS}}{V_t}}\right)e^{\frac{V_{GS}-\overline{V_{on}}}{nV_t}} \tag{4.44}$$

and from (4.37) for $V_{GS} > \overline{V_{on}}$

$$\frac{dI_D}{dV_{GS}} = \begin{cases} \beta\left(1 - \frac{d\overline{V_T}}{dU_S}.\frac{dU_S}{dV_{GS}}\right).V_{DS} & V_{DS} \leq V'_{DS} \\ \beta\left(1 - \frac{d\overline{V_T}}{dU_S}.\frac{dU_S}{dV_{GS}}\right).\sqrt{\frac{2I_D}{\beta(1+\delta)}} & V_{DS} > V'_{DS} \end{cases} \tag{4.45}$$

It should be noted that $dV_{GS} = dV_{GB}$ in the derivation of (4.45). The value of V'_{DS} is also modified corresponding to the new threshold voltage.

The derivatives in (4.45) can be calculated from (4.40) and (4.41). From (4.41)

$$\frac{d\overline{V_T}}{dU_S} = V_t\left(1 + \frac{\gamma}{2\sqrt{U_S V_t}}\right) \tag{4.46}$$

and from (4.40) it can be shown that

$$\frac{dU_S}{dV_{GB}} = \frac{1}{V_t\left(1 + \frac{\gamma'(1+\alpha)}{2\sqrt{\alpha+U_S-1}}\right)} \tag{4.47}$$

where

$$\alpha = e^{U_S - 2U_F - \xi} = \left(\frac{U_G - U_S}{\gamma'}\right)^2 - U_S + 1. \tag{4.48}$$

At the joining point, $V_{GS} = \overline{V_{on}}$ and the corresponding values of U_S and U_G can be represented by $U_{S(on)}$ and $U_{G(on)}$ $\left(U_{G(on)} = \frac{\overline{V_{on}} - V_{FB}}{V_t}\right)$. It is important to note that the appropriate value of $U_{S(on)}$ along with $U_{G(on)}$ must satisfy equation (4.40) as follows:

$$U_{G(on)} = U_{S(on)} + \gamma'\left(e^{U_{S(on)} - 2U_F + \xi} + U_{S(on)} - 1\right)^{1/2}. \tag{4.49}$$

Evaluating (4.44) and (4.45) at the joining point by using (4.46) and (4.47), the drain current slope at the joining point for both sides can be found. Forcing the slope to be continuous at the joining point when switching between (4.44) and (4.45), the following equations can be derived depending

on the value of V_{DS}. For $V_{DS} \leq V'_{DS}$

$$\left[1 - \frac{1 + \frac{\gamma'}{2\sqrt{U_{S(on)}}}}{1 + \frac{\gamma'(1+\alpha_{on})}{2\sqrt{\alpha_{on}+U_{S(on)}-1}}}\right] = \frac{\gamma V_t}{2nV_{DS}\sqrt{\phi_B + V_{SB}}} \cdot \left(1 - e^{-\frac{V_{DS}}{V_t}}\right) \tag{4.50}$$

and for $V_{DS} > V'_{DS}$

$$\left[1 - \frac{1 + \frac{\gamma'}{2\sqrt{U_{S(on)}}}}{1 + \frac{\gamma'(1+\alpha_{on})}{2\sqrt{\alpha_{on}+U_{S(on)}-1}}}\right] = \sqrt{\frac{\beta(1+\delta)}{2I_{D(on)}(\phi_B + V_{SB})}} \frac{\gamma V_t}{2n} \cdot \left(1 - e^{-\frac{V_{DS}}{V_t}}\right). \tag{4.51}$$

In (4.50) and (4.51), $I_{D(on)}$ is the drain current at the joining point which can be calculated from (4.38) when $V_{GS} = \overline{V_{on}}$ as

$$I_{D(on)} = \frac{\beta\gamma V_t^2}{2\sqrt{\phi_B + V_{SB}}} \left(1 - e^{-\frac{V_{DS}}{V_t}}\right) \tag{4.52}$$

and

$$\alpha_{on} = e^{U_{S(on)} - 2U_F - \xi} = \left(\frac{U_{G(on)} - U_{S(on)}}{\gamma'}\right)^2 - U_{S(on)} + 1. \tag{4.53}$$

The only unknown parameter in (4.50) and (4.51) is $U_{S(on)}$. Therefore, by solving (4.50) or (4.51) (depending on the value of V_{DS}) $U_{S(on)}$ can be calculated. Once $U_{S(on)}$ is known, ξ can be found from (4.49) as follows

$$\xi = U_{S(on)} - 2U_F - \ln(\alpha_{on}). \tag{4.54}$$

Using the values of ξ and $V_{T(Shift)}$ that are calculated above in the procedure of Fig. 4.5, the drain current can be found at any value of V_{GS}.

It should be noted that a set of ξ and $V_{T(Shift)}$ values must be calculated for each value of V_{DS}. However, at values of V_{DS} such that V_{DS} is several times larger than V_t, ξ and as a result $V_{T(Shift)}$ are independent of V_{DS} and therefore it is not necessary to calculate them for each V_{DS} value.

4.3.3 Approximate Values of $V_{T(Shift)}$ and ξ

Since the exact solution of (4.50) and (4.51) requires numerical calculations, an approximation is developed to obtain simple equations for ξ and $V_{T(Shift)}$.

For practical values of the device parameters, $\frac{\alpha_{on}}{U_{S(on)}} \ll 1$ and $\gamma'(1+\alpha_{on}) \ll 2\sqrt{\alpha_{on}+U_{S(on)}}$. Therefore, in equations (4.50) and (4.51) it can be shown that

$$\left[1-\frac{1+\frac{\gamma'}{2\sqrt{U_{S(on)}}}}{1+\frac{\gamma'(1+\alpha_{on})}{2\sqrt{\alpha_{on}+U_{S(on)}-1}}}\right] \simeq \frac{\alpha_{on}\gamma'}{2\sqrt{U_{S(on)}}}. \tag{4.55}$$

Using (4.55) and assuming that $U_{S(on)} \simeq 2U_F + \xi_S$, equations (4.50) and (4.51) can be simplified to

$$\alpha_{on} \simeq \begin{cases} \dfrac{V_t}{nV_{DS}}\left(1-e^{-\frac{V_{DS}}{V_t}}\right) & V_{DS} \le V'_{DS} \\ \left[\dfrac{(1+\delta)\sqrt{\phi_B+V_{SB}}}{n^2\gamma}\left(1-e^{-\frac{V_{DS}}{V_t}}\right)\right]^{\frac{1}{2}} & V_{DS} > V'_{DS} \end{cases} \tag{4.56}$$

An approximate value for $U_{S(on)}$ can be found from (4.49) by assuming $\frac{\alpha_{on}}{U_{S(on)}} \ll 1$, given by

$$U_{S(on)} \simeq \left(\frac{-\gamma'}{2}+\sqrt{\left(\frac{\gamma'}{2}\right)^2+U_{G(on)}}\right)^2. \tag{4.57}$$

The simple equations (4.56) and (4.57) can be used to calculate ξ and $V_{T(Shift)}$ from (4.54) and (4.43).

These approximations significantly simplify the procedure for finding ξ and $V_{T(Shift)}$. In Section 4.6, the approximate values of ξ and $V_{T(Shift)}$ have been used for the new model calculations. The results show the validity of these approximations.

4.4 Compatibility with SPICE Models

Since this new model uses the same fundamental equations (equations (4.37) and (4.38)) as most SPICE models such as the SPICE level 3 and BSIM models, it can be easily incorporated into SPICE programs. All other effects such as short channel and saturation effects can then be taken into account as before. For instance, in Section 4.6 the SPICE level 3 model has been modified using the new variable threshold voltage technique to produce an improved comprehensive model. The implementation of the modified SPICE level 3 model is described in Section 4.5.

4.5 Implementation

The details of how the new variable threshold voltage method is incorporated into the SPICE level 3 model are presented in this section.

4.5.1 The SPICE Level 3 Model

In the SPICE level 3 model, the drain current is given by [34]

$$I_D = \mu_{eff} C'_{ox} \frac{W_{eff}}{L_{eff}} \left[V_{GS} - V_T - \frac{1 + f_b}{2} v_{de} \right] v_{de} \tag{4.58}$$

where L_{eff} and W_{eff} are the effective channel length and width, respectively. f_b is determined by the following sequence of equations:

$$f_b = f_n + \frac{GAMMA.f_s}{4(PHI + V_{SB})^{1/2}} \tag{4.59}$$

$$f_n = DELTA \frac{\pi \varepsilon_{si}}{2 C'_{ox} W_{eff}} \tag{4.60}$$

$$f_s = 1 - \frac{X}{L_{eff}} \left[\frac{LD + w_c}{XJ} \left(1 - \frac{w_p}{XJ + w_p} \right)^{1/2} - \frac{LD}{XJ} \right] \tag{4.61}$$

$$w_p = x_d\sqrt{PHI + V_{SB}} \tag{4.62}$$

$$x_d = \sqrt{\frac{2\varepsilon_{si}}{q.NSUB}} \tag{4.63}$$

$$w_c = XJ\left[0.0631353 + 0.8013929\frac{w_p}{XJ} - 0.0111077\left(\frac{w_p}{XJ}\right)^2\right] \tag{4.64}$$

$$PHI = 2\frac{kT}{q}\ln\left(\frac{NSUB}{n_i}\right) \tag{4.65}$$

$$GAMMA = \frac{\sqrt{2q\varepsilon_{si}NSUB}}{C_{ox}}. \tag{4.66}$$

The effective carrier mobility, μ_{eff}, is defined by

$$\mu_{eff} = \frac{\mu_s}{1 + \frac{v_{de}}{v_c}} \qquad VMAX > 0 \tag{4.67}$$

$$\mu_{eff} = \mu_s \qquad VMAX = 0 \tag{4.68}$$

where $VMAX$ is the maximum drift velocity of carriers and

$$\mu_s = \frac{U0}{1 + THETA.(V_{GS} - V_T)}. \tag{4.69}$$

In equation (4.67), v_c is given by

$$v_c = \frac{VMAX.L_{eff}}{\mu_s}, \tag{4.70}$$

and v_{de} is determined by

$$v_{de} = \min\left(V_{DS}, v_{D(sat)}\right), \tag{4.71}$$

where

$$v_{D(sat)} = v_{sat} + v_c - \left(v_{sat}^2 + v_c^2\right)^{1/2}, \tag{4.72}$$

and

$$v_{sat} = \frac{V_{GS} - V_T}{1 + f_b}. \tag{4.73}$$

In saturation, the drain current is given by

$$I_{D(sat)} = \frac{I_D}{1 - \frac{\Delta L}{L_{eff}}} \tag{4.74}$$

where I_D is calculated from (4.58) and

$$\Delta L = -\frac{ep.x_d^2}{2} + \left[\left(\frac{ep.x_d^2}{2}\right)^2 + KAPPA.x_d^2.\left(V_{DS} - v_{D(sat)}\right)\right]^{1/2}. \tag{4.75}$$

ep is the lateral electric field at the pinch off point given by

$$ep = \frac{v_c\left(v_c + v_{D(sat)}\right)}{L_{eff}.v_{D(sat)}}. \tag{4.76}$$

If the value of ΔL calculated from (4.75) is larger than $L_{eff}/2$, ΔL is modifed to

$$\Delta L = L_{eff} - \frac{(L_{eff}/2)^2}{\Delta L}. \tag{4.77}$$

In the conventional SPICE level 3 model, the subthreshold region is defined as $V_{GS} < V_{on}$ and V_{on} is given by

$$V_{on} = V_T + nV_t. \tag{4.78}$$

The subthreshold slope factor, n, is calculated from

$$n = 1 + \frac{qNFS}{C'_{ox}} + \frac{GAMMA.f_s.\sqrt{PHI + V_{SB}} + f_n(PHI + V_{SB})}{2(PHI + V_{SB})} \tag{4.79}$$

where NFS is the fast surface state density. The subthreshold current is calculated as follows

$$I_{D(sub)} = I_{D0}.\exp\left(\frac{V_{GS} - V_{on}}{nV_t}\right). \tag{4.80}$$

In equation (4.80), I_{D0} is the drain current at the beginning of the subthresh-

old region ($V_{GS} = V_{on}$) calculated from (4.58).

The most important parameter in the new model is the threshold voltage defined by

$$V_T = V_{FB} + PHI + GAMMA.f_s.\sqrt{PHI + V_{SB}} - \sigma V_{DS} + f_n(PHI + V_{SB}) \tag{4.81}$$

where

$$\sigma = \frac{ETA \times 8.15 \times 10^{-22}}{C'_{ox} L^3_{eff}}. \tag{4.82}$$

4.5.2 The Modified SPICE Level 3 Model

In the modified SPICE level 3 model, we keep all the parameters which have been used in the conventional model in order to take advantage of the effects that have been taken into account in this model. The only parameter to be modified in the new model is the threshold voltage (equation (4.81)). The first three terms in equation (4.81) correspond to the first three terms in equation (4.41). To apply the variable threshold technique to the SPICE level 3 model, these three terms can be replaced by the terms in equation (4.41). Thus, the new threshold voltage, $\overline{V_T}$, is defined by

$$\begin{aligned} \overline{V_T} &= V_{FB} + (U_S - \xi)V_t + GAMMA.f_s.\sqrt{U_S V_t} + V_{T(Shift)} \\ &\quad -\sigma V_{DS} + f_n(PHI + V_{SB}). \end{aligned} \tag{4.83}$$

It should be noted that f_s has been added to the third term in equation (4.83) to take into account the effect of the short channel. Also, γ has been replaced by $GAMMA$ to be consistent with the SPICE level 3 terminology.

The calculation of the drain current in the modified SPICE level 3 model can be performed using the following steps:

1. For the specified values of V_{SB} and V_{DS}, calculate n, f_n, x_d, w_p, w_c, f_s, f_b and V_T from their appropriate equations given in Section 4.5.1.

V_T is the conventional value for the threshold voltage calculated from (4.81).

2. For the specified value of V_{GS}, calculate μ_{eff}, v_c, v_{sat}, $v_{D(sat)}$, ep, ΔL, and v_{de} using the conventional value of the threshold voltage V_T. These parameters are required for the variable threshold voltage method calculations. Later these parameters can be calculated again using the modified threshold voltage.

3. Calcuate ξ and $V_{T(Shift)}$ using the procedure described in Section 4.3.2.

4. Calculate the modified threshold voltage from equation (4.83).

5. The parameters calculated in step 2 may be calculated again using the new threshold voltage. The new threshold voltage does not change these parameters significantly. Therefore, this step can be ignored.

6. Calculate the drain current using equation (4.58) when $V_{GS} \geq \overline{V_{on}}$. The drain current in subthreshold where $V_{GS} < \overline{V_{on}}$ is given by

$$I_{D(sub)} = \mu_{eff} C'_{ox} \frac{W_{eff}}{L_{eff}} . \frac{GAMMA.V_t^2}{2\sqrt{PHI + V_{SB}}} . \left(1 - e^{-\frac{V_{DS}}{V_t}}\right) . e^{\frac{V_{GS} - \overline{V_{on}}}{nV_t}} \quad (4.84)$$

where $\overline{V_{on}} = V_T$ given by equation (4.81).

4.6 Simulation and Experimental Results

Figure 4.6 shows the drain current of an NMOS transistor as a function of the gate-bulk voltage for different drain-source voltages. As can be seen, the results of equations (4.37) and (4.38) along with the variable threshold voltage method (equation (4.41)) are in very good agreement with the Pao-Sah and MISNAN model results. However, the SPICE model which is based on a constant threshold voltage introduces large errors around the turn-on region. The drain current calculation error with respect to the gate-bulk voltage using different models is shown in Fig. 4.7. In this plot the Pao-Sah model has been chosen as the accurate reference model.

Figures 4.8 and 4.9 compare the new model results with those of the other

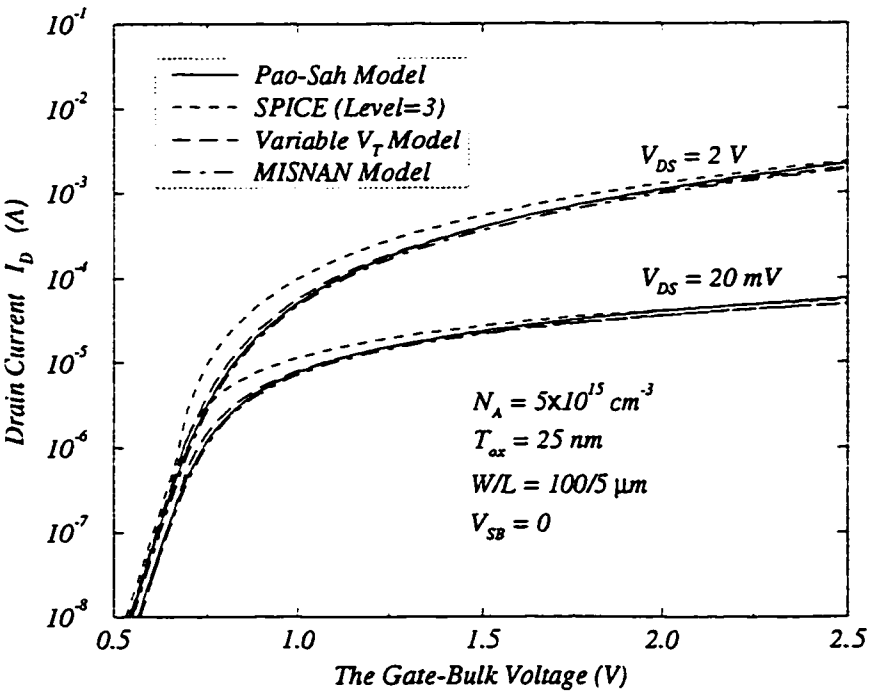

Figure 4.6: Comparison of different models for various drain-source voltages.

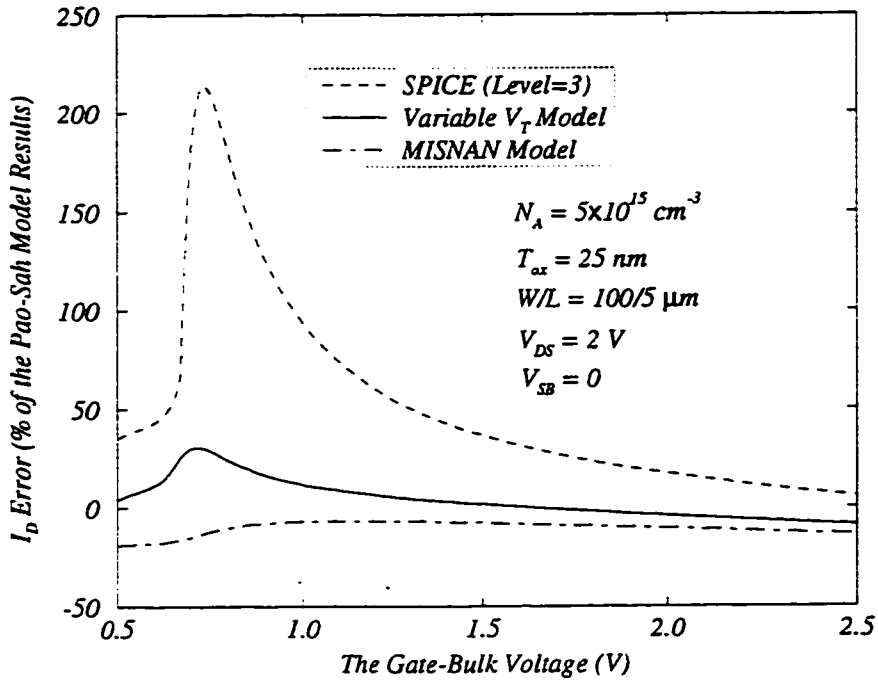

Figure 4.7: Comparison of drain current obtained using various models with that given by the Pao-Sah model.

models for various substrate dopings (N_A) and oxide thickness values (T_{ox}), respectively.

The experimental and the new model results are compared in Figs. 4.10-4.12 using a commercial 0.8 μm BiCMOS process. In this process, $N_A = 3.23 \times 10^{16} cm^{-3}$, $T_{ox} = 17.5nm$ and the SPICE level 3 parameters used for the simulations are $ETA = 1.069$, $THETA = 0.063V^{-1}$, $KAPPA = 8.348V^{-1}$ and $\mu_0 = 502.9cm^2/(V.S)$. As can be seen, the model provides very good results for different terminal voltages in all regions of operation. The experimental data was obtained by accurate measurement of the drain current in a transistor array fabricated in this process.

This model is also less sensitive to the number of iterations for the surface

potential calculation than the MISNAN model. Simulation shows (Fig. 4.13) that at large values of V_{SB} and small values of N_A, the MISNAN model requires more than one iteration to provide a smooth transition between the weak and strong inversion regions.

Figures 4.14 to 4.16 compare the results of the new model with those of the SPICE level 3, BSIM3v3 and experiment. In this simulation, the parameters of a commercial $0.8\mu m$ CMOS process have been used. In this process, $N_A = 1.846 \times 10^{16} cm^{-3}$ and $T_{ox} = 17.7nm$. This was the only available set of parameters with experimental data for the BSIM model. As can be seen, very good agreement has been achieved between the new model and the BSIM3v3 model. The experimental data also verifies the accuracy of both models particularly in the moderate inversion region.

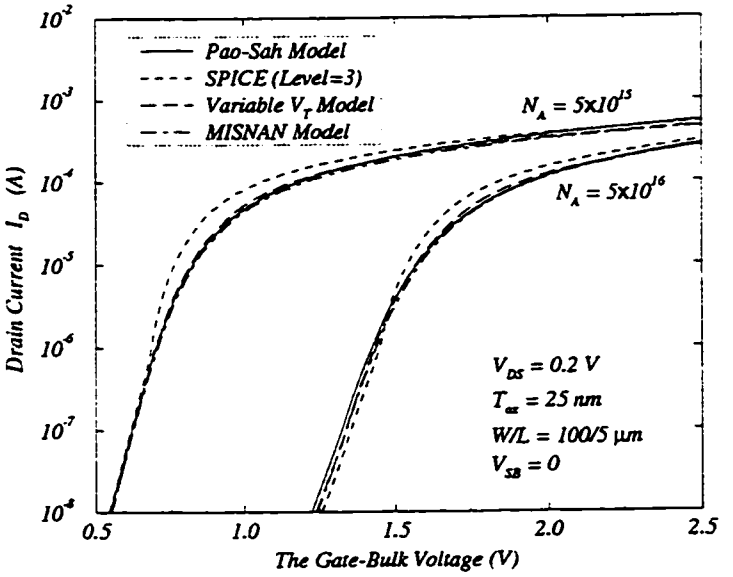

Figure 4.8: Comparison of different models for various substrate dopings.

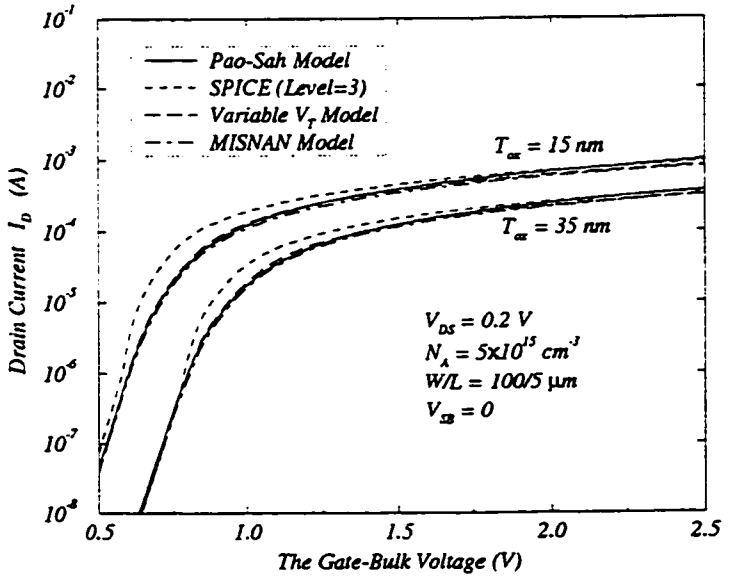

Figure 4.9: Comparison of different models for various oxide thickness values.

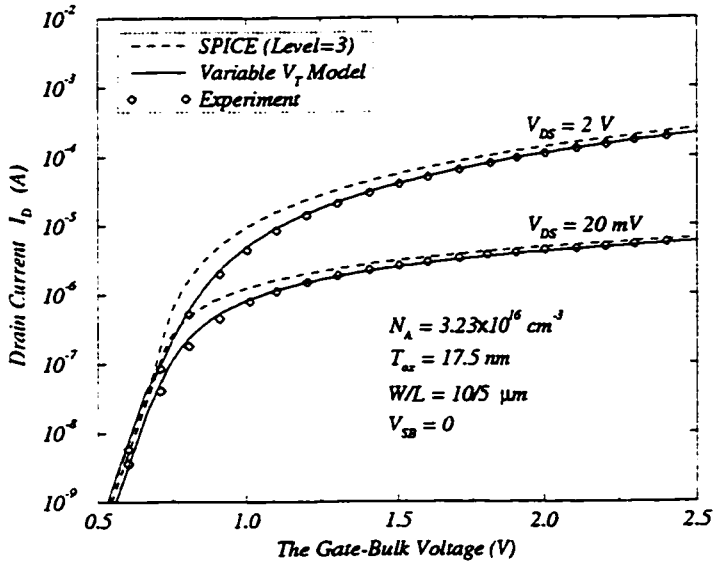

Figure 4.10: Comparison of the experimental and new model results for various drain-source voltages.

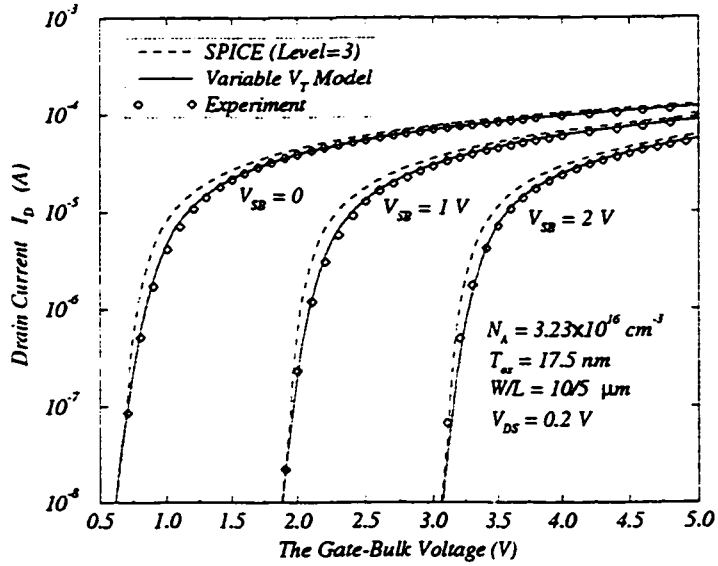

Figure 4.11: Comparison of the experimental and new model results for various source-bulk voltages.

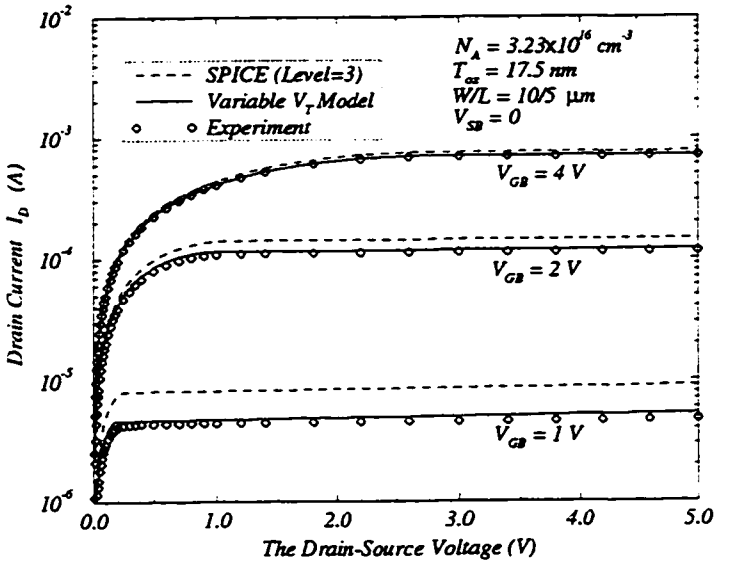

Figure 4.12: $I_D - V_{DS}$ characteristics of a MOS transistor using the variable V_T model.

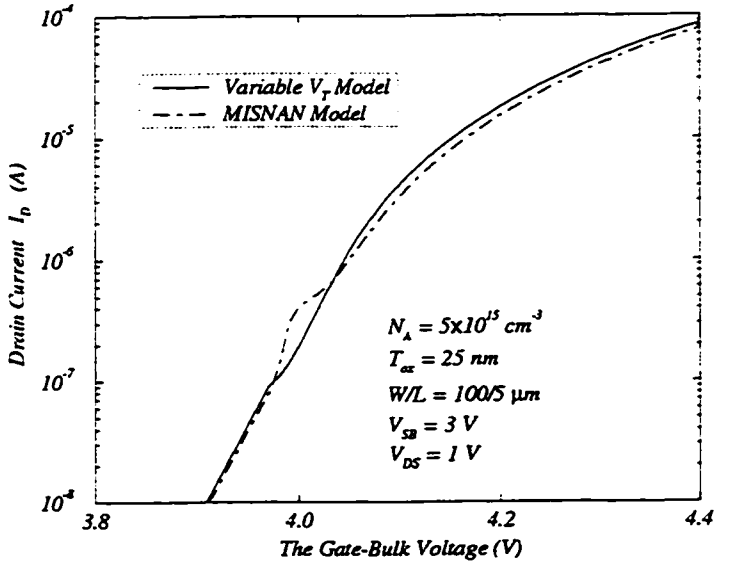

Figure 4.13: Comparison between the new model and MISNAN model when only one iteration is used for the boundary surface potential calculation.

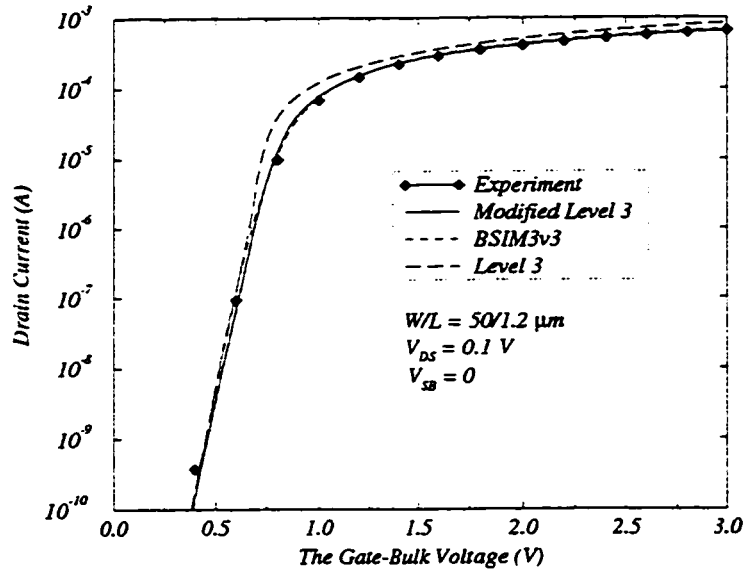

Figure 4.14: Comparison of different models for $V_{DS} = 0.1V$.

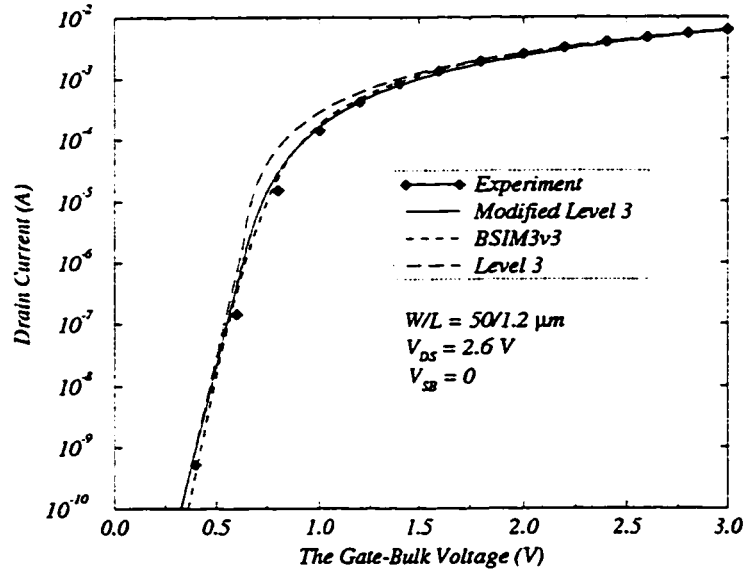

Figure 4.15: Comparison of different models for $V_{DS} = 2.6V$.

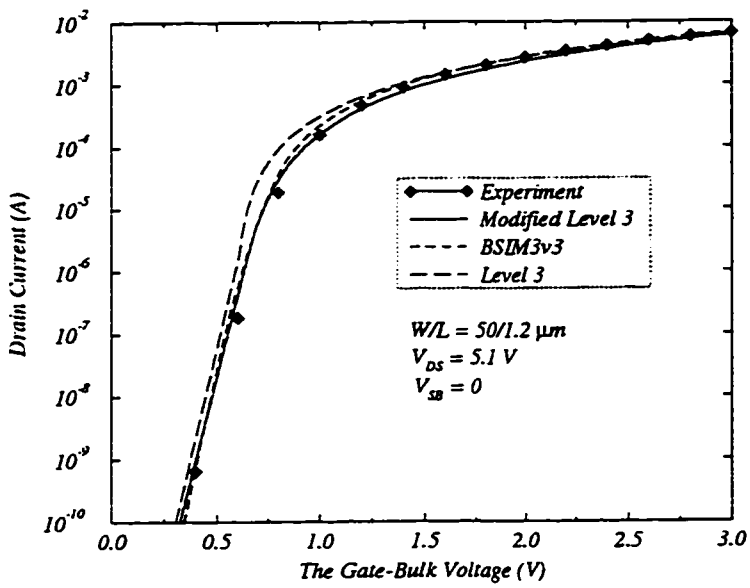

Figure 4.16: Comparison of different models for $V_{DS} = 5.1V$.

4.7 Summary

A new dc model based on the simple piece-wise model for a MOS transistor has been described. The model has a continuous transition between the subthreshold and strong inversion regions and provides accurate results in all regions of operation. The model was compared to the Pao-Sah, MISNAN, BSIM3v3 and SPICE level 3 models. Very good agreement between the new model and Pao-Sah model was achieved in all cases. The agreement between the new model results and experimental data was also illustrated. The advantages of the new model can be summarized as follows:

1. This new model is compatible with SPICE models such as the SPICE level 3 and BSIM models and can be easily incorporated into SPICE programs. Due to this compatibility all other effects such as short channel and saturation effects can be added to the

model by SPICE.

2. For V_{DS} values several times larger than kT/q, only one surface potential calculation is required in the strong inversion region.
3. The surface potential calculation is not required for the subthreshold region.
4. The model is also less sensitive to the number of iterations in the surface potential calculation.

Therefore, due to the advantages in terms of the surface potential calculation, this model is computationally more efficient than the MISNAN model while providing accurate results. Because of its compatibility with SPICE models, the new model can easily be incorporated into SPICE programs by modifying only the threshold voltage calculation procedure.

Chapter 5

Moderate Inversion Modeling in MOS Analog Switches

The simple Sheu and Hu's model and its modified model presented in Chapters 2 and 3, respectively, both utilize a simple MOS transistor model for the analog switch. This piece-wise model is based on a constant threshold voltage with quadratic and exponential equations in the strong and weak inversion regions, respectively. Although this model is simple and computationally efficient, it introduces large errors into the drain current calculation in the moderate inversion region where the gate-source voltage approaches the threshold voltage. Error in the drain current calculation can cause significant error in the final charge injection error prediction.

This chapter presents a new charge injection error analysis using the accurate dc model discussed in Chapter 4 for the MOS transistor in the moderate inversion region. The importance of accurate drain current modeling in the final error calculation is studied. It is shown that this effect is less significant at very low and very high gate voltage falling rates.

5.1 Introduction

The analysis in this chapter focuses on the special case of switch charge injection where the input source resistance and capacitance are small (Fig. 2.2(a)). This analysis will be extended to the general case in Chapter 6. Also, since the charge injection error occurs during the turn-off transient, the analysis is only performed during this period of time. The behavior of the switch during this transient is studied here by developing a new analysis.

Section 5.2 explains the moderate inversion current effect in charge injection error analysis. The charge injection error equations using the accurate MOS dc model are derived in Section 5.3. Simulation and experimental results are discussed in Section 5.4. A summary is given in Section 5.5.

5.2 Moderate Inversion Effect on Charge Injection Error

The accuracy of the transistor model is not critical for the prediction of the output voltage at the end of the turn-on transient. This is because the output voltage finally reaches the input voltage in the sampling state. However, during the turn-off transient, an accurate prediction of the sampled voltage depends on the accuracy of the drain current calculation. During the turn-off transient, the drain current cancels part of the injected charge into the output node and decreases the final charge injection error. Therefore, an accurate dc model for all regions of operation including the moderate inversion region is important in the analysis of the charge injection error in analog switching circuits.

In the literature, the computationally efficient charge injection error analyses [16] are based on a simple quadratic equation for the MOS transistor [24]. However, this model introduces large errors into the drain current calcula-

tion in the moderate inversion region [24,25]. It will be shown in Section 5.4 that this simple model underestimates the final charge injection error due the high drain current prediction in the moderate inversion region. The error in the charge injection prediction can be significant depending on the switch transistor size, load capacitance, process parameters and transistor terminal voltages.

5.3 The Charge Injection Error Equations

As discussed in Section 2.2, in the simple model developed by Sheu and Hu [7], the output error voltage ($v_o = V_o - V_{in}$) due to charge injection is described by

$$C_L \frac{dv_o}{dt} = \begin{cases} -i_d - (\frac{C_{ox}}{2} + C_{ol})U & V_{GS} \geq V_{on} \\ -(\frac{C_{ox}}{2} + C_{ol})U & V_{GS} < V_{on} \end{cases} \tag{5.1}$$

where C_L is the hold capacitance, C_{ox} is the gate-oxide capacitance, C_{ol} is the gate overlap capacitance, U is the gate voltage falling rate, V_{on} is the transistor turn-on voltage and i_d is the channel current when $V_{GS} \geq V_{on}$.

In order to take into account second order effects such as the subthreshold current and gate-source capacitance (C_{gs}) variations, following the method developed in Chapter 3, (5.1) can be modified to [16]

$$C_L \frac{dv_o}{dt} = \begin{cases} -i_d - (C_{gs} + C_{ol})U & V_{GS} \geq V_{on} \\ -i_{d(sub)} - (C_{gs} + C_{ol})U & V_{GS} < V_{on} \end{cases} \tag{5.2}$$

where $i_{d(sub)}$ is the subthreshold current and

$$C_{gs} = \begin{cases} \frac{C_{ox}}{2} - (\frac{C_{ox}}{2} - C_{gsm}) .e^{-\frac{V_{GS}-V_{on}}{kV_t}} & V_{GS} \geq V_{on} \\ C_{gsm}.e^{\frac{V_{GS}-V_{on}}{nV_t}} & V_{GS} < V_{on} \end{cases} . \tag{5.3}$$

C_{gsm} is the gate-source capacitance when $V_{GS} = V_{on}$ [16], n is the subthreshold slope factor, V_t is the thermal voltage (kT/q), β is the transistor conductance coefficient ($\mu C'_{ox}\frac{W}{L}$) and k is a fitting factor.

In the model, the conventional quadratic equation for MOS transistors is used to model the channel current, i_d, where

$$i_d = \beta\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]. \tag{5.4}$$

To simplify the analysis, the second term in (5.4) is usually ignored for the small output error voltages. This increases the inherent inaccuracy of (5.4) in moderate inversion.

In this new analysis, equation (5.2) along with the modified version of the SPICE level 3 model (equations (4.37) and (4.38)) are used to calculate the charge injection error. Equation (5.2) can be solved using numerical methods. At each time step, the MOS transistor threshold voltage is adjusted corresponding to the terminal voltages.

The model proposed in this section takes into account the subthreshold current effect and gate-source capacitance variation effect and also utilizes an accurate model for the MOS transistor drain current calculation in all regions of operation including the moderate inversion region.

5.4 Simulation and Experimental Results

5.4.1 Simulation Results

The results of the charge injection error analysis using both the modified SPICE model and the SPICE level 3 model are shown in Fig. 5.1. The percentage of the error due to the inaccuracy of the moderate inversion current in the SPICE level 3 model has been plotted in Fig. 5.2. The model parameters of a commercial 1.5-μm CMOS process were chosen as the simulation

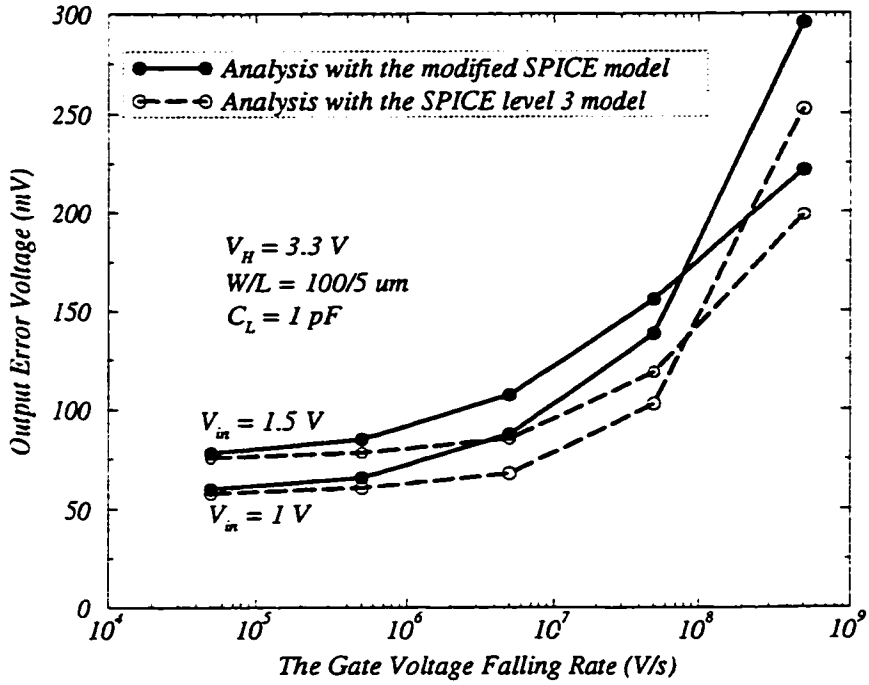

Figure 5.1: The effect of accurate modeling in the moderate inversion region for different input voltages (V_{in}).

parameters where $N_A = 1.345 \times 10^{16}\ cm^{-3}$, $T_{ox} = 26.7nm$, $V_{T0} = 0.8204\ V$ and the gate overlap capacitance is 2.716×10^{-12} farads per transistor width (cm). As can be seen, the error in the charge injection error prediction can be as high as 25% if an accurate model for the moderate inversion current is not used. This error decreases at higher input voltages where the channel current effect is generally less important. The moderate inversion consideration is also less significant at high and low gate voltage falling rates (see Fig. 5.2). At high falling rates, the channel charges contribution to the final error is dominant. At low falling rates, most of the channel charges return to the source. This reduces the output error voltage and as a result the drain-source voltage. The lower the channel current at small drain-source voltages, the lower the effect of this current on the final output error.

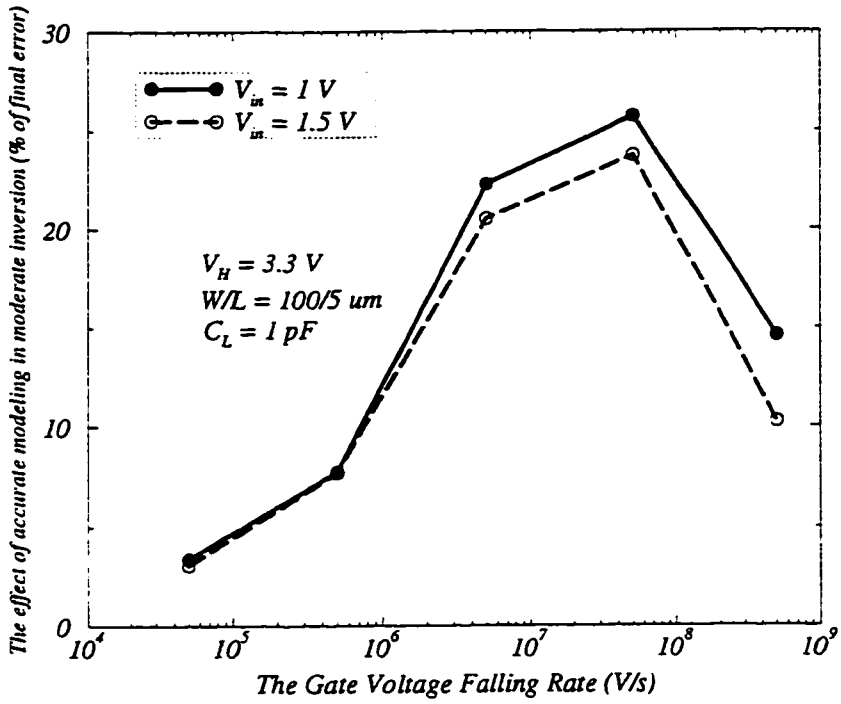

Figure 5.2: The effect of accurate modeling in the moderate inversion region for different input voltages (V_{in}) as a percentage of the final charge injection error.

5.4.2 Experimental Results

Figure 5.3 shows an on-chip test circuit for measuring charge injection error. This circuit consists of an NMOS switch transistor, a load capacitance (C_L) and a buffer. The buffer is realized using a single-stage cascode operational amplifier in unity-gain feedback and has a linear transfer characteristic for input voltages between 1 and 2.5 volts [13, 35]. In this range, the amplifier output represents the voltage at the load capacitance node with reasonable accuracy. A chip containing four versions of the circuit in Fig. 5.3 for different load capacitance sizes was designed and fabricated in 1.5μm CMOS P-well technology. The layout of the chip is shown in Fig. 5.4.

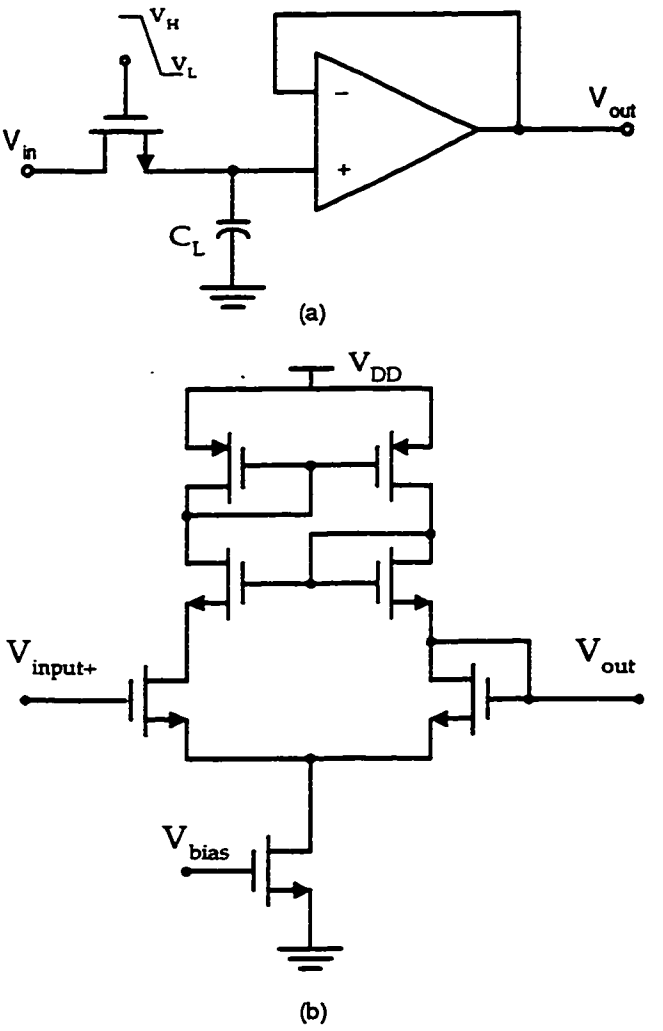

Figure 5.3: (a) On-chip test circuit for the charge injection error measurement, (b) Schematic of the opamp.

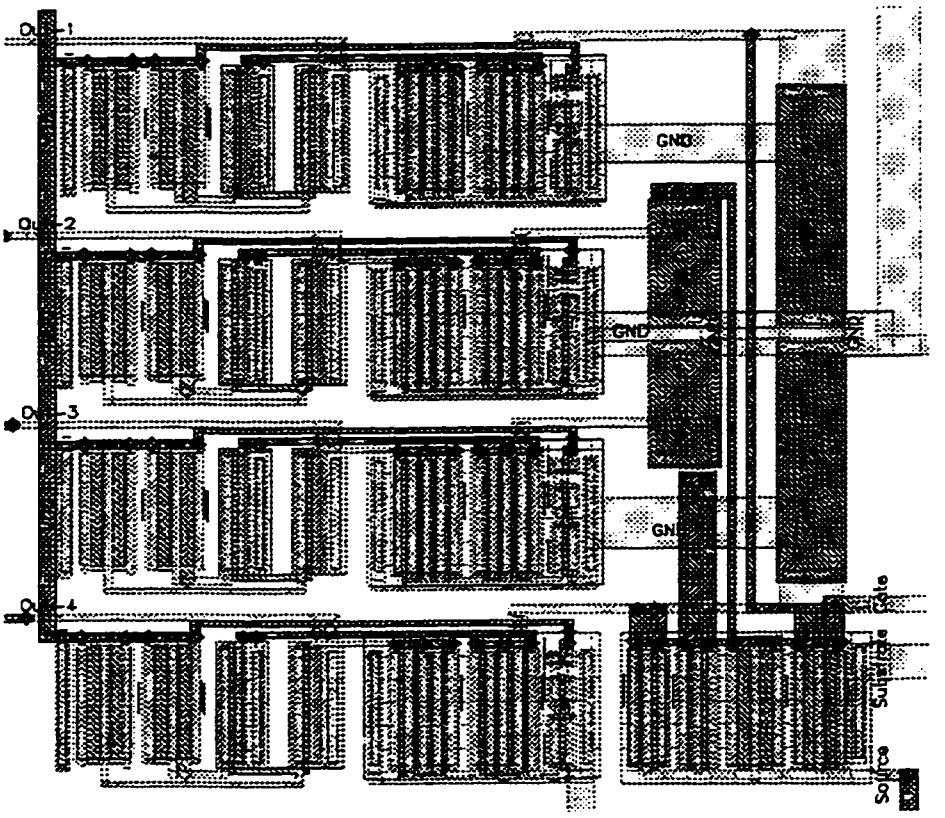

Figure 5.4: The layout of the test circuit.

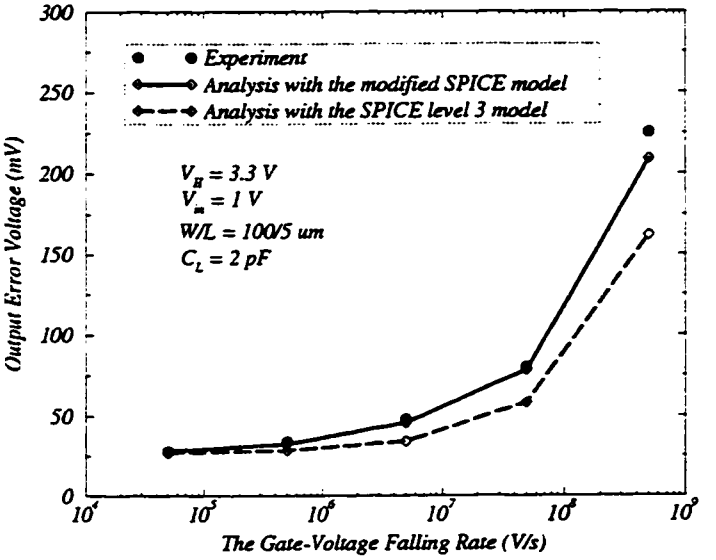

Figure 5.5: Comparison of the experimental data and simulation using different models for $C_L = 2pF$.

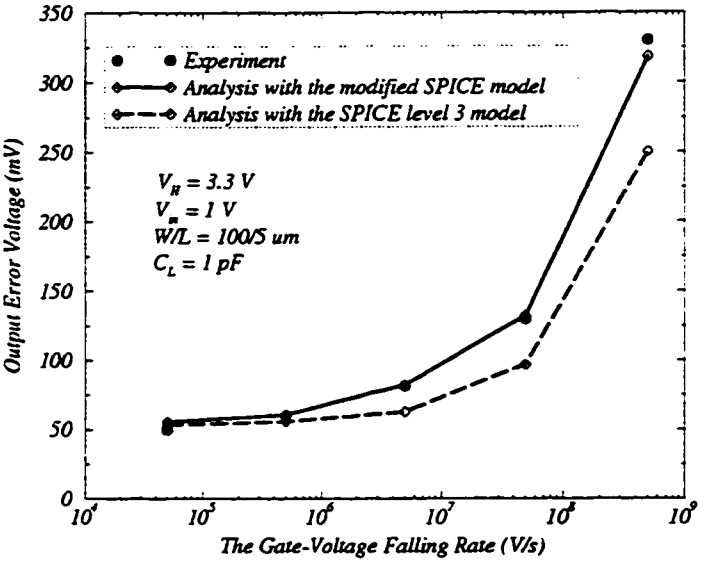

Figure 5.6: Comparison of the experimental data and simulation using different models for $C_L = 1pF$.

The comparison of the experimental data and simulation results using the modified SPICE model and the SPICE level 3 model is shown in Figs. 5.5 and 5.6 for $C_L = 1pF$ and $C_L = 2pF$, respectively. As can be seen, there is excellent agreement between experiment and simulation with the modified SPICE model over a wide range of gate voltage falling rates. The discrepancy between the experimental data and the simulation results using the SPICE level 3 model is due to the inaccuracy in moderate inversion modeling. The overestimation of the drain current by the SPICE level 3 model in the moderate inversion region gives rise to the inaccuracy in the prediction of the final charge injection error.

5.5 Summary

A new charge injection error analysis using an accurate switch transistor model has been described. The subthreshold effects were also taken into account. The effect of the moderate inversion current on the final charge injection error calculation was discussed. The results of this analysis were compared to those of the analysis with the SPICE level 3 model and experimental data. Excellent agreement between the new analysis results and experimental measurements was achieved. It was shown that an inaccurate transistor model can cause error in the final charge injection error prediction. The magnitude of this error depends on the transistor size, load capacitance, process parameters and transistor terminal voltages. This error is particularly important at moderate gate voltage falling rates.

Chapter 6

Comprehensive Analysis of the Charge Injection Problem

In previous chapters, the importance of adding second order effects into the switch charge injection error analysis was discussed. The most important second order effects such as the transistor subthreshold current, gate-source capacitance variations and accuracy of the drain current in the moderate inversion region were also explained. In addition, appropriate modelling techniques were developed to take these effects into account.

In this chapter, a comprehensive model based on the simple model described in Section 2.6 is proposed. The model is capable of accurately predicting the switch charge injection error in the general case, where both source resistance and capacitance are present, by taking into account second order effects. To numerically solve the differential equations, the Transmission Line Matrix (TLM) method is used. The TLM technique is a computationally efficient method for solving ordinary differential equations [36–39]. Using this method reduces the computation time by a significant factor.

The comprehensive charge injection model is developed in Section 6.1. Section 6.2 is devoted to introducing the TLM method. The TLM repre-

sentation of the charge injection error problem is given in Section 6.3. The simulation results, which show the effects of the most important parameters involved with charge injection error, are discussed in Section 6.4. A summary is given in Section 6.5.

6.1 Comprehensive Charge Injection Model

In Section 2.6, equations (2.30) and (2.31) were derived for the general case of switch charge injection error shown in Fig. 2.1. It can be easily shown that under the practical conditions $|dV_G/dt| \gg |dv_d/dt|$ and $|dv_s/dt|$, these equations can be simplified to

$$C_L\frac{dv_d}{dt} = -i_d - \left(C_{ol} + \frac{C_{ox}}{2}\right)U \tag{6.1}$$

$$\frac{v_s}{R_S} + C_S\frac{dv_s}{dt} = i_d - \left(C_{ol} + \frac{C_{ox}}{2}\right)U, \tag{6.2}$$

where the switch transistor is in strong inversion ($V_G \geq V_S + V_T$) and to

$$C_L\frac{dv_d}{dt} = -C_{ol}U \tag{6.3}$$

$$\frac{v_s}{R_S} + C_S\frac{dv_s}{dt} = -C_{ol}U, \tag{6.4}$$

where the switch transistor operates below threshold ($V_G < V_S + V_T$).

6.1.1 Adding the Subthreshold Current

To add the subthreshold current into the model, the drain current model explained in Section 3.2.1 can be used. This model predicts the following drain currents above and below the threshold voltage:

$$i_d = \begin{cases} \beta\left(V_{GS} - V_T\right)V_{DS} & V_{DS} < V'_{DS}, V_{GS} \geq V_{on} \\ \beta n V_t V_{DS} e^{\frac{V_{GS}-V_{on}}{nV_t}} & V_{GS} < V_{on} \end{cases} \tag{6.5}$$

where V_{on} is the modified threshold voltage given by equation (3.5).

Using this model in equations (6.1) to (6.4), the charge injection error differential equations to be solved in the presence of the subthreshold current are

$$C_L\frac{dv_d}{dt} = -\beta\left(V_{GS}-V_T\right)\left(v_d-v_s\right)-\left(C_{ol}+\frac{C_{ox}}{2}\right)U \quad (6.6)$$

$$\frac{v_s}{R_S}+C_S\frac{dv_s}{dt} = \beta\left(V_{GS}-V_T\right)\left(v_d-v_s\right)-\left(C_{ol}+\frac{C_{ox}}{2}\right)U \quad (6.7)$$

for $V_G \geq V_S + V_T$ and

$$C_L\frac{dv_d}{dt} = -\beta n V_t\left(v_d-v_s\right)e^{\frac{V_{GS}-V_{on}}{nV_t}}-C_{ol}U \quad (6.8)$$

$$\frac{v_s}{R_S}+C_S\frac{dv_s}{dt} = \beta n V_t\left(v_d-v_s\right)e^{\frac{V_{GS}-V_{on}}{nV_t}}-C_{ol}U \quad (6.9)$$

for $V_G < V_S + V_T$.

6.1.2 Adding the Gate-Source Capacitance Variations

The gate-source capacitance model developed in Section 3.2.2 can be used to include the gate-source capacitance variation effect into the equations (6.8) and (6.9). The final equations are given by

$$C_L\frac{dv_d}{dt} = -\beta\left(V_{GS}-V_T\right)\left(v_d-v_s\right)-\left(C_{ol}+C_{gs}\right)U \quad (6.10)$$

$$\frac{v_s}{R_S}+C_S\frac{dv_s}{dt} = \beta\left(V_{GS}-V_T\right)\left(v_d-v_s\right)-\left(C_{ol}+C_{gs}\right)U, \quad (6.11)$$

where $V_G \geq V_S + V_T$ and

$$C_L\frac{dv_d}{dt} = -\beta n V_t\left(v_d-v_s\right)e^{\frac{V_{GS}-V_{on}}{nV_t}}-\left(C_{ol}+C_{gs}\right)U \quad (6.12)$$

$$\frac{v_s}{R_S}+C_S\frac{dv_s}{dt} = \beta n V_t\left(v_d-v_s\right)e^{\frac{V_{GS}-V_{on}}{nV_t}}-\left(C_{ol}+C_{gs}\right)U \quad (6.13)$$

where $V_G < V_S + V_T$. In these equations, C_{gs} is given by equation (3.9).

This C_{gs} model introduces a smooth transition from $\frac{C_{ox}}{2}$ to zero for the gate-source capacitance compared to an abrupt change from $\frac{C_{ox}}{2}$ to zero proposed in the simple Sheu and Hu's model. In the new model, the non-zero value of C_{gs} below threshold represents the weak inversion channel charges which contribute to the final error. However, the new model predicts a smaller value of C_{gs} in strong inversion compared to $\frac{C_{ox}}{2}$ in the simple model, especially near the threshold voltage. This reduction in C_{gs} introduces less charge injection in strong inversion. Therefore, adding the new gate-source capacitance model can increase or decrease the final error depending on the other electrical and process parameters.

6.1.3 Using an Accurate Drain Current Model in Moderate Inversion

In order to improve the accuracy of the proposed charge injection model, the accurate transistor dc model developed in Chapter 4 can be used to calculate the channel current during the switching transient. In this case, the charge injection error equations can be simply written as follows

$$C_L \frac{dv_d}{dt} = -I_d - (C_{ol} + C_{gs})\,U \tag{6.14}$$

$$\frac{v_s}{R_S} + C_S \frac{dv_s}{dt} = I_d - (C_{ol} + C_{gs})\,U, \tag{6.15}$$

where I_d can be calculated from (4.37) and (4.38) at each time step of the numerical integration of equations (6.14) and (6.15). Also, the appropriate value of C_{gs} can be calculated from (3.9) depending on the terminal voltages at each time step. Since equation (4.37) also gives the drain current in the saturation region, the condition where v_d and v_s have to be small in order that the switch transistor remains in the triode region is not required in the

new model.

Equations (6.14) and (6.15) along with the new models for I_d and C_{gs} provide an accurate model for the prediction of the final charge injection error for the general switching circuit case.

6.2 The Transmission Line Matrix Method

Solving differential equations (6.14) and (6.15) requires numerical calculation. There are different numerical methods for solving a set of ordinary differential equations such as Runge-Kutta, Adams-Bashforth and Adams-Moulton method. The well known Runge-Kutta method was initially chosen in this work to solve the switch charge injection differential equations. To implement this technique, the optimized function embedded in MATLAB was used. This method was found to be computationally very inefficient particularly at low gate voltage falling rates. Therefore, it was not practical to use this method for a wide range of electrical and process parameters.

In order to reduce the computation time while preserving the accuracy of the final answer, the Transmission Line Matrix (TLM) method was chosen for solving the switch charge injection differential equations. The TLM method is one of the most recent developments in numerical methods and was first introduced by Johns and Beurle [36] to solve time-space scattering problems. This method was first used to solve ordinary differential equations (ODE) by Saleh [37] using his multi-compartment (MC-TLM) model. It was also extended to give a general solution to arbitrary order, nonlinear ODE's with variable coefficients [38]. This technique uses a constant time step which must be found by using some dummy runs. Since preliminary testing to find the appropriate value of step size is time consuming, an automatic time-stepping technique was added to the MC-TLM method (see Appendix C). This technique provides an adaptive step size capability which is based on

estimation of the error of the answer at each time step [39].

Using this method, a general purpose simulator was developed which is capable of solving different sets of equations including the switch charge injection problem. A user interface was also developed in MATLAB particularly for the charge injection problem. The results in Section 6.4 have been generated using this simulator.

6.3 The TLM Representation of the Charge Injection Problem

Equations (6.14) and (6.15) have three different forms depending on the terminal voltages which determine the operation region of the switch transistor. The TLM representation of each case is given in this section.

6.3.1 The Switch Transistor in Saturation

In the case with the transistor in saturation, equations (6.14) and (6.15) can be written as follows

$$\frac{dv_d}{dt} = -\beta\frac{(V_{GS}-\overline{V_T})^2}{2(1+\delta)C_L} - (C_{ol}+C_{gs})\frac{U}{C_L} \tag{6.16}$$

$$\frac{dv_s}{dt} = \beta\frac{(V_{GS}-\overline{V_T})^2}{2(1+\delta)C_S} - \frac{v_s}{R_S C_S} - (C_{ol}+C_{gs})\frac{U}{C_S}, \tag{6.17}$$

where C_{gs} is given by (3.9). Following the method described in Appendix C, the TLM representation of equations (6.16) and (6.17) can be summarized as shown in Table 6.1.

	v_d	v_s
d_1	0	$\frac{1}{R_S C_S}$
d_2	0	0
g_1	$\beta\frac{(V_{GS}-\overline{V_T})^2}{2(1+\delta)C_L}$	$\beta\frac{(V_{GS}-\overline{V_T})^2}{2(1+\delta)C_S}$
g_2	$-(C_{ol}+C_{gs})\frac{U}{C_L}$	$-(C_{ol}+C_{gs})\frac{U}{C_S}$
V_1	-1	1
V_2	1	1

Table 6.1: The TLM representation of the charge injection problem when the switch transistor is in saturation.

6.3.2 The Switch Transistor in Triode

When the switch transistor operates in the triode region, equations (6.14) and (6.15) result in the following equations.

$$\frac{dv_d}{dt} = -\frac{\beta}{C_L}\left[V_{GS} - \overline{V_T} - \frac{(v_d - v_s)}{2(1+\delta)}\right](v_d - v_s) - (C_{ol} + C_{gs})\frac{U}{C_L} \tag{6.18}$$

$$\frac{dv_s}{dt} = \frac{\beta}{C_S}\left[V_{GS} - \overline{V_T} - \frac{(v_d - v_s)}{2(1+\delta)}\right](v_d - v_s) - \frac{v_s}{R_S C_S} - (C_{ol} + C_{gs})\frac{U}{C_S}. \tag{6.19}$$

Table 6.2 summarizes the TLM representation of these equations.

	v_d	v_s
d_1	$\frac{\beta}{C_L}\left[V_{GS} - \overline{V_T} - \frac{(v_d-v_s)}{2(1+\delta)}\right]$	$\frac{\beta}{C_S}\left[V_{GS} - \overline{V_T} - \frac{(v_d-v_s)}{2(1+\delta)}\right] + \frac{1}{R_S C_S}$
d_2	0	0
g_1	$\frac{\beta}{C_L}\left[V_{GS} - \overline{V_T} - \frac{(v_d-v_s)}{2(1+\delta)}\right]$	$\frac{\beta}{C_S}\left[V_{GS} - \overline{V_T} - \frac{(v_d-v_s)}{2(1+\delta)}\right]$
g_2	$-(C_{ol}+C_{gs})\frac{U}{C_L}$	$-(C_{ol}+C_{gs})\frac{U}{C_S}$
V_1	$-v_s$	v_d
V_2	1	1

Table 6.2: The TLM representation of the charge injection problem when the switch transistor is in triode.

6.3.3 The Switch Transistor in Subthreshold

In the case where the switch transistor is in the subthreshold region, equations (6.14) and (6.15) are reduced to

$$\frac{dv_d}{dt} = -\frac{\beta\gamma V_t^2}{2C_L\sqrt{\phi_B + V_{SB}}}\left(1 - e^{-\frac{v_d - v_s}{V_t}}\right) e^{\frac{V_{GS} - \overline{V_{on}}}{nV_t}} - (C_{ol} + C_{gs})\frac{U}{C_L} \quad (6.20)$$

$$\frac{dv_s}{dt} = \frac{\beta\gamma V_t^2}{2C_S\sqrt{\phi_B + V_{SB}}}\left(1 - e^{-\frac{v_d - v_s}{V_t}}\right) e^{\frac{V_{GS} - \overline{V_{on}}}{nV_t}} - \frac{v_s}{R_S C_S} - (C_{ol} + C_{gs})\frac{U}{C_S}. \quad (6.21)$$

The TLM representation of these equations is given in Table 6.3.

	v_d	v_s
d_1	0	$\frac{1}{R_S C_S}$
d_2	0	0
g_1	$\frac{\beta\gamma V_t^2}{2C_L\sqrt{\phi_B - V_{SB}}}\left(1 - e^{-\frac{v_d - v_s}{V_t}}\right) e^{\frac{V_{GS} - \overline{V_{on}}}{nV_t}}$	$\frac{\beta\gamma V_t^2}{2C_S\sqrt{\phi_B + V_{SB}}}\left(1 - e^{-\frac{v_d - v_s}{V_t}}\right) e^{\frac{V_{GS} - \overline{V_{on}}}{nV_t}}$
g_2	$-(C_{ol} + C_{gs})\frac{U}{C_L}$	$-(C_{ol} + C_{gs})\frac{U}{C_S}$
V_1	-1	1
V_2	1	1

Table 6.3: The TLM representation of the charge injection problem when the switch transistor is in subthreshold.

6.4 Simulation Results

The simulation results of the new charge injection model developed in this chapter are presented in this section. These results cover the effects of the important parameters under different terminal voltage conditions.

In this section, the model paramteters of a commertial CMOS $1.5\mu m$ process were chosen as the simulation parameters unless otherwise specified. In this process $N_A = 1.405 \times 10^{16} cm^{-3}$, $T_{ox} = 26.17nm$, $V_{T0} = 0.8486V$, $\mu = 526.7 cm^2/V.s$ and the gate overlap capacitance is 2.771×10^{-12} farads per transistor width (cm). In all the figures shown in this section, the contri-

bution of the parameters have been calculated based on the following equation

$$\% \text{ Contribution} = \frac{\text{Result without the effect} - \text{Result with the effect}}{\text{Result with the effect}} \times 100\%.$$

6.4.1 Subthreshold Current and Gate-Source Capacitance Variation Effects

Figure 6.1 shows the subthreshold current (I_{sub}) and gate-source capacitance (C_{gs}) variation effects with respect to the input source resistance (R_S) for two load capacitance values. At large R_S values where the input source time constant ($R_S C_S$) is large compared to the gate voltage fall time (V_H/U),

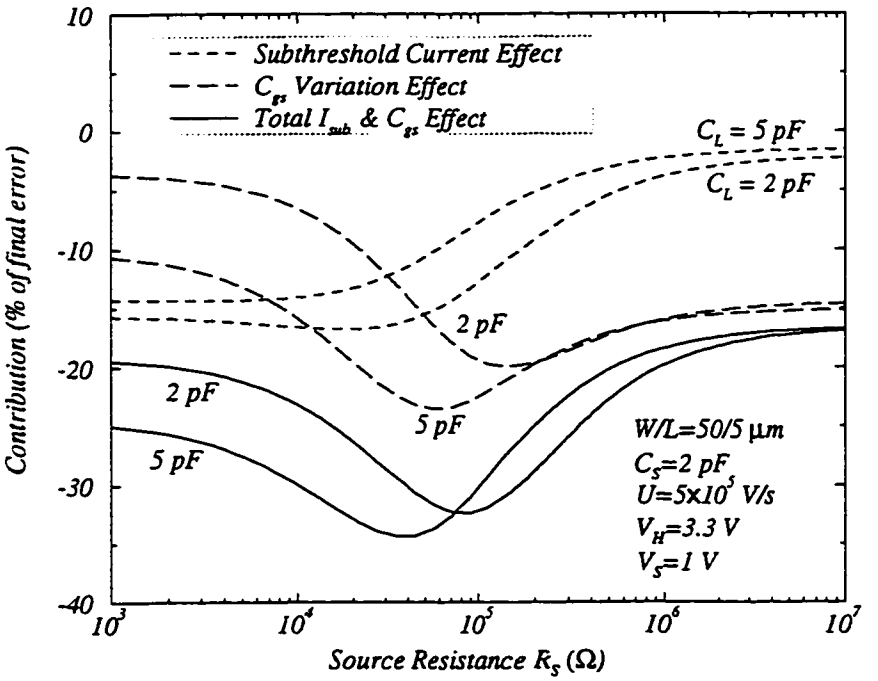

Figure 6.1: The subthreshold current and gate-source capacitance variation effects with respect to the input source resistance for two different load capacitance values.

the input source, V_S, cannot compensate the charge injection to the input node and recharge this node to V_S (node B in Fig. 2.1) fast enough. Therefore, the voltages at both output and input nodes (nodes A and B) are reduced, which in turn reduces the drain-source voltage and as a result the channel current is reduced. This causes the subthreshold current to be less important at large values of R_S. Also, because of the lower charge communication between the input and output (smaller channel current) at high R_S values, the C_{gs} variation effect saturates at a value corresponding to the difference between the charge injection predicted by the simple and accurate C_{gs} models. The total effect is more significant where the time constant R_SC_S and the gate voltage fall time values are close ($R_SC_S \approx V_H/U$). The negative value indicates that the effect tends to reduce the error from the value predicted by the simple model.

I_{sub} and C_{gs} variation effects with respect to the gate voltage falling rate for different R_S values are shown in Fig. 6.2. As can be seen, the subthreshold current is more important at low gate voltage falling rates. At low falling rates, when the gate voltage fall time is larger than the time constant R_SC_S, the input source has enough time to compensate the charge injected to the input node (node B). This causes more voltage to be developed across the transistor drain-source terminals. This in turn increases the channel current including the subthreshold current. The C_{gs} variation does not have a significant effect at low gate voltage falling rate where most of the channel charges injected by the gate-source capacitance in strong inversion are compensated by the channel current. The total effect is more important when the time constant R_SC_S is close to the gate voltage fall time V_H/U. Therefore, the maximum total effect occurs at lower gate falling rates as the source resistance increases.

The percentage of the I_{sub} and C_{gs} variation effects as a function of the input source voltage are illustrated in Fig. 6.3. As can be seen, at high

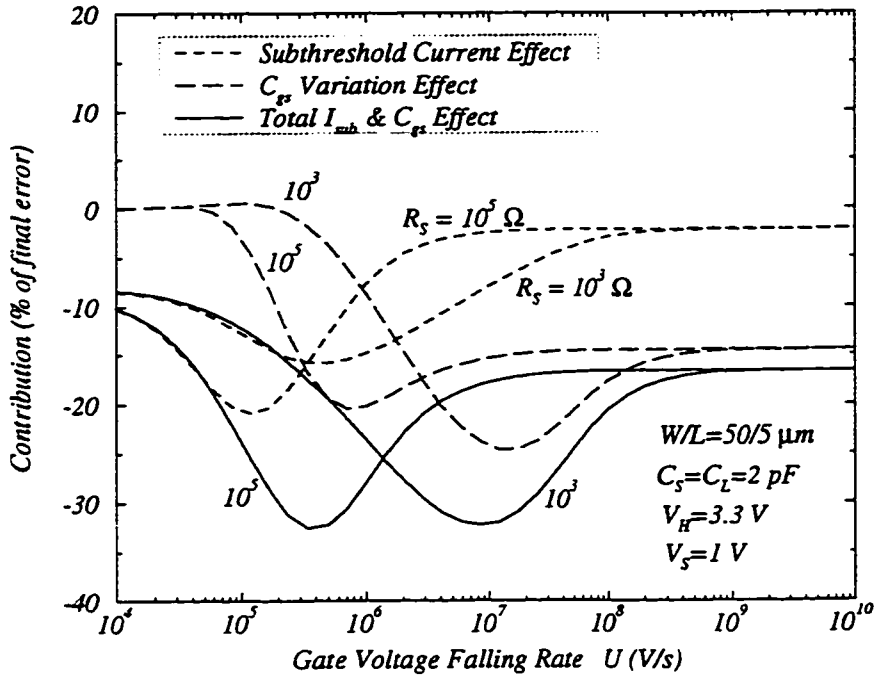

Figure 6.2: The percentage of I_{sub} and C_{gs} variation effects as a function of the gate voltage falling rate for two different source resistance values.

input source voltages where the switch transistor is mostly in the turn-off region, both effects approach zero. The most important effects occur where the transistor is already in moderate inversion at high gate voltage (V_H).

Figure 6.4 shows the total subthreshold current and C_{gs} variation effects with respect to the dimensionless quantity $(V_H - V_T)\sqrt{\frac{\beta}{UC_L}}$ for different C_S/C_L values. In this case, a very large value has been chosen for the source resistance. Therefore, the transistor switch is connected between two capacitors C_S and C_L. This figure also confirms that second order effects are less important where the ratio between the input and output capacitance is close to unity.

The percentage of the I_{sub} and the new C_{gs} model effects with respect

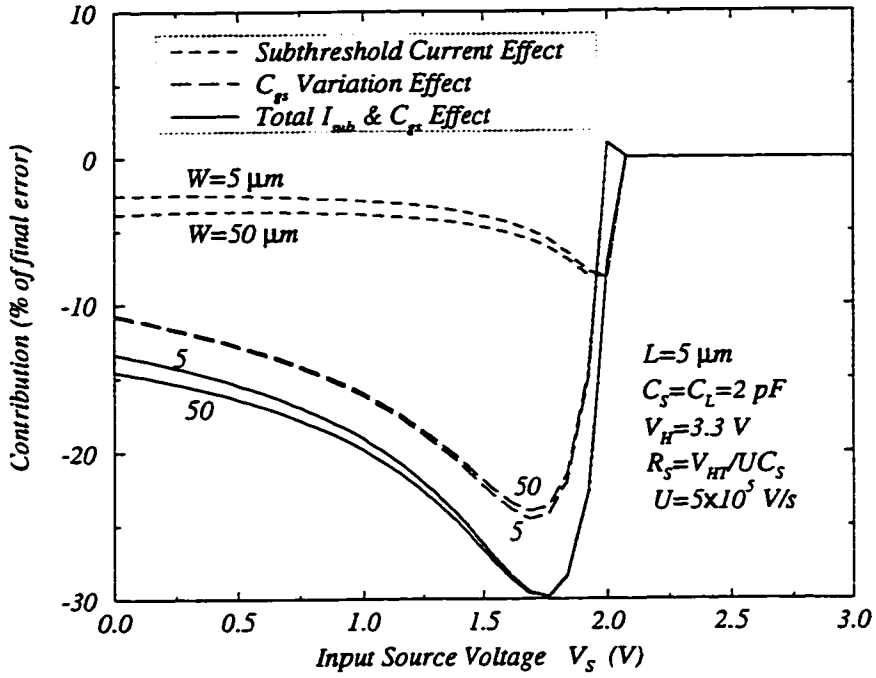

Figure 6.3: The percentage of I_{sub} and C_{gs} variation effects as a function of the input source voltage for two different channel width values.

to the dimensionless quantity $(V_H - V_T)\sqrt{\frac{\beta}{UC_L}}$ for various C_S/C_L values are shown in Figs. 6.5 and 6.6. In these figures, R_S is finite with a value of $\frac{V_{HT}}{UC_S}$ and $\frac{V_{HT}}{5UC_S}$ in Figures 6.5 and 6.6, respectively. In other words, the source resistance at each point in Fig. 6.6 is five times smaller than the one at the same point in Fig. 6.5. As can be seen, the percentage of total effect varies significantly at large values of C_S/C_L. However, this variation does not change much with the source resistance at high C_S/C_L values. On the other hand, at C_S/C_L values closer to unity the variation of I_{sub} and C_{gs} effects change significantly with R_S value.

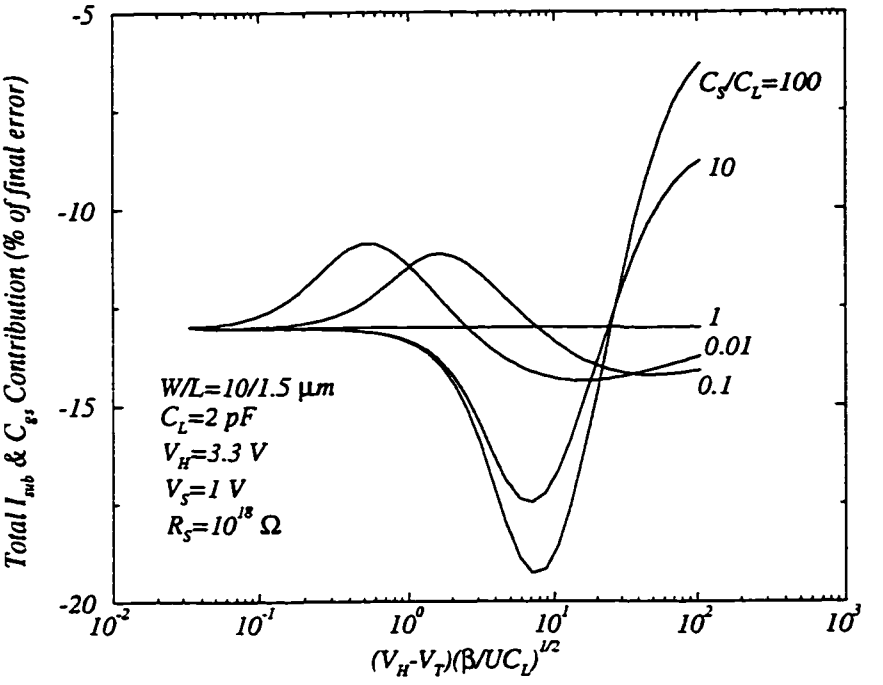

Figure 6.4: The total subthreshold current and gate-source capacitance variation effects for different C_S/C_L values.

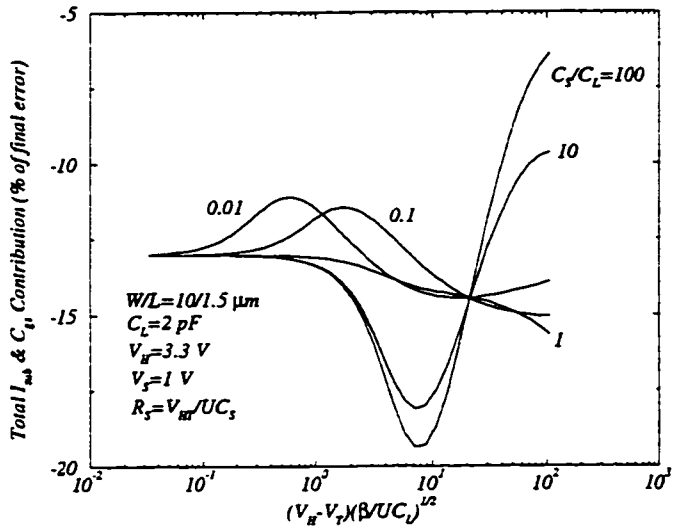

Figure 6.5: The percentage of total I_{sub} and C_{gs} effects for different C_S/C_L values when $\frac{V_{HT}}{UR_SC_S} = 1$.

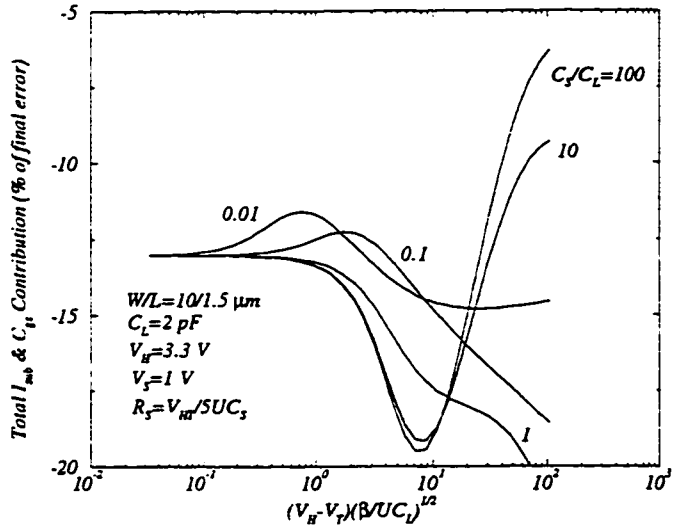

Figure 6.6: The percentage of total I_{sub} and C_{gs} effects for different C_S/C_L values when $\frac{V_{HT}}{UR_SC_S} = 5$.

6.4.2 Moderate Inversion Current Effect

Figure 6.7 shows the effect of the accurate drain current modelling in switch charge injection analysis with respect to the input source resistance for different load capacitances. To show the zero-crossing points, the zero line has been shown using the dashed line. As explained in Chapter 4, the accurate transistor model is particularly important in the moderate inversion region. Therefore, the modelling effects illustrated in Fig. 6.7 are mostly because of the better drain current prediction in moderate inversion. As can be seen, at small source resistances, using the simple transistor model underestimates the final error whereas at high source resistances, it overestimates the error. In other words, the final error predicted using the accurate transistor model increases and decreases from its corresponding value using the simple

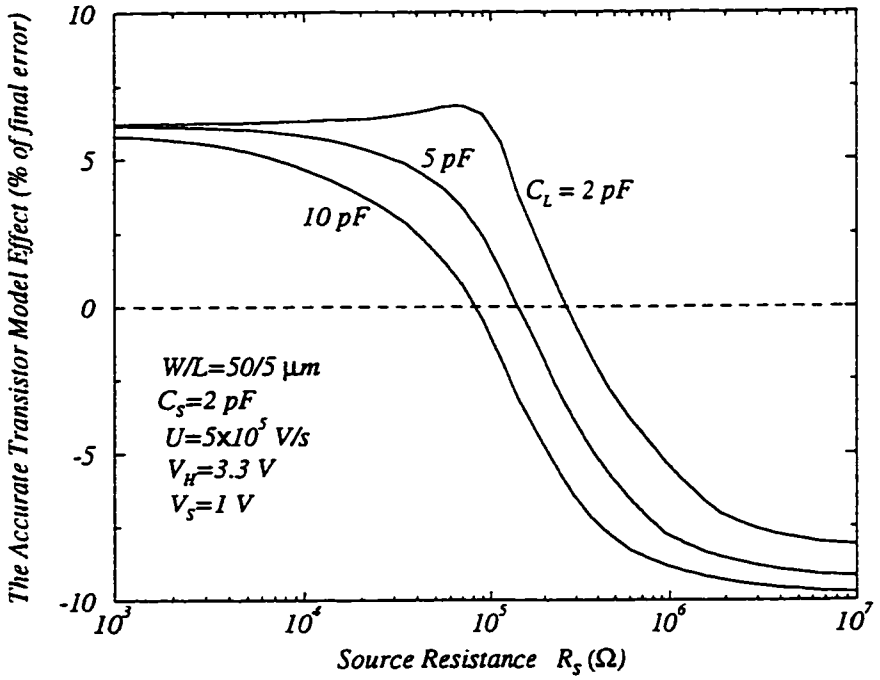

Figure 6.7: The effect of the accurate drain current modelling with respect to the input source resistance for different load capacitances.

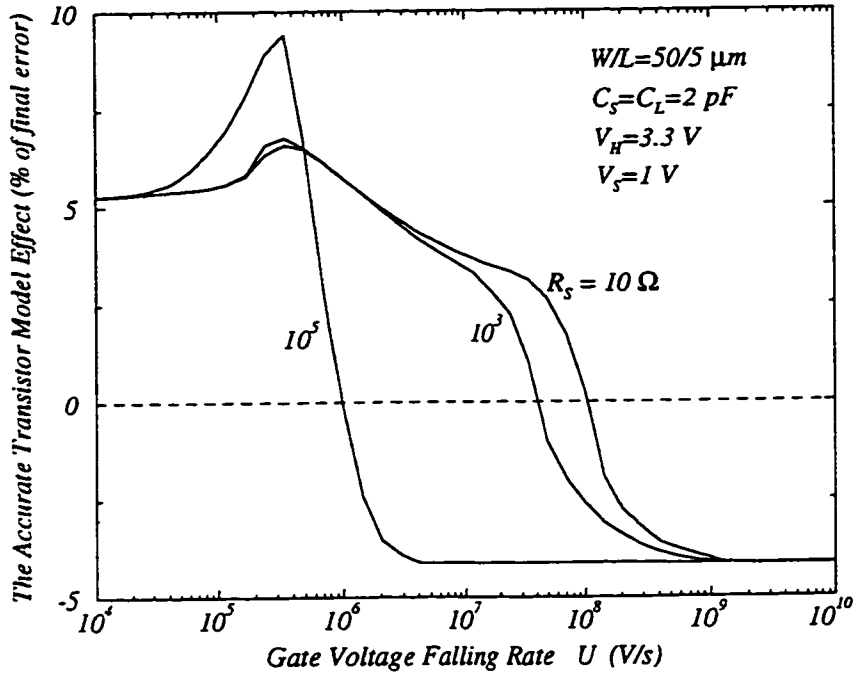

Figure 6.8: The accurate transistor model effect as a function of the gate voltage falling rate for different source resistances.

model at low and high source resistances, respectively. The zero crossing point occurs when the drain current is zero which in turn occurs when the transistor drain-source voltage is zero. The drain-source voltage remains at zero if the charge injection errors at the input and output nodes (nodes A and B) are equal during the gate voltage transient time. At higher load capacitances, the output error voltage decreases, therefore, the zero-crossing occurs at lower values of the charge injection error at the input node (node B) which corresponds to smaller source time constant values $R_S C_S$ (smaller source resistances).

The accurate transistor model effect with respect to the gate voltage falling rate for different source resistances is illustrated in Fig. 6.8. As can

be seen, the application of the accurate transistor model tends to increase and decrease the final predicted error voltage at low and high gate voltage falling rates, respectively. It should be noted that at very high gate voltage falling rates, the charge injected by the gate-source capacitance is the dominant term in the final output error voltage. Also, the amount of predicted channel charge is smaller using the accurate transistor model compared to the one using the simple model. This is because the accurate transistor model tends to have a larger threshold voltage. Therefore, estimating the charge injection error by using the new transistor model results in smaller error voltages. However, at low gate voltage falling rates, where the drain current cancelling the output error voltage is significant, the analysis using the accurate transistor model predicts a larger output error voltage. This is because the lower drain current predicted by using the accurate transistor model, particularly in moderate inversion, leads to lower output error cancellation and as a result to higher estimate of the final error voltage. The zero-crossing occurs where the drain current effect and the gate-source capacitance charge injection effect are equal. Therefore, at higher source resistances which corresponds to lower drain current effects, the zero-crossing occurs at lower gate voltage falling rates where the gate-source capacitance charge injection effect is also lower.

Figure 6.9 shows the effect of the accurate transistor model as a function of the input source voltage for different transistor channel widths. In this figure, the source resistance R_S has been chosen so that the time constant $R_S C_S$ remains equal to the gate voltage fall time. As can be seen, the application of the accurate transistor model is most important at signal levels closer to $V_H - V_T$ where the moderate inversion current is significant compared to the switch current in strong inversion.

Figure 6.10 shows the accurate transistor model effect for different C_S/C_L values when the source resistance is very large. The results have been plot-

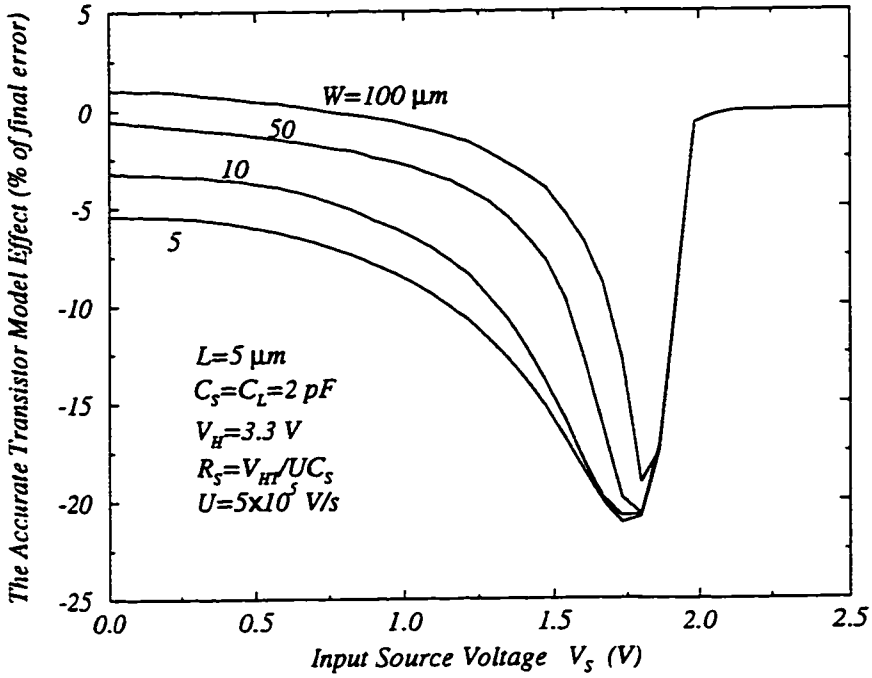

Figure 6.9: The accurate transistor model effect as a function of the input source voltage for different transistor channel widths.

ted as a function of the dimensionless quantity $(V_H - V_T)\sqrt{\frac{\beta}{UC_L}}$. In this simulation, the gate voltage falling rate, U, has been varied from high to low values corresponding to low and high values of $(V_H - V_T)\sqrt{\frac{\beta}{UC_L}}$, respectively. As can be seen from the figure, at $C_S/C_L = 1$ the total effect is negligible because of the small drain-source voltage during the gate voltage transient time which allows small drain currents to flow through the transistor channel. The drain-source voltage is small since the charge injections into the input and output nodes (nodes A and B) are almost equal. The total effect saturates at both ends because the final charge injection error saturates and is independent of the gate voltage falling rate in the extreme cases of U.

The effect of the accurate transistor model for various C_S/C_L values is

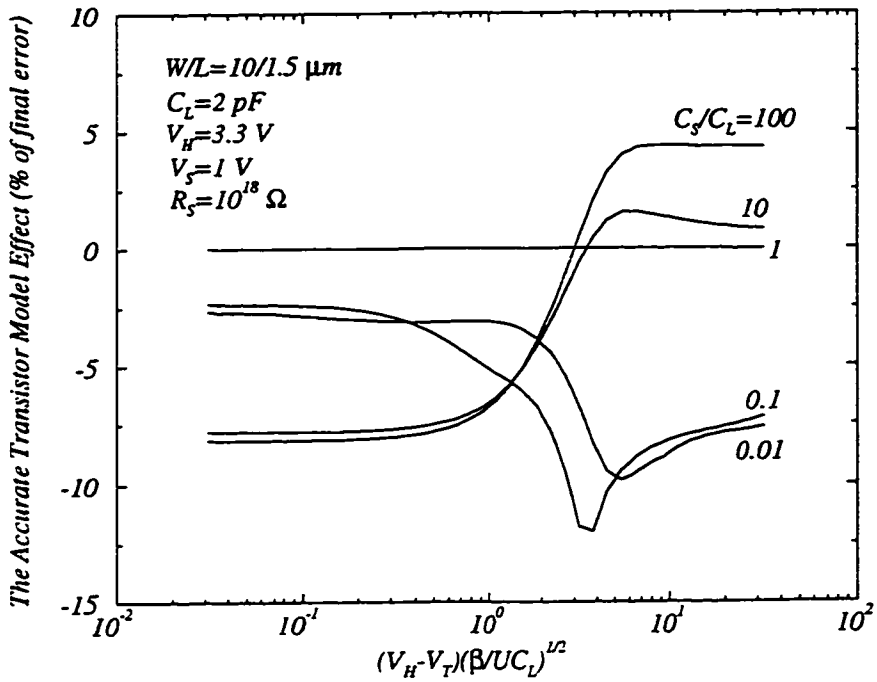

Figure 6.10: The accurate transistor model effect for different C_S/C_L values when the input source resistance is very large.

shown in Figs. 6.11 and 6.12. In these figures, R_S has been chosen to be $\frac{V_{HT}}{UC_S}$ and $\frac{V_{HT}}{5UC_S}$ in Figs. 6.11 and 6.12, respectively. Therefore, the source resistance at each point in Fig. 6.12 is five times smaller than the one at the same point in Fig. 6.11. As can be seen, the accurate transistor model effect varies significantly at large values of C_S/C_L. However, this variation does not change much with the source resistance at high C_S/C_L values. On the other hand, at C_S/C_L values closer to unity the variation of the transistor model effect changes significantly with R_S value.

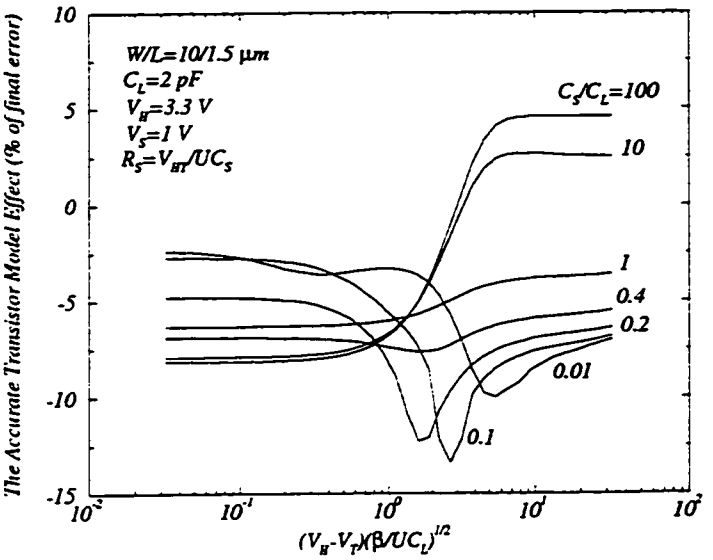

Figure 6.11: The percentage of the accurate transistor model effect for different C_S/C_L values when $\frac{V_{HT}}{UR_SC_S} = 1$.

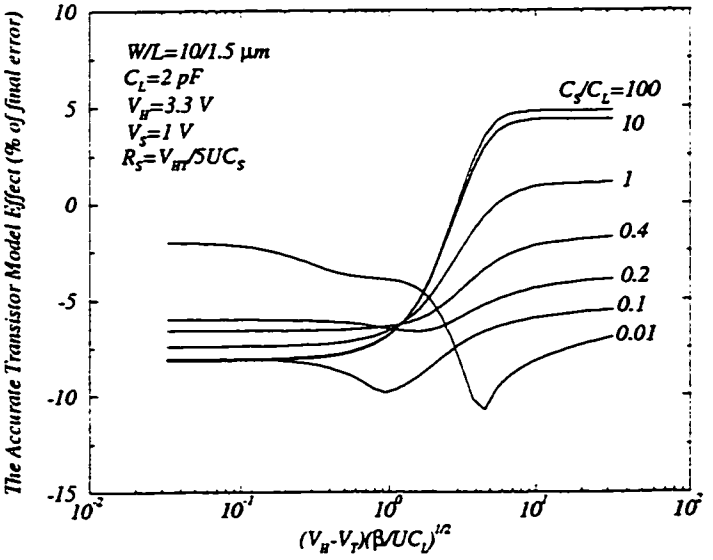

Figure 6.12: The percentage of the accurate transistor model effect for different C_S/C_L values when $\frac{V_{HT}}{UR_SC_S} = 5$.

6.5 Summary

A comprehensive switch charge injection model was developed in this chapter for the general case of the switching problem. This model takes into account second order effects such as the subthreshold current, gate-source capacitance variation and uses as accurate transistor model for the drain current. The use of an accurate transistor model is particularly important in the moderate inversion region.

To solve the differential equations, a modified TLM method was used. This method was found to be computationally very efficient for solving charge injection equations.

The effects of the most important parameters involved with switch charge injection were illustrated and a detailed discussion was given in each case.

Chapter 7

Conclusion

7.1 Summary

A new charge injection error analysis for analog switching circuits was developed in this work. In order to obtain more accurate prediction of the final charge injection error, second order effects were also added in the new analysis. The second order effects discussed in this work are the subthreshold current, gate-source capacitance variation and drain current in the moderate inversion region. Based on this analysis, a comprehensive study was performed on the importance of each effect with regard to the most important electrical and process parameters involved with switch charge injection error. The results show that the second order effects studied in this work can have a significant impact on the final charge injection error calculation and therefore, they need to be considered in the simulation of switching circuits.

The analytical model developed in Chapter 3 provides an excellent insight into the switch charge injection problem with regard to the subthreshold current and gate-source capacitance variation effects.

The accurate transistor model proposed in Chapter 4 is not only useful for precise modelling of the channel current in the switch charge injection

problem but also it can be used as an accurate MOS transistor dc model in circuit simulators. This model is simple and provides a smooth transition in the moderate inversion region between the subthreshold and strong inversion region of operation.

The comprehensive model developed for the general case of switch charge injection in Chapter 5 and 6 can be used for accurate prediction of the final error voltage for various combinations of electrical and process parameters.

7.2 Contributions

Some of the contributions of this work include:

- Introducing the importance of second order effects in charge injection analysis of MOS analog switches.
- Proposing a new analytical model for switch charge injection which takes into account the subthreshold current and gate-source capacitance variation by developing appropriate models for these effects.
- Developing a new dc model for MOS transistors which provides a smooth transition as well as accurate drain current calculation in the moderate inversion region.
- Developing a comprehensive model for the general case of switch charge injection which includes second order effects and utilizes the accurate MOS transistor model.
- Introducing the application of the newly developed transmission line matrix (TLM) method for solving the differential equations involved with the switch charge injection problem.
- Developing a new error estimation procedure for automatic time-stepping technique in the TLM method.

7.3 Future Work

The validity of the new model was verified by designing a test circuit for the special case where the input resistance and capacitance are negligible. It would be interesting to compare the results of this model with the experimental data in the general case. This requires designing a similar test circuit with different resistance and capacitance values connected to the input node.

In this work, a new user interface program was developed to use the new charge injection model. This model should be eventually incorporated into a circuit simulator in order to use the model for analyzing switch charge injection error in more complex circuits. This can be easily done since the model has been developed to be compatible with the SPICE models. An example of this work was explained in Chapter 4 for the SPICE level 3 model. Also, further comparison between this model and the BSIM models is required to investigate the advantages and disadvantages of this new model.

In applications where the switch on-resistance is important, analog switches are replaced by transmission gates. The new model can also be used to study the charge injection problem in transmission gates. It would be useful to investigate the importance of second order effects in these switches.

In the proposed MOS transistor dc model in Chapter 4, the SPICE level 3 model was used as the base model. Since the final model inherits the charactristics of the base model, more improved models such as the BSIM model can be used to develop a similar MOS transistor dc model.

Bibliography

[1] G. Wegmann, E.A. Vittoz, and F.Rahali, "Charge injection in analog MOS switches", *IEEE J. Solid-State Circuits*, vol. SC-22, no. 6, pp. 1091–1097, Dec. 1987.

[2] R.C. Yen and P.R. Gray, "An MOS switched capacitor instrumentation amplifier", *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 1008–1013, Dec. 1982.

[3] R. Suarez, P. Gray, and D. Hodges, "All-MOS charge redistribution Analog-to-Digital conversion techniques-Part II", *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 379–385, Dec. 1975.

[4] F. Sabouri, *A CMOS High-Performance Analog-to-Digital Converter*, Ph.D. dissertation, The University of Calgary, Canada, 1996.

[5] F. Sabouri, F. N. Trofimenkoff, and J. W. Haslett, "A High-Performance Calibration-Free Charge-Balancing Analog-to-Digital converter", *IEEE Trans. Instrumentation and Measurements*, vol. 45, no. 5, pp. 847–853, Oct. 1996.

[6] D. MacQuigg, "Residual charge on a switched capacitor", *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 811–813, Dec. 1983.

[7] B.J. Sheu and C. Hu, "Switched-induced error voltage on a switched capacitor", *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 519–525, Aug. 1984.

[8] J.H. Sheu, M. Patil, and B.J. Sheu, "Modeling charge injection in MOS analog switches", *IEEE Trans. Circuits Syst.*, vol. CAS-34, pp. 214–216, Feb. 1987.

[9] B.J. Sheu, J.H. Shieh, and M. Patil, "Measurement and analysis of charge injection in MOS analog switches", *IEEE J. Solid-State Circuits*, vol. SC-22, no. 2, pp. 277–281, Apr. 1987.

[10] C. Eichenberger and W. Guggenbuhl, "On charge injection in analog MOS switches and dummy switch compensation techniques", *IEEE Trans. Circuits and Systems*, vol. 37, no. 2, pp. 256–264, Feb. 1990.

[11] H.J. Park, P.K. Ko, and C. Hu, "A non-quasi-static MOSFET model for SPICE-transient analysis", *IEEE Trans. Electron Devices*, vol. 36, no. 3, pp. 561–575, March 1989.

[12] H.J. Park, P.K. Ko, and C. Hu, "A charge conserving non-quasi-static(NQS) MOSFET model for SPICE transient analysis", *IEEE Trans. Computer Aided Design*, vol. 10, no. 5, pp. 629–642, May 1991.

[13] M.J. Chen, Y.B. Gu, T. Wu, P.C. Hsu, and T.H. Liu, "Weak inversion charge injection in analog MOS switches", *IEEE J. Solid-State Circuits*, vol. 30, no. 5, pp. 604–606, May 1995.

[14] M.J. Chen, Y.-B. Gu, T. Wu, P.-C. Hsu, and T.-H. Liu, "New observation of charge injection in MOS analogue switches", *Electronics Letters*, vol. 30, pp. 213–214, 1994.

[15] Y.-B. Gu and M.-J. Chen, "A new quantitative model for weak inversion charge injection in MOSFET analog switches", *IEEE Trans. Electron Devices*, vol. 43, no. 2, pp. 295–301, Feb. 1996.

[16] S. Aghtar, J.W. Haslett, and F.N. Trofimenkoff, "Subthreshold analysis of an MOS analog switch", *IEEE Trans. Electron Devices*, vol. 44, no. 1, pp. 89–96, Jan. 1997.

[17] J. S. Brugler and P. G. Jespers, "Charge pumping in MOS devices", *IEEE Trans. Electron Devices*, vol. ED-16, pp. 297–302, March 1969.

[18] C. Turchetti, P. Mancini, and G. Masetti, "A CAD-oriented Non-Quasi-Static approach for the transient analysis of MOS IC's", *IEEE J. Solid-State Circuits*, vol. SC-21, no. 5, pp. 827–836, Oct. 1986.

[19] J. B. Kuo, R. W. Dutton, and B. A. Wooley, "Turn-Off transient in circular geometry MOS pass transistors", *IEEE J. Solid-State Circuits*, vol. SC-21, no. 5, pp. 837–844, Oct. 1986.

[20] E. Kreyszig, *Advance engineering mathematics*, John Wiley & Sons, 1967.

[21] R.M. Swanson and J.D. Meindl, "Ion-implanted complementary MOS transistor in low-voltage circuits", *IEEE J. Solid-State Circuits*, vol. SC-7, no. 2, pp. 146–153, April 1972.

[22] Y. Cheng, M. C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P. K. Ko, and C. Hu, "A physically and scalable I-V model in BSIM3v3 for Analog/Digital circuit simulation", *IEEE Trans. Electron Devices*, vol. 44, no. 2, pp. 277–287, Feb. 1997.

[23] "TMA MEDICI: Two-Dimentional device simulation program", *Technology Modeling Association, Inc*, 1993.

[24] Y.P. Tsividis, *Operation and modeling of the MOS transistor*, New York, McGraw-Hill, 1987.

[25] S. Aghtar, J.W. Haslett, and F.N. Trofimenkoff, "A DC model for MOS transistors using a variable threshold voltage method", *To be published.*

[26] H.C. Pao and C.T. Sah, "Effect of diffusion current on characteristics of metal-oxide-semiconductor transistors", *Solid-State Electronics*, vol. 9, pp. 927–937, 1966.

[27] J.R. Brews, "A charge sheet model of the MOSFET", *Solid-State Electronics*, vol. 21, pp. 345–355, 1978.

[28] R.F. Pierret and J.A. Shields, "Simplified long-channel MOSFET theory", *Solid-State Electronics*, vol. 26, pp. 143–147, 1983.

[29] A.R. Boothryod, S.W. Tarasewicz, and C. Slaby, "MISNAN- a physically based continuous MOSFET model for CAD applications", *IEEE Trans. Computer Aided Design*, vol. CAD-10, pp. 1512–1529, 1991.

[30] H.J. Park, P.K. Ko, and C. Hu, "A charge sheet capacitance model of short channel MOSFET's for SPICE", *IEEE Trans. Computer Aided Design*, vol. CAD-10, pp. 376–389, 1991.

[31] M. Shur, T. A. Fjeldly, T. Ytterdal, and Lee, "An unified MOSFET model", *Solid-State Electron*, vol. 35, pp. 1795–1802, 1992.

[32] N. D. Arora, R. Rios, C. L. Huang, and K. Raol, "PCIM: A physically based continuous Short-Channel IGFET model for circuit simulation", *IEEE Trans. Electron Devices*, vol. 41, pp. 988–997, 1994.

[33] M.B. Barron, "Low level currents in insulated gate field effect transistor", *Solid-State Electronics*, vol. 15, pp. 293–302, 1972.

[34] Meta-Software, Inc, *HSPICE User's Manual*, 1990.

[35] P.J. Lim and B.A. Wooley, "A High-Speed Sample-and-Hold technique using a Miller hold capacitance", *IEEE J. Solid-State Circuits*, vol. 26, pp. 643–651, 1991.

[36] P. B. Johns and R. L. Beaurle, "Numerical solution of 2-dimentional scattering problems using a transmission line matrix", *Proc. IEE*, vol. 118, pp. 1203–1208, 1971.

[37] A. H. M. Saleh, "A multicompartment TLM model for solving First-Order rate equations", *Int. J. Numerical Modelling: Electronic Networks, Device and Fields*, vol. 2, pp. 53–60, 1989.

[38] A. H. M. Saleh and D. De Cogan, "Numerical solution of inhomogeneous and nonlinear ordinary differential equations using the TLM multicompartment model", *Int. J. Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 3, pp. 215–228, 1990.

[39] X. Gui, S. Aghtar, J. W. Haslett, and D. De Cogan, "Error estimation and control in the multicompartment TLM model for Initial-Value problems in ordinary differential equations", *Proceeding of the 2nd International Workshop on Transmission Line Matrix (TLM) Modelling-Theory and Applications, Munich, Germany*, pp. 126–134, Oct. 1997.

[40] S. H. Pulko, A. Mallik, R. Allen, and P. B. Johns, "Automatic timestepping in TLM routines for the modelling of thermal diffusion processes", *Int. J. Numer. Model. : Electron. Netw. Devices Field*, vol. 3, pp. 127–136, 1990.

[41] P. W. Webb and X. Gui, "Implementation timestep changes in Transmission-Line matrix diffusion modelling", *Int. J. Numer. Model. : Electron. Netw. Devices Fields*, vol. 5, pp. 251–257, 1992.

[42] S. Y. R. Hui, K. K. Fung, M. Q. Zhang, and C. Christopoulos, "Variable time step technique for transmission line modelling", *IEE Proc.-A*, vol. 140, pp. 299–302, 1993.

[43] S. Y. R. Hui, K. K. Fung, M. Q. Zhang, and C. Christopoulos, "Variable-Time-Step TLM algorithm: A unified approach", *Electron. Lett.*, vol. 29, pp. 978–979 and 1232, 1993.

[44] C. W. Gear, *Numerical Initial Value Problems in Ordinary Differential Equations*, Printice-Hall, Englewood Cliffs, NJ, 1971.

Appendix A

The Gate-Source Capacitance Variation in a MOS Switch

Charge neutrality in a MOS transistor results in

$$Q_G = Q_I + Q_B, \tag{A.1}$$

where Q_G is the total gate charge, Q_I is the inversion layer charge and Q_B is the total bulk charge. Q_G and Q_B are given by

$$\begin{aligned} Q_G &= -C_{ox}(V_G - V_{FB} - \psi_S) \\ Q_B &= -C_{ox}\gamma\sqrt{\psi_S}. \end{aligned} \tag{A.2}$$

V_{FB} is the flat band voltage and ψ_S is the surface potential at the source given by

$$\psi_S = V_G - V_{FB} - \gamma\sqrt{\psi_S + V_t e^{(\psi_S - 2\phi_F - V_S)/V_t}}. \tag{A.3}$$

Based on the drain-source voltage, Q_I is divided into source and drain charges (Q_S and Q_D). For small V_{DS} where $Q_S \simeq Q_D$, the gate charges can be written as

$$Q_G = 2Q_S + Q_B. \tag{A.4}$$

The gate-source capacitance is defined by

$$C_{gs} = -\frac{dQ_S}{dV_G}. \tag{A.5}$$

Substituting (A.1)-(A.4) into (A.5), yields C_{gs} at the threshold voltage where $\psi_S = 2\phi_F + V_S$ to be

$$C_{gsm} = C_{gs}(\psi_S = 2\phi_F + V_S) = \frac{1}{1 + \sqrt{2\phi_F + V_S}/\gamma}\left(\frac{C_{ox}}{4}\right). \tag{A.6}$$

Above the threshold voltage C_{gs} increases with respect to the gate-source voltage and saturates at $\frac{C_{ox}}{2}$. However, the inversion layer charges decrease exponentially with respect to the gate-source voltage in the weak inversion region [24]. Assuming the variation of the depletion region charges is negligible below threshold where the gate-source voltage is still close to V_T, the total gate charges and consequently the gate-source capacitance (C_{gs}) decrease exponentially with respect to the gate-source voltage in the weak inversion region. In other words, in weak inversion

$$C_{gs} \propto \exp\left(\frac{V_{GS} - V_{on}}{nV_t}\right). \tag{A.7}$$

The exponential behavior is assumed throughout the weak inversion region although at lower gate-source voltages, the depletion region charge variation is not negligible. The error due to this assumption is not important in the final results since in this region the value of C_{gs} is very small and can not change the overall answer significantly. Therefore, (C_{gs}) can be approximated by two exponential functions above and below the threshold voltage as follows,

$$C_{gs} = \begin{cases} C_{gsm}\exp\left(\frac{V_{GS}-V_{on}}{nV_t}\right) & V_{GS} < V_{on} \\ \frac{C_{ox}}{2} - \left(\frac{C_{ox}}{2} - C_{gsm}\right).\exp\left(-\frac{V_{GS}-V_{on}}{kV_t}\right) & V_{GS} \geq V_{on}\ . \end{cases} \tag{A.8}$$

In (A.8), k is a fitting factor between 5 and 10 for the practical range of substrate dopings and gate oxide thickness.

A comparison of (A.8) and the accurate NQS model results for different substrate dopings (Fig.A.1) shows that (A.8) is a good approximation of C_{GS} for small drain-source voltages. Equation (A.8) can be used to model the gate-source capacitance variations above and below threshold in the charge injection error analysis.

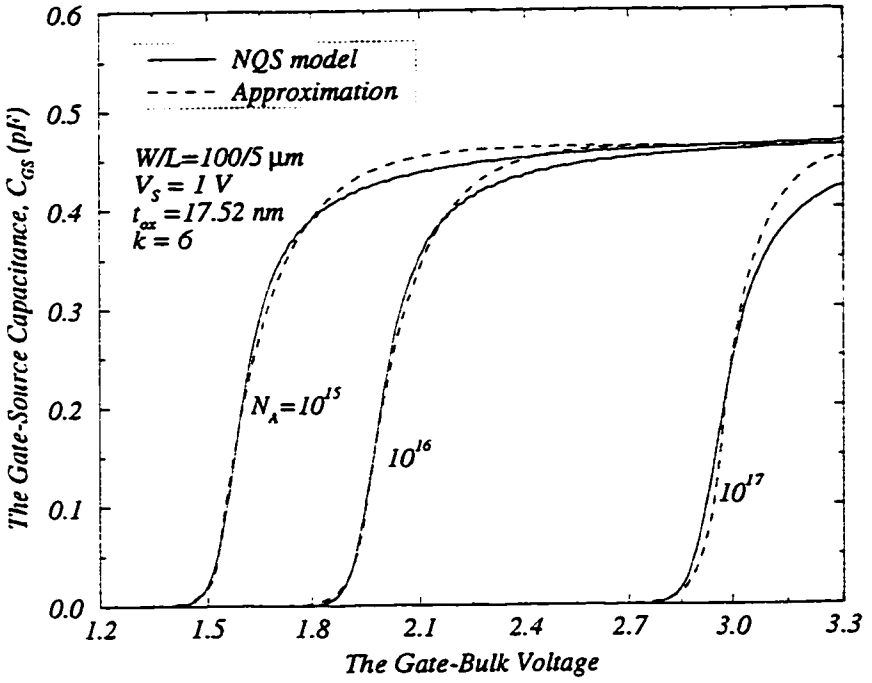

Figure A.1: The gate-source capacitance approximation for different substrate dopings.

Appendix B

Surface Potential Calculation

Equations (4.34) can be rearranged to the following form:

$$e^{U_S-\xi-2U_F} = a^2\left(U_G - U_S\right)^2 - U_S + 1, \tag{B.1}$$

where

$$a = \frac{1}{\gamma'}. \tag{B.2}$$

An intial guess can be made for U_S depending on its value above and below $\xi + 2U_F$. For $U_{sm} \leq \xi + 2U_F$

$$U_S = U_{sm} = U_G + \frac{1}{2a^2}\sqrt{\left(U_G + \frac{1}{2a^2}\right)^2 - U_G^2}, \tag{B.3}$$

and for $U_{sm} > \xi + 2U_F$

$$U_S = \xi + 2U_F + \ln\left[a^2\left(U_G - \xi - 2U_F\right)^2 - \xi - 2U_F\right]. \tag{B.4}$$

U_{sm} corresponds to the condition when the channel charge-sheet density is zero and defines the maximum possible surface potential value U_{sm} for a given gate voltage. U_{sm} is the value of U_S for which (B.1) equates to zero.

The initial guess calculated from (B.3) and (B.4) may not be accurate

enough. To improve the accuracy of U_S, the second-order Newton-Raphson iteration can be used which gives

$$U_S^{i+1} = U_S^i - \frac{F}{F'}\left[1 - \frac{FF''}{2(F')^2}\right]^{-1}, \tag{B.5}$$

where

$$F = a^2(U_G - U_S)^2 - U_S - F_e, \tag{B.6}$$

$$F' = \frac{\partial F}{\partial U_S} = -2a^2(U_G - U_S) - 1 - F_e, \tag{B.7}$$

$$F'' = \frac{\partial^2 F}{\partial U_S^2} = 2a^2 - F_e, \tag{B.8}$$

and

$$F_e = e^{U_s - \xi - 2U_F}. \tag{B.9}$$

The surface potential calculation can be summarized as follows:

```
Us = UG+1/(2*a^2)-sqrt((UG+1/(2*a^2))^2-UG^2);
Usm = Us;
if (Usm > 2*UF+ξ)
    Us = ξ+2*UF+log(a^2*(UG-ξ-2*UF)^2-ξ-2*UF);
end
for (I = 0; I < Num_Iteration;)
    Fe = exp(Us-2*UF-ξ);
    F = a^2(UG-Us)^2-Us-Fe;
    F1 = -2a^2(UG-Us)-1-Fe;
    F2 = 2a^2-Fe;
    Us = Us-(F/F1)/(1-(F*F2)/(2*F1^2));
end
```

Appendix C

Transmission-Line Matrix (MC-TLM) Method for Solving Ordinary Differential Equations

We start with a single rate equation given by [1]

$$\frac{dV_x}{dt} = g_1V_1 + g_2V_2 + g_3V_3 + g_4V_4 - d_1V_x - d_2V_x - d_3V_x - d_4V_x \qquad \text{(C.1)}$$

where V_1 to V_4 are the neighboring compartments, g_1 to g_4 are the rate constants representing the effects of V_1 to V_4 on the compartment V_x , respectively, and d_1 to d_4 are the decay rates of the compartment V_x into the compartments V_1 to V_4, respectively.

In the general form, a set of first-order equations can be written as follows

$$\frac{dV_m}{dt} = \sum_{j=1}^{n} g_jV_j - \sum_{j=1}^{n} d_jV_m \qquad (m = 1, 2, \cdots, n). \qquad \text{(C.2)}$$

[1]The Appendix is a summary of references [36–39] regarding the MC-TLM algorithms, which is included here to give the reader an outline of the model. More detailed information can be found in the references given.

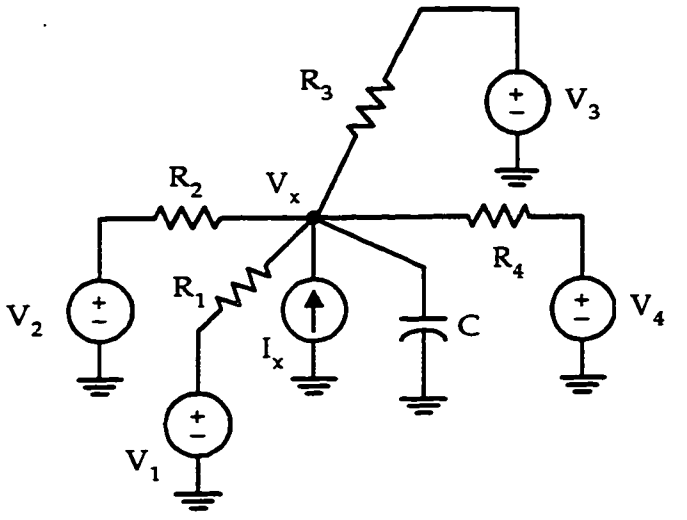

Figure C.1: The equivalent circuit of a single compartment.

In equation (C.2), n is the number of neighboring compartments and the equation describes the mth compartment.

Now let us consider the analysis of the circuit shown in Fig. C.1. The voltage V_x across the capacitor C is given by

$$C\frac{dV_x}{dt} = \frac{V_1 - V_x}{R_1} + \frac{V_2 - V_x}{R_2} + \frac{V_3 - V_x}{R_3} + \frac{V_4 - V_x}{R_4} + I_x. \qquad \text{(C.3)}$$

Equation (C.3) can be rearranged to the following form

$$\frac{dV_x}{dt} = \frac{I_x}{C} - \frac{V_x}{C}\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4}\right] + \frac{V_1}{R_1C} + \frac{V_2}{R_2C} + \frac{V_3}{R_3C} + \frac{V_4}{R_4C}. \qquad \text{(C.4)}$$

As can be seen, equation (C.4) has a similar form to equation (C.1) where

$$C = 1, \quad R_1 = \frac{1}{g_1}, \quad R_2 = \frac{1}{g_2}, \quad R_3 = \frac{1}{g_3}, \quad R_4 = \frac{1}{g_4}, \qquad \text{(C.5)}$$

and

$$I_x = g_m V_x, \qquad \text{(C.6)}$$

where

$$g_m = \sum_{j=1}^{4}(g_j - d_j). \tag{C.7}$$

Therefore, equation (C.4) can be written as follows

$$\frac{dV_x}{dt} = g_1V_1 + g_2V_2 + g_3V_3 + g_4V_4 - V_x(d_1 + d_2 + d_3 + d_4) \tag{C.8}$$

The constant rates for the general form of equation (C.2) are given by

$$g_j = \frac{1}{R_j} \qquad j = 1, \cdots, n \tag{C.9}$$

where

$$g_m = \sum_{j=1}^{n}(g_j - d_j). \tag{C.10}$$

To solve a set of differential equations with the TLM method, each equation is modelled by its equivalent circuit representation shown in Fig. C.1. Therefore, solving the set of equations (C.2) is reduced to the problem of solving the circuit representation of each equation for the corresponding capacitor voltages.

In the TLM representation of the electric circuit in Fig. C.1, the capacitor C is replaced by an open-circuit transmission line stub as shown in Fig. C.2. The stub capacitance is defined by

$$C = y_s\frac{\Delta t}{2}, \tag{C.11}$$

where y_s is the stub admittance and Δt is the time required for the pulse to reach the end of the stub and return. For $C = 1$,

$$y_s = \frac{1}{z_s} = \frac{2}{\Delta t}. \tag{C.12}$$

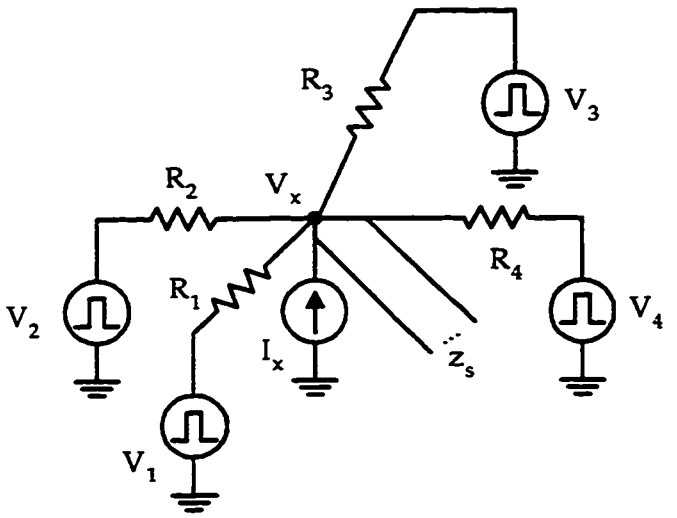

Figure C.2: The TLM representation of a single compartment.

C.1 The Scattering Algorithm

In Fig. C.2, first a voltage pulse is sent by each voltage source which generates a current in the corresponding resistor. The resulting pulse which appears at node V_x, travels along the stub and returns within Δt second time period. The reflected pulse scatters at the junction due to the mismatch of impedances. Then, the combination of the scattered pulse and the new pulse generated by the sources travels along the stub and returns to node V_x again.

Figure C.3 shows the equivalent circuit of the stub for the pulse scattering problem. V_s^i and V_s^r are the incident voltage pulse returned from the stub and the reflected pulse to the stub, respectively. I_s^i is the incident current.

The equivalent circuit for pulse scattering analysis of a single compartment is shown in Fig. C.4. To find V_x as a function of time, an iterative method can be used by employing the principle of superposition at each time step. At iteration interval k, the node voltage due to the voltage sources is

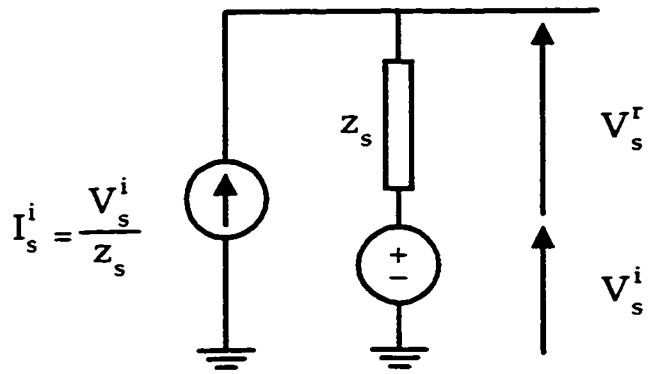

Figure C.3: Stub equivalent circuit for the pulse scattering problem.

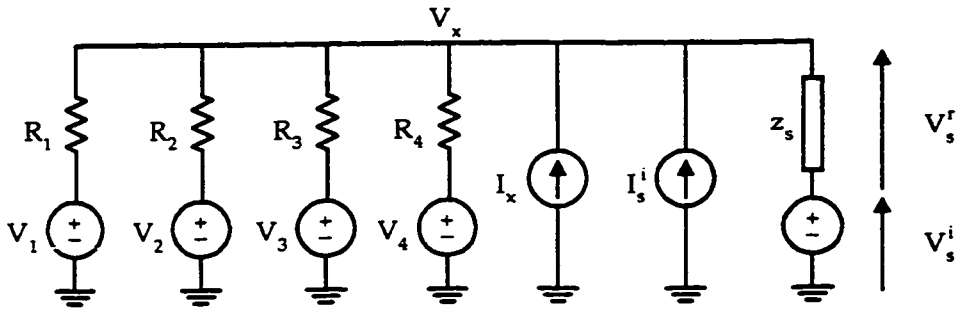

Figure C.4: The equivalent circuit for pulse scattering analysis of a single compartment.

given by

$$\frac{\sum_{j=1}^{4} V_j(k) g_j + V_s^i y_s}{\sum_{j=1}^{4} g_j + y_s}$$

and the node voltage due to the current sources ($I_x = g_m V_x$ and $I_s^i = y_s V_s^i$) is given by

$$\frac{g_m V_x + y_s V_s^i(k)}{\sum_{j=1}^{4} g_j + y_s}.$$

V_x is the node voltage at the previous time step. Therefore, the final node

voltage V_x at iteration interval k, $V_x(k)$, becomes

$$V_x(k) = \frac{\sum_{j=1}^{4} V_j(k)g_j + 2y_s V_s^i(k) + V_x(k-1)g_m}{\sum_{j=1}^{4} g_j + y_s} \tag{C.13}$$

The returned voltage to the stub at iteration interval k, $V_s^r(k)$, is given by

$$V_s^r(k) = V_x(k) - V_s^i(k). \tag{C.14}$$

$V_s^r(k)$ becomes the incident voltage into the stub at the next time interval after travelling along the stub and reflecting back. Therefore,

$$V_s^i(k+1) = V_s^r(k). \tag{C.15}$$

The node voltage V_x can be calculated iteratively using equations (C.13) to (C.15).

The initial value of the compartment V_x can be included in this method as an initial voltage across the capacitor C in Fig. C.1. To set the initial value of the voltage controlled current generator I_x, a pulse voltage can be sent through the stub at time $t = 0$. If the compartment V_x has an initial condition A_0, it can be shown that the stub-charging voltage at $t = 0$ is given by

$$V_s^i(0) = \frac{A_0\left(\sum_{j=1}^{4} g_j + y_s\right)}{2y_s}. \tag{C.16}$$

In the general case of equation (C.2), the node voltage of the mth compartment at iteration interval k is given by

$$V_m(k) = \frac{\sum V_j(k)g_j + 2y_s V_s^i(k) + V_m(k-1)g_m}{\sum g_j + y_s} \tag{C.17}$$

and

$$V_s^r(k) = V_m(k) - V_s^i(k) \tag{C.18}$$

$$V_s^i(k+1) = V_s^r(k). \tag{C.19}$$

The initial value of each compartment can be incorporated in the analysis as

$$V_s^i(0) = \frac{V_m(0)\,(\sum g_j + y_s)}{2y_s}. \tag{C.20}$$

Equation (C.17) is the form which was used by Saleh [37]. An explicit expression independent of the previous value of V_x can be derived [39] as follows

$$V_m(k) = \frac{\sum V_j(k) g_j + 2y_s V_s^i(k)}{\sum g_j + y_s - g_m} = \frac{\sum V_j(k) g_j + 2y_s V_s^i(k)}{\sum d_j + y_s}. \tag{C.21}$$

If equation (C.21) is used for the analysis, a slightly different expression for the initial value condition needs to be used which is given by

$$V_s^i(0) = \frac{V_m(0)\,(\sum g_j + y_s - g_m)}{2y_s} = \frac{V_m(0)\,(\sum d_j + y_s)}{2y_s}. \tag{C.22}$$

C.2 Variable Time-Step

In the new variable time step TLM method, pulses are scattered from nodes and half-way through their transit the impedances of the lines are altered and the incident voltages are modified. This is a similar approach to the one used in TLM diffusion modelling [40, 41]. In this case the requirement of the incident voltage pulse at each iteration is dictated by equations (C.17) and (C.21). Although equation (C.19) cannot be used directly if a time-step change occurs between the kth and $(k+1)$th iteration, equation (C.18) is still valid. This means that a new reflected pulse can be calculated by

$$V_s^{i\prime}(k+1) = V_s^{r\prime}(k) = V_m(k) - V_s^{i\prime}(k) \tag{C.23}$$

where the prime is used to denote the revised parameters after a time-step change.

The net current in a stub with a pulse $V_s^i(k)$ incident on the node is given by

$$I_s(k) = \frac{V_m(k) - 2V_s^i(k)}{z_s}. \tag{C.24}$$

It is a requirement of continuity that both the voltage, $V_m(k)$, and the current, $I_s(k)$, be unaffected by the time-step change. Thus

$$V_s^{i\prime}(k) = \frac{V_m(k) - I_s(k)z_s'}{2}. \tag{C.25}$$

Inserting equations (C.24) and (C.25) into (C.23) yields

$$V_s^{i\prime}(k+1) = V_s^{r\prime}(k) = \frac{1+\alpha}{2}V_m(k) - \alpha V_s^i(k) \tag{C.26}$$

where α is the ratio between the new and the old time steps. It is also the ratio (reciprocal ratio) between the new and old impedances (admittances). These outcomes are consistent with the time-stepping techniques of Hui et al [42, 43].

C.3 Error Analysis

The error of a pth order accurate numerical technique can be predicted using Richardson extrapolation [44]

$$\frac{V^*(k+1) - V^{(\Delta t)}(k+1)}{V^*(k+1) - V^{(\Delta t/2)}(k+1)} \cong 2^{p-1} \tag{C.27}$$

or

$$V^*(k+1) - V^{(\Delta t/2)}(k+1) \cong \frac{1}{2^{p-1}-1}\left[V^{(\Delta t/2)}(k+1) - V^{(\Delta t)}(k+1)\right] \tag{C.28}$$

where $V^*(k+1)$ is the exact solution at the $(k+1)$th iteration. $V^{(\Delta t)}$ and $V^{(\Delta t/2)}$ are the TLM results based on time steps (Δt) and $(\Delta t/2)$, respectively. Equation C.28 provides a practical way to estimate the error without the need for the exact analytical solution as follows:

$$\Delta = \left| V^{(\Delta t/2)}(k+1) - V^{(\Delta t)}(k+1) \right|. \tag{C.29}$$

The basic time-step control mechanism is to execute computation one step with Δt and two steps with $\Delta t/2$, and to perform an accuracy test. For a given tolerance value $\varepsilon > 0$, the magnitude of Δt is halved if $\Delta \geq \varepsilon$, otherwise it is doubled. The computation proceeds this way at each iteration according to the solution variation with time so that the requirements in both accuracy and efficiency are hopefully satisfied.

C.4 Time-Step Control

To implement the above procedure, a tentative time step with a small value is used at the beginning of the computation [39]. This initial time step may be enlarged according to a prescribed tolerance (ε) and a reasonable value can be found quickly to continue the computation. As discussed above, the information at the end of one time step and two half-valued time steps may be stored for Richardson error estimation. However, this would require performing the nodal potential calculation three times for a single iteration. An alternative way of estimating the error and controlling the time step is to consider the deviation of nodal potential with respect to time step. From equation (C.21), we have

$$\frac{dV_m(k)}{dy_s} = \frac{2V_s^i(k) - V_m(k)}{\sum_j d_j + y_s(k)} + \frac{2y_s}{\sum_j d_j + y_s(k)} \frac{dV_s^i(k)}{dy_s(k)} \tag{C.30}$$

where the $V_s^i(k)$ variation with y_s can be obtained from equation (C.26) as follows

$$\frac{dV_s^i(k)}{dy_s(k)} = \frac{y_s(k-1)}{y_s^2(k)}\left(V_s^i(k-1) - \frac{V_m(k-1)}{2}\right). \tag{C.31}$$

Also, we have

$$\frac{dV_m(k)}{d(\Delta t)} = \frac{dV_m(k)}{dy_s(k)}\frac{dy_s(k)}{d(\Delta t)} = -\frac{2}{(\Delta t)^2}\frac{dV_m(k)}{dy_s(k)}. \tag{C.32}$$

Therefore,

$$\begin{aligned}\Delta &= \left|V^*(k) - V^{(\Delta t)}(k)\right| = \left|V^{(\Delta t)}(k) - V^{(2\Delta t)}(k)\right| = \left|\frac{dV_m(k)}{d(\Delta t)}(\Delta t - 2\Delta t)\right| \\ &= \left|\frac{2V_s^i(k) - V_m(k)}{\sum_j d_j + y_s(k)}y_s(k) + \frac{2V_s^i(k-1) - V_m(k-1)}{\sum_j d_j + y_s(k)}y_s(k-1)\right|. \end{aligned} \tag{C.33}$$

Here, Richardson extrapolation $V^{(\Delta t)}(k) - V^{(2\Delta t)}(k)$ is approximated by the differential of the nodal potential. For error estimation at the first iteration ($k = 1$), initial conditions are used for calculating the second term on the right-hand side of equation (C.33). Owing to this equation, the data storage and computational effort for estimating errors are minimized and the procedure of time-step control is greatly simplified.

C.5 Example

An MC-TLM general-purpose program for solving initial-value problems in ODEs employing a constant time step (CTS) or a variable time step (VTS) has been written and tested for a range of differential equations. To explain the details of this method, solving the Van Der Pol equation with the TLM method is discussed here.

The Van Der Pol equation is given by

$$\frac{d^2x}{dt^2} + \epsilon(x^2 - 1)\frac{dx}{dt} + x = 0. \tag{C.34}$$

This equation can be reduced to two first order rate equations as follows

$$\frac{dx}{dt} = y \tag{C.35}$$

$$\frac{dy}{dt} = -\epsilon(x^2 - 1)y - x. \tag{C.36}$$

The TLM representation of this equation has two compartments, x and y. The parameters of this representation are summarized in Table C.1.

	x	y
d_1	0	$\epsilon(x^2 - 1)$
d_2	0	0
g_1	1	1
g_2	0	0
V_1	y	$-x$
V_2	0	0

Table C.1: The TLM multicompartment representation of the Van Der Pol equation.

The decay rate d_1 of the compartment y at the iteration interval k depends on the value of the compartment x at the iteration $k - 1$. Figure C.5 shows the answers for x and y as a function of time when $\epsilon = 1$, $x(0) = 2.5$ and $y(0) = \frac{dx}{dt}|_{t=0} = 0$. The variation of the time-step is plotted in Fig. C.6. As can be seen, in the variable time-step TLM method, the time step is adjusted automatically to preserve the accuracy of the answer and maximize the speed by increasing the time step where it is possible.

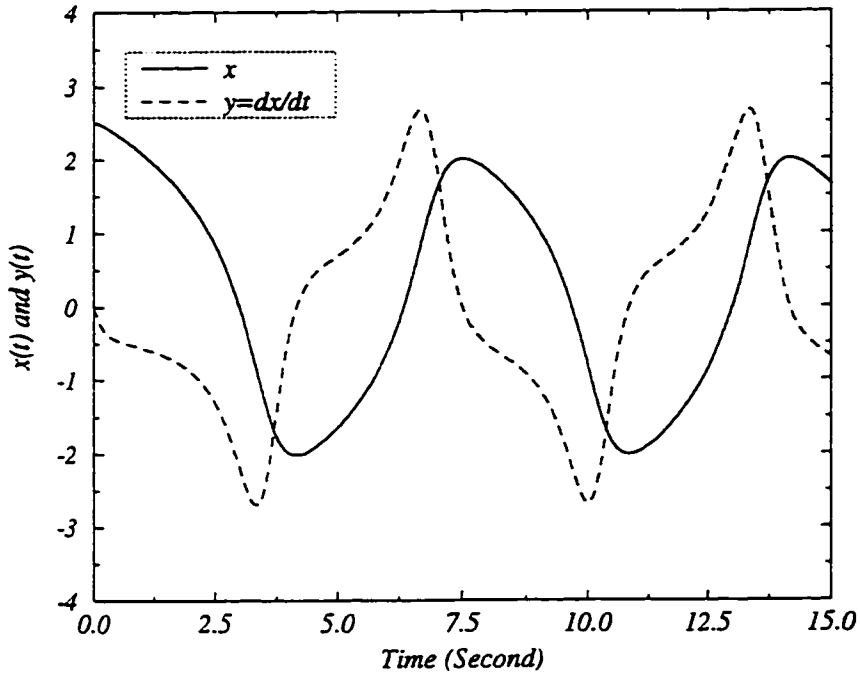

Figure C.5: The solution to the Van Der Pol equation using the variable time-step TLM method.

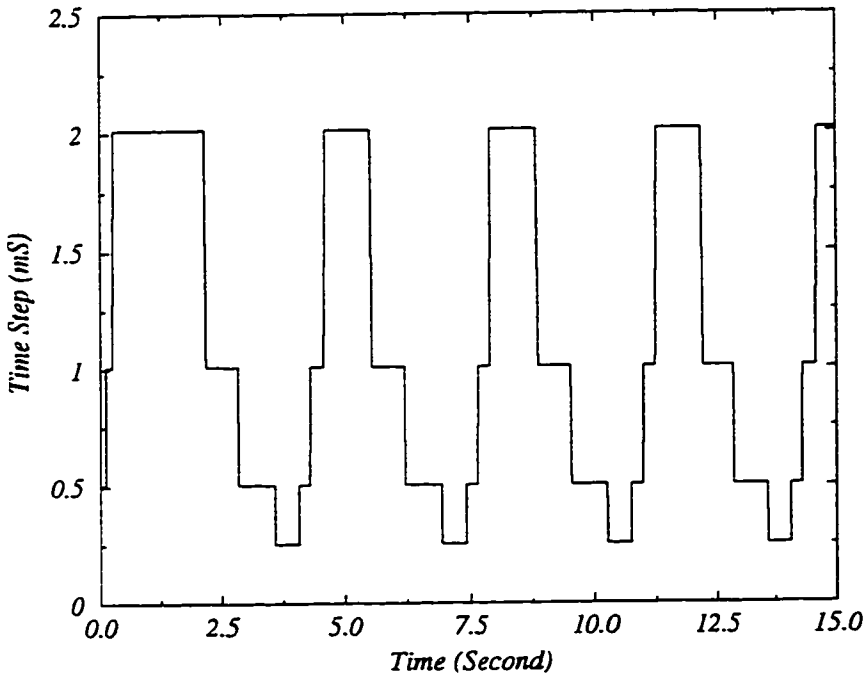

Figure C.6: The time-step variation in solving the Van Der Pol equation using the variable time-step TLM method.

IMAGE EVALUATION TEST TARGET (QA-3)

150mm

6"

APPLIED IMAGE . Inc
1653 East Main Street
Rochester, NY 14609 USA
Phone: 716/482-0300
Fax: 716/288-5989

© 1993, Applied Image, Inc., All Rights Reserved