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NOISE IN METAL-OXIDE-SEMICONDUCTOR
FIELD-EFFECT TRANSISTORS

by

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A THESIS

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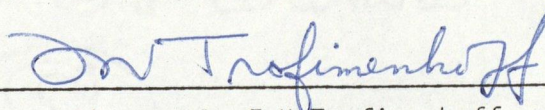
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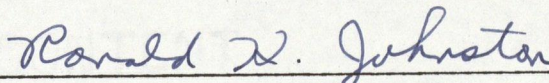
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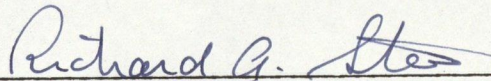
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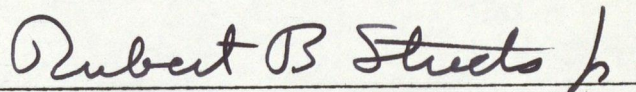
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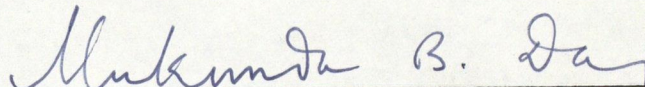
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ABSTRACT

The dc and small signal ac theories for the Weimer and bulk charge models of an n-channel enhancement MOS FET are reviewed to form a basis for noise calculations at low and moderately high frequencies. A circuit analysis approach is utilized to evaluate thermal noise characteristics for both models. Results are presented explicitly in terms of device parameters and bias conditions. The calculations of gate noise for the bulk charge model indicate an error in recently published results.

Low frequency generation-recombination noise and surface-state noise are analyzed using a unified approach to obtain the bias dependence of the noise. A method of modifying the gradual channel approximation to account for the saturated condition is described, and the results are used to prevent the noise calculations from diverging at pinch-off. The theory of noise due to carrier trapping by bulk oxide traps is improved and effects of the substrate on the noise are analyzed in detail. The analysis is applicable to a variety of situations.

A method of performing noise measurements using statistical analysis is described. The method facilitates the measurement of equivalent noise resistance quickly and accurately over a wide range of frequencies. The dependence of the shape and magnitude of the noise spectra on bias in four commercially available MOS FET's is studied using this technique. It is found that existing theories cannot explain

all the effects observed. In particular, the validity of the tunneling model appears questionable at this time.

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LIST OF SYMBOLS

B_e = equivalent resolution bandwidth for power spectra calculations

c = correlation coefficient, used in thermal noise calculations

c_n = probability per unit time that an electron will be captured by a trap

c_p = probability per unit time that a hole will be captured by a trap

C_{gs} = gate-source capacitance for the intrinsic MOS FET

C_{gst} = total gate-source capacitance, including strays

C_{gd} = gate-drain capacitance for the intrinsic MOS FET

C_{gdt} = total gate-drain capacitance, including strays

C_{gb} = gate-bulk 'capacitance'

C_{bg} = bulk-gate 'capacitance'

C_{bd} = bulk-drain capacitance

C_{bs} = bulk-source capacitance

} for the bulk charge model
of the MOS FET

$C_{gg} = C_{gs} + C_{gd} + C_{gb}$

C_{ox} = oxide capacitance per unit area

$C_o = C_{ox} L_z$, the total oxide capacitance

C_ℓ = gate-drain capacitance for the transistor of channel length x

C_r = gate-source capacitance for the transistor of channel length $(L-x)$

$C_t = C_{gst} + C_{gdt}$

d = maximum depth for surface state traps distributed uniformly over distance into the oxide at a single energy level

LIST OF SYMBOLS (CONT'D)

$d_t(E)$ = maximum depth of surface state traps at energy E

dR = resistance of a section of channel of length dx at a point x in the channel

dv_n = noise voltage generated in a length of channel dx at x

dv_{nd} = noise voltage at the drain resulting from a fluctuation at a point x in the channel

e_n = probability per unit time that an electron will be emitted by a trap

e_p = probability per unit time that a hole will be emitted by a trap

E_F = Fermi level of energy

E_n = quasi-Fermi level for electrons

E_p = quasi-Fermi level for holes

E_c = energy corresponding to the edge of the conduction band

E_v = energy corresponding to the edge of the valence band

$E_i = \frac{1}{2} \left[E_c + E_v - kT \ln \left(\frac{N_v}{N_c} \right) \right]$, where N_v and N_c are the densities of states in the valence and conduction bands, respectively

E_t = energy level of traps

f_m = maximum frequency of interest for noise measurements

f_o = noise factor cutoff frequency, given by $1/(2\pi R_g C_t)$

f_s = sampling frequency required for noise measurements

LIST OF SYMBOLS (CONT'D)

$f_t(V, E)$ = fraction of occupied traps at energy E

f_t = fraction of occupied traps for traps at a single energy level

$f_{tp}(V, E) = 1 - f_t(V, E)$

$f_{tp} = 1 - f_t$

Δf = equivalent noise bandwidth, analogous to B_e in the noise measurement system

F = noise factor

F_{min} = minimum noise factor, obtained by using $R_g = R_{gopt}$

g_m = gate transconductance

g_{ms} = gate transconductance with the drain in saturation

g_{mr} = gate transconductance for the transistor of channel length $(L-x)$

g_{mb} = substrate transconductance

g_{mbr} = substrate transconductance for the transistor of channel length $(L-x)$

g_o = output conductance

g_{ol} = output conductance for the transistor of channel length x

g_{or} = output conductance for the transistor of channel length $(L-x)$

$g(n)$ = generation rate for electrons

$G(f)$ = spectral density of a single time constant relaxation process

$G_I(f)$ = power spectral density of the short-circuit noise current at the drain

LIST OF SYMBOLS (CONT'D)

$G_V(f)$ = power spectral density of the open circuit noise voltage at the drain

\hbar = Plank's constant divided by 2π

I_d = direct drain current

I = total drain current, composed of a dc portion and a fluctuating component

$\Delta(\delta I_d)$ = incremental fluctuation in I_d

$\overline{i_d^2}$ = mean square value of the short circuit thermal noise current at the drain

$\overline{i_{dt}^2}$ = mean square value of the total noise current at the drain

$\overline{i_g^2}$ = mean square value of the short circuit thermal noise current at the gate

$\overline{i_g^* i_d}$ = term representing the cross correlation between the gate and drain noise currents

$\overline{i_{gR}^2}$ = mean square value of the noise current generator associated with thermal noise of the gate resistance

R_g

$J(x,y)$ = electron current density in the channel

k = Boltzmann's constant

K_o = decay constant associated with carrier tunneling in the oxide

L = metallurgical channel length

L_e = position in the channel at which the depletion theory matches with the gradual channel approximation, in the pinch-off calculations

LIST OF SYMBOLS (CONT'D)

- L_d, L'_d = Debye length and modified Debye length,
respectively
- m^* = effective electron mass
- n = electron density
- n_o = equilibrium density of electrons
- δn = deviation in the electron density from equilibrium
- δn_o = deviation in the electron density from equilibrium
at time $t = 0$
- n_i = density of electrons in the conduction band for
intrinsic material
- n_l = density of electrons in the conduction band when
the trap energy E_t corresponds to E_n
- n_s = electron density at the interface
- n_{os} = electron density at the interface at the source
- n_t = density of occupied traps in the depletion region
in the substrate
- n_{ts} = density of occupied traps in the oxide
- $\delta n_t, \delta n_{ts}$ = fluctuations in n_t and n_{ts} , respectively
- N = total number of data samples used for noise
measurements
- N_a = acceptor impurity density
- N_d = donor impurity density
- N_o = trap density for a uniform distribution of traps
in the oxide
- N_t = trap density in the depletion region
- N_s = trap density at the interface

LIST OF SYMBOLS (CONT'D)

$N(y)$ = trap density as a function of distance into the oxide at a single energy level

$N_t(E)$ = trap concentration per unit volume per electron volt in the oxide

$N_{ss}(E)$ = trap concentration per unit volume per electron volt for a uniform distribution of traps over energy in the oxide

N_T = effective trap density for the case of traps distributed in energy around the electron quasi-Fermi level

p = hole density

p_0 = equilibrium density of holes

p_1 = density of holes in the valence band when the trap energy E_t coincides with E_p

p_s = hole density at the interface

$P(n)$ = probability distribution function for electrons

q = magnitude of the electronic charge

Q_B = bulk charge

$\Delta(\delta Q_B)$ = incremental fluctuation in Q_B

Q_n = inversion charge at a point x in the channel

$\Delta(\delta Q_n)$ = incremental fluctuation in Q_n

Q_{ns} = value of Q_n at the source

Q_{n1} = value of Q_n at $x = x_1$

Q_{n2} = value of Q_n at $x = x_2$

Q_{ne} = value of Q_n at $x = L_e$

Q_{nd} = value of Q_n at the drain

Q_g = gate charge

per
unit
area*

*It should be noted that the terms 'charge' and 'charge per unit area' are used interchangeably throughout the text.

LIST OF SYMBOLS (CONT'D)

Q'_s	= charge induced in the semiconductor by charges trapped in the oxide	} per unit area*
$-Q'_{ss}$	= equivalent charge placed in the oxide at the oxide semiconductor interface that induces charge Q'_s in the semiconductor	
Q''_{ss}	= true interface charge	
Q_{ss}	= $Q'_{ss} + Q''_{ss}$	
Q	= total inversion charge, composed of a dc portion and a fluctuating component	
$r(n)$	= recombination rate for electrons	
R_g	= external resistance in series with the gate lead of the device	
R_{gopt}	= value of R_g that minimizes the noise factor	
R_n	= equivalent noise resistance, evaluated with the input ac short circuited	
R_{ns}	= value of R_n at pinch-off	
R_ℓ	= resistance seen looking into the drain of the transistor of channel length x	
R_r	= resistance seen looking into the source of the transistor of channel length $(L-x)$	
R_o	= output resistance	
$R(\tau)$	= autocorrelation function used for spectral density calculations	
T	= absolute temperature in degrees Kelvin	

*It should be noted that the terms 'charge' and 'charge per unit area' are used interchangeably throughout the text.

LIST OF SYMBOLS (CONT'D)

- T_{ox} = oxide thickness
- T_r = record length required for noise measurements
- $U = \frac{q}{kT} (\Psi - \phi)$
- U_B, U_s = values of U in the bulk and at the surface, respectively
- $U' = \frac{q}{kT} \left[\Psi - \frac{1}{2}(\phi_p + \phi_n) \right]$
- U'_B, U'_s = values of U' in the bulk and at the surface, respectively.
- v = gate-channel potential at any point x in the channel
- v_s = value of v at the source
- v_d = value of v at the drain
- v_{gs} = small-signal gate-source voltage
- V = channel potential with respect to the source at a point x in the channel
- V_1 = value of V at $x = x_1$
- V_2 = value of V at $x = x_2$
- V_e = value of V at $x = L_e$
- V_t = total channel potential, composed of a dc portion and a fluctuating component
- V_T = threshold voltage
- V_p = pinch-off voltage
- V_B = equivalent bulk charge voltage, defined by equation (2.50)
- V_{bs} = direct bulk-source voltage
- V_{gs} = direct gate-source voltage
- V_{gs2} = direct gate-source voltage for the transistor of

LIST OF SYMBOLS (CONT'D)

channel length (L-x)

V_{ds} = direct drain-source voltage

V_{ds2} = direct drain-source voltage for the transistor of
channel length (L-x)

$$V_g' = V_{gs} - V_T$$

$$V_{ss} = Q_{ss}/C_{ox}$$

V_{ox} = potential of the gate with respect to the interface
with no external bias

V_{ox}' = potential of the gate with respect to the interface
with external bias

V_d = potential corresponding to the depletion width ξ_{max}
used in the pinch-off calculations

$$V_{dt} = V_d - \psi_o$$

$$V_{dst} = V_{ds} - \psi_o$$

$$V_{dl} = V_{ds} - V_e$$

$\Delta(\delta V)$ = incremental fluctuation in V

W = height of the energy barrier at the interface used
for tunneling calculations

W_o = energy of an electron impinging upon the barrier

W_m = work function of the metal gate electrode

W_{sc} = work function of the semiconductor substrate

W_{bs} = energy corresponding to the potential of the bulk
with respect to the surface with no external bias

W_{bs}' = energy corresponding to the potential of the bulk
with respect to the surface with external bias

LIST OF SYMBOLS (CONT'D)

- W_{ox} = energy corresponding to the potential of the gate
with respect to the interface with no external bias
- \hat{W}_{ox} = energy corresponding to the potential of the gate
with respect to the interface with external bias
- x = distance coordinate, measured along the channel from
the source
- x_1, x_2 = positions along the channel which define the edges
of the Δx strip used for noise calculations
- y = distance coordinate, measured from the interface
into the oxide and the substrate
- \hat{y}_d = depletion width at any point x along the channel,
with no external bias
- y_d = depletion width at any point x along the channel,
with external bias
- y_i = distance from the interface into the semiconductor
where $n = n_i$
- $\Delta(\delta y_d)$ = incremental fluctuation in y_d
- z = device breadth
- $\phi = -E_F/q$, the quasi-Fermi potential
- ϕ_{ms} = metal-semiconductor work function difference
- ϕ_n = quasi-Fermi potential for electrons
- ϕ_p = quasi-Fermi potential for holes
- $\phi_F = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right)$
- ϕ_{BS} = potential of the bulk with respect to the surface
with no external bias

LIST OF SYMBOLS (CONT'D)

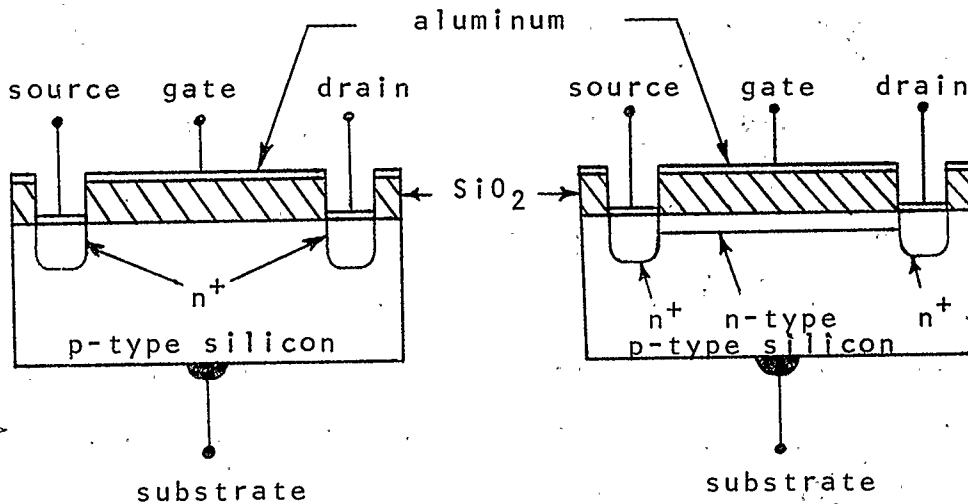
- ϕ_{BS} = potential of the bulk with respect to the surface
with external bias
- ϕ_{BS0} = potential of the bulk with respect to the surface
when $V_{gs} = V_T$
- ϵ_s = permittivity of the semiconductor substrate
- ϵ_{ox} = permittivity of the oxide insulator
- μ_n = electron mobility
- μ_b = bulk mobility
- μ_{eff} = effective mobility at the surface.
- ω = radian frequency
- ω_o = lower corner frequency at which the noise spectra
level off
- $\gamma = c_n/c_p$
- ν = number of degrees of freedom used for noise spectra
calculations
- $\alpha = \frac{2}{\hbar} \sqrt{2m^*W}$
- η = factor that determines the shape of $N(y)$, the trap
density profile in the oxide
- ζ = integral defined by (5.99)
- T = integral defined by (C.44)
- $\xi = L-x$, position in the channel referred to the drain
- ξ_{max} = depletion width corresponding to the potential V_d
- χ = electron affinity, the energy required to remove an
electron from the bottom of the conduction band to
a point just outside the material
- Ψ = electrostatic potential

LIST OF SYMBOLS (CONT'D)

- Ψ_{bm} = potential of the bulk with respect to the metal
- $\Delta(\delta\Psi_{bm})$ = incremental fluctuation in Ψ_{bm}
- Ψ_o = equilibrium contact potential
- $\theta = \frac{I_d L}{\mu_n z C_{ox}}$
- θ_1 = a function of voltage defined by (4.75)
- θ_2 = a function of voltage defined by (4.78)
- $\Gamma = Q_n / C_{ox}$
- $\Gamma_d = Q_{nd} / C_{ox}$
- \mathcal{E}_y = normal electric field at the surface
- \mathcal{E}_x = electric field along the channel
- $\Delta\Lambda$ = elemental volume element in the oxide or in the substrate
- τ_o = relaxation time constant determining the return in carrier density from a small deviation to equilibrium
- τ_t = time constant for traps located in the substrate depletion region
- τ = time constant for traps located in the oxide
- τ_s = time constant for traps located at the interface

1. INTRODUCTION

The basic metal-oxide-semiconductor FET structures shown in Fig. 1.1 were first proposed by D. Kahng¹ and M.M. Atalla² in 1960.



(a) Enhancement MOS FET.

(b) Depletion MOS FET.

Fig. 1.1 Basic MOS FET structures.

The enhancement FET is constructed from a uniformly-doped wafer of p-type silicon, known as the substrate. The surface of the wafer is polished and thermally oxidized to form an insulating layer of silicon dioxide. The oxide is etched to allow n-type impurities to be diffused into the p-type substrate, forming heavily-doped n^+ source and drain regions as shown. A layer of aluminum is then deposited over the oxide between the source and drain contacts to form the gate, and ohmic contacts are made to the source, drain and substrate to complete the device.

In the normal mode of operation the bias voltages are connected as shown in Fig. 1.2.

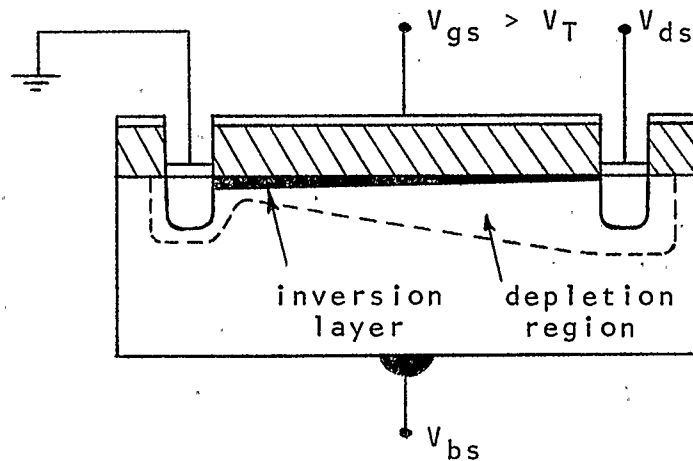


Fig. 1.2 The MOS FET with bias voltages applied.

With no bias between gate and source, drain current cannot flow since the application of a bias voltage between drain and source results in either the source-substrate or drain-substrate p-n junction becoming reverse biased. The application of a negative voltage from gate to source causes an accumulation of holes at the oxide-semiconductor interface and again no current can flow. However, if the gate voltage is made positive, holes are depleted from the interface region and eventually an inversion layer of electrons will appear as shown in Fig. 1.2. The gate voltage at which this occurs is designated the threshold voltage. The inversion layer has a shielding action so that any further increase in gate voltage past threshold results in an increase in the inversion charge density, and the depletion region width remains

approximately constant at any point in the channel once inversion occurs.

The inversion layer is in contact with the n^+ source and drain regions, allowing drain current to flow. Since there is no substrate current, the substrate is an equipotential region. The potential along the oxide-semiconductor interface varies from source to drain, and as a result the depletion region width increases from source to drain, while the inversion charge decreases. For any particular gate voltage above threshold, the drain voltage can be increased until the inversion charge disappears at the drain, and the drain current saturates. The drain voltage at which this occurs is known as the pinch-off voltage, and the FET is said to be pinched off or saturated at this point. As the gate voltage is increased, the pinch-off voltage increases, since the gate-to-drain voltage required to sustain inversion is a constant for any particular substrate bias. This results in a family of curves which resemble those for the junction-gate FET, as shown in Fig. 1.3.

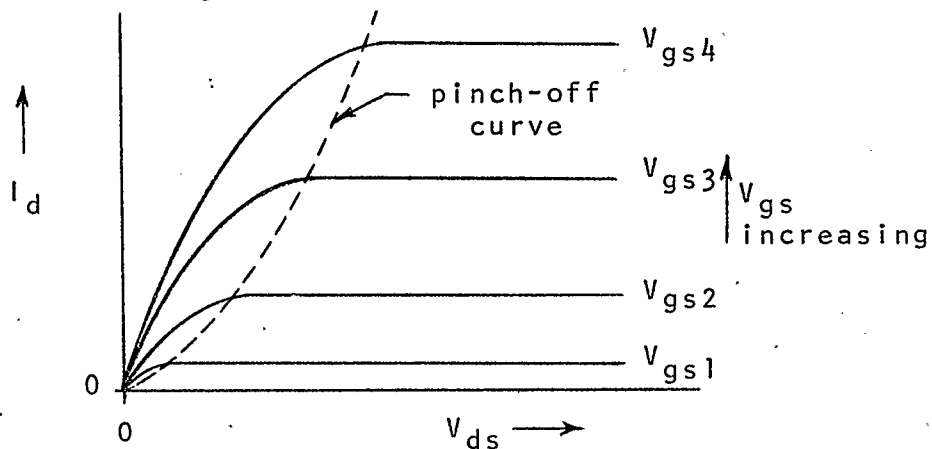


Fig. 1.3 DC characteristics of the MOS FET.

A p-channel enhancement MOS FET is constructed in an identical manner to the n-channel device just described, except that an n-type silicon substrate and p^+ source and drain diffusions are used.

The depletion FET shown in Fig. 1.1(b) is slightly different in that an n-type region is diffused into the substrate before growing the insulating oxide layer. This allows drain current to flow with no gate bias. A positive gate bias causes an accumulation of electrons, increasing the drain current, while a negative gate bias depletes the n-type region of electrons, decreasing the drain current. A large negative gate bias will deplete the channel completely, and the device cuts off, in contrast to the enhancement MOS FET, which is cut off until threshold is exceeded.

In recent years, semiconductor surface technology has advanced to the point where it is possible to grow very clean oxides, and as a result the MOS FET has become an important device for use in integrated circuit design. It is often used as a first stage in integrated circuit amplifiers, so that the noise performance of the device is of major concern.

The basic MOS FET concepts were first proposed in detail by Kahng¹ and Atalla² in 1960. The operation of the enhancement-type MOS FET was described in an unpublished report by Ihantola³ in 1961, and later published by Ihantola and Moll.⁴ This analysis neglected interface states, fixed charges in the insulator, and the metal-insulator-semiconductor

work function. However, the voltage-dependent bulk charge in the depletion region was included explicitly. A description of the thin-film insulated-gate transistor was given by Weimer⁵ in 1962, and an analysis including the initial charge in the semiconductor was published by Borken and Weimer⁶ in 1963. A year later, Sah⁷ published a theoretical description of the device, based on the mode of operation conceived in Kahng's¹ patent, using the same approach as Ihantola and Moll.⁴ The familiar 'gradual channel' approximation of Shockley⁸ was used. The theory was presented with the assumption of constant surface and bulk charge, and constant surface mobility. An equivalent circuit was derived and basic parameters were related to the materials and geometry of the device. Further work dealt with post pinch-off operation,⁹⁻¹⁴ and high field effects,⁹⁻¹¹ as well as the effects of substrate resistivity.^{15,17,36}

Small signal analyses valid at moderately high frequencies were performed for the Weimer model by Sah⁷ and Das.¹⁶ More detailed calculations treating the transistor as a non-uniform active transmission line were subsequently carried out for the Weimer model.^{18,19,20,21} The effects of the fixed bulk charge on the dc and low frequency characteristics were presented in detail by Sah and Pao.¹⁷ However, the small-signal equivalent circuit for the bulk charge model was left incomplete. Since the small-signal equivalent circuits for the pre-pinch-off case are essential to the calculation of the noise performance of the device, a portion of

this work is devoted to the review of the equivalent circuit for the Weimer model and the development of the equivalent circuit for the bulk charge model in the pre-pinch-off mode.

The first quantitative theory of noise in MOS devices was published by Jordan and Jordan²² in 1965. Subsequent work dealt with thermal noise calculations utilizing a transmission line model of the channel,²³ excess noise calculations at very high frequencies,^{52,53} and with the effects of substrate doping on the thermal noise.^{24,25} A number of authors^{26-31,37} have attempted to predict the low frequency noise mechanisms which give rise to the $1/f$ type noise observed at audio frequencies. In most cases the results are only valid for moderate drain voltages, the equivalent noise resistance approaching infinity as the pinch-off voltage is reached. This work uses an equivalent circuit approach that yields identical results with those obtained previously for thermal noise for both the Weimer model and the bulk charge model. The technique is used to extend the calculations to include gate noise and correlation for the bulk charge model. The results are presented in a form convenient for comparison with experimental measurements. Low-frequency generation-recombination noise and surface state noise are analyzed in detail, and a method is presented for preventing the noise resistance from diverging at pinch-off.

A fast method of measuring the spectral density of the noise is described. The equipment used allows measurements to be made from 2Hz to 10kHz, quickly and accurately.

Measurements are performed on a number of enhancement type MOS FET's with both p and n-type silicon substrates, in order to observe variations in the noise spectra as gate and drain bias conditions are altered.

2. DC THEORY

2.1 THE WEIMER MODEL

The simplest model of the MOS FET neglects the bulk charge variation that was described by Ihantola.³ This assumption yields a simple theory that predicts the general shape of the experimental characteristics, although it does not account for some of the fine structure observed. The theory is reviewed briefly here to serve as a basis for the small-signal analysis to follow.

Utilizing the schematic representation shown in Fig. 2.1,

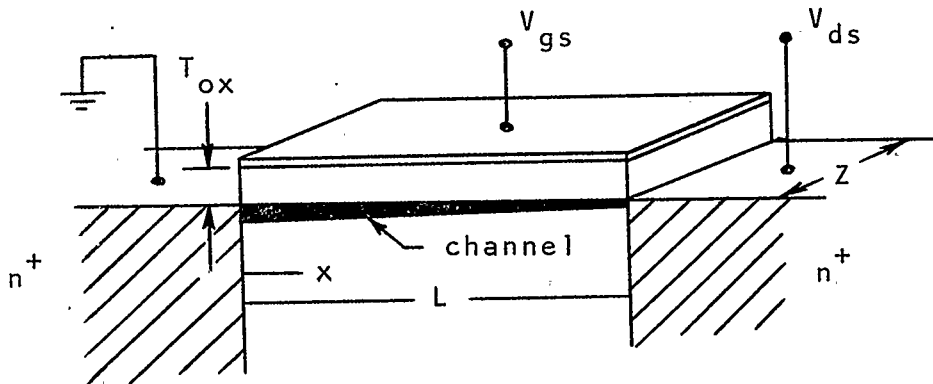


Fig. 2.1 Schematic representation of the MOS structure.

it can be shown⁶ that the drain current I_d is given by

$$I_d = -\mu_n \frac{\epsilon_{ox} z}{T_{ox}} v \frac{dv}{dx} \quad (2.1)$$

where v = gate-to-channel potential at any point x in the channel

μ_n = electron mobility in the channel

ϵ_{ox} = permittivity of the insulating layer

T_{ox} = oxide thickness

z = device breadth

x = distance co-ordinate, defined in Fig. 2.1.

At the source,

$$v_s = (V_{gs} - V_T) \quad (2.2)$$

and at the drain

$$v_d = (V_{gs} - V_T) - V_{ds} \quad (2.3)$$

where V_{gs}, V_{ds} = gate-source and drain-source bias voltages respectively, and

V_T = threshold voltage, positive for an n-channel enhancement device.

Integration of (2.1) from $x = 0$ to $x = L$ then yields

$$I_d = \frac{\mu_n z C_{ox}}{L} \left[V_{ds} (V_{gs} - V_T) - \frac{V_{ds}^2}{2} \right] \quad (2.4)$$

where $C_{ox} = \frac{\epsilon_{ox}}{T_{ox}}$.

The transconductance g_m and output conductance g_o are easily obtained from (2.4) by taking the appropriate partial derivatives, so that

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{\mu_n z C_{ox}}{L} V_{ds} \quad (2.5)$$

and

$$g_o = \frac{\partial I_d}{\partial V_{ds}} = \frac{\mu_n z C_{ox}}{L} \left[(V_{gs} - V_T) - V_{ds} \right] \quad (2.6)$$

Then at pinch-off, $V_{ds} = V_{gs} - V_T$,

$$g_m = g_{ms} = \frac{\mu_n z C_{ox}}{L} (V_{gs} - V_T), \quad (2.7)$$

and

$$g_o = 0. \quad (2.8)$$

These equations lead to a zero frequency small signal equivalent circuit of the form shown in Fig. 2.2.

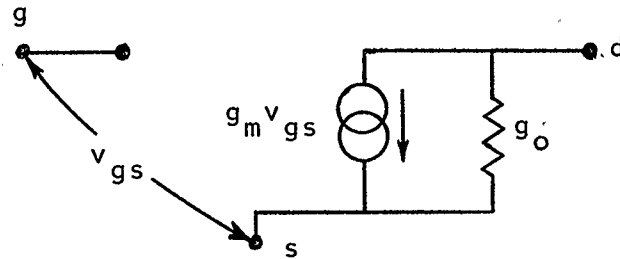


Fig. 2.2 Zero frequency small signal equivalent circuit for the MOS FET.

2.2 THE BULK CHARGE MODEL

The spatially and applied voltage dependent bulk charge in the channel due to the depletion of majority carriers was included explicitly by Ithantola³ in his original analysis of the MOS FET. Sah and Pao¹⁷ improved the analysis by differentiating between the surface potential and the quasi-Fermi potential along the channel, and by including the effects of oxide charge and interface charges. The dc theory is derived in the following section using a similar approach in order to establish the notation and indicate the approximations involved.

2.2.1 The MOS Capacitor at Equilibrium

For a p-type silicon bar with a 'perfect' surface, the energy band diagram will appear as shown in Fig. 2.3(a). A perfect surface is defined as one whose properties are

identical to those in the bulk, so that no band bending occurs, as shown.

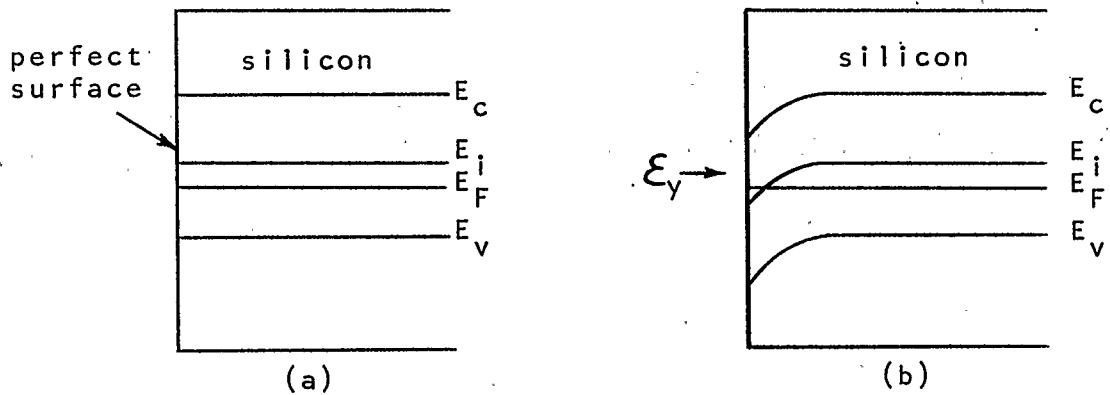


Fig. 2.3 (a) Band configuration at a perfect surface
(b) Energy band variations near the surface due to an externally applied field.

Using the well-known quasi-Fermi or imref notation of Shockley (1949), the hole and electron concentrations may be expressed in terms of electrostatic potentials as

$$n = n_i \exp \left[\frac{q}{kT} (\Psi - \phi) \right] \quad (2.9)$$

$$p = n_i \exp \left[\frac{q}{kT} (\phi - \Psi) \right] \quad (2.10)$$

where n = electron density

p = hole density

n_i = intrinsic concentration per unit volume

q = magnitude of the electronic charge

k = Boltzmann's constant

T = absolute temperature

$\phi = -E_F/q$, the Fermi potential

E_F = Fermi level of energy

$\Psi = -E_i/q$, the electrostatic potential.

Now $p > n$ in the bulk, so that $\Psi - \phi = -(E_i - E_F)/q$ must be negative which implies that E_F is below the midgap position as indicated in Fig. 2.3.

With an electric field directed toward the surface, holes are depleted from the surface region so that $(E_i - E_F)$ decreases and may even become negative. This indicates an increase in the electron concentration near the surface, and the bands are bent downward as shown in Fig. 2.3(b). It should be noted that the Fermi level remains constant as the system is in equilibrium.

With the basic band structure established, it is now possible to analyze the metal-oxide-semiconductor capacitor system shown in Fig. 2.4.

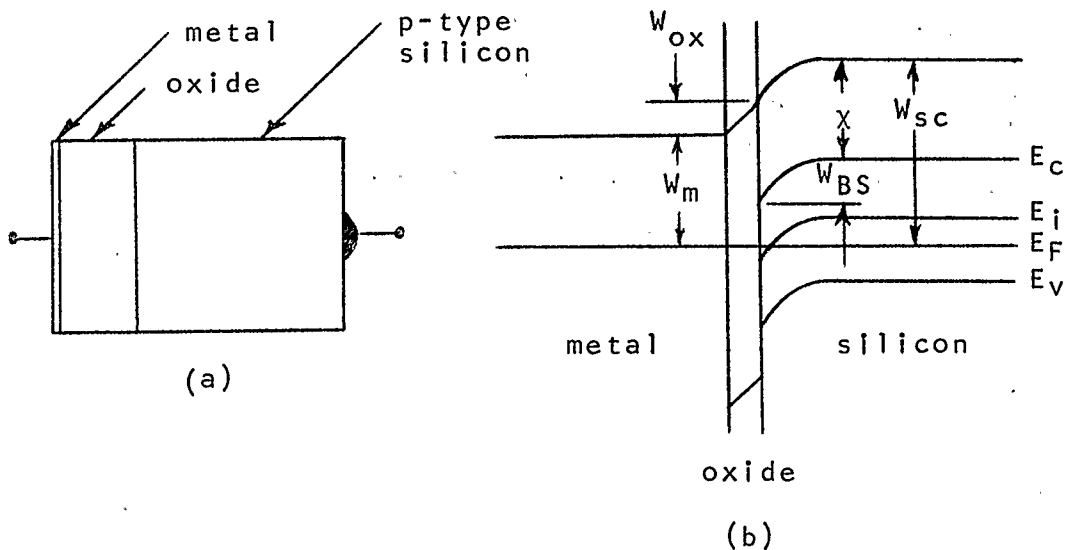


Fig. 2.4 (a) The basic MOS capacitor.
(b) Detailed band structure at equilibrium.

The principle of detailed balance requires that the Fermi levels correspond to the same potential, since an energy transfer will occur without any work being done if this is not the case. The Fermi level in the metal is well defined. However, its position in the semiconductor depends on the doping level. Rather than trying to define the position of E_F in the semiconductor, an 'electron affinity', χ , is defined as the energy required to remove an electron from the bottom of the conduction band to a point just outside the semiconductor. The electron affinity is independent of the electrostatic potential. It takes the same amount of energy to remove an electron from the Fermi level to a point outside the metal as it does to take the electron into the semiconductor at constant energy, remove it through the boundary of the semiconductor and move it along the boundary to the point in question. This leads to

$$W_m + W_{ox} = \chi + (E_c - E_F) + W_{BS} \quad (2.11)$$

where W_{BS} = energy corresponding to the potential difference between the bulk and the surface

$\chi + (E_c - E_F) = W_{sc}$, the semiconductor work function.

In terms of potential, the metal-semiconductor potential difference is written as

$$\phi_{ms}' = \phi_m - \phi_{sc} = \phi_{BS} - V_{ox}. \quad (2.12)$$

Equation (2.12) can be taken as the definition of ϕ_{ms}' .

2.2.2 The MOS Capacitor With External Bias

With the application of an external bias, the energy band diagram is modified as shown in Fig. 2.5.

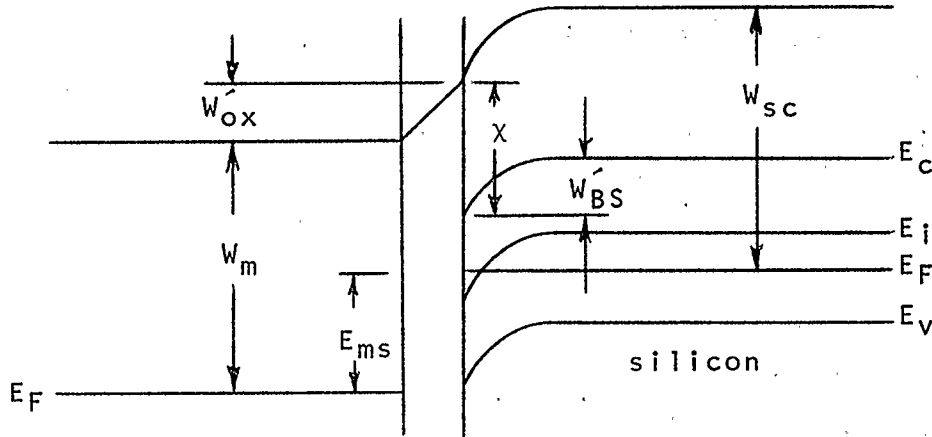


Fig. 2.5 The energy band diagram for an MOS capacitor with external bias.

The ohmic contact to the silicon is a region of high recombination, so that $\phi_n = \phi_p = \phi$ at the contact. Since there can be no current flow in the semiconductor, $\frac{d\phi_p}{dx} = \frac{d\phi_n}{dx} = 0$. Thus $\phi_n = \phi_p = \phi$ is constant, and $\phi = -E_F/q$ implies that E_F is also constant. The Fermi levels are merely shifted by an amount E_{ms} as shown. This leads immediately to

$$\phi'_{ms} - \phi'_{BS} = V_{msc} - V'_{ox} \quad (2.13)$$

where V_{msc} = applied voltage, metal-to-semiconductor.

2.2.3 Effect of Charge in the Oxide

The oxide growth phase of the MOS fabrication process takes place at high temperatures, and as a result it is difficult to prevent impurities from getting into the oxide.

This results in a distribution of charges throughout the insulating layer as shown in Fig. 2.6.

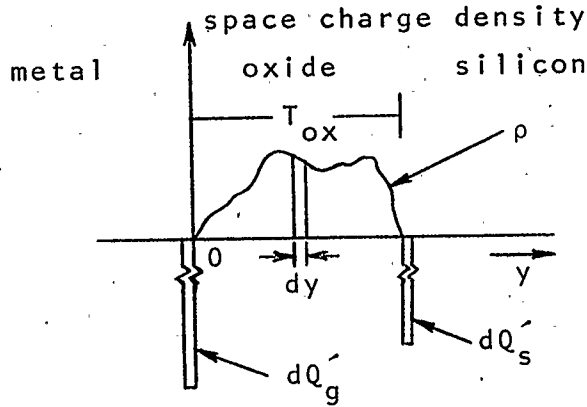


Fig. 2.6 Impurity charge distribution in the oxide.

If the metal and semiconductor are shorted together, taking moments about $y = 0$ yields

$$y\rho dy + T_{ox}dQ'_s = 0 \quad (2.14)$$

so that

$$Q'_s = -\int_0^{T_{ox}} \frac{y}{T_{ox}} \rho dy. \quad (2.15)$$

Taking moments about $y = T_{ox}$, it is easy to show that

$$Q'_g = -\int_0^{T_{ox}} \frac{(T_{ox}-y)}{T_{ox}} \rho dy. \quad (2.16)$$

An equivalent surface charge of $Q'_{ss} = -Q'_s$ placed in the oxide at the oxide-semiconductor interface will then induce charge Q'_s in the semiconductor. If, in addition, charges Q'_{ss} are present at the silicon dioxide-silicon interface, then the total equivalent charge Q_{ss} at the interface is given by

$$Q_{ss} = Q_{ss}' + Q_{ss}'' \quad (2.17)$$

The charge distribution in an induced n-channel MOS capacitor may thus be represented as shown in Fig. 2.7.

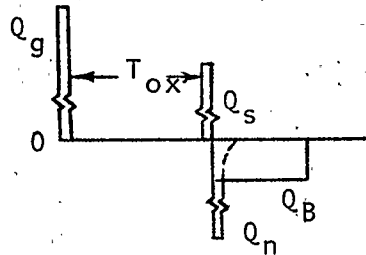


Fig. 2.7 Charge distribution for an inverted MOS capacitor.

It should be noted that Q_n is the induced electron charge at the oxide-semiconductor interface, and Q_B is the charge corresponding to the bared acceptor ion concentration in the depletion region formed in the semiconductor.

2.2.4 Depletion Width Calculations

The exact dependence of the depletion width on the gate voltage under post-inversion conditions is complicated. However, for conditions of heavy inversion, the inversion layer supplies any increase in charge necessary to absorb any increase in surface field strength, and the width of the depletion region becomes almost independent of the voltage.⁵⁹ Using this approximation, a calculation of the depletion width may be performed directly.

The onset of inversion is somewhat arbitrarily defined as the point where $n = N_a$.⁴ If the bulk to surface potential ϕ_{BS} is known prior to inversion, the depletion width

can be computed using Poisson's equation in the form

$$\nabla^2 U = \frac{1}{L_d^2} \left[\sinh U + \frac{N_a}{2n_i} \right] \quad (2.18)$$

where ∇^2 = the Laplacian

L_d = Debye length

$$U = \frac{q}{kT} (\Psi - \phi).$$

Deep in the bulk $\nabla^2 U = 0$, so that

$$U_B = \sinh^{-1} \left(\frac{N_a}{2n_i} \right). \quad (2.19)$$

At the surface,

$$n_s = N_a = n_i e^{U_s} \quad (2.20)$$

so that

$$U_s = \ln \left(\frac{N_a}{n_i} \right). \quad (2.21)$$

Then the surface potential when $n_s = N_a$ is given by

$$\phi_{BS0} = \frac{kT}{q} (U_B - U_s) \approx - \frac{2kT}{q} \ln \left(\frac{N_a}{n_i} \right). \quad (2.22)$$

In addition, if the inversion charge is much smaller than the depletion charge, then the solution of

$$\nabla^2 \Psi = \frac{-\rho}{\epsilon_s}$$

where Ψ = electrostatic potential

$$\rho = -qN_a$$

ϵ_s = semiconductor permittivity

with $\frac{d\Psi}{dy} = 0$ at $y = y_d'$ as boundary condition yields

$$\phi_{BS0} = \frac{-qN_a (\gamma_d')^2}{2\epsilon_s} \quad (2.23)$$

Equating (2.22) and (2.23) then gives

$$\gamma_d' = \left[\frac{4\epsilon_s kT}{q^2 N_a} \ln \left(\frac{N_a}{n_i} \right) \right]^{\frac{1}{2}} \quad (2.24)$$

2.2.5 Surface Charge Calculations

The exact solution for the charge distribution in the semiconductor would require a numerical integration. However, using the above approximation for the depletion width, it is possible to obtain a useful expression for the inversion charge in terms of bias voltages and device parameters.

The total charge in the semiconductor to the right of the surface, Q_s , is made up of the channel charge Q_n and the depletion charge Q_B .

$$Q_s = Q_n + Q_B \quad (2.25)$$

The end of the inversion layer is again somewhat arbitrarily defined as the point where $p = n$, so that

$$n_i e^U = n_i e^{-U} \quad (2.26)$$

or $U = 0$ at this point. The inversion charge may then be calculated immediately by integrating from the surface to $U = 0$, so that

$$Q_n = -q \int_{U=U_s}^{U=0} n \left(\frac{dy}{dU} \right) dU \quad (2.27)$$

The gate charge Q_g and oxide charge both act to induce charge Q_s , so that

$$Q_g + Q_{ss} + Q_s = 0 \quad (2.28)$$

where $Q_s = Q_n + Q_B$ from (2.25).

It can be shown⁵⁹ that once inversion occurs, the depletion width does not increase significantly with increasing gate voltage, and the bulk-to-surface potential remains approximately at its value given by (2.22). The inversion charge can be obtained from

$$Q_n = -Q_{ss} - Q_B - Q_g \quad (2.29)$$

where $Q_B = -qN_a y_d$

$$Q_g = C_{ox} V_{ox}$$

and V_{ox} is given by (2.13), so that Q_n may be written as

$$Q_n = -Q_{ss} + qN_a \left[\frac{4\epsilon_s kT}{q^2 N_a} \ln \left(\frac{N_a}{n_i} \right) \right]^{\frac{1}{2}} - C_{ox} (V_{msc} + \phi_{BS} - \phi_{ms}). \quad (2.30)$$

where V_{msc} is the applied voltage of the metal with respect to the semiconductor.

2.2.6 Addition of a Source Contact

The addition of an n^+ source region to the MOS capacitor yields the three-terminal device shown in Fig. 2.8.

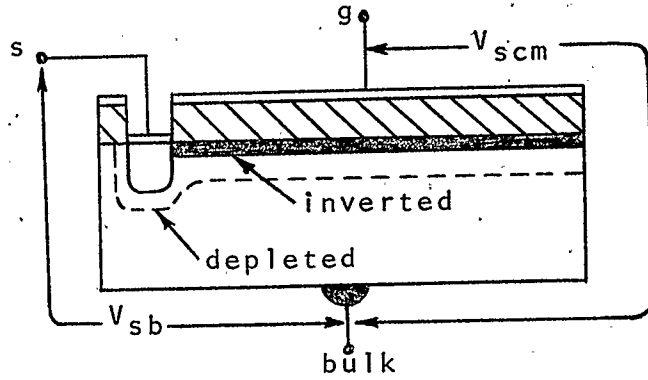


Fig. 2.8. The MOS capacitor with a source contact.

Since there is no current flow along the induced channel, the quasi-Fermi level ϕ_n for electrons remains constant in that direction. As well, since there is negligible current in the substrate, the quasi-Fermi level for holes ϕ_p remains approximately constant in the semiconductor. Then ϕ_p and ϕ_n are separated by the bulk-to-source bias V_{bs} ,^{7,57} so that

$$\phi_p - \phi_n = V_{bs}. \quad (2.31)$$

Utilizing

$$p = n_i e^{\frac{q}{kT}(\phi_p - \psi)} \quad (2.32)$$

$$n = n_i e^{\frac{q}{kT}(\psi - \phi_n)} \quad (2.33)$$

it can be shown that

$$\nabla^2 U' = \frac{1}{(L_d')^2} \left[\sinh U' + \frac{N_a}{2n_i} e^{\left(\frac{q}{2kT} V_{sb}\right)} \right] \quad (2.34)$$

where

$$U' = \frac{q}{kT} \left[\psi - \frac{1}{2}(\phi_p + \phi_n) \right]$$

and

$$L_d' = \left\{ \frac{kT\epsilon_s}{2q^2 n_i} \exp \left[\frac{q}{2kT} (\phi_n - \phi_p) \right] \right\}^{\frac{1}{2}}.$$

The condition $\nabla^2 U_B' = 0$ yields

$$U_B' = \frac{1}{2}(\phi_p + \phi_n - V_{sb}) - \frac{kT}{q} \ln \left(\frac{N_a}{n_i} \right) \quad (2.35)$$

and again defining inversion as the point where $n_s = N_a$, it can be shown that

$$\phi_{BS0}' = \psi_B - \psi_s = V_{bs} - \frac{2kT}{q} \ln \left(\frac{N_a}{n_i} \right). \quad (2.36)$$

Thus the depletion width and inversion charge are easily modified to include the effects of the source contact by substituting (2.36) for (2.22) in (2.23) and (2.29).

2.2.7 The Four-Terminal MOS FET

The dc equations for the three terminal device have now been obtained, and it is a simple matter to extend the calculations to include the four-terminal MOS FET shown in Fig. 2.9.

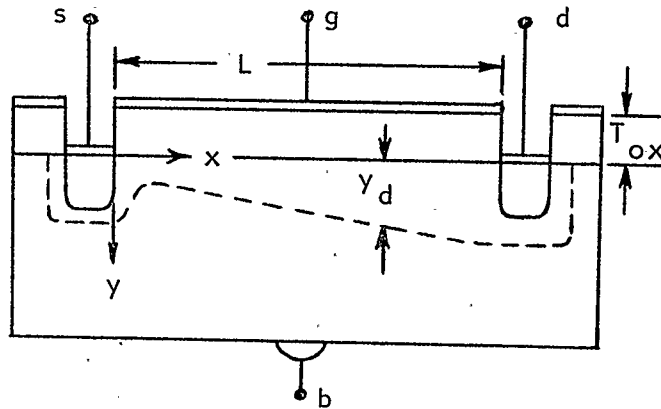


Fig. 2.9 Bulk charge model of the MOS FET.

In order to perform the analysis, the following assumptions are made:

1. Non-degenerate substrate doping.
2. Carrier mobility in the inversion layer is field-independent.
3. The substrate is thick.
4. The charge Q_{ss} is independent of the surface field.
5. Diffusion current in the channel is negligible compared to drift current.
6. Electron-hole generation and recombination in the channel is negligible.
7. The effects of source-substrate and drain-substrate reverse bias currents can be ignored.

The effect of the drain contact is easily included by considering the separation of the quasi-Fermi levels ϕ_n and ϕ_p along the channel. If the surface potential along the channel with respect to the origin of the co-ordinate system of Fig. 2.9 is denoted as V , then it can be shown^{7,58} that the electron quasi-Fermi level is separated from the hole quasi-Fermi level by an additional amount proportional to V at any point x in the channel. The inversion charge, from (2.30), is then written as

$$Q_n = -Q_{ss} + qN_a y_d - C_{ox}(V_{gs} - V + \phi'_{BS} - V_{bs} - \phi'_{ms}) \quad (2.37)$$

where $V_{gs} = V_{msc} + V_{bs}$, ϕ'_{BS} is the bulk to surface potential at the source, and the depletion region width y_d is found

from (2.24) to be

$$y_d \approx \left\{ \frac{2\epsilon_s}{qN_a} \left[V - V_{bs} + \frac{2kT}{q} \ln\left(\frac{N_a}{n_i}\right) \right] \right\}^{\frac{1}{2}}. \quad (2.38)$$

The drain current I_d may be obtained by integrating the electron current density $J(x,y)$ over the cross-sectional area of the channel, so that

$$I_d = z \int_0^{y_i} J(x,y) dy \quad (2.39)$$

where z is the device breadth and the integration is performed from the oxide-semiconductor interface to the edge of the inversion layer. From the transport equation, neglecting diffusion current in the channel,

$$J(x,y) = q\mu_n n \mathcal{E}_x \quad (2.40)$$

where μ_n = electron mobility

\mathcal{E}_x = electric field along the channel.

Then combining (2.39) and (2.40),

$$I_d = -\mu_n z \frac{dV}{dx} \int_0^{y_i} -qndy. \quad (2.41)$$

Noting that the integral in (2.41) is the inversion charge density defined by (2.37), the drain current can be expressed simply by

$$I_d = -Q_n \mu_n z \frac{dV}{dx}. \quad (2.42)$$

Integration from $x = 0$ to $x = L$ yields

$$I_d = \frac{\mu_n z C_{ox}}{L} \left\{ V_{ds} (V_{gs} - V_{bs} + \phi_{BS}' + V_{ss} - \phi_{ms}') - \frac{V_{ds}^2}{2} - \frac{2}{3} \sqrt{\frac{2qN_a \epsilon_s}{C_{ox}^2}} \left[(V_{ds} - \phi_{BS}')^{\frac{3}{2}} - (-\phi_{BS}')^{\frac{3}{2}} \right] \right\} \quad (2.43)$$

where $C_{ox} = \epsilon_{ox}/T_{ox}$ as for the Weimer model, and

$V_{ss} = Q_{ss}/C_{ox}$. The threshold voltage can be obtained either by letting V_{ds} become very small and examining the gate voltage at which the drain current goes to zero, or by letting the inversion charge go to zero. Both methods give

$$V_T = V_{bs} - \phi_{BS}' - V_{ss} + \phi_{ms}' + \left[\frac{2qN_a \epsilon_s}{C_{ox}^2} (-\phi_{BS}') \right]^{\frac{1}{2}}. \quad (2.44)$$

The pinch-off voltage can be found either by calculating the value of $V = V_{ds}$ at the drain required to reduce Q_n to zero for a specific gate voltage, or by finding the value of V_{ds} at which I_d reaches a maximum. Again both methods give

$$V_p = V_{gs} - V_{bs} + \phi_{BS}' + V_{ss} - \phi_{ms}' + \frac{qN_a \epsilon_s}{C_{ox}^2} \left\{ 1 - \left[1 + \frac{2C_{ox}^2}{qN_a \epsilon_s} (V_{gs} - V_{bs} + V_{ss} - \phi_{ms}') \right]^{\frac{1}{2}} \right\}. \quad (2.45)$$

The gate transconductance g_m and substrate transconductance g_{mb} are calculated from the expression for the drain current, so that

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{\mu_n z C_{ox}}{L} V_{ds} \quad (2.46)$$

$$g_{mb} = \frac{\partial I_d}{\partial V_{bs}} = \frac{\mu_n z C_{ox}}{L} \sqrt{\frac{2qN_a \epsilon_s}{C_{ox}^2}} \left[(V_{ds} - \phi_{BS}')^{\frac{1}{2}} - (-\phi_{BS}')^{\frac{1}{2}} \right]. \quad (2.47)$$

As well, the output conductance is given by

$$g_o = \frac{\partial I_d}{\partial V_{ds}} = \frac{\mu_n z C_{ox}}{L} \left\{ (V_{gs} - V_{bs} + \phi_{BS}' + V_{ss} - \phi_{ms}') - V_{ds} - \left[\frac{2qN_a \epsilon_s}{C_{ox}^2} (V_{ds} - \phi_{BS}') \right]^{\frac{1}{2}} \right\}. \quad (2.48)$$

At pinch-off, V_{ds} is replaced by V_p , and it is found that (2.48) reduces to zero, as expected, since Q_n is also zero at the drain.

Thus, the basic equations for the bulk charge model are given by (2.37), (2.38), (2.43) and (2.44) through (2.48). The equations can be put in a convenient form by noting that ϕ_{BS}' is relatively independent of gate voltage for $n \gg N_a$ at the surface,^{17,59} so that from (2.36),

$$-\phi_{BS}' \approx -V_{bs} + \frac{2kT}{q} \ln\left(\frac{N_a}{n_i}\right) = -V_{bs} + 2\phi_F \quad (2.49)$$

and ϕ_F represents the position of the hole quasi-Fermi level in the bulk, with respect to the intrinsic level.

If an effective bulk charge voltage V_B is defined as

$$V_B = \left[\frac{4qN_a \epsilon_s \phi_F}{C_{ox}^2} \right]^{\frac{1}{2}} \quad (2.50)$$

then the basic equations may be rewritten as follows:

$$Q_n = C_{ox} \left\{ V_B \left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F} \right)^{\frac{1}{2}} - \left[V_{gs} - V_T + V_B \left(1 - \frac{V_{bs}}{2\phi_F} \right)^{\frac{1}{2}} - V \right] \right\} \quad (2.51)$$

$$y_d = \frac{C_{ox}}{qN_a} V_B \left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F} \right)^{\frac{1}{2}} \quad (2.52)$$

$$g_m = \frac{\mu_n z C_{ox}}{L} V_{ds} \quad (2.53)$$

$$g_{mb} = \frac{\mu_n z C_{ox}}{L} V_B \left[\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V_{ds}}{2\phi_F}\right)^{\frac{1}{2}} - \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right] \quad (2.54)$$

$$g_o = \frac{\mu_n z C_{ox}}{L} \left[V_{gs} - V_T - V_{ds} + V_B \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} - V_B \left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V_{ds}}{2\phi_F}\right)^{\frac{1}{2}} \right] \quad (2.55)$$

$$V_T \approx 2\phi_F - V_{ss} + \phi_{ms} + V_B \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \quad (2.56)$$

$$V_p = V_{gs} - V_T + V_B \left\{ \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} + \frac{V_B}{4\phi_F} - \left[1 - \frac{V_{bs}}{2\phi_F} + \frac{V_{gs} - V_T}{2\phi_F} + \frac{V_B^2}{16\phi_F^2} + \frac{V_B}{2\phi_F} \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right]^{\frac{1}{2}} \right\} \quad (2.57)$$

$$I_d = \frac{\mu_n z C_{ox}}{L} \left\{ V_{ds} \left(V_{gs} - V_T + V_B \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right) - \frac{V_{ds}^2}{2} - \frac{4}{3} \phi_F V_B \left[\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V_{ds}}{2\phi_F}\right)^{\frac{3}{2}} - \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{3}{2}} \right] \right\} \quad (2.58)$$

3. AC THEORY

3.1. THE WEIMER MODEL

A small-signal equivalent circuit for the Weimer model that is valid at moderately high frequencies has been described in the literature.^{7,16} The gate-source and gate-drain capacitances are derived by calculating the total charge stored on the gate and examining the charge variations with fluctuating gate and drain voltages. This analysis results in an equivalent circuit of the form shown in Fig. 3.1,

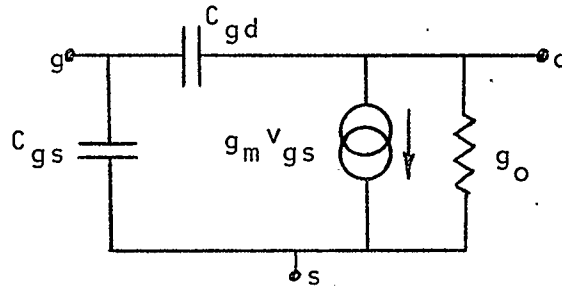


Fig. 3.1 Small-signal equivalent circuit for the MOS FET.

where the gate-source and gate-drain capacitances C_{gs} and C_{gd} respectively, are given by

$$C_{gs} = \frac{2}{3} \frac{LzC_{ox}(V_{gs}-V_T) [3(V_{gs}-V_T)-2V_{ds}]}{[V_{ds} - 2(V_{gs}-V_T)]^2} \quad (3.1)$$

$$C_{gd} = \frac{2}{3} \frac{LzC_{ox}(V_{gs}-V_T-V_{ds}) [3(V_{gs}-V_T)-V_{ds}]}{[V_{ds} - 2(V_{gs}-V_T)]^2} \quad (3.2)$$

Equations (3.1) and (3.2) may be written more conveniently using (2.2) and (2.3) as

$$C_{gs} = \frac{2}{3} \frac{LzC_{ox}v_s(v_s+2v_d)}{(v_s+v_d)^2} \quad (3.3)$$

and
$$C_{gd} = \frac{2}{3} \frac{LzC_{ox}v_d(2v_s+v_d)}{(v_s+v_d)^2} \quad (3.4)$$

The transconductance g_m and output conductance g_o as given by (2.5) and (2.6) may be written in the new notation as

$$g_m = \frac{\mu_n z C_{ox}}{L} (v_s - v_d) \quad (3.5)$$

$$g_o = \frac{\mu_n z C_{ox}}{L} v_d \quad (3.6)$$

and the drain current is given by

$$I_d = \frac{\mu_n C_{ox} z}{2L} (v_s^2 - v_d^2) \quad (3.7)$$

3.2 THE BULK CHARGE MODEL

The short-circuit gate capacitance for the bulk charge model has been calculated by Sah and Pao.¹⁷ The analysis is extended here to differentiate between gate-source, gate-drain and gate-bulk capacitances under non-saturated conditions.

For an element of channel of length dx , the incremental gate charge is given by

$$dQ_g = C_{ox} z V_{ox}' dx \quad (3.8)$$

where V_{ox}' is the potential across the oxide, given by

$$V_{ox}' = V_{gs} - V_{bs} - \phi_{ms} + \phi_{BS} - V \quad (3.9)$$

From the expression for the drain current,

$$dx = - \frac{\mu_n z Q_n}{I_d} dV \quad (3.10)$$

and the total gate charge is found by integrating (3.8) from source to drain. Then

$$Q_{gt} = - \frac{\mu_n z^2 C_{ox}}{I_d} \int_0^{V_{ds}} (V_{gs} - V_{bs} - \phi_{ms} + \phi_{BS} - V) Q_n dV. \quad (3.11)$$

The short circuit gate capacitance C_{gg} can be obtained directly from (3.11), since

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} = \frac{\partial Q_{gt}}{\partial V_{gs}} \quad (3.12)$$

where C_{gs} , C_{gd} and C_{gb} are the gate-source, gate-drain and gate-bulk capacitances respectively.

It can be shown (Appendix A) that

$$C_{gd} = - \frac{\partial Q_{gt}}{\partial V_{ds}} \quad (3.13)$$

and

$$C_{gb} = - \frac{\partial Q_{gt}}{\partial V_{bs}} \quad (3.14)$$

so that

$$C_{gs} = \frac{\partial Q_{gt}}{\partial V_{gs}} + \frac{\partial Q_{gt}}{\partial V_{ds}} + \frac{\partial Q_{gt}}{\partial V_{bs}}. \quad (3.15)$$

The integral in (3.11) is performed for constant V_{gs} , so that in evaluating (3.12), the partial derivative is allowed to operate on the integrand, yielding

$$C_{gg} = C_{ox} L z f(V_{gs}, V_{ds}, V_{bs}) \quad (3.16)$$

where

$$f(V_{gs}, V_{ds}, V_{bs}) = 1 - \frac{V_{ds}^2}{2\theta} - \frac{V_{ds}}{\theta^2} \int_0^{V_{ds}} V dV \quad (3.17)$$

$$\theta = \frac{I_d L}{\mu_n z C_{ox}} \quad (3.18)$$

$$\Gamma = Q_n / C_{ox}, \quad (3.19)$$

and it is assumed that ϕ_{BS} is practically independent of gate voltage for $V_{gs} > V_T$.^{17,59} The gate-drain capacitance can be evaluated by noting that

$$\int_0^{V_{ds}} \frac{\Gamma}{\theta} dV = -1. \quad (3.20)$$

Then (3.11) may be written as

$$Q_{gt} = C_{ox} z L (V_{gs} - V_{bs} - \phi_{ms} + \phi_{BS}) + \frac{C_{ox} z L}{\theta} \int_0^{V_{ds}} \Gamma V dV \quad (3.21)$$

and substitution of (3.21) into (3.13) yields

$$C_{gd} = -C_{ox} z L \frac{\partial}{\partial V_{ds}} \left(\int_0^{V_{ds}} \frac{\Gamma}{\theta} V dV \right). \quad (3.22)$$

Utilizing Liebnitz's rule, the differentiation can be performed directly to yield

$$C_{gd} = C_{ox} z L f_1(V_{gs}, V_{ds}, V_{bs}) \quad (3.23)$$

where

$$f_1(V_{gs}, V_{ds}, V_{bs}) = -\left(\frac{\Gamma_d}{\theta^2} \int_0^{V_{ds}} \Gamma V dV + \frac{V_{ds} \Gamma_d}{\theta} \right) \quad (3.24)$$

and $\Gamma_d = Q_{nd} / C_{ox}$.

Similarly, C_{gb} is obtained from (3.11) and (3.14). In integral form,

$$C_{gb} = C_{ox} z L f_2(V_{gs}, V_{ds}, V_{bs}) \quad (3.25)$$

where

$$f_2(V_{gs}, V_{ds}, V_{bs}) = -\left\{ \frac{V_B}{\Theta^2} \left[\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V_{ds}}{2\phi_F}\right)^{\frac{1}{2}} - \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right] \right. \\ \left. \left\{ \left[V_{gs} - V_T + V_B \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right] \int_0^{V_{ds}} r dv \right. \right. \right. \\ \left. \left. - \int_0^{V_{ds}} r v dv \right\} \right. \\ \left. + \frac{V_B}{4\phi_F \Theta} \int_0^{V_{ds}} \frac{\left[V_{gs} - V_T + V_B \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} - v \right] dv}{\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{v}{2\phi_F}\right)^{\frac{1}{2}}} \right\}. \quad (3.26)$$

Finally, substitution of (3.16), (3.23) and (3.25) into (3.15) gives

$$C_{gs} = C_{ox} z L f_3(V_{gs}, V_{ds}, V_{bs}) \quad (3.27)$$

where

$$f_3(V_{gs}, V_{ds}, V_{bs}) = f(V_{gs}, V_{ds}, V_{bs}) - f_1(V_{gs}, V_{ds}, V_{bs}) - f_2(V_{gs}, V_{ds}, V_{bs})$$

and the integrals involved are listed in final form below.

$$\int_0^{V_{ds}} r v dv = \frac{16}{15} \phi_F^2 V_B \left[\left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{5}{2}} - \left(1 - \frac{V_{bs}}{2\phi_F} - \frac{3V_{ds}}{4\phi_F}\right) \left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V_{ds}}{2\phi_F}\right)^{\frac{3}{2}} \right] \\ - \left[V_{gs} - V_T + V_B \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right] \frac{V_{ds}^2}{2} + \frac{1}{3} V_{ds}^3 \quad (3.28)$$

$$\int_0^{V_{ds}} \Gamma dV = \frac{4}{3} \phi_F V_B \left[\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V_{ds}}{2\phi_F}\right)^{\frac{3}{2}} - \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{3}{2}} \right] - \left[V_{gs} - V_T + V_B \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right] V_{ds} + \frac{1}{2} V_{ds}^2 \quad (3.29)$$

$$\int_0^{V_{ds}} \frac{\left[V_{gs} - V_T + V_B \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right] dV}{\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F}\right)^{\frac{1}{2}}} = 4\phi_F \left[V_{gs} - V_T + V_B \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right] \cdot \left[\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V_{ds}}{2\phi_F}\right)^{\frac{1}{2}} - \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{1}{2}} \right] \quad (3.30)$$

$$\int_0^{V_{ds}} \frac{V dV}{\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F}\right)^{\frac{1}{2}}} = -\frac{16}{3} \phi_F^2 \left[\left(1 - \frac{V_{bs}}{2\phi_F} - \frac{V_{ds}}{4\phi_F}\right) \left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V_{ds}}{2\phi_F}\right)^{\frac{1}{2}} + \left(1 - \frac{V_{bs}}{2\phi_F}\right)^{\frac{3}{2}} \right]. \quad (3.31)$$

The remaining capacitances are obtained by performing the appropriate partial derivatives. However, the procedure is lengthy, and will be omitted here as only C_{gs} and C_{gd} are of interest as far as the noise calculations are concerned.

The form of the equivalent circuit for the bulk charge model has been discussed by Das.^{15,91}

4. THERMAL NOISE

The high frequency thermal noise of the enhancement MOS FET has been analyzed by Shoji,²³ using a transmission line model of the channel for an intrinsic substrate. Other authors have analyzed the effects of the substrate on the thermal noise using a physical approach.^{24,25,54} However, the gate noise parameters for the simple model have not been presented explicitly in terms of bias conditions and geometrical parameters. In addition, the effects of the substrate on the gate noise have not been analyzed correctly. An alternative analysis based on a lumped model approach^{74,75,32-34} is used in this work, and the results are obtained in a form convenient for comparison with experimental measurements. Both the Weimer model and the bulk charge model are treated in detail in both the pre-pinch-off and the pinch-off mode.

4.1 THE WEIMER MODEL

4.1.1 Thermal Channel Noise

The transistor can be split at a point x in the channel as shown in Fig. 4.1.

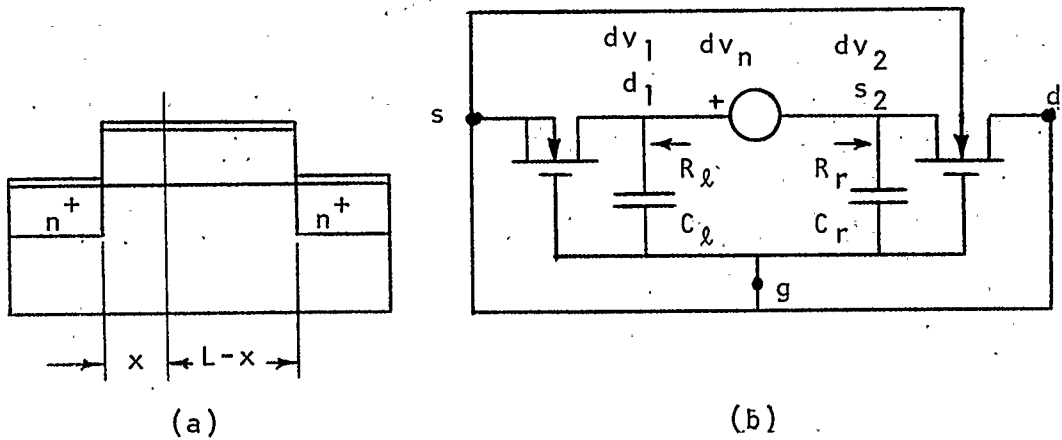


Fig. 4.1 (a) Schematic representation of the MOS FET.
(b) Two-transistor representation of an FET of channel length L .

Utilizing the equivalent circuit of Fig. 2.2, it can be shown that

$$R_\ell = \frac{1}{g_{o1}} \quad (4.1)$$

and,

$$R_r = \frac{1}{g_{o2} + g_{m2}} \quad (4.2)$$

where

$$g_{o1} = \frac{\mu_n C_{ox} z}{x} v \quad (4.3)$$

is the output conductance for the transistor of channel length x ,

$$g_{o2} = \frac{\mu_n C_{ox} z}{L-x} v_d \quad (4.4)$$

is the output conductance for the transistor of channel length $L-x$, and

$$g_{m2} = \frac{\mu_n C_{ox} z}{L-x} (v-v_d) \quad (4.5)$$

is the transconductance of the transistor of channel length $L-x$. It should be noted that v is the gate-channel potential at any point x in the channel, given by

$$v = V_{gs} - V_T - V. \quad (4.6)$$

Addition of (4.1) and (4.2) yields

$$R_{\ell} + R_r = \frac{L}{\mu_n C_{ox} z v}. \quad (4.7)$$

The thermal noise voltage $\overline{dv_n^2}$ generated in a length of channel dx at x is given by

$$\overline{dv_n^2} = 4kT\Delta f dR \quad (4.8)$$

where the incremental channel resistance dR is given by

$$dR = \frac{dx}{\mu_n C_{ox} z v}. \quad (4.9)$$

From (2.1), the elemental channel length dx may be expressed in terms of the drain current as

$$dx = - \frac{\mu_n C_{ox} z}{I_d} v dv. \quad (4.10)$$

Substituting (4.10) and (4.9) into (4.8) yields

$$\overline{dv_n^2} = - \frac{4kT\Delta f}{I_d} dv. \quad (4.11)$$

The contribution to the drain noise current from the element dx is, neglecting capacitive coupling to the gate,

$$\begin{aligned}\overline{i_d^2} &= \frac{\overline{dv_n^2}}{(R_l + R_r)^2} \\ &= - \frac{4kT\Delta f}{I_d} \left(\frac{\mu_n C_{ox} z}{L} \right)^2 v_d^2 dv. \quad (4.12)\end{aligned}$$

The spectral density of the noise current in the drain is then obtained by substituting for I_d from (3.7) and integrating from source to drain. This yields

$$\frac{\overline{i_d^2}}{\Delta f} = \frac{8}{3} \frac{kT\mu_n C_{ox} z}{L} \frac{(v_s^2 + v_s v_d + v_d^2)}{(v_s + v_d)}. \quad (4.13)$$

The equivalent noise resistance R_n is obtained by writing

$$\overline{i_d^2} = 4kT\Delta f R_n g_m^2 \quad (4.14)$$

so that

$$R_n = \frac{2}{3} \frac{L}{\mu_n z C_{ox}} \frac{(v_s^2 + v_s v_d + v_d^2)}{(v_s - v_d)^2 (v_s + v_d)} \quad (4.15)$$

or

$$R_n g_m = \frac{2}{3} \frac{(v_s^2 + v_s v_d + v_d^2)}{(v_s^2 - v_d^2)}. \quad (4.16)$$

At pinch-off,

$$\overline{i_d^2} = \frac{8}{3} kT\Delta f g_{ms} \quad (4.17)$$

and

$$R_n g_{ms} = \frac{2}{3} \quad (4.18)$$

where g_{ms} , the transconductance at saturation, is given by

$$g_{ms} = \frac{\mu_n z C_{ox}}{L} v_s \quad (4.19)$$

Graphs of the normalized drain noise and the $R_n g_m$ product given by (4.16) are shown for various bias conditions in Figs. 4.2 and 4.3.

4.1.2 Gate Noise

The noise current that flows in the gate due to capacitive coupling between the gate and channel can be calculated by considering the capacitances C_ℓ and C_r in Fig. 4.1(b).

Neglecting capacitive currents in calculating voltages at d_1 and s_2 , it is clear that

$$dv_1 = di_d R_\ell \quad (4.20)$$

and

$$dv_2 = -di_d R_r \quad (4.21)$$

where

$$dv_n = dv_1 - dv_2 \quad (4.22)$$

$$di_d = \frac{dv_n}{R_\ell + R_r} \quad (4.23)$$

Substituting for R_ℓ and R_r in (4.20), (4.21) and (4.23),

$$dv_1 = \frac{x}{L} dv_n \quad (4.24)$$

$$dv_2 = \frac{-(L-x)}{L} dv_n \quad (4.25)$$

Then the differential current flowing into the gate is given by

$$di_g = -dv_1(j\omega C_\ell) + dv_2(j\omega C_r) \quad (4.26)$$

or

$$di_g = -j\omega \left[C_\ell \left(\frac{x}{L} \right) - C_r \left(\frac{L-x}{L} \right) \right] dv_n \quad (4.27)$$

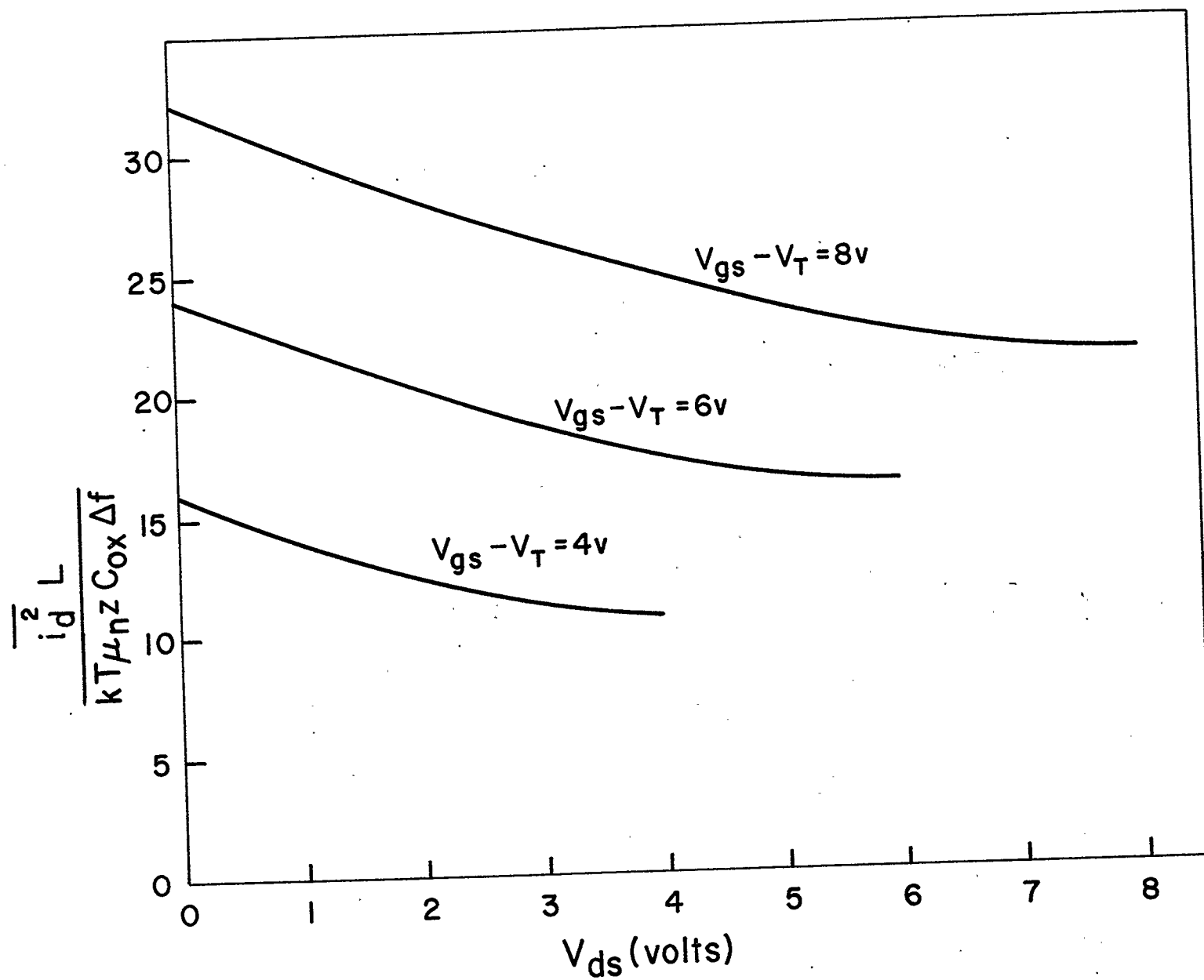


Fig. 4.2 Normalized drain noise as a function of bias for the Weimer model.

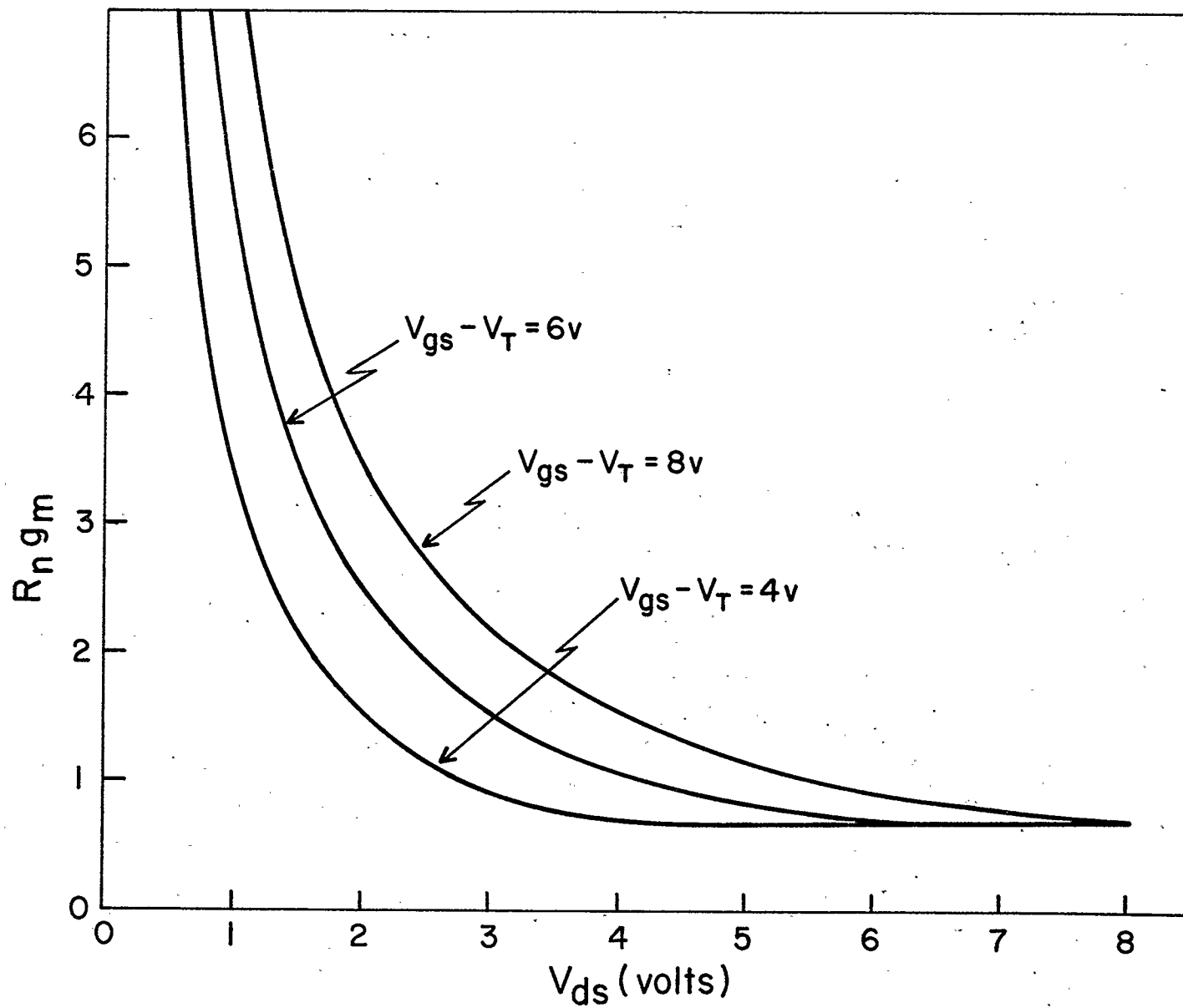


Fig. 4.3 The $R_n g_m$ product as a function of bias for the Weimer model.

For the transistor of channel length x , v_d is replaced by v in (3.4) to give

$$C_{\ell} = \frac{2}{3} LzC_{ox} \frac{v (v_s + 2v)}{(v_s + v)^2} \left(\frac{x}{L} \right) \quad (4.28)$$

and (3.7) yields

$$\frac{x}{L} = \frac{\mu_n C_{ox} z}{2LI_d} (v_s^2 - v^2). \quad (4.29)$$

For the transistor of channel length $(L-x)$, v_s is replaced by v in (3.3) to yield

$$C_r = \frac{2}{3} LzC_{ox} \frac{v (v + 2v_d)}{(v + v_d)^2} \frac{L-x}{L} \quad (4.30)$$

and

$$\frac{L-x}{L} = \frac{\mu_n C_{ox} z}{2LI_d} (v^2 - v_d^2) \quad (4.31)$$

from (3.7).

Substitution of (4.28) to (4.31) in (4.27) gives

$$di_g = \frac{-j\omega \frac{2}{3} C_{ox} zLv}{(v_s^2 - v_d^2)} \left[\frac{2(v_s^3 - v_d^3)}{(v_s^2 - v_d^2)} - 3v \right] dv_n. \quad (4.32)$$

The gate noise is obtained by integrating

$$\overline{i_g^2} = \int_{v_s}^{v_d} \overline{di_g^* di_g}. \quad (4.33)$$

Substituting from (4.11) and (4.32) into (4.33) and integrating from source to drain yields

$$\frac{\overline{i_g^2}}{\Delta f} = \frac{32}{9} \omega^2 kT (C_{ox} Lz)^2 g(v_s, v_d) \quad (4.34)$$

$$g_m (v_s^2 - v_d^2)^2 (v_s + v_d)$$

where

$$g(v_s, v_d) = \frac{4}{3} \frac{(v_s^3 - v_d^3)^3}{(v_s^2 - v_d^2)^2} - 3(v_s^2 + v_d^2)(v_s^3 - v_d^3) + \frac{9}{5} (v_s^5 - v_d^5) \quad (4.35)$$

or simplifying,

$$g(v_s, v_d) = \frac{(v_s - v_d)^3}{15(v_s + v_d)^2} \left[2v_s^4 + 10v_s^3 v_d + 21v_s^2 v_d^2 + 10v_s v_d^3 + 2v_d^4 \right]. \quad (4.36)$$

At pinch-off $v_d = 0$ and

$$\overline{i_g^2} = \frac{64}{135} \frac{\omega^2 k T \Delta f (C_{ox} z L)^2}{g_{ms}}. \quad (4.37)$$

Substituting for g_{ms} from (4.19),

$$\frac{\overline{i_g^2}}{k T \Delta f \omega^2 (C_{ox} z L)^2} = \frac{32}{45} R_{ns}. \quad (4.38)$$

The normalized gate noise is plotted for pre-pinch-off conditions in Fig. 4.4.

4.1.3 The Correlation Coefficient

The correlation coefficient c is defined by

$$c = \frac{\overline{i_g^* i_d}}{\sqrt{\overline{i_g^2} \cdot \overline{i_d^2}}} \quad (4.39)$$

where

$$\overline{i_g^* i_d} = \int_{v_s}^{v_d} \overline{d i_g^* d i_d} \quad (4.40)$$

is obtained by substituting (4.23) and (4.32) into (4.40).

The result may be written as

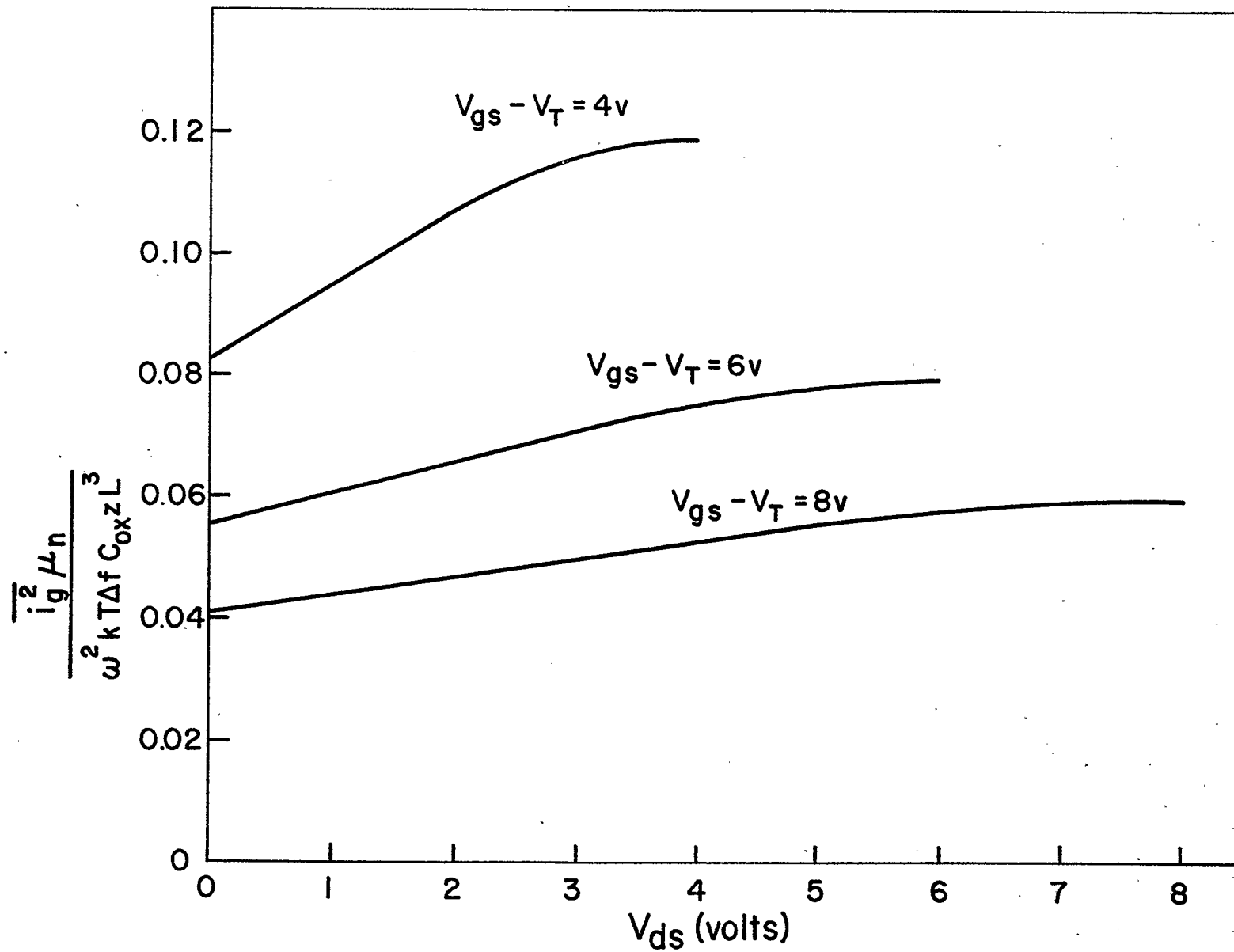


Fig. 4.4 Normalized gate noise as a function of bias for the Weimer model.

$$\overline{i_g^* i_d} = -j\omega \frac{16}{3} \frac{kT\Delta f C_{ox} z L}{(v_s^2 - v_d^2)^2} \left[\frac{3}{4} (v_s^4 - v_d^4) - \frac{2}{3} \frac{(v_s^3 - v_d^3)^2}{(v_s^2 - v_d^2)} \right]. \quad (4.41)$$

Substituting (4.41), (4.34) and (4.13) into (4.39) yields

$$c = \frac{j \left[\frac{3}{4} (v_s^4 - v_d^4) - \frac{2}{3} \frac{(v_s^3 - v_d^3)^2}{(v_s^2 - v_d^2)} \right]}{\left[\frac{1}{3} (v_s^3 - v_d^3) g(v_s, v_d) \right]^{\frac{1}{2}}}. \quad (4.42)$$

At pinch-off, $v_d = 0$ and

$$c = \frac{j}{4} \sqrt{\frac{5}{2}} = 0.395j. \quad (4.43)$$

The magnitude of the correlation coefficient is shown in Fig. 4.5 for the pre-pinch-off case.

4.1.4 Noise Figure Calculations

The equivalent circuit for a simple MOS FET amplifier with source bias resistance by-passed is shown in Fig. 4.6,

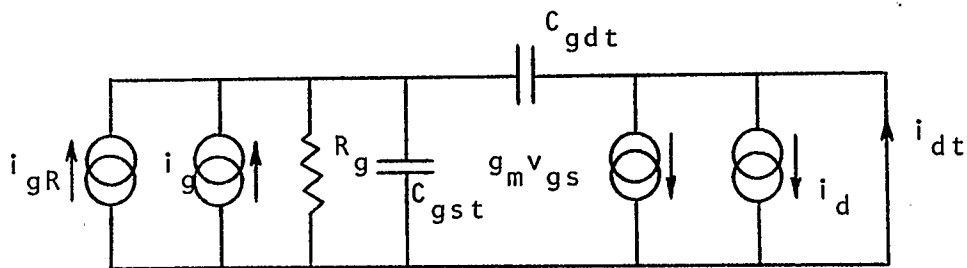


Fig. 4.6 Equivalent circuit for a simple amplifier at moderately high frequencies.

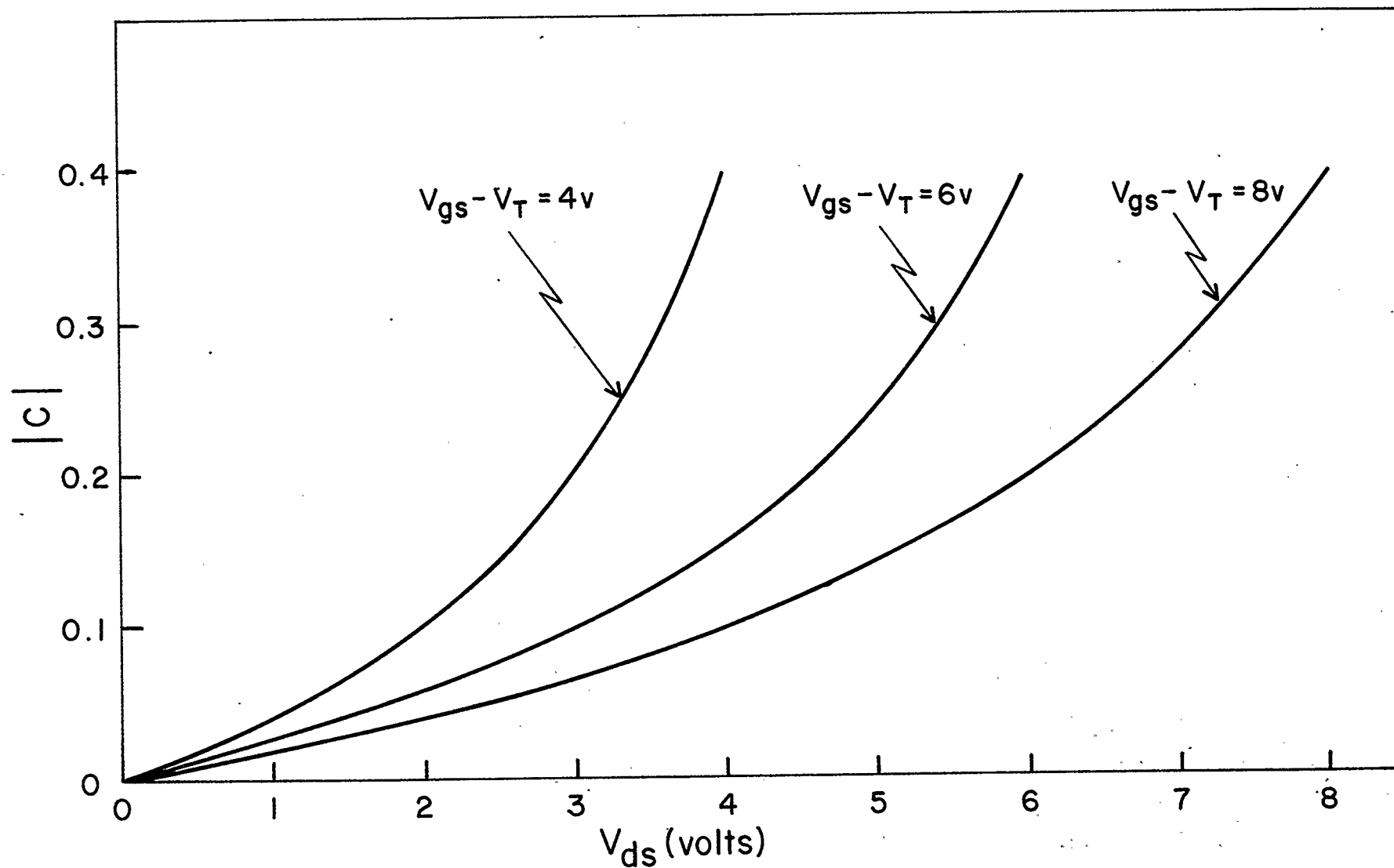


Fig. 4.5 Magnitude of the correlation coefficient as a function of bias for the Weimer model.

where C_{gst} = total gate-source capacitance, including strays

C_{gdt} = total gate-drain capacitance, including strays

i_{gR} = thermal noise current resulting from Johnson
noise of R_g

i_g = gate noise current due to capacitive coupling
with the channel

i_d = thermal noise current from the conducting
channel

i_{dt} = total noise current in the drain lead.

The output is shown ac short-circuited for convenience since the load resistance does not enter into the expression for the noise factor.³⁴

It has been shown^{34,35} that it is possible to write circuit equations for the model of Fig. 4.6 in the normal manner, replace currents with Fourier spectra, take the product with the complex conjugate, and perform a suitable averaging procedure to obtain the mean squared noise currents directly.

A nodal analysis of the circuit yields

$$i_{dt} = i_d + \frac{(i_g + i_{gR})R_g(g_m - j\omega C_{gdt})}{1 + j\omega R_g(C_{gst} + C_{gdt})}. \quad (4.44)$$

Replacing currents with equivalent current spectra in (4.44), taking the product with the complex conjugate noting that i_g and i_d are correlated, and averaging yields

$$\overline{i_{dt}^2} = \overline{i_d^2} + \frac{(\overline{i_g^2} + \overline{i_{gR}^2}) R_g^2 (g_m^2 + \omega^2 C_{gdt}^2)}{1 + [\omega R_g (C_{gst} + C_{gdt})]^2} - \frac{2|c| \sqrt{\overline{i_g^2} \cdot \overline{i_d^2}} R_g^2 \left[\omega g_m (C_{gst} + C_{gdt}) + \frac{\omega C_{gdt}}{R_g} \right]}{1 + [\omega R_g (C_{gst} + C_{gdt})]^2} \quad (4.45)$$

Similarly, the mean square contribution to the output current from the gate resistance only is given by

$$\overline{i_{dtR}^2} = \frac{\overline{i_{gR}^2} R_g^2 (g_m^2 + \omega^2 C_{gdt}^2)}{1 + [\omega R_g (C_{gst} + C_{gdt})]^2} \quad (4.46)$$

The noise factor is then defined as

$$F = \frac{\overline{i_{dt}^2}}{\overline{i_{dtR}^2}} \quad (4.47)$$

At pinch-off, substituting for $\overline{i_g^2}$ from (4.37), $\overline{i_d^2}$ from (4.13), $|c|$ from (4.43), and noting that

$$\overline{i_{gR}^2} = \frac{4kT\Delta f}{R_g} \quad (4.48)$$

yields the noise factor F, where

$$F-1 = \frac{2}{3g_{ms}R_g} \left[\frac{1 + (\omega R_g C_t)^2}{1 + \left(\frac{\omega C_{gdt}}{g_{ms}}\right)^2} \right] + \frac{16}{135} \frac{\omega^2 R_g C_o^2}{g_{ms}} - \frac{2}{9} \frac{\omega^2 R_g C_t C_o}{g_{ms}} \left[\frac{1 + \frac{C_{gdt}}{R_g C_t g_{ms}}}{1 + \left(\frac{\omega C_{gdt}}{g_{ms}}\right)^2} \right] \quad (4.49)$$

$$C_t = C_{gst} + C_{gdt}$$

and

$$C_o = C_{ox} Lz.$$

The first, second and third terms are due to channel noise, gate noise and correlation respectively. At moderately high frequencies, the term $\frac{\omega C}{g_{ms}} \frac{g_{dt}}{g_{ms}}$ is much smaller than unity. If $R_g \gg \frac{1}{g_{ms}}$ and $C_t > C_o$, which is usually the case, it is found that channel noise dominates and F becomes

$$F \approx 1 + \frac{2}{3g_{ms}R_g} \left[1 + \left(\frac{f}{f_o} \right)^2 \right] \quad (4.50)$$

where

$$f_o = \frac{1}{2\pi R_g C_t} \quad (4.51)$$

The minimum noise factor is found by differentiating (4.49) with respect to R_g and equating the result to zero. This results in an optimum gate resistance

$$R_{gopt} = \frac{1}{\omega C_t} \quad (4.52)$$

and

$$F_{min} \approx 1 + \frac{4}{3R_{gopt}g_{ms}} \quad (4.53)$$

Since the optimum gate resistance depends on frequency, it is not possible to minimize F over a wide frequency range using a fixed value for R_g .

4.2 THE BULK CHARGE MODEL

The effects of the substrate on the thermal noise characteristics have been analyzed in detail by Sah et al,²⁴ and Klaassen and Prins.²⁵ An analysis of the gate noise and correlation coefficient has been presented by Rao⁵⁴ using the bulk charge theory of van Nielen and Memelink.³⁶

Identical results can be obtained by utilizing the lumped model approach used to calculate the noise quantities for the Weimer model. An error has been discovered in previous work involving the gate noise. The correct expressions are derived and discussed in detail.

4.2.1 Thermal Channel Noise

The two-transistor representation of the FET with drain, gate and substrate ac short-circuited to the source is shown in Fig. 4.7.

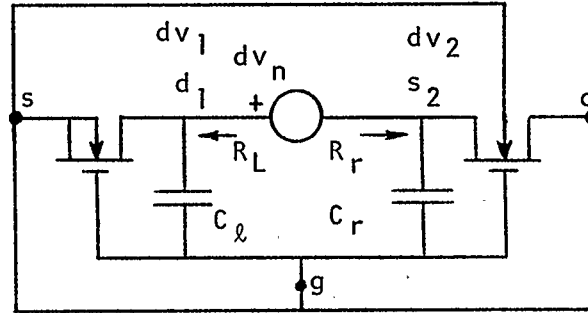


Fig. 4.7 Two-transistor representation of a MOS FET of channel length L .

The resistances R_ℓ and R_r are found from the small-signal equivalent circuit to be

$$R_r = \frac{1}{g_{mr} + g_{mbr} + g_{or}} \quad (4.54)$$

$$R_\ell = \frac{1}{g_{o\ell}} \quad (4.55)$$

where g_{mr} , g_{mbr} are the gate and substrate transconductances respectively, and g_{or} is the output conductance for the transistor of channel length $(L-x)$, given by

$$g_{mr} = \frac{\mu_n z C_{ox}}{L-x} (V_{ds} - V) \quad (4.56)$$

$$g_{mbr} = \frac{\mu_n z C_{ox}}{L-x} V_B \left[\left(1 + \frac{V_{ds}}{2\phi_F}\right)^{\frac{1}{2}} - \left(1 + \frac{V}{2\phi_F}\right)^{\frac{1}{2}} \right] \quad (4.57)$$

$$g_{or} = \frac{\mu_n z C_{ox}}{L-x} \left[(V_{gs} - V_T + V_B - V_{ds}) - V_B \left(1 + \frac{V_{ds}}{2\phi_F}\right)^{\frac{1}{2}} \right] \quad (4.58)$$

and g_{ol} is the output conductance for the transistor of channel length x , given by

$$g_{ol} = \frac{-\mu_n z Q_n}{x} \quad (4.59)$$

where Q_n is the inversion charge density at any point in the channel, described by (2.51).

Then substitution into (4.54) and (4.55) gives

$$R_l = \frac{-x}{\mu_n z Q_n} \quad (4.60)$$

$$R_r = \frac{-(L-x)}{\mu_n z Q_n} \quad (4.61)$$

The channel conductance is given by $-\mu_n z Q_n$, so that the thermal noise voltage generated in an element of channel of length dx is

$$\overline{dv_n^2} = \frac{-4kT\Delta f dx}{\mu_n z Q_n} \quad (4.62)$$

Neglecting capacitive currents flowing to the gate, the contribution to the short-circuited drain noise is given by

$$\overline{di_d^2} = \frac{\overline{dv_n^2}}{(R_\ell + R_r)^2} \quad (4.63)$$

and substitution of (4.60), (4.61) and (4.62) into (4.63) yields

$$\overline{di_d^2} = \frac{4kT\Delta f}{I_d} \left(\frac{\mu_n z}{L}\right)^2 Q_n^2 dV \quad (4.64)$$

The total short-circuited noise current in the drain, $\overline{i_d^2}$, is obtained by integrating (4.64) from $x = 0$ to $x = L$, where

$$\overline{i_d^2} = \frac{4kT\Delta f}{I_d} \left(\frac{\mu_n z C_{ox}}{L}\right)^2 \int_0^{V_{ds}} \left(\frac{Q_n}{C_{ox}}\right)^2 dV \quad (4.65)$$

and

$$\begin{aligned} \int_0^{V_{ds}} \left(\frac{Q_n}{C_{ox}}\right)^2 dV &= \frac{1}{3} \left\{ 3V_B^2 V_{ds} \left(1 + \frac{V_{ds}}{4\phi_F}\right) + (V_{gs} - V_T + V_B)^3 \right. \\ &\quad \left. - (V_{gs} - V_T + V_B - V_{ds})^3 \right. \\ &\quad \left. - 8\phi_F V_B (V_{gs} - V_T + V_B + 2\phi_F) \left[\left(1 + \frac{V_{ds}}{2\phi_F}\right)^{\frac{3}{2}} - 1 \right] \right. \\ &\quad \left. + \frac{48}{5} \phi_F^2 V_B \left[\left(1 + \frac{V_{ds}}{2\phi_F}\right)^{\frac{5}{2}} - 1 \right] \right\}. \end{aligned} \quad (4.66)$$

In (4.65), it has been assumed that $V_{bs} = 0$, for convenience. Equation (4.65) yields results which are identical to those presented by Sah et al.²⁴

The equivalent noise resistance is found by writing

$$\overline{i_d^2} = 4kT\Delta f R_n g_m^2 \quad (4.67)$$

and comparison of (4.67) with (4.65) yields

$$R_n g_m = \frac{\int_0^{V_{ds}} r^2 dV}{\Theta V_{ds}} \quad (4.68)$$

where Θ and r are given by (3.18) and (3.19) respectively. Graphs of $R_n g_m$ are shown in Fig. 4.8 as a function of drain bias for various values of the gate voltage. For values of $V_{ds} \gg \phi_F$, (4.68) can be simplified considerably by considering the expression for the output conductance, (2.55), with $V_{bs} = 0$. When $g_o = 0$, $V_{ds} = V_p$ and

$$V_{gs} - V_T = V_p - V_B \left(1 - \sqrt{1 + \frac{V_p}{2\phi_F}} \right). \quad (4.69)$$

If $V_{ds} = V_p \gg \phi_F$, then

$$V_{gs} - V_T \approx V_p + V_B \left(\frac{V_p}{2\phi_F} \right)^{\frac{1}{2}}. \quad (4.70)$$

Substitution of (4.70) into (4.68) and simplification gives²⁴

$$R_{ns} g_{ms} \approx \frac{2}{3} \left[1 + \frac{11}{15} \frac{V_B}{\sqrt{2\phi_F V_p}} \right]. \quad (4.71)$$

From (4.71), it is apparent that the noise is increased over its value of $\frac{2}{3}$ as indicated by the Weimer model. Figure 4.9 illustrates the increase in the $R_n g_m$ product at saturation as the substrate doping increases in value. The pinch-off voltage V_p decreases as the doping is increased, so that g_m decreases and R_n can become much larger than the value of $\frac{2}{3g_m}$ obtained for the Weimer model.

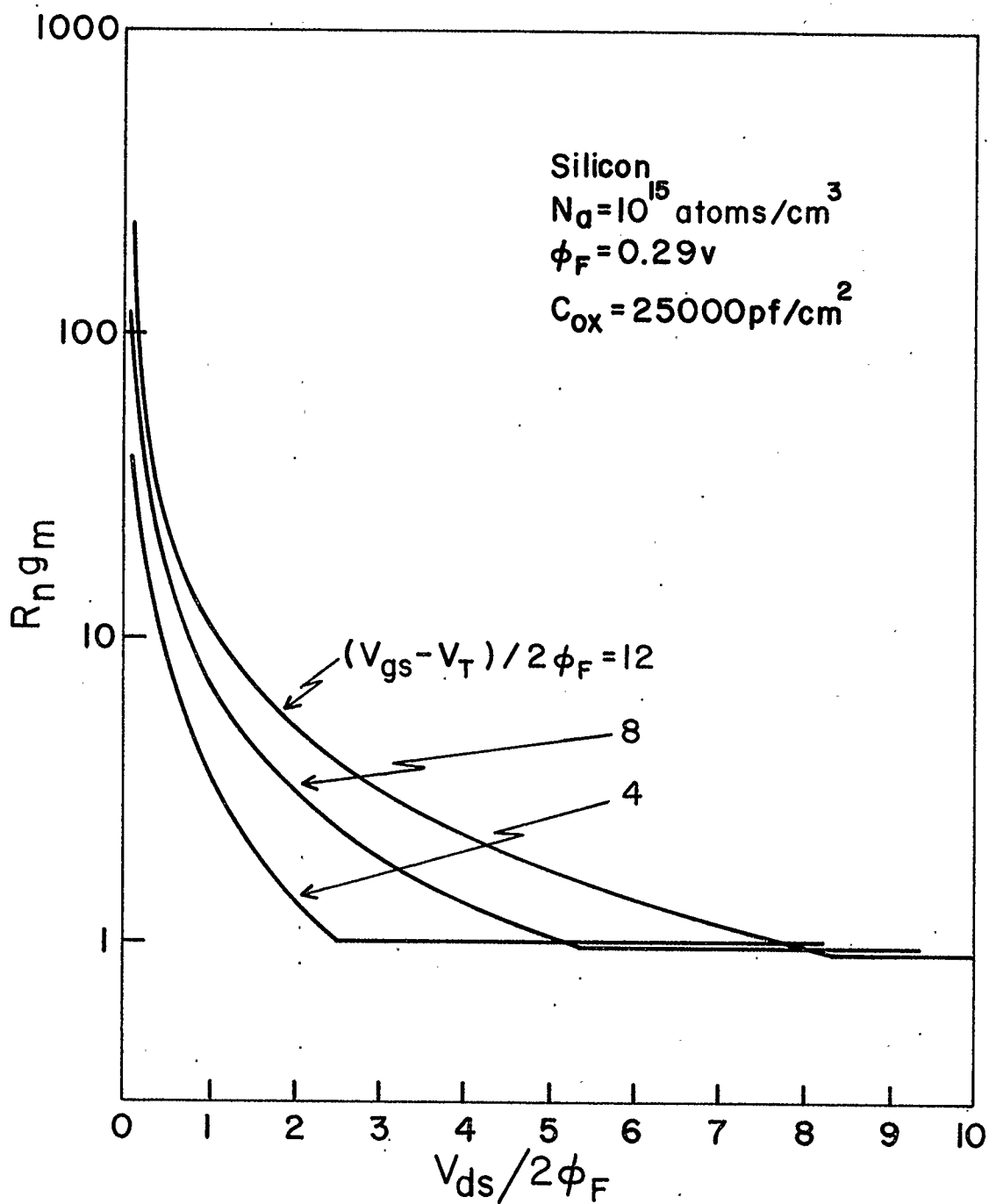


Fig. 4.8 The $R_n g_m$ product as a function of bias for the bulk charge model.

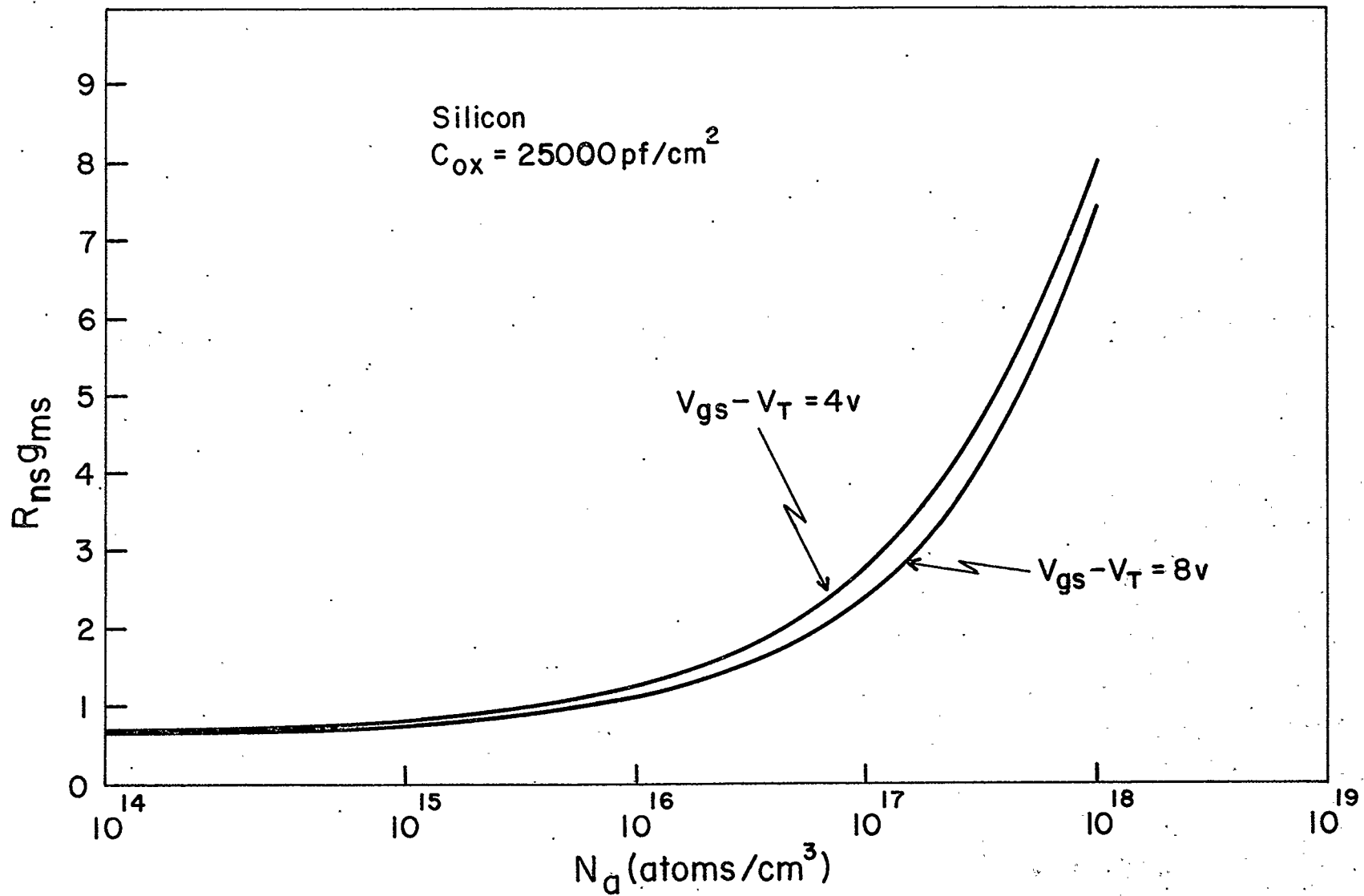


Fig. 4.9 The $R_{n}g_m$ product as a function of doping at pinch-off for the bulk charge model.

4.2.2 Gate Noise at Moderately High Frequencies

As for the Weimer model, a straightforward calculation of the gate noise can be performed by considering the effects of C_ℓ and C_r as shown in Fig. 4.7. The analysis given in section 4.1.2 applies, and the capacitive current flowing into the gate is given by

$$di_g = -j\omega \left[C_\ell \left(\frac{x}{L} \right) - C_r \left(\frac{L-x}{L} \right) \right] dv_n. \quad (4.72)$$

The capacitance C_ℓ represents the gate-drain capacitance for the transistor of channel length x , and is found by substituting V for V_{ds} and x for L in (3.23), so that

$$C_\ell = C_{ox} z L \left(\frac{x}{L} \right) f_3(V, V_{gs}) \quad (4.73)$$

where

$$f_3(V, V_{gs}) = - \left(\frac{\Gamma}{\theta_1^2} \int_0^V \Gamma V dV + \frac{\Gamma V}{\theta_1} \right) \quad (4.74)$$

and θ_1 is found by replacing V_{ds} by V in (3.18), viz.

$$\theta_1 = V(V_{gs} - V_T + V_B) - \frac{V^2}{2} - \frac{4}{3} \phi_F V_B \left[\left(1 + \frac{V}{2\phi_F} \right)^{\frac{3}{2}} - 1 \right]. \quad (4.75)$$

Similarly, C_r represents the gate-source capacitance for the transistor of channel length $L-x$, and is found by substituting $V_{ds}-V$ for V_{ds} , $V_{gs}-V$ for V_{gs} , $-V$ for V_{bs} , and $L-x$ for L in (3.26). Then

$$C_r = C_{ox} z L \left(\frac{L-x}{L} \right) f_4(V_{gs}, V, V_{ds}) \quad (4.76)$$

where

$$\begin{aligned}
 f_4(V_{gs}, V, V_{ds}) = & \left\{ 1 - \frac{V_{ds2}}{\theta_2} \left(\frac{V_{ds2}}{2} - r_d \right) - \frac{1}{\theta_2^2} (V_{ds2} - r_d) \cdot \right. \\
 & \int_0^{V_{ds2}} r V dV + \frac{V_B}{\theta_2^2} \left[\left(1 + \frac{V_{ds}}{2\phi_F} \right)^{\frac{1}{2}} - \left(1 + \frac{V}{2\phi_F} \right)^{\frac{1}{2}} \right] \cdot \\
 & \left[(V_{gs2} - V_T + V_B) \int_0^{V_{ds2}} r dV - \int_0^{V_{ds2}} r V dV \right] \\
 & \left. + \frac{V_B}{4\phi_F \theta_2} \left[(V_{gs2} - V_T + V_B) \int_0^{V_{ds2}} \frac{dV}{\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F} \right)^{\frac{1}{2}}} - \int_0^{V_{ds2}} \frac{V dV}{\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F} \right)^{\frac{1}{2}}} \right] \right\}
 \end{aligned}
 \tag{4.77}$$

$$V_{ds2} = V_{ds} - V$$

$$V_{gs2} = V_{gs} - V$$

and θ_2 is found by replacing V_{ds} , V_{gs} and V_{bs} by V_{ds2} , V_{gs2} and $-V$ respectively in (3.18), so that

$$\theta_2 = V_{ds2} (V_{gs2} - 2\phi_F - \phi'_{ms}) - \frac{1}{2} V_{ds2}^2 - \frac{4}{3} \phi_F V_B \left[\left(1 + \frac{V_{ds}}{2\phi_F} \right)^{\frac{3}{2}} - \left(1 + \frac{V}{2\phi_F} \right)^{\frac{3}{2}} \right]. \tag{4.78}$$

It should be noted that

$$\int_0^{V_{ds2}} \frac{V dV}{\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F} \right)^{\frac{1}{2}}} = -\frac{16}{3} \phi_F^2 \left[\left(1 + \frac{3V}{4\phi_F} - \frac{V_{ds}}{4\phi_F} \right) \left(1 + \frac{V_{ds}}{2\phi_F} \right)^{\frac{1}{2}} - \left(1 + \frac{V}{2\phi_F} \right)^{\frac{3}{2}} \right]
 \tag{4.79}$$

and

$$\int_0^{V_{ds2}} \frac{dV}{\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F}\right)^{\frac{1}{2}}} = 4\phi_F (V_{gs} - V_T + V_B - V) \left[\left(1 + \frac{V_{ds}}{2\phi_F}\right)^{\frac{1}{2}} - \left(1 + \frac{V}{2\phi_F}\right)^{\frac{1}{2}} \right]. \quad (4.80)$$

In addition, from (3.18) we have

$$\frac{I_d L}{\mu_n z C_{ox}} = \theta \quad (3.18)$$

and it follows that

$$\frac{I_d x}{\mu_n z C_{ox}} = \theta_1. \quad (4.81)$$

Then

$$\frac{x}{L} = \frac{\theta_1}{\theta}. \quad (4.82)$$

Similarly, it is easy to show that

$$\frac{L-x}{L} = \frac{\theta_2}{\theta}. \quad (4.83)$$

Substitution of (4.73), (4.76), (4.82) and (4.83) into (4.72) gives

$$di_g = \frac{j\omega C_{ox} z L}{\theta^2} \left[\theta_1^2 f_3(V, V_{gs}) - \theta_2^2 f_4(V, V_{gs}, V_{ds}) \right] dv_n. \quad (4.84)$$

The gate noise is then obtained from

$$\overline{i_g^2} = \int_0^{V_{ds}} di_g^* di_g. \quad (4.85)$$

and utilizing (4.62) and (4.84) yields

$$\overline{i_g^2} = \frac{2kT\Delta f \omega^2 C_{ox} z L^3}{\mu_n \phi_F \left[\frac{\theta}{(2\phi_F)^2} \right]^5} \int_0^{\frac{V_{ds}}{2\phi_F}} Y^2 d\left(\frac{V}{2\phi_F}\right) \quad (4.86)$$

where

$$Y = \frac{1}{(2\phi_F)^4} \left[\theta_1^2 f_3(V, V_{gs}) - \theta_2^2 f_4(V, V_{gs}, V_{ds}) \right] \quad (4.87)$$

The integral in (4.86) can be evaluated numerically. Graphs of the normalized gate noise are shown in Fig. 4.10 as a function of drain bias for various gate voltages in excess of the threshold voltage V_T . It should be noted that all voltages are normalized to $2\phi_F$ for convenience.

4.2.3 The Correlation Coefficient

The correlation coefficient c is obtained using (4.39) as before. The term $\overline{i_g^* i_d}$ is calculated using

$$\overline{i_g^* i_d} = \int_0^{V_{ds}} \overline{di_g^* di_d} \quad (4.88)$$

Substitution of (4.84), and di_d from (4.64) into (4.88) gives

$$\overline{i_g^* i_d} = \frac{-j\omega 4kT\Delta f C_{ox} z L}{\left[\frac{\theta}{(2\phi_F)^2} \right]^3} \int_0^{\frac{V_{ds}}{2\phi_F}} \frac{\Gamma}{2\phi_F} Y d\left(\frac{V}{2\phi_F}\right) \quad (4.89)$$

Then combining (4.89), (4.86) and (4.65), the correlation coefficient can be written in integral form as

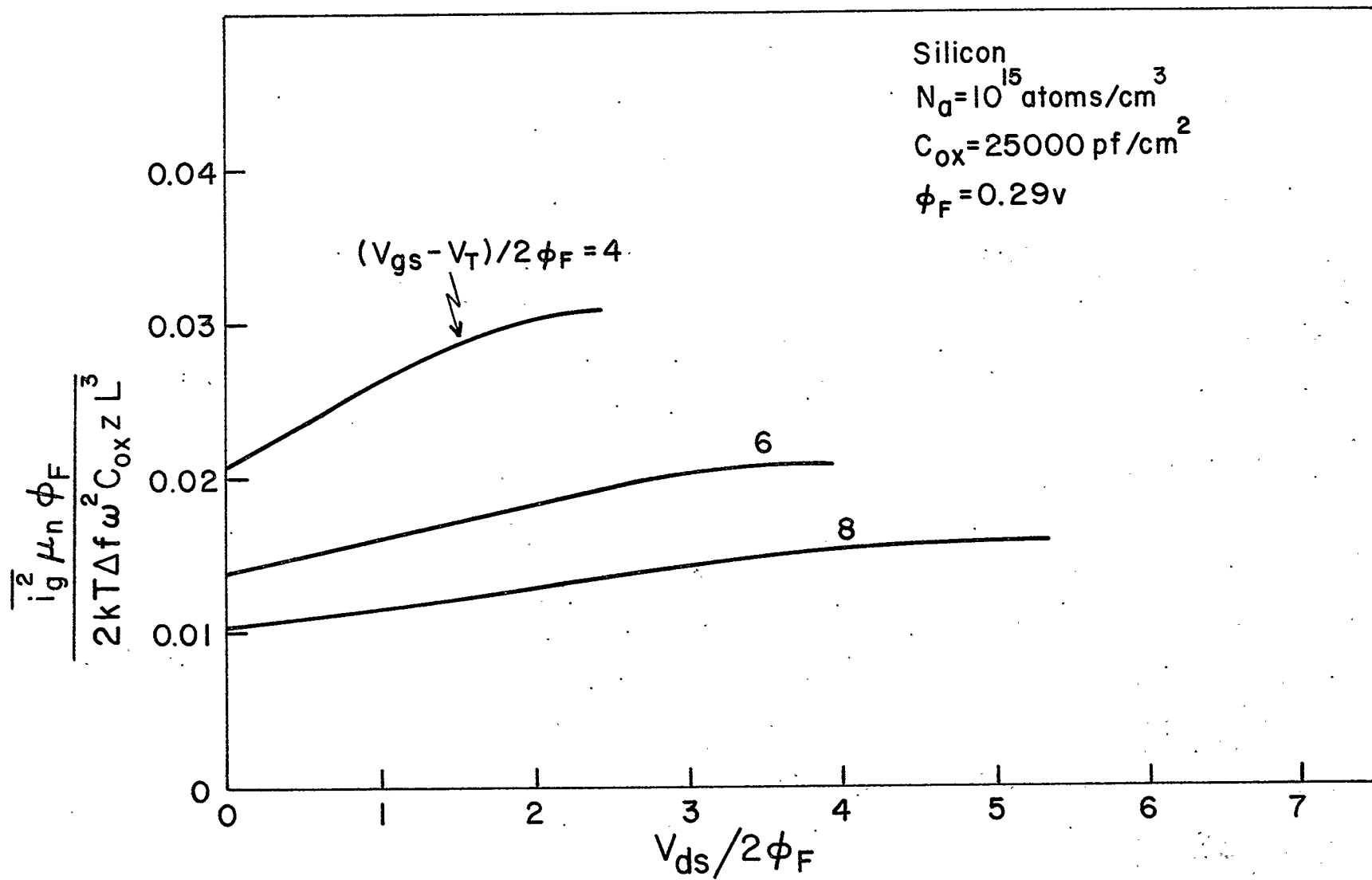


Fig. 4.10 Normalized gate noise as a function of bias for the bulk charge model.

$$c = \frac{-j \int_0^{\frac{V_{ds}}{2\phi_F}} \frac{\Gamma}{2\phi_F} \gamma d\left(\frac{V}{2\phi_F}\right)}{\left[\int_0^{\frac{V_{ds}}{2\phi_F}} \gamma^2 d\left(\frac{V}{2\phi_F}\right) \int_0^{\frac{V_{ds}}{2\phi_F}} \left(\frac{\Gamma}{2\phi_F}\right)^2 d\left(\frac{V}{2\phi_F}\right) \right]^{\frac{1}{2}}} \quad (4.90)$$

The integrals in (4.90) can again be evaluated using numerical techniques. The magnitude of the correlation coefficient is shown in Fig. 4.11 for bias conditions corresponding to those used in Fig. 4.10.

As the substrate doping becomes small, $N_a \rightarrow n_i$, $\phi_F \rightarrow 0$, and the expressions for the gate noise (4.86) and the correlation coefficient (4.90) should reduce to those given by (4.34) and (4.42) for the Weimer model. At pinch-off, with $\phi_F = 0$, $V_{gs} - V_T = V_p$ and it can be shown that

$$\theta_1^2 f_3(V, V_{gs}) = \frac{V_p^2}{6} (V - V_p)(V - 3V_p) \quad (4.91)$$

$$\theta_2^2 f_4(V, V_{gs}, V_p) = \frac{1}{6} (V_p - V)^4 \quad (4.92)$$

so that (4.87) becomes

$$\gamma = \frac{V_p^2}{6} (V - V_p)(V_p - 3V). \quad (4.93)$$

Substitution into (4.86) and (4.90) yields

$$\overline{i_{go}^2} = \frac{64}{135} \frac{kT \Delta f \omega^2 (C_{ox} L_z)^2}{g_{ms}} \quad (4.94)$$

$$\overline{i_{go}^* i_{do}} = -\frac{4}{9} kT \Delta f j \omega C_{ox} L_z \quad (4.95)$$

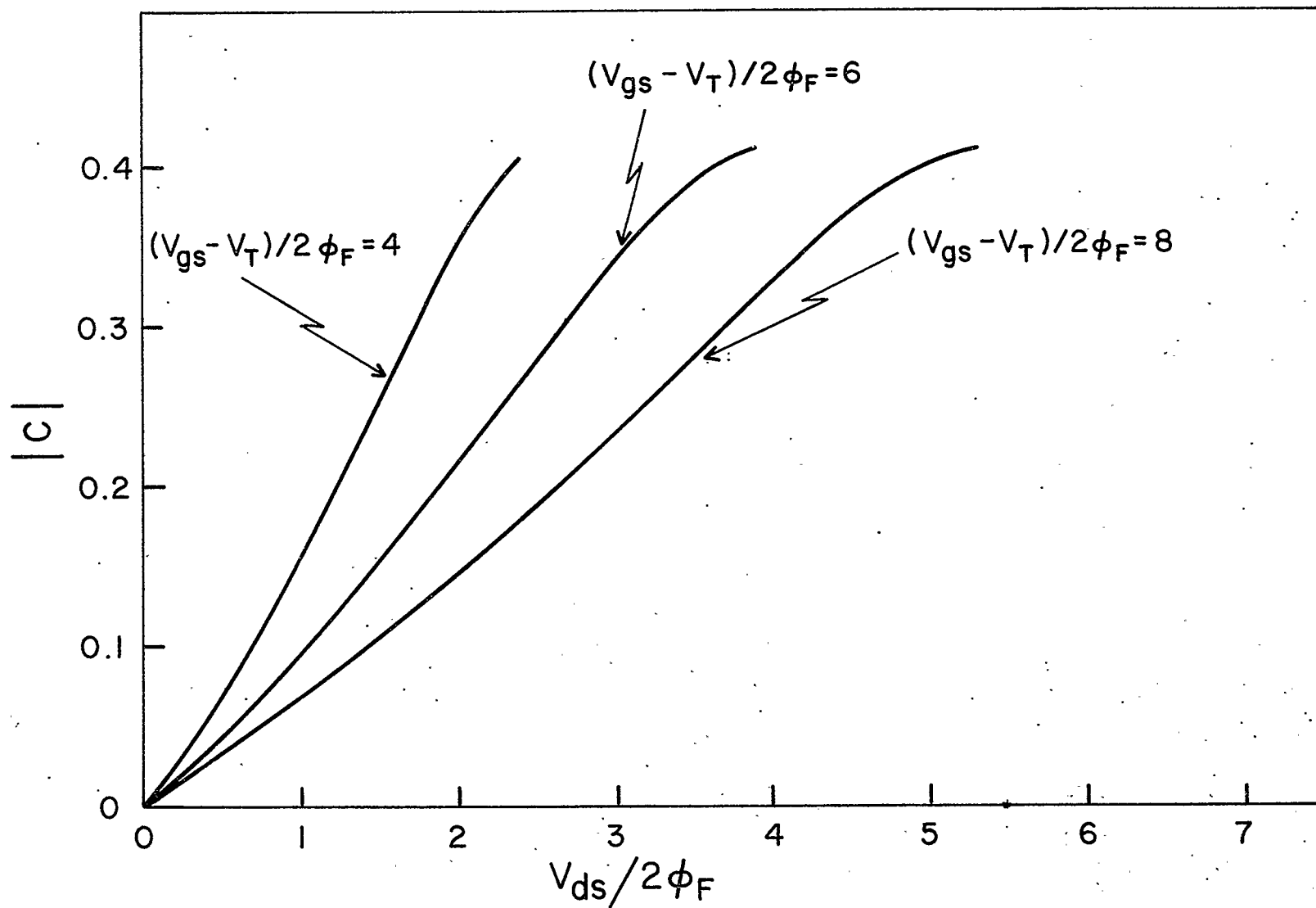


Fig. 4.11 Magnitude of the correlation coefficient as a function of bias for the bulk charge model.

and

$$c = \frac{j}{4} \sqrt{\frac{5}{2}} \quad (4.96)$$

in agreement with the results for the Weimer model.

The effects of substrate doping on the gate noise, cross correlation term, and correlation coefficient at pinch-off are shown in Figs. 4.12, 4.13 and 4.14 respectively. The gate noise and correlation term are normalized to (4.94) and (4.95) so that the effects of the doping can clearly be seen.

The results for the gate noise and cross correlation agree in magnitude and form with those given by Rao, but the correlation coefficient does not. Rao's numerical results indicate a monotonically decreasing $|c|$ with increasing N_a , due to increasing $\overline{i_d^2}$. Figure 4.15 illustrates that this is not the case. While it is true that $R_{ns}g_{ms}$ increases with doping, the pinch-off voltage V_p and thus g_{ms} decrease with increasing N_a , so that $\overline{i_d^2} = 4kT\Delta f R_{ns}g_{ms}^2$ does not vary appreciably at pinch-off over a wide range of values for the doping. The magnitude of c is seen to increase slightly over the value of 0.395 for an intrinsic substrate, in agreement with Halladay and van der Ziel's⁵⁵ experimental results. The dependence of $|c|$ on N_a was used to support their theory of an "excess" noise generator operating in the channel at high frequencies. It has recently been shown⁶⁰ that the excess noise does not exist, and that their measurements were not performed at sufficiently high frequencies to ensure that the $1/f$ component of noise was negligible.

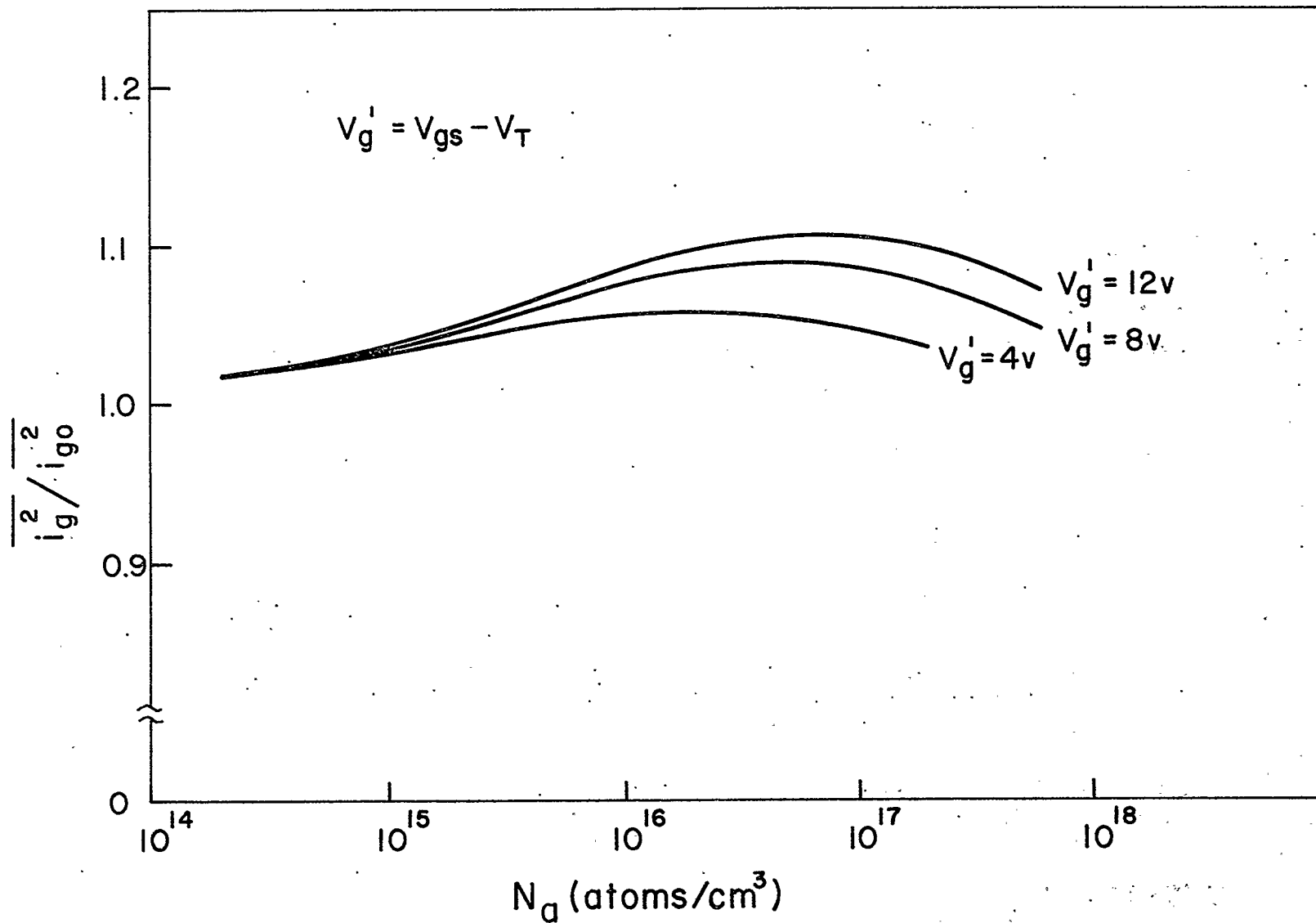


Fig. 4.12 Normalized gate noise as a function of doping at pinch-off.

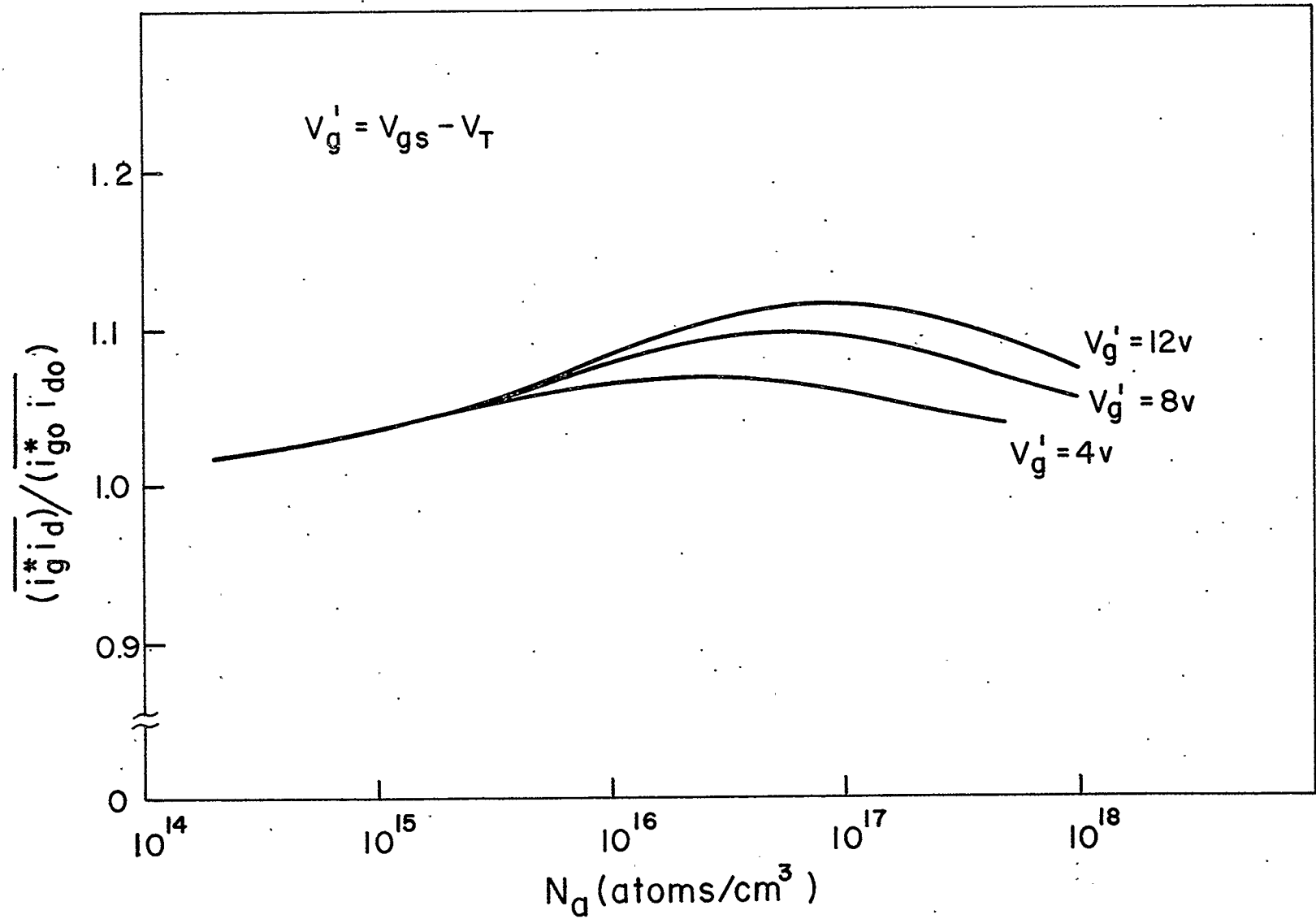


Fig. 4.13 Normalized cross-correlation as a function of doping at pinch-off.

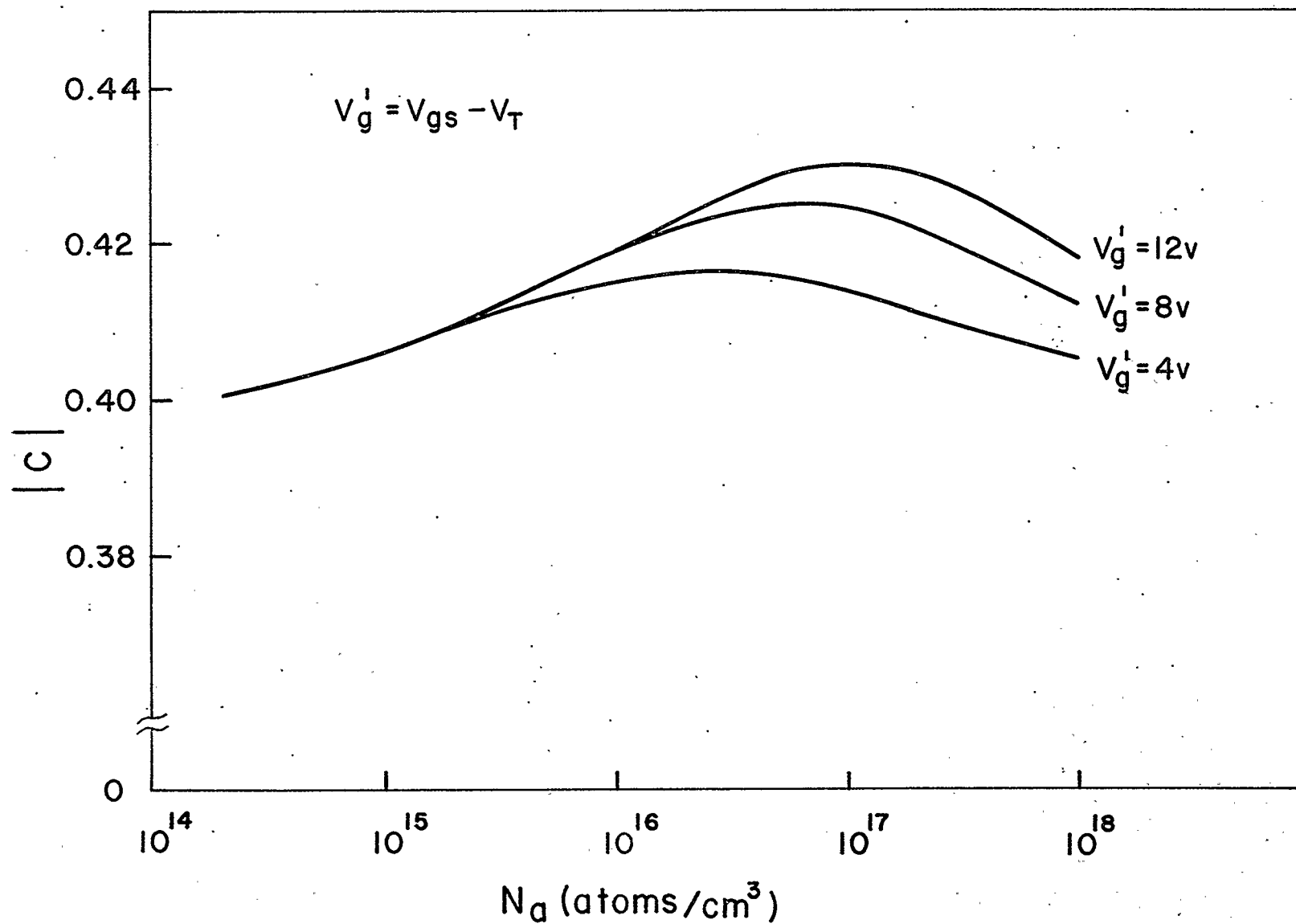


Fig. 4.14 Magnitude of the correlation coefficient as a function of doping at pinch-off.

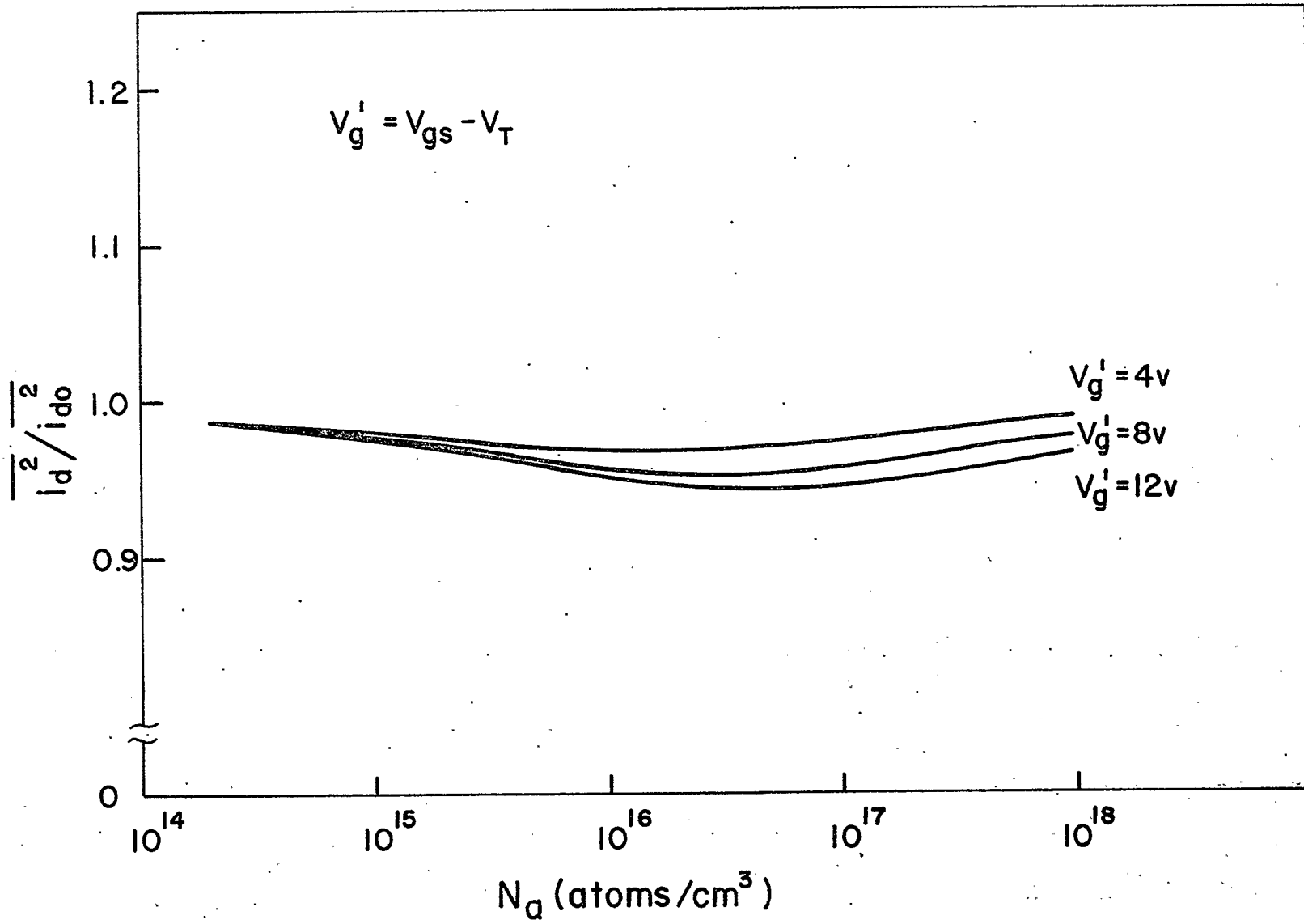


Fig. 4.15 Normalized drain noise as a function of doping at pinch-off.

5. LOW FREQUENCY NOISE MECHANISMS

In addition to thermal noise in the channel of the MOS FET, there appear to be two major noise mechanisms which dominate the noise performance of the device at lower frequencies. The first of these is surface noise at the oxide-semiconductor interface,^{22,26,27,29,37} and the second is generation-recombination noise^{28,31,71,74} due to random emission and capture of carriers at the trapping centres in the depletion region of the semiconductor. In this work, both mechanisms will be analyzed in detail, using a straightforward approach to evaluate the magnitude of the noise.

5.1 SHOCKLEY-READ-HALL (SRH) STATISTICS

The statistics of the SRH generation-recombination centres in a p-n junction depletion region have been well known for a number of years.³⁸⁻⁴⁴ A simple two-level trap will alternately emit a hole and an electron and simultaneously fluctuate between a charged and neutral state in the process. The random fluctuation in charge states causes low-frequency noise due to the long time constants involved in the capture and emission processes. The energy band diagram showing a simple trap is given in Fig. 5.1.

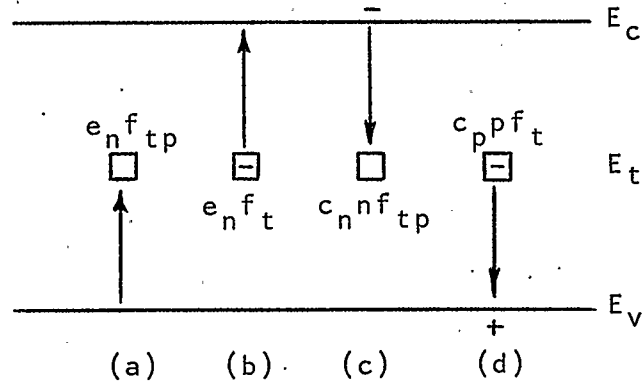


Fig. 5.1 Energy band diagram showing a simple two-level trap in the forbidden band.
(a) hole emission, (b) electron emission,
(c) electron capture, (d) hole capture.

It should be noted that

- e_p = emission probability of a hole by SRH centre
- e_n = emission probability of an electron by SRH centre
- f_t = fraction of SRH centres occupied by electrons
- f_{tp} = fraction of empty SRH centres
- c_n = electron capture probability of SRH centre
- c_p = hole capture probability of SRH centre
- n, p = electron and hole concentrations, respectively.

For such a single level acceptor centre which is either negatively charged when filled with an electron or neutral when empty, it can be shown that the maximum decay time constant for a regression in the trapped electron concentration n_t is

$$\tau_t = \frac{1}{c_p(p_0 + p_1) + c_n(n_0 + n_1)} \quad (5.1)$$

As well, the fraction of filled centres is given by

$$f_t = 1 - f_{tp} = \frac{1}{1 + \exp((E_t - E_F)/kT)} \quad (5.2)$$

where E_t = energy level of SRH centre

E_F = Fermi level of energy

p_o, n_o = steady-state hole and electron concentrations,
respectively

$$p_l = e_p/c_p = n_i \exp \left[(E_i - E_t)/kT \right] \quad (5.3)$$

$$n_l = e_n/c_n = n_i \exp \left[(E_t - E_i)/kT \right] \quad (5.4)$$

f_{tp} = fraction of unfilled SRH centres.

The variance of the charge fluctuation $q\delta n_t$ in an elemental volume can be calculated using either a statistical approach^{42,43,44} or a thermodynamical approach.⁴⁵ Both methods give (Appendix B)

$$\overline{\delta n_t^2} = \frac{N_t f_t f_{tp}}{\Delta \Lambda} \quad (5.5)$$

where N_t is the SRH centre concentration per unit volume, and $\Delta \Lambda$ is the elemental volume element.

The one-sided power spectral density of the noise which results from a single time constant process of this type can be obtained (Appendix B) by calculating the autocorrelation function and utilizing the Wiener-Khintchine theorem⁴⁶ to give

$$G(f) = \frac{\overline{4\delta n_t^2 \tau_t}}{1 + \omega^2 \tau_t^2} \quad (5.6)$$

where τ_t is the relaxation time constant for a particular trap level. Then for a system in which there are traps at many different levels, it can be shown^{49,76} that the spectrum

is inversely proportional to some power of the frequency, usually close to unity. This leads to the well-known $1/f$ noise quoted in the literature.

5.2 GENERATION-RECOMBINATION NOISE

Since the Weimer model of the FET assumes the substrate to be intrinsic, the channel-substrate depletion region does not enter into the calculations, and it is not meaningful to talk about noise from this mechanism. The analysis which follows applies only to the bulk charge model described in Chapter 2.

The calculation of the effects of fluctuations in the trap occupancy can be carried out by using the model shown in Fig. 5.2.

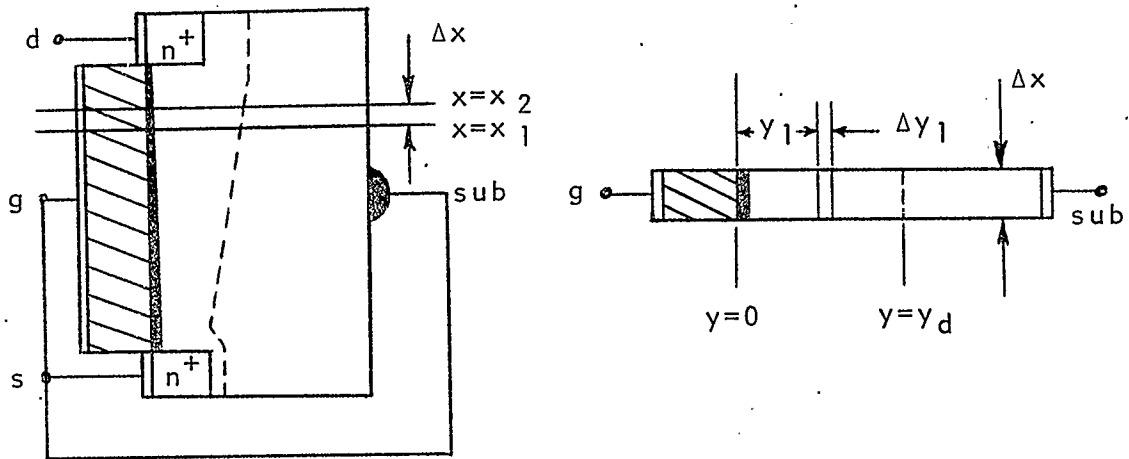


Fig. 5.2 An incremental length of channel used for calculating the noise voltage due to generation-recombination in the depletion region.

The charge density profile for the element of channel in Fig. 5.2 is shown in Fig. 5.3.

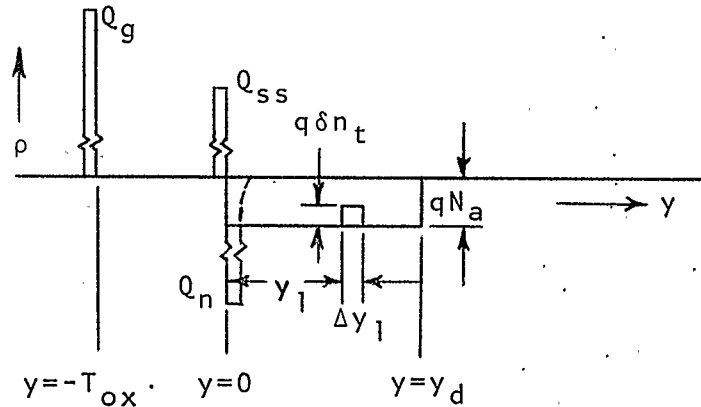


Fig. 5.3 Charge density profile of a Δx element of channel showing a fluctuation δn_t in an elemental volume $\Delta \Lambda$ in the depletion region.

The source, gate and substrate are ac short-circuited while the drain is open circuited for ac signals, and the channel is divided into three sections by the lines at $x = x_1$ and $x = x_2$. Fluctuations in n_t are permitted in a small elemental volume $\Delta \Lambda$ in the region between x_1 and x_2 but are assumed to be suppressed elsewhere in the region $x_1 \leq x \leq x_2$ as well as in the regions $0 \leq x < x_1$ and $x_2 < x \leq L$. The contribution to the total noise voltage at the drain due to fluctuations in n_t in the volume element $\Delta \Lambda$ is calculated, the volume element is reduced to a differential element $d\Lambda$, and the total noise at the drain due to fluctuations in n_t in the entire depletion region is calculated by performing a suitable integration.

The noise voltage due to a fluctuation δn_t in an elemental volume ΔA at $y = y_1$ can be obtained by examining the total potential from the metal to the bulk. The well-known moment formula is written as

$$\psi_{21} = \int_1^2 \frac{\rho}{\epsilon} y dy \quad (5.7)$$

so that a fluctuation δn_t in n_t in a small volume of width Δy causes an incremental fluctuation $\Delta(\delta\psi_{mb})$ in the potential from metal to bulk, given by

$$\Delta(\delta\psi_{mb}) = -\frac{q}{\epsilon_s} \delta n_t y \Delta y. \quad (5.8)$$

At the same time, the fluctuation δn_t gives rise to an incremental fluctuation in the bulk charge of magnitude

$$\Delta(\delta Q_B) = q \delta n_t \Delta y. \quad (5.9)$$

Under static conditions, the total potential of the bulk with respect to the metal is determined by taking moments about $y = 0$, so that

$$\psi_{bm} = -\frac{Q_g}{C_{ox}} + \int_0^{y_d} -\frac{qN_a}{\epsilon_s} y dy. \quad (5.10)$$

In addition, if Q_{ss} is assumed to be small,

$$Q_g + Q_n + Q_B = 0 \quad (5.11)$$

where

$$Q_B = -qN_a y_d. \quad (5.12)$$

Substituting (5.11) and (5.12) into (5.10) yields

$$\Psi_{bm} = \frac{Q_n}{C_{ox}} - \frac{qN_a y_d}{C_{ox}} - \frac{qN_a y_d^2}{2\epsilon_s} \quad (5.13)$$

Fluctuations in n_t then cause incremental fluctuations in Ψ , Q_n and y_d , so that

$$\begin{aligned} \Psi_{bm} + \Delta(\delta\Psi_{bm}) &= \frac{[Q_n + \Delta(\delta Q_n)]}{C_{ox}} - \frac{qN_a}{C_{ox}} [y_d + \Delta(\delta y_d)] \\ &\quad + \frac{q\delta n_t \Delta y}{C_{ox}} - \frac{qN_a}{2\epsilon_s} [y_d + \Delta(\delta y_d)]^2 + \frac{q}{\epsilon_s} \delta n_t y_d \Delta y. \end{aligned} \quad (5.14)$$

Neglecting second order terms and separating static and fluctuating components yields

$$\begin{aligned} \Delta(\delta\Psi_{bm}) &= \frac{\Delta(\delta Q_n)}{C_{ox}} - \frac{qN_a}{C_{ox}} \Delta(\delta y_d) + \frac{q\delta n_t \Delta y}{C_{ox}} - \frac{qN_a y_d}{\epsilon_s} \Delta(\delta y_d) \\ &\quad + \frac{q}{\epsilon_s} \delta n_t y_d \Delta y. \end{aligned} \quad (5.15)$$

Since the gate and bulk are ac short-circuited, $\delta\Psi_{bm} = 0$, and utilizing (2.52) to find δy_d in terms of δV yields

$$\Delta(\delta Q_n) = [\Delta(\delta V)] \left(\frac{\epsilon_s}{y_d} + C_{ox} \right) - q\delta n_t \Delta y \left(1 + \frac{C_{ox} y_d}{\epsilon_s} \right). \quad (5.16)$$

If I , Q , and V_t represent the total drain current, inversion charge and channel potential, respectively, then

$$I = I_d + \Delta(\delta I_d) \quad (5.17)$$

$$Q = Q_n + \Delta(\delta Q_n) \quad (5.18)$$

$$V_t = V + \Delta(\delta V) \quad (5.19)$$

where I_d , Q_n and V are the average values of I , Q and V_t and $\Delta(\delta I_d)$, $\Delta(\delta Q_n)$, $\Delta(\delta V)$ are incremental fluctuations in I , Q and V_t at any point x in the channel. For the regions $0 \leq x < x_1$ and $x_2 < x \leq L$, the drain current is written as

$$I = -\mu_n z Q \frac{dV_t}{dx} \quad (5.20)$$

Substitution of (5.17), (5.18) and (5.19) into (5.20) and retention of only first order fluctuations yields

$$\Delta(\delta I_d) = -\mu_n z \left\{ Q_n \frac{d[\Delta(\delta V)]}{dx} + [\Delta(\delta Q_n)] \frac{dV}{dx} \right\} \quad (5.21)$$

For open circuit conditions at the drain $\delta I_d = 0$ and (5.21) may be written as

$$\frac{d[\Delta(\delta V)]}{dQ_n} + \frac{[\Delta(\delta Q_n)]}{Q_n} \frac{dV}{dQ_n} = 0. \quad (5.22)$$

From the expression for the inversion charge Q_n given by (2.51) it is easy to show that

$$\frac{dQ_n}{dV} = \left(C_{ox} + \frac{\epsilon_s}{y_d} \right). \quad (5.23)$$

Substitution of (5.16) and (5.23) into (5.22) yields

$$\frac{d[\Delta(\delta V)]}{dQ_n} + \frac{\Delta(\delta V)}{Q_n} = \frac{q\delta n_t \Delta y \left(1 + \frac{C_{ox} y}{\epsilon_s} \right)}{Q_n \left(C_{ox} + \frac{\epsilon_s}{y_d} \right)}. \quad (5.24)$$

This is a linear first-order differential equation of the form

$$\frac{db}{da} + f(a)b = r(a) \quad (5.25)$$

with solution

$$b = e^{-h} \left[\int e^h r(a) da + A \right], \quad h = \int f(a) da \quad (5.26)$$

where A is an arbitrary constant.

Substitution of appropriate variables from (5.24) gives

$$\Delta(\delta V) = \frac{A}{Q_n} + \frac{1}{Q_n} q \delta n_t \Delta y \left(1 + \frac{C_{ox} y}{\epsilon_s}\right) V \quad (5.27)$$

which is valid in the region $x_1 \leq x \leq x_2$.

In order to solve for A, the boundary conditions are determined as follows:

Fluctuations in n_t are suppressed in the regions $0 \leq x < x_1$ and $x_2 < x \leq L$. Only fluctuations in I and V are allowed. Substitution of (5.17) to (5.19) into (5.20), expansion in series and retention of only first order terms yields, for $\delta I_d = 0$,

$$d[Q_n \Delta(\delta V)] = 0 \quad (5.28)$$

or

$$Q_n \Delta(\delta V) = \text{a constant.} \quad (5.29)$$

This can be seen more directly if it is noted that Q_n is an explicit function of the channel voltage V , so that

$$\Delta(\delta Q_n) = \frac{dQ_n}{dV} \Delta(\delta V). \quad (5.30)$$

Substitution of (5.30) into (5.21) for $\delta I_d = 0$ gives (5.28) directly.

At the source, $\delta V_s = 0$ so that

$$Q_{ns} \Delta(\delta V_s) = Q_{n1} \Delta(\delta V_1) = 0 \quad (5.31)$$

implies that the fluctuation $\Delta(\delta V_1)$ at $x = x_1$ is zero as well, since $Q_{n1} \neq 0$. Then from (5.27),

$$\Delta(\delta V_1) = 0 = \frac{A}{Q_{n1}} + \frac{1}{Q_{n1}} q \delta n_t \Delta y \left(1 + \frac{C_{ox} y}{\epsilon_s}\right) V_1 \quad (5.32)$$

and

$$A = -q \delta n_t \Delta y \left(1 + \frac{C_{ox} y}{\epsilon_s}\right) V_1. \quad (5.33)$$

Substituting (5.33) into (5.27) and examining δV at $x = x_2$ gives

$$\Delta(\delta V_2) = \frac{q \delta n_t \Delta y}{Q_{n2}} \left(1 + \frac{C_{ox} y}{\epsilon_s}\right) (V_2 - V_1). \quad (5.34)$$

If x_1 is now allowed to approach x_2 , then

$$V_2 - V_1 \rightarrow dV. \quad (5.35)$$

For the region $x_2 < x \leq L$, the condition (5.29) gives

$$Q_{n2} \Delta(\delta V_2) = Q_{nd} \Delta(\delta V_d) = Q_{nd} dv_{nd} \quad (5.36)$$

where dv_{nd} is the contribution to the drain noise voltage due to the fluctuation in the elemental volume $\Delta \Lambda$. Substituting for $Q_{n2} \Delta(\delta V_2)$ from (5.34) gives

$$\overline{dv_{nd}^2} = \frac{q^2 \overline{\delta n_t^2}}{Q_{nd}^2} \left[\left(1 + \frac{C_{ox} y}{\epsilon_s}\right) \Delta y \right]^2 (dV)^2. \quad (5.37)$$

The power spectral density of the noise is then obtained by utilizing (5.6) and noting that the fluctuations dv_{nd} are a result of fluctuations in n_t which are characterized by a single time constant process. The incremental voltage dV is found from (2.42) in terms of dx and I_d , and substituting for $\overline{\delta n_t^2}$ from (5.5) with $\Delta \Lambda = z dx dy$ yields

$$G_V(f) = \frac{4q^2 I_d^2 N_t}{\mu_n^2 z^3 Q_{nd}^2} \int_0^L \int_0^{y_d} \frac{\tau_t f_t f_{tp}}{1 + \omega^2 \tau_t^2} \frac{(1 + \frac{C_{ox} y}{\epsilon_s})^2}{Q_n^2} dy dx. \quad (5.38)$$

The short-circuit noise current spectrum at the drain, $G_I(f)$, can be obtained by multiplying $G_V(f)$ by the square of the output conductance g_o , where

$$g_o = - \frac{\mu_n z}{L} Q_{nd}. \quad (5.39)$$

The equivalent noise resistance R_n can then be obtained by noting that

$$G_I(f) = 4kTR_n g_m^2 \quad (5.40)$$

where

$$g_m = \frac{\mu_n z C_{ox}}{L} V_{ds}. \quad (5.41)$$

The integration with respect to y in (5.38) can be performed readily. If it is assumed that the electron and hole densities in the depletion region are small so that the trap fluctuation parameters τ_t , f_t and f_{tp} are constant, then using (5.38) to (5.41) and substituting for dx in terms of I_d and dV gives

$$R_n = \frac{-q^2 \tau_t N_t f_t f_{tp} \epsilon_s}{kT (1 + \omega^2 \tau_t^2) L z C_{ox}^3} \int_0^{V_{ds}} \frac{\theta(\frac{C_{ox} y_d}{\epsilon_s}) \left[1 + \frac{C_{ox} y_d}{\epsilon_s} + \frac{1}{3} \left(\frac{C_{ox} y_d}{\epsilon_s} \right)^2 \right] dV}{V_{ds}^2 \Gamma} \quad (5.42)$$

where

$$\frac{C_{ox} y_d}{\epsilon_s} = \frac{8\phi_F}{V_B} \left(1 + \frac{V}{2\phi_F} \right)^{\frac{1}{2}}. \quad (5.43)$$

Recently, Yau and Sah³¹ have shown that the assumption of constant τ_t , f_t and f_{tp} is reasonable and only becomes invalid for small gate and drain voltages. If the spatial dependences of f_t , f_{tp} and τ_t are to be taken into account, the expressions (5.1) and (5.2) must be used and the results become very complex for the bulk charge model.

Graphs of R_n as a function of gate and drain bias are shown in Figs. 5.4 and 5.5. It should be noted that the resistance diverges as saturation is approached. This is expected, since the calculations have been performed using the 'gradual channel' approximation. In order to obtain meaningful values of R_n in saturation, an attempt is made to derive a simple pinch-off theory for the device which will indicate the point at which the calculations should be terminated.

5.2.1 A Method of Preventing the Noise Resistance From Diverging at Pinch-Off

A comprehensive treatment of the operation of the bulk FET in the pinch-off mode has been presented by Trofimenkoff and Nordquist.⁴⁷ The calculations were carried out by obtaining the potential distribution along the centre line of the 'capacitor box' model for the pinched-off region near the drain, and then matching the potential and electric field as well as requiring that the charge density in the channel be continuous at the matching point near the drain.

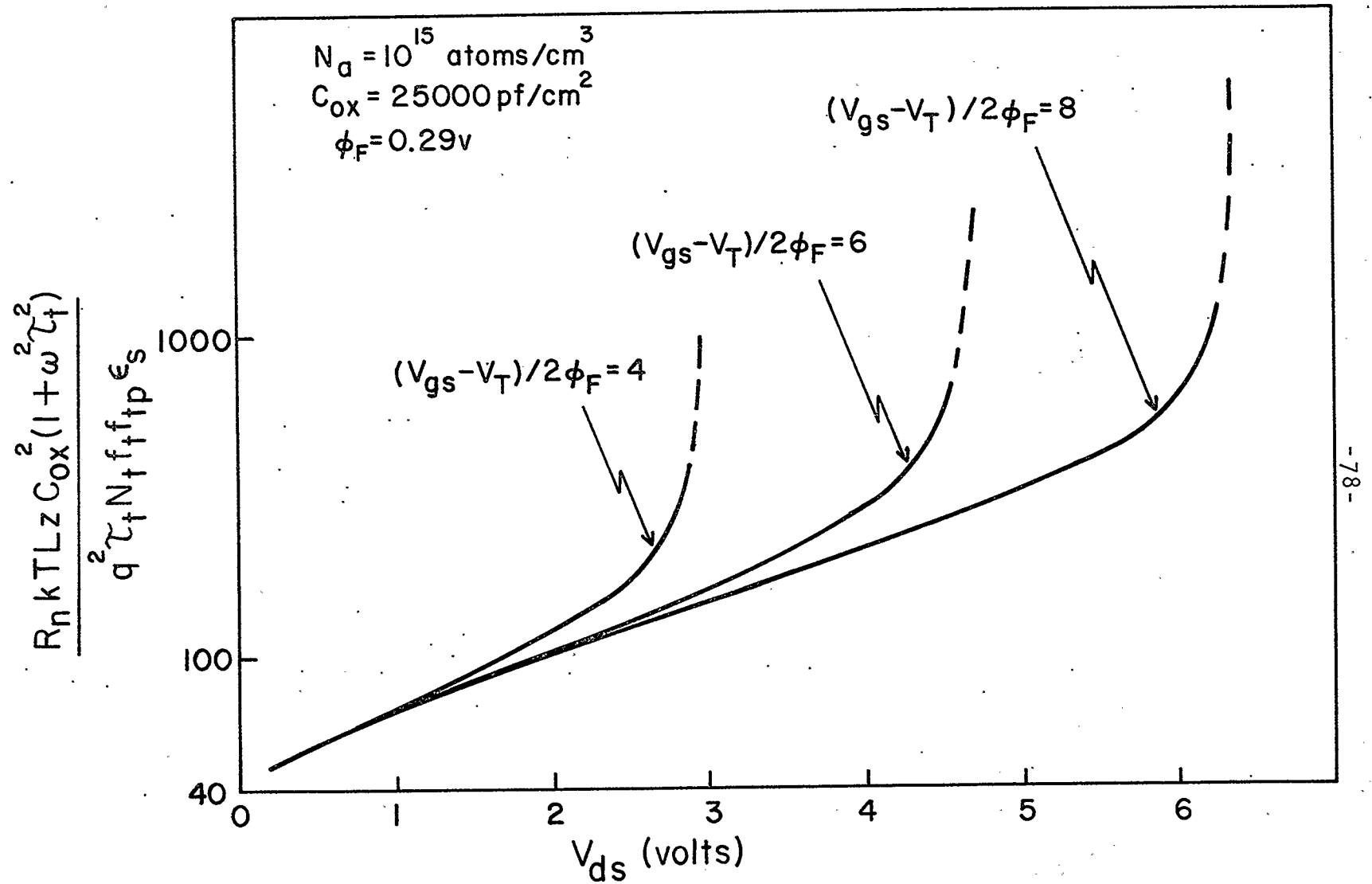


Fig. 5.4 Normalized R_n due to generation-recombination noise, as a function of bias.

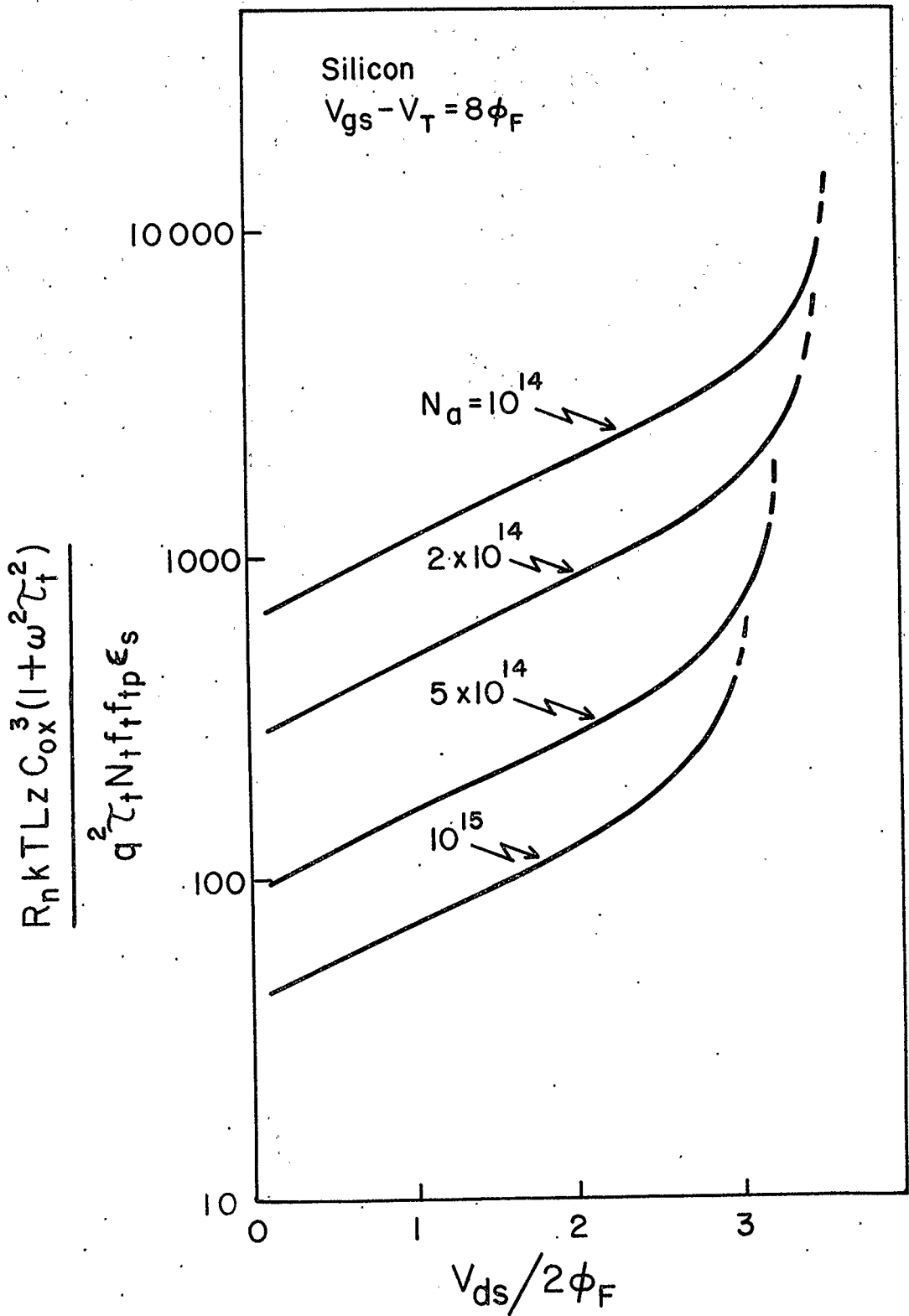


Fig. 5.5 Normalized R_n due to generation-recombination noise for various values of substrate doping.

A similar procedure may be used to obtain an approximate description of the operation of the MOS FET in saturation. Consider the drain end of the channel as shown in Fig. 5.6.

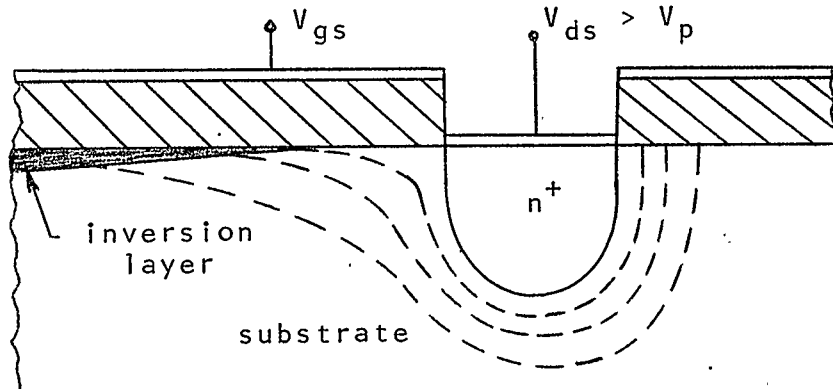


Fig. 5.6 Expanded view of the drain area showing equipotential lines.

The depletion region that exists around the n^+ drain diffusion is a result of the applied bias V_{ds} , if the substrate is at source potential. Thus the voltage throughout the region is spatially dependent. Under post pinch-off conditions, the channel is nearly depleted near the drain, and the electric field is high in this region, so that the equipotential lines will appear as shown. It is reasonable to assume that at some point $x = L_e$ in the channel depletion region near the drain there will exist a potential V_e such that conditions to the left and right of the point will be similar. If this is the case, potential calculations can be carried out using conventional p-n junction theory and a procedure similar to that used by Trofimenkoff and Nordquist⁴⁷ can be utilized to match conditions with those from the 'gradual approximation' which are valid for the inverted portion of the channel.

As a first order approximation it is assumed that the equipotential lines near the drain can be extended up to the oxide-semiconductor interface as shown in Fig. 5.7:

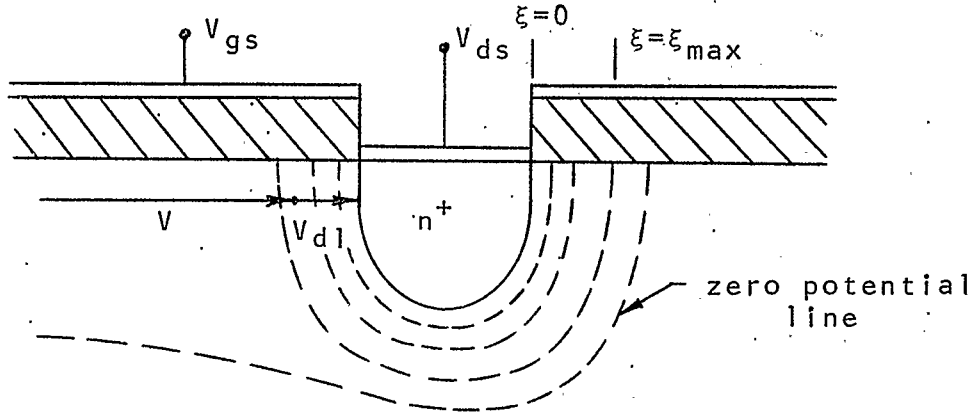


Fig. 5.7 Approximate form of the equipotential lines at the drain, used to calculate V_e and L_e .

Clearly the zero potential line cannot be extended, as this would require that the potential near the drain be zero at some point. Instead, it is assumed that there will exist some voltage $V_d < V_{ds}$ to which there will be a corresponding depletion width ξ_{max} . Then the point $x = L_e$ will be somewhere in the region between $\xi = 0$ and $\xi = \xi_{max}$ and this point will always occur such that $L - L_e < \xi_{max}$ and $V_e + V_{d1} = V_{ds}$, where $V_{d1} < V_d$. It should be noted that the source n^+ diffusion is in contact with the inversion layer, so that it is assumed that there is no potential drop from source to channel at $x = 0$.

The potential variation from $\xi = 0$ to $\xi = \xi_{max}$ can be obtained from the one dimensional Poisson's equation,

$$\frac{d^2\psi}{d\xi^2} = -\frac{\rho}{\epsilon_s} \approx -\frac{qN_a}{\epsilon_s} \quad (5.44)$$

The solution of (5.44) is obtained using $\psi = 0$ at $\xi = 0$ and $\frac{d\psi}{d\xi} = 0$ at $\xi = \xi_{\max}$ as boundary conditions. This gives

$$\psi = -V_{dt} \frac{\xi}{\xi_{\max}} \left[2 - \frac{\xi}{\xi_{\max}} \right] \quad (5.45)$$

where $V_{dt} = V_d - \psi_0$

ψ_0 = equilibrium contact potential

$\xi = L - x$

$$\text{and } \xi_{\max} = \sqrt{\frac{2\epsilon_s V_{dt}}{qN_a}} \quad (5.46)$$

The potential V (with respect to the source) at any point in the region between $\xi = 0$ and $\xi = \xi_{\max}$ is then given by

$$V - (\psi - \psi_0) = V_{ds} \quad (5.47)$$

Substituting (5.45) into (5.47) and taking first and second derivatives with respect to x yields

$$V + V_{dt} \frac{\xi}{\xi_{\max}} \left[2 - \frac{\xi}{\xi_{\max}} \right] = V_{dst} \quad (5.48)$$

$$\frac{dV}{dx} = -\frac{2V_{dt}}{\xi_{\max}} \left[\frac{L-x}{\xi_{\max}} - 1 \right] \quad (5.49)$$

$$\frac{d^2V}{dx^2} = \frac{qN_a}{\epsilon_s} \quad (5.50)$$

where $V_{dst} = V_{ds} - \psi_0$.

From the prepinch-off or gradual theory, (2.42) and (2.51) yield

$$\frac{dV}{dx} = -\frac{I_d}{\mu_n z Q_n} \quad (5.51)$$

$$\frac{d^2V}{dx^2} = \frac{I_d C_{ox}}{\mu_n z Q_n^2} \left[1 + \frac{V_B}{4\phi_F \left(1 + \frac{V}{2\phi_F}\right)^{\frac{1}{2}}} \right] \frac{dV}{dx} \quad (5.52)$$

It is required that V , $\frac{dV}{dx}$ and $\frac{d^2V}{dx^2}$ be continuous at $x = L_e$, so that (5.48) to (5.52) give

$$V_{dst} - V_e = \frac{V_{dt}(L-L_e)}{\xi_{max}} \left[2 - \frac{(L-L_e)}{\xi_{max}} \right] \quad (5.53)$$

$$\frac{2V_{dt}}{\xi_{max}} \left[\frac{L-L_e}{\xi_{max}} - 1 \right] = \frac{I_d}{\mu_n z Q_{ne}} \quad (5.54)$$

$$\frac{qN_a}{\epsilon_s} = \left[\frac{V_B}{4\phi_F \left(1 + \frac{V_e}{2\phi_F}\right)^{\frac{1}{2}}} + 1 \right] \frac{I_d^2 C_{ox}}{(\mu_n z)^2 (-Q_{ne})^3} \quad (5.55)$$

where

$$I_d = \frac{\mu_n z C_{ox}}{L_e} \left\{ V_e (V_{gs} - V_T + V_B) - \frac{V_e^2}{2} - \frac{4}{3} \phi_F V_B \left[\left(1 + \frac{V_e}{2\phi_F}\right)^{\frac{3}{2}} - 1 \right] \right\} \quad (5.56)$$

$$Q_{ne} = C_{ox} \left[V_B \left(1 + \frac{V_e}{2\phi_F}\right)^{\frac{1}{2}} - (V_{gs} - V_T + V_B - V_e) \right] \quad (5.57)$$

Equations (5.53) to (5.57) are then sufficient to describe the operation of the FET in the pinch-off mode.

If the matching procedure is correct, the output conductance for post pinch-off conditions should match with that for the pre-pinch off case. Utilizing (5.53) to (5.57), the output conductance for post-saturated conditions is found from

$$g_o = \frac{\partial I_d}{\partial V_{ds}} = \frac{\partial I_d}{\partial L_e} \frac{\partial L_e}{\partial V_{ds}} + \frac{\partial I_d}{\partial V_e} \frac{\partial V_e}{\partial V_{ds}} \quad (5.58)$$

and straightforward manipulation leads to

$$R_o = \frac{L}{-\mu_n z Q_{ne}} + \frac{qN_a}{\epsilon_s} \frac{L_e}{I_d} (L - L_e). \quad (5.59)$$

At first glance it appears that (5.59) would match with R_o for the pre-pinch-off case when $L = L_e$ and $V_e = V_{ds}$. However, the model has been chosen such that L_e will never equal L , and V_e can never equal V_{ds} , as it could for the bulk FET. Thus it is difficult to match the output conductance for the pre-pinch-off case with the value calculated using (5.59).

The noise calculations can now be terminated at V_e , rather than V_p . Although it is difficult to obtain explicit expressions for V_e and L_e , results can be obtained numerically as follows.

Substituting for ξ_{max} from (5.46) into (5.54) yields

$$\sqrt{\frac{2qN_a V_{dt}}{\epsilon_s}} = \frac{qN_a}{\epsilon_s} (L - L_e) - \frac{I_d}{\mu_n z Q_{ne}}. \quad (5.60)$$

Noting that (5.53) may be written as

$$V_{dst} - V_e = (L - L_e) \left[\left(\frac{2qN_a V_{dt}}{\epsilon_s} \right)^{\frac{1}{2}} - (L - L_e) \frac{qN_a}{2\epsilon_s} \right] \quad (5.61)$$

it is apparent that V_{dt} may be eliminated by substituting from (5.60) to yield

$$V_{dst} - V_e = \frac{qN_a}{2\epsilon_s} (L - L_e)^2 - \frac{I_d}{\mu_n z Q_{ne}} (L - L_e) \quad (5.62)$$

and solving the quadratic for $(L - L_e)$ gives

$$L - L_e = \frac{\epsilon_s I_d}{q N_a \mu_n z Q_{ne}} \left(1 \pm \left[1 + \frac{2 q N_a (\mu_n z Q_{ne})^2}{\epsilon_s I_d} (V_{dst} - V_e) \right]^{\frac{1}{2}} \right) \quad (5.63)$$

where the negative root is retained since Q_{ne} is negative, the term inside the radical is always greater than unity and L_e must be less than L . Values for V_e can be obtained using an iterative procedure by starting with $L_e = L$ in (5.55) and (5.56), substituting the value of V_e obtained into (5.63), using the new value of L_e obtained to recalculate V_e and continuing the procedure to obtain the desired tolerance. Curves obtained using this procedure for a typical device are shown in Figs. 5.8, 5.9, 5.10 and 5.11. The effects of channel shortening are only appreciable at low values of substrate doping, as expected.

5.2.2 Application of the Pinch-Off Theory

The noise calculations can now be terminated at the point V_e , and if it is assumed that R_n remains constant past pinch-off, the normalized generation noise appears as shown in Fig. 5.12 for various values of gate voltage. Figure 5.13 represents the generation noise as a function of substrate doping at pinch-off.

5.2.3 Suggestions for Reducing the Noise

From Fig. 5.13, it is observed that for a constant trap density N_t , the noise may be decreased significantly if the substrate doping is increased. This may be due to the decrease in the depletion width which results in less effective trapping sites in the substrate. Unfortunately,

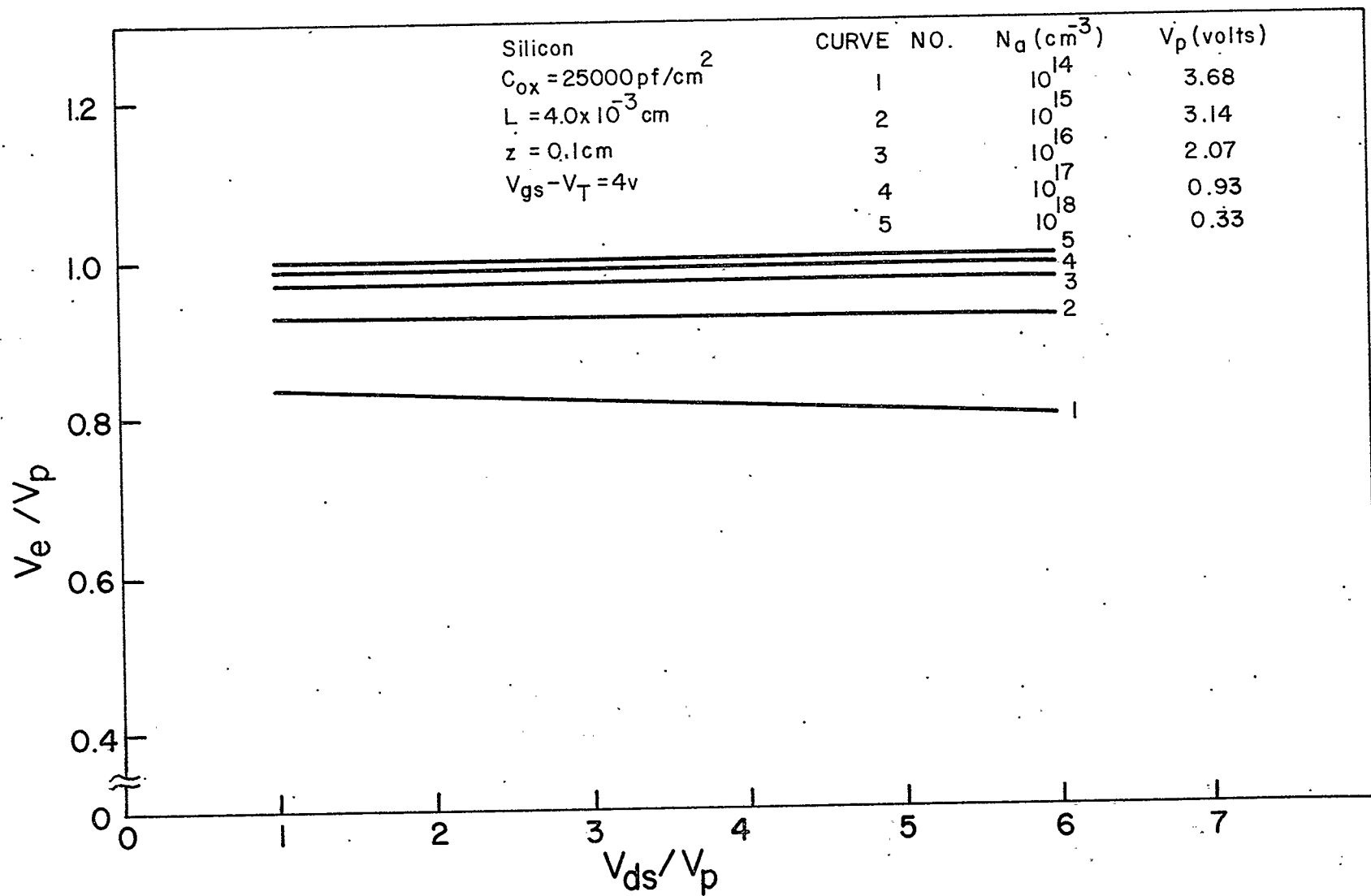


Fig. 5.8 V_e as a function of V_{ds} with substrate doping as a parameter.

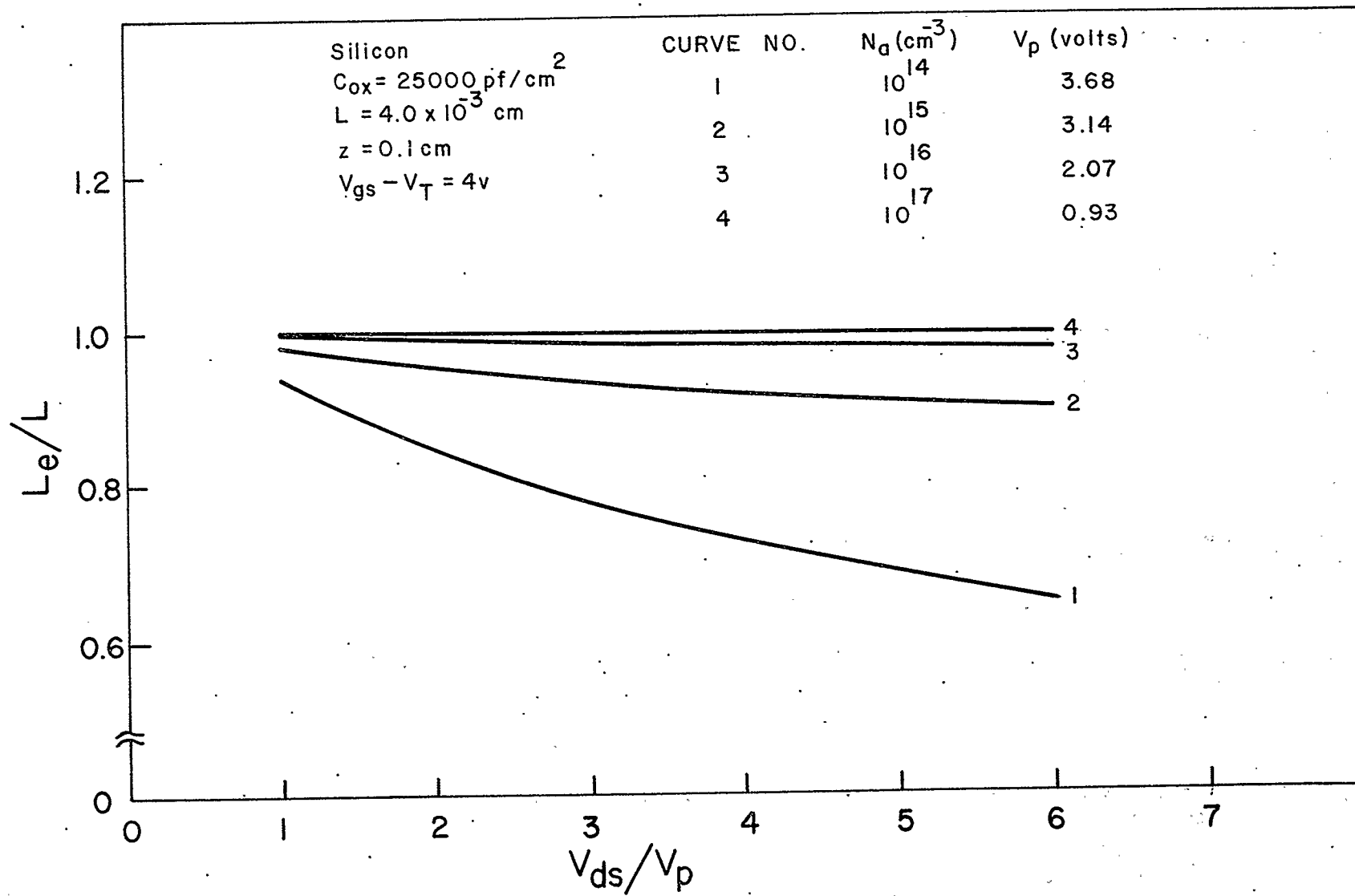


Fig. 5.9 L_e as a function of V_{ds} with substrate doping as a parameter.

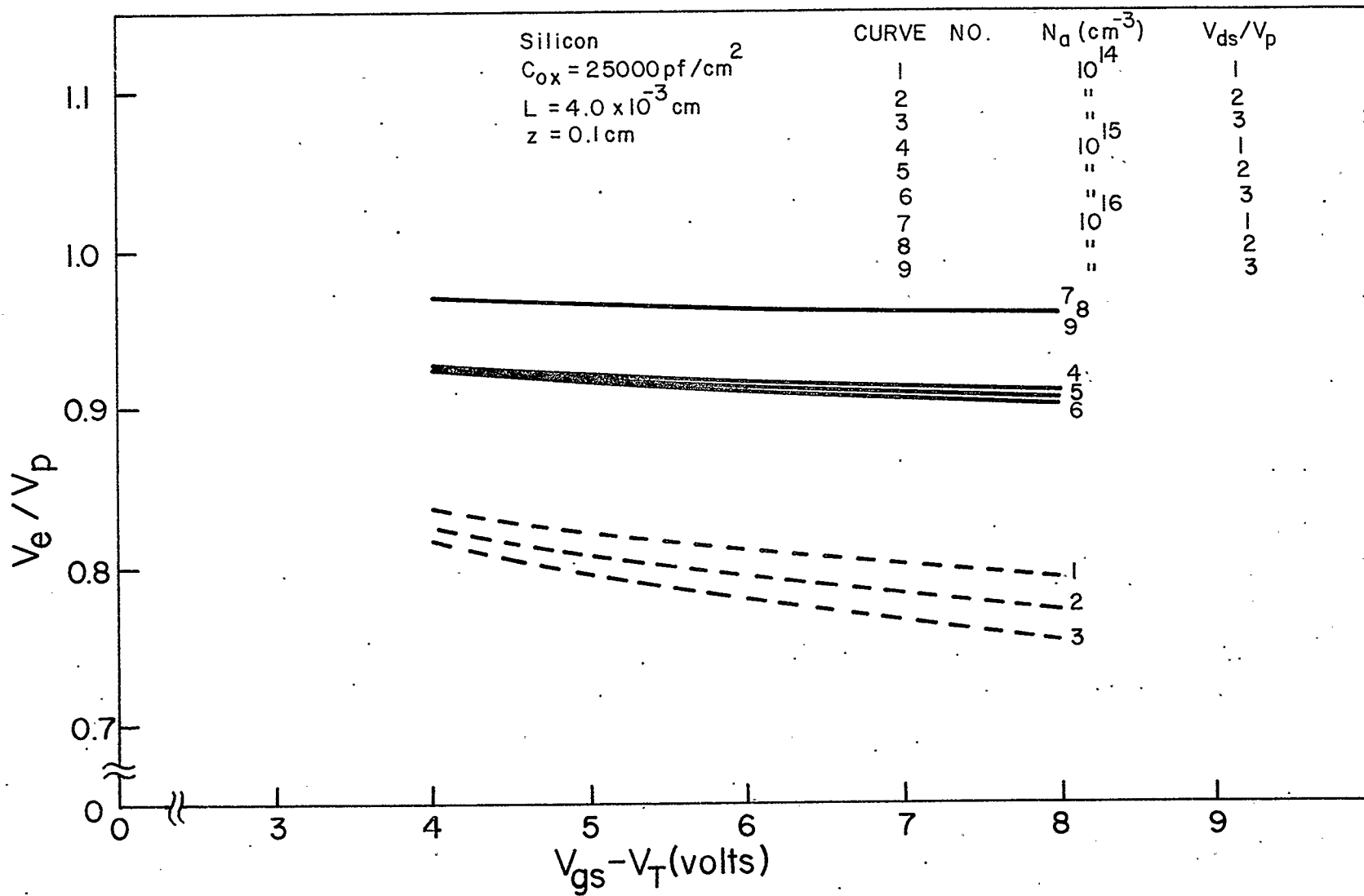


Fig. 5.10 V_e as a function of V_{gs} with V_{ds} as a parameter.

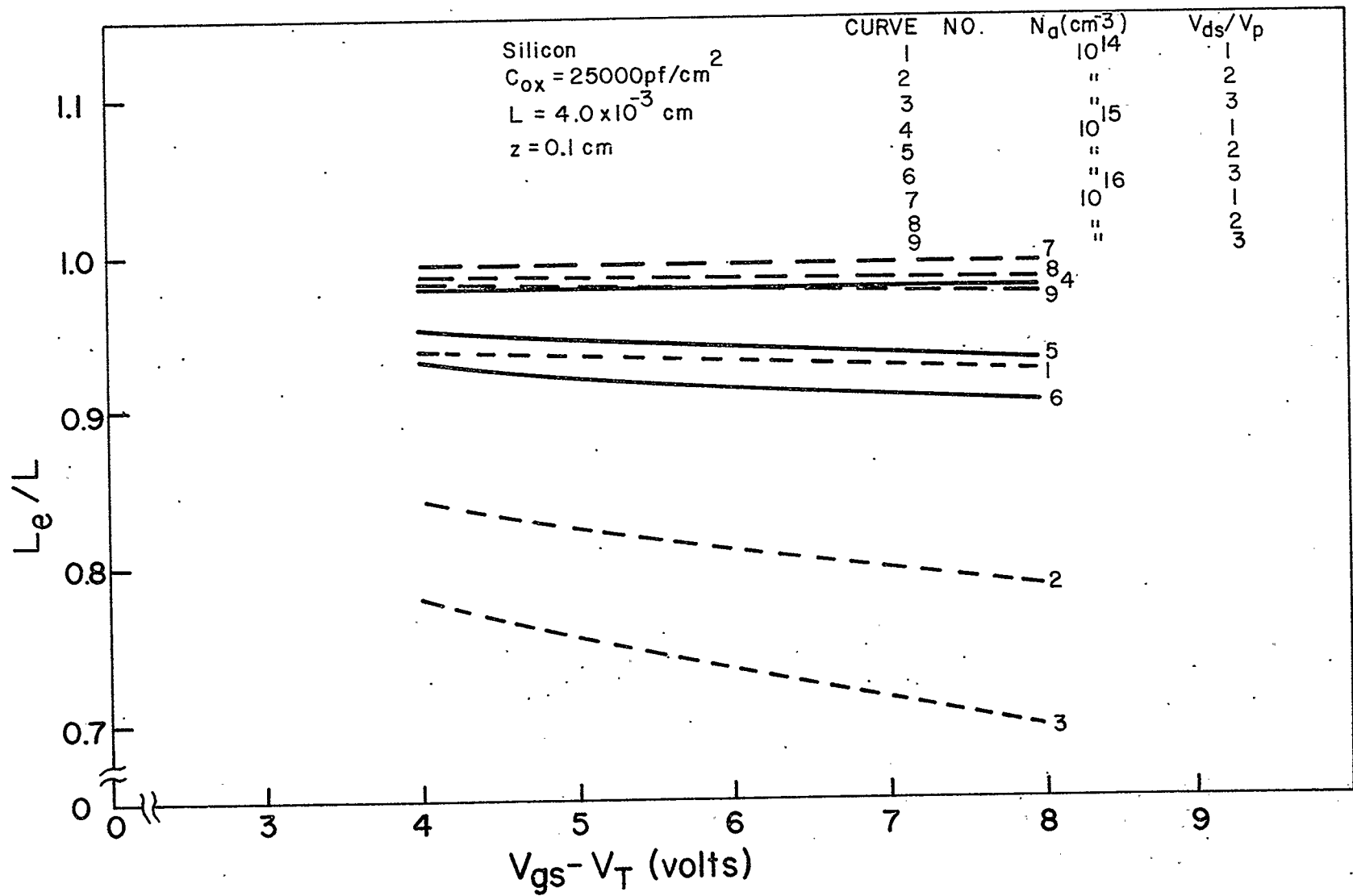


Fig. 5.11 L_e as a function of V_{gs} with V_{ds} as a parameter.

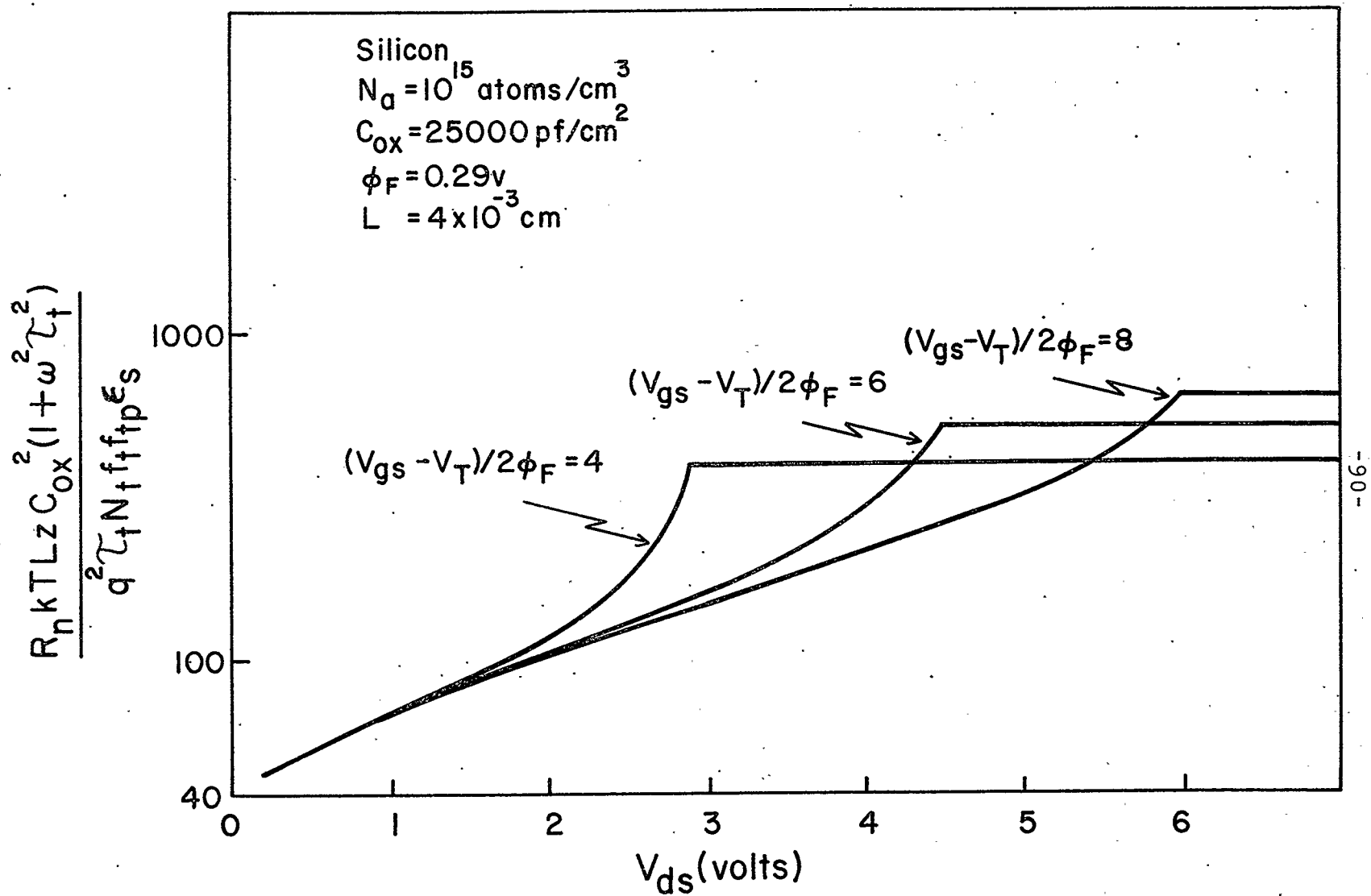


Fig. 5.12 Generation noise as a function of V_{ds} using the pinch-off theory.

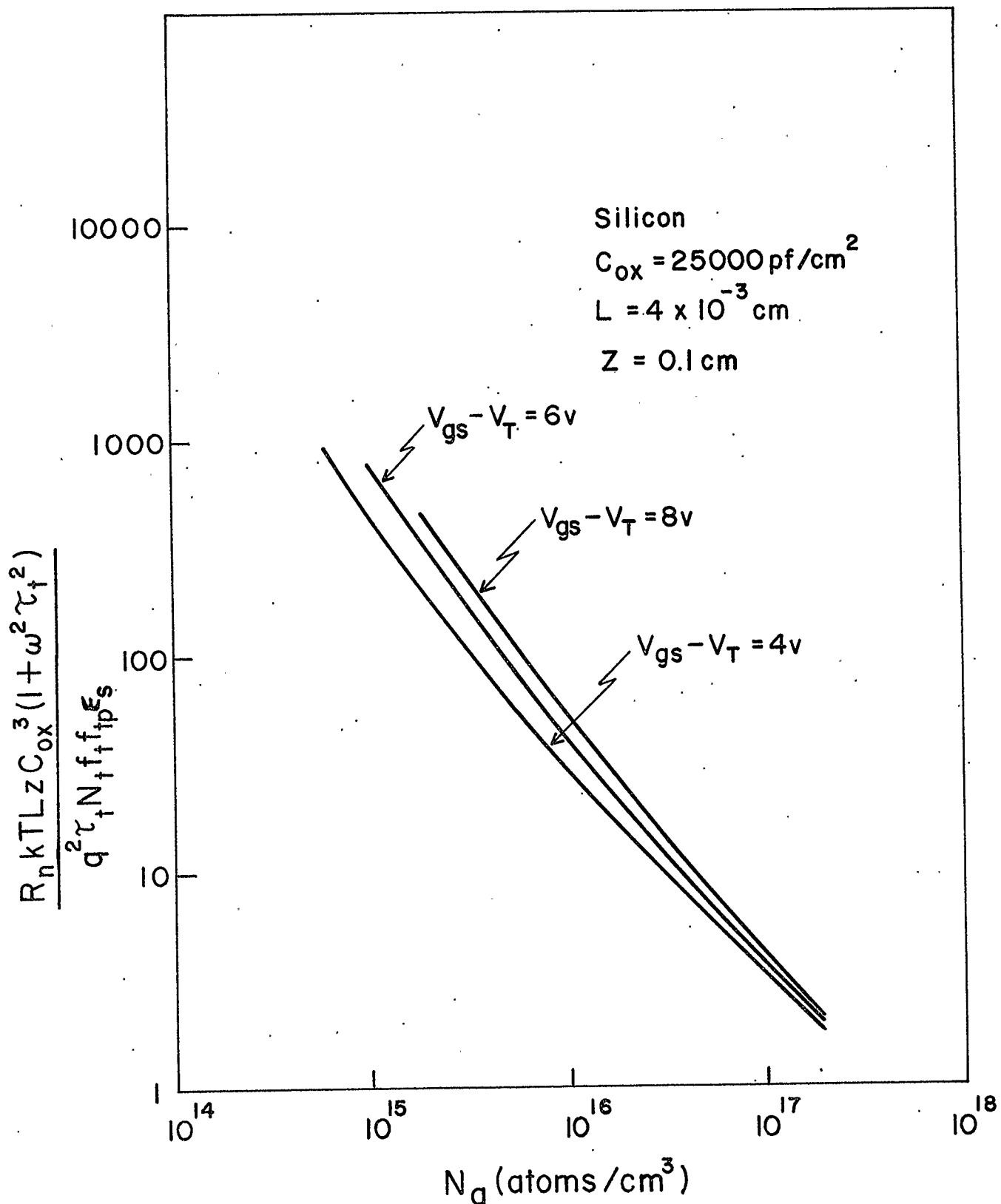


Fig. 5.13 Normalized generation noise resistance as a function of doping at pinch-off.

higher substrate doping has undesirable effects on the electrical characteristics of the device, so that a compromise must be reached in trying to reduce noise in this manner. An alternative approach would be to increase the gate area, but again, a compromise must be reached when using this technique since the electrical characteristics of devices with large gate areas are usually undesirable.

5.3 SURFACE STATE NOISE

The effects of surface states on the energy band configuration in the semiconductor were discussed in section 2.2.3. Trapped charges within the oxide as well as charges at the oxide-semiconductor interface cause band bending to occur at the surface of the semiconductor. Fluctuations in the occupancy of the surface states appear to contribute largely to the low-frequency noise in MOS FET's.^{22,26,27,29,48,49} For a single time constant fluctuation in the surface state occupancy, it has been shown that the noise spectrum is invariant with frequency at low frequencies, and varies with $1/f^2$ at higher frequencies. However, experimental results indicate that the noise actually varies inversely with frequency over a large range of frequencies. It can be shown quantitatively that a large dispersion in time constants will produce this type of a result.⁴⁹ A number of different mechanisms have been proposed that will result in the interface state time constant dispersion necessary to produce the $1/f$ type nature of the noise spectrum.^{29,48,49,50,51} It is

generally accepted that the dispersion in time constants originates from capture and emission of bulk minority carriers, since fluctuations in bulk majority carriers only give a $1/f$ spectrum over a narrow range of frequencies.⁵¹ Leventhal³⁷ postulates carrier motion in a surface band, assuming that the surface states form a continuous band of conducting states. Nicollian and Melchoir⁴⁸ assume that the distribution of trapping times can be explained by a random distribution of surface potential caused by a random distribution over the plane of the interface of fixed charges located in the oxide. Jäntschi⁵¹ postulates modulation of surface recombination by dissociation of the chemisorbed molecules from their active centres. Bess^{50,56} also assumes a Brownian motion of impurity atoms at the surface. Recently, an analysis of surface state noise in MOS FET's has been presented using the Weimer model of the device and utilizing the concept of minority carrier tunneling to traps located inside the oxide.^{29,49,72} The analysis is oversimplified and does not consider the effects of the substrate on the noise. Rather than trying to postulate a new mechanism for the $1/f$ noise, this model is considered in detail in this work. The effects of the substrate and of different trap distributions on the spectrum are analyzed in detail to improve the previous theory and test its validity.

5.3.1 The Tunneling Model

The theory of carrier tunneling to traps located on

the surface of the oxide layer on germanium filaments was first introduced by McWhorter.⁴⁹ Heiman and Warfield⁷² later used the same approach to analyze the effects of oxide traps on the MOS capacitance. Recently, Christensson et al²⁹ applied the theory to p-channel MOS transistors. This 'simple' theory is reviewed in Appendix C for an n-channel device. It is shown that the equivalent noise resistance R_n due to surface state noise can be written, in general, as

$$R_n \approx \frac{-q^2 \pi \Theta}{2kTLzC_{ox}^2 \alpha \omega V_{ds}^2} \int_0^{V_{ds}} \int_{E_v}^{E_c} \frac{N_t(E) f_t f_{tp}}{\Gamma} dE dV, \quad (5.64)$$

or for traps at a single energy level,

$$R_n \approx \frac{-q^2 N_o \pi \Theta}{2kTLzC_{ox}^2 \alpha \omega V_{ds}^2} \int_0^{V_{ds}} \frac{f_t f_{tp}}{\Gamma} dV \quad (5.65)$$

where $N_t(E)$ = trap density per unit volume per electron volt in the oxide

N_o = volume density of traps when the distribution is uniform over distance into the oxide at a single energy level

and α is a constant. The $f_t f_{tp}$ product is obtained from (5.2), and, in general,

$$f_t f_{tp} = \frac{p_1 p_s + n_1 n_s + \gamma (n_i^2 + n_s p_s)}{[n_s + n_1 + \gamma (p_s + p_1)]^2} \quad (5.66)$$

where $\gamma = c_p / c_n$, assumed to be unity in all cases

c_p = hole capture probability of a surface state

c_n = electron capture probability of a surface state

p_s = hole concentration per unit volume at the interface

n_s = electron concentration per unit volume at the interface

p_1, n_1 = hole and electron concentrations per unit volume in the valence and conduction bands, respectively, when the Fermi level coincides with the trap energy, E_t .

In order to evaluate the integrals in (5.64) and (5.65), it is necessary to know the variations in n_s and p_s with distance along the channel, and also to know the dependence of n_s on gate voltage at the source. The theory presented by Christensson et al²⁹ assumes that n_s may be described by

$$n_s = \frac{n_{os}(V_p - V)}{V_p} \quad (5.67)$$

where n_{os} = electron concentration per unit volume at the interface at the source

$V_p = V_{gs} - V_T$, the pinch-off voltage for the Weimer model

and V is the channel potential at any point x in the channel, with respect to the source. Equation (5.67) indicates that the electron concentration disappears at the drain when $V_{ds} = V_p$. If it is further assumed that $n_s n_1 > n_i^2$ everywhere when applying (5.66), the integrals in (5.64) and (5.65) are convergent for all values of V_{ds} . The magnitude of the noise can then be evaluated using a typical value for n_{os} . Traps

at four different energy locations have been considered, as described in Appendix C. The results can be summarized briefly as follows.

Case (a). Traps at the conduction band edge at the interface.

For traps at this single energy level, the use of (5.66) and (5.67) in (5.65) yields the voltage dependent portion of R_n , given by

$$F(V_{ds}) \approx \frac{n_{os}}{n_i} \frac{(2V_p - V_{ds})}{2V_p} . \quad (5.68)$$

This indicates that the noise decreases with increasing drain voltage prior to pinch-off, and increases with increasing gate voltage for a given drain voltage.

Case (b). Traps at the electron quasi-Fermi level at the source.

In this case, it is found that

$$F(V_{ds}) \approx \frac{1}{4} \quad (5.69)$$

and the noise is independent of bias.

Case (c). Traps at midgap at the interface.

With traps at the intrinsic Fermi level the voltage dependent portion of R_n becomes

$$F(V_{ds}) \approx \frac{n_i}{2n_{os}} \frac{(2V_p - V_{ds})}{(V_p - V_{ds}) + \frac{2n_i}{n_{os}}(2V_p - V_{ds})} . \quad (5.70)$$

the energy band diagram at a point x in the channel will appear as shown in Fig. 5.14.

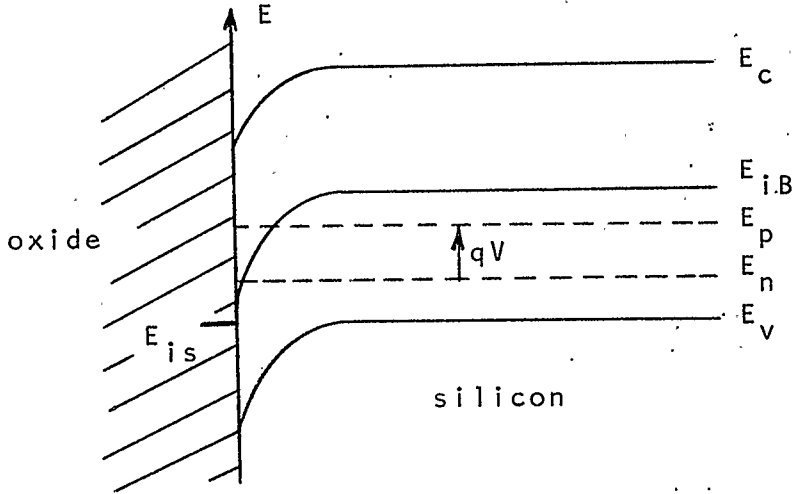


Fig. 5.14 Energy band diagram at a point x in the channel.

From (2.9) and (2.10), the electron and hole concentration can be written as

$$p = n_i \exp [q(\phi_p - \Psi)/kT] \quad (5.72)$$

$$n = n_i \exp [q(\Psi - \phi_n)/kT] \quad (5.73)$$

where $\Psi = -E_i/q \quad (5.74)$

and $\phi = -E_F/q. \quad (5.75)$

Poisson's equation is given by

$$\nabla^2 \Psi = \frac{-q}{\epsilon_s} (p - n + N_d - N_a). \quad (5.76)$$

Substituting for p and n , noting that ϕ_p and ϕ_n are approximately constant in the substrate yields

$$\nabla^2 U' = \frac{1}{(L_d')^2} \left[\sinh U' + \frac{N_a}{2n_i} \exp\left(\frac{qV}{kT}\right) \right] \quad (5.77)$$

where

$$U' = \frac{q}{kT} \left[\psi - \frac{1}{2}(\phi_p + \phi_n) \right] \quad (5.78)$$

and

$$(L_d')^2 = \frac{kT\epsilon_s}{2q^2 n_i} \exp\left(\frac{qV}{kT}\right) \quad (5.79)$$

In addition, in the bulk

$$U_B' = -\ln\left(\frac{N_a}{n_i}\right) - \frac{qV}{2kT} \quad (5.80)$$

Equation (5.77) cannot be integrated directly with respect to x . However, if it is noted that

$$\frac{\partial}{\partial x} \left(\frac{\partial U'}{\partial x} \right)^2 = \frac{2 \partial U'}{\partial x} \left(\frac{\partial^2 U'}{\partial x^2} \right), \quad (5.81)$$

then the square of the normal field at the surface, \mathcal{E}_y , given by $\left(\frac{\partial U'}{\partial x}\right)^2$, can be obtained by direct integration of (5.77) with respect to U' . Using Gauss' law to find the equivalent surface charge per unit area, Q_s , yields

$$Q_s = -\epsilon_s \mathcal{E}_y = -2qn_i L_d' \exp\left(\frac{-qV}{2kT}\right) \left\{ 2 \left[\cosh U_s' - \cosh U_B' + (U_s' - U_B') \frac{N_a}{2n_i} \exp\left(\frac{qV}{2kT}\right) \right] \right\}^{\frac{1}{2}} \quad (5.82)$$

The surface electron concentration is obtained from

$$n_s = n_i \exp\left[\left(\psi_s - \phi_n\right) \frac{q}{kT}\right] = n_i \exp\left[\left(E_n - E_{is}\right)/kT\right] \quad (5.83)$$

From Fig. 5.14, $E_p - E_n = qV$, and U_s' , U_B' can be written as

$$U'_s = \frac{1}{2kT} (E_p - E_{is} + E_n - E_{is}) \quad (5.84)$$

$$U'_B = \frac{1}{2kT} (E_p - E_{iB} + E_n - E_{iB}) \quad (5.85)$$

so that

$$U'_s - U'_B = \ln\left(\frac{N_a n_s}{n_i^2}\right) + \frac{qV}{kT} \quad (5.86)$$

Substituting for U'_B from (5.80) yields

$$n_s = \frac{n_i^2}{N_a} \exp\left[U'_s + \ln\left(\frac{N_a}{n_i}\right) - \frac{qV}{2kT}\right] = n_i \exp(U'_s - \frac{qV}{2kT}) \quad (5.87)$$

Using the depletion width concept, the surface charge can be related to the threshold voltage by using

$$Q_s = Q_n + Q_B \quad (5.88)$$

where Q_n is given by (2.51) and

$$Q_B = -qN_a y_d \quad (5.89)$$

where y_d is given by (2.52), assuming $V_{bs} = 0$.

The procedure for calculating n_s for a particular N_a and V is to calculate U'_B from (5.80), calculate Q_s from (5.88) for a given value of $V_{gs} - V_T$, and then require that the value given by (5.88) agree with that given by (5.82), iterating U'_s until the desired tolerance is obtained. Substitution of the final value of U'_s into (5.87) yields n_s directly. A graph of n_{os} as a function of $V_{gs} - V_T$ for various values of N_a may be obtained using the above procedure with $V = 0$. The results are given in Fig. 5.15.

It is possible to approximate n_s by writing

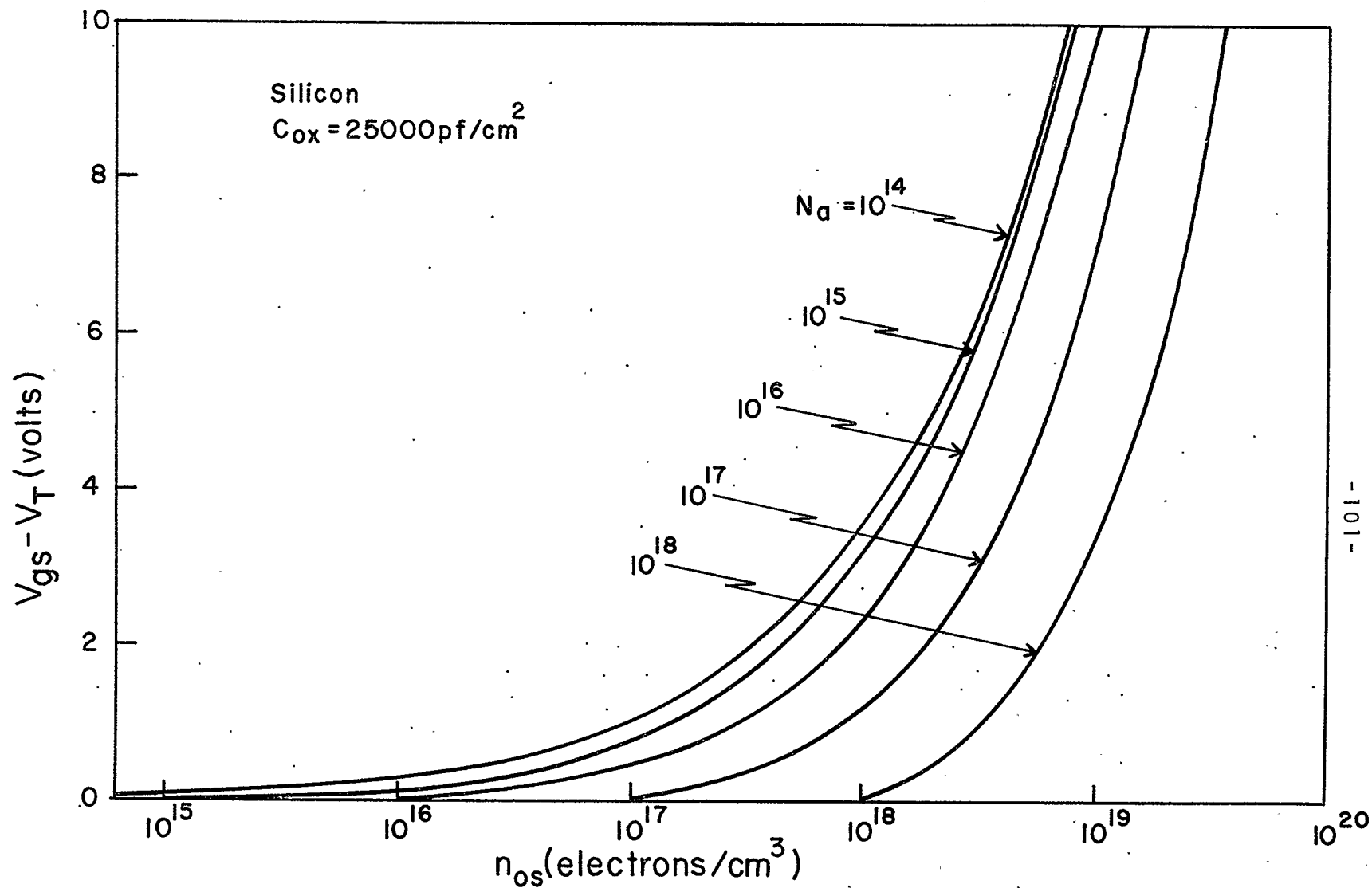


Fig. 5.15 Variation of the electron concentration per unit volume at the interface at the source with varying gate bias.

$$n_s = \frac{n_{os} [-Q_n]}{C_{ox} (V_{gs} - V_T)} \quad (5.90)$$

using the same type of an approximation as (5.67). This approximate solution is compared with the improved solution in Fig. 5.16, for a typical device. It can be seen that in mid-channel, the error is of the order of a factor of two, while at the drain, where $V_{ds} = V_p$, the improved solution yields $n_s = N_a$ while the approximation says $n_s = 0$. It will be shown in the following calculations that the approximate solution can be very misleading if the procedure adopted by Christensson et al²⁹ is used.

5.4.2 The Improved Theory

The theory of trapping by surface states can now be examined, since the electron concentration at the interface is known. It is important to note that carriers in the inversion layer near the interface may be trapped, as well as carriers directly at the interface. The present theory assumes that the density of carriers to be trapped is given by n_s . This is a reasonable assumption, since the largest portion of mobile carriers is very near the interface. (The channel thickness concept has recently been discussed by Gnädinger and Talley¹⁰⁰.) The necessary data required for the calculation of the surface state noise is then available. The four cases mentioned previously will be considered.

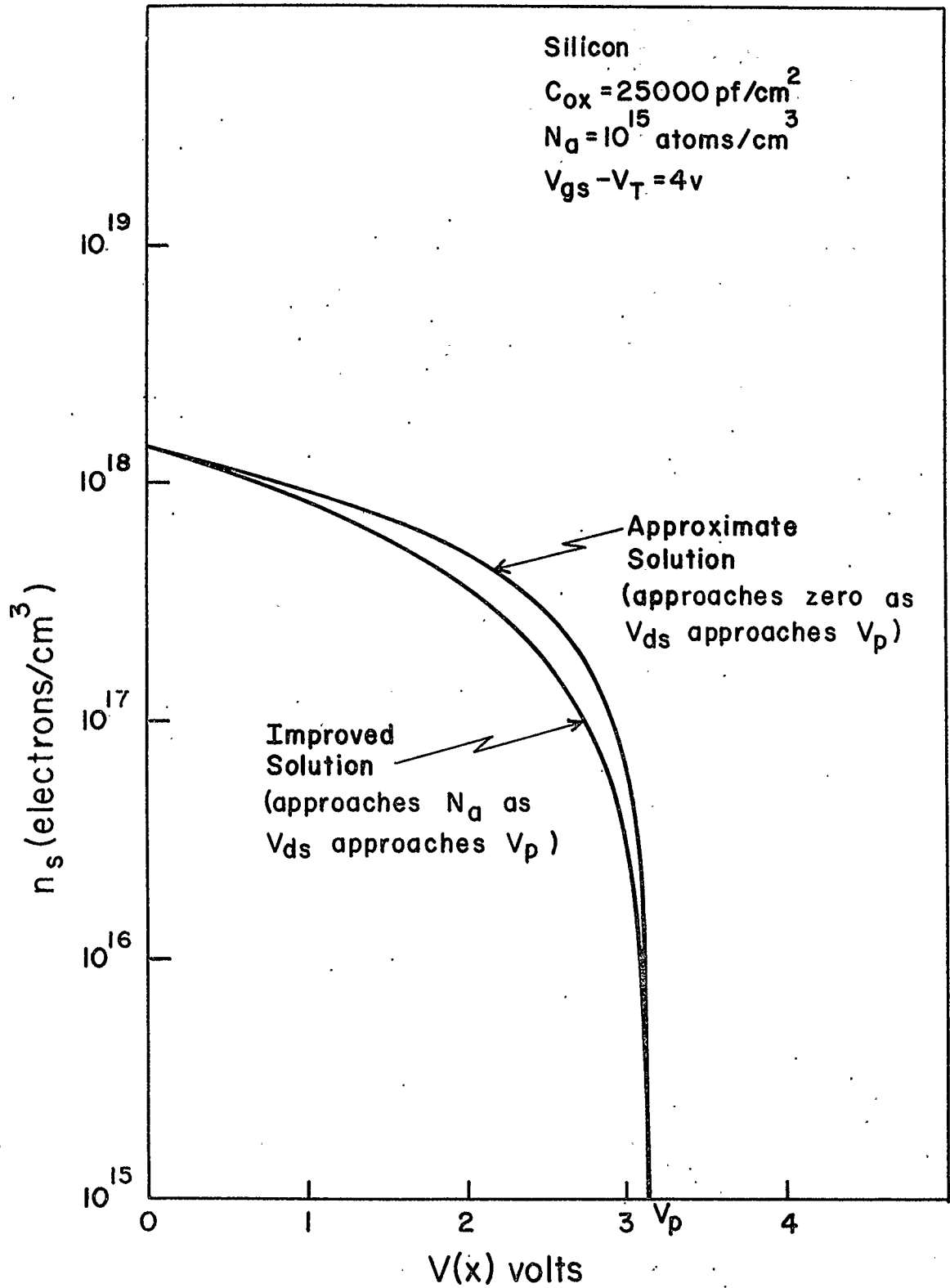


Fig. 5.16 Electron concentration at the interface along the channel at pinch-off.

Case (a). Traps at the conduction band edge.

When $E_t = E_c$, it can be shown (Appendix C) that $n_1 > n_s \gg p_1$, and (5.66) is almost exactly given by

$$f_t f_{tp} \approx \frac{n_1 n_s}{(n_1 + n_s)^2} \quad (5.91)$$

where

$$n_1 \approx n_i \exp(E_g/2kT) \quad (5.92)$$

and $E_g/2 \approx 0.555$ eV for silicon.

Equation (5.65) may be evaluated using (5.91). The procedure is complicated, since at each interval of the integration the iterative procedure must be employed to calculate n_s . This can be readily achieved using numerical techniques, and results are shown in Figs. 5.17, 5.18 and 5.19. The difference between the approximate and the improved theory is not appreciable in this case. However, it should be noted that at low values of N_a , the value of n_{os} is strongly dependent on the gate voltage, so that the overall level of the noise will increase by an order of magnitude as V_{gs} increases from just above threshold to some larger value. This must be kept in mind when comparing noise from this trap level with others in the gap.

The calculations have been performed using the pinch-off theory of section 5.2.1 with $V_{ds} = V_p$. The noise should theoretically increase past pinch-off due to the effects of channel shortening, particularly at low values of N_a . This dependence can be obtained using the results of section 5.2.1.

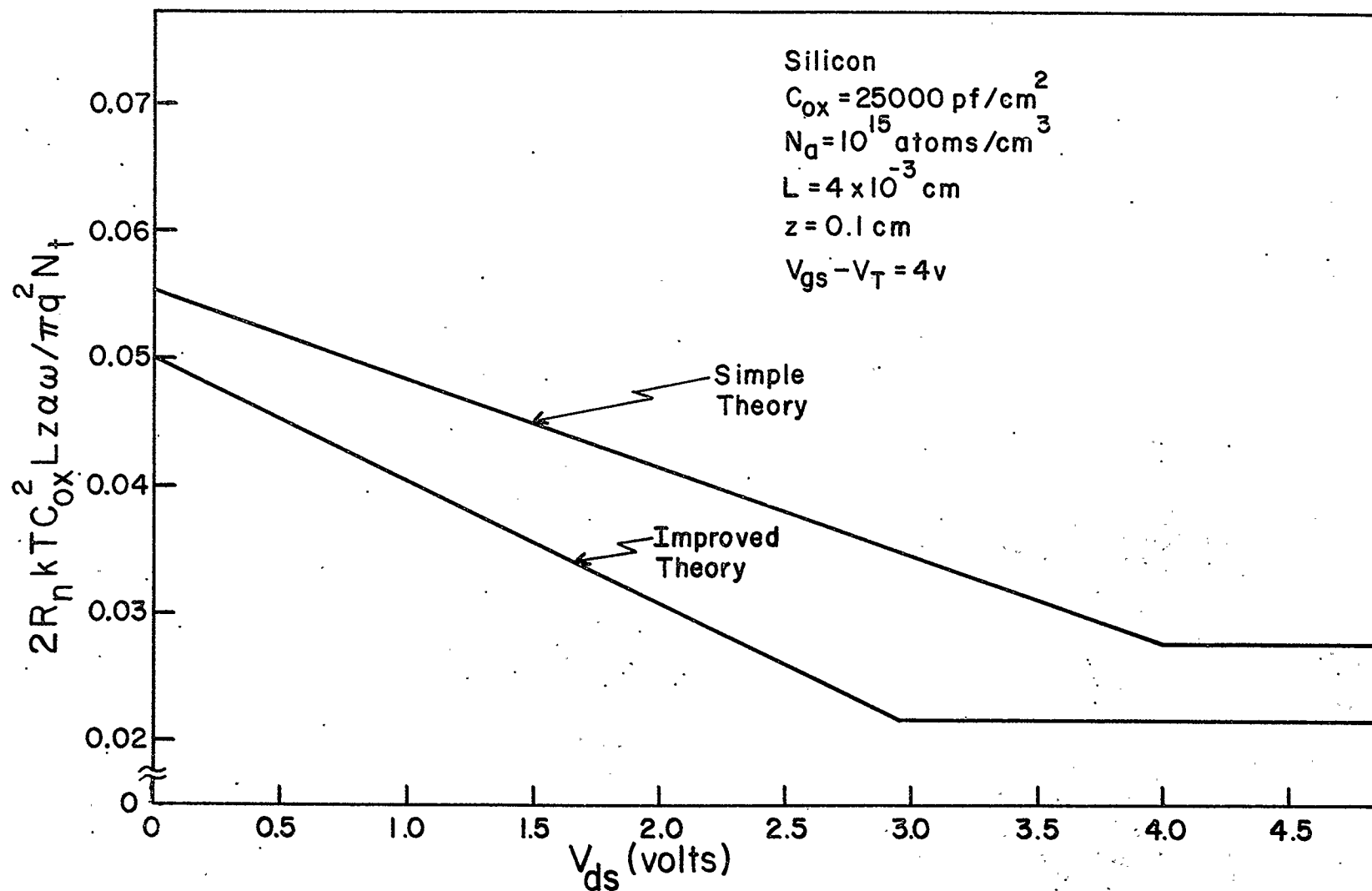


Fig. 5.17 Normalized R_n for traps at A. Comparison of simple and improved theory for a typical device.

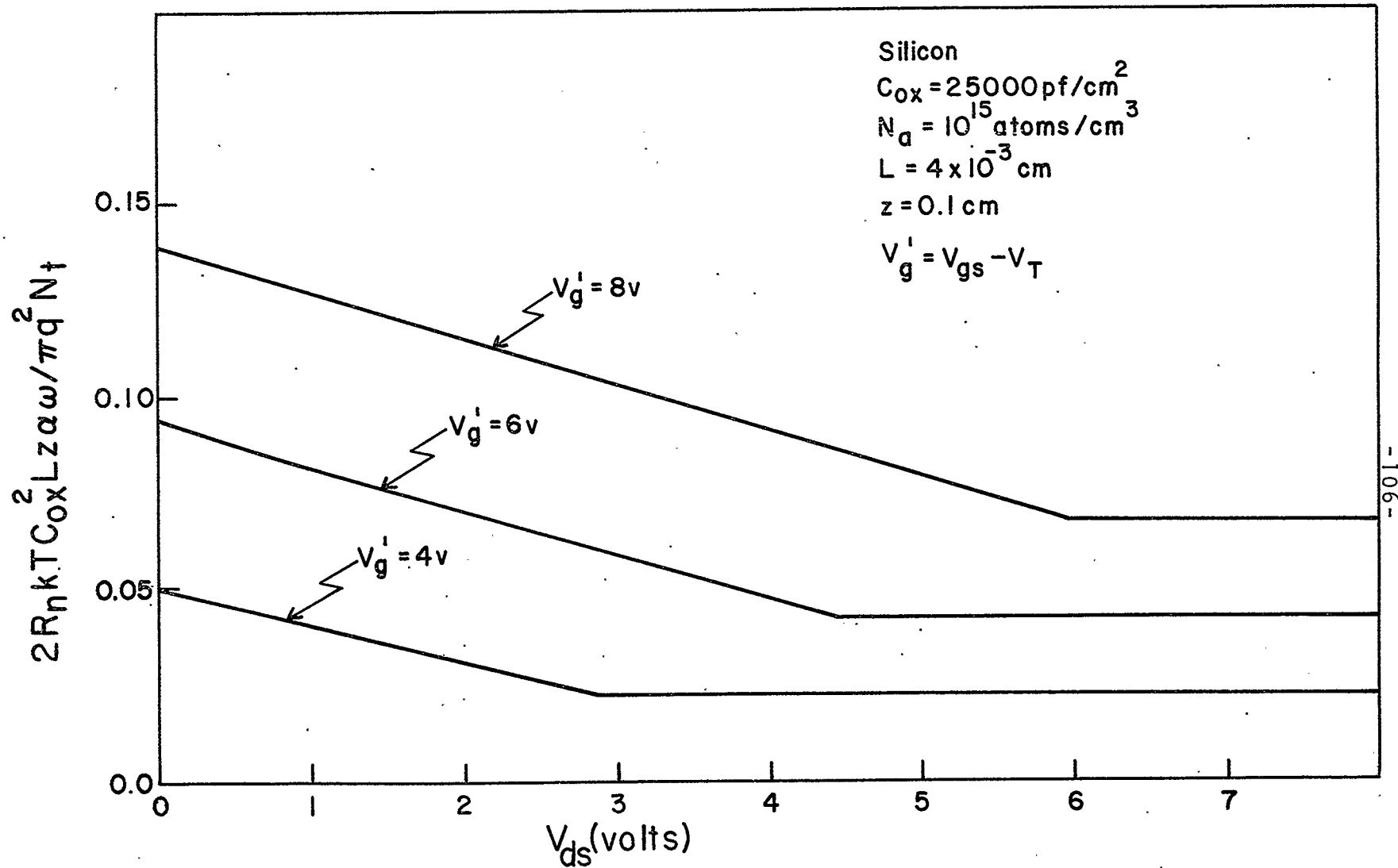


Fig. 5.18 Normalized R_n as a function of bias using the improved theory for traps at A.

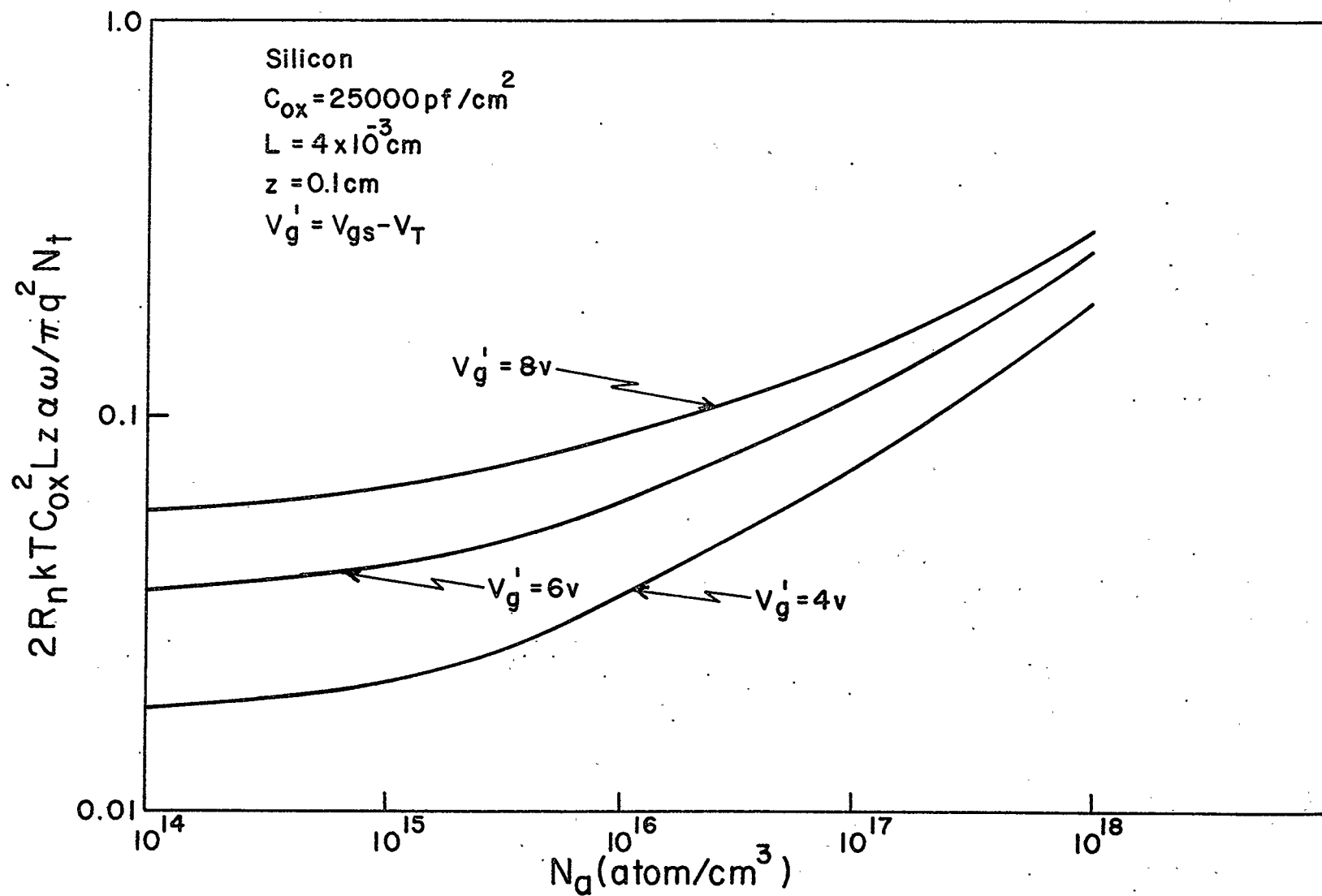


Fig. 5.19 Normalized R_n as a function of doping at pinch-off using the improved theory for traps at A.

However, for normal values of the doping the effect is not pronounced, except at very large drain voltages where other effects may become important.

Case (b). Traps at the electron quasi-Fermi level at the source.

When the trap energy corresponds with the Fermi energy at the source, it can be shown that

$$f_t f_{tp} = \frac{n_s n_{os}}{(n_s + n_{os})^2} . \quad (5.93)$$

The procedure for calculating R_n is similar to that for case (a). Results are presented in Figs. 5.20, 5.21 and 5.22 for a typical device. In this case, the simple theory predicts the noise to be independent of bias, while the improved theory predicts a decrease with increasing gate voltage at saturation, and a decrease with increasing drain voltage below saturation, for constant gate voltage.

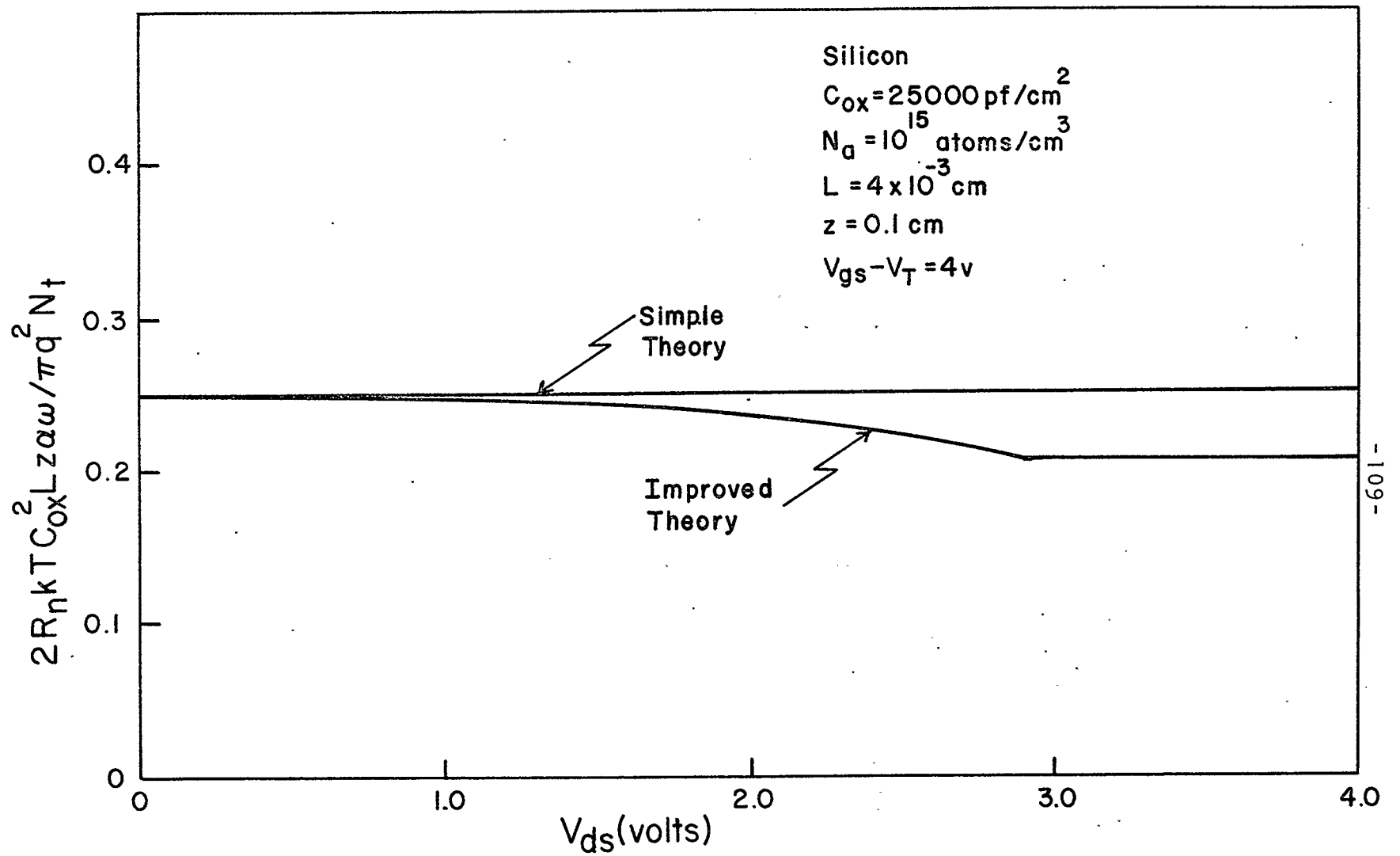


Fig. 5.20 Normalized R_n for traps at B. Comparison of simple and improved theory for a typical device.

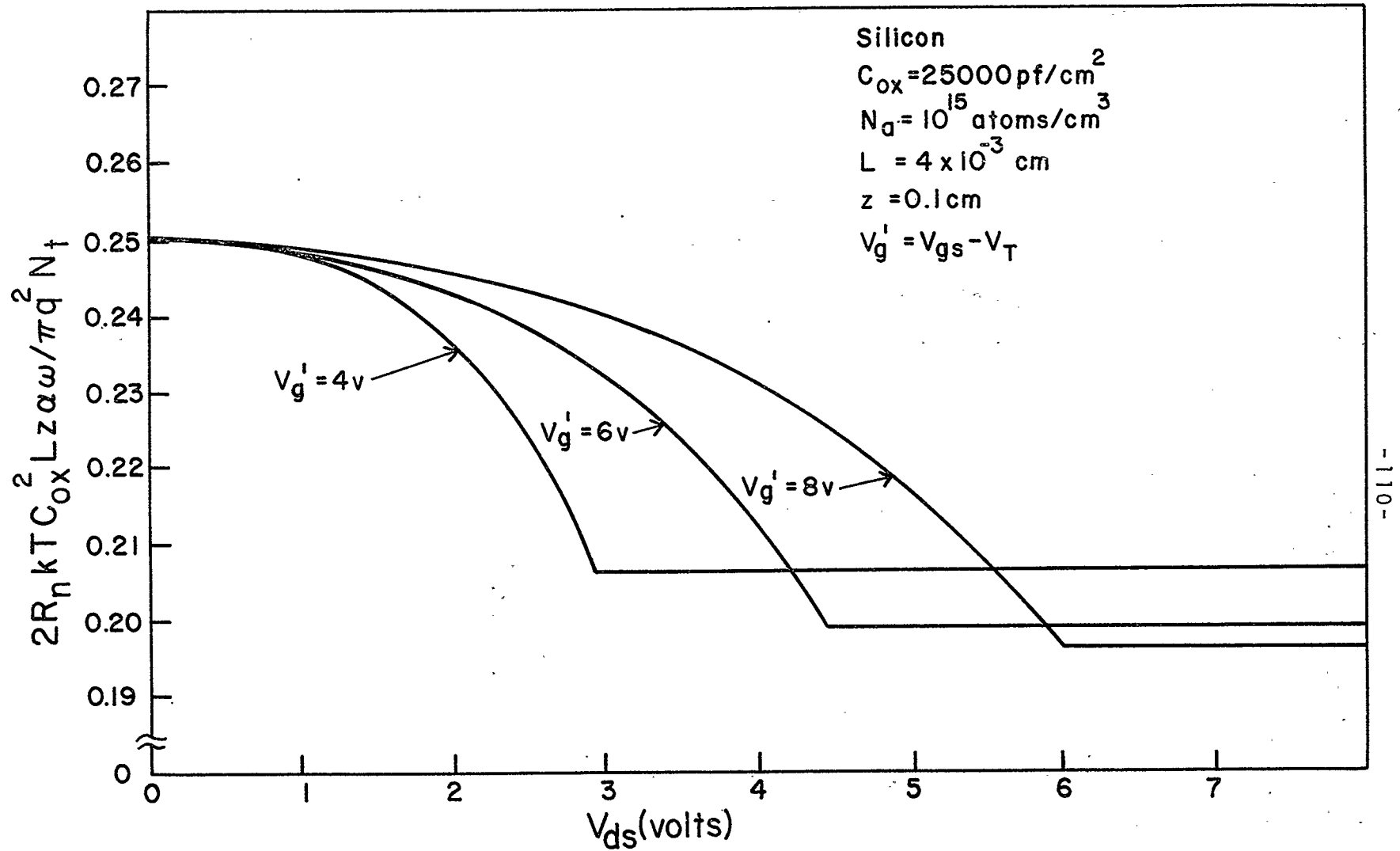


Fig. 5.21 Normalized R_n as a function of bias using the improved theory for traps at B.

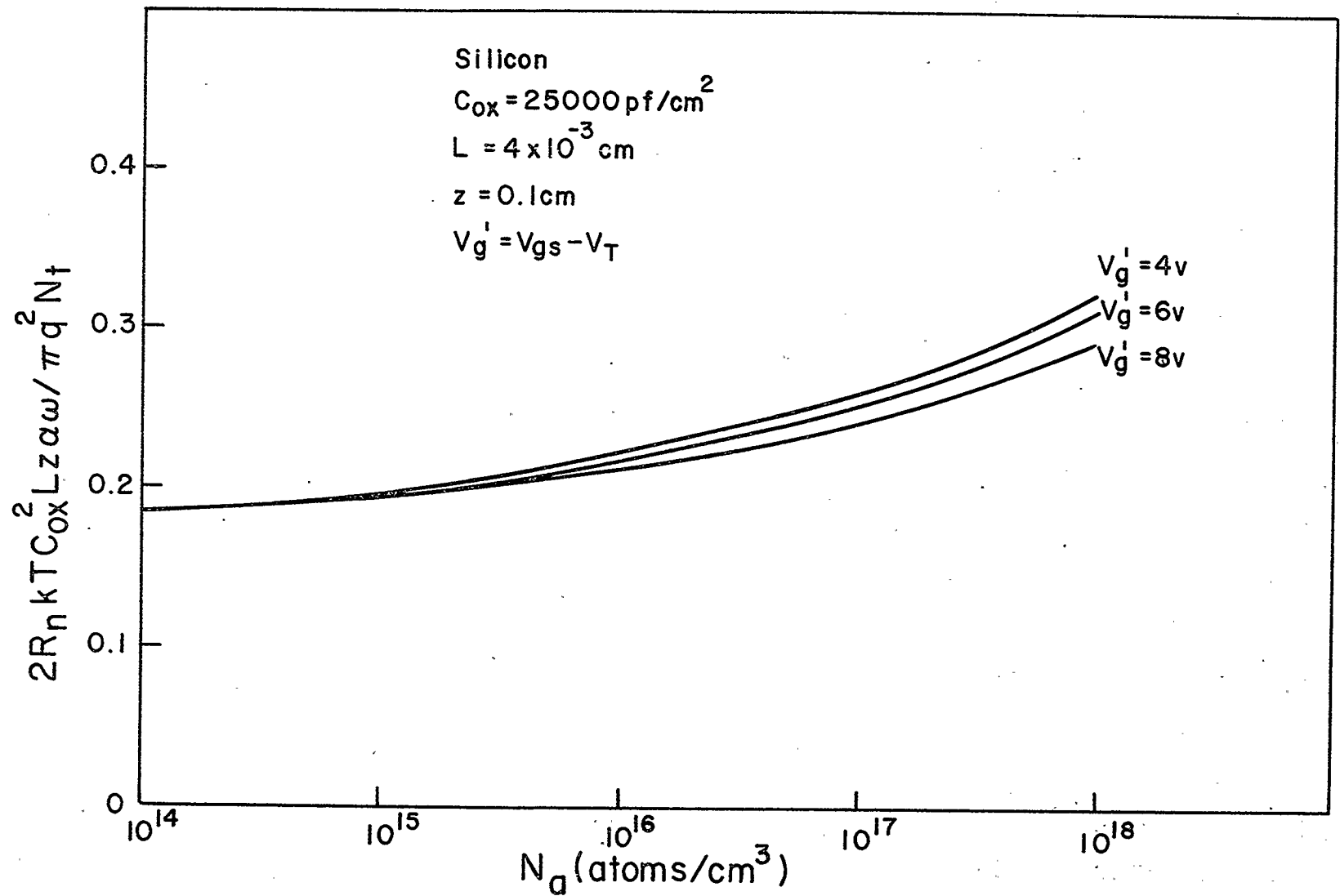


Fig. 5.22 Normalized R_n as a function of doping at pinch-off using the improved theory for traps at B.

Case (c). Traps at midgap at the interface.

For traps located at energy E_i , the $f_t f_{tp}$ product becomes

$$f_t f_{tp} \doteq \frac{n_s n_i}{(n_s + 2n_i)^2} \doteq \frac{n_i}{n_s}. \quad (5.94)$$

The dependence of the noise on doping and bias is illustrated in Figs. 5.23, 5.24 and 5.25. In this case, there is a serious discrepancy between the simple and improved theory. The reason for this is apparent from (5.94). In reality, n_s is always much greater than n_i , while the simple theory predicts that $n_s \ll n_i$ right at the drain. As V_{ds} approaches V_p , equation (5.70) indicates that $F(V_{ds})$ tends rapidly to a value of 0.25, independent of the value of n_{os} , while the improved theory indicates a much smaller increase with drain voltage, and a decrease in the noise at saturation with increasing gate voltage. A closer approximation would be to say that

$$F(V_{ds}) \approx \frac{n_i}{n_s} \quad (5.95)$$

although this still indicates too large an increase in the noise near the drain. It must also be noted that the overall level of the noise is strongly dependent on n_{os} , as for the case of traps at (a).

Case (d). Traps at the electron quasi-Fermi level along the whole channel.

For the simple theory, the term n_i^2/n_s could not be neglected when evaluating the noise for this situation. In

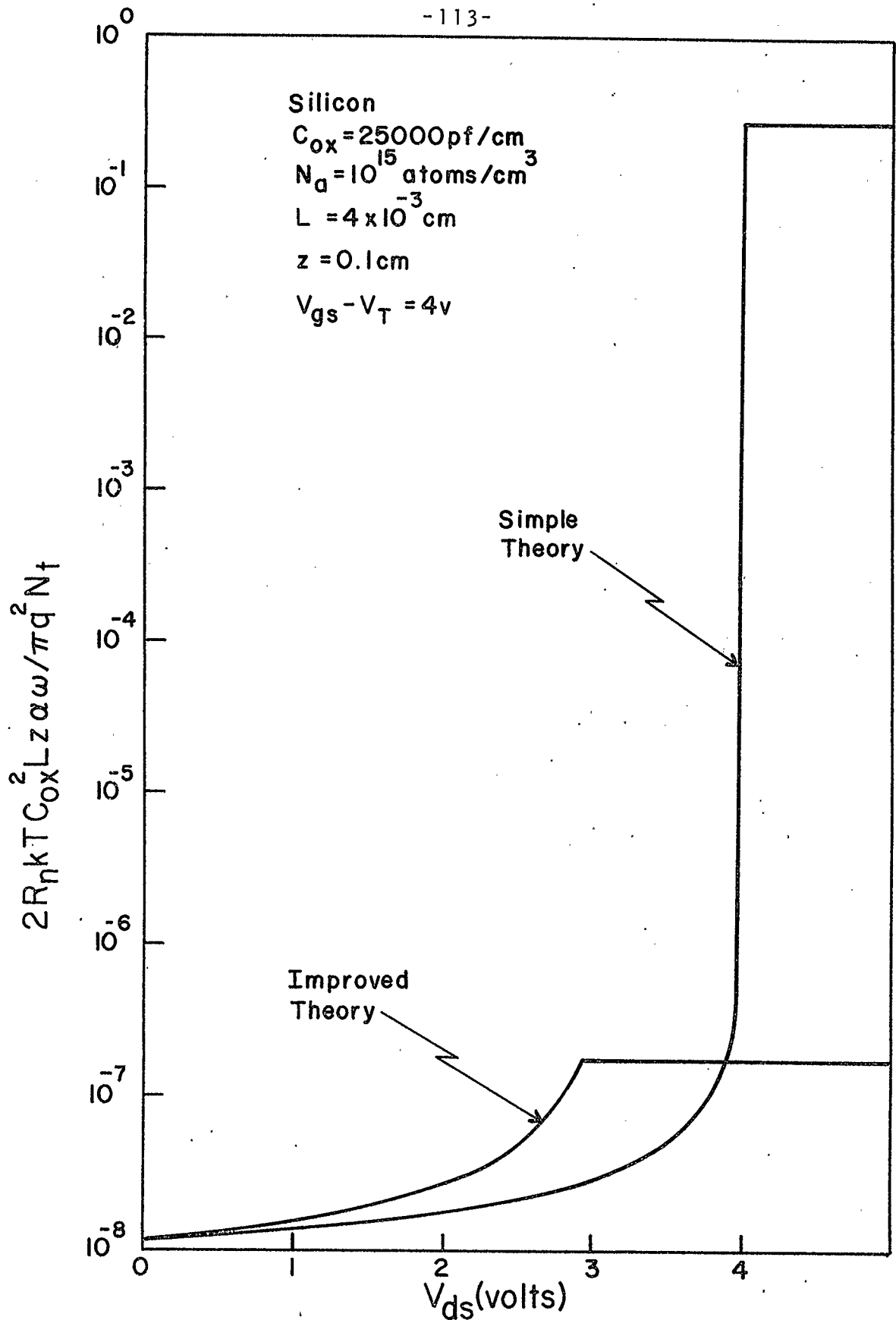


Fig. 5.23 Normalized R_n for traps at C. Comparison of simple and improved theory for a typical device.

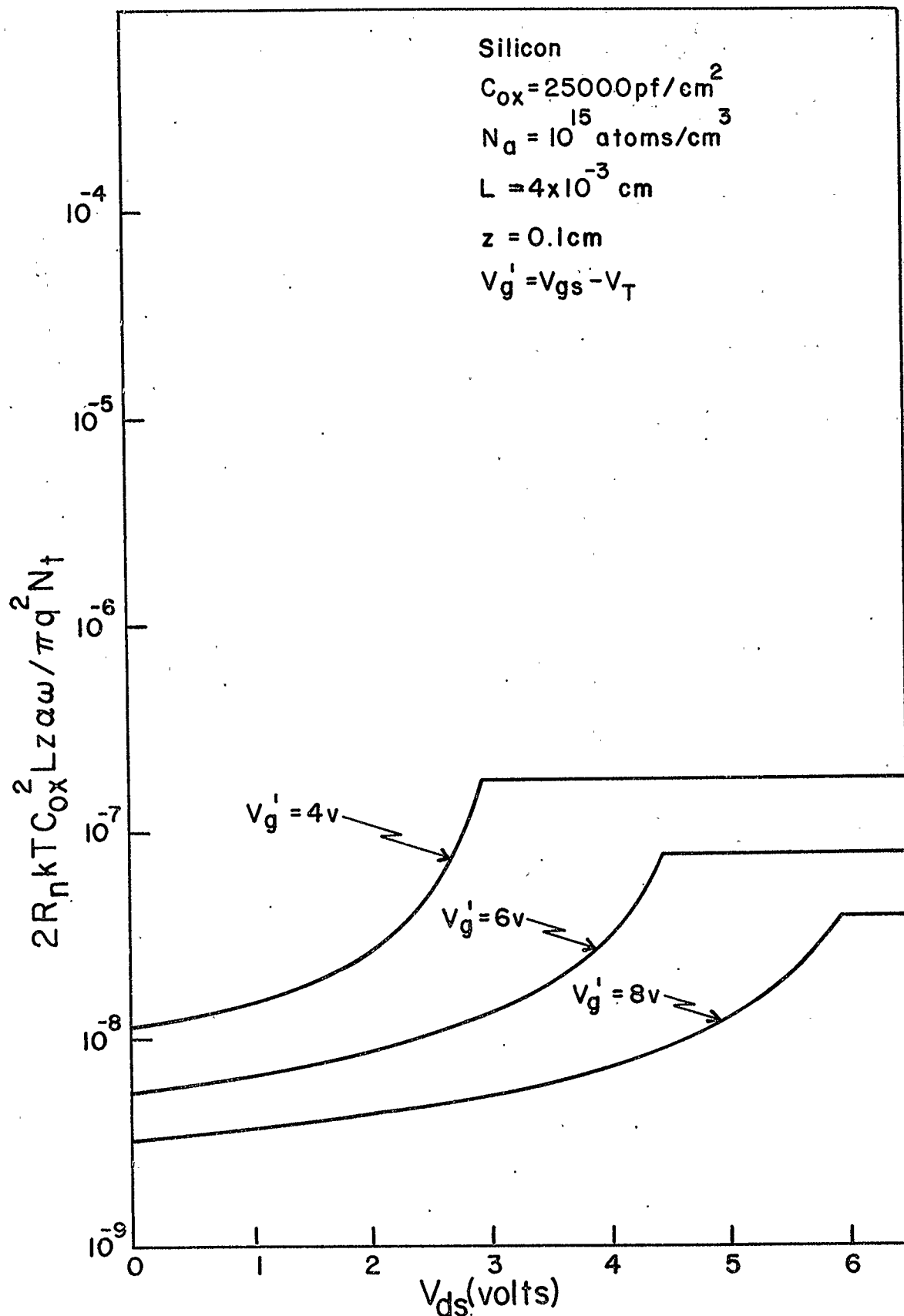


Fig. 5.24 Normalized R_n as a function of bias using the improved theory for traps at C.

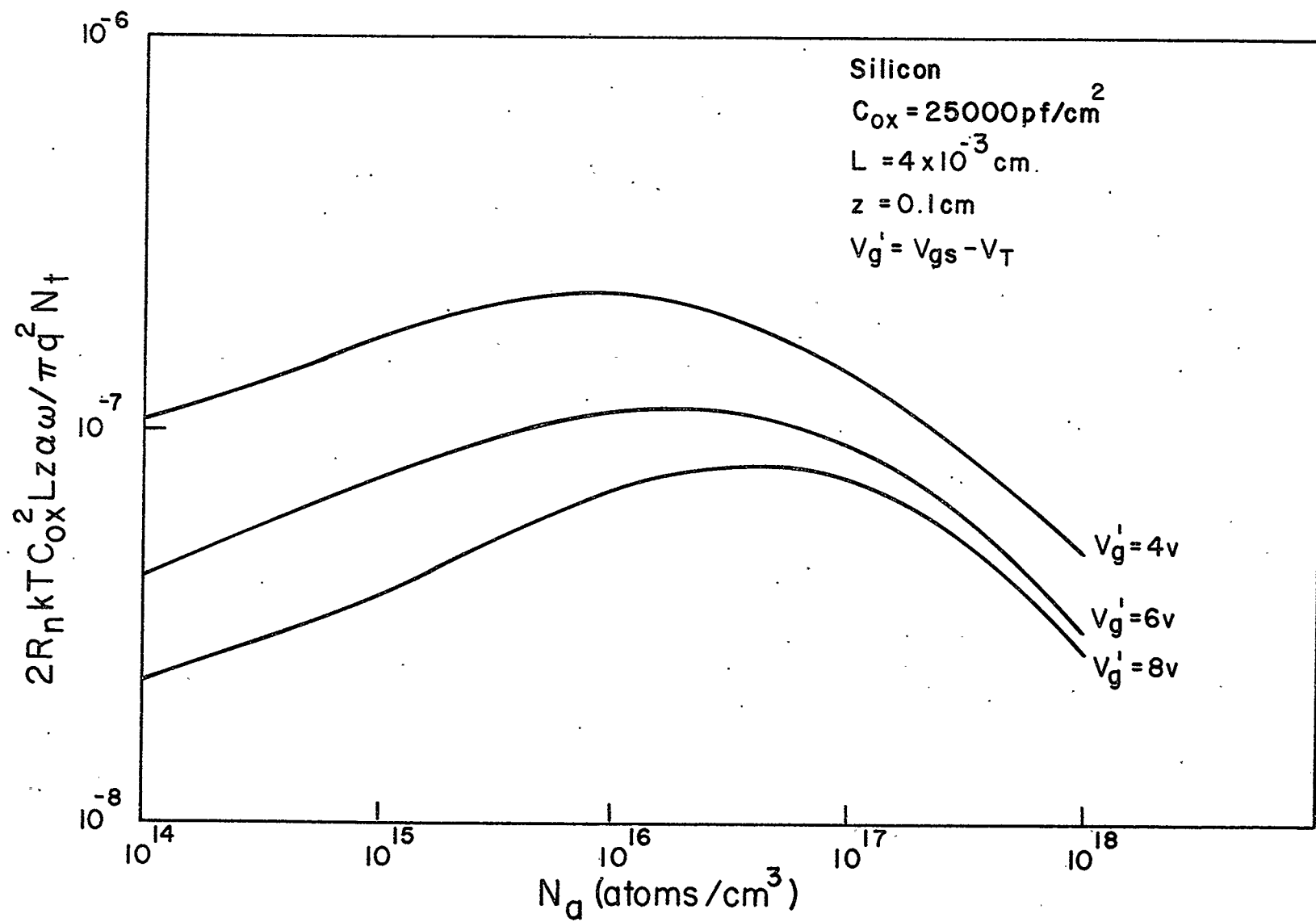


Fig. 5.25 Normalized R_n as a function of doping at pinch-off using the improved theory for traps at C.

reality, the electron concentration at the interface, n_s , is always orders of magnitude above n_i , even at pinch-off, and

$$f_t f_{tp} \approx \frac{1}{4} \quad (5.96)$$

at all points in the channel. The expression for R_n reduces to

$$R_n \approx \frac{-q^2 N_T \pi \theta}{8 \alpha \omega k T L z C_{ox}^2 V_{ds}^2} \int_0^{V_{ds}} \frac{1}{V} dV \quad (5.97)$$

where N_T is the 'effective' volume density of traps in the oxide, as defined in Appendix C.

Results are shown in Figs. 5.26, 5.27 and 5.28 for a typical device. The improved theory again indicates significant differences over the simple theory as indicated in Figs. 5.26 and 5.27. For a constant gate voltage, the increase in noise with drain voltage is not as pronounced as the simple theory predicts. In addition, the simple theory indicates an increasing noise voltage at pinch-off with increasing gate voltage, while the improved theory shows that the noise is almost constant for this condition.

5.5 EFFECT OF NON-UNIFORM TRAP DISTRIBUTIONS ON THE SHAPE OF THE SPECTRUM

In the preceding calculations, the trap distribution was assumed to be uniform over distance into the oxide. In reality, the density of surface states is expected to be large at the interface, decreasing with distance into the

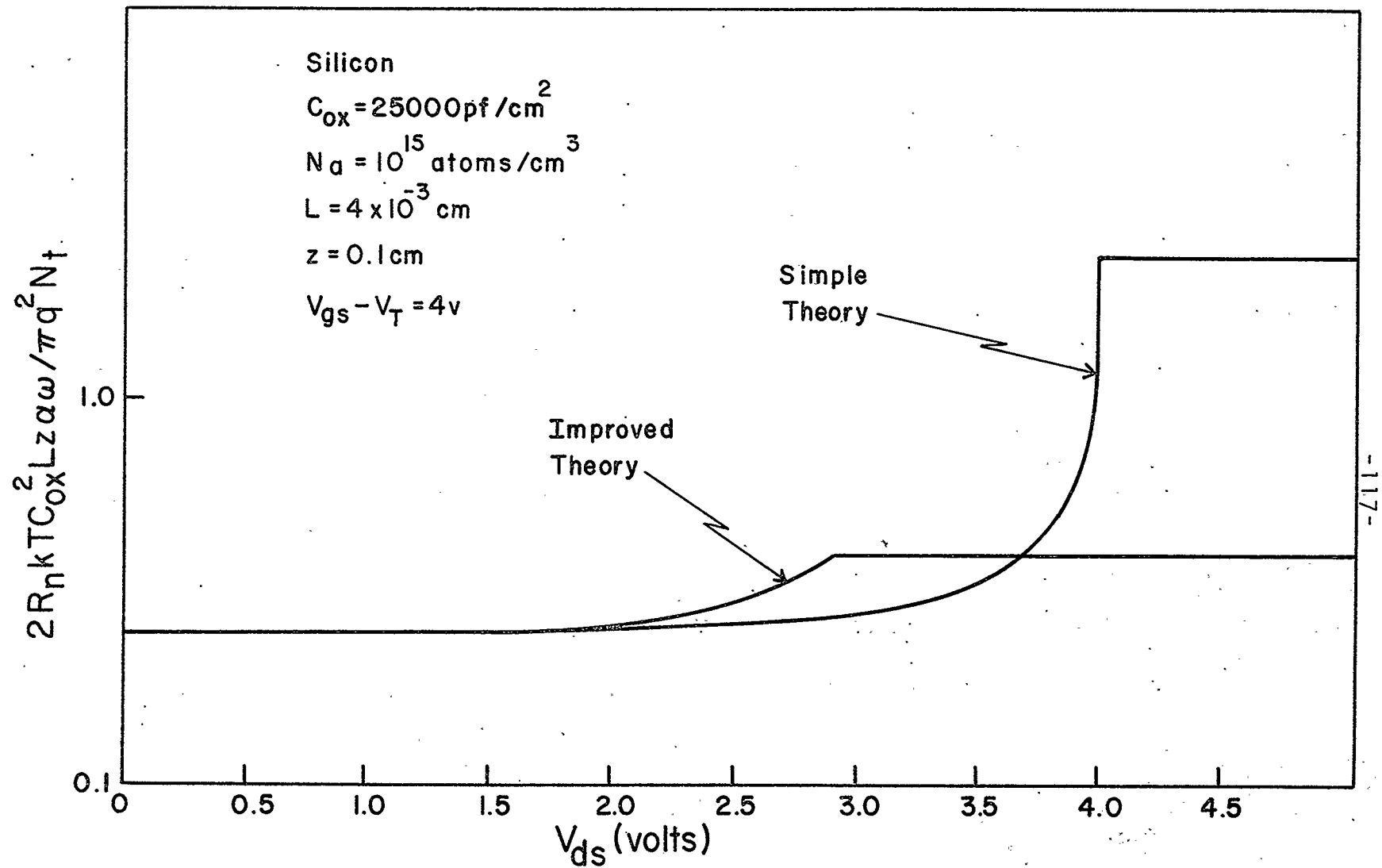


Fig. 5.26 Normalized R_n for traps at D. Comparison of simple and improved theory for a typical device.

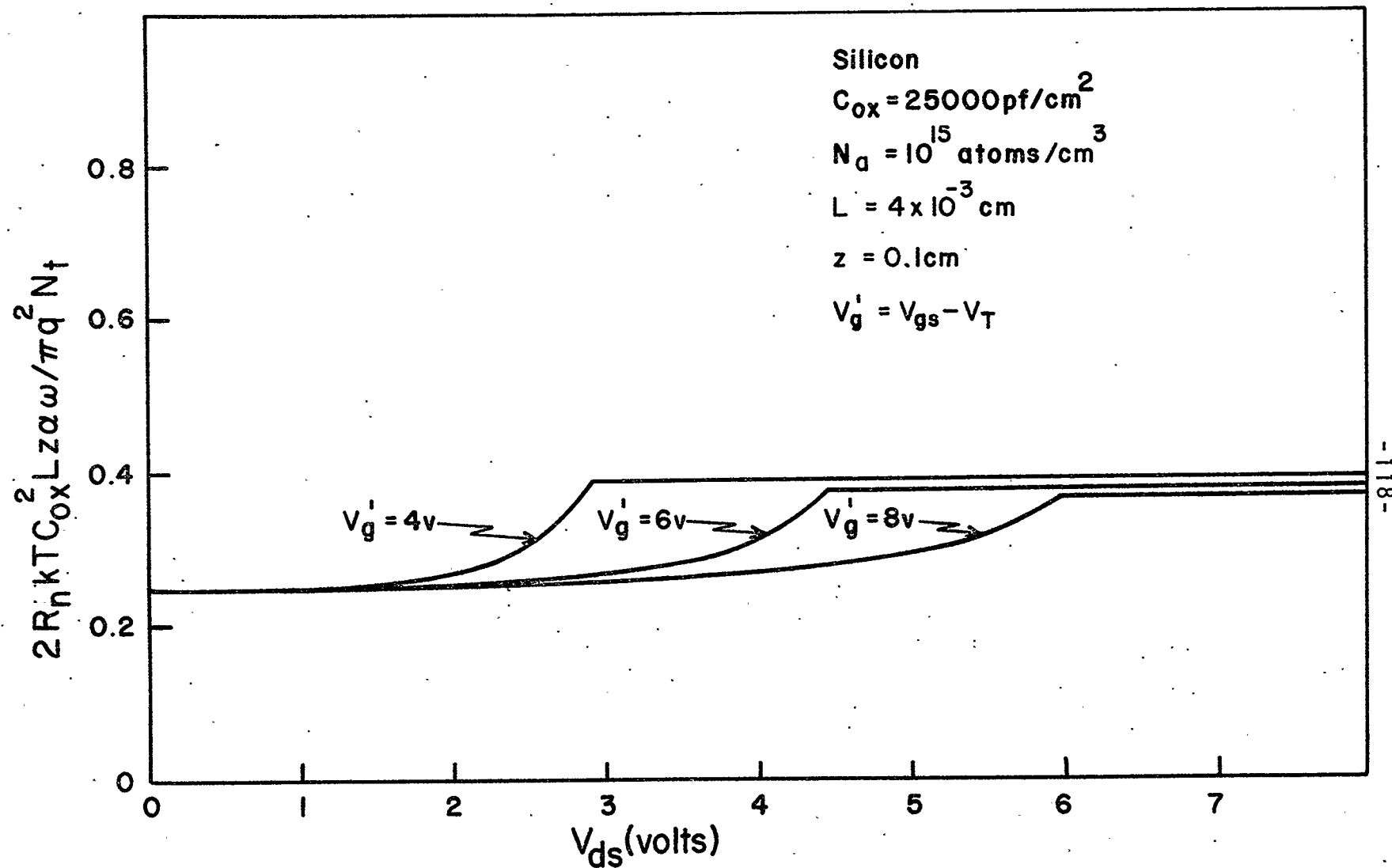


Fig. 5.27 Normalized R_n as a function of bias using the improved theory for traps at D.

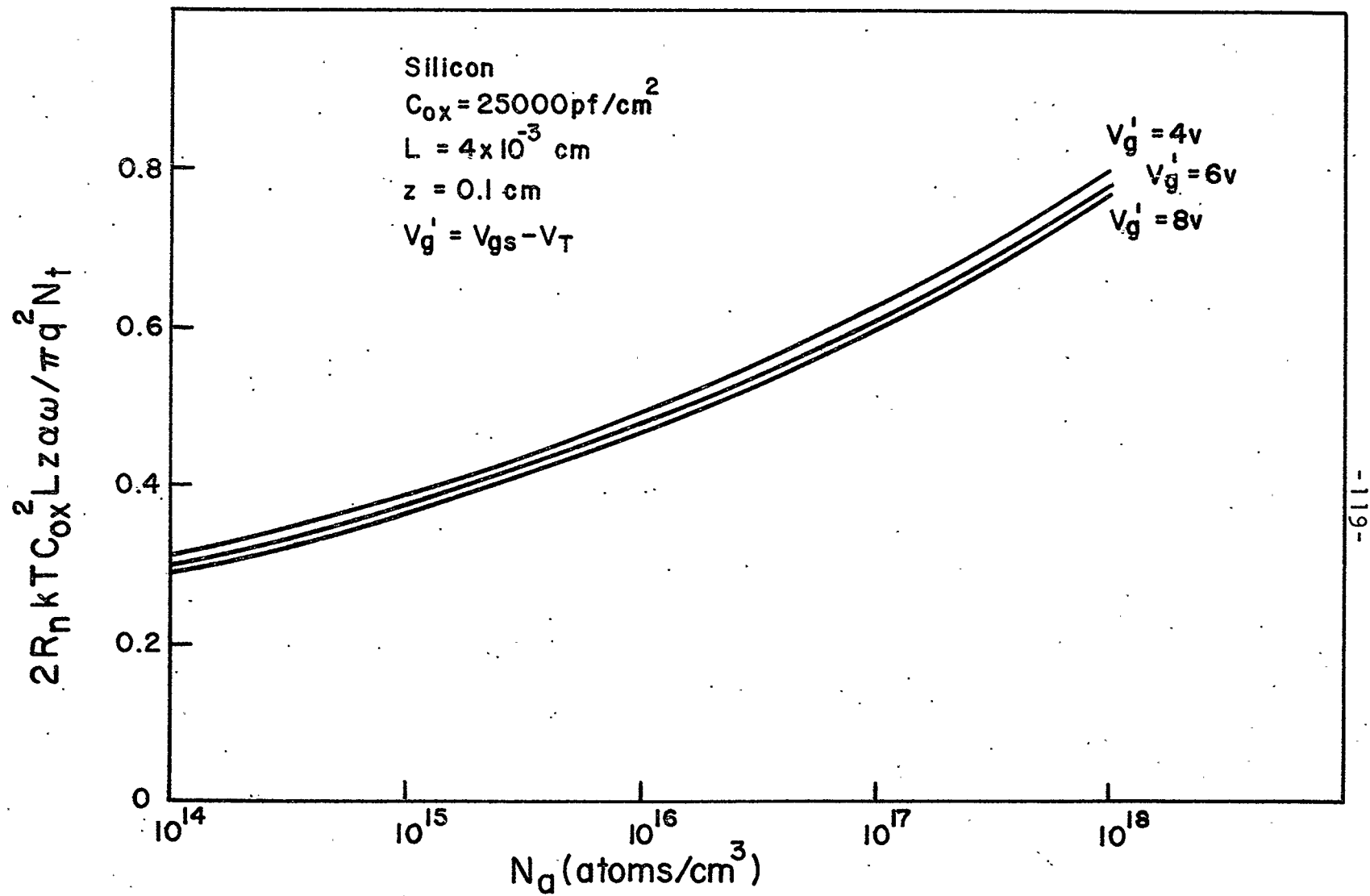


Fig. 5.28 Normalized R_n as a function of doping at pinch-off using the improved theory for traps at D.

oxide.⁴⁹ The effect of an exponentially decreasing density with distance from the interface was investigated by Christensson et al²⁹ for a single bias condition. However, the distribution, chosen for mathematical convenience, was physically unrealistic because the density changed orders of magnitude in less than an atomic distance at the interface. A more reasonable distribution is given by

$$N(y) = N_s - (N_s - N_o) \left(\frac{y}{d}\right)^\eta \quad (5.98)$$

where N_s = trap concentration per unit volume in the oxide at the interface

N_o = trap concentration per unit volume at $y = d$

d = maximum depth in the oxide at which surface state traps are located

η = factor that determines the shape of $N(y)$.

Then at the interface, $y = 0$ and $N(y) = N_s$ while at $y = d$, $N(y) = N_o$ independent of η . The form of the distribution is shown in Fig. 5.29.

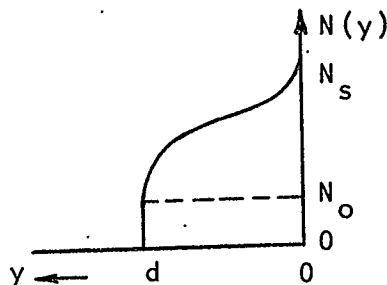


Fig. 5.29 A realistic distribution of traps in the oxide.

Using (5.98), it is possible to examine the effects of the ratio N_s/N_o , the distance d , and the trap time constant on the shape of the spectrum. It can be shown (Appendix C) that the factor which determines the shape of the spectrum is given by

$$\zeta = \int_0^d \frac{[N(y)] \tau_s \exp(\alpha y)}{1 + \omega^2 \tau_s^2 \exp(2\alpha y)} dy \quad (5.99)$$

It is then possible to show that the low-frequency limit of the $1/f$ region is approximately determined by

$$\omega_o = \frac{1}{\tau_s} \exp(-\alpha d) \quad (5.100)$$

where

$$\tau_s = \frac{1}{c_n (n_s + n_l)} \quad (5.101)$$

and α is approximately $2 \times 10^8 \text{ cm}^{-1}$. Thus, ω_o is a function of n_s . If traps are located only to a distance of 10\AA instead of 20\AA , the value of ω_o will be altered by many orders of magnitude, since α is large. Thus, depending on the depth of the traps and the gate voltage, the lower end of the spectrum may flatten at much higher frequencies than first expected. The results obtained by substituting (5.98) into (5.99) are shown in Figs. 5.30, 5.31 and 5.32 for a number of different situations.

The effect of the exponential distribution is to raise the level of the spectrum at higher frequencies. However, for distributions such as those shown in Fig. 5.30 for $n \geq 1/8$, the effect is only to raise the overall level of the

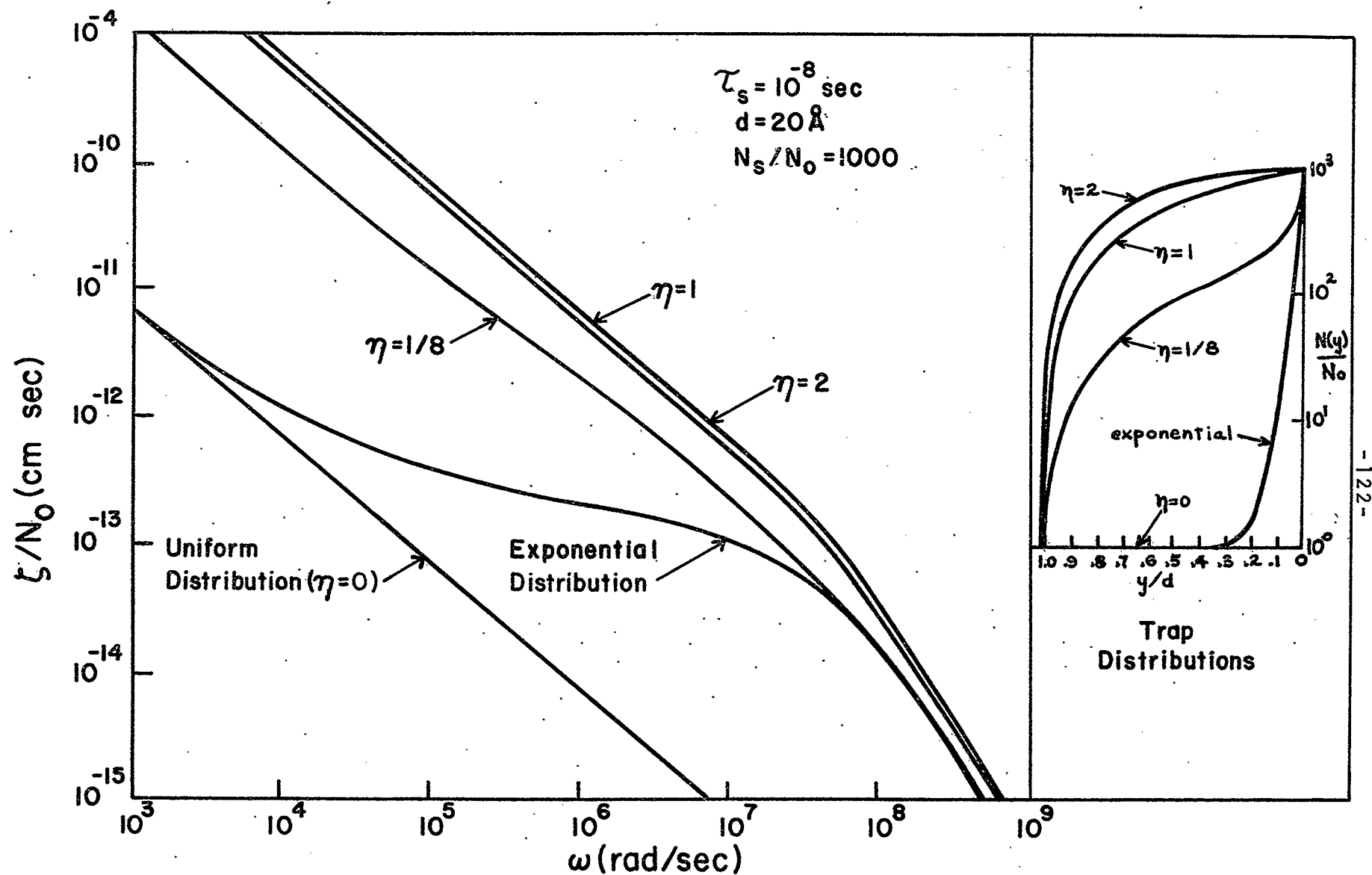


Fig. 5.30 Effects of different trap distributions on the shape of the spectrum at higher frequencies.

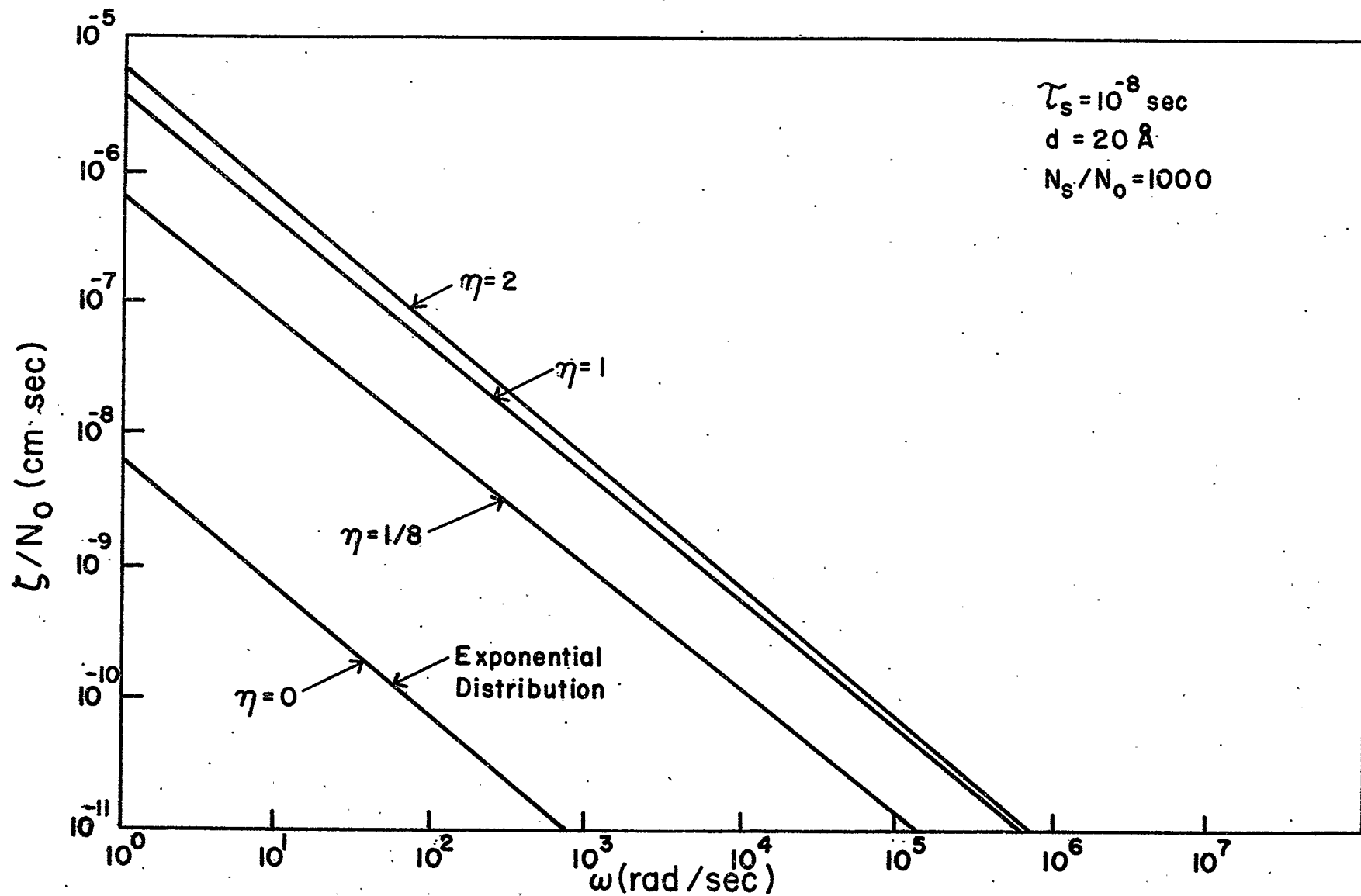


Fig. 5.31 Effects of different trap distributions on the shape of the spectrum at low frequencies.

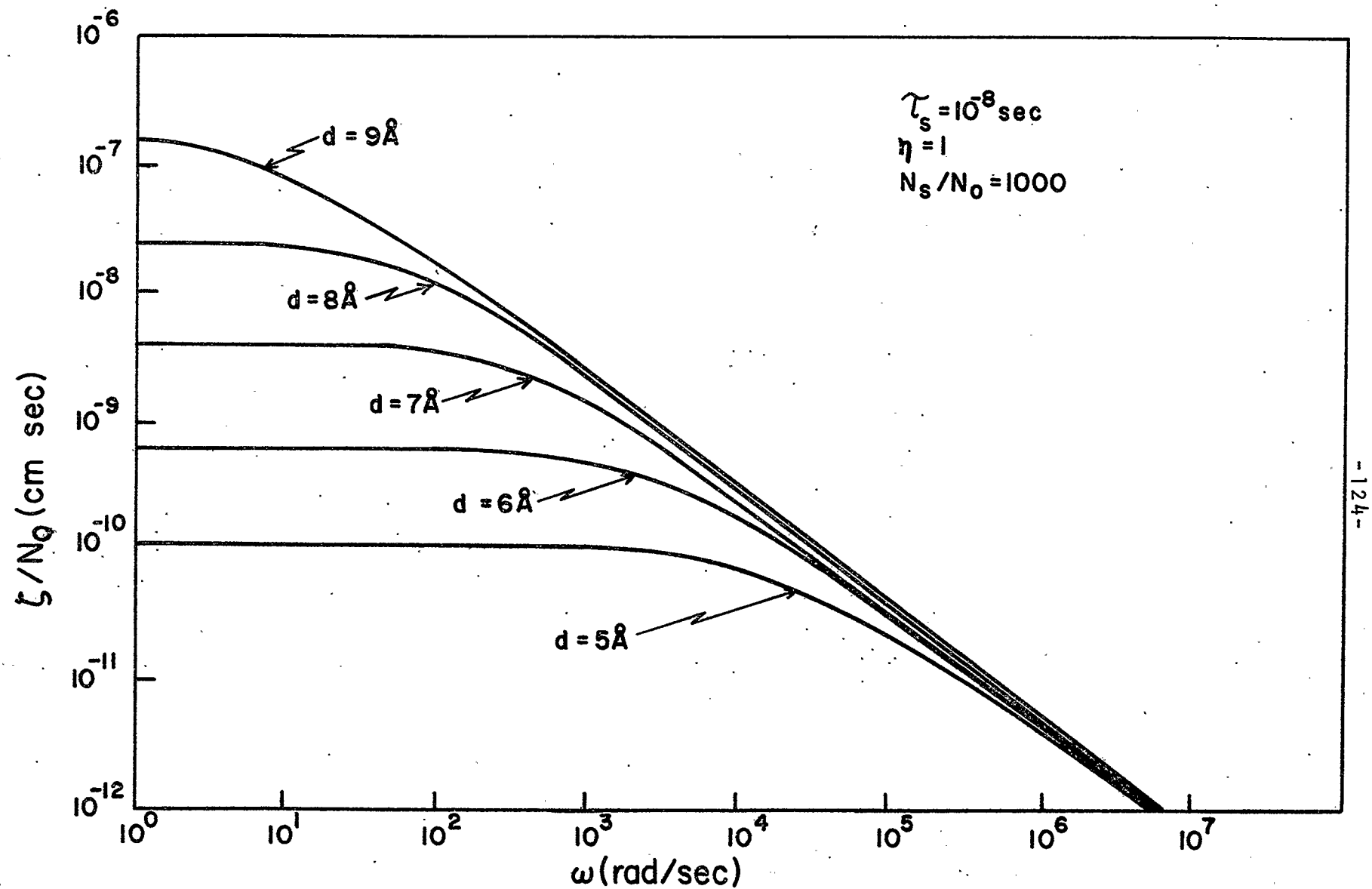


Fig. 5.32 Effect of the trap depth d on the lower corner frequency ω_0 .

spectrum. It is also apparent that as the depth of traps, d , varies the low frequency break point, ω_0 , (Fig. 5.32) varies over a wide range, but is always asymptotic to a level determined by the value of N_0 at moderate frequencies. For traps that are effective at distances greater than 10\AA , it appears that the low-frequency plateau would not be observable using conventional measurement techniques. If it were possible to observe this plateau, it would provide a useful check on the theory, since τ_s decreases and thus ω_0 should increase as the gate voltage increases above threshold.

5.6 SOME COMMENTS ON THE VALIDITY OF THE MODEL

The tunneling model appears to be a very attractive one for explaining surface state noise in MOS FET's, since it gives correct results for reasonable values of the parameters involved. The model has been investigated extensively through the use of germanium filaments⁸⁰ and MOS diodes.^{72,79} (This is discussed in detail by Many et al.⁷⁸) There is some controversy as to the validity of the theory,⁹⁵ and some authors say hysteresis should be observable in the capacitance-voltage characteristics of the MOS capacitance,⁷² if traps with very long time constants exist. The hysteresis that is observed is usually not as large as theory predicts. However, as pointed out by Christensson et al,²⁹ noise measurements are usually carried out at frequencies greater than 10Hz, while hysteresis is sensitive to states corresponding to much lower frequencies. In addition, the results of the preceding

section show that the level of the spectrum seems to be very dependent on the trap distribution in the oxide near the interface, and the low-frequency break point may vary considerably with bias and depth of traps. The break point could occur anywhere below the measurement frequency, and it would be difficult to estimate the hysteresis that should be observed. Apparently, a paper concerning hysteresis measurements will be published in the near future.⁸¹

Finally, as pointed out by van Vliet,⁸⁰ the model is attractive because of its temperature independence. The magnitude of the spectrum is relatively independent of the magnitude of $\tau_s \exp(\alpha d)$ as long as the factor is large. There are, of course, situations where the noise in MOS FET's may be temperature dependent, if traps are located at certain levels in the gap. Since carrier concentration, mobility, etc. are dependent on temperature, a complete analysis would be difficult to make.

At this point, it is important to note that the results of the preceding sections do not need to be associated directly with the tunneling model. The bias dependence of the noise has been calculated using the fact that the integral of the time constant over distance is a constant and may be removed from the integration. It is conceivable that other types of trapping mechanisms could result in the same type of situation. Provided the integral with respect to channel voltage does not involve any additional terms, the analysis will still apply. This may be useful for

evaluating the noise from mechanisms which will no doubt be postulated in the future.

5.7 SUGGESTIONS FOR REDUCING THE NOISE

Since the noise is associated with conditions at the interface in this case, no significant reduction can be obtained by altering the substrate doping as was the case for generation-recombination noise. The usual technique of increasing the gate area applies, but, as before the electrical characteristics of the device deteriorate as the area increases. A decrease in the oxide thickness would increase the oxide capacitance as well, but there are practical limitations to the thickness of oxide that can be used. Much attention in recent years has been focused on growing clean oxides and oxide-semiconductor junctions with low interface state density.⁷⁸ This appears to be the most useful method of improving the noise performance to date.

6. EXPERIMENTAL RESULTS

At this point, in view of the theory derived in the preceding chapters, the value of performing conventional noise measurements on commercially available devices seems questionable. In order to verify the theory for each separate noise mechanism that has been discussed, it would be necessary to manufacture MOS FET's with different impurity concentrations under many different conditions. Fortunately, devices have been fabricated by others in an attempt to determine the effects of different factors on the overall noise performance. Yau and Sah^{31,71} have constructed gold doped devices in order to observe the dependence of the generation-recombination noise on doping, geometry, and operating point. They have also constructed devices with low surface state density in order to examine the thermal noise characteristics at high frequencies.⁶⁰ However, most measurements have been carried out only at a few discrete frequencies in the range of interest.^{28-31,53,55} It is desirable to carry out measurements over a range of frequencies, since the $1/f$ dependence of the noise can exist over many decades of frequency.⁶¹⁻⁶⁷ This has not been done for a wide range of operating points due to the tedious nature of conventional measuring techniques. In order to reduce the tedious nature of the experimental work, as well as to obtain high resolution and accuracy over a wide range of frequencies, a different method of noise measurement has been used in this work. The method

is based on statistical analysis of sampled data, and is described in detail in Appendix D. The technique allows spectral measurements to be made from 2Hz to 10kHz at almost any desired resolution and statistical accuracy, with a minimum of effort. A total of 33 noise spectra have been measured to observe the frequency dependence of the noise under many different bias conditions.

6.1 DESCRIPTION OF THE MOS FET'S UNDER TEST

The theory presented in the previous chapters should apply equally to p- and n-channel enhancement-type FET's. Accordingly, measurements have been carried out on four commercially available enhancement MOS FET's of both channel polarities. Two complementary p- and n-channel devices are tested to eliminate differences in geometry, thus allowing a direct comparison of noise performance using the two types of material.

6.1.1 Determination of the Device Parameters

In order to calculate the noise characteristics of the devices under test, it was necessary to obtain a reasonable estimate of geometric factors and substrate properties. These were determined as follows.

The substrate doping was obtained by performing breakdown measurements on the drain-bulk and source-bulk junctions. The method provides an estimate of N_a since the breakdown voltage is related to impurity density. The results are accurate provided the source and drain are much more

heavily doped than the substrate, and provided the p-n junctions are abrupt.^{68,69} An alternate method, apparently used with considerable success,¹⁷ is to consider the ratio of the transconductance in saturation to the output conductance when $V_{ds} \approx 0$, with gate voltages slightly above threshold so that $V_p < 2\phi_F$. It can be shown¹⁷ that

$$\left[g_{ms}/g_o(V_{ds}=0) \right]_{I_d=0} = \left(1 + \frac{V_B}{4\phi_F} \right), V_p < 2\phi_F \quad (6.1)$$

which gives a value of N_a directly from the ratio $V_B/4\phi_F$. A more accurate value may be obtained from high-frequency C-V data for the MOS capacitance,⁷⁰ but this technique requires a knowledge of the test pads incorporated into the device geometry, and is a difficult measurement to make.

Channel length and width measurements were made by removing the can from the header of each transistor, and photographing the chip with a known magnification. The geometry of the chip was easily obtained with the aid of a compass and scale.

Oxide thickness measurements were made by etching the gate metallization and observing the oxide under a microscope. The color of the oxide is a very good indication of its thickness, and charts are available for comparison with observations. The order of the thickness was obtained by comparing measurements of I_d and g_m with theory. Since the mobility μ_n is not known, this method may not be particularly accurate, but should give a rough idea of the thickness under the gate metallization.

Threshold voltages were obtained from plots of I_d/g_m as a function of gate-source voltage, and were compared with approximate values from static I_d-V_{ds} curves for each transistor.

The parameters obtained for the four transistors are shown in Table 6.1.

6.2 MEASUREMENT OF THE NOISE

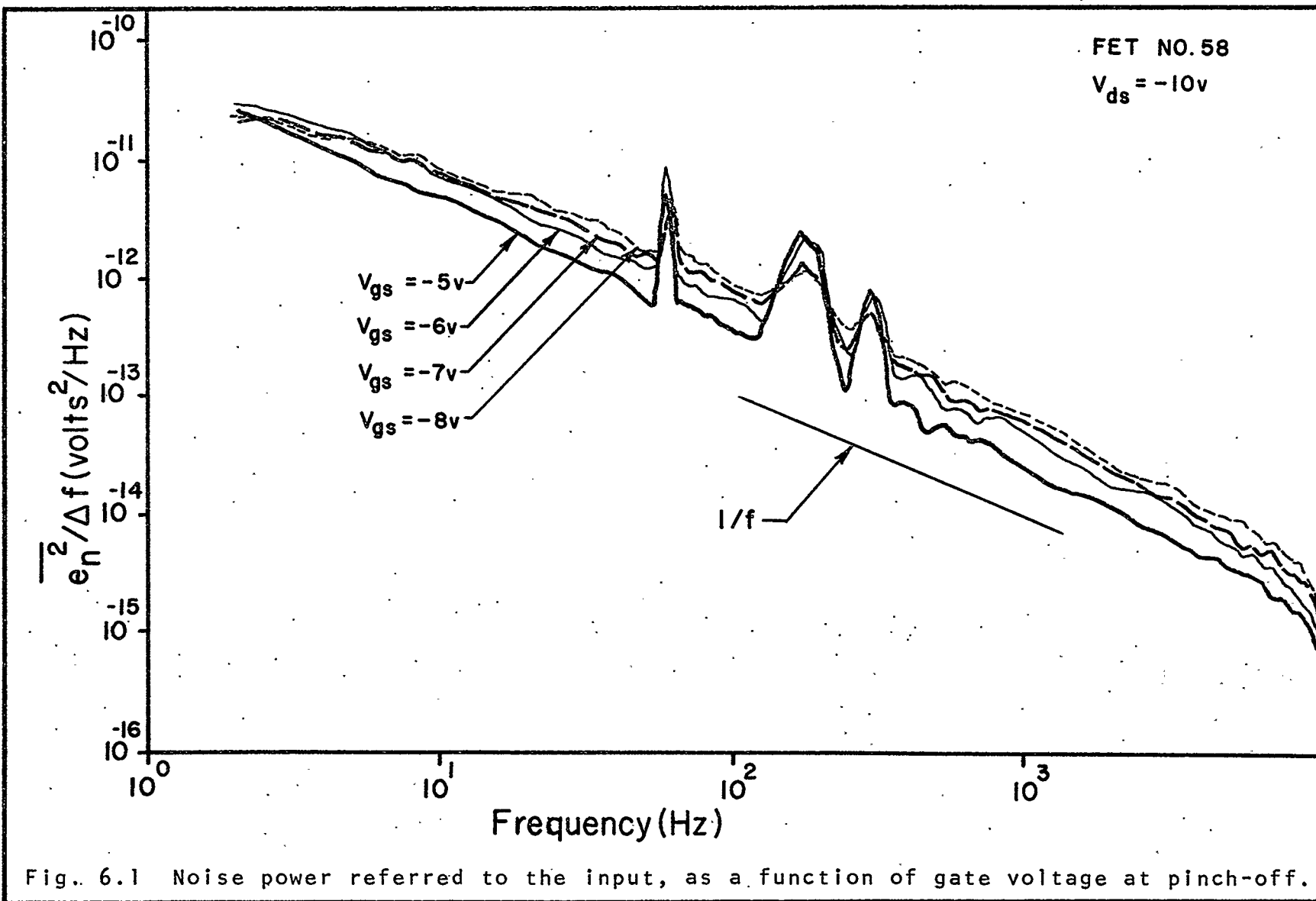
The measurements in this work have been performed keeping in mind that the bias dependence of the noise appears to be the best indication of the mechanisms involved. Accordingly, noise spectra were obtained for a variety of bias conditions. The parameter chosen for measurement was the equivalent noise resistance referred to the input; the reasons for this choice are given in Appendix D.

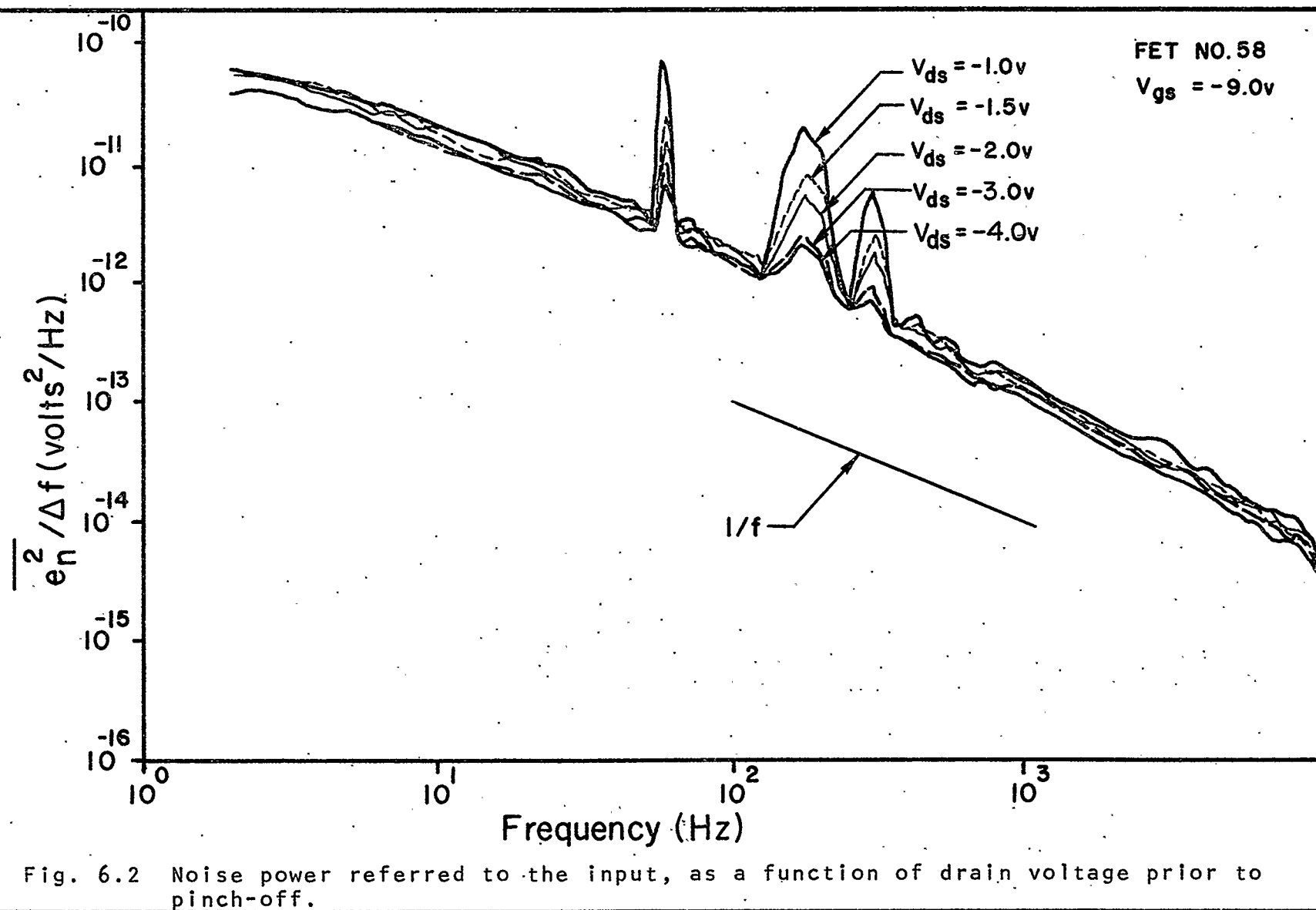
The results for the four FET's described in Table 6.1 are shown in Figs. 6.1 to 6.9. Table 6.2 is included to give an overall view of the quantities being measured. The sharp peaks in the spectra are due to 60Hz and its harmonics. The problem can be avoided by using higher resolution, as described in Appendix D, but processing time is significantly increased. All measurements were made at case temperatures of $25^\circ \pm 2^\circ\text{C}$.

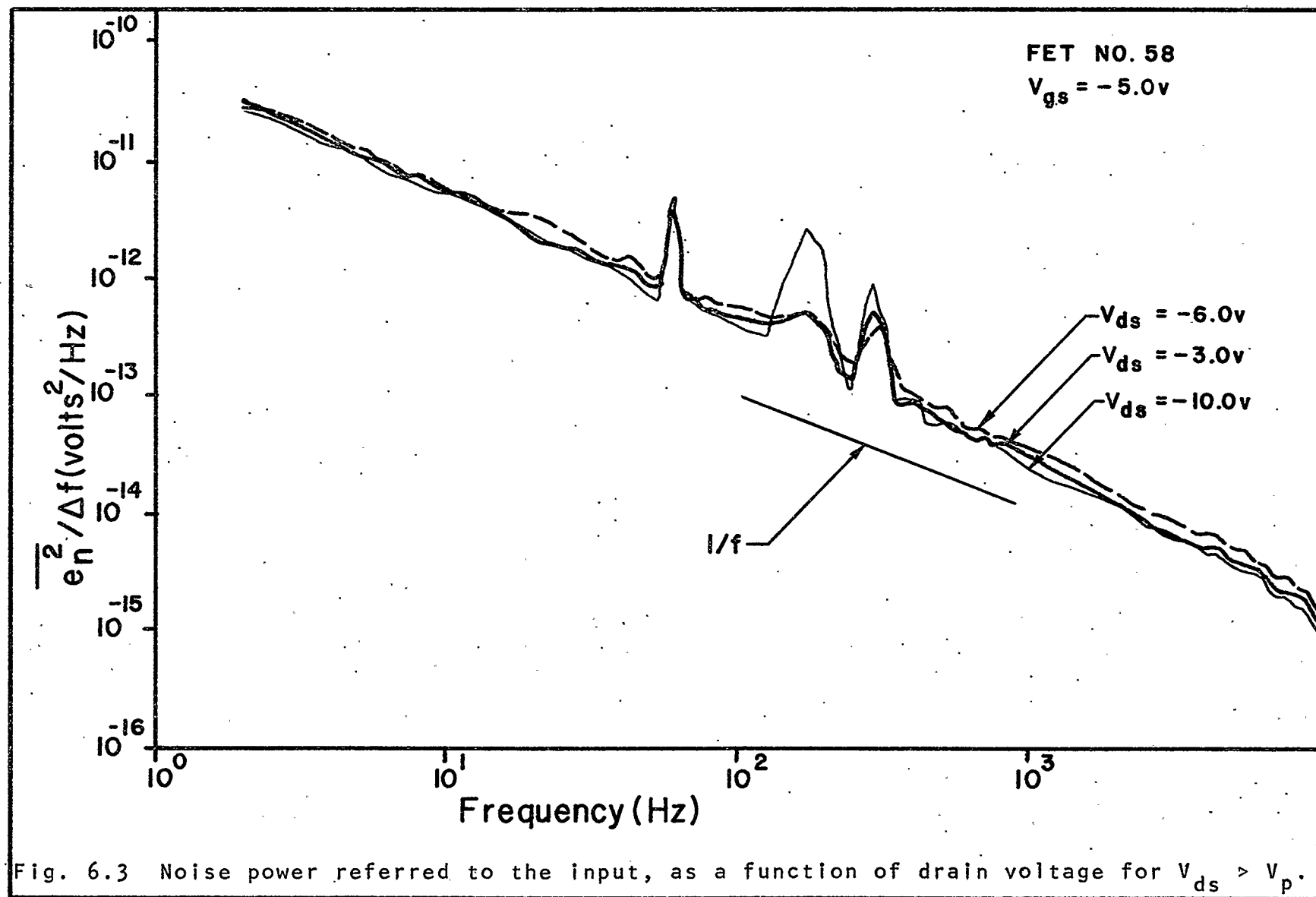
Table 6.1

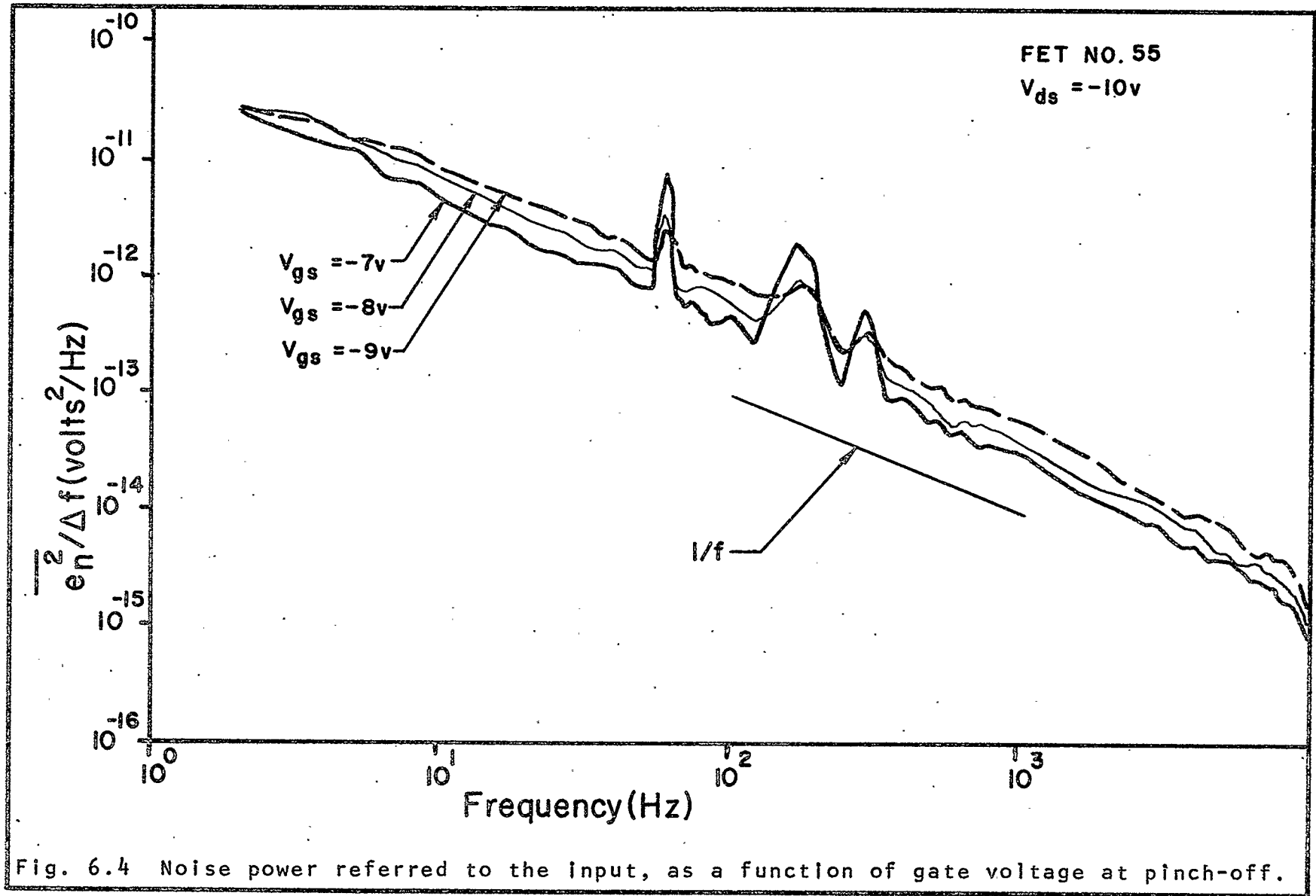
Experimental Device Parameters

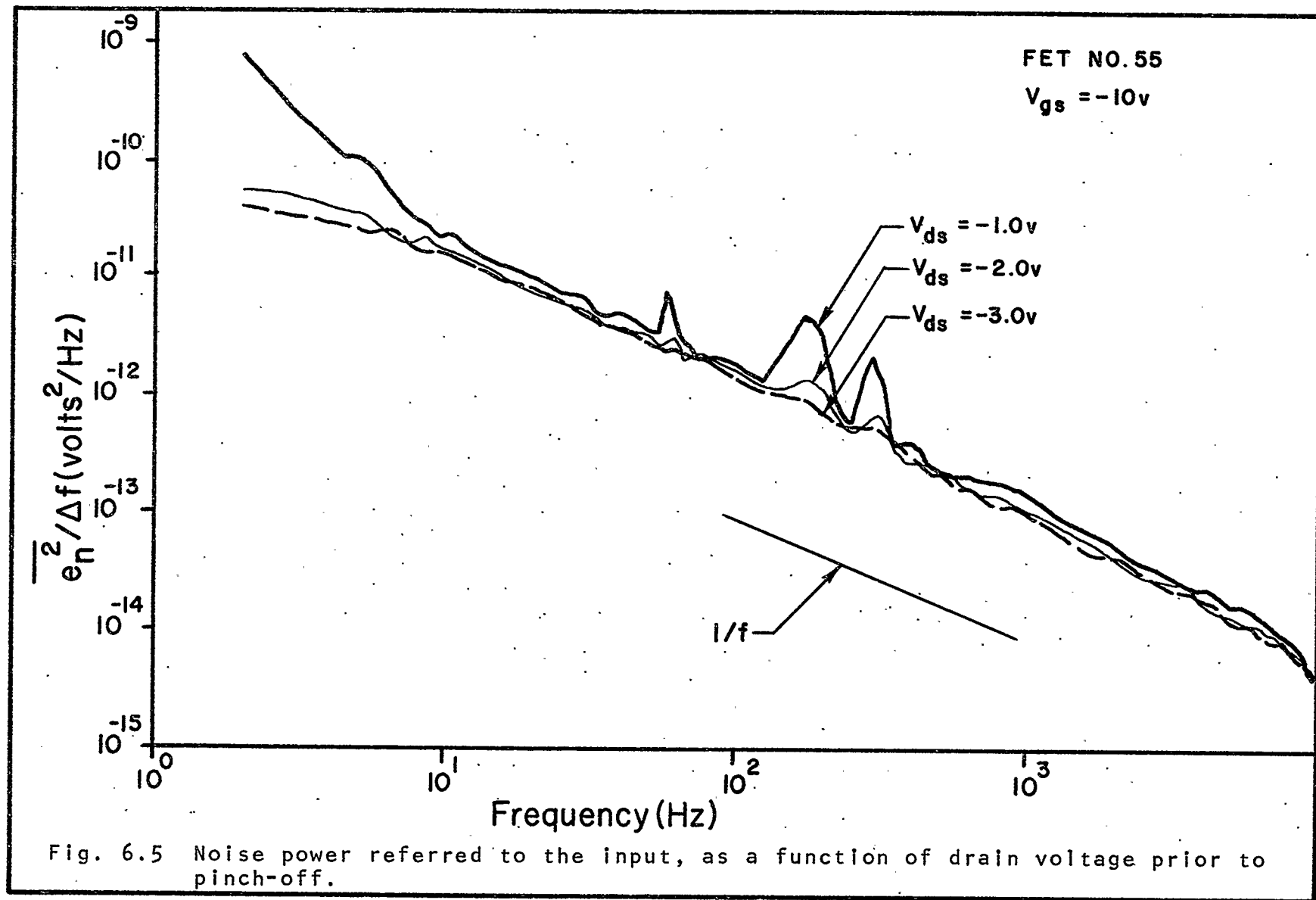
FET Make and Number	Channel Polarity	Substrate Doping (cm^{-3})	Threshold Voltage (volts)	Channel Length (cm)	Channel Width (cm)	Oxide Thickness (Angstroms)
Northern Electric #58	p-channel, zener gate protection	3.5×10^{15}	-4.65	0.0012	0.112	1800
Motorola 2N4351 #61	n-channel, no gate protection	2.5×10^{16}	2.40	0.0014	0.106	1600
Motorola 2N4352 #126	p-channel no gate protection	4.3×10^{15}	-4.05	0.0014	0.106	1700
Siliconix M511 #55	p-channel, zener gate protection	7.0×10^{15}	-5.50	0.0016	0.180	1500

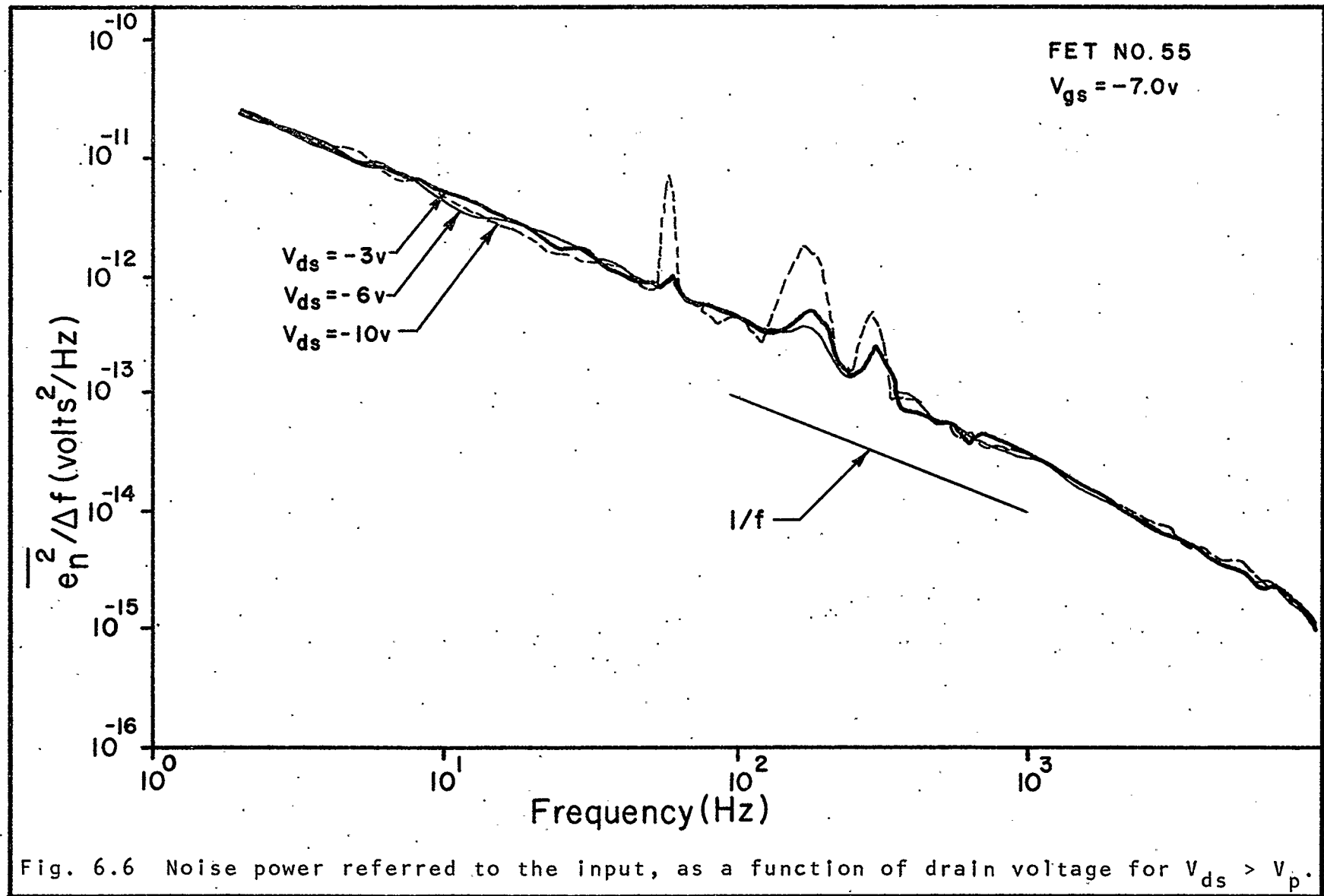


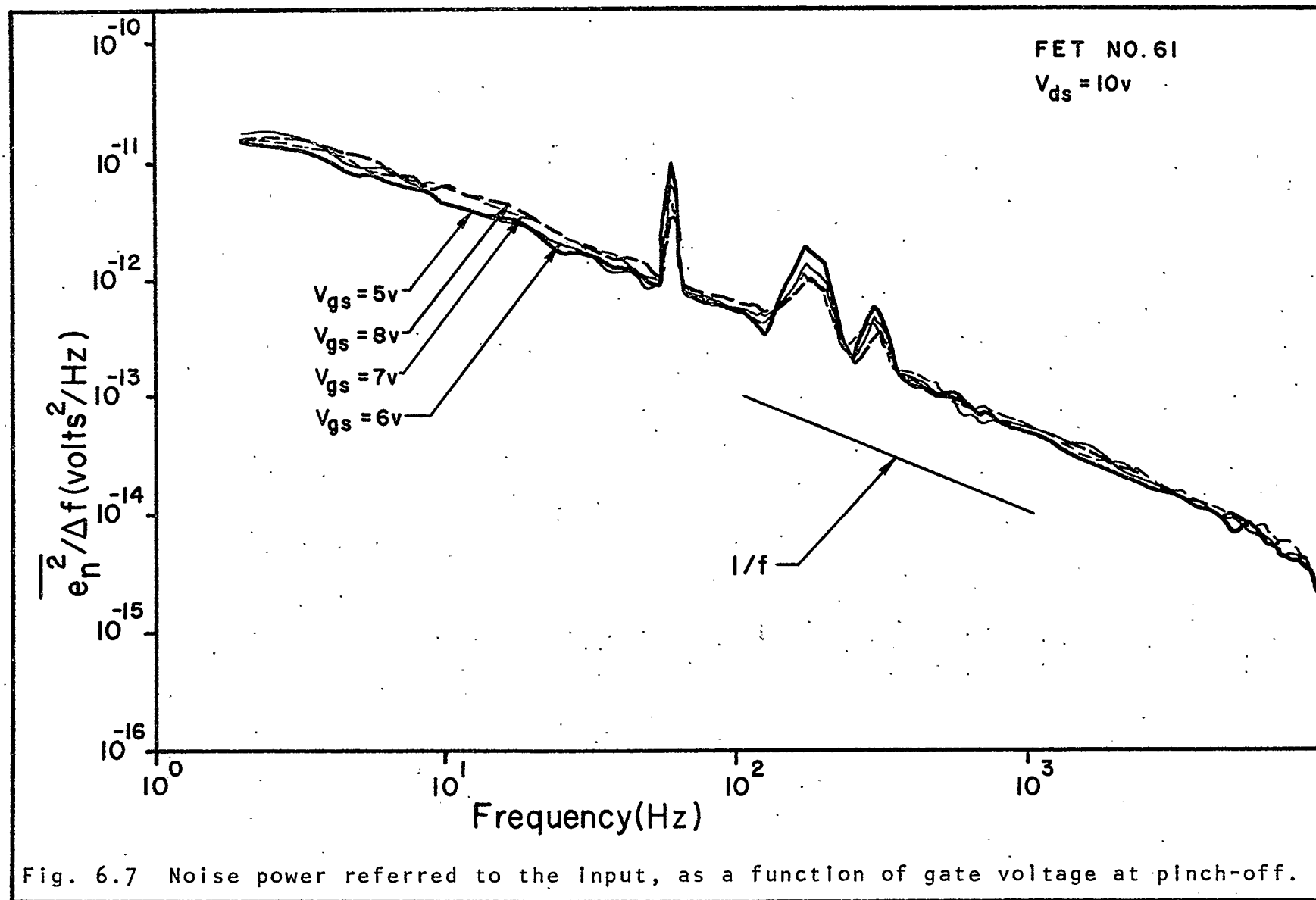


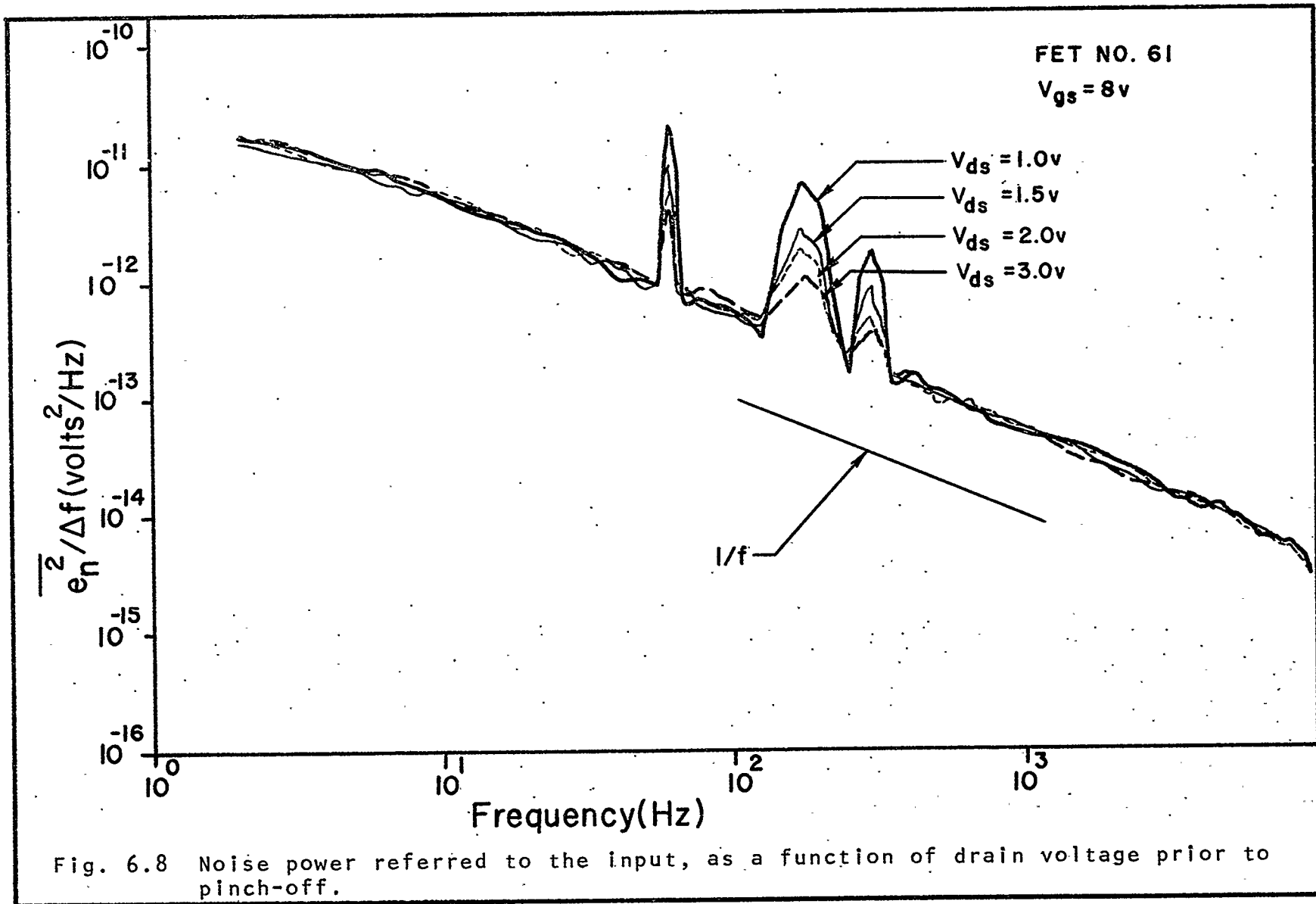












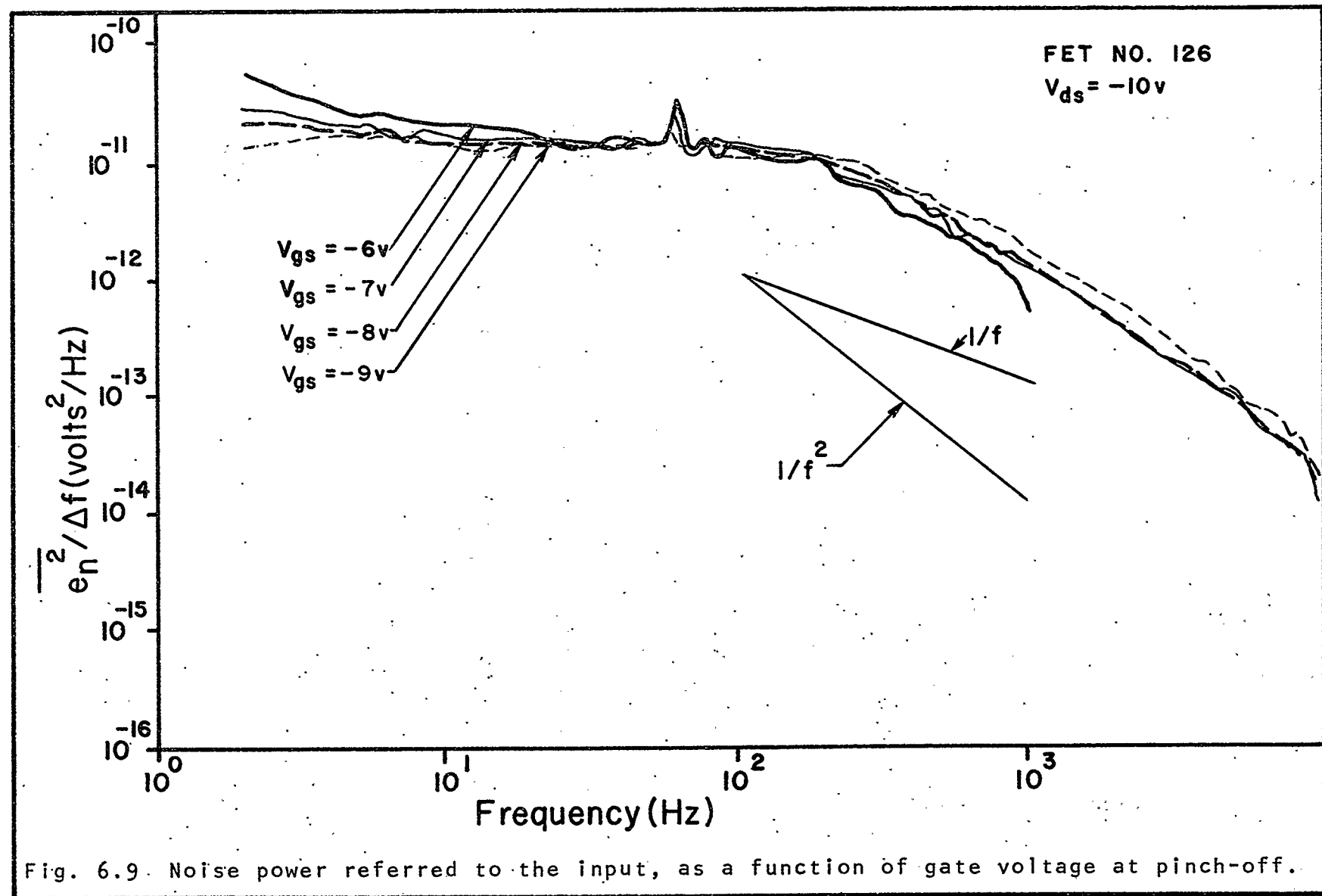


Table 6.2

PARAMETER OF INTEREST	MOS FET NO.	FIGURE NO.
Equivalent mean square noise voltage	58	6.1
referred to the input, as a function	55	6.4
of gate voltage with the drain in	61	6.7
saturation.	126	6.9
Equivalent mean square noise voltage	58	6.2
referred to the input, as a function	55	6.5
of drain voltage below pinch-off for	61	6.8
constant gate voltage.		
Equivalent mean square noise voltage	58	6.3
referred to the input, as a function	55	6.6
of drain voltage past saturation for		
constant gate voltage.		

6.3 ANALYSIS OF RESULTS

The surface state noise calculations indicate that without a detailed knowledge of the distributions of the traps over energy and distance in the MOS FET, it is difficult to predict the noise performance of the device. However, the model for the generation-recombination noise appears to be a good one, so that the variations of noise from this source with bias can be readily calculated using the experimental parameters in Table 6.1. The results, shown in Figs. 6.10 to 6.13, indicate that in all cases the noise increases by a

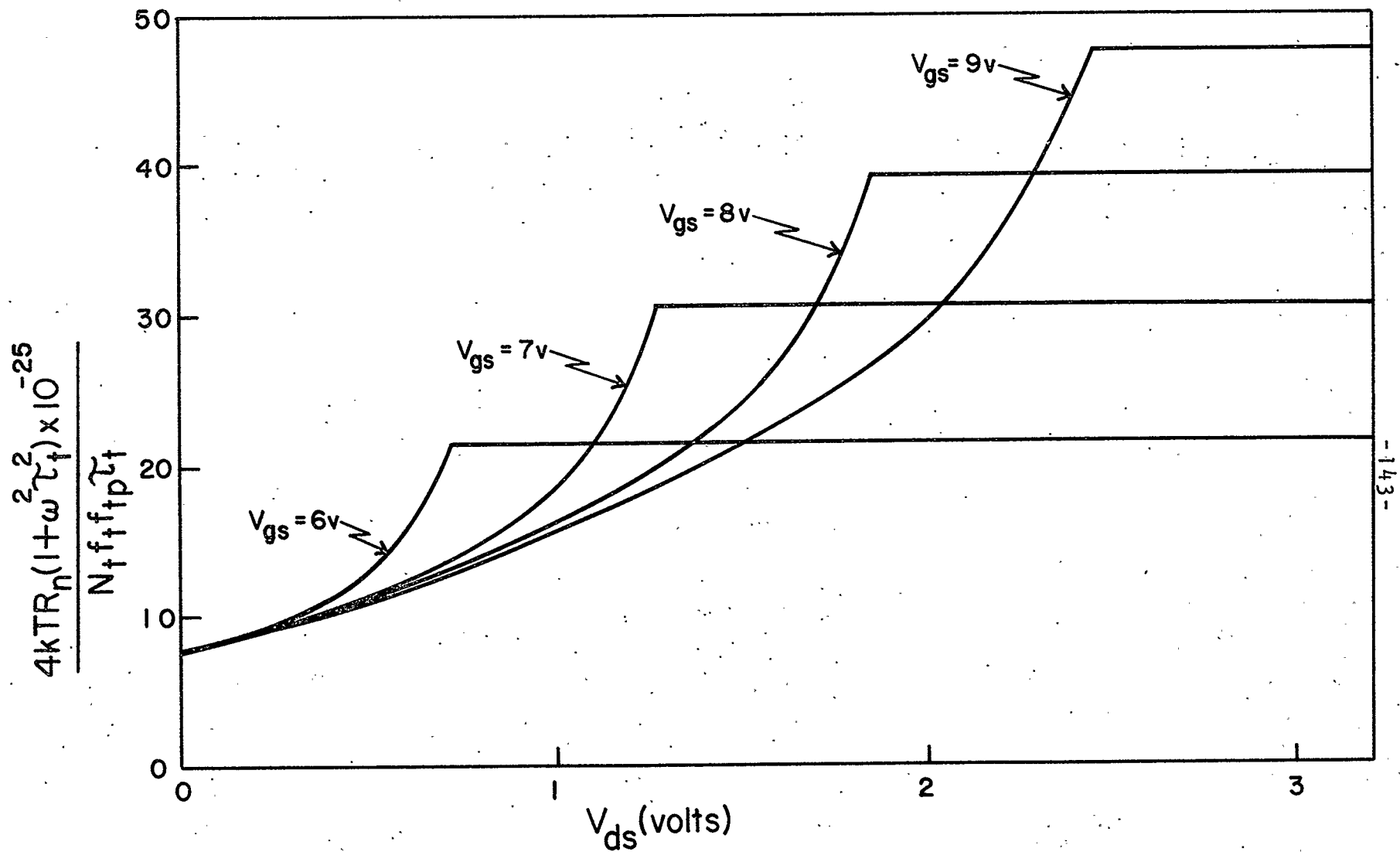


Fig. 6.10 Theoretical generation noise as a function of bias for FET #58.

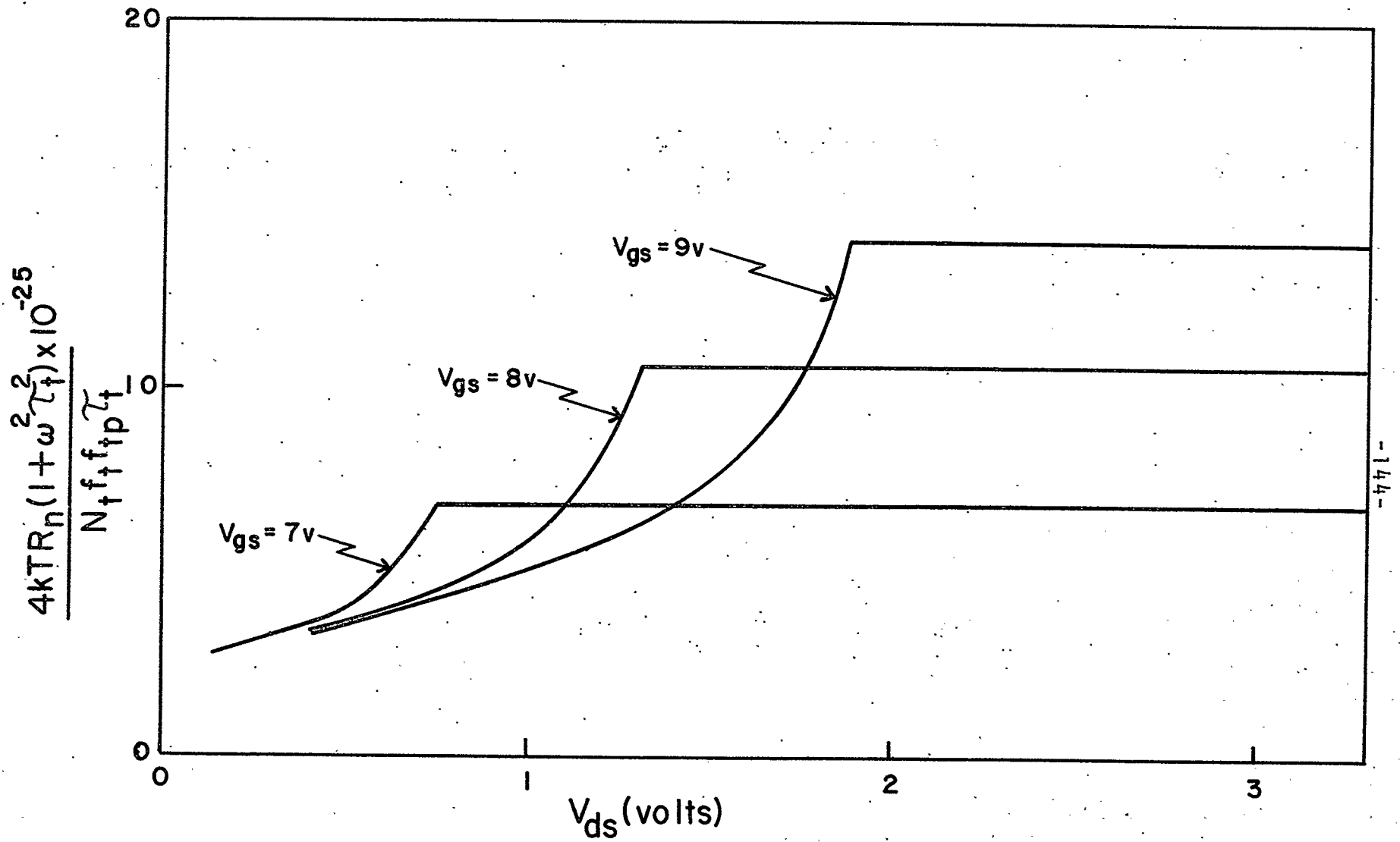


Fig. 6.11 Theoretical generation noise as a function of bias for FET #55.

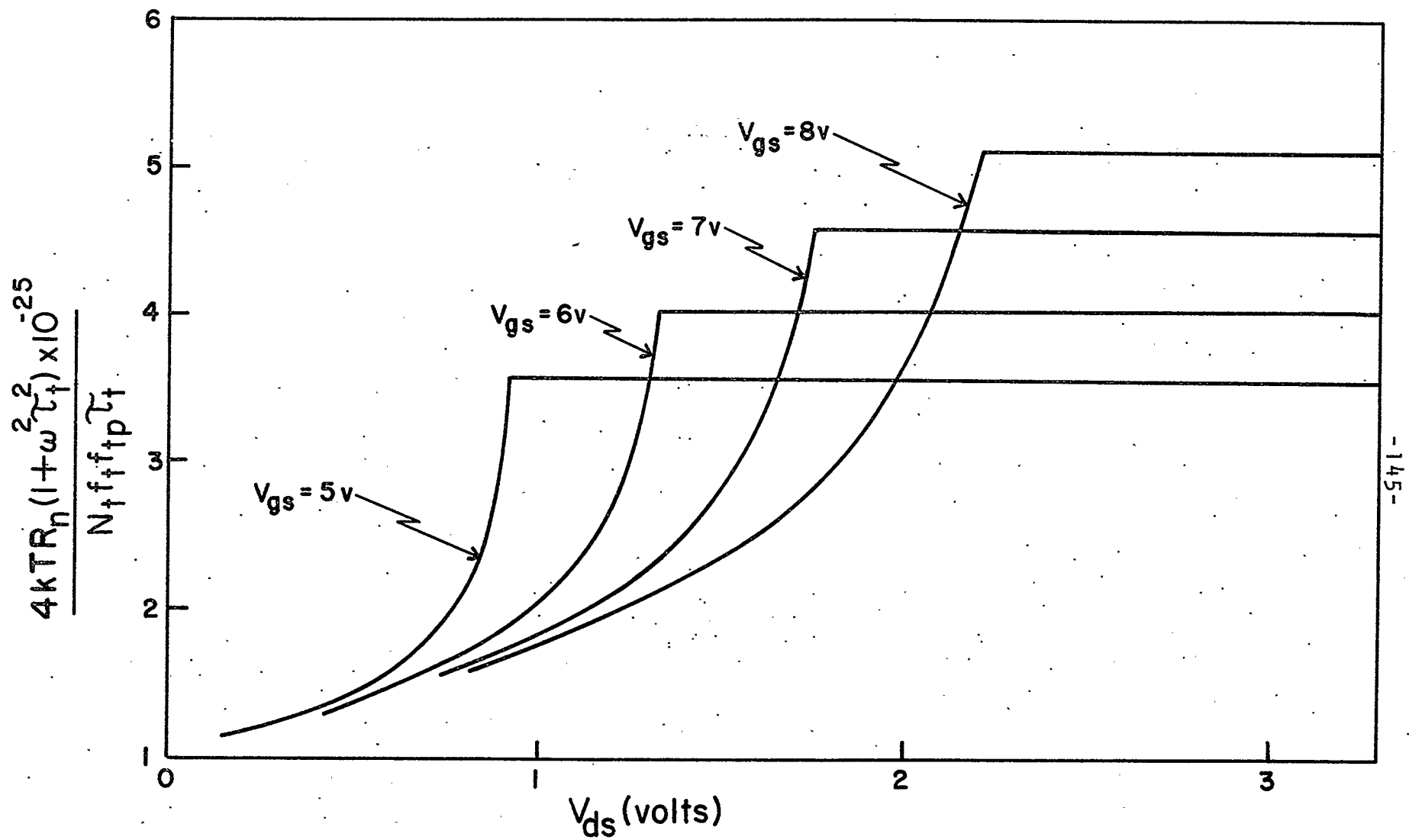


Fig. 6.12 Theoretical generation noise as a function of bias for FET #61.

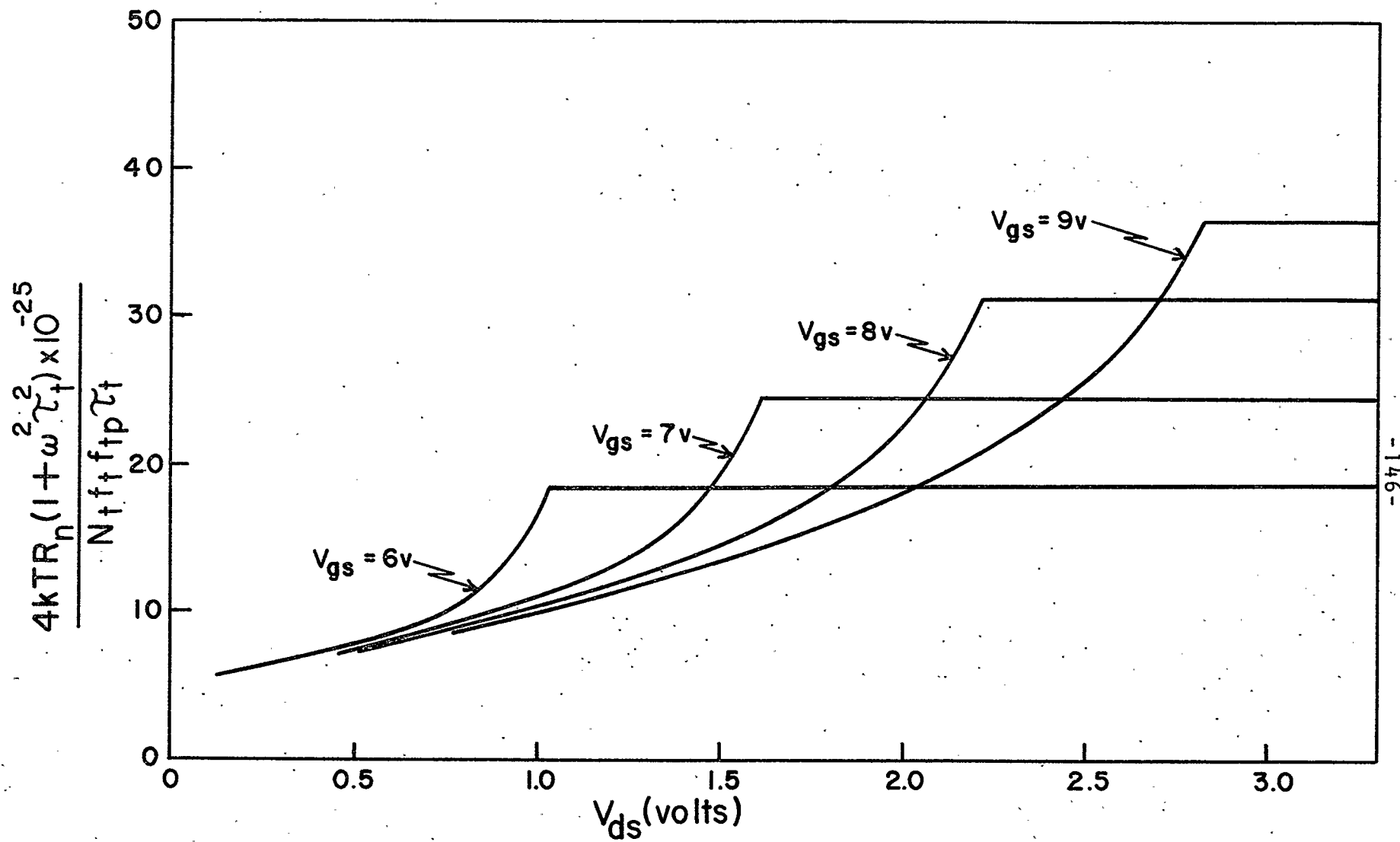


Fig. 6.13 Theoretical generation noise as a function of bias for FET #126.

factor of 2 to 5 for increasing drain voltage prior to pinch-off, and also increases with gate voltage at saturation. This same type of dependence was predicted for the simple theory of surface state noise due to traps at the electron quasi-Fermi level all along the channel. However, the improved theory shows that this type of bias dependence is not expected at all for surface state noise from the tunneling model. With these factors in mind the results can be investigated more closely.

A number of prominent features can be readily observed from the diagrams.

(1) The overall level for the noise from transistor nos. 58 and 55 increases significantly with increasing gate voltage at saturation, while no noticeable increase is observed for nos. 61 and 126.

(2) No increase in the noise level is observed with drain voltage increasing from well below pinch-off to well past pinch-off for any of the four devices. For nos. 58 and 55, the noise decreases slightly.

(3) The shape of the spectrum below 10Hz varies considerably with bias changes for nos. 55, 58 and 126.

(4) For frequencies above 10Hz, the spectrum follows a $1/f$ dependence in all cases except for FET no. 126, where the spectrum is flat to 200Hz, and exhibits a near $1/f^2$ dependence at higher frequencies.

Separate consideration can now be given to the results for each transistor as follows.

(a) FET #58.

From Figs. 6.1 and 6.2, it can be seen that the noise increases with gate bias at pinch-off, and decreases slightly with drain bias increasing prior to pinch-off. This type of dependence indicates that the noise may be due to a high concentration of traps near the valence band edge (it is a p-channel device). Traps at this location are not unreasonable and, in fact, measurements performed by Sah, Pao and Hielscher^{17,26} have indicated that it is common to have high surface state densities at both the conduction and valence band edges. Since the device parameters are known, it is possible to calculate

$$\frac{\overline{e_n^2}}{N_o \Delta f} = \frac{4kTR_n}{N_o} \quad (6.2)$$

using (5.65) where $f_t f_{tp}$ is given by (5.91) and N_o is the trap density per unit volume in the oxide, assumed to be uniformly distributed to a depth of 20\AA . At 1kHz, with $V_{gs} \approx 9\text{v}$, $\overline{e_n^2}/\Delta f$ is approximately $10^{-13} \text{volt}^2/\text{Hz}$ from Fig. 6.2. The calculated value for $\overline{e_n^2}/N_o \Delta f$ is $6.05 \times 10^{-35} \text{volt}^2 \text{cm}^3/\text{Hz}$ which indicates an N_o of approximately $1.6 \times 10^{21}/\text{cm}^3$. This value is slightly larger than would be expected.^{17,26,29,48} However, it should be noted that the overall level of the spectrum is directly proportional to n_1 from (5.91). The temperature would thus have to be known exactly to get an accurate value of n_1 . Finally, traps at or near the electron quasi-Fermi level give larger theoretical noise contributions than traps near the band edges. It is probable that traps

are distributed over the energy gap, thus giving a larger magnitude of the noise for a smaller volume distribution of traps in the oxide.

(b) FET #55

The overall level of the spectrum for this transistor varies in much the same fashion with bias as FET #58, indicating that a large contribution to the noise may be due to traps near the valence band edge. However, in this case the shape of the spectrum varies considerably at low frequencies under conditions of high inversion prior to pinch-off. From Fig. 6.5, it can be seen that below 10Hz, the spectrum follows a near $1/f^2$ dependence with $V_{DS} = 1$ volt, decreasing to something less than a $1/f$ dependence as V_{DS} increases. None of the theories presented in this work would indicate this type of dependence with bias. It is possible that mobility variations at the interface could cause the shape of the spectrum to change. The study of carrier mobility in inversion layers on silicon is very complicated, and will not be reviewed in this work.

(c) FET #'s 61 and 126

These two devices are complementary p and n-channel enhancement type low-power switching transistors. They were chosen to eliminate geometrical dependence of the noise and allow a direct comparison of the two types of transistors. From Figs. 6.7, 6.8 and 6.9 it has become clear that the noise characteristics of the two devices are quite different. The

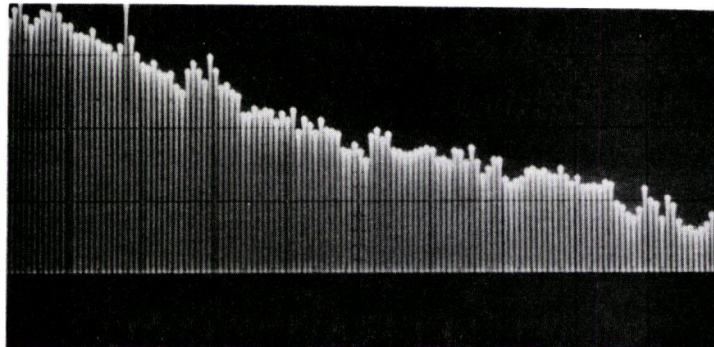
n-channel device (no. 61) shows very little change in the noise with all variations in bias, and follows a near $1/f$ spectrum over the entire measurement range. The p-channel device (no. 126) exhibits a flat spectrum from 10Hz to 200Hz, and then follows a near $1/f^2$ dependence at higher frequencies. Below 10Hz, the shape of the spectrum again varies. However, in this case the shape varies with gate bias with the drain pinched-off, whereas for FET #55, the shape was seen to vary with drain bias prior to pinch-off under heavy inversion conditions.

The distinct corner frequency in the spectrum is indicative of a single time constant trapping process. From Fig. 6.13, it is apparent that generation-recombination noise can be ruled out as the possible cause since the experimental spectrum decreases slightly with increasing gate voltage at saturation, while the theory for generation-recombination noise indicates that the noise should nearly double as V_{gs} goes from 6 to 9 volts. On the other hand, if the plateau is the result of shallow traps in the oxide, then the corner frequency should be a function of bias, since τ_s depends inversely on the electron concentration at the interface. From Fig. 6.9, no such dependence is observed. This indicates that either traps with a single time constant independent of bias exist in the oxide, which is unlikely, or that the pre-dominant noise mechanism is of some other type.

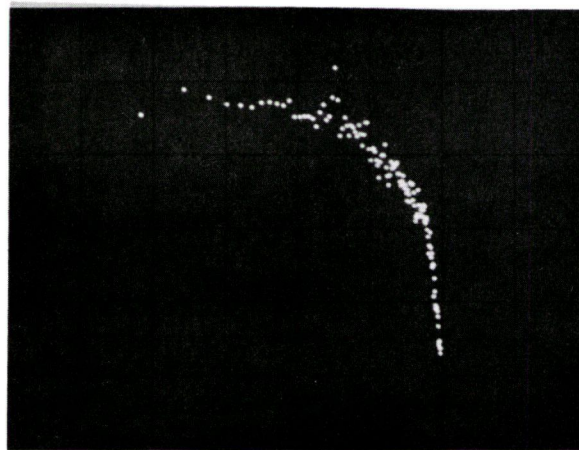
As a matter of interest, a qualitative test of the temperature dependence of the spectrum was made using a real

time Fourier Analyzer. The Analyzer uses an ensemble averaging technique, and 50 ensembles were used for the tests. Two devices of the same make were tested to ensure that the spectrum was not characteristic of a single device. The results are shown in Figs. 6.14 to 6.16.

The shape of the spectrum for both transistors of this type is thus found to be very sensitive to temperature, the lower corner frequency decreasing with a decrease in temperature. From Figs. 6.14 and 6.15, the break frequency decreases from 200Hz at room temperature to less than 20Hz simply by wetting the heat sink with a small amount of contact cleaner. This high sensitivity to temperature seems to indicate the presence of generation-recombination noise, since the time constant has been shown to be highly temperature sensitive,^{31,83} and theoretically varies in the direction observed in this case. This is contrary to the conclusion that generation-recombination noise was not present, as was mentioned earlier. The effect of temperature on the spectrum for surface state noise in MOS FET's is not quite as clear, and to date, to the author's knowledge, no detailed analysis has been performed for the model being used. In fact, the type of spectrum exhibited by FET #126 is not common to all. The response is, indeed, peculiar and warrants further investigation.



(a)

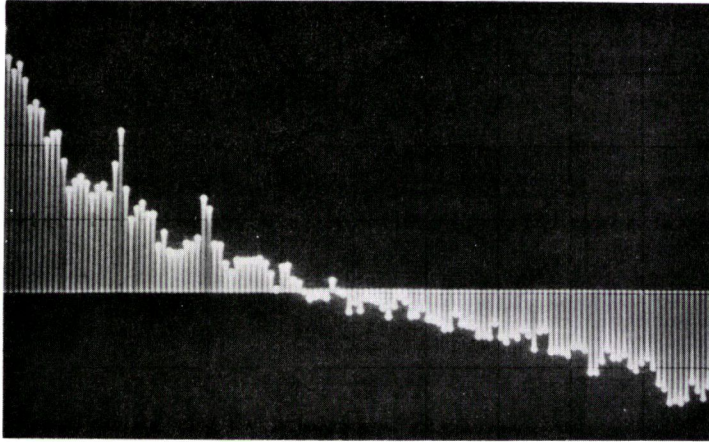


(b)

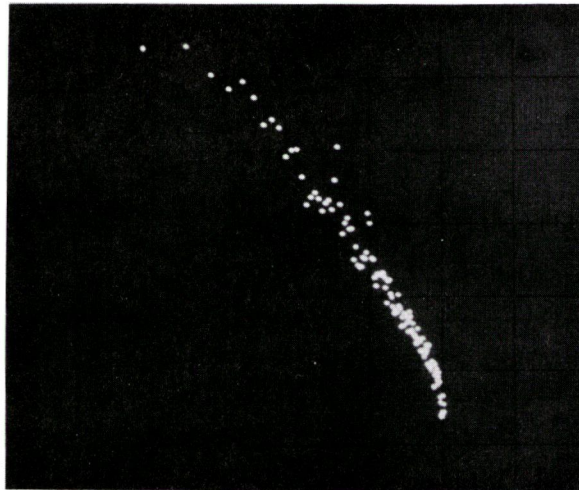
Fig. 6.14 FET #126

(a) Power spectrum with log magnitude vs. linear frequency scale, 0-1 kHz, $V_{gs} = -6V$, $V_{ds} = -10V$, transistor at room temperature.

(b) Same data as in (a) displayed with log-log axes.



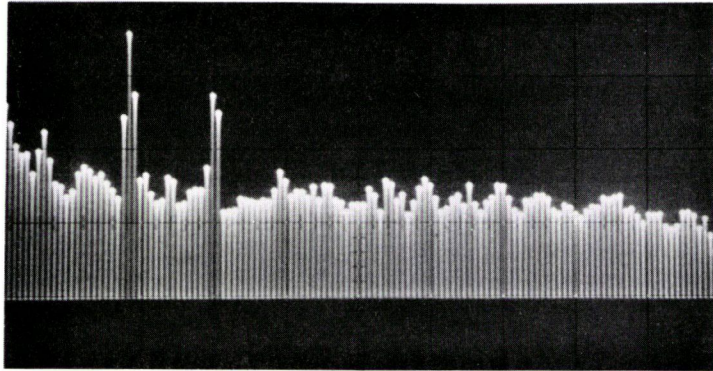
(a)



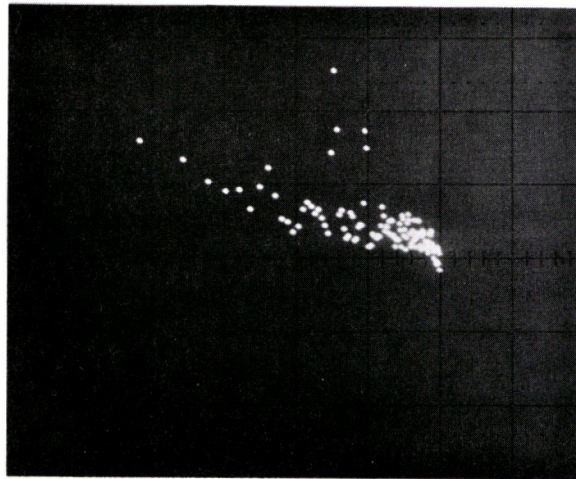
(b)

Fig. 6.15 FET #126

Effect of a slight decrease in temperature on the shape of the spectrum. (a) Log-linear axes. (b) Log-log axes.



(a)



(b)

Fig. 6.16 FET #126.

Effect of an increase in temperature on the shape of the spectrum. (a) Log-linear axes. (b) Log-log axes.

7. CONCLUSIONS AND SUGGESTIONS FOR FUTURE RESEARCH

A unified approach has been used to analyze noise in silicon enhancement-type MOS field-effect transistors at low and moderately high frequencies. Low-frequency generation-recombination noise has been analyzed for a single trapping process using the bulk charge model of Sah,¹⁷ and a theory is derived that prevents the results from diverging at pinch-off. The analysis is found to be in close agreement with recently published results.^{31,71} The effects of the substrate on low frequency surface state noise due to carrier tunneling to traps in the oxide are analyzed in detail. A technique for calculating the carrier concentration per unit volume at the interface along the channel is presented to show that previous theory is oversimplified and misleading in some cases. The effects of different trap distributions in the oxide on the shape and magnitude of the spectrum are examined. The major contribution to the noise comes from traps at energies near or above the quasi-Fermi level for electrons along the channel. The bias dependence of the spectrum is complicated by the energy distribution of traps over the bandgap of the silicon substrate.

The thermal noise characteristics of the Weimer model at moderately high frequencies are presented explicitly in terms of device parameters and bias conditions.³³ The bulk charge theory is reviewed with the inclusion of an external

substrate bias, and the results are used to examine the effects of the substrate on the gate noise at moderately high frequencies.⁸⁴ The results for gate noise and correlation between gate and drain noise are found to be in agreement with those presented recently by Rao⁵⁴ using a different approach. An error has been discovered in his results for the correlation coefficient c , and it is found that c increases slightly over the value for an intrinsic substrate. The gate noise expressions are shown to reduce analytically to the results for the Weimer model for the case of an intrinsic substrate at pinch-off.

Noise measurements are performed using a statistical analysis approach to obtain high resolution and accuracy over a wide frequency range. Experimental variations with bias are compared with theoretical calculations based on the theories derived in previous chapters. The dominant mechanisms are speculated and an estimate of the trap density per unit volume in the oxide is obtained. The model appears to give an approximate order of magnitude for the noise, as well as a $1/f$ dependence over many decades of frequency. However, one of the transistors tested does not behave as the theory predicts. Thus, even though the model appears to give correct results in many cases, it cannot be used to explain all the variations observed. While it was originally hoped that the bias dependence of the noise might be a good indication of the mechanism involved, it has become apparent that no conclusive results can be obtained using this

technique.

There is still a large amount of work to be done on low-frequency noise in semiconductor devices. It has been generally accepted that noise in MOS devices is a surface phenomena, but, as mentioned earlier, there is a wide variety of opinion as to the actual mechanism involved. The theory of the tunneling model has been investigated thoroughly in this work, and it has been found that the model cannot explain all the results observed. It would be very useful to perform a detailed analysis of the effects of temperature on the noise characteristics. However, at this stage it appears that the approach would be very complicated, due to the number of variables involved.

Until very recently, it was thought that an excess noise generator was operating in the channel at high frequencies.^{53,55,85,87} A model assuming mobility fluctuations in the channel was utilized to explain the experimental data. Rao's⁵⁴ results for the correlation coefficient were used to support this theory. However, it has now been shown⁶⁰ that the measurements were not performed at sufficiently high frequencies, and that the results obtained were due to a $1/f$ component in the noise. This work has shown that the correlation coefficient calculations were also in error, so that it appears that the excess noise generator does not exist.

Additional work has been done on very high frequency noise by Klassen and Prins.^{52,88,89} However, many aspects

of high frequency noise can still be investigated. A starting point would be the calculation of thermal noise using a lumped model approach as has been used in this work at moderate frequencies. The author has derived a small-signal high-frequency equivalent circuit for the Weimer model that could be used for this calculation.⁹⁰ Further work would then deal with the effects of the substrate on the noise at high frequencies. Das⁹¹ has recently published a detailed description of high-frequency properties of MOS FET's including the effects of substrate resistivity, which could be used as a basis for the noise calculations.

In general, it appears that until $1/f$ noise mechanisms are more fully understood for MOS capacitors, no significant results will be obtained for the more complicated MOS transistor. Further work should proceed with this in mind.

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APPENDIX A
INTERELECTRODE CAPACITANCE CALCULATIONS FOR
THE MOS FET

A difficulty arises in the calculation of small-signal capacitances for the MOS FET, due to the non-reciprocal nature of the gate-to-bulk characteristics. A small-signal variation in V_{gs} with the substrate ac short-circuited to the source will result in different variations in Q_g , Q_B and Q_n than a small-signal variation in V_{bs} with the gate ac short-circuited to the source. It is therefore difficult to represent the gate-bulk branch of the equivalent circuit with a capacitance. The method of representation that is normally adopted is to calculate the components of small-signal gate and bulk currents associated with the mutual coupling between the gate and substrate and then represent these components by current generators connected to the gate and substrate terminals.^{15,82} In this work, we are only concerned with capacitances associated with the gate-source and gate-drain terminals, as the noise calculations using the split transistor technique are performed assuming gate, source and bulk are ac short-circuited for the transistor of channel length x , and the gate, drain and bulk are ac short-circuited for the transistor of channel length $(L-x)$. The small signal gate and bulk currents can be written as

$$i_g = \frac{dQ_{gt}}{dt} \quad (A.1)$$

$$i_b = \frac{dQ_{Bt}}{dt} \quad (A.2)$$

where Q_{gt} and Q_{Bt} are the total gate and bulk charges, respectively. Using the chain rule, these can be expanded in the form

$$i_g = \frac{dQ_{gt}}{dt} = \frac{\partial Q_{gt}}{\partial V_{gs}} \frac{dV_{gs}}{dt} + \frac{\partial Q_{gt}}{\partial V_{bs}} \frac{dV_{bs}}{dt} + \frac{\partial Q_{gt}}{\partial V_{ds}} \frac{dV_{ds}}{dt} \quad (A.3)$$

$$i_b = \frac{dQ_{Bt}}{dt} = \frac{\partial Q_{Bt}}{\partial V_{gs}} \frac{dV_{gs}}{dt} + \frac{\partial Q_{Bt}}{\partial V_{bs}} \frac{dV_{bs}}{dt} + \frac{\partial Q_{Bt}}{\partial V_{ds}} \frac{dV_{ds}}{dt} \quad (A.4)$$

If the capacitances associated with the gate terminal are denoted as C_{gs} , C_{gd} and C_{gb} , then the gate current may be written in the form

$$i_g = C_{gd} \frac{dV_{gd}}{dt} + C_{gs} \frac{dV_{gs}}{dt} + C_{gb} \frac{dV_{gb}}{dt} \quad (A.5)$$

which can be rewritten as

$$i_g = (C_{gs} + C_{gd} + C_{gb}) \frac{dV_{gs}}{dt} - C_{gd} \frac{dV_{ds}}{dt} - C_{gb} \frac{dV_{bs}}{dt} \quad (A.6)$$

The total gate capacitance, C_{gg} , is represented by

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} \quad (A.7)$$

and is usually associated with the variation in Q_g with V_{gs} from (A.3). This yields

$$C_{gs} + C_{gd} + C_{gb} = \frac{\partial Q_{gt}}{\partial V_{gs}} \quad (A.8)$$

Similarly, the gate-drain capacitance is represented by

$$-C_{gd} = \frac{\partial Q_{gt}}{\partial V_{ds}} \quad (A.9)$$

This means that the component of gate current due to mutual 'capacitance' between gate and bulk is connected with $\partial Q_{gt} / \partial V_{bs}$, and the gate-source and gate-drain capacitances can be written as

$$C_{gs} = \frac{\partial Q_{gt}}{\partial V_{gs}} + \frac{\partial Q_{gt}}{\partial V_{ds}} + \frac{\partial Q_{gt}}{\partial V_{bs}} \quad (A.10)$$

$$C_{gd} = - \frac{\partial Q_{gt}}{\partial V_{ds}} \quad (A.11)$$

for the calculations performed in this work. Other elements of the equivalent circuit can be derived in a similar fashion, but are not of interest as far as the noise calculations are concerned in Chapter 4.

APPENDIX B

STATISTICS OF A FLUCTUATION PROCESS INVOLVING A SINGLE TIME CONSTANT

The statistics of charge carrier density fluctuations in semiconductors has been analyzed in detail by Burgess.^{42,43,44} The statistics for an electron trapping process involving a single time constant are derived here in order to justify the use of equations (5.5) and (5.6) in the noise analysis of Chapter 5.

Consider a situation in which there are n electrons in the conduction band. If the probability that an electron enters the band in time dt is $g(n)dt$ and the probability that an electron leaves in time dt is $r(n)dt$, where $g(n)$ and $r(n)$ are the generation and recombination rates for electrons, then the probability of a transition out of the state n (i.e. into some other state) in time dt is

$[r(n)P(n)+g(n)P(n)]dt$, where $P(n)$ is the probability distribution function of n . Similarly, the probability of a transition into the state n in time dt is

$[r(n+1)P(n+1)+g(n-1)P(n-1)]dt$. The change in the probability of the state (n) with time is then

$$\frac{dP(n)}{dt} = [r(n+1)P(n+1)+g(n-1)P(n-1)] - [r(n)P(n)+g(n)P(n)] \quad (B.1)$$

where $\frac{dP(n)}{dt} = 0$ if $P(n)$ is stationary.

From (B.1) it can be shown⁴² that

$$P(n) = \frac{P(0) \prod_{v=0}^{n-1} g(v)}{\prod_{v=1}^n r(v)}. \quad (B.2)$$

The most probable value of n , denoted as n_0 , is found at the extremum of $P(n)$, that is at the point where

$$P(n) - P(n+1) \approx 0. \quad (B.3)$$

Substituting into (B.2) yields $r(n+1) = g(n)$ and if $n = n_0 \gg 1$,

$$r(n_0) \approx g(n_0). \quad (B.4)$$

Equation (B.4) can also be obtained by examining $\ln[P(n)]$.

Increasing n by 1 yields a change in $\ln[P(n)]$ of

$$\ln \left[\frac{P(n)}{P(n+1)} \right] = 0 \quad (B.5)$$

and substituting from (B.2) gives

$$\ln \left[\frac{r(n+1)}{g(n)} \right] = 0 \quad (B.6)$$

or $r(n_0) \approx g(n_0)$ as before.

Thus for large values of n

$$\frac{d}{dn} \left\{ \ln[P(n)] \right\} \Big|_{n=n_0} \approx 0 \quad (B.7)$$

and it is easy to show that

$$\frac{d^2 \ln[P(n)]}{dn^2} = \frac{g'(n)}{g(n)} - \frac{r'(n)}{r(n)}. \quad (B.8)$$

where the primes denote differentiation with respect to n .

A Taylor series expansion of $\ln[P(n)]$ about n_0 retaining only second order terms yields

$$\ln[P(n)] = \ln[P(n_0)] + (n-n_0) \frac{d}{dn} \ln[P(n)] \Big|_{n=n_0} + \frac{(n-n_0)^2}{2!} \frac{d^2}{dn^2} \ln[P(n)] \Big|_{n=n_0} \quad (B.9)$$

and substituting from (B.7) and (B.8) gives

$$P(n) = [P(n_0)] \exp \left\{ -\frac{1}{2} (n-n_0)^2 \left[\frac{r'(n_0)}{r(n_0)} - \frac{g'(n_0)}{g(n_0)} \right] \right\} \quad (B.10)$$

which is a Gaussian distribution of n about n_0 with variance

$$\overline{(n-n_0)^2} = \left[\frac{r'(n_0)}{r(n_0)} - \frac{g'(n_0)}{g(n_0)} \right]^{-1} \quad (B.11)$$

and the primes denote differentiation with respect to n .

Now the variance of n is also the variance of n_t , the number of occupied traps. In order to apply (B.11) it is necessary to obtain expressions for the rate of generating positively charged trap levels in a given volume $\Delta\Lambda$ and for the rate of generating neutral levels. The total number of traps in the elemental volume $\Delta\Lambda$ is $N_t\Delta\Lambda$. The rate of generating positively charged trap levels is then given by

$$r(n_t, \Delta\Lambda) = (e_n + c_p p) f_t N_t \Delta\Lambda, \quad (B.12)$$

since e_n is the emission probability of an electron, c_p is the capture probability of a hole, and $f_t N_t \Delta\Lambda$ is the fraction of occupied traps in the volume $\Delta\Lambda$. Similarly, the rate of generating neutral levels is

$$g(n_t, \Delta\Lambda) = (e_p + c_n n) f_{tp} N_t \Delta\Lambda \quad (B.13)$$

where e_p , c_n are the emission probability of a hole and capture probability of an electron, respectively, and

$$f_{tp}N_t = (1-f_t)N_t = N_t - n_t. \quad (B.14)$$

Substituting (B.12) and (B.13) into (B.11), and performing the differentiations with respect to n_t gives

$$\overline{(\delta n_t \Delta \Lambda)^2} = \left[\frac{1}{n_t} + \frac{1}{N_t - n_t} \right]^{-1} \Delta \Lambda \quad (B.15)$$

It is then easy to show that the variance of the fluctuation in the occupied trap density is given by

$$\overline{\delta n_t^2} = \frac{N_t f_t f_{tp}}{\Delta \Lambda}. \quad (B.16)$$

The relaxation time constant determining the return from a small deviation to equilibrium is obtained by considering that if at any moment $n \neq n_0$, the rate of change of n towards n_0 is

$$\frac{d}{dt} (n - n_0) = g(n) - r(n) \quad (B.17)$$

where for small deviations

$$g(n) \approx g(n_0) + (n - n_0)[g'(n_0)] \quad (B.18)$$

$$r(n) \approx r(n_0) + (n - n_0)[r'(n_0)] \quad (B.19)$$

so that

$$\frac{d}{dt} (n - n_0) \approx - \frac{(n - n_0)}{\tau_0} \quad (B.20)$$

where

$$\tau_0 = \frac{1}{r'(n_0) - g'(n_0)}. \quad (B.21)$$

Solving (B.20) using $(n-n_0) = \delta n$ and $\delta n = \delta n_0$ at $t = 0$ as a boundary condition yields

$$\delta n = \delta n_0 \exp(-t/\tau_0). \quad (\text{B.22})$$

The autocorrelation function for the aperiodic function of time (B.22) is found from the definition,⁴⁶

$$R(\tau) = \int_0^\infty f(t)f(t+\tau)dt. \quad (\text{B.23})$$

Substituting $\delta n = f(t)$ from (B.22) gives

$$R(\tau) = (\delta n_0)^2 \frac{\tau_0}{2} \exp(-|\tau|/\tau_0). \quad (\text{B.24})$$

The square of the mean value μ is given by

$$\mu^2 = R(\infty) = 0 \quad (\text{B.25})$$

and the mean square value is found from

$$\psi^2 = R(0) = (\delta n_0)^2 \frac{\tau_0}{2}. \quad (\text{B.26})$$

The variance $\overline{\delta n^2}$ is given by

$$\begin{aligned} \overline{\delta n^2} &= \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T (\delta n - \mu)^2 dt \\ &= \psi^2 - \mu^2 \end{aligned} \quad (\text{B.27})$$

or

$$\overline{\delta n^2} = (\delta n_0)^2 \frac{\tau_0}{2} \quad (\text{B.28})$$

so that (B.24) becomes

$$R(\tau) = \overline{\delta n^2} \exp(-|\tau|/\tau_0) \quad (\text{B.29})$$

and the physically realizable one-sided spectral density is given by

$$G(f) = 4 \int_0^{\infty} R(\tau) \cos 2\pi f \tau d\tau \quad 0 < f < \infty. \quad (\text{B.30})$$

where (B.30) is known as the Wiener-Khinchine Theorem.⁴⁶

Substituting from (B.29) and integrating yields

$$G(f) = \frac{\overline{4\delta n^2} \tau_0}{1 + \omega^2 \tau_0^2}, \quad (\text{B.31})$$

the one-sided spectral density for a relaxation process involving a single time constant.

APPENDIX C

A REVIEW OF THE TUNNELING THEORY

A simple model for the potential variation between semiconductor and oxide has been utilized to explain the dispersion in time constants which gives rise to the $1/f$ spectrum for the noise.^{29,72} Traps are assumed to be located randomly in the oxide near the oxide-semiconductor interface, so that electrons will tunnel to the traps, remain for a time that depends on the distance of the trap from the interface and the surface density of free carriers, and then return to the conduction band and the inversion layer at the interface. The theory and its application to MOS transistors as presented by Christensson et al²⁹ is reviewed in detail in the following sections.

C.1 The Tunneling Model

A simple step in energy is assumed between the oxide and silicon as shown in Fig. C.1.

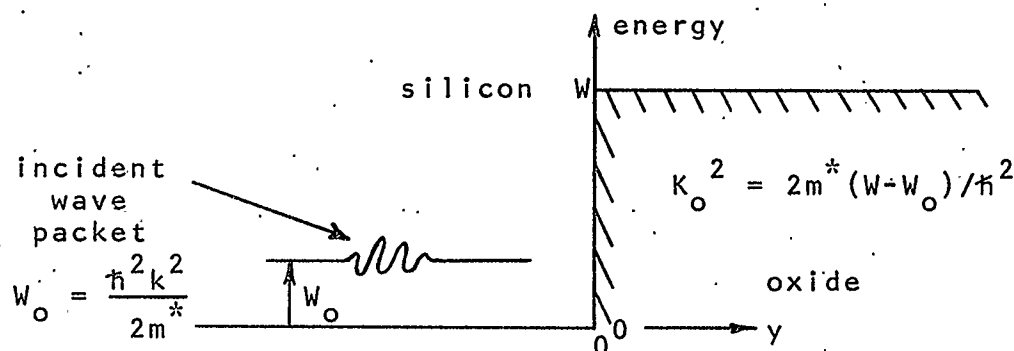


Fig. C.1 Simple potential barrier used for calculating trap time constants.

It can then be shown⁷² that for an electron at the surface, the 'capture probability' for a trap located at a distance y from the interface into the oxide is given by

$$c_n(y) = c_n \exp(-2K_0 y) \quad (C.1)$$

where c_n = capture probability for an electron near a trap in the oxide, assumed to be the same for all traps

$$K_0 = \left[2m^* (W - W_0) / \hbar \right]^{\frac{1}{2}}$$

W = height of the potential barrier

W_0 = energy of the impinging electron

\hbar = Plank's constant divided by 2π

m^* = effective electron mass.

Then using (5.1), assuming that p_0 and p_1 are small, the relaxation time constant is given by

$$\tau = \frac{1}{[c_n(y)] (n_s + n_1)} = \tau_s \exp(\alpha y) \quad (C.2)$$

where

$$\alpha = \frac{2}{\hbar} \sqrt{2m^* W} \quad (C.3)$$

$$\tau_s = \frac{1}{c_n (n_s + n_1)} \quad (C.4)$$

and it is assumed that $W \gg W_0$ to ensure that the decay constant K_0 is the same for all electrons. The capture cross section c_n is of the order of $10^{-8} \text{ cm}^3/\text{sec}$,⁷³ while n_s varies from 10^{16} to $10^{19}/\text{cm}^3$. For traps located a few angstroms into the oxide, the time constant can vary over many orders

of magnitude, thus giving the required dispersion necessary to produce the $1/f$ noise.

C.1.1 Application of the Model

In order to perform the noise calculations for the MOS FET, it is necessary to consider that traps may be distributed in energy over the forbidden gap, as well as spatially distributed in the oxide. The two types of distributions are shown in Fig. C.2.

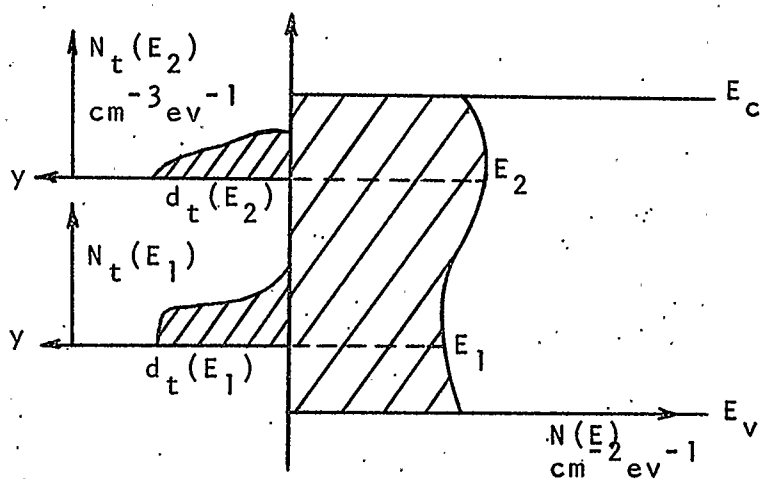


Fig. C.2 Two different types of trap distributions: over energy, $N(E)$, and in the oxide, $N_t(E)$.

If traps are located at a distance y from the interface, the surface state noise must be evaluated by considering a fluctuation in the trapped charge in a volume element $z\Delta x\Delta y$ located in the oxide. It is assumed that there is a uniform distribution of traps N_0 per unit volume over a distance d from the interface into the oxide, where the traps may be distributed over the energy bandgap of the substrate, and the

distance d is much less than the oxide thickness T_{ox} . The situation is then similar to that in section 5.2, where the bulk charge is assumed uniform over a distance y_d in the bulk. In this case a fluctuation δn_{ts} in the trapped charge n_{ts} located in a volume $z\Delta x\Delta y$ causes an incremental fluctuation in the potential from bulk to metal given by the moment formula,

$$\Delta(\delta\psi_{bm}) = - \frac{q}{\epsilon_{ox}} \delta n_{ts} y \Delta y \quad (C.5)$$

and at the same time the charge in the oxide fluctuates by an amount $q\delta n_{ts}\Delta y$. Straightforward analysis then leads to

$$\Delta(\delta Q_n) = [\Delta(\delta V)] (C_{ox} + \frac{\epsilon_s}{y_d}) + q\delta n_{ts}\Delta y(1 + \frac{y}{T_{ox}}) \quad (C.6)$$

and repeating the procedure for calculating R_n assuming traps to be located at a single energy level gives

$$R_n = \frac{-q^2 N_o}{kTLzC_{ox}^2} \frac{\theta}{V_{ds}^2} \int_0^{V_{ds}} \int_0^d \frac{\tau(1 + \frac{y}{T_{ox}})^2}{1 + \omega^2 \tau^2} \frac{f_t f_{tp}}{\Gamma} dy dV. \quad (C.7)$$

where $\theta = \frac{I_d L}{\mu_n z C_{ox}}$ and $\Gamma = Q_n / C_{ox}$. The factors θ and Γ may be evaluated for either the Weimer or bulk charge models of the device. The integral with respect to y is performed from zero to d , so that the term $(1 + \frac{y}{T_{ox}})$ is at most $(1 + \frac{d}{T_{ox}})$. Normally d is only a few angstroms, compared to a typical oxide thickness of 2000 angstroms, so that $d/T_{ox} \ll 1$ and to a very good approximation the term can be neglected in the integral. Then noting that f_t , f_{tp} and Γ are independent of y , and that

$$\frac{d\tau}{dy} = \alpha\tau \quad (C.8)$$

from (C.2), it can be shown that

$$\int_0^d \frac{\tau(1+\frac{y}{T_{ox}})^2}{1+\omega^2\tau^2} dy \doteq \frac{1}{\alpha\omega} \left\{ \tan^{-1} [\omega\tau_s \exp(\alpha d)] - \tan^{-1}(\omega\tau_s) \right\} \quad (C.9)$$

The factor τ_s varies between 10^{-8} and 10^{-11} seconds. If d is 20 Å, and $W = 4.0$ eV, $\tau_s \exp(\alpha d)$ is greater than 10^6 under normal conditions, and $\tan^{-1}[\omega\tau_s \exp(\alpha d)]$ is nearly $\frac{\pi}{2}$ down to very low frequencies. The spectrum is of the form

$$\int_0^d \frac{\tau(1+\frac{y}{T_{ox}})^2}{1+\omega^2\tau^2} dy = \frac{1}{\alpha\omega} \left[\frac{\pi}{2} - \tan^{-1}(\omega\tau_s) \right] \quad (C.10)$$

which exhibits a $1/f$ dependence down to very low frequencies and up to frequencies where thermal noise becomes important. (A more general analysis which results in a dependence other than $1/f$ has recently been published by Berz.⁹⁹) Then in the frequency range of interest, (C.7) becomes

$$R_n \approx \frac{-q^2 N_o \pi}{2kTLzC_{ox}^2 \alpha \omega} \frac{\theta}{V_{ds}^2} \int_0^{V_{ds}} \frac{f_t f_{tp}}{\Gamma} dV. \quad (C.11)$$

It has been shown²⁴ that the assumption of constant $f_t f_{tp}$ is reasonable for the case of generation-recombination noise, since the electron and hole concentrations in the depletion region are small. However, at the surface, the electron concentration is large and varies from source to

drain, so that the dependence of f_t and f_{tp} on drain voltage must be taken into account for the case of surface state noise.

If the trapping processes are governed by Fermi-Dirac statistics, it can be shown that, in general,

$$f_t f_{tp} = \frac{p_1 p_s + n_1 n_s + \gamma (n_i^2 + n_s p_s)}{[n_s + n_1 + \gamma (p_s + p_1)]^2} \quad (C.12)$$

where p_s , p_1 , n_s and n_1 are given by

$$p_s = n_i \exp (E_i - E_p) / kT \Big|_{y=0} \quad (C.13)$$

$$p_1 = n_i \exp (E_i - E_t) / kT \Big|_{y=0} \quad (C.14)$$

$$n_s = n_i \exp (E_n - E_i) / kT \Big|_{y=0} \quad (C.15)$$

$$n_1 = n_i \exp (E_t - E_i) / kT \Big|_{y=0} \quad (C.16)$$

In order to evaluate (C.12), it is necessary to know the energy location of the traps. It is possible to have traps at many energy levels in the gap, as shown in Fig. C.3.

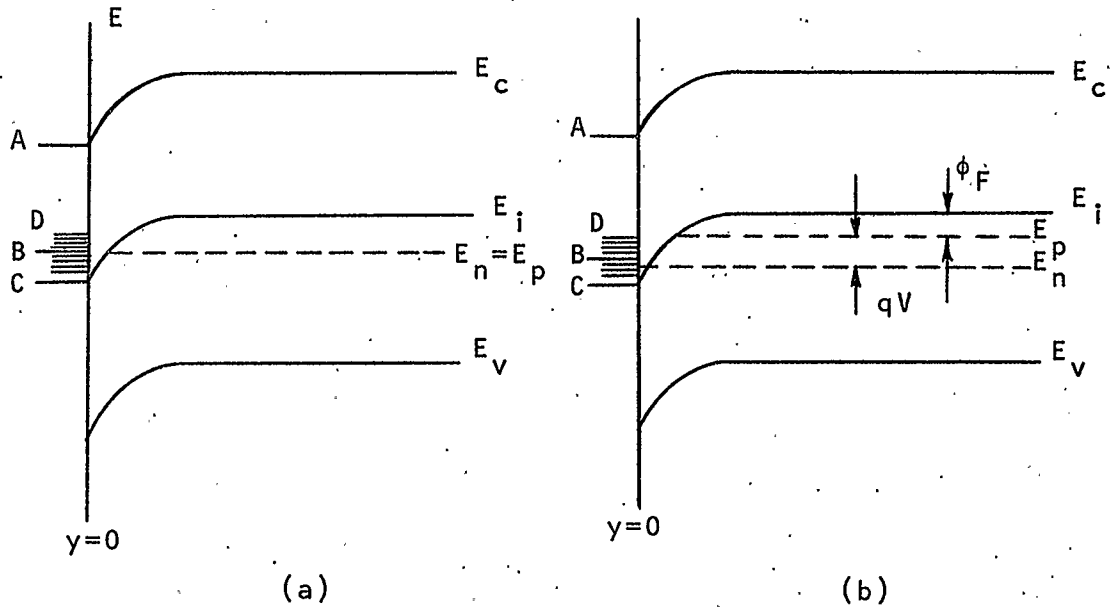


Fig. C.3 Energy band diagram at (a) the source
(b) a point x in the channel.

The letters correspond to

- A. Traps at the conduction band edge
- B. Traps at the Fermi level at the source
- C. Traps at midgap
- D. Traps at the electron Fermi level along the whole channel.

Traps at the valence band edge are not of particular interest. This can be seen as follows. With $E_t = E_v$, it can be shown that

$$p_1 \approx n_i \exp(E_g/2kT) \quad (C.17)$$

$$n_1 \approx n_i \exp(-E_g/2kT) \quad (C.18)$$

so that $p_1 \gg n_1$. There are two cases to consider, namely light and heavy inversion.

If the surface is lightly inverted, then

$$(E_p - E_i)|_{y=0} < (E_i - E_v)|_{y=0} \quad (C.19)$$

and

$$p_i p_s = n_i^2 \exp \left[(E_i - E_p + E_i - E_v) / kT \right] |_{y=0} > n_i^2 \quad (C.20)$$

so that

$$p_i > n_s \gg p_s > n_i \quad (\text{light inversion}) \quad (C.21)$$

and

$$f_t f_{tp} \approx \frac{p_s}{(p_i + n_s)} \quad (C.22)$$

For conditions of heavy inversion, it is possible to have

$$(E_p - E_i)|_{y=0} > (E_i - E_v)|_{y=0} \quad (C.23)$$

Then

$$p_i p_s < n_i^2 \quad (C.24)$$

$$n_s p_s \leq n_i^2 \quad (C.25)$$

and

$$n_{os} > p_i \gg n_i > p_s \quad (\text{heavy inversion}) \quad (C.26)$$

so that $f_t f_{tp}$ is given by

$$f_t f_{tp} \approx \frac{n_i^2}{(p_i + n_s)^2} \quad (C.27)$$

In both cases p_i and n_s are so much larger than n_i and p_s that $f_t f_{tp}$ is very small and the noise contribution from traps at this level is negligible. Even the case of traps at midgap

at the interface gives a noise contribution which is small compared to traps located at energies above the quasi-Fermi level for electrons in the channel, as will be shown in the analysis to follow.

In order to evaluate the integral in (C.11), it is necessary to know the variations in n_s and p_s with distance along the channel, and also to know the dependence of n_{os} on gate voltage. The theory presented by Christensson et al²⁹ assumed that the concentration varied as

$$n_s = \frac{n_{os}(V_p - V)}{V_p} \quad (C.28)$$

where $V_p = V_{gs} - V_T$, the pinch-off voltage for the Weimer model.

It was further assumed that $n_s n_i > n_i^2$ everywhere, which made the integral in (C.11) convergent for all values of V_{ds} . The magnitude of the noise was then evaluated using a typical value for n_{os} of $10^{16}/\text{cm}^3$ for normal inversion conditions. The simple theory using (C.28) is reviewed briefly here to serve as a basis for the analysis in Chapter 5.

At the surface, the electron concentration n_s is much larger than p_s , and

$$p_s n_s = n_i^2 \exp \left[(E_n - E_p) / kT \right] \leq n_i^2 \quad (C.29)$$

so that with $\gamma = 1$, (C.12) is given by

$$f_t f_{tp} \approx \frac{n_i n_s}{(n_s + n_i + p_i)^2} \quad (C.30)$$

Using this approximation, the noise calculations can be performed analytically for the four trap situations shown in Fig. C.3.

Case (a). Traps at the conduction band edge at the interface.

In this case, $E_t = E_c$, and both E_p and E_n are larger than E_i so that

$$n_1 > n_{os} \gg p_1. \quad (C.31)$$

Using (C.31) to evaluate (C.30), the voltage dependent portion of R_n becomes

$$F(V_{ds}) = \frac{(v_s + v_d)}{2(v_s - v_d)} \int_0^{V_{ds}} \frac{f_t f_{tp}}{v} dv \quad (C.32)$$

where v_s , v_d and v are defined by (2.2), (2.3) and (4.6) respectively.

Equation (C.32) can be integrated to yield

$$F(V_{ds}) \approx \frac{n_{os}}{n_1} \frac{(2V_p - V_{ds})}{2V_p}. \quad (C.33)$$

When $V_{ds} = V_p$,

$$F(V_{ds}) \approx \frac{1}{2} \frac{n_{os}}{n_1} \quad (C.34)$$

and

$$F(0) \approx \frac{n_{os}}{n_1}. \quad (C.35)$$

Thus the noise decreases with increasing drain voltage prior to pinch-off, and increases with increasing gate voltage at any given drain bias.

Case (b). Traps at the electron quasi-Fermi level at the source.

If $E_n = E_p = E_t$, it is easy to show that

$$n_1 = n_{os} > p_1 = p_{os}. \quad (C.36)$$

Substitution into (C.32) yields

$$F(V_{ds}) \approx \frac{1}{4} \quad (C.37)$$

and the noise is independent of bias.

Case (c). Traps at midgap at the interface.

For this situation $E_t = E_i$ and E_n, E_p are both greater than E_i so that

$$p_1 = n_1 = n_i \ll n_{os}. \quad (C.38)$$

Substitution and integration gives

$$F(V_{ds}) \approx \frac{n_i}{2n_{os}} \frac{(2V_p - V_{ds})}{(V_p - V_{ds}) + \frac{2n_i}{n_{os}}(2V_p - V_{ds})}. \quad (C.39)$$

When $V_{ds} = V_p$,

$$F(V_p) \approx \frac{1}{4} \quad (C.40)$$

and when $V_{ds} = 0$,

$$F(0) \approx \frac{n_i}{n_{os}}. \quad (C.41)$$

The noise apparently increases many orders of magnitude as the drain voltage increases prior to pinch-off for traps in this location.

Case (d). Traps at the electron quasi-Fermi level along the whole channel.

In this case it is assumed that traps are distributed over energy in the region of the electron quasi-Fermi level, and that traps at the Fermi level at each point along the channel are effective in the capture process. Since the trap density, fraction of occupied traps, and trap time constant are functions of energy as well as voltage and spatial location, the direct integration of (C.7) is not valid for this case. The expression for R_n in modified form is given by

$$R_n = \frac{-q^2 \theta}{kTLzC_{ox}^2 V_{ds}^2} \int_0^{V_{ds}} \int_{E_v}^{E_c} d_t(E) \frac{\tau N_t(E) (1 + \frac{y}{T_{ox}})^2}{1 + \omega^2 \tau^2} \frac{f_t(V,E) f_{tp}(V,E)}{\Gamma} dy dE dV \quad (C.42)$$

where $f_t(V,E)$ = fraction of occupied traps at energy E

$$f_{tp}(V,E) = 1 - f_t(V,E)$$

$d_t(E)$ = distance into the oxide over which traps of energy E are distributed

and $N_t(E)$ = trap distribution over energy and over distance into the oxide (see Fig. C.2).

If the trap density is uniform over distance, and assuming $d_t(E) = d$ for all trap energies, (C.42) becomes

$$R_n \approx \frac{-q^2 \pi \theta}{2kTLzC_{ox}^2 V_{ds}^2 \alpha \omega} \int_0^{V_{ds}} \int_{E_v}^{E_c} \frac{[N_t(E)] f_t(V,E) f_{tp}(V,E)}{\Gamma} dE dV \quad (C.43)$$

in the frequency range of interest.

It is necessary to evaluate

$$T = \int_{E_v}^{E_c} [N_t(E)] f_t(V, E) f_{tp}(V, E) dE \quad (C.44)$$

since

$$n_i = n_i \exp [(E - E_i)/kT] \quad (C.45)$$

and

$$p_i = n_i \exp [(E_i - E)/kT] \quad (C.46)$$

For a uniform distribution of traps over energy, given by $N_{ss}(E)$, it can be shown²⁹ that

$$T \approx [N_{ss}(E)] kT \left[1 - 2 \left(\frac{n_i}{n_s} - \frac{p_s}{n_i} \right) \frac{(E_i - E_n)}{kT} \right] \quad (C.47)$$

$$\approx [N_{ss}(E)] kT, \quad n_s \gg n_i. \quad (C.48)$$

However, for the simple theory, when $n_s \rightarrow 0$ at the drain, (C.47) diverges to infinity, and the dependence of $f_t f_{tp}$ on n_s is not properly reflected. In order to integrate with respect to channel voltage, Christensson et al²⁹ have shown that a good approximation is

$$\int_{E_v}^{E_c} [N_t(E)] f_t(V, E) f_{tp}(V, E) dE \approx [N_t(E_n)] 4kT f_t(V, E_n) f_{tp}(V, E_n) \quad (C.49)$$

since the integrand is sharply peaked about $E = E_t$ with a value of 1/4 at the peak. From (C.49), the result is that the 'effective trap density' N_T is given by

$$N_T \approx 4kT [N_t(E_n)]. \quad (C.50)$$

Then $f_t(V, E_n) f_{tp}(V, E_n)$ can be found by examining the quantities n_s , n_i , p_s and p_i , given by

$$n_s = n_i \exp \left[\frac{(E_n - E_i)}{kT} \right] \Big|_{y=0} \quad (C.51)$$

$$n_i = n_s \exp \left[\frac{(E_t - E_n)}{kT} \right] \Big|_{y=0} \quad (C.52)$$

$$p_s = \frac{n_i^2}{n_s} \exp \left[\frac{(E_n - E_t)}{kT} \right] \Big|_{y=0} \quad (C.53)$$

$$p_i = n_i \exp \left[\frac{(E_i - E_t)}{kT} \right] \Big|_{y=0} \quad (C.54)$$

If $E_t = E_n$ at all points along the channel, (C.12) becomes

$$f_t(V, E_n) f_{tp}(V, E_n) \approx \frac{n_s^2}{\left(2n_s + \frac{n_i^2}{n_s} \right)^2} \quad (C.55)$$

The term n_i^2/n_s cannot be neglected in the simple theory, since $n_s \rightarrow 0$ at the drain at pinch-off. Substituting (C.49) into (C.43), and using $n_i \ll n_{os}$ after integrating gives

$$F(V_{ds}) \approx \frac{(2V_p - V_{ds})}{16V_{ds}} \ln \left[\frac{2}{2 \left(\frac{V_p - V_{ds}}{V_p} \right)^2 + \left(\frac{n_i}{n_{os}} \right)^2} \right] \quad (C.56)$$

and

$$F(V_p) \approx \frac{1}{8} \ln \left(\frac{n_{os} \sqrt{2}}{n_i} \right) \quad (C.57)$$

$$F(0) \approx \frac{1}{4} \quad (C.58)$$

This indicates that the noise increases with gate voltage at pinch-off and with drain voltage prior to pinch-off.

The theory described in the previous sections forms a basis for the improved analysis of Chapter 5.

APPENDIX D

THE NOISE MEASUREMENT SYSTEM

It is possible to measure a number of parameters when comparing device noise performance with theoretical calculations. For junction transistors, the minimum parameters required to describe the noise performance are two equivalent noise generators and a cross-correlation coefficient. With field-effect transistors, the main origin of noise is the fluctuation of the drain current, so that it is possible to represent the noise performance of the device by a single current generator at the output. If the input is ac short circuited, the noise can also be represented by a single voltage generator in series with the input, which can then be associated with the thermal noise of an equivalent noise resistance R_n .^{30,93,94,95} In this work, the equivalent noise voltage referred to the input is measured exclusively. Flinn et al³⁰ have mentioned that it is not practical to refer the noise to the input at low drain voltages, since g_m decreases and the gain decreases proportionately. However, measuring the noise current at the output is also a problem since at low drain voltages, part of the noise current flows through the output impedance and the current through the load resistance must be corrected accordingly. The decrease in drain voltage will only cause a problem if the gain of the first stage decreases to the point where amplifier noise becomes important. The measurements in this work were performed

under conditions where this was not a problem. If it is desired to obtain the mean square current at the output from the experimental results, the relationship

$$\overline{i_d^2}/\Delta f = 4kTR_n g_m^2 = \overline{e_n^2} g_m^2 / \Delta f \quad (D.1)$$

can be used with the results shown in Figs. D.1 and D.2. In Fig. D.2, the carrier mobility μ_{eff} has been reduced from the bulk value μ_b to bring the theoretical curves into close proximity with the experimental results. When using (D.1) for the measured values of the noise, the experimental values of g_m should be chosen throughout.

D.1 THE STATISTICAL ANALYSIS APPROACH

The digital processing approach to noise measurements is not a completely new idea. Firlie and Winston⁶² used standard IBM methods to measure noise at frequencies below 10^{-2} Hz in 1955. In this work, it was desired to have a fast method of measuring complete noise spectra as a function of bias, rather than to measure the noise at one or two discrete frequencies. A generalized commercially available spectral analysis program written for use on the IBM 360/50 system provided the speed and accuracy desired. No attempt will be made to describe the operation of the program, as it is discussed in detail by Enochson and Otens.⁹⁶

The basic noise measurement system is shown in Fig. D.3.

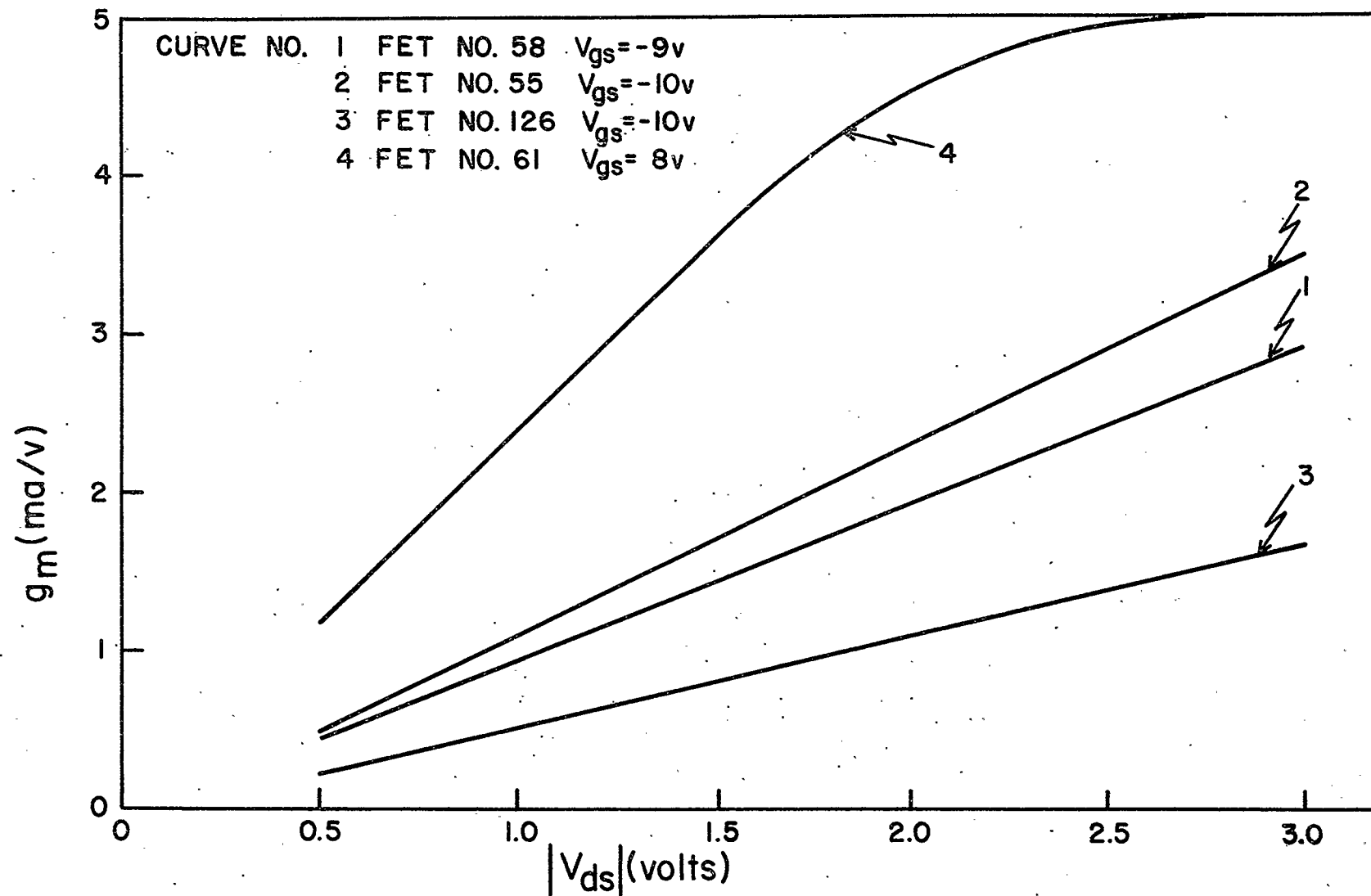


Fig. D.1 Transconductances as a function of drain voltage below pinch-off.

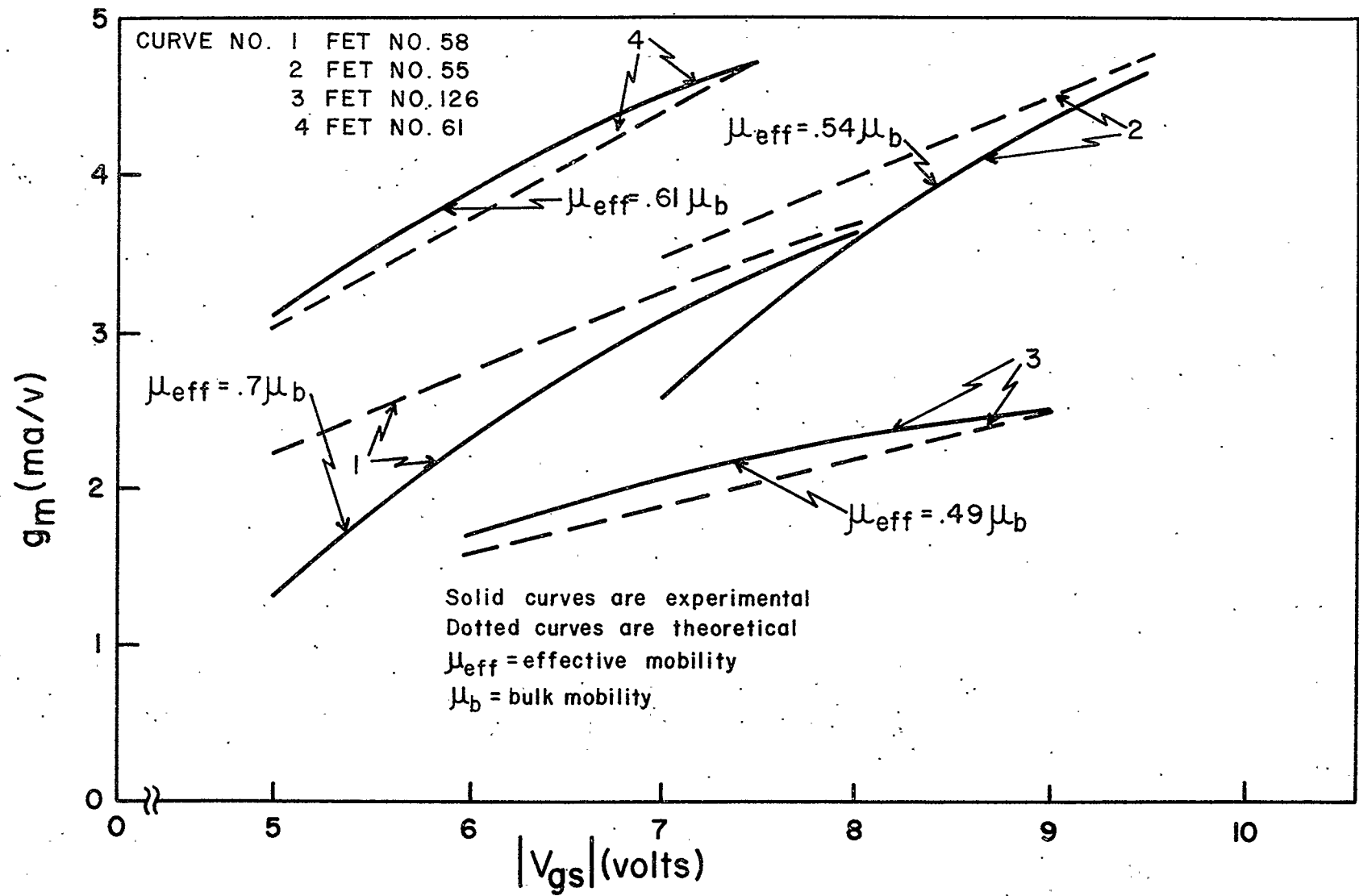


Fig. D.2 Transconductances as a function of gate voltage at pinch-off.

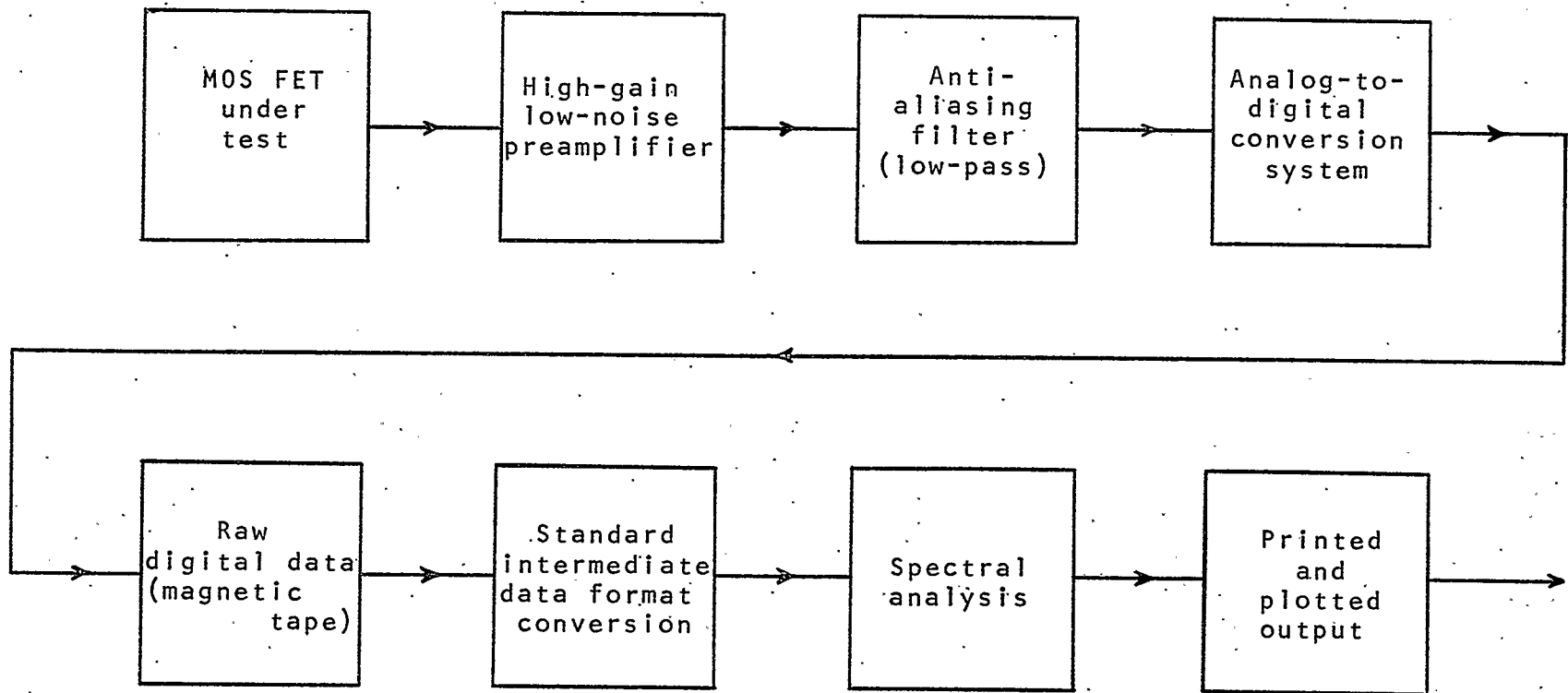


Fig. D.3 The basic noise measurement system.

To prepare the random analog noise signal for digital analysis, appropriate amplification, low-pass filtering, analog-to-digital conversion, magnetic tape storage, and tape format conversion are required. Details of the analog-to-digital conversion system are shown in Fig. D.4. The appropriate single-channel sampling program is read by the paper tape reader and stored in the small digital computer. The required sampling frequency and number of samples is specified on the teletype unit and the corresponding rate is set on the pulse generator. The computer collects samples in blocks of 2000 'words', and then dumps them onto digital magnetic tape. The teletype prints out a permanent record of tape file numbers and relevant information required for digital processing. The raw data tape obtained is compatible with IBM tape readers, but is not in the correct format for the spectral analysis program. A conversion to the standard intermediate data tape format is performed using a separate program. Spectral analysis then yields printed and plotted output of the power spectral density of the input noise. The input data is scaled by the gain factor before processing so that the output plot is a direct measure of the noise power referred to the input of the system.

The method of choosing the sampling frequency, number of samples, resolution bandwidth, and statistical accuracy desired is as follows.^{97,98}

- (1) The maximum frequency of interest, f_m , is chosen. Low-pass filtering of the analog data at the maximum frequency

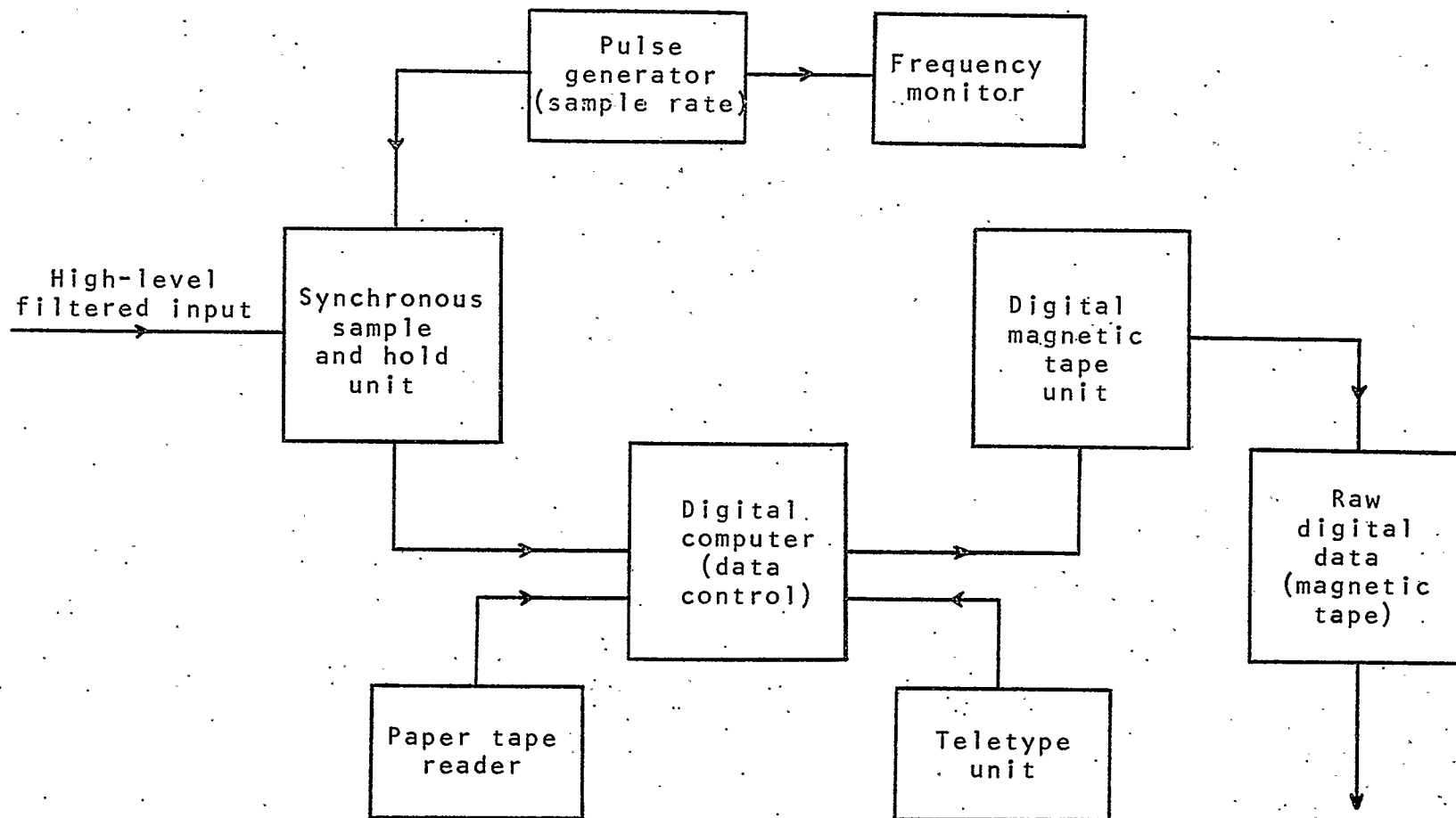


Fig. D.4 The A/D conversion system.

of interest is required to prevent 'aliasing'. Aliasing refers to the effect of frequency folding about the Nyquist frequency (one half the sampling frequency, f_s). The power spectral density evaluated after sampling can be distorted if frequency components beyond the Nyquist frequency are allowed to alias or add to the true spectrum. Filtering assures that the high-frequency components are removed and the resulting power spectral density is a true representation.

The sampling frequency f_s must be at least twice f_m and is normally chosen as

$$f_s = 3f_m. \quad (D.2)$$

The cut-off frequency of the anti-aliasing filter is then set at f_m .

- (2) The minimum resolvable frequency bandwidth B_e for the spectral calculations is next specified. This parameter represents the narrowest frequency band which can be discriminated in the calculation of the power spectral density. It is analogous to Δf used in the preceding chapters. As B_e increases, the power spectral density curves become artificially smoothed, covering up prominent frequency components in the data. Care must be taken to choose B_e small enough to detect any significant periodicity in the noise.

- (3) The statistical accuracy is selected to ensure that the resulting spectra are statistically reliable and smooth. The number of statistical degrees of freedom, ν , can be used as a measure of statistical accuracy, with $\nu = 100$ assuring that the calculated spectrum will lie within ± 1 db of the true spectrum 90% of the time. The choice of ν with a fixed value of B_e then determines the minimum record length T_r required, since

$$\nu = 2B_e T_r. \quad (D.3)$$

- (4) The number of samples, N , required to achieve the specified n and B_e at the sampling frequency f_s , is given by

$$N = \frac{\nu f_s}{2B_e}. \quad (D.4)$$

If the data record length T_r is limited or if there is a limitation in the number of samples which can be economically processed, a trade-off between n and B_e is required, as shown in equation (D.3) where

$$T_r = N/f_s. \quad (D.5)$$

- (5) Finally, it can be shown that the values of the power spectral density should be calculated at the following discrete frequencies:

$$f = \frac{\ell B_e}{2}, \quad \ell = 0, 1, 2, \dots, f_s/B_e, \quad (D.6)$$

to provide independent spectral estimates.^{97,98}

The system is set up to provide spectral estimates down to very low frequencies. In this work, the preamplifiers used were ac coupled to prevent drift problems which arose due to the large gain needed to provide large enough signals for the A/D conversion system. The frequency response of the system was approximately flat from 2Hz to 10kHz. Schematic diagrams of the preamplifiers and typical gain characteristics are shown in Figs. D.5, D.6, D.7 and D.8. The upper limit of 10kHz was imposed by the A/D system, and the amplifier response was adjusted accordingly.

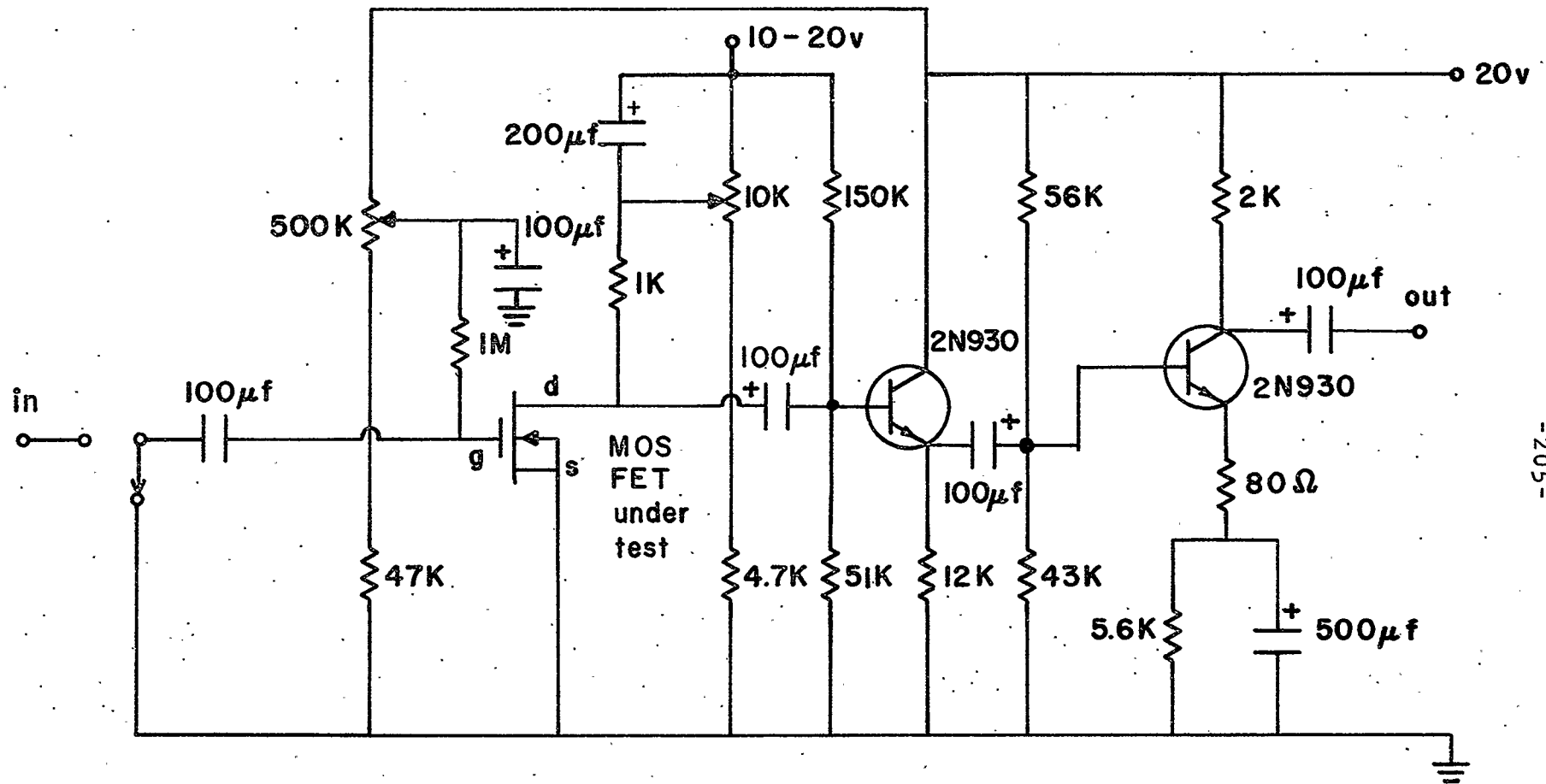


Fig. D.5 The preamplifier incorporating the MOS FET as a first stage.
A similar amplifier was used for p-channel FET's.

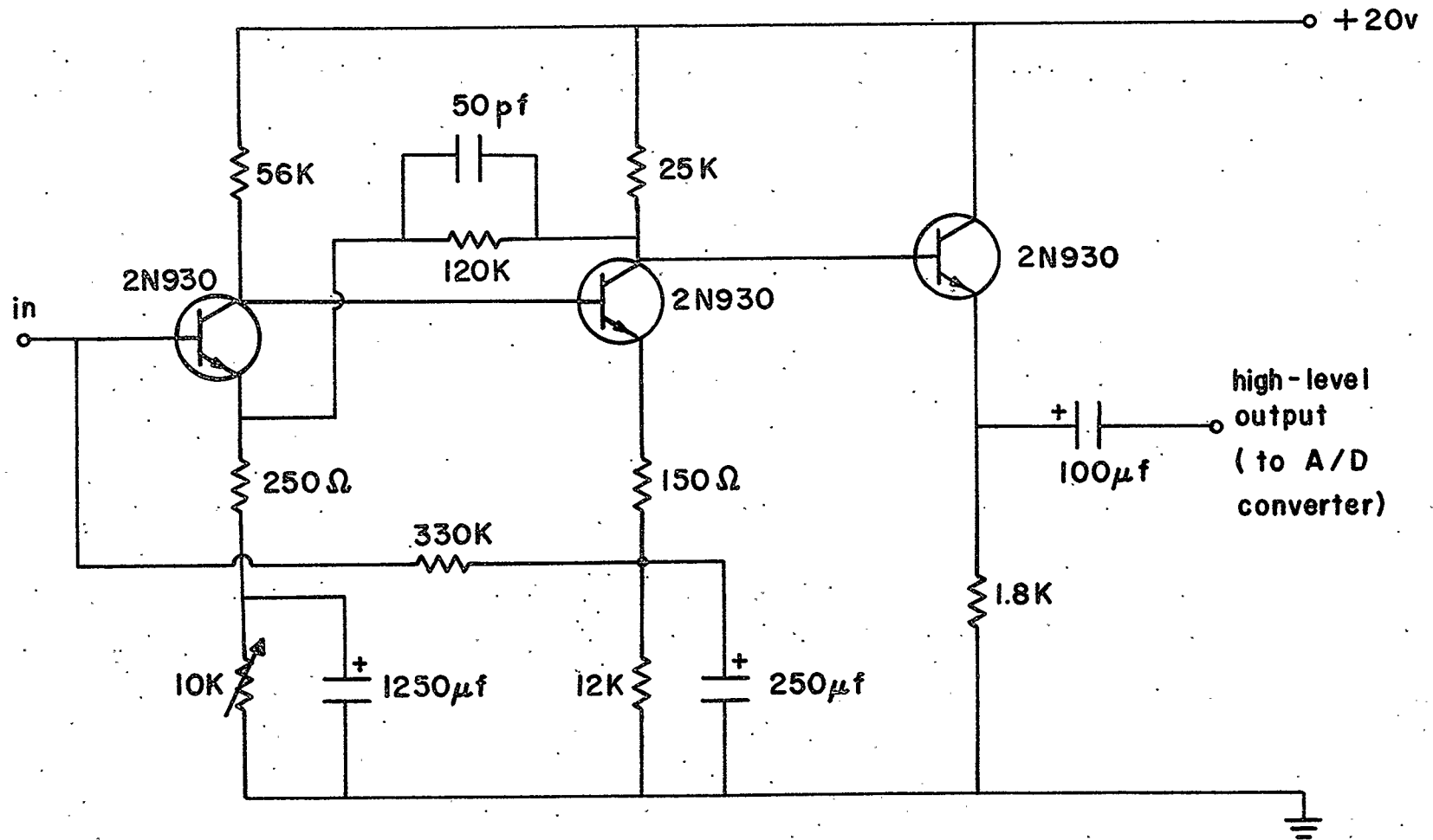


Fig. D.6 Amplifier used in conjunction with the preamplifier in Fig. D.5.

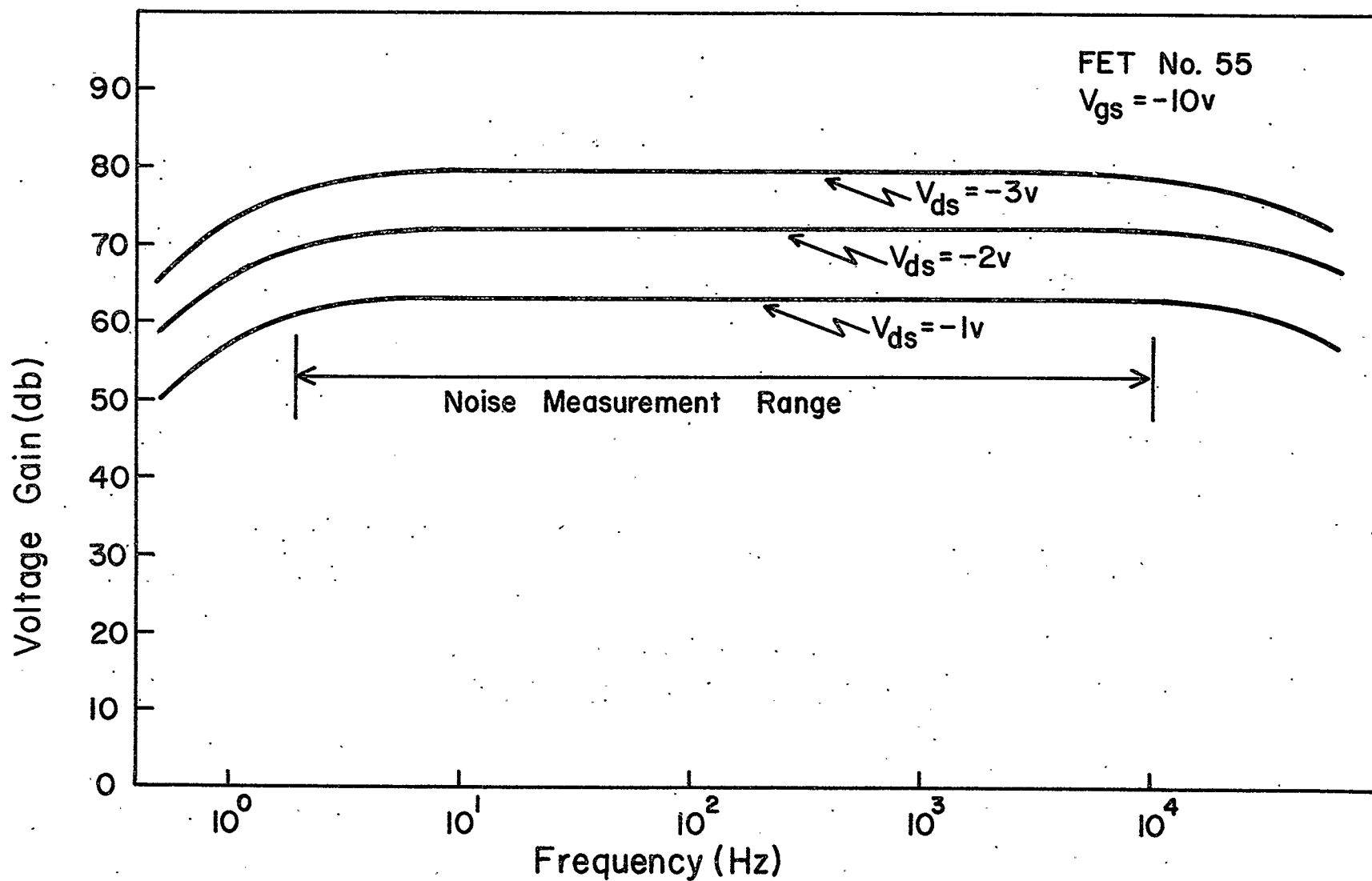


Fig. D.7 Typical gain characteristics of the combined amplifier system with the MOS FET in the pre pinch-off mode.

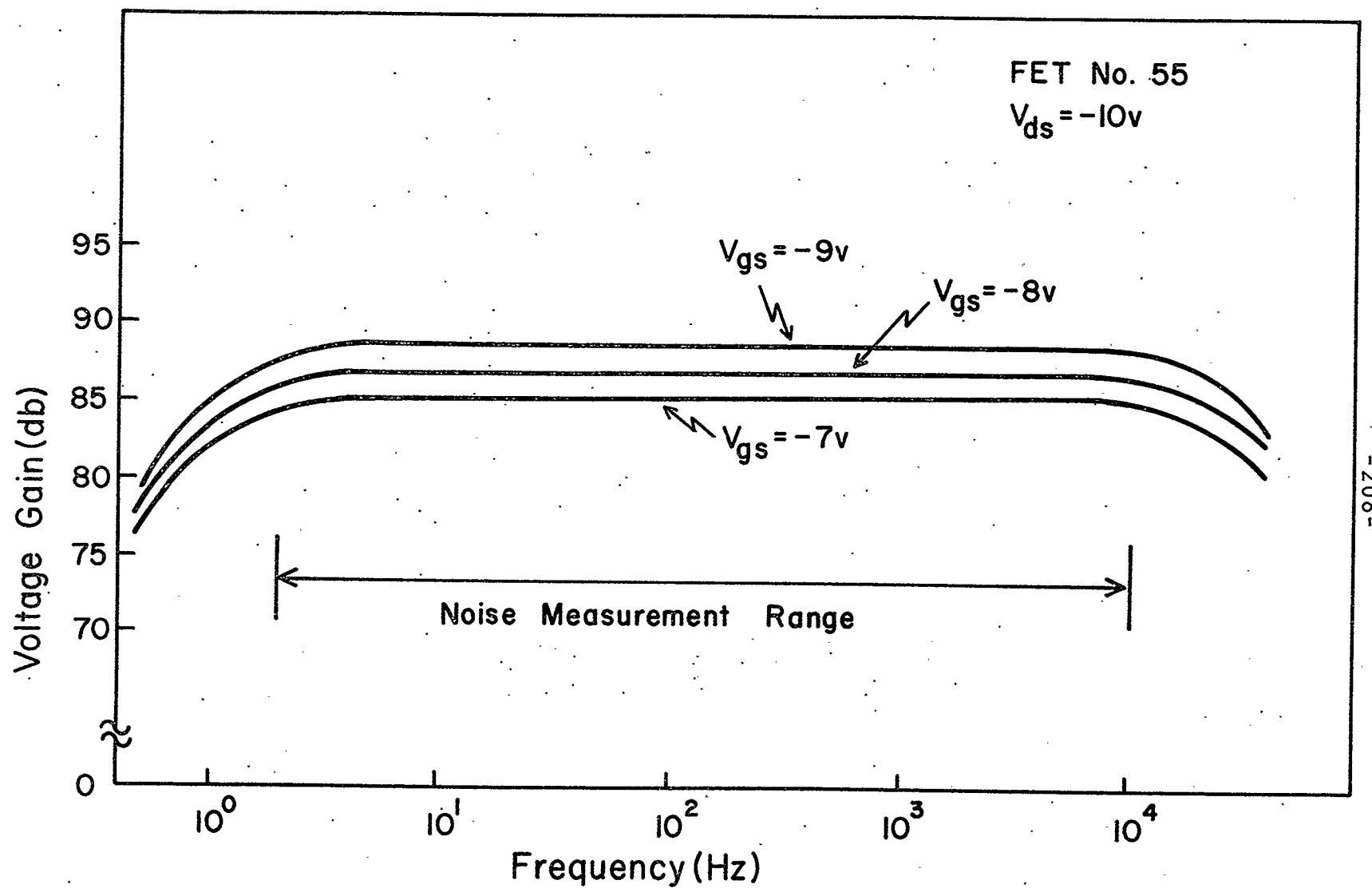


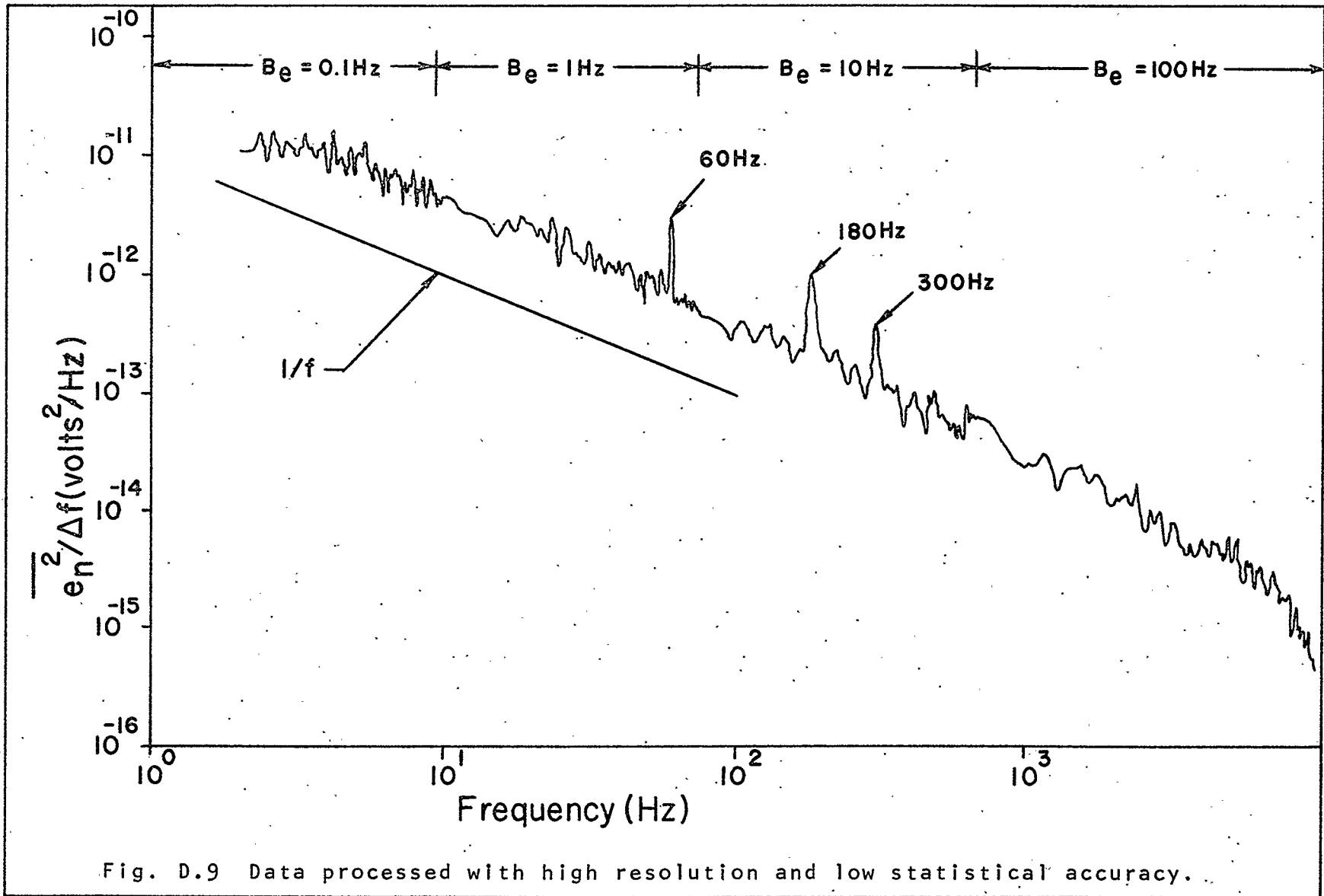
Fig. D.8 Typical gain characteristics of the combined amplifier system with the MOS FET pinched off.

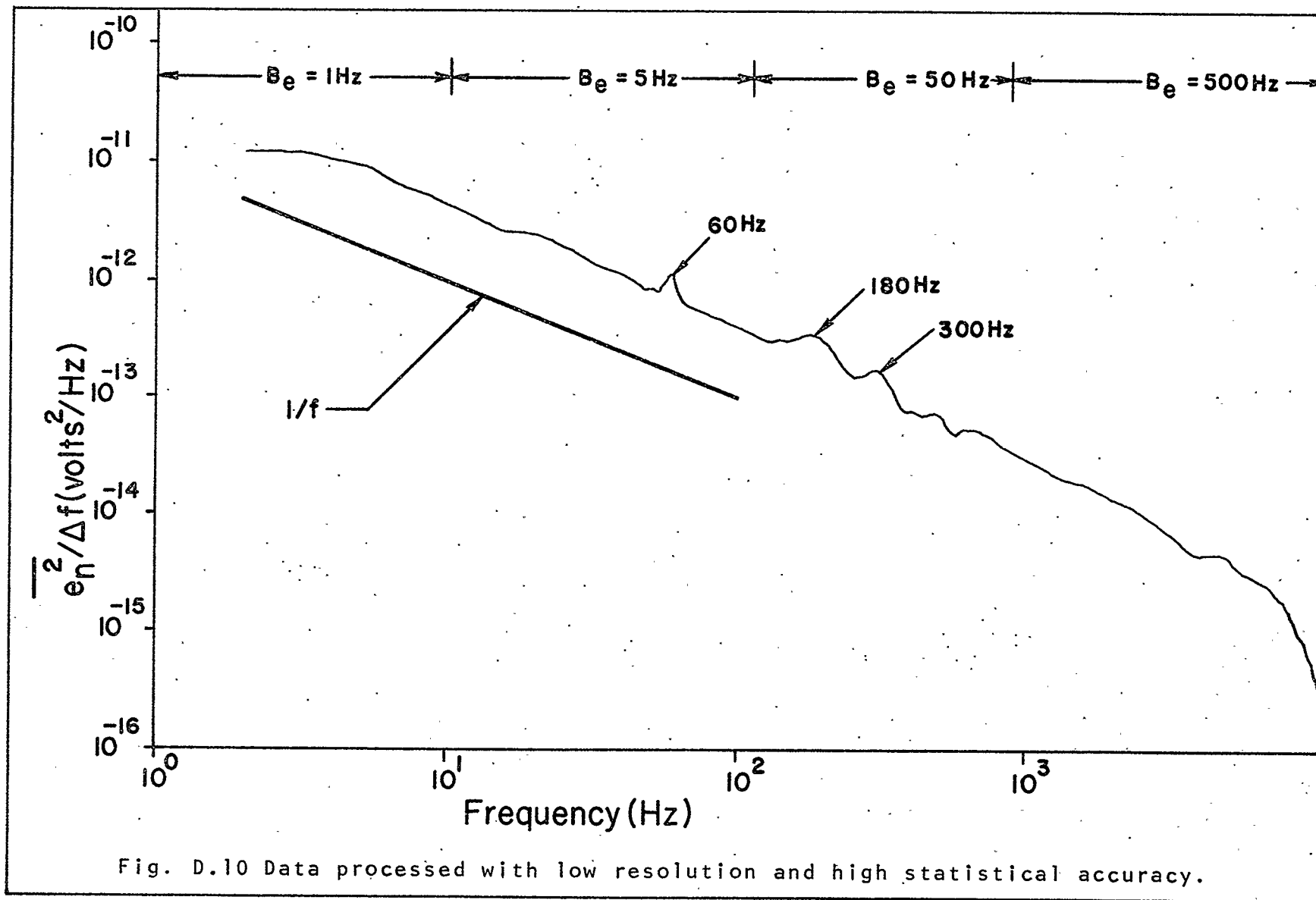
To obtain estimates of the power spectral density over the frequency range from 2Hz to 10kHz using a reasonable number of data points while retaining high resolution, the data for each frequency decade was processed separately. The number of samples and the statistical accuracy were held approximately constant while the resolution bandwidth B_e increased for each succeeding decade. Typical output spectra are given in Figs. D.9, D.10 and D.11 for the same data processed in three different fashions. Details pertaining to the data acquisition are given in Table D.1.

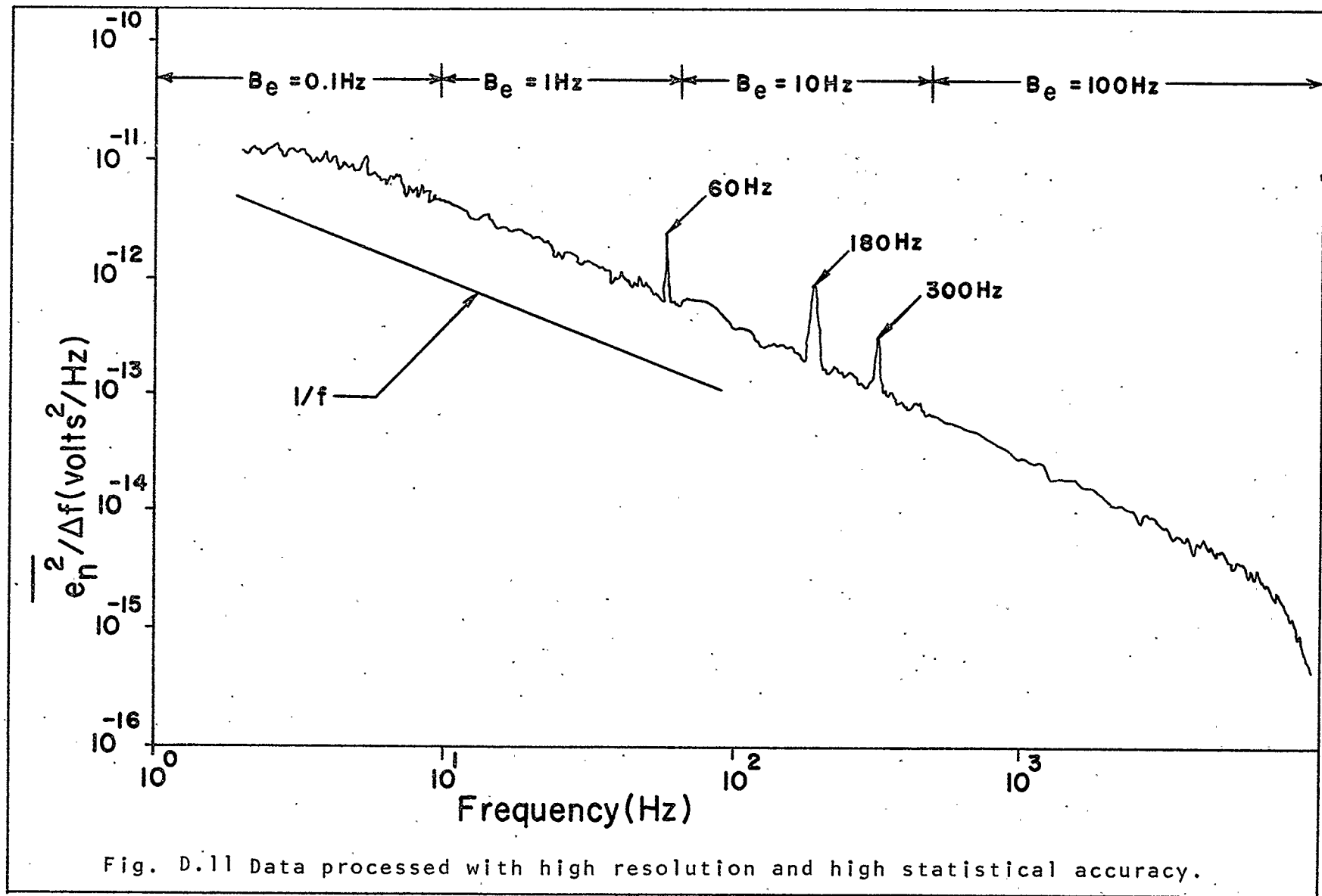
A comparison of Figs. D.10 and D.11 illustrates the 'smearing' that can take place if a periodic component is present and the bandwidth B_e is large. The periodic components show up in the data when processed with high resolution and accuracy, but the processing time increases formidably as shown in Table D.1. As a result, the data in Fig. D.10 was accepted as a compromise between record length, and resolution bandwidth. The usefulness of the measurement system is apparent from Table D.1. The total processing time for a spectral measurement from 2Hz to 10kHz is under seven minutes, while the same measurements using conventional filter techniques would have been much longer. In addition, the data is stored permanently on magnetic tape and may be reprocessed at any time to obtain spectra with different resolution, axis size and range for the same data. The entire statistical analysis program is compiled under 180K of core, to decrease turnaround time on the 360 system, and

Table D.1
Data Acquisition Parameters

Fig. No.	Frequency Range (Hz)	# of Data Points (N)	Sampling Frequency Hz	v	B_e (Hz)	Data Acquisition Time(sec)	Total Processing Time (min)
D.9	2-10	6000	40	30	0.1	150	16.68
	5-100	6000	300	40	1	20	
	50-10 ³	6000	3000	40	10	2	
	500-10 ⁴	6000	24000	50	100	0.25	
D.10	2-10	6000	40	300	1	150	6.77
	5-100	6000	300	200	5	20	
	50-10 ³	6000	3000	200	50	2	
	500-10 ⁴	6000	24000	250	500	0.25	
D.11	2-10	34000	40	170	0.1	850	93.1
	5-100	34000	300	227	1	113.3	
	50-10 ³	34000	3000	227	10	11.33	
	500-10 ⁴	34000	24000	284	100	1.42	







the technique is thus very useful for performing measurements of noise spectra on many devices in a short time.

A second method of processing the data is available using the Fast Fourier Transform Algorithm. This reduces processing time significantly, but does not allow the freedom in choosing ν , B_e , N and axis parameters that is obtained by the standard Blackman-Tukey procedure,⁹⁸ and as a result it was not used in this work.

D.2 THE ACCURACY OF THE MEASUREMENTS

It is always important to consider possible sources of error which may arise in noise measurement systems, since these errors are not always noticeable in the results.

The accuracy of the statistical analysis is determined by ν , which varied between 200 and 300 in this work. This means that the spectrum obtained will lie within 10% of the true spectrum more than 90% of the time, which is more than sufficient for observing overall level changes in the spectra with bias variations.

For low drain voltages and thus low first stage gain, a high noise contribution from the preamplifiers could artificially enhance the noise. To make sure that this was not the case, two different preamplifiers were built and tested. The noise contribution from the amplifiers at the output, measured with the input terminated in R_L , was found to be negligible in comparison with the noise from the MOS FET. Noise measurements using both amplifiers were found to be in

excellent agreement and were very repeatable, so that this source of noise was assumed to be negligible.

The final amplifiers used are shown in Figs. D.5 and D.6. It should be pointed out that at low drain voltages, the drain of the FET was coupled with back-to-back coupling capacitors and also direct coupled to the following stage. Again the results were in good agreement, which indicates that noise from the second stage is negligible. If this were not the case, the noise should have been smaller in the case of direct coupling, since the second stage current is decreased when the base voltage is low, and the noise is proportional to the collector current.

The final source of noise suspected of contributing at small drain voltages was thermal noise of the MOS FET. An examination of Fig. 4.8 indicates that the thermal noise increases significantly at small drain voltages. However, the level is orders of magnitude below the $1/f$ noise at audio frequencies. In addition, the thermal noise spectrum is flat so if the level was significant the overall spectrum would be expected to 'tilt' as the thermal noise contribution became more dominant. This was not observed.

It is concluded that the accuracy of the measurements is more than sufficient for the requirements of this work.

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