THE UNIVERSITY OF CALGARY

Capacitance-to-Frequency Converters

by

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled, "Capacitance-to-Frequency Converters" submitted by Jichang Qin in partial fulfillment of the requirements for the degree of Master of Science.

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ABSTRACT

Three capacitance-to-frequency conversion circuits for interfacing capacitive transducers with digital system are presented in this thesis. The free-running relaxation oscillator generates an output pulse train with a frequency which is dependent on the capacitor to be measured, one resistor and three resistance ratios. The R-pumped converter uses the switched capacitor concept to create a simulated resistor to manipulate charge. To maintain a charge balance this resistor must be switched at a suitable rate which is indicative of the measured capacitance. In the two-capacitor pumped converter, capacitor ratioing is used to compare the capacitor to be measured to a standard capacitor. A crystal clock controls the switching rate of the measured capacitor and the output frequency, which indicates the ratio of two capacitors, controls the switching of the standard capacitor. Detailed analysis of effects of nonidealities on the operation of these circuits is presented in this thesis. All of these circuits have been implemented and tested. The test results indicate that the stability of these circuits in terms of ppm standard deviation from average output frequency is less than 3.0 and that the measured temperature characteristics of these circuits match the theoretical characteristics very well. All of these circuits can be applied in high temperature environments such as oil and gas reservoirs.

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DEDICATION

To my wife Wan and my daughter Meng-meng,

my mother and father,

and all my brothers

for their love and encouragement

over the years.

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A_d	Operational Amplifier differential gain
$A_d(jf)$	Amplifier gain transfer function
A_{do}	Operational Amplifier dc gain
C	Capacitance
$CMRR$	Operational Amplifier common-mode rejection ratio
C_o	Gate oxide capacitance per unit area
C_s	Stray capacitance
f_o	Output frequency
f_{oa}	First-order frequency pole location
f_{max}	Maximum output frequency
f_{oideal}	Output frequency for ideal case
f_{max}	Maximum output frequency
$g(t)$	Interpolation function
$G(j\omega)$	Spectrum of interpolation function
I_b^+	Operational Amplifier positive input bias current

I_b^-	Operational Amplifier negative input bias current
I_D	Drain current of MOS transistor
I_G	Current source associated with MOS transistor in macromodel
q	Charge accumulated on the plates of capacitor
R	Resistance
r_d	Difference between high and low output resistance of logic gate
r_h	Output resistance of logic gate in high state
r_l	Output resistance of logic gate in low state
R_{on}	On-resistance of MOS switch
S_e	Noise voltage spectral density
S_i	Noise current spectral density
T	Temperature
T_o	Output period
T_{oideal}	Output period for ideal case
T_p	Circuit output pulse width
V_+	Non-inverting input voltage
V_{+r}	Ripple voltage at non-inverting input

V_-	Inverting input voltage
V_h	High threshold voltage of Schmitt trigger
V_l	Low threshold voltage of Schmitt trigger
V_{or}	Output ripple voltage
V_{os}	Operational amplifier offset voltage
V_{out}	Output voltage of the circuit
V_{ref}	Reference or supply voltage
V_t	VFC input voltage
V_T	Threshold voltage of MOS transistor
W / L	Ratio of channel width to channel length
$X(kT)$	Random sequence
$X(j\omega)$	Spectrum of random sequence X(kT)
ε	Error term
η	Ratio of threshold voltage to power-supply voltage
μ	Channel surface carrier mobility
Δq	Charge difference
ΔV	Voltage difference

$\Phi(jf)$	Angle phase of gain transfer function
γ	Resistance ratio

Chapter 1

Introduction

Capacitance-to-frequency conversion circuits which can convert a change in capacitance of a capacitive transducer to a variation in output frequency are important components of data acquisition and control systems. The reason is that capacitive transducers are widely used in automatic control of vehicles, robots and industrial processes for the purpose of measuring pressure, displacement, liquid level, flow rate, humidity and so on [1], [2], [3]. These transducers are usually located far away from central control units where microcomputers or microprocessors are used to accomplish linearization, compensation and calibration and are exposed to the noisy environments so that data transmission is easily disturbed by external electromagnetic interference. The best solution to overcome these problems is to convert the sensed variable directly into an equivalent digital number by means of built-in interface circuits at the transducer.

A number of different interface circuits can be used to realize capacitance-to-digital conversion [4], [5], [6]. The most common method used in these circuits is to generate a voltage proportional to the change of capacitance by using an integrator or a capacitance bridge, and then to convert this voltage into a binary output using an analog-to-digital converter. Although these circuits permit an accurate capacitance measurement, their main disadvantages include relatively large component count, relatively long conversion times and the requirement for a multi-phase clock.

The subject of this thesis involves the implementation of three capacitance-to-frequency conversion circuits. These circuits have a small component count, high stability and provision for single power supply operation. The first of these circuits described here is an RC free-running relaxation oscillator in which the frequency of oscillation is determined by the capacitor to be measured and circuit resistors. The circuit design is such that the output frequency is not appreciably affected by the input offset voltage and the input bias currents of the two operational amplifiers in the circuit. The disadvantage of this circuit is the requirement for five high precision and stable resistors. In addition, a very stable time base is also needed for the accurate measurement of output frequency.

The second of these circuits is an R-pumped capacitance-to-frequency converter. Actually, it is a switched capacitor charge pump circuit in which the capacitor to be measured is used to pump charge from a capacitive charge reservoir which is being replenished by current flow through a resistor. The rate at which the capacitor must be switched to maintain a charge balance is controlled and is indicative of the capacitor size. Compared with the RC free-running oscillator, an advantage of this circuit is that its stability is only dependent on one resistor instead of five resistors in the RC oscillator. However, the output frequency measurement of this circuit still requires a stable time base.

To eliminate the requirement of high precision resistors and a stable time base, a third conversion circuit has been developed. This circuit is a two-capacitor pumped switched capacitor capacitance-to-frequency converter which can be used to compare the capacitor to be measured to a standard capacitor. The basic circuit consists of the

capacitor to be measured, a standard capacitor, four MOS switches, a large capacitor which is used as a charge reservoir, an open-loop voltage amplifier and a voltage-to-frequency converter. The rate at which the measured capacitor is switched is controlled by a crystal clock and the rate at which the standard capacitor must be switched is controlled to indicate the ratio of the two capacitors. If the same clock is used to measure the output frequency, the system will be independent of the clock frequency. Therefore, the problems encountered in the RC free-running oscillator and R-pumped converter are completely overcome in this circuit. Furthermore, the basic circuit can be modified by adding a second standard capacitor and another two MOS switches to offset the value of the capacitor to be measured in order to enhance capacitance changes.

This thesis is divided into chapters as follows. The basic circuit configuration and the operation of the RC-free running oscillator are described in chapter 2. An analysis of the effects of circuit nonidealities on the output frequency is presented. Several modifications of the basic circuits are addressed and some practical applications are suggested. Measurements on an implementation of the basic circuit are also presented in this chapter.

Chapter 3 deals with the operation of the basic R-pumped conversion circuit and concentrates on a detailed analysis of the effects of a number of circuit nonidealities such as the size of capacitor used as charge reservoir, the frequency-dependence of the gain of the amplifier, the on-resistance of switches, etc., on the output frequency of this circuit. Results of tests of the stability and temperature characteristics of this circuit are also included in this chapter.

A technique which can be used to eliminate the effect of the input offset voltage of the open-loop amplifier on the output frequency in the conversion circuit by interchanging the position of the ordinary resistor and the switched capacitor simulated resistor is investigated in chapter 4.

In chapter 5, the concept of using capacitance ratioing, i.e., comparing the measured capacitor to a standard capacitor, and its application in the two-capacitor pumped conversion circuit are examined. A modification of the basic circuit is presented. Test results for the basic circuit are also included in this chapter.

In practical applications, noise is a primary concern. In chapter 6, the use of SPICE simulation to evaluate the noise characteristics of these circuits is described. The approach of using a macromodel of the operational amplifier to improve the simulation speed and to reduce the circuit complexity is presented along with the generation of a white noise voltage by means of a SPICE piecewise linear source function. Finally, some simulation results are presented.

Chapter 7 is the summary of the work. Some recommendations for further studies relating to the circuits described in this thesis are presented.

Chapter 2

The Resistance-Capacitance Free-Running Relaxation Oscillator

2.1 Introduction

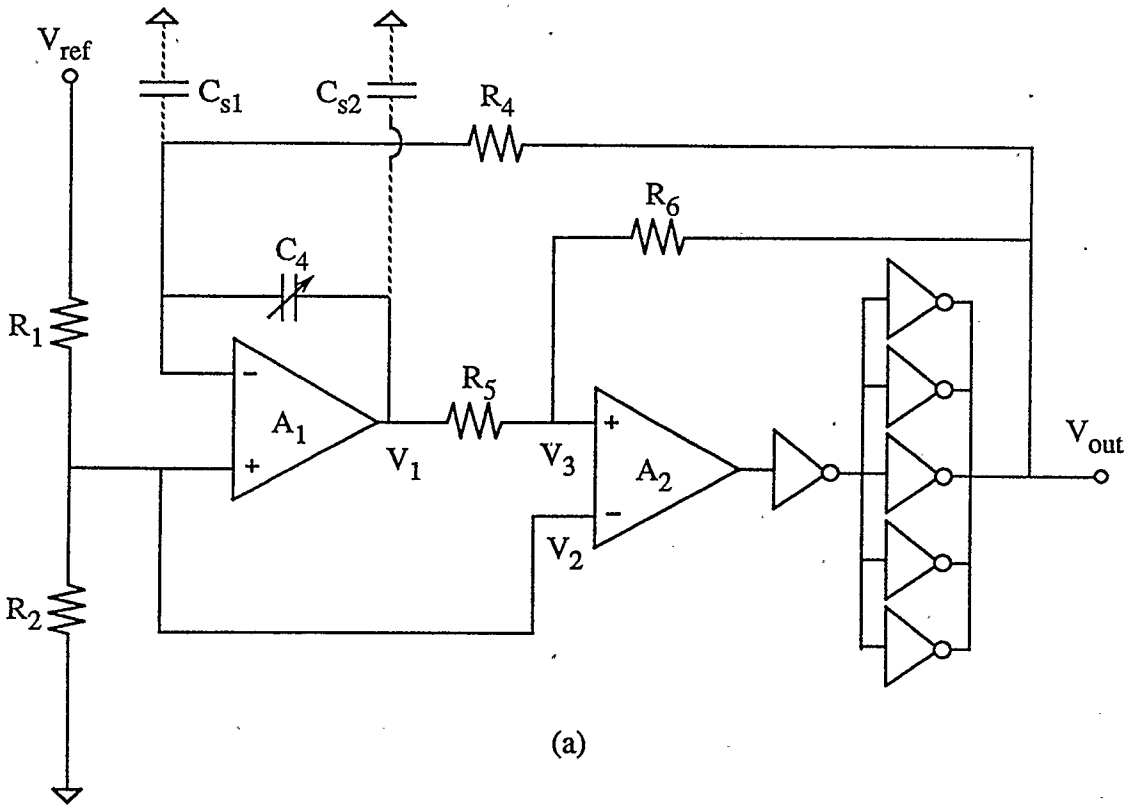
A resistance-capacitance free-running relaxation oscillator (RC oscillator) whose oscillation frequency is determined by the capacitance of a capacitive transducer and is not effected by the plate-to-ground stray capacitances is useful in the area of instrumentation and measurement. The RC oscillator described in this chapter utilizes the well known charge balance principle [7] and can generate a square-wave output with a frequency which is dependent on the measured capacitance C_4, a resistor R_4 and on two other resistance ratios. The basic oscillator circuit consists of an integrator and a non-inverting Schmitt trigger. Basically, it is a capacitance-to-frequency converter, but a small modification of the basic circuit can produce a voltage-to-frequency conversion circuit. The circuit design scheme is such that the output frequency is not appreciably affected by the input offset voltage and the input bias currents of the two operational amplifiers in the circuit. An analysis of the effects of component nonidealities on the oscillation frequency is presented and a practical implementation example is introduced to show how a large value equivalent charging-discharging resistance can be obtained by modification of the basic circuit.

2.2 Basic RC Oscillator

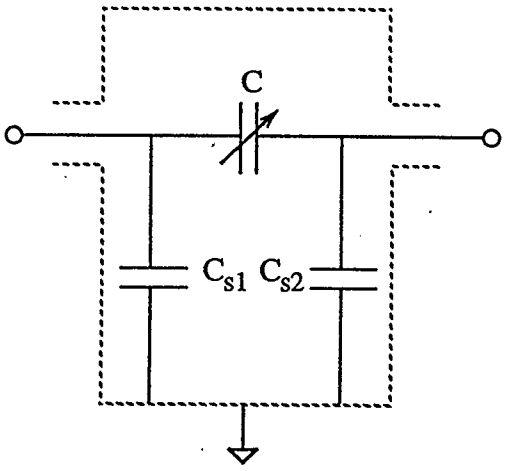
A simple low parts count RC relaxation oscillator circuit can be constructed as shown in Fig. 2.1(a) to produce the waveforms given in Fig. 2.2. It consists of an integrator formed by operational amplifier A_1, resistor R_4 and capacitor C_4 which is the capacitor under measurement, and a non-inverting Schmitt trigger formed by operational amplifier A_2, two resistors R_5 and R_6 and six inverters. The transfer characteristics of the Schmitt trigger is shown in Fig. 2.3. The lower-threshold voltage V_l and upper-threshold voltage V_h are voltage levels at which the Schmitt trigger changes state. In this oscillator circuit, the two operational amplifiers and six inverters are all powered from a single reference voltage V_{ref}. The purpose of using six inverters here is to ensure that resistor R_4 is large in comparison to the output resistance of inverters, so that the output high is equal to V_{ref} and output low is equal to zero.

The operation of this circuit can be described as follows. When V_{out}, the output of the circuit, is high, capacitor C_4 will be charged by the current through resistor R_4, causing V_1, the output of integrator A_1, to ramp down until it drops just below the lower-threshold voltage V_l of the Schmitt trigger. Then V_{out} will go low causing capacitor C_4 to discharge and V_1 to ramp up towards V_{ref}. When V_1 reaches the upper-threshold voltage V_h, V_{out} will return to the high state, and the cycle will repeat itself. The lower-threshold voltage V_l and upper-threshold voltage V_h of the Schmitt trigger can be expressed as follows

$$V_l = (1 + \frac{R_5}{R_6})(\frac{R_2}{R_1 + R_2} - \frac{R_5}{R_5 + R_6})\, V_{ref} \qquad (2.1)$$



(a)



(b)

Fig. 2.1 (a) Schematic of the basic RC oscillator with three-terminal capacitor (b) Typical three-terminal capacitor with a grounded shield and plate-to-ground stray capacitances C_{s1} and C_{s2}

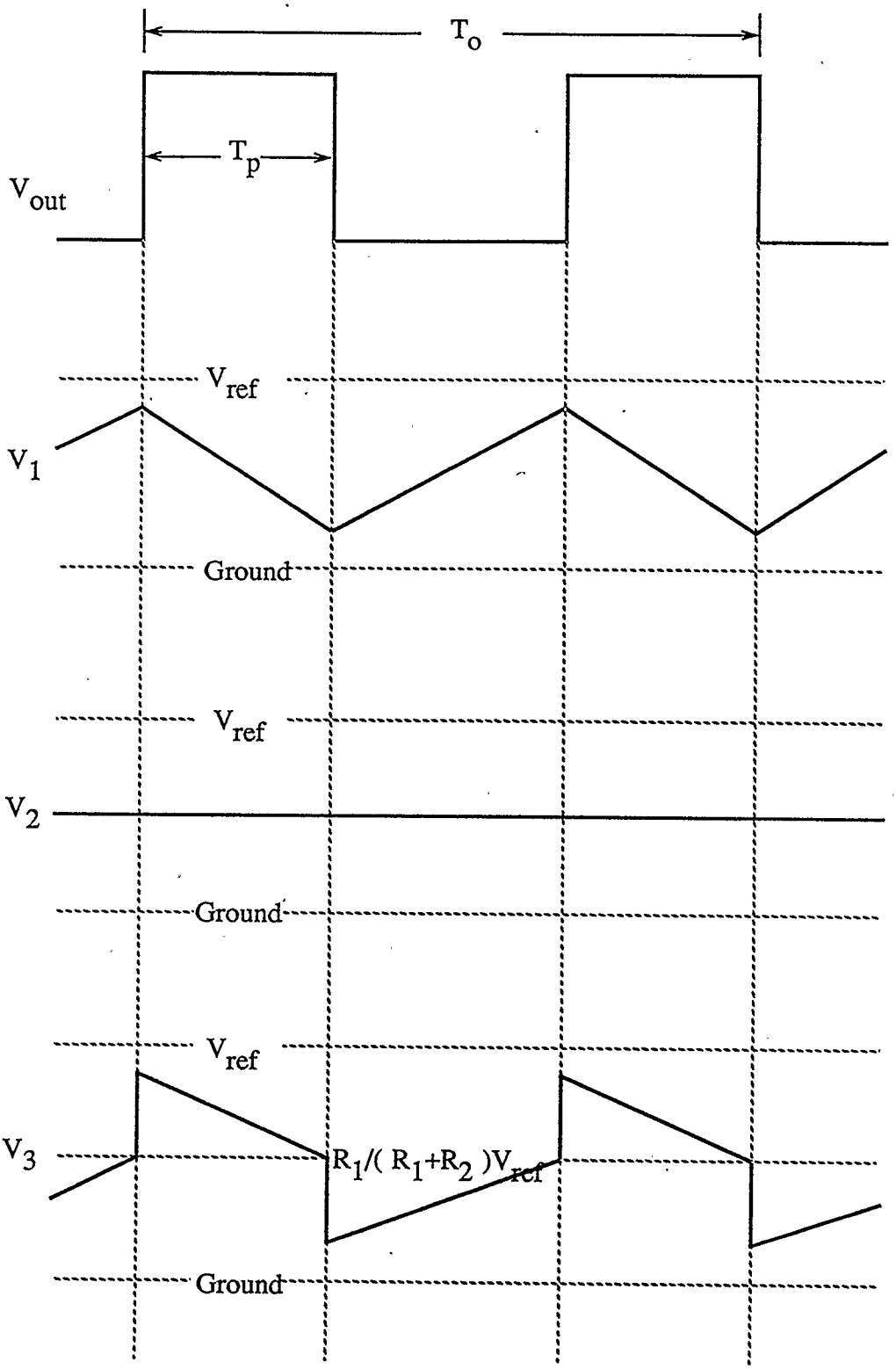


Fig.2.2 Voltage waveforms of the RC oscillator

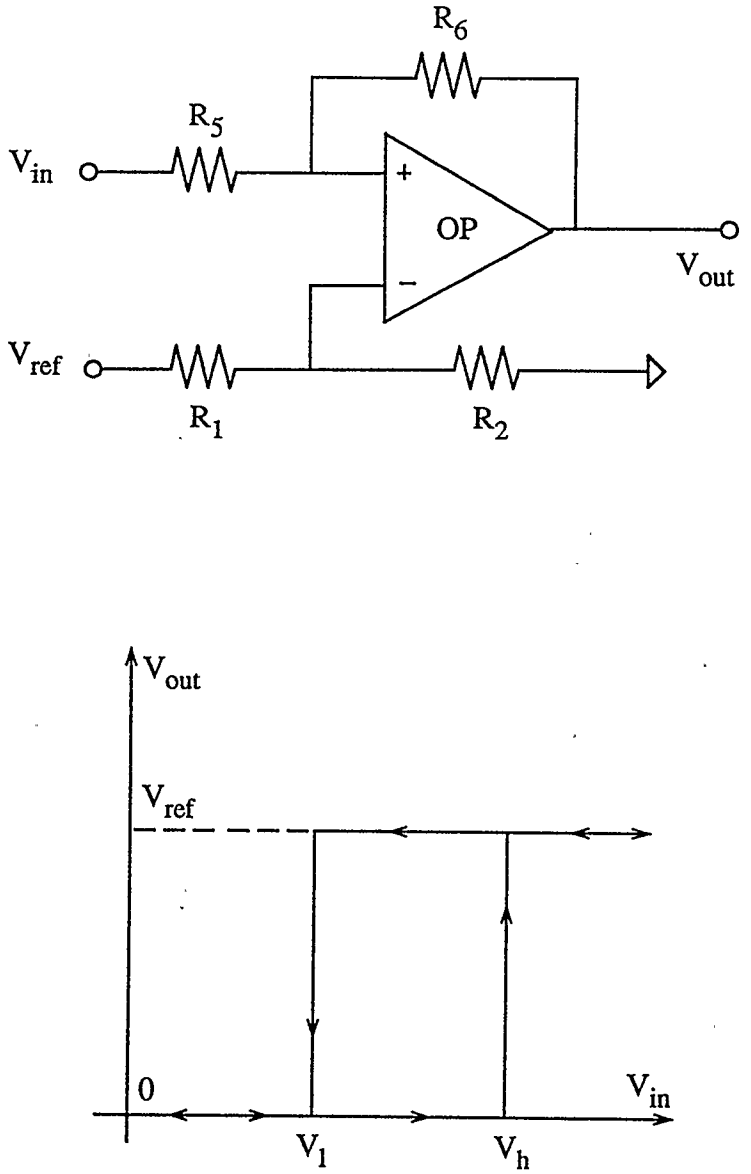


Fig.2.3 Schmitt trigger and its transfer characteristic

$$V_h = (1 + \frac{R_5}{R_6}) \frac{R_2}{R_1 + R_2} V_{ref} \tag{2.2}$$

If the period of oscillation is T_o and the time interval for which V_{out} is high is T_p, a charge balance equation for capacitor C_4 can be written as follows

$$\frac{V_{ref}}{R_4} T_p - \frac{V_{ref} R_2}{R_1 + R_2} \frac{1}{R_4} T_o = 0 \tag{2.3}$$

so that

$$T_p = \frac{R_2}{R_1 + R_2} T_o . \tag{2.4}$$

Eq. (2.4) can be re-arranged to give

$$\frac{T_p}{T_o} = \frac{R_2}{R_1 + R_2}, \tag{2.5}$$

i.e., the pulse width-to-period ratio is dependent only on the ratio of R_1 to R_2 and is independent of the other circuit components. T_p can be calculated by noting that during the time T_p capacitor C_4 charges at a rate of I/C_4 and that the charging current I can be determined from

$$I = \frac{V_{ref}}{R_4} (1 - \frac{R_2}{R_1 + R_2}). \tag{2.6}$$

Thus,

$$T_p = \frac{V_h - V_l}{V_{ref} (1 - \frac{R_2}{R_1 + R_2})} R_4 C_4 \tag{2.7}$$

and

$$T_o = \frac{R_4 C_4}{\frac{R_1}{R_1+R_2}(1-\frac{R_1}{R_1+R_2})\frac{R_6}{R_5}} \tag{2.8}$$

so that the output frequency f_o, which is the reciprocal of the period T_o, can be obtained from

$$f_o = \frac{1}{R_4 C_4}\frac{R_1}{R_1+R_2}(1-\frac{R_1}{R_1+R_2})\frac{R_6}{R_5}. \tag{2.9}$$

It is seen from Eq. (2.9) that the output oscillation frequency of this circuit is inversely proportional to the capacitance C_4 and resistance R_4 and is dependent on the two resistance ratios R_1/R_2 and R_5/R_6.

In some practical applications, the outputs of the capacitive transducers are connected to the RC oscillator circuit by a length of cable with a grounded shield. In this situation, the capacitance to be measured is a typical three-terminal capacitor with two plate-to-ground stray capacitances C_{s1} and C_{s2} as shown in Fig.2.1(b). The effects of the stray capacitances C_{s1} and C_{s2} on the output frequency can be analyzed by using the charge balance concept. It is noted that the stray capacitance C_{s1}, which is associated with one plate of capacitor C_4, is charged to $V_{ref}\, R_2/(R_1+R_2)$ and then fixed at that value, and the stray capacitance C_{s2}, which is associated with the other plate of C_4 is charged to V_h and then discharged to V_l once every cycle. Since there is no charge loss as far as the charge balance for C_4 is concerned , the effects of these stray capacitances on the output frequency can be completely ignored.

2.3 Modification of Basic RC Oscillator

A second charging-discharging resistor, R_7, can be incorporated into the basic oscillator circuit as shown in Fig. 2.4 for the purpose of obtaining a large effective value of charging-discharging resistance for capacitor C_4. The reason for doing so is that large valued precision resistors are not readily available. In the circuit of Fig. 2.4, R_4 and R_7 are two ratioed resistors and the numbers of parallel inverters in the branch consisting of R_4 and in the new added branch are also ratioed so that the two combined output resistances of inverters can have the same ratio as R_4 and R_7. For example, if R_4 is equal to 2R and R_7 is equal to 3R, the ratio $\gamma=R_7/R_4$ is equal to 3/2. To maintain the same ratio, the number of parallel inverters connected in the branch consisting of R_4 has to be three and the number in the branch consisting of R_7 has to be two.

The charge balance equation for capacitor C_4 can be written as

$$\frac{V_{ref}}{R_4}T_p-\frac{V_{ref}R_2}{R_1+R_2}\frac{T_o}{R_4}-\frac{V_{ref}R_2}{R_1+R_2}\frac{T_p}{\gamma R_4}+\frac{V_{ref}R_1}{(R_1+R_2)\gamma R_4}(T_o-T_p)=0 \quad (2.10)$$

assuming that $R_7=\gamma R_4$ and that the combined output resistances are small in comparison to R_4 and R_7. Then

$$\frac{T_p}{T_o}=\frac{R_2}{R_1+R_2}\left[\frac{1-\frac{R_1}{R_2}\frac{1}{\gamma}}{1-\frac{1}{\gamma}}\right]. \quad (2.11)$$

The output frequency f_o can be calculated by noting that during the time T_p

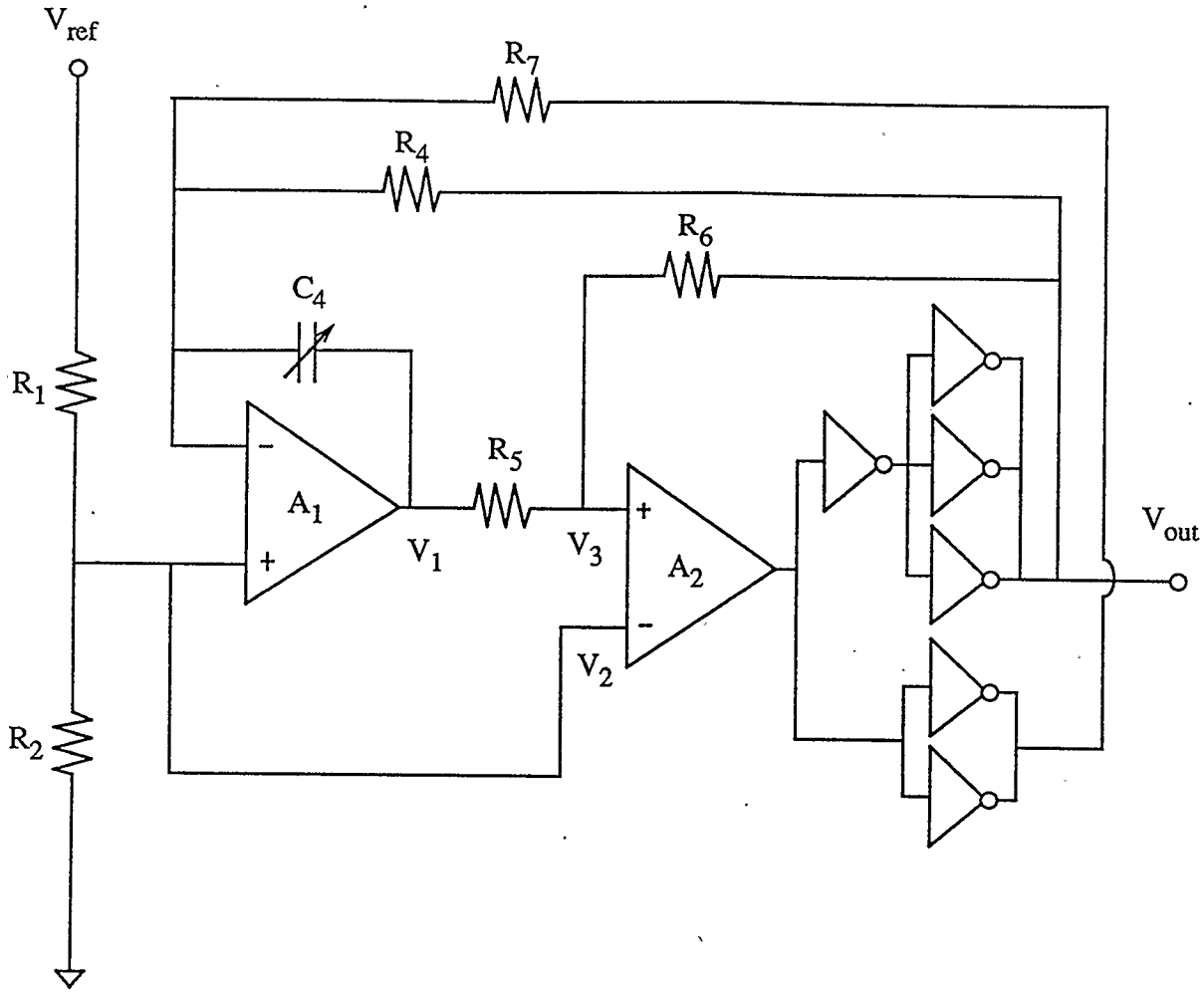


Fig.2.4 Schematic of RC oscillator with two ratioed charging-discharging resistors

$$\left[\frac{V_{ref}-V_{ref}\dfrac{R_2}{R_1+R_2}}{R_4}-\frac{V_{ref}\dfrac{R_2}{R_1+R_2}}{\gamma R_4}\right]\frac{T_p}{C_4}=V_h-V_l \tag{2.12}$$

and

$$T_p=\frac{C_4R_4\dfrac{R_5}{R_6}}{\dfrac{R_1}{R_1+R_2}(1-\dfrac{1}{\gamma}\dfrac{R_2}{R_1})}. \tag{2.13}$$

Thus,

$$T_o=\frac{R_4C_4}{\dfrac{R_1}{R_1+R_2}(1-\dfrac{R_1}{R_1+R_2})\dfrac{R_6}{R_5}}\left[\frac{1-\dfrac{1}{\gamma}}{(1-\dfrac{1}{\gamma}\dfrac{R_2}{R_1})(1-\dfrac{R_1}{R_2}\dfrac{1}{\gamma})}\right]. \tag{2.14}$$

The effective charging-discharging resistance R_4' is

$$R_4'=R_4\left[\frac{1-\dfrac{1}{\gamma}}{(1-\dfrac{1}{\gamma}\dfrac{R_2}{R_1})(1-\dfrac{R_1}{R_2}\dfrac{1}{\gamma})}\right]. \tag{2.15}$$

For example, if $\gamma=3/2$ and $R_1=R_2$, then R_4' is equal to $3R_4$, i.e., the effective charging-discharging resistance for capacitance C_4 is three times larger than the original R_4.

2.4 Voltage-to-Frequency Conversion

The basic RC oscillator can be changed into a voltage-to-frequency converter by disconnecting the non-inverting terminal input of operational amplifier A_1 from the voltage divider R_1 and R_2 and connecting it to the input voltage V_t as shown in Fig.

2.5. All of the circuit components are also powered by a single supply V_{ref} so that V_{out} high is equal to V_{ref} and V_{out} low is zero, assuming that the resistance R_4 is much larger than the combined output resistance of inverters. The output of integrator A_1 is constrained to move from the lower-threshold voltage V_l to the upper-threshold voltage V_h given by Eq. (2.1) and Eq. (2.2) during one period of oscillation. As described for the case of the basic RC oscillator circuit, a charge balance for integrating capacitor C_4, a fixed capacitor in this case, can be written as

$$\frac{V_{ref}}{R_4} T_p - \frac{V_t}{R_4} T_o = 0 \tag{2.16}$$

so that

$$\frac{T_p}{T_o} = \frac{V_t}{V_{ref}}, \tag{2.17}$$

Thus, to first order, the pulse-width to period ratio or duty cycle is directly proportional to the ratio of the input voltage to the reference voltage and is independent of all circuit components.

Now,

$$\frac{V_{ref} - V_t}{R_4 C_4} T_p = V_h - V_l \tag{2.18}$$

where $V_h - V_l = \frac{R_5}{R_6} V_{ref}$, and the output frequency is

$$f_o = \frac{\frac{V_t}{V_{ref}}(1 - \frac{V_t}{V_{ref}})}{R_4 C_4} \frac{R_6}{R_5}. \tag{2.19}$$

The output frequency f_o increases from zero for V_t being equal to zero to $f_{\max}$ when

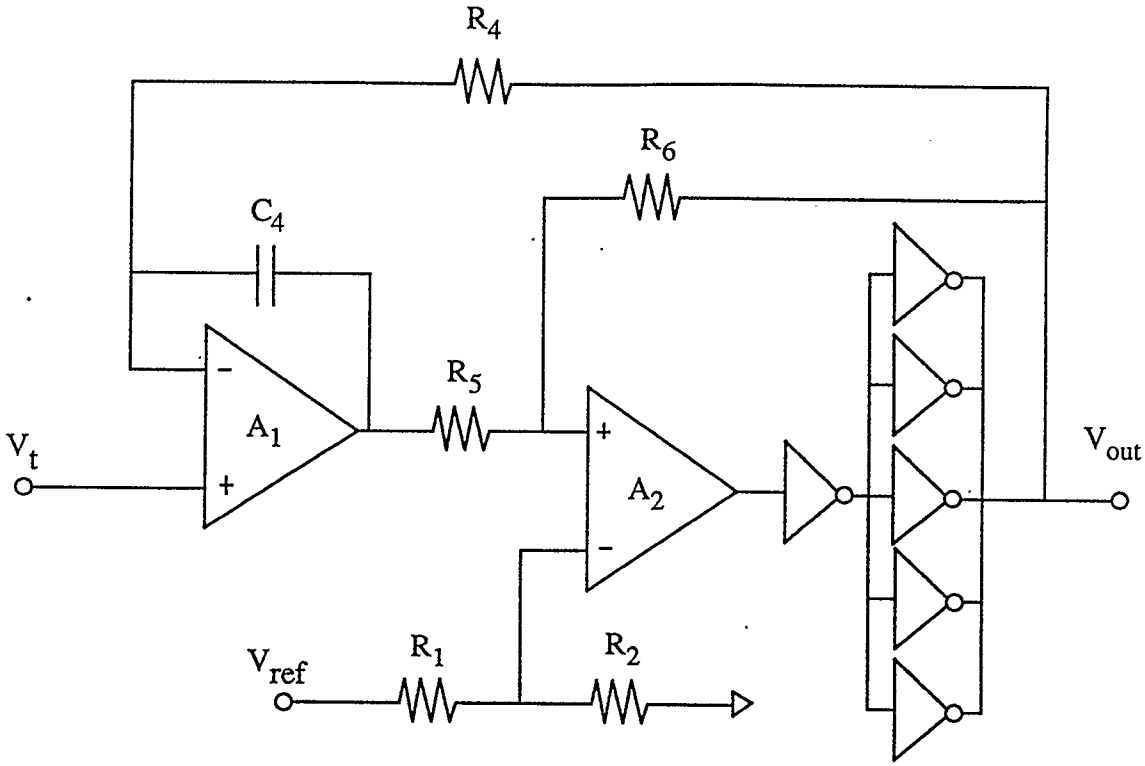


Fig. 2.5 Schematic of VFC

V_t is equal to $\frac{1}{2}V_{ref}$ and then decreases to zero as V_t changes from $\frac{1}{2}V_{ref}$ to zero. The maximum oscillation frequency is

$$f_{\max} = \frac{1}{4R_4C_4}\frac{R_6}{R_5} \tag{2.20}$$

2.5 VFC with Gain and Linearization

Voltage gain can be easily provided by connecting a resistor R_1' between the inverting input terminal of operational amplifier A_1 and ground as shown in Fig. 2.6(a). The charge balance for C_4 can then be rewritten as

$$\frac{V_{ref}}{R_4}T_p - \frac{V_t}{R_4}T_o - \frac{V_t}{R_1'}T_o = 0 \tag{2.21}$$

so that

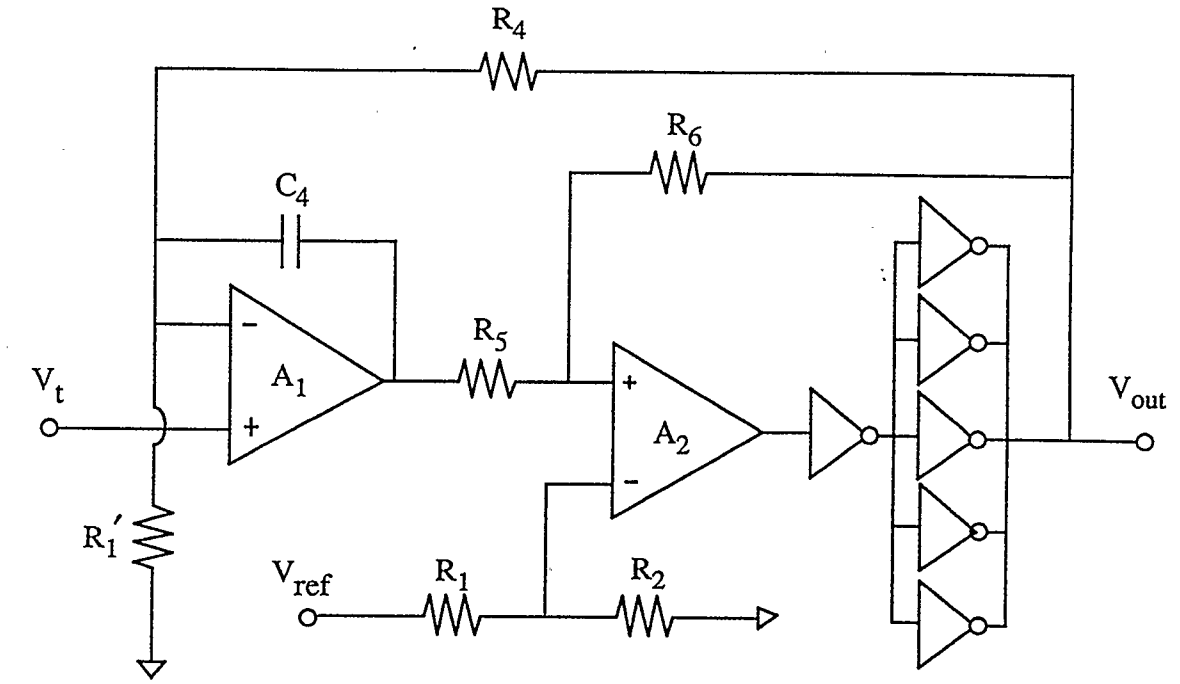
$$\frac{T_p}{T_o} = \frac{V_t}{V_{ref}}\left[1 + \frac{R_4}{R_1'}\right] \tag{2.22}$$

and

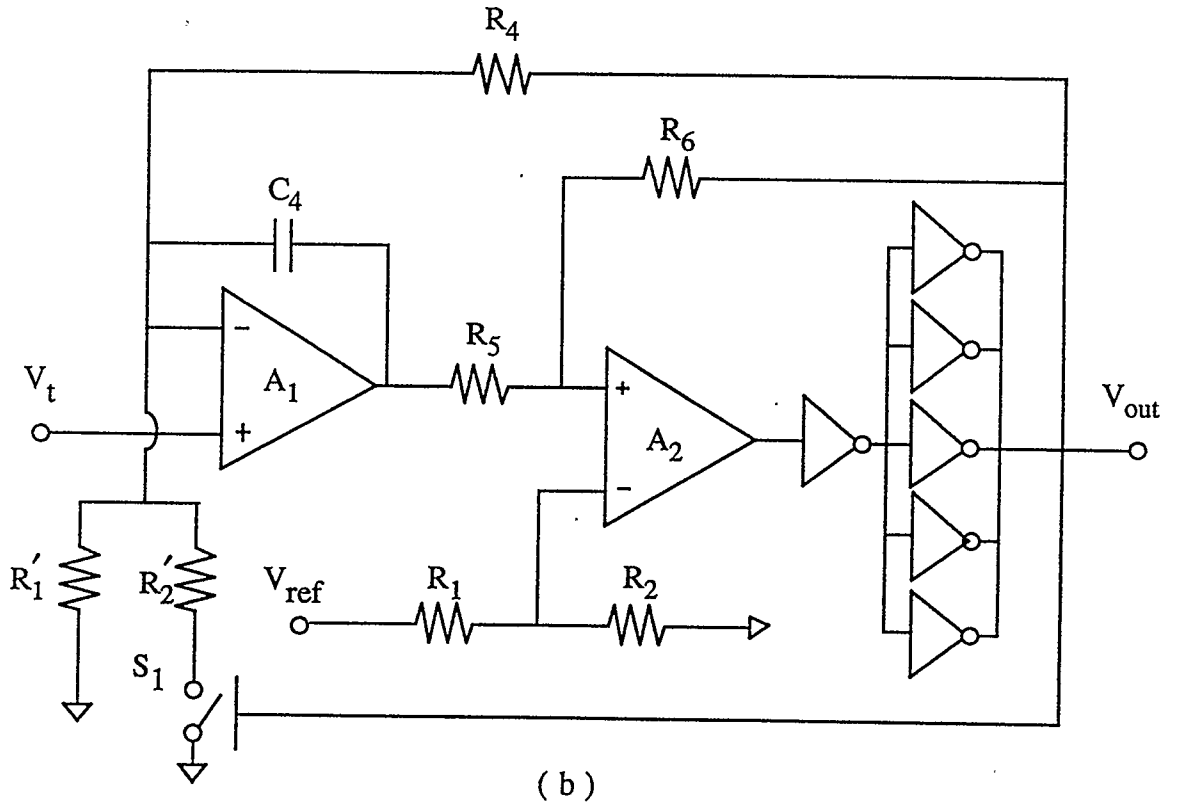
$$f_o = \frac{\frac{V_t}{V_{ref}}(1+\frac{R_4}{R_1'})\left[1 - \frac{V_t}{V_{ref}}(1+\frac{R_4}{R_1'})\right]}{R_4C_4}\frac{R_6}{R_5}. \tag{2.23}$$

Gain can thus be provided at the expense of making f_o dependent on the resistance ratio $\frac{R_4}{R_1'}$.

In practical applications, the input voltage to the VFC might be from a transducer and V_t may be a nonlinear function of the sensed variable. For example, the voltage-



(a)



(b)

Fig.2.6 (a) VFC with gain (b) VFC with gain and linearization

temperature characteristic for an ice-point referenced copper-constantan thermocouple is in the form of

$$\frac{V_t}{V_{ref}} = \frac{a\,t}{1 + b\,t} \tag{2.24}$$

where a and b are constants [8]. In such cases, the VFC can be modified to give a direct indication of V_t as shown in Fig. 2.6(b), where a second resistor R_2' in series with a switch S_1 is connected between the inverting input terminal of operational amplifier A_1 and ground, and the switching is controlled by the output V_{out}. If the switch S_1 is closed when V_{out} is high and left open otherwise, the charge balance for C_4 can be rewritten as

$$\frac{V_{ref}}{R_4} T_p - \frac{V_t}{R_4} T_o - \frac{V_t}{R_1'} T_o - \frac{V_t}{R_2'} T_p = 0 \tag{2.25}$$

so that

$$\frac{T_p}{T_o} = \frac{\dfrac{V_t}{V_{ref}} \left(1 + \dfrac{R_4}{R_1'}\right)}{1 - \dfrac{R_4}{R_2'} \dfrac{V_t}{V_{ref}}}. \tag{2.26}$$

During the time T_p,

$$\left[\frac{V_{ref} - V_t}{R_4 C_4} - \frac{V_t}{R_1' C_4} - \frac{V_t}{R_2' C_4} \right] = V_h - V_l \tag{2.27}$$

so that

$$f_o = \frac{\frac{V_t}{V_{ref}} \frac{R_6}{R_5} (1 + \frac{R_4}{R_1'}) \left[1 - \frac{V_t}{V_{ref}} (1 + \frac{R_4}{R_1'} + \frac{R_4}{R_2'}) \right]}{R_4 C_4 \left[1 - \frac{R_4}{R_2'} \frac{V_t}{V_{ref}} \right]}. \tag{2.28}$$

Alternatively, if the switch S_1 is closed when V_{out} is low and left open otherwise, a charge balance analysis similar to the one presented above yields

$$\frac{T_p}{T_o} = \frac{\frac{V_t}{V_{ref}} (1 + \frac{R_4}{R_1'} + \frac{R_4}{R_2'})}{1 + \frac{R_4}{R_2'} \frac{V_t}{V_{ref}}} \tag{2.29}$$

and

$$f_o = \frac{\frac{V_t}{V_{ref}} \frac{R_6}{R_5} (1 + \frac{R_4}{R_1'} + \frac{R_4}{R_2'}) \left[1 - \frac{V_t}{V_{ref}} (1 + \frac{R_4}{R_1'}) \right]}{R_4 C_4 \left[1 + \frac{R_4}{R_2'} \frac{V_t}{V_{ref}} \right]}. \tag{2.30}$$

If, for example, a and b are both positive, and the switch is in place when V_{out} is high, Eq.(2.26) becomes

$$\frac{T_p}{T_o} = a\, t\, (1 + \frac{R_4}{R_1'}) \tag{2.31}$$

where $\frac{R_4}{R_2'} = \frac{b}{a}$. Similarly, if a is positive while b is negative, and the switch is in place when V_{out} is low, Eq.(2.29) becomes

$$\frac{T_p}{T_o} = a\,t\,(1 + \frac{R_4}{R_1'} + \frac{R_4}{R_2'}) \tag{2.32}$$

In either case, linearization is achieved.

2.6 Nonidealities

Errors are introduced when the circuit is implemented because of component nonidealities. Referring to Fig. 2.7, the two operational amplifiers A_1 and A_2 have input offset voltages V_{os} and input bias currents I_b^+, I_b^-. The common mode rejection ratio (CMRR) of these two amplifiers is not infinite, and the inverters used to drive the integrator A_1 have non-zero output resistances. When these nonidealities are considered, the lower-threshold voltage V_l and upper-threshold voltage V_h of comparator A_2 are given by

$$V_l = (1+\frac{R_5}{R_6})[V_{t2}' - \frac{V_{ref}R_5}{R_5+R_6} + \frac{I_{b2}^+ R_5 R_6}{R_5+R_6} - \frac{R_1 R_2}{R_1+R_2}(I_{b1}^+ + I_{b2}^-)] \tag{2.33}$$

and

$$V_h = (1+\frac{R_5}{R_6})[V_{t2}' + \frac{I_{b2}^+ R_5 R_6}{R_5+R_6} - \frac{R_1 R_2}{R_1+R_2}(I_{b1}^+ + I_{b2}^-)] \tag{2.34}$$

where $V_{t2}' = V_{ref}\,\dfrac{R_2}{R_1+R_2} - \dfrac{\dfrac{V_{ref}}{2} - \dfrac{V_{ref}R_2}{R_1+R_2}}{CMRR_2} - V_{os2}$

V_{os2} = the input offset voltage of operational amplifier A_2

$CMRR_2$ = the common mode rejection ratio of operational amplifier A_2

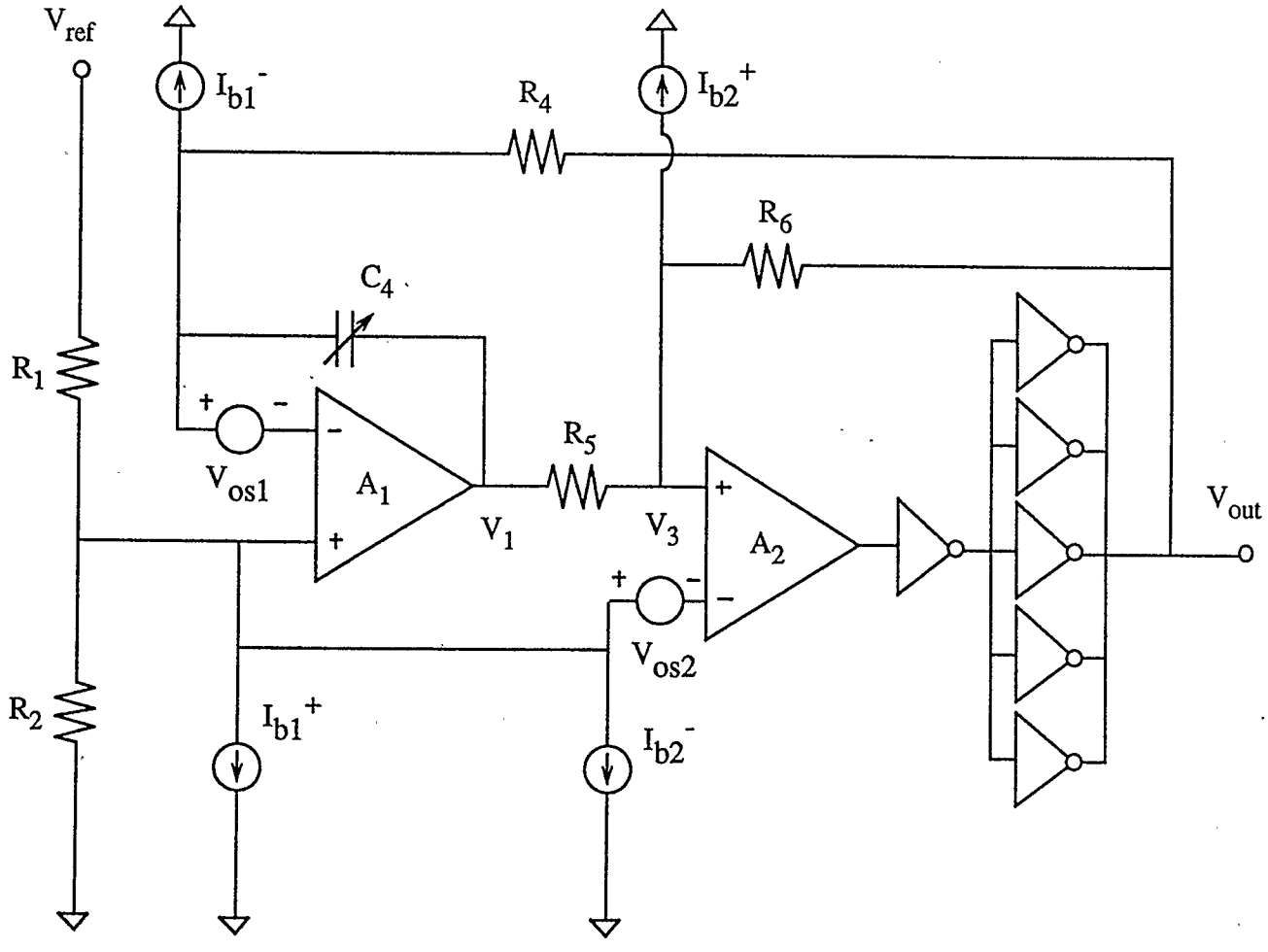


Fig.2.7 Basic RC oscillator showing effects of input offset voltage and input bias currents

I_{b2}^{-} = the input bias current associated with the inverting input of A_2

I_{b1}^{+} and I_{b2}^{+} = the input bias currents associated with the non-inverting inputs of A_1 and A_2 respectively.

The effects of nonidealities can also be included in writing the charge balance for capacitance C_4 as follows [9]:

$$\frac{V_{ref}\,T_p}{R_4+r_h}-\frac{V_t^{'}T_p}{R_4+r_h}-\frac{V_t^{'}(T_o-T_p)}{R_4+r_l}-I_{b1}^{-}T_o=0 \tag{2.35}$$

so that

$$\frac{T_p}{T_o}=\frac{V_t^{'}\left(1+\dfrac{r_h-r_l}{R_4+r_l}\right)+\dfrac{I_{b1}^{-}(R_4+r_h)}{V_{ref}}}{1+\dfrac{V_t^{'}}{V_{ref}}\dfrac{r_h-r_l}{R_4+r_l}}. \tag{2.36}$$

where $V_t^{'}=V_{ref}\dfrac{R_2}{R_1+R_2}+V_{os1}-\dfrac{R_1R_2}{R_1+R_2}(I_{b1}^{+}+I_{b2}^{-})+\dfrac{\dfrac{V_{ref}}{2}-\dfrac{V_{ref}R_2}{R_1+R_2}}{CMRR_1}$

V_{os1} = the input offset voltage of operational amplifier A_1

$CMRR_1$ = the common mode rejection ratio of operational amplifier A_1

r_h = the combined output resistance of the inverters when the output is high

r_l = the combined output resistance of the inverters when the output is low.

The charge balance for capacitor C_4 during the time period T_p is

$$(\frac{V_{ref} - V_t^{'}}{R_4 + r_h} - I_{b1}^{-})T_p = (V_h - V_l)C_4 \tag{2.37}$$

and therefore

$$T_p = \frac{V_{ref}\frac{R_5}{R_6}}{\frac{V_{ref} - V_t^{'}}{C_4(R_4 + r_h)} - \frac{I_{b1}^{-}}{C_4}}$$

$$= \frac{\frac{R_5}{R_6}(R_4 + r_h)C_4}{1 - \frac{V_t^{''}}{V_{ref}}} \tag{2.38}$$

where $V_t^{''} = V_t^{'} + I_{b1}^{-}(R_4 + r_h)$. Thus, if it is assumed that $\frac{r_h - r_l}{V_{ref}} I_{b1}^{-}$ is small, it is easy to show that the oscillation frequency is given by

$$f_o = \frac{(1 - \frac{V_t^{''}}{V_{ref}})\frac{V_t^{''}}{V_{ref}}(1 + \frac{r_h - r_l}{R_4 + r_l})}{(R_4 + r_l)C_4\frac{R_5}{R_6}(1 + \frac{V_t^{''}}{V_{ref}}\frac{r_h - r_l}{R_4 + r_l})}. \tag{2.39}$$

If the input offset voltage V_{os1} and V_{os2}, input bias currents I_{b1}^{+}, I_{b1}^{-}, I_{b2}^{+} and I_{b2}^{-} and inverter output resistances r_l and r_h are all zero, the output oscillation frequency f_o becomes

$$f_o = \frac{1}{R_4 C_4}\frac{R_1}{R_1 + R_2}(1 - \frac{R_1}{R_1 + R_2})\frac{R_6}{R_5}, \tag{2.40}$$

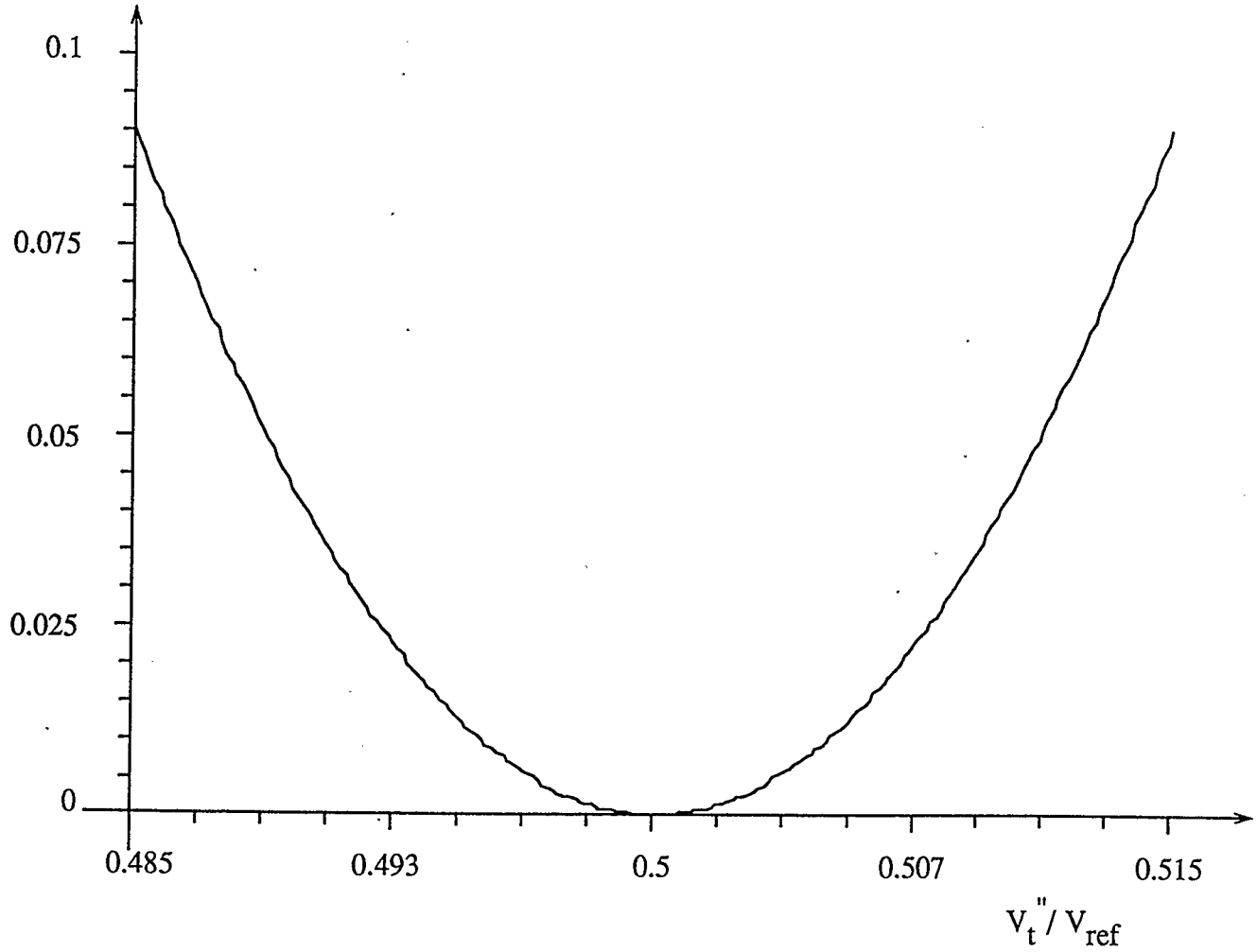


Fig. 2.8 Variation in f_o due to variations in V_t'' / V_{ref} about an operating point $V_t'' / V_{ref} = 0.5$

i.e., the oscillation frequency obtained without considering component nonidealities.

A choice of $R_1 = R_2$ results in a very marked desensitization of f_o to variations in R_1, R_2, V_{os1} and I_{b1}^- as shown in Fig. 2.8 As an example, if V_{ref} is 5.0 volts, the input offset voltage V_{os1} can be as high as 2.5 millivolts and the input bias current I_{b1}^- can be as high as 200pa before the total error due to these operational amplifier nonidealities exceeds to 0.00012% of full scale. Similarly, R_1 and R_2 changes of 0.1% in opposite directions will result in a total frequency change of only 0.0001% of full scale.

2.7 Implementation and Testing

Based on the scheme shown in Fig. 2.1, a prototype RC free-running oscillator has been built by using one half of an HA5142 dual op-amp chip, one half of a ALD2301 dual comparator chip and one MC4069 CMOS inverter chip as shown in Fig. 2.9. A high temperature capacitor of 100pF with a temperature coefficient of 140ppm ± 25ppm per Celsius degree was selected to be capacitor C_4. The resistors R_1, R_2, R_4, R_5 and R_6 were high precision low temperature coefficient resistors with temperature coefficient of -1.8 ± 2.3 ppm per Celsius degree and component values were chosen to be 100 $k\,\Omega$, 100 $k\,\Omega$, 1 $M\,\Omega$, 10 $k\,\Omega$ and 20 $k\,\Omega$, respectively. Finally, a single power supply of 5.0 volts was selected for this circuit.

The prototype oscillator was tested at a constant temperature of 27 degrees Celsius by using an oil bath with temperature control accuracy of 0.01 Celsius degree. An HP5316 universal counter was used to measure the output frequency using different

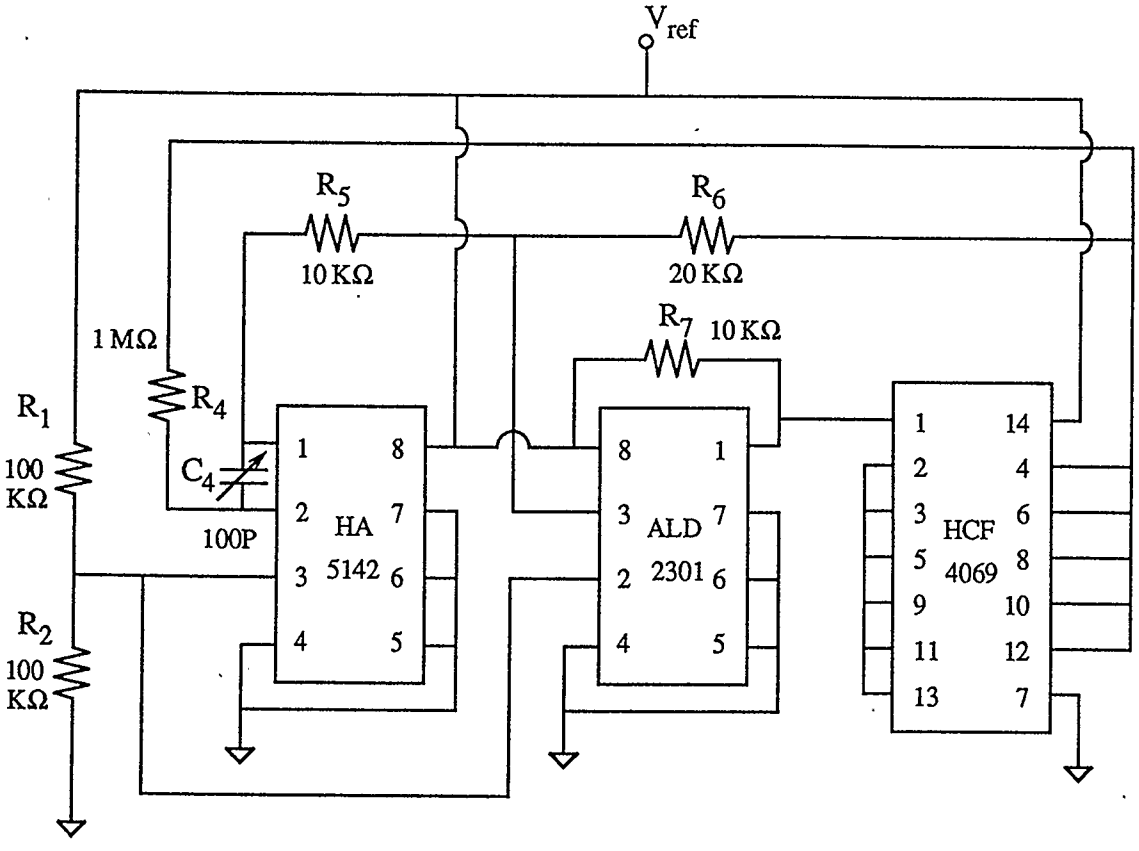


Fig. 2.9 Practical implementation for the RC free-running relaxation oscillator

gate times. The purpose of this testing was to demonstrate the stability of the oscillator, and the test results are listed in Table 2.1. It can be seen that the maximum ppm standard deviation of average output frequency is about 2.74 ppm.

Gate Time	Average Frequency (HZ)	Standard Deviation (HZ)	ppm of Average Frequency
100ms	4865.54	0.01	2.74
200ms	4865.79	0.01	2.24
500ms	4865.807	0.009	1.76
800ms	4865.841	0.008	1.69
1.0s	4865.888	0.009	1.76

Table 2.1 *Test Results for RC free-running relaxation oscillator*

The temperature characteristics of the prototype oscillator were tested at various temperatures ranging from 25 degrees Celsius to 175 degrees Celsius. Shown in Fig. 2.10 is a graph of the tested temperature characteristic of the oscillator compared with the temperature characteristic of the high temperature capacitor C_4, and it illustrates the percentage change in the period of output frequency signal and the percentage change of the capacitance C_4 vs. the variation of temperature. The gap between the two curves of Fig. 2.10 can be attributed to the temperature coefficient of resistor R_4 and the temperature coefficient mismatches of resistors R_1, R_2, R_5 and R_6. The test results also demonstrate that the oscillator circuit can work at temperature of 175 degrees Celsius.

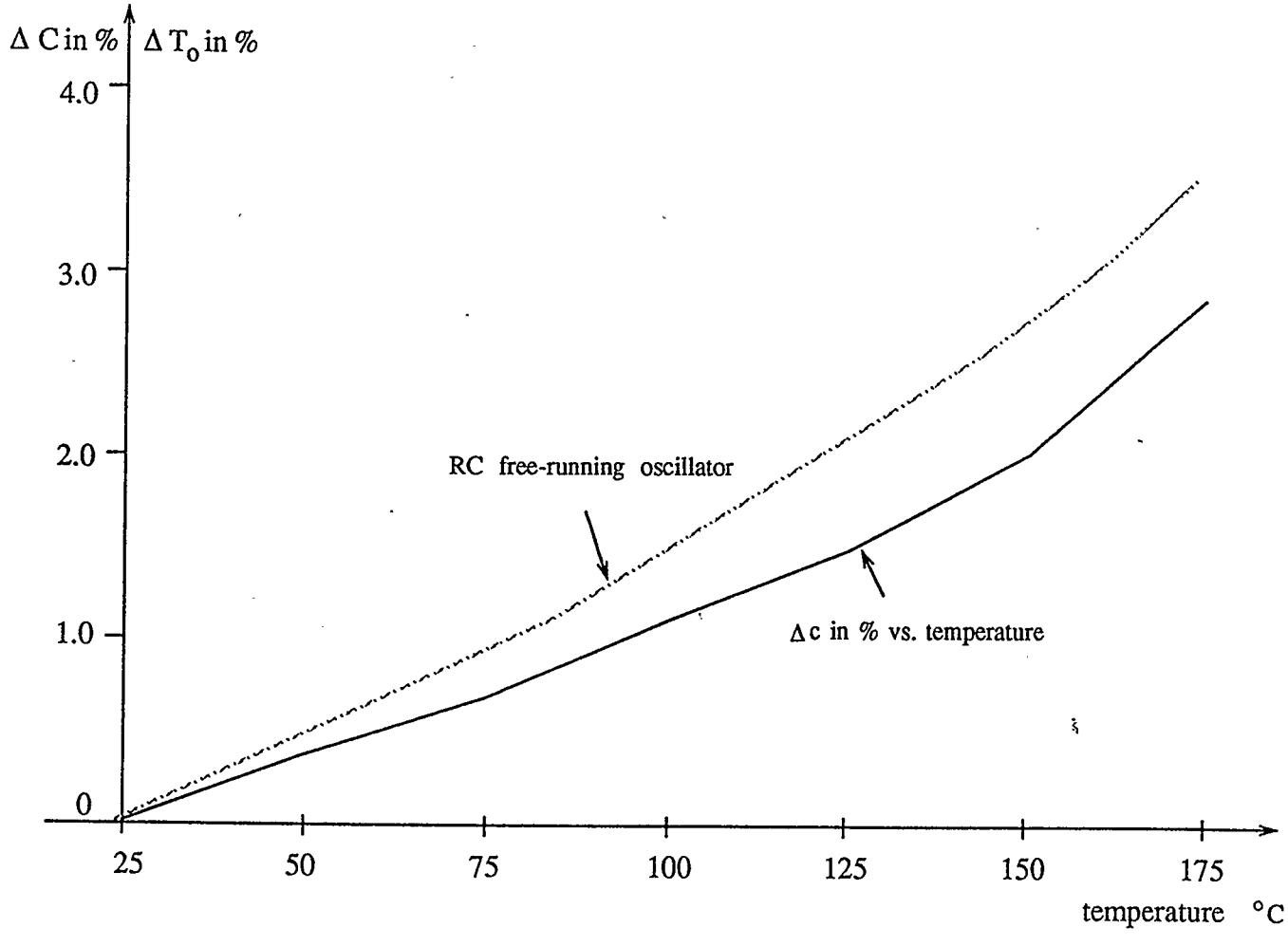


Fig. 2.10 % capacitance change and % period change vs. temperature

Chapter 3

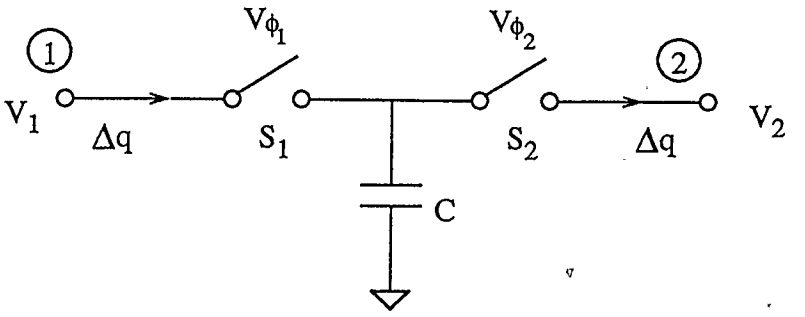
R-Pumped SC Capacitance-to-Frequency Converter

3.1 Introduction

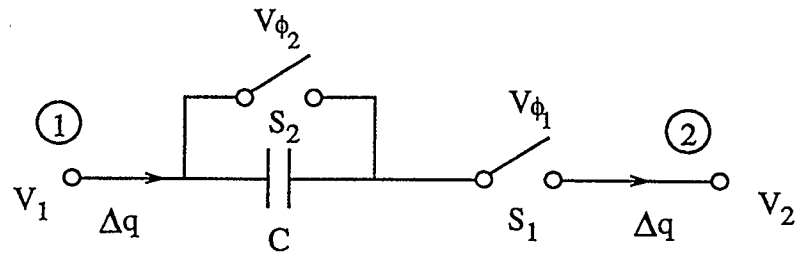
The advent of switched-capacitor techniques has led to new and innovative methods of capacitance measurement. In this chapter, a new switched-capacitor capacitance-to-frequency converter with exceptional frequency stability is described. In the basic conversion circuit, the capacitor under measurement is utilized to pump charge from a capacitive charge reservoir which is replenished by a current flow through a resistor. In order to maintain a charge balance , the capacitor must be switched at a suitable rate which is governed by the output frequency and is dependent on the capacitor size and one resistor value. A switching scheme has been devised to make the circuit insensitive to operational amplifier input offset voltage and input bias currents and all but one resistor. The operation of the conversion circuit is discussed, the effects of component nonidealities on the output frequency are analyzed, and methods for elimination of these nonideal effects are presented.

3.2 Simulated Resistor Concepts

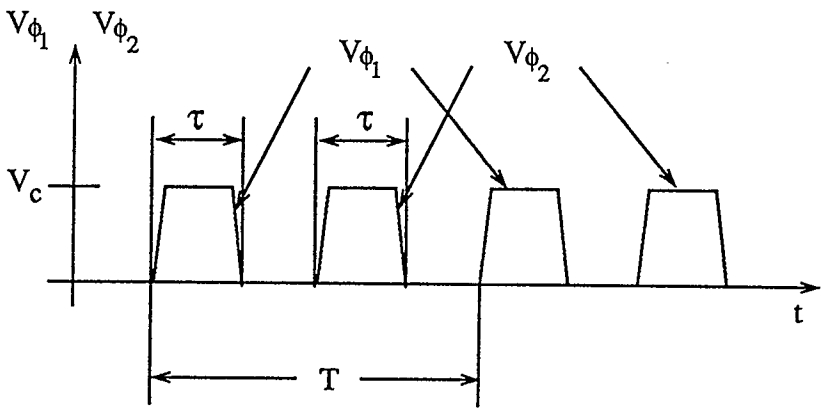
The fundamental principle in all switched-capacitor circuits is the transfer of charge from one node to another in a circuit. Two simple switched-capacitor elements, or simulated resistors, which are constructed from capacitors and switches and can perform this function are shown in Fig. 3.1 [10], [11]. In the shunt circuit of Fig. 3.1(a),



(a)



(b)



(c)

Fig. 3.1 Switched capacitor simulated resistors :(a) shunt circuit; (b) series circuit; (c) clock waveforms

capacitor C is alternatively charged to V_1 and V_2. Each cycle results in a charge $\Delta q = C\,(V_1 - V_2)$ flowing into node 2. For the series circuit of Fig. 3.1(b), the capacitor C is alternatively discharged, and then recharged to a voltage $V_1 - V_2$. During recharging, a charge $\Delta q = C\,(V_1 - V_2)$ flows into node 2. The charge flows in sharp pulses, at the leading edge of the clock pulses used for controlling the operation of switches. However, for each of the elements in Fig. 3.1 we can define an average current, i_{ave}, as the charge flow Δq during each clock period T divided by that period giving:

$$i_{ave} = \frac{\Delta q}{T} = \frac{C\,(V_1 - V_2)}{T}$$

Thus both switched-capacitor elements behave (on average) as resistors of value

$$R = T\,/\,C\,. \tag{3.1}$$

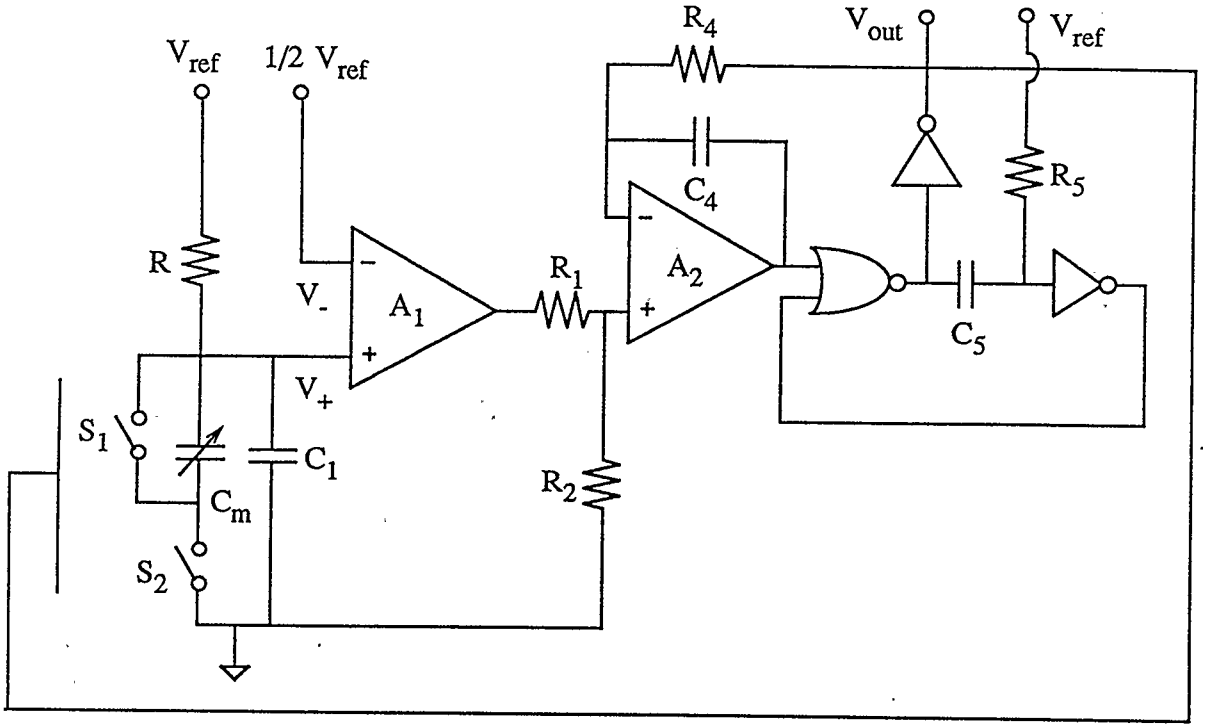
Eq. (3.1) indicates the possibility of simulating ratioed resistors by the switching of ratioed capacitors. Furthermore, the resistive ratios can be varied by using different switching frequencies for different resistors.

3.3 Circuit Configuration

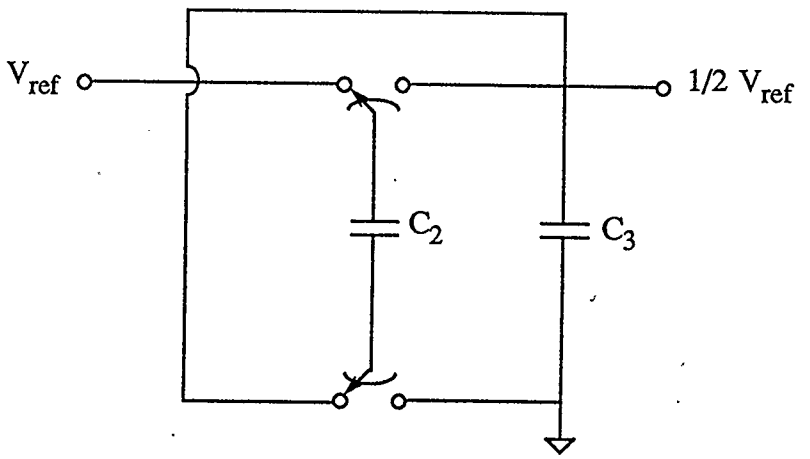
Fig. 3.2 shows the schematic diagram of the R-pumped switched-capacitor capacitor to frequency converter circuit. It consists of three main parts:

(1). The half reference voltage generator formed by one double-pole, double-throw (DPDT) switch and two capacitors C_2 and C_3.

(2). The open-loop amplifier formed by op-amp A_1, a resistor R, two switches S_1, S_2, a large capacitor C_1 and capacitor C_m which is the capacitor under measurement.



(a)



(b)

Fig. 3.2 Schematic of R-pumped SC capacitor-to-frequency converter: (a) circuit diagram; (b) half reference voltage generator

(3). The voltage to frequency converter formed by an integrator A_2 and a one-shot multivibrator consisting of one nor-gate, one inverter, resistor R_5 and capacitor C_5. For single-supply operations, all components of this circuit are powered from a single reference voltage V_{ref}.

The half reference voltage generator shown in Fig. 3.2(b) utilizes one DPDT switch and two capacitors to produce a high precision voltage equal to $1/2\,V_{ref}$. When the input switches close, capacitor C_2 and capacitor C_3 are in series connection with input voltage V_{ref} and are charged by input voltage V_{ref}. When the input switch is opened, and the output switch is closed, the capacitors C_2 and C_3 are connected in parallel. Finally, the output voltage will be equal to $1/2\,V_{ref}$ whether or not capacitor C_2 is equal to capacitor C_3.

The inverting input terminal of the open-loop amplifier A_1 is connected to the half reference voltage $1/2\,V_{ref}$, while the non-inverting input terminal is connected to a voltage divider formed by a conventional resistor R and a switched capacitor simulated resistor constructed from capacitor C_m and two switches as shown in Fig. 3.1(b). Node 1 is connected to a large capacitor C_1 which is used as a charge reservoir. The difference voltage between the output of the voltage divider and the half reference voltage is amplified by op-amp A_1 and the output of A_1 is fed into a voltage to frequency converter as an input voltage through another voltage divider R_1 and R_2.

The free-running voltage-to-frequency converter used here was developed by Trofimenkoff and Haslett [8]. In this circuit, the op-amp A_2, the CMOS nor-gate and two CMOS inverters are all powered from the single supply voltage V_{ref}. If R_4 is

large, the low level of the output pulse will be very nearly equal to zero and the high level of the output pulse will be very nearly equal to V_{ref}. Then if the threshold voltage of the inverter is taken to be equal to ηV_{ref}, the pulse width of the output pulse, T_p, which is controlled by the one-shot multivibrator will be given by

$$T_p = R_5 C_5 \ln \frac{1}{(1-\eta)}. \tag{3.2}$$

While the output pulse is present, the outputs of both inverters will be high. At all other times, these outputs will be low. A charge balance for capacitor C_4 can then be written as

$$-\frac{V_t}{R_4} T_o + \frac{V_{ref}}{R_4} T_p = 0 \tag{3.3}$$

where T_o is the period of output pulse, so that

$$f_o = \frac{1}{T_o} = \frac{V_t}{V_{ref}\, T_p}. \tag{3.4}$$

Hence the output frequency, f_o, is directly proportional to the input voltage V_t. Furthermore, Eq.(3.4) can be re-arranged to

$$\frac{T_p}{T_o} = \frac{V_t}{V_{ref}} \tag{3.5}$$

which states that the output pulse width-to-period ratio is equal to the input-to-reference voltage ratio, independent of circuit component values.

Since the action of the two switches in the simulated resistor is controlled by the non-overlapping clock pulse signal which is generated from the output pulse of the

voltage-to-frequency converter and has the same frequency of output pulse, there exists a feed-back loop in the capacitor-to-frequency circuit. This feed-back configuration improves the characteristics of this circuit.

3.4 Circuit Operation

The operation of the conversion circuit can be described as follows. At power on, the output of the circuit remains low before the potential of the non-inverting input terminal of op-amp A_1 is increased to a little higher than the half reference voltage $1/2\,V_{ref}$ by charging capacitor C_1 through resistor R. The two switches S_1 and S_2 of the circuit act alternately. When S_1 is open, S_2 is closed and vice versa. When the output V_{out} becomes high, switch S_1 is opened and switch S_2 is closed, so that capacitance C_m receives charge from charge reservoir C_1, and at the same time, C_1 is replenished by the current flow through resistor R. If the capacitance of C_1 is much larger than capacitance of C_m, the potential of the non-inverting input terminal of A_1 will be constant and the charge stored in capacitor C_m is $Q_m = C_m V_+$, where V_+ is the potential at non-inverting terminal of A_1. When the output V_{out} goes low, S_1 is closed and S_2 is opened, allowing capacitor C_m to discharge through S_1. When V_{out} goes high, C_m will receive charge again, completing one period of oscillation.

For an ideal case, it is assumed the capacitance of C_1 is much much larger than the capacitance of C_m so that the potential at non-inverting input terminal can be considered to be constant. If the period of the output signal is $T_{O_{ideal}}$, the charge balance equation for C_1 can be written as

$$\frac{V_{ref} - V_+}{R} T_{o_{ideal}} = C_m V_+ \tag{3.6}$$

where V_+ is equal to $1/2\,V_{ref}$ so that

$$T_{o_{ideal}} = R\,C_m \tag{3.7}$$

$$f_{o_{ideal}} = \frac{1}{T_{o_{ideal}}} = \frac{1}{R\,C_m}. \tag{3.8}$$

It is seen that the output frequency $f_{o_{ideal}}$ is only dependent on the resistance R and the capacitance C_m and is, to first order, independent of the other circuit components making up the capacitance-to-frequency converter.

3.5 Nonidealities

By inspecting Fig. 3.2, it is easy to find that the output frequency of the conversion circuit is affected by nonidealities such as the size of capacitance C_1, parasitic capacitance between each terminal of switch S_1 and ground, the input offset voltage and input bias currents of op-amp A_1, and the non-zero on-resistance R_{on} of two switches. The influence of these nonidealities is analyzed in the following section, and methods for eliminating these nonideal effects are discussed.

3.5.1 The Effects of Size of Capacitor C_1 and Time Interval T_p

In order to illustrate the effects of the size of capacitor C_1 and the time interval T_p on the output frequency, the open-loop amplifier A_1 of Fig. 3.2, which is reproduced in Fig. 3.3, is considered. When output V_{out} is turned high and switch S_1 is opened while switch S_2 is closed, capacitor C_m is in parallel connection with capacitor

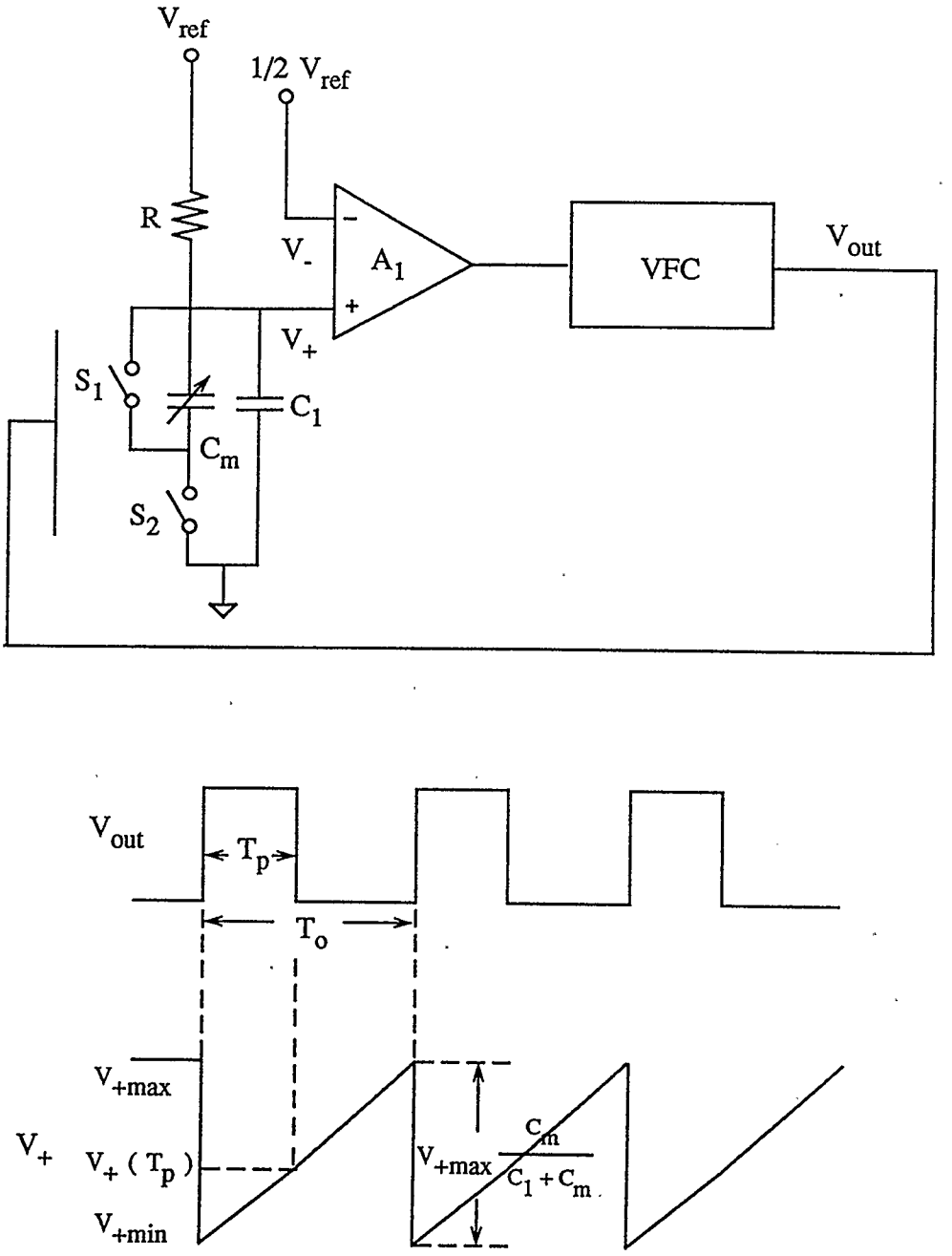


Fig. 3.3 The basic capacitance-to-frequency converter and the voltage waveform at the non-inverting input of A_1

C_1. Capacitor C_m will acquires charge from capacitor C_1 until the voltages across both capacitor C_1 and C_m are same. The voltage between the two plates of capacitor C_1 drops from V_{+max} to V_{+min} due to the loss of charge. V_{+min} can be expressed as follows.

$$V_{+min} = V_{+max} \frac{C_1}{C_1 + C_m} \tag{3.9}$$

At the same time, capacitor C_1 and C_m are charged by the power supply V_{ref} through resistor R. After time interval T_p, the output V_{out} goes low, the switch S_1 is closed but switch S_2 is opened. Capacitor C_m is fully discharged through switch S_1 while capacitor C_1 is continuously charged by the power supply V_{ref} until the voltage across capacitor C_1 is equal to V_{+max}. When the circuit is in the steady state, the average voltage of V_+ has to be $1/2 V_{ref}$, so that V_{+max} can be found from

$$V_{+ave} = \frac{1}{2}(V_{+max} + V_{+min}) = \frac{1}{2} V_{ref}$$

by substituting $V_{+min} = V_{+max} \frac{C_1}{C_1 + C_m}$.

Therefore,

$$V_{+max} = V_{ref} \frac{C_1 + C_m}{2C_1 + C_m}. \tag{3.10}$$

During the time interval T_p, the voltage across capacitor C_1 is given by

$$V_+(t) = V_{ref} \frac{C_1}{2C_1 + C_m} e^{-\frac{t}{R(C_1 + C_m)}} + V_{ref}\left(1 - e^{-\frac{t}{R(C_1 + C_m)}}\right)$$

$$= V_{ref} - V_{ref} \frac{C_1 + C_m}{2C_1 + C_m} e^{-\frac{t}{R(C_1 + C_m)}}, \tag{3.11}$$

and when $t = T_p$, the voltage of C_1 can be written to be

$$V_+(T_p) = V_{ref} - V_{ref} \frac{C_1 + C_m}{2C_1 + C_m} e^{-\frac{T_p}{R(C_1 + C_m)}}. \tag{3.12}$$

Then, during the time when output V_{out} is low ($T_p < t < T_o - T_p$), capacitor C_1 is charged by the power supply V_{ref} with a time constant $T = R\,C_1$, the voltage across C_1 is

$$V_+(t) = [V_{ref} - V_{ref} \frac{C_1 + C_m}{2C_1 + C_m} e^{-\frac{T_p}{R(C_1 + C_m)}}] e^{-\frac{t}{RC_1}} + V_{ref}(1 - e^{-\frac{t}{RC_1}})$$

$$= V_{ref} - V_{ref} \frac{C_1 + C_m}{2C_1 + C_m} e^{-\left[\frac{T_p}{R(C_1 + C_m)} + \frac{t}{RC_1}\right]}. \tag{3.13}$$

Hence, the oscillation period of the circuit, T_o, can be obtained by substituting Eq.(3.10) into Eq.(3.13) and solving Eq.(3.13). The result is

$$T_o = R\,C_m [\frac{C_1}{C_m} \ln \frac{C_1 + C_m}{C_1} + \frac{T_p}{R(C_1 + C_m)}]. \tag{3.14}$$

If it is assumed C_1 / C_m is small, then $\ln \frac{C_1 + C_m}{C_1} \approx \frac{C_m}{C_1} - \frac{1}{2}(\frac{C_m}{C_1})^2$, so that

$$T_o = R\,C_m [1 - \frac{1}{2} \frac{C_m}{C_1} + \frac{T_p}{R(C_1 + C_m)}]. \tag{3.15}$$

Thus, as a comparison with Eq. (3.7), the fractional error is

$$\varepsilon = -\frac{1}{2}\frac{C_m}{C_1} + \frac{T_p}{R(C_1 + C_m)}.$$

The oscillation period of the circuit can also be calculated by writing down the charge balance equation for capacitor C_1 as discussed previously for the ideal case.

$$\frac{V_{ref} - \overline{V_+}}{R} T_o = V_+(t = T_p) C_m \tag{3.16}$$

where $\overline{V_+} = \frac{1}{T_o}[a_1 + a_2]$ and

$$a_1 = \int_0^{T_p} V_{ref}\left(1 - \frac{C_1 + C_m}{2C_1 + C_m} e^{-\frac{t}{R(C_1 + C_m)}}\right) dt$$

$$a_2 = \int_0^{T_o - T_p} V_{ref}\left(1 - \frac{C_1 + C_m}{2C_1 + C_m} e^{-\left[\frac{T_p}{R(C_1 + C_m)} + \frac{t}{RC_1}\right]}\right) dt$$

so that period T_o can be expressed as follows by noting that $\overline{V_+} = 1/2\, V_{ref}$ to yield

$$T_o = 2\left[1 - \frac{C_1 + C_m}{2C_1 + C_m} e^{-\frac{T_p}{R(C_1 + C_m)}}\right] R\, C_m \tag{3.17}$$

The oscillation period of the circuit for the ideal case is calculated using Eq.(3.7), and is compared to the results obtained by using Eq.(3.14) and Eq.(3.17) in Table 3.1 and Table 3.2. It can be seen from Table 3.1 and Table 3.2 that the difference between the ideal period and the real period obtained by using Eq.(3.14) and Eq.(3.17) is dependent on the ratio of capacitance C_m to capacitance C_1 and the ratio of pulse width T_p to period T_o. The error will be affected by the capacitance ratio C_m / C_1, increasing with increased ratio C_m / C_1. Thus, in order to reduce output frequency error, the ratio of C_m / C_1 should be chosen to be as small as possible.

$C_m / C_1 = 0.001$

	T_{oideal} by Eq.(3.7)	T_o by Eq.(3.14)	Error (%)
$T_p = 1/2\,R\,C_m$	1.0 RC_m	0.999999833 RC_m	0.0000167
$T_p = 1/3\,R\,C_m$	1.0 RC_m	0.999833333 RC_m	0.0166667
$T_p = 1/4\,R\,C_m$	1.0 RC_m	0.999750083 RC_m	0.0249917
$T_p = 1/8\,R\,C_m$	1.0 RC_m	0.999625208 RC_m	0.0374792
$T_p = 1/10\,R\,C_m$	1.0 RC_m	0.999600233 RC_m	0.0399767

	T_{oideal} by Eq.(3.7)	T_o by Eq.(3.17)	Error (%)
$T_p = 1/2\,R\,C_m$	1.0 RC_m	0.999999874 RC_m	0.0000126
$T_p = 1/3\,R\,C_m$	1.0 RC_m	0.999833361 RC_m	0.0166639
$T_p = 1/4\,R\,C_m$	1.0 RC_m	0.999750092 RC_m	0.0249908
$T_p = 1/8\,R\,C_m$	1.0 RC_m	0.999625178 RC_m	0.0374822
$T_p = 1/10\,R\,C_m$	1.0 RC_m	0.999600194 RC_m	0.0399806

Table 3.1 The oscillation period calculated by using Eq.(3.7), Eq.(3.14) and Eq.(3.17) for $C_m / C_1 = 0.001$

$C_m / C_1 = 0.01$

	T_{oideal} by Eq.(3.7)	T_o by Eq.(3.14)	Error (%)
$T_p = 1/2\,R\,C_m$	1.0 RC_m	0.999983580 RC_m	0.0016419
$T_p = 1/3\,R\,C_m$	1.0 RC_m	0.998333415 RC_m	0.1666584
$T_p = 1/4\,R\,C_m$	1.0 RC_m	0.997508332 RC_m	0.2491667
$T_p = 1/8\,R\,C_m$	1.0 RC_m	0.996270709 RC_m	0.372929
$T_p = 1/10\,R\,C_m$	1.0 RC_m	0.996023184 RC_m	0.3976815

	T_{oideal} by Eq.(3.7)	T_o by Eq.(3.17)	Error (%)
$T_p = 1/2\,R\,C_m$	1.0 RC_m	0.999987705 RC_m	0.0012294
$T_p = 1/3\,R\,C_m$	1.0 RC_m	0.998336158 RC_m	0.1663842
$T_p = 1/4\,R\,C_m$	1.0 RC_m	0.997509361 RC_m	0.2490638
$T_p = 1/8\,R\,C_m$	1.0 RC_m	0.996267887 RC_m	0.3732112
$T_p = 1/10\,R\,C_m$	1.0 RC_m	0.996019408 RC_m	0.3980591

Table 3.2 The oscillation period calculated by using Eq.(3.7), Eq.(3.14) and Eq.(3.17) for $C_m / C_1 = 0.01$

3.5.2 The Effects of Frequency-Dependent Gain of Op-Amp A_1

As mentioned in the above section, the potential at the non-inverting input terminal of op-amp A_1 is a dc voltage with some ripple instead of an ideal dc voltage. This ripple is amplified by the open-loop amplifier A_1 and the waveform at the output terminal of A_1 depends on the frequency response characteristic of op-amp A_1.

If the capacitance C_m is very small in comparison to the capacitance C_1, the difference between the two time constants $R\,(C_m+C_1)$ and $R\,C_1$ can be ignored. Therefore, as shown in Fig. 3.4, the ripple at the non-inverting input terminal V_+ can be approximately expressed as

$$V_{+r} \approx -\frac{A}{2}+\frac{A}{T_o}t\,, \tag{3.18}$$

where $A = V_{+max}\,(1-\dfrac{C_1}{C_1+C_m}) = V_{ref}\,\dfrac{C_m}{2C_1+C_m}$ and T_o is the oscillation period of the output frequency signal. The potential also can be expanded in a Fourier series to yield [12]

$$V_{+r} \approx -\frac{A}{\pi}\sum_{k=1}^{\infty}\frac{1}{k}\sin 2k\,\pi f_o\,t\,, \tag{3.19}$$

where f_o is the output frequency. It can be seen from Eq.(3.19) and Fig. (3.4) that the ripple contains a series of sinusoidal harmonics whose amplitude decreases with frequency by a factor of $1/k$.

The differential gain of the op-amp A_1 can be expressed as [13]

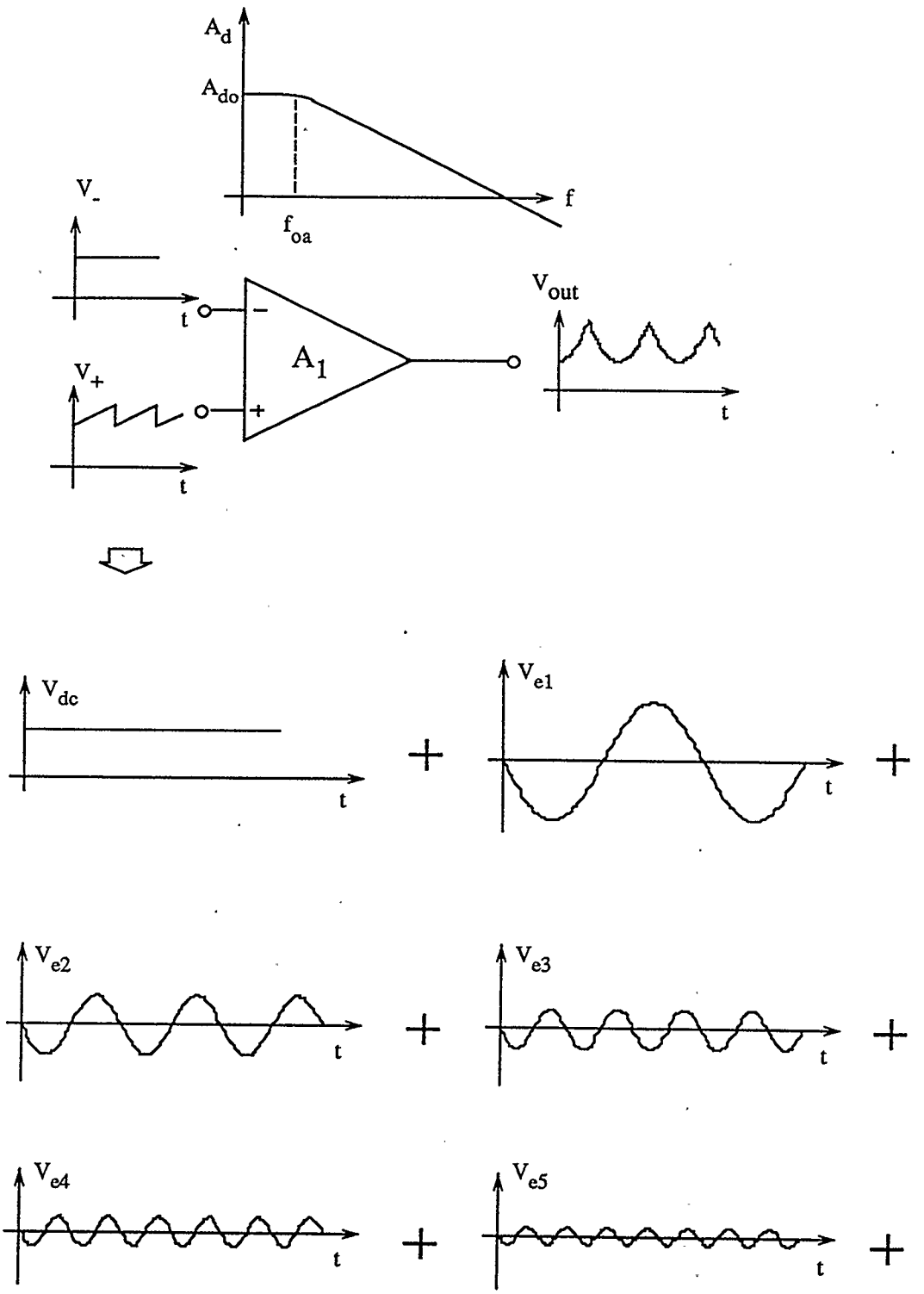


Fig. 3.4 A diagram illustrating the effects of input ripple voltage and frequency response characteristics of op-amp A_1

$$A_d = \frac{A_{d0}}{1 + j\frac{f}{f_{oa}}} \tag{3.20}$$

by using a dominant-pole frequency response model, where A_{d0} is the open-loop dc gain of the amplifier, $j = \sqrt{-1}$, f is the frequency and f_{oa} is the location of the frequency pole. For a sinusoidal harmonic input voltage connected to the non-inverting input of A_1, the voltage gain is

$$A_d(jf) = \frac{A_{d0}}{\sqrt{1 + (\frac{f}{f_{oa}})^2}}, \tag{3.21}$$

and the phase angle is

$$\phi(jf) = \tan^{-1}\frac{f}{f_{oa}}. \tag{3.22}$$

Hence, for the open-loop amplifier A_1 with an input voltage V_{+r} given by Eq.(3.19), the output ripple voltage V_{or} can be easily shown to be

$$V_{or} \approx -\frac{A\,A_{d0}}{\pi}\sum_{k=1}^{\infty}\frac{1}{k\sqrt{1+(\frac{k f_o}{f_{oa}})^2}}\sin(2k\pi f_o t - \tan^{-1}\frac{k f_o}{f_{oa}}). \tag{3.23}$$

As an example, if it is assumed the pole frequency f_{oa} is 1.5 Hz, the open-loop gain A_{d0} is 120db, C_m is 120pf, C_1 is 0.1uf, resistor R is 100kΩ, and the output frequency is about 83.33 kHz, the output ripple voltage V_{or}, calculated by Eq.(3.23), has a peak-to-peak value of about 30 millivolts as shown in Fig.(3.5).

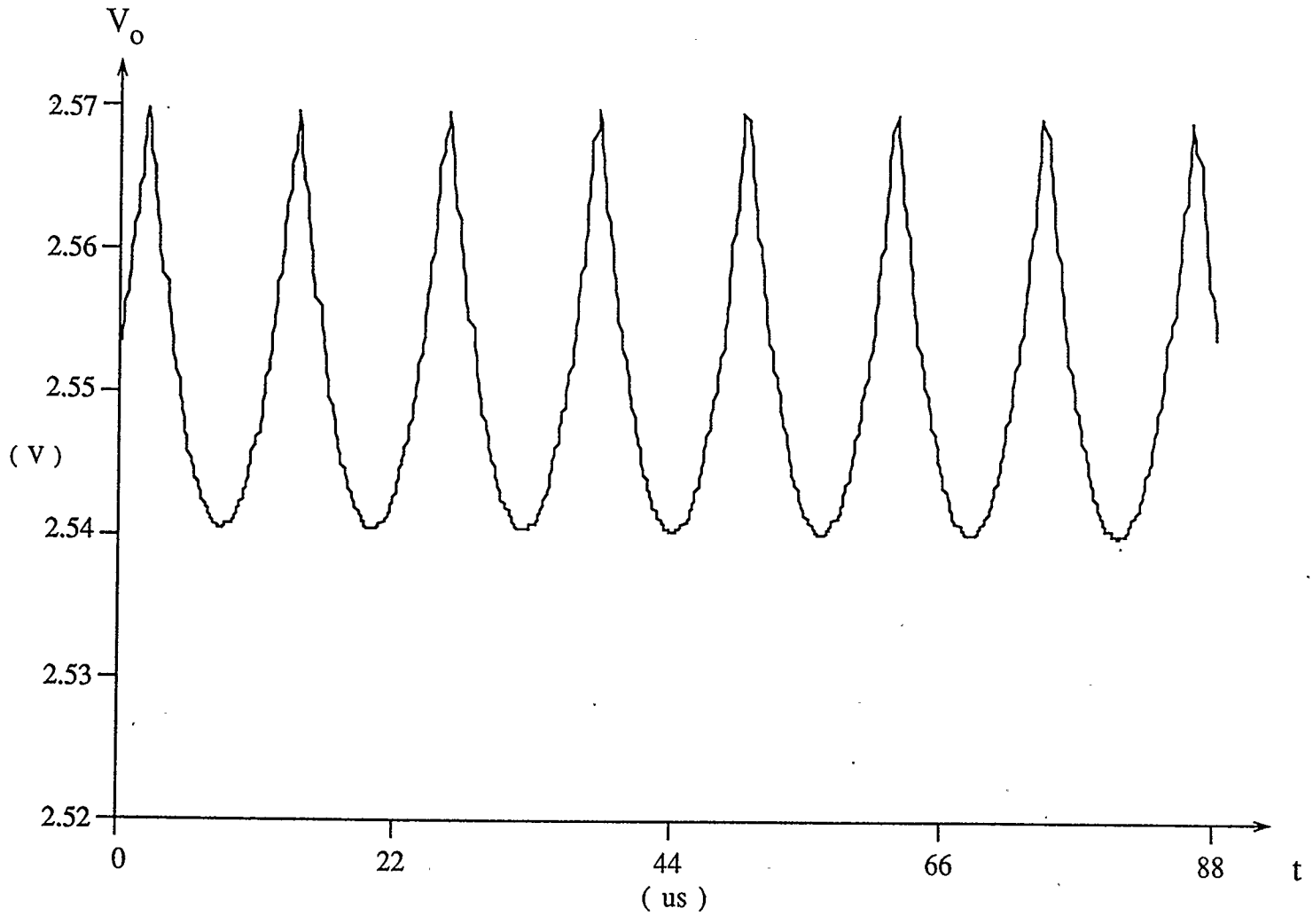


Fig. 3.5 Output waveform of open-loop amplifier A_1

From the above analysis, it can be concluded that the peak-to-peak value of the output ripple voltage depends on the capacitance ratio C_m / C_1 , the open-loop gain and the pole frequency of op-amp A_1. If the peak-to-peak value is large, the output frequency will be affected even though the integrator of the VFC has an ability to suppress high frequency harmonics. One approach for reducing output ripple voltage is to choose a small capacitance ratio C_m / C_1 by using a large capacitor C_1.

3.5.3 The Effects of Stray Capacitances

In some situations, the capacitance to be measured C_m is a typical three-terminal capacitor with two plate-to-ground stray capacitances C_{s1} and C_{s2} as shown in Fig. (3.6). To simplify the analysis, the assumption that capacitance C_1 is much much larger than capacitances C_m, C_{s1} and C_{s2} is made so that the potential of the non-inverting input of op-amp A_1 can be considered to be unchanged during the switching period.

In this ideal case, at power on, the output of the circuit remains low before the potential of the non-inverting input terminal of op-amp A_1 increases to a little higher than the half reference voltage $1/2 V_{ref}$ by the charging of capacitor C_1 and stray capacitance C_{s1}, which is in parallel with capacitance C_1, through resistor R. When the output V_{out} becomes high, switch S_1 is opened and switch S_2 is closed, so that capacitance C_m receives charge from charge reservoir C_1 and C_{s1}, and at the same time, C_1 and C_{s1} are replenished by the current flow through resistor R. The charge stored in capacitor C_m is $Q_m = C_m V_+$, where V_+ is the potential at the non-inverting

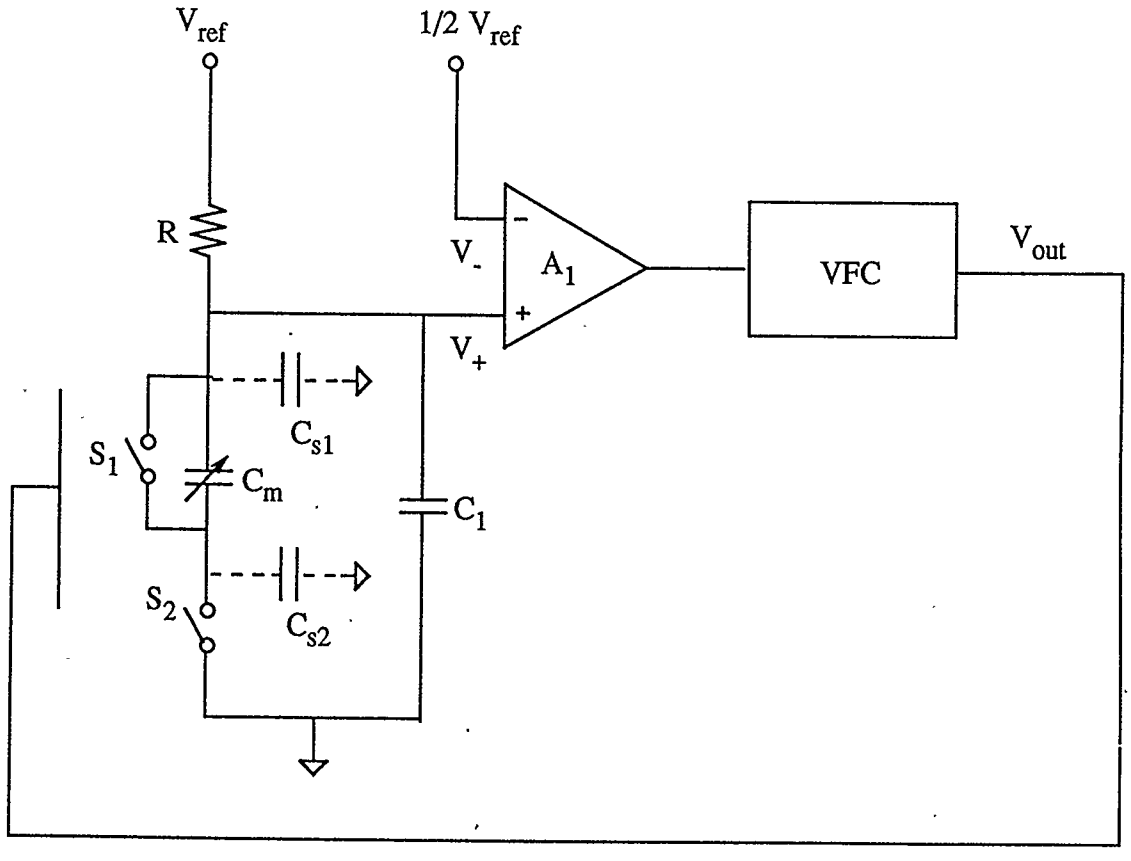


Fig. 3.6 The switched capacitor capacitance-to-frequency conversion circuit with a typical three-terminal capacitor

terminal of A_1. After the output V_{out} is turned to be low, S_1 is closed and S_2 is opened. This allows capacitor C_m to discharge through S_1 and the stray capacitor C_{s2} acquires charge $Q_{s2}=C_{s2}V_+$ from C_1 and C_{s1}. When V_{out} goes high, C_{s2} will be discharged through S_2 while C_m will receive charge again, and completing one period of oscillation.

It can be seen that the charge taken away in one period by capacitor C_m and C_{s2} is Q_m+Q_{s2}, and this charge must be compensated by the current flow through resistor R in order to maintain a charge balance. Hence, the charge balance equation can be written as

$$\frac{V_{ref}-V_+}{R}T_o = C_m V_+ + C_{s2}V_+, \tag{3.24}$$

and the oscillation period can be found to be

$$T_o = R\,(C_m+C_{s2}) \tag{3.25}$$

by substituting $V_+=1/2\,V_{ref}$ into Eq.(3.24).

The above simplified discussion ignored the role which the capacitor size of C_1 plays. Nevertheless, it leads to a qualitatively correct conclusion, namely that the effect of stray capacitance C_{s1} on the output frequency can be ignored since C_{s1} plays no role in drawing charge from the charge reservoir. However, the effect of stray capacitance C_{s2} on the output frequency must be considered since capacitance C_{s2} does take charge from the charge reservoir just as capacitance C_m does, and this will cause an error in the output frequency.

3.5.4 The Effects of On-Resistance of Switches

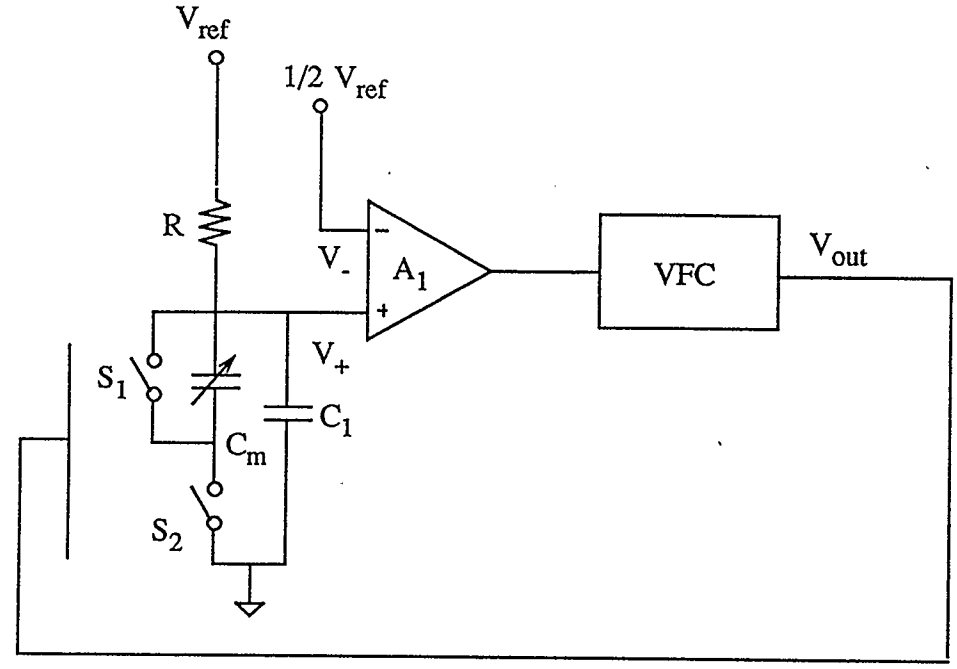
When the switches S_1 and S_2 are closed, both of them have non-zero on-resistance R_{on} and the value of R_{on} can be in the range of a few hundred ohms to a few kilohms. In order to illustrate the effect of the non-zero R_{on} on the operation of the capacitance-to-frequency conversion circuit, the open-loop amplifier of Fig. 3.2 , reproduced in Fig. 3.7(a), is considered. Including the on-resistance of both switches S_1 and S_2, results in the equivalent circuit of Fig. 3.7(b). If it is assumed that the switch resistances R_{on1} and R_{on2} are linear and equal, and the capacitance C_1 is much larger than C_m, the potential of the non-inverting input of A_1, V_+, can be considered to be constant. Then, when $t = T_p$, the voltage across C_m is of the form

$$V_{cm}(t = T_p) = V_+(1 - e^{-\frac{T_p}{R_{on2}C_m}}). \tag{3.26}$$

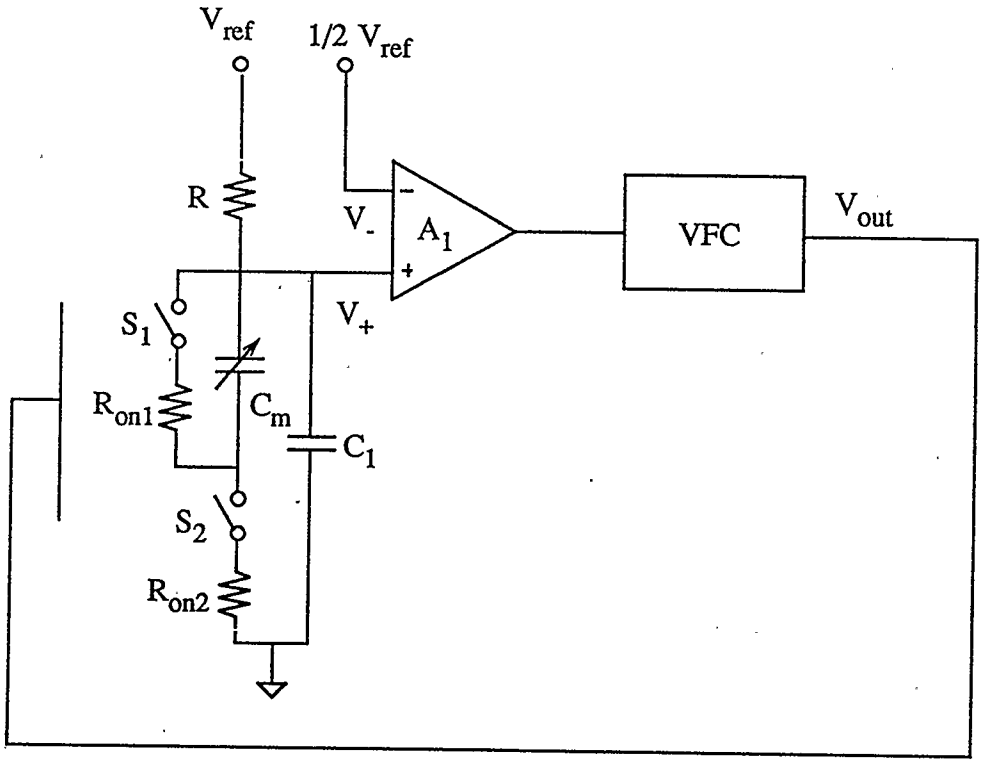
Here, it is assumed that C_m was initially fully discharged. Capacitor C_m discharges through resistor R_{on1}, and at the time when the output is about to turn high, i.e., when $t = T_o$, the voltage across capacitor C_m is

$$V_{cm}(t = T_o) = V_{cm}(t = T_p)\, e^{-\frac{T_o - T_p}{R_{on1}C_m}}. \tag{3.27}$$

Thus, as a comparison with the ideal case where $R_{on1} = R_{on2} = 0$ shows, on-resistances reduce the effective value of capacitance C_m, and increase the output frequency. Because R_{on1} and R_{on2} have the same value, and $T_o - T_p > T_p$ is usually valid, switch on-resistance R_{on} should be chosen at least one hundred times smaller than the resistance of R so that the capacitance C_m can fully charge and discharge when this circuit



(a)



(b)

Fig. 3.7 Open-loop amplifier A_1: (a) circuit diagram; (b) equivalent circuit including switch resistances

is used to measure the capacitance of C_m.

3.5.5 The Effects of Amplifier Nonidealities

Both operational amplifier A_1 and A_2 have input offset voltage V_{os} and input bias currents I_b^+ and I_b^-, these amplifier nonidealities can cause errors in the output frequency of the circuit. However, the error associated with input offset voltage and input bias currents of A_2 is reduced because there exists a feed-back loop in which the amplifier A_2 is enclosed in the circuit and the amplifier A_1 is an open-loop amplifier whose gain is about 120db. Here, only the effects of nonidealities of A_1 on the output frequency are considered, and these effects can be illustrated by writing down the charge balance equation of C_m assuming that the capacitance of C_1 is much larger than that of C_m. If the input offset voltage of A_1 is V_{os1} and input bias currents of A_1 are I_{b1}^+ and I_{b1}^-, the charge balance equation for C_1 is

$$\frac{V_{ref} - V_+}{R} T_o - I_{b1}^+ T_o = C_m V_+ \tag{3.28}$$

so that

$$f_o = \frac{1}{T_o} = \frac{1}{R C_m} \left(1 + \frac{2V_{os1} - I_{b1}^+ R}{\frac{1}{2} V_{ref} - V_{os1}}\right) \tag{3.29}$$

where V_+ is the potential at the noninverting terminal of A_1, and $V_+ = \frac{1}{2} V_{ref} - V_{os1}$. The error introduced by the input offset voltage V_{os1} and input bias current I_{b1}^+ is small. For example, if V_{ref} is 5 volts, V_{os1} is 2.5 millivolts, I_{b1}^+ is 100pa, and R is

$100k\ \Omega$, the total error due to these operational amplifier nonidealities will at most be equal to 0.0002 percent of full scale.

3.6 Implementation and Testing

As shown in Fig. 3.8, a prototype implementation has been built by using discrete components. The op-amps and switches used were HA5142 and LTC1043 respectively. The capacitors C_1, C_2 and C_3 were chosen to be 0.1uF. A high temperature capacitor with a temperature coefficient of 140ppm ± 25ppm per Celsius degree was selected for capacitor C_m and the capacitor value was chosen to be 100pF. An high precision low temperature coefficient ($-1.8 \pm 2.3 ppm/^{o}C$) resistor of $100k\ \Omega$ was used for resistor R, and finally, the power supply V_{ref} was set to be 5 Volts.

Measurement were made at a constant temperature of 27 degrees Celsius to show the stability of the prototype converter. In order to obtain a very stable working temperature, an oil bath with temperature control accuracy of about 0.01 Celsius degree was used in the testing. The measurement data listed in Table 3.3 are obtained at different gate times by using an HP5316 universal counter. From Table 3.3, it can be seen that the R-pumped converter is very stable, and the maximum ppm standard deviation of average frequency is only 0.76.

The prototype converter was tested under various temperature ranging from 25 degrees Celsius to 175 degrees Celsius. The measurement results are plotted in Fig. 3.9. In Fig. 3.9, the two curves show the percentage change in the period of output frequency signal vs. the variation of temperature and the percentage change of the capacitance C_m vs. the variation of temperature, respectively. Compared with the

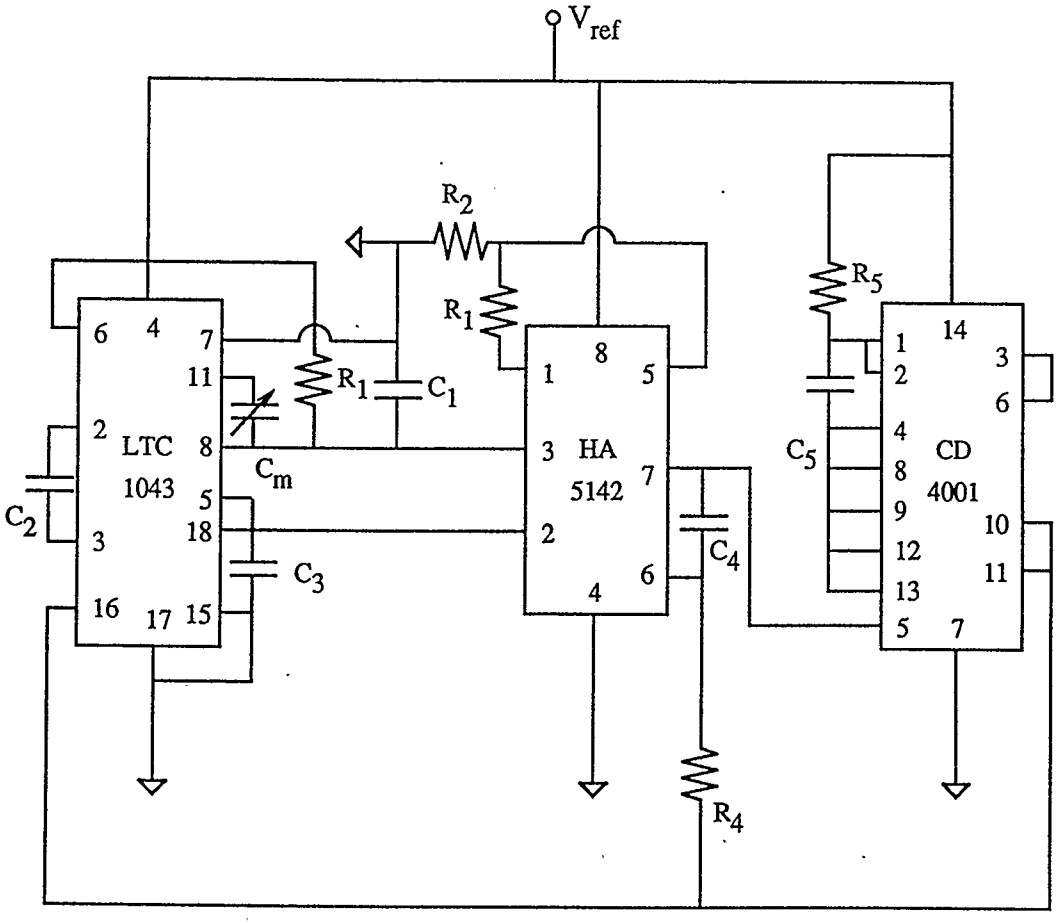


Fig. 3.8 Practical implementation for the R-pumped capacitance-to-frequency converter

Gate Time	Average Frequency (Hz)	Standard Deviation (Hz)	ppm of Average Frequency
100ms	91575.49	0.07	0.76
190ms	91575.30	0.07	0.76
500ms	91575.31	0.06	0.67
800ms	91575.301	0.053	0.57
1.0s	91575.225	0.052	0.57

Table 3.3 *Test Results for R-pumped Converter*

temperature characteristic of capacitor C_m, the temperature characteristic of the output frequency matches the capacitor temperature characteristic very well. It is obvious that the temperature characteristic of this converter is primarily dependent on the capacitor C_m if a high precision low temperature coefficient resistor is selected for resistor R. This conclusion is verified by the curves shown in Fig. 3.9.

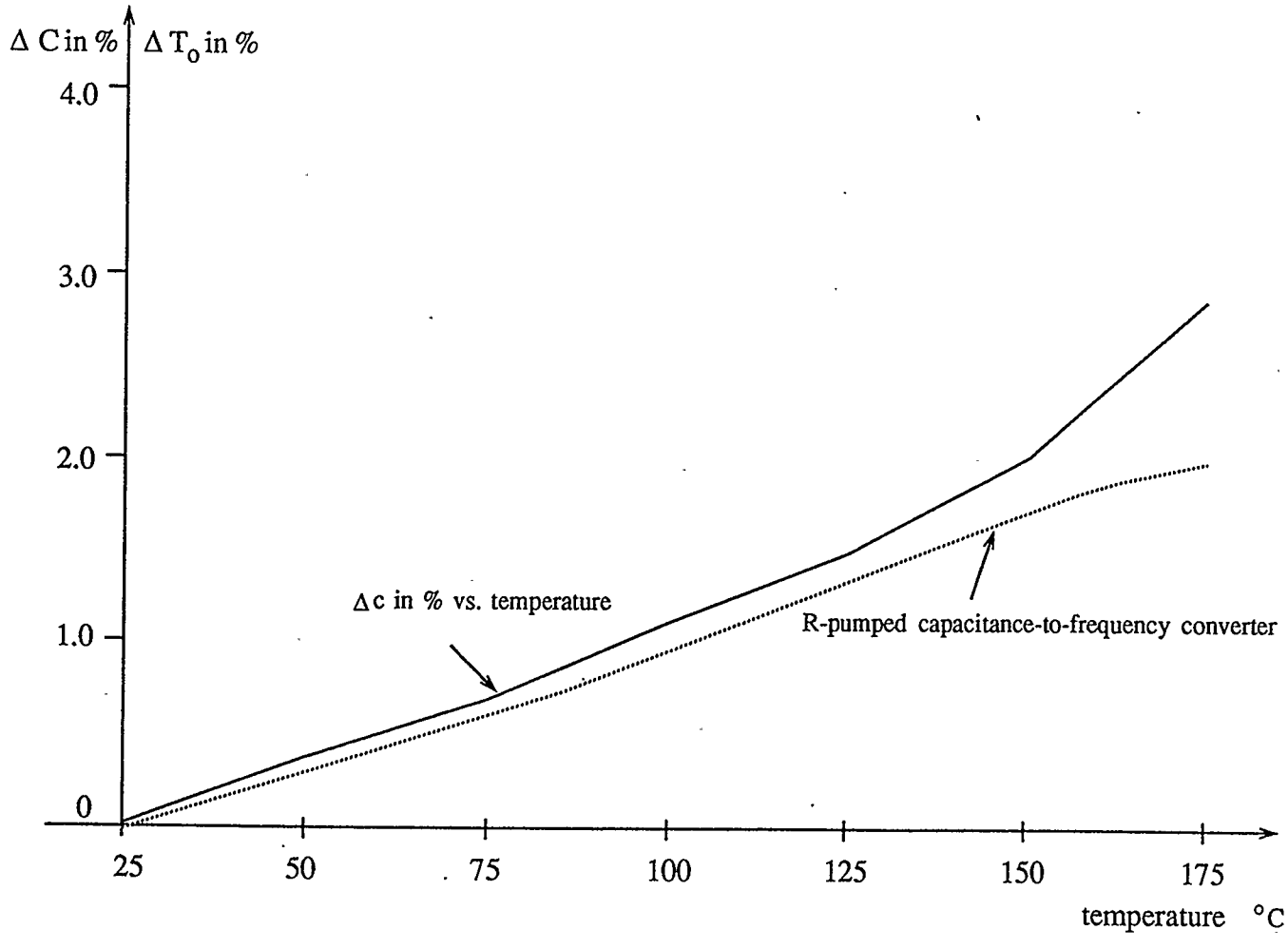


Fig. 3.9 % capacitance change and % period change vs. temperature

Chapter 4

High-Accuracy R-Pumped SC Capacitance-to-Frequency Converter

4.1 Introduction

As mentioned in chapter 3, the R-pumped switched capacitor capacitance-to-frequency converter is useful in the area of instrumentation and measurement. However, this basic conversion circuit has an important disadvantage in that its output frequency is affected by the input offset voltage and input bias currents of op-amp A_1 as shown in Fig. 3.2. It is desirable to reduce the effects of input offset voltage and input bias currents of op-amp A_1 so that a high accuracy capacitance-to-frequency converter can be achieved. The basic conversion circuit discussed in chapter 3 can be modified for this purpose by alternatively interchanging the voltages applied to normal resistor R and the simulated switched capacitor resistor at a frequency which is much lower than the output frequency of the circuit. The technique for implementing such a modified capacitance-to-frequency conversion circuit and a discussion of the operation and performance of the modified circuit are presented in this chapter.

4.2 The Modified Conversion Circuit

The basic conversion circuit discussed in chapter 3 can be modified for the purpose of reducing the influence of input offset voltage and input bias currents of A_1 by adding a binary counter and a D-type flip flop to change the voltage polarity applied to

the input voltage divider consisting of resistor R and a simulated switched capacitor resistor as shown in the schematic diagram of Fig. 4.1. The modified circuit consists of four main parts:

(1) the pulse voltage generator formed by binary counter and D-type flip flop

(2) the half reference voltage generator

(3) the open-loop amplifier

(4) the voltage-to-frequency converter.

Since the last three parts play the same functions as they do in the basic circuit, only the function of the pulse voltage generator is discussed here.

The function of the pulse voltage generator can be described as follows. The output of the circuit V_{out} is fed into the binary counter as a clock frequency so that the output pulse of the counter is a square waveform with a pulse width T which is a multiple of the output oscillation period T_o of the circuit. Therefore,

$$T = m\,T_o \tag{4.1}$$

where the options of $m = 1, 2, 4, ..., 2^{11}$ are available on an MC 14040 12-bit binary counter. The output of the counter is connected to the D input of the D flip flop, while the voltage divider of resistor R and the simulated switched capacitor resistor consisting of two capacitors C_m and C_1 and two switches S_1 and S_2 is connected between the Q terminal and $\overline{Q}$ terminal of the D flip flop. For single-supply operation, all of the circuit components are powered from a single reference voltage V_{ref}, so that the high levels of both Q and $\overline{Q}$ are V_{ref} and the low levels of Q and $\overline{Q}$ are zero. As shown in the timing diagram of Fig. 4.2, when the Q terminal of the D flip flop is

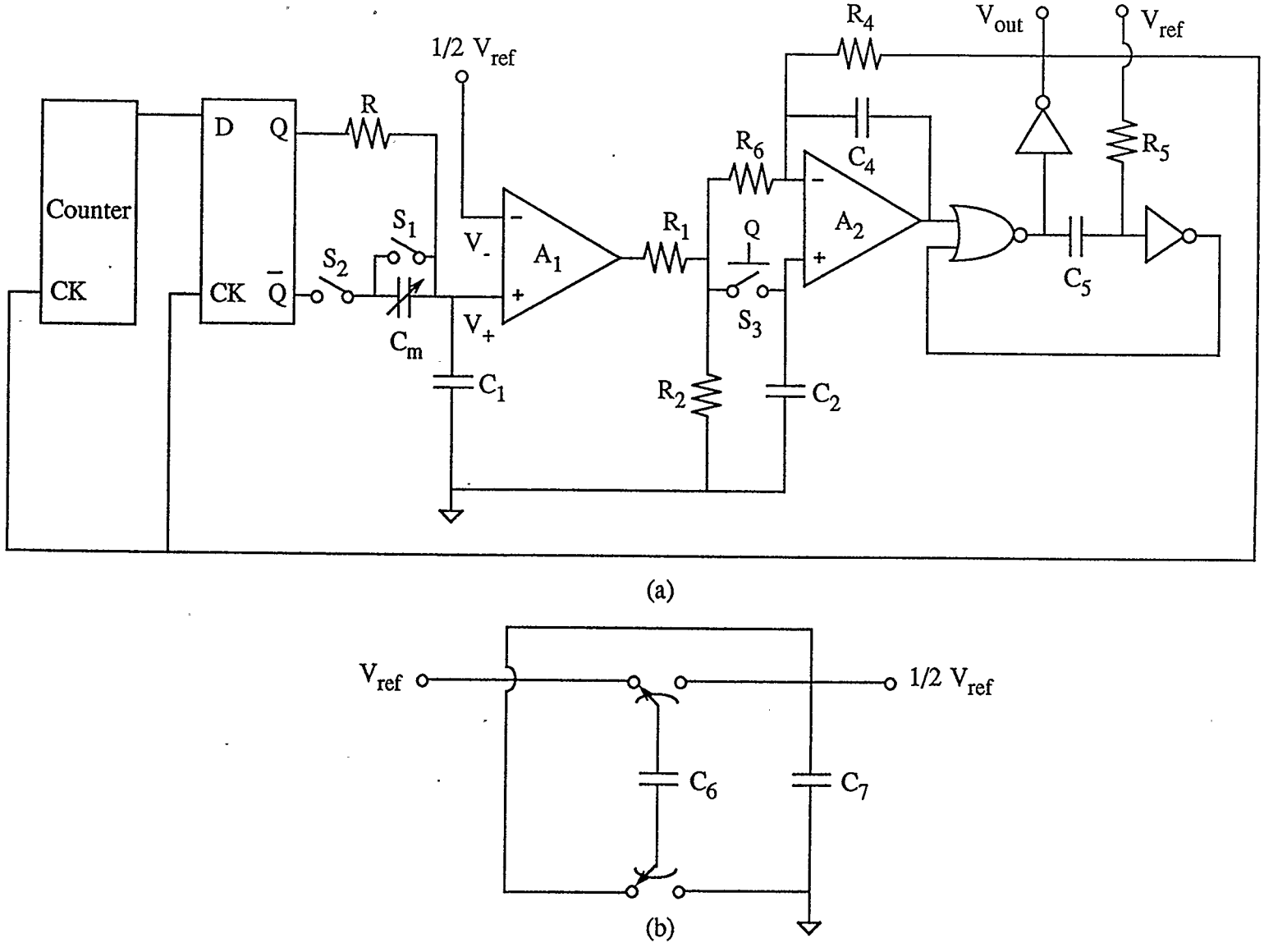


Fig. 4.1 Schematic of modified capacitance-to-frequency converter:
(a) circuit diagram; (b) half reference voltage generator

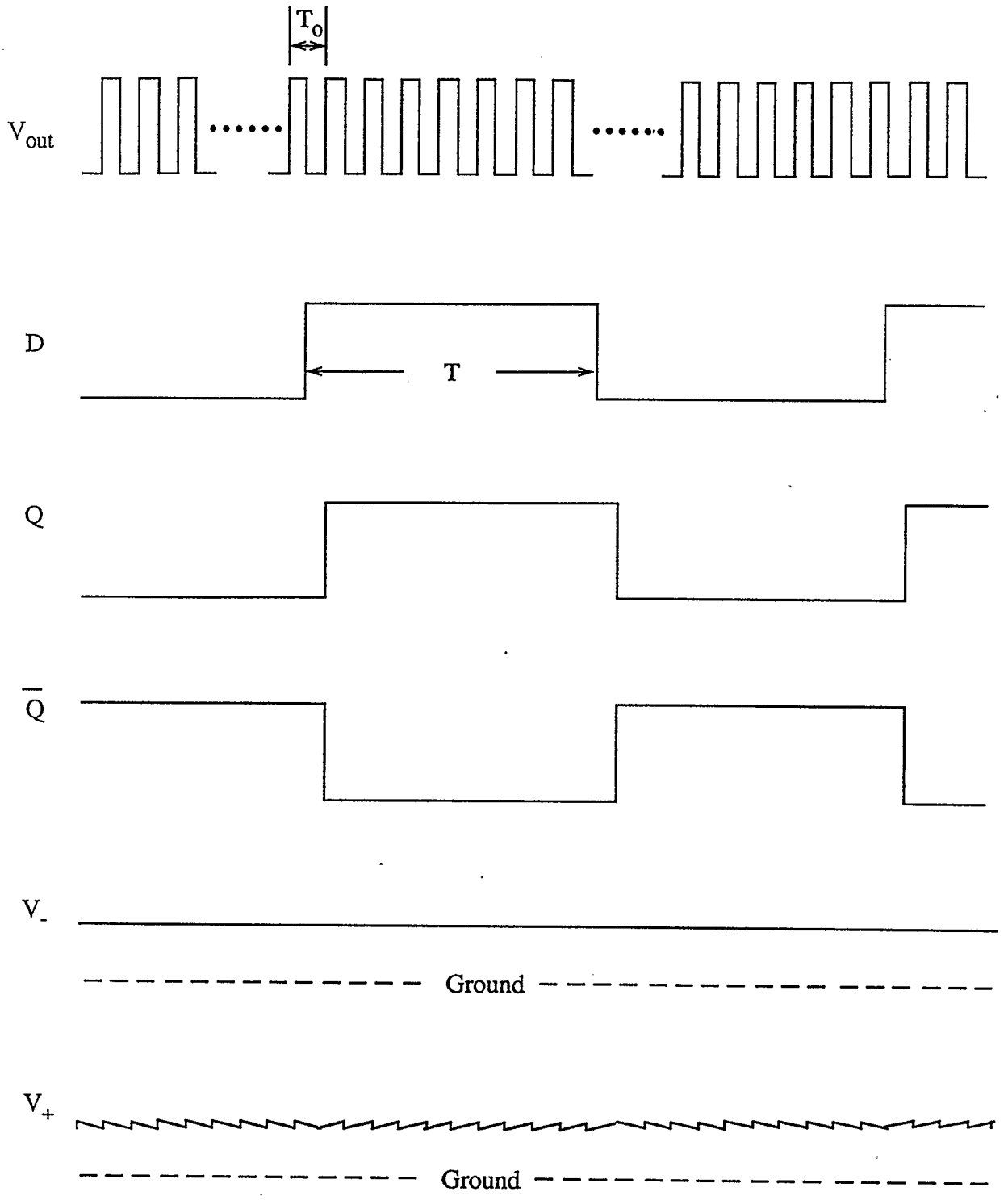
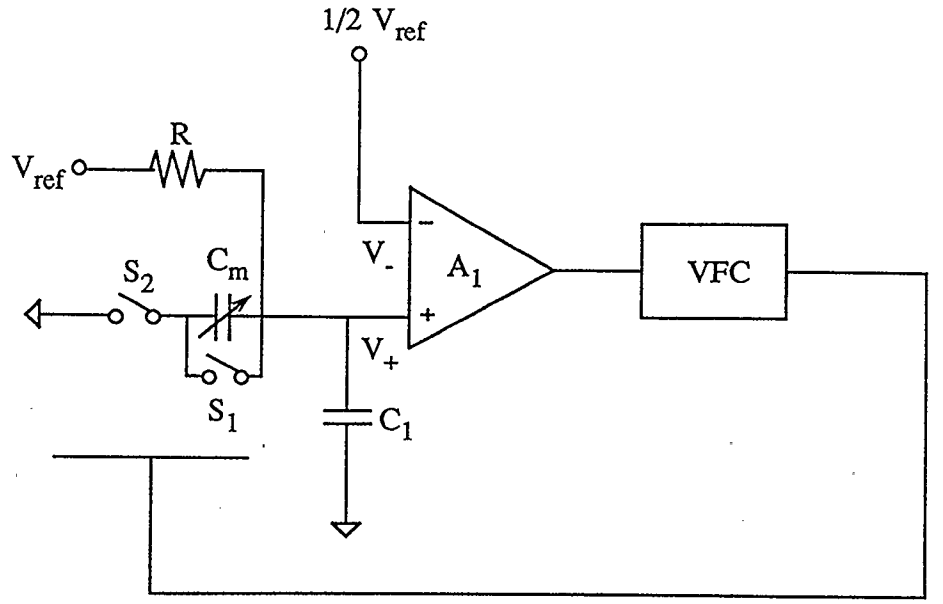


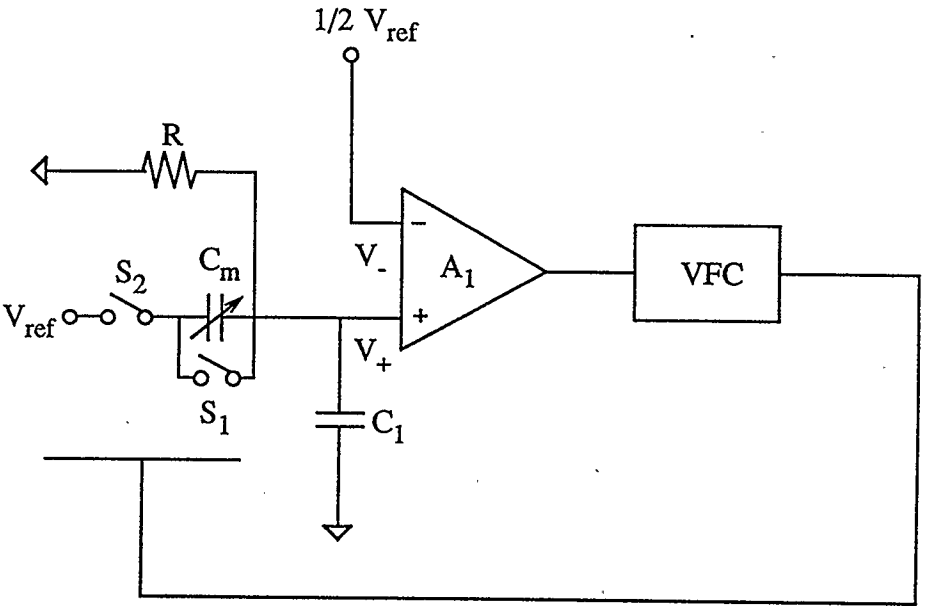
Fig. 4.2 Timing diagram for the modified capacitance-to-frequency conversion circuit

V_{ref} and $\overline{Q}$ is zero, the voltage input into the non-inverting input of the open-loop amplifier A_1 is the voltage across the simulated switched capacitor resistor, while the Q terminal of the D flip flop is zero and $\overline{Q}$ is V_{ref}, the voltage across the resistor R is fed into the non-inverting input of the open-loop amplifier. Because op-amp A_1 is working in an open-loop state, the open-loop gain of A_1 is as large as 120 db, and the differential voltage between the non-inverting input V_+ and inverting input V_- is very small so that it can be assumed to be zero. To simplify the analysis, it is assumed that the capacitance of C_1 is much larger than the capacitance of C_m.

When the potential at the Q terminal of the D flip flop is V_{ref}, and the potential at the $\overline{Q}$ terminal is zero, the conversion circuit diagram appears as shown in Fig. 4.3(a). At this time, the input voltage divider, which consists of a normal resistor R and a switched capacitor simulated resistor, is connected between the Q and $\overline{Q}$ terminals of the D flip flop. Because the input voltage of the voltage divider is generated from the output frequency of the circuit via a division by the binary counter, its frequency is much lower than the output frequency of the circuit. When the output of the circuit goes high, the switch S_1 is open and the switch S_2 is closed. Capacitor C_m acquires charge $Q = C_m V_+$ from charge reservoir C_1, and C_1 is replenished by the current through resistor R. When the output of the circuit turns low, the switch S_2 is opened and switch S_1 is closed. Capacitor C_m will discharge completely through the switch S_1. The output frequency of the circuit when Q is high and $\overline{Q}$ is low can be derived by considering the charge balance for capacitor C_1



(a)



(b)

Fig.4.3 (a) The circuit when Q is high and $\overline{Q}$ is low

(b) The circuit when $\overline{Q}$ is high and Q is low

$$\frac{V_{ref}-V_{+}}{R}-f_{o1}C_m V_{+}-I_{b1}^{+}=0 \tag{4.2}$$

where $V_{+}=\frac{1}{2}V_{ref}-V_{os1}$ for the modified circuit, and V_{os1} is the input offset voltage of op-amp A_1 and I_{b1}^{+} is the input bias current associated with the non-inverting input of op-amp A_1. Thus

$$f_{o1}=\frac{1}{R\,C_m}\frac{\frac{1}{2}V_{ref}-I_{b1}^{+}R+V_{os1}}{\frac{1}{2}V_{ref}-V_{os1}}. \tag{4.3}$$

When the potential at the Q terminal of the D flip flop drops to zero, the potential at the $\overline{Q}$ terminal rises to V_{ref}. Compared with the situation discussed above, the positions of the resistor R and the switched capacitor simulated resistor are interchanged. When the output of the circuit goes high, the switch S_1 is open and the switch S_2 is closed. The capacitor C_1 will acquire charge $Q=(V_{ref}-V_{+})C_m$ from the power supply V_{ref} through the charging of capacitor C_m and C_1, and at the same time, the current flow through resistor R will take away charge from the capacitor C_1. When the output of the circuit turns low, the switch S_2 is open and the switch S_1 is closed, so that the capacitor C_m can discharge through switch S_2. The charge balance for C_1 can be written as

$$(V_{ref}-V_{+})C_m f_{o2}-\frac{V_{+}}{R}-I_{b1}^{+}=0. \tag{4.4}$$

Therefore, the output frequency for the case when Q is low and $\overline{Q}$ is high can be expressed as

$$f_{o2} = \frac{1}{R\,C_m}\,\frac{\frac{1}{2}V_{ref} - V_{os1} + I_{b1}^{+}R}{\frac{1}{2}V_{ref} + V_{os1}}. \tag{4.5}$$

Eq.(4.3) and Eq.(4.5) indicate that the output frequency f_{o1} is a little higher than the output frequency for the ideal case where the effects of input offset voltage and input bias currents of op-amp A_1 are ignored and that the output frequency f_{o2} is a little lower than the output frequency of the ideal case. It is possible to partly cancel the error caused by the input offset voltage and input bias currents of A_1 by averaging the output frequency in time interval of measurement $t = 2nT$. Therefore, the average output frequency is

$$f_{ave} = \frac{n\,(f_{o1}+f_{o2})}{2n} = \frac{1}{R\,C_m}\left(1 + \frac{2V_{os1}^2 - I_{b1}^{+}R\,V_{os1}}{\frac{1}{4}V_{ref}^2 - V_{os1}^2}\right) \tag{4.6}$$

Comparing the output frequency obtained from Eq.(4.6) with the output frequency of Eq.(3.28), it is easy to observe that the influence of op-amp nonidealities on the output frequency is greatly reduced in the modified conversion circuit. For example, if the power supply is 5 volts, and the input offset voltage V_{os1} and input bias current I_{b1}^{+} are the same as those in chapter 3, i.e., V_{os1} is 2.5 millivolts, I_{b1}^{+} is 100pa, and R is 100 $k\,\Omega$, the total error introduced by these amplifier nonidealities is equal to 3.2×10^{-10} percent of full scale, which is approximately equal to the square of the error of the basic conversion circuit.

4.3 The Negative Feedback Configuration

As discussed in chapter 3, the basic conversion circuit has a negative feedback loop so that the characteristics of the circuit can be greatly improved. For the modified conversion circuit, since the two switches S_1 and S_2 are controlled by the output frequency, there still exists a feedback loop. However, to ensure the feedback is negative feedback rather than positive feedback when the polarity of the pulse voltage connected to the input voltage divider changes alternatively , a new branch consisting of switch S_3, capacitor C_2 and resistor R_6 has to be added. In this section, the operation of the negative feedback loop in the conversion circuit without the new branch of switch S_3, capacitor C_2 and resistor R_6 will be investigated first, then the operation of the voltage-to-frequency converter with the new branch will be analyzed to show how the modified circuit assures that the feedback is negative rather than positive.

Suppose that in the circuit shown in Fig. 4.1, the potential at the Q terminal of the D flip flop is V_{ref} and the potential at the $\overline{Q}$ terminal is zero. If at time $t = t_o$ the output frequency suddenly increases due to external interference or internal noise, the rise of output frequency will be fed back to the input voltage divider and will cause the rate of switching of S_1 and S_2 to increase so that more charge will be taken away from capacitor C_1. This will cause the potential at the non-inverting input of A_1 to drop slightly and cause the output voltage of op-amp A_1, which is fed into the voltage-to-frequency converter as an input voltage, to decrease to a new value which tends to decrease the output frequency and to restore the output frequency at time $t = t_o$. It can be seen that the function of the feedback configuration is opposite to the

action of external interference and internal noise so the feedback is negative feedback.

When the potential at the Q terminal drops to zero and the potential at the $\overline{Q}$ terminal rises to V_{ref}, the position of the resistor R and the simulated switched capacitor resistor are interchanged. If the external interference and internal noise causes a sudden increase in the output frequency, this will cause the rate of switching of S_1 and S_2 to increase. Therefore, the capacitor C_1 would acquire more charge from the power supply V_{ref} causing the potential at the non-inverting input of A_1 to rise slightly and the output of op-amp A_1 to raise to a new value which will tend to increase the output frequency. Obviously, in this case the feedback is positive instead of negative, and that is undesirable in the conversion circuit. This problem can be corrected by making a modification in the voltage-to-frequency converter circuit so that its output frequency will decrease when its input voltage increases.

A voltage-to-frequency converter with the characteristic that its output frequency increases with increasing input voltage when the potential at the Q output is high and that its output frequency decreases when the input voltage decreases when the potential at the Q output is low can be constructed as follows. When the potential at the Q terminal is V_{ref} and that at the $\overline{Q}$ terminal is zero, the switch S_3, which is controlled by the D flip flop, is closed. The resistor R_6 is shorted because both of its two ends have the same potential. The equivalent circuit for this case can be reproduced as shown in Fig. 4.4(a). If at this time the input voltage of the voltage-to-frequency converter is V_{t_1}, the output frequency of the voltage-to-frequency converter, which is the same as that discussed in the basic R-pumped conversion circuit of chapter 3, can be expressed as

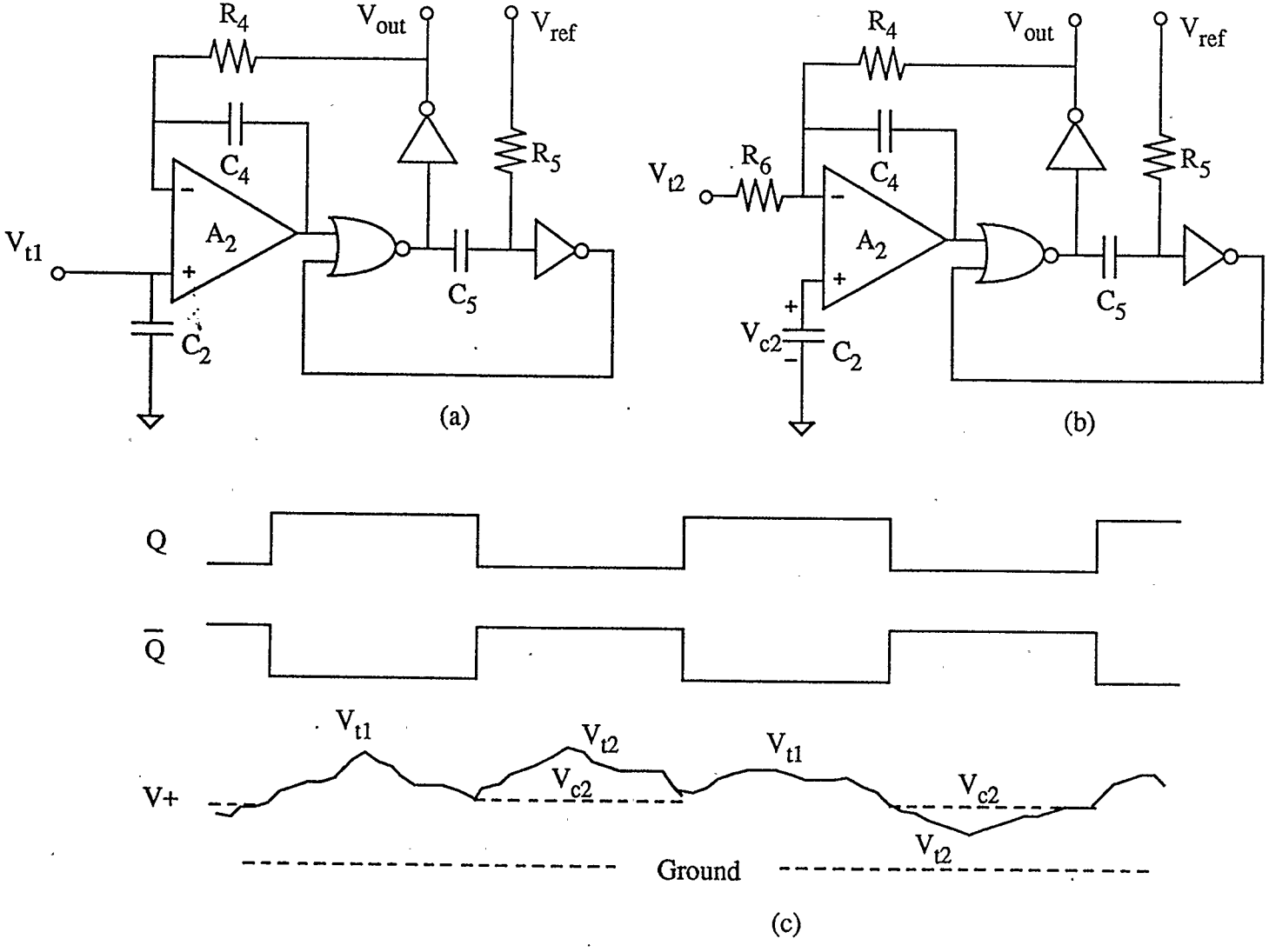


Fig.4.4 (a) The VFC circuit when Q is high (b) The VFC circuit when Q is low
(c) The waveforms for the modified circuit

$$f_{o1_{vfc}} = \frac{V_{t_1}}{V_{ref}\, T_p} \tag{4.7}$$

since the output frequency of the voltage-to-frequency converter is proportional to the input voltage V_{t_1}, it can satisfy the requirement for negative feedback in the modified conversion circuit.

When the potential at the Q terminal becomes zero and that at the $\overline{Q}$ terminal turns to be V_{ref}, the switch S_3 is opened. As shown in the equivalent circuit of Fig. 4.4(b), the capacitor C_2 holds the input voltage V_{t_1} of the time just before the potential at Q turns low and the input voltage V_{t_2} is input into the inverting input of op-amp A_1 through the resistor R_6. It is assumed that the input voltage is V_{t_2}, the voltage across the capacitor C_2 is $V_{t_1}^{'}$ and the voltage difference between V_{t_2} and $V_{t_1}^{'}$ is $\Delta V = V_{t_2} - V_{t_1}^{'}$, then a charge balance for capacitor C_2 can be written as

$$\frac{\Delta V}{R_4} T_o - \frac{V_{t_1}^{'}}{R_4} T_o + \frac{V_{ref}}{R_4} T_p = 0, \tag{4.8}$$

so that the output frequency is

$$f_{o2_{vfc}} = \frac{V_{t_1}^{'} - \Delta V}{V_{ref}\, T_p}. \tag{4.9}$$

It can be seen from Eq.(4.8) that when the potential at Q is low and that at $\overline{Q}$ is high the output frequency f_o will decrease if input voltage V_{t_2} is larger than the voltage across the capacitor C_2, $V_{t_1}^{'}$ so that the requirement for negative feedback is satisfied. From the above analysis, it can be concluded that the basic voltage-to-frequency con-

verter with this modification guarantees that the feedback is negative at all times.

4.4 Implementation and Testing

A prototype high-accuracy R-pumped converter was implemented by using discrete components to confirm the principle of operation. The operational amplifier and switches used were HA5142 and LTC1043, respectively. CMOS chips MC14040 and MC14013 were used for the binary counter and the D-type flip-flop, respectively, and transmission gate MC14066 was selected for switch S_6. Capacitors C_1, C_6 and C_7 were chosen to be 0.1 μF. A high temperature capacitor of 100pF with temperature coefficient of 140ppm ± 25ppm per Celsius degree was chosen for capacitor C_m, and a high precision low temperature coefficient ($-1.8 \pm 2.3\ ppm/^{o}C$) resistor of 100 $k\,\Omega$ was chosen for resistor R. A single power supply V_{ref} was set to be 5.0 volts.

The stability of the prototype circuit was tested at a constant temperature of 27 degrees Celsius by using an HP 5316 universal counter. The measurement data taken at different gate times are listed in Table 4.1. Compared with the test results of the basic R-pumped converter, the ppm standard deviations of average frequency are much larger. The reason is that the output frequency of the high accuracy converter has to be

Gate Time	Average Frequency (HZ)	Standard Deviation (HZ)	ppm of Average Frequency
100ms	90624.63	1.51	16.61
1.0s	90624.621	0.832	9.22
5.0s	90624.621	0.546	6.03

Table 4.1 *Test Results for High Accuracy R-pumped Converter*

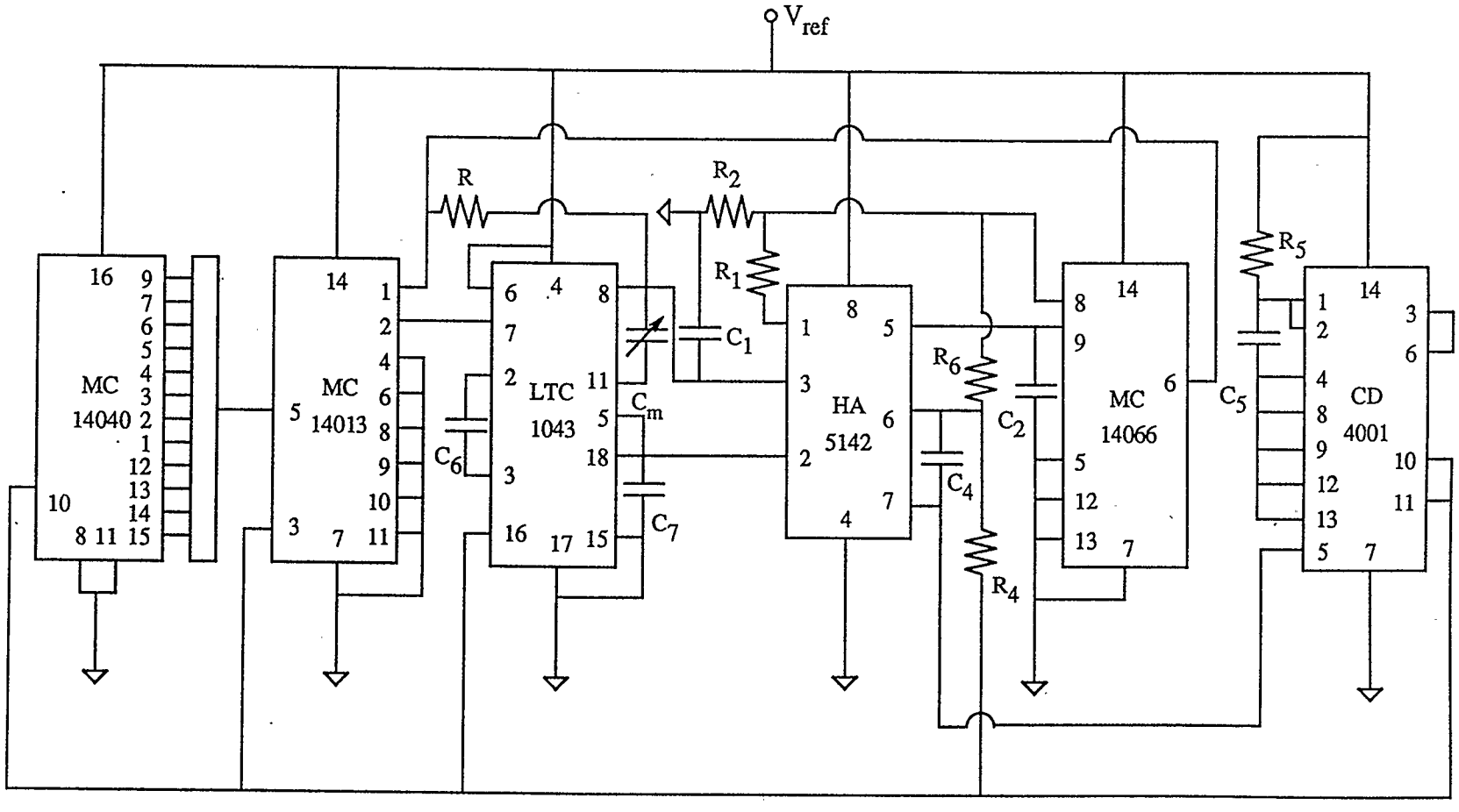


Fig. 4.5 Practical implementation for the modified R-pumped capacitance-to-frequency converter

changed to eliminate the effect of input offset voltage V_{os} so that the output frequency is not as stable as the basic R-pumped converter.

The temperature characteristic of the prototype circuit was tested at different temperature in the range from 25 degrees Celsius to 175 degrees Celsius. The test results are plotted in Fig. 4.6, and the test results are the same as that of the basic R-pumped converter except that the gap between the two curves is smaller than that of Fig. 3.9.

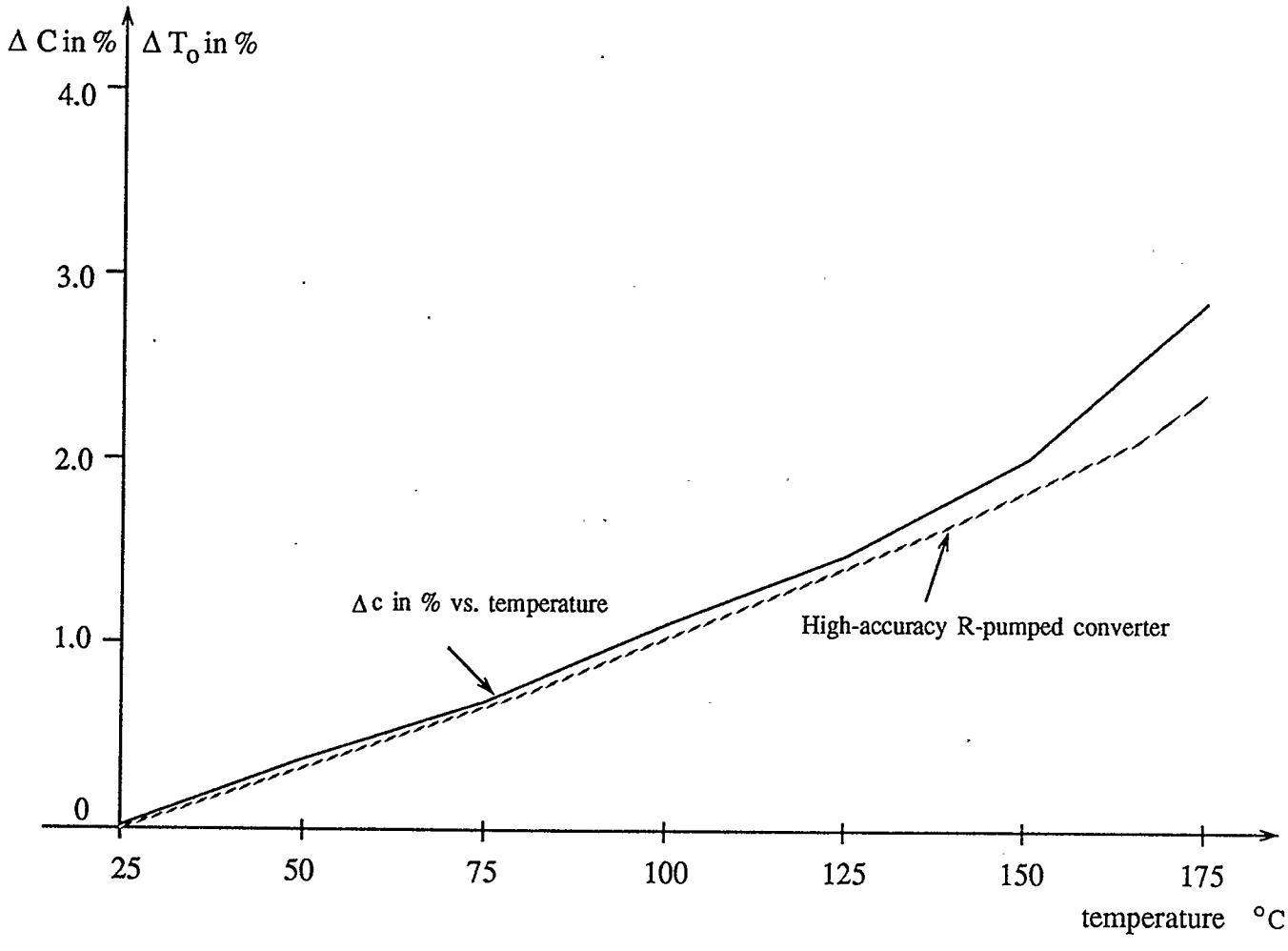


Fig. 4.6 % capacitance change and % period change vs. temperature

Chapter 5

Two-Capacitor Pumped SC

Capacitance-to-Frequency Converter

5.1 Introduction

A circuit which can compare the capacitance under measurement to a standard capacitance is very useful in the capacitive sensor system. This chapter discusses a novel two-capacitor pumped switched capacitor capacitance-to-frequency conversion circuit which can be used to measure the capacitance ratio of two capacitors of which one is the capacitor to be measured and the other is a standard capacitor. Unlike the R-pumped switched capacitor capacitance-to-frequency converter discussed in chapter 3, this circuit can generate an output with a frequency which is proportional to the capacitance of the capacitor under measurement and the clock frequency and is inversely proportional to the capacitance of the standard capacitor.

The basic two-capacitor pumped switched capacitor capacitance-to-frequency conversion circuit consists of the capacitor to be measured, C_m, a standard capacitor, C_s, four MOS switches, a large capacitor C_1 which is used as a charge reservoir, a high-gain open-loop amplifier A_1 and a voltage-to-frequency converter which is the same as that used in the R-pumped conversion circuit. The rate at which the measured capacitor is switched is controlled by a crystal clock and the rate at which the standard capacitor must be switched is controlled by the output frequency to indicate the ratio

of the two capacitors. If the same clock is used to measure the output frequency, the measurement system will be independent of the clock frequency. Furthermore, the basic circuit can be modified by adding another two MOS switches and a second standard capacitor to offset the value of the capacitor to be measured in order to enhance capacitance changes.

5.2 The Basic Circuit Configuration

The basic two-capacitor pumped conversion circuit is shown in Fig. 5.1. It is similar to the R-pumped switched capacitor conversion circuit except that the resistor R in the R-pumped circuit is replaced by a switched capacitor simulated resistor formed by the capacitor to be measured, C_m, switch S_1 and switch S_2 and that a standard capacitor, C_s, is used with switches S_3 and S_4 to form another simulated resistor. An external clock frequency f_c is introduced to control the switching of capacitor C_m and the output frequency f_o is used to control the switching of capacitor C_s in this circuit.

The operation of the basic two-capacitor pumped conversion circuit can be described as follows. As shown in Fig. 5.2, when the f_c clock frequency waveform goes high, switch S_1 is closed and switch S_2 is opened and when the f_c waveform turns low, switch S_2 is opened and switch S_1 is closed. The switching of capacitor C_m pumps charge of amount $(V_{ref} - V_+)C_m$ into capacitor C_1 where V_+ is the potential at the non-inverting input of A_1. At the positive-edge of the output V_{out}, switch S_3 is closed and switch S_4 is opened and at the negative-edge of V_{out}, switch S_4 is closed and switch S_3 is opened. The switching of capacitor C_s takes away charge equal to

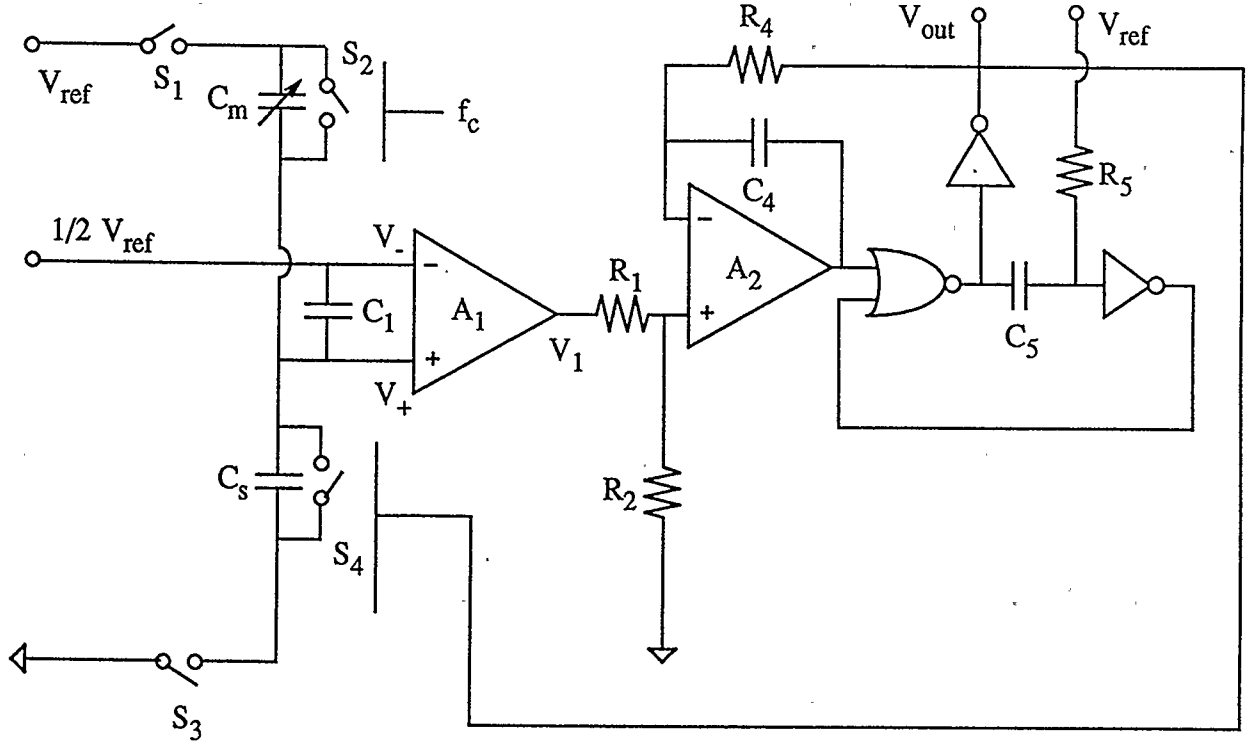


Fig. 5.1 Schematic diagram of the two-capacitor pumped capacitance-to-frequency conversion circuit

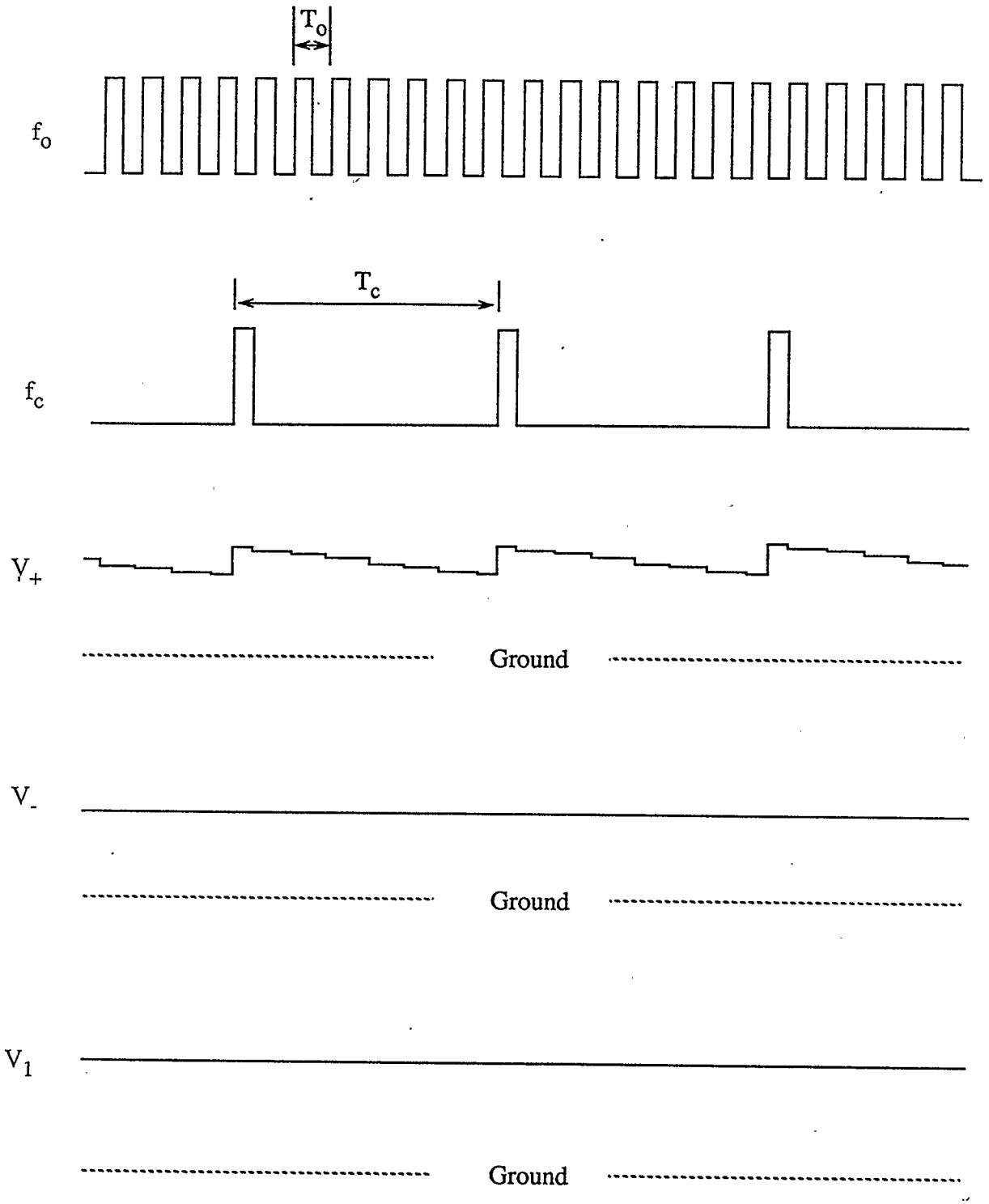


Fig. 5.2 Timing diagram of the two-capacitor pumped capacitance-to-frequency conversion circuit

$V_+ C_s$ from the capacitor C_1.

For the ideal case, i.e., the effects of the nonidealities such as the input offset voltage, V_{os}, of operational amplifier A_1, input bias currents I_b^+ and I_b^- of A_1, the parasitic capacitor from the non-inverting input terminal of A_1 to ground can be ignored and the potential at the non-inverting input of A_1 can be considered to be $\frac{1}{2} V_{ref}$. In one second, the total charge pumped into capacitor C_1 by the switching of C_m is $\frac{1}{2} V_{ref}\, C_m f_c$ and the charge taken away from capacitor C_1 by the switching of capacitor C_s is $\frac{1}{2} V_{ref}\, C_s f_o$. By considering charge balance for capacitor C_1, the total charge pumped into large capacitor C_1 by the switching of capacitor C_m and by the switching of capacitor C_s should be zero. Therefore, it follows that

$$\frac{1}{2} V_{ref}\, C_m f_c - \frac{1}{2} V_{ref}\, C_s f_o = 0. \tag{5.1}$$

The output frequency of this circuit can be obtained from the above equation and can be expressed as

$$f_o = f_c \frac{C_m}{C_s}. \tag{5.2}$$

It can be seen that the output frequency of this circuit is only proportional to the clock frequency f_c and to the capacitance ratio C_m to C_s. If the f_c clock is used to measure the output frequency, the measurement system will be independent of the clock frequency.

5.3 Effects of Nonidealities

As for the R-pumped capacitance-to-frequency converter, the output frequency of the two-capacitor pumped capacitance-to-frequency conversion circuit is affected by component nonidealities. Referring to Fig. 5.1, both of the operational amplifiers have input offset voltages and input bias currents, and the gains of the operational amplifiers are frequency-dependent. The capacitance of capacitor C_1 is not infinite, and the capacitance to be measured is a three-terminal capacitor with two plate-to-ground stray capacitances. Only the effects of input offset voltage V_{os}, input bias currents I_b^+ and I_b^- and the size of capacitor C_1 will be analyzed in the following section.

5.3.1 The Effects of Amplifier Nonidealities

The amplifier nonidealities, such as the input offset voltage V_{os} and input bias currents I_b^+ and I_b^- can introduce some errors in the output frequency of this circuit. However, because the operational amplifier A_2 is enclosed in the negative feed-back loop, the error caused by the input offset voltage V_{os2} and input bias currents I_{b2}^+ and I_{b2}^- is negligible. The effects of the input offset voltage V_{os1} and input bias currents I_{b1}^+, I_{b1}^- are considered as follows.

If it is assumed that the size of capacitor C_1 is much larger than that of the capacitor C_m and C_s, the potential at the non-inverting terminal of A_1 can be considered to be constant. Each time the clock waveform f_c goes high, the capacitor C_1 receives charge through capacitor C_m from power supply V_{ref}, which is equal to

$(V_{ref}-V_+)C_m$, and each time the f_o waveform turns high, the charge taken away from capacitor C_1 by the switching of capacitor C_s is equal to V_+C_s. If charge balance is considered for capacitor C_1, it follows that

$$(V_{ref}-V_+)f_c\,C_m - I_{b1}^+ = V_+C_s f_o\,. \tag{5.3}$$

By substituting $V_+ = \frac{1}{2}V_{ref} - V_{os1}$ into the above equation, the output frequency f_o can be shown to be

$$f_o = f_c\,\frac{C_m}{C_s}\left(1+\frac{2V_{os1}}{\frac{1}{2}V_{ref}-V_{os1}}\right) - \frac{I_{b1}^+}{(\frac{1}{2}V_{ref}-V_{os1})C_s}\,. \tag{5.4}$$

It is noted that the output frequency is affected not only by the input offset voltage V_{os1}, but by the input bias current I_{b1}^+ as well. The term $\dfrac{2V_{os1}}{\frac{1}{2}V_{ref}-V_{os1}}$ is very small. For example, if V_{os1} = 2.5 microvolts, V_{ref} = 5 volts, $\dfrac{2V_{os1}}{\frac{1}{2}V_{ref}-V_{os1}}$ is only 0.000002, so that the error caused by input offset voltage V_{os1} is relatively small. The second term in Eq.(5.4) is error introduced by the bias current I_{b1}^+. If it is assumed that $C_m = 100$ pF and $I_{b1}^+ = 100$ nA, the second term in Eq.(5.4) is equal to 400 Hz. If the output frequency f_o is about 100 kHz, the error caused by the bias current I_{b1}^+ is about 0.4%, which is much larger than the error introduced by the offset voltage V_{os1}.

5.3.2 The Effects of the Size of Capacitor C_1

The size of the capacitor C_1 contributes an error in the output frequency f_o. Assuming that the operational amplifier A_1 is ideal, i.e., the input offset voltage and input bias currents are zero, the effect of capacitor C_1 can be analyzed by using the charge balance principle.

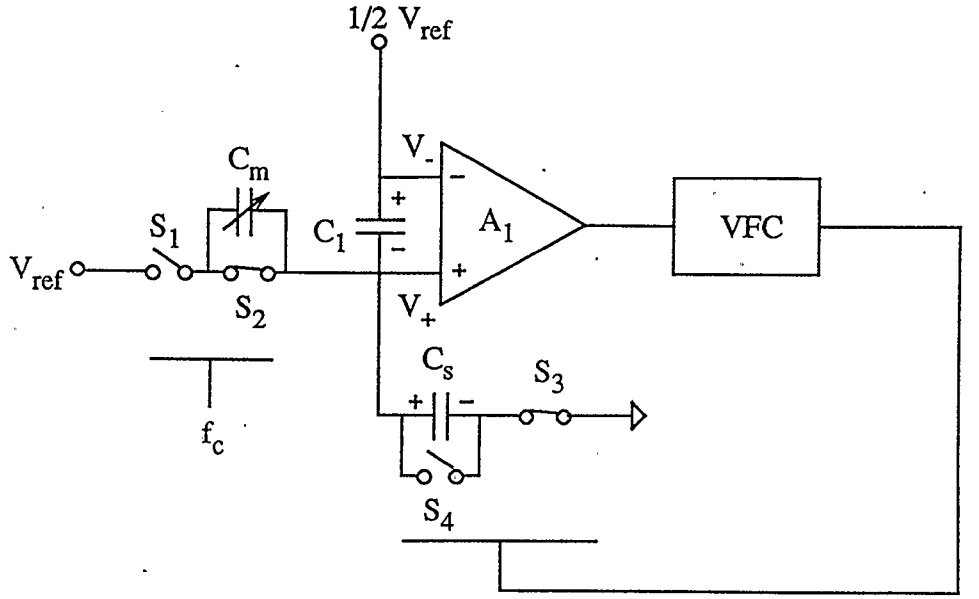
As shown in the Fig. 5.3, assume the f_c clock waveform is low so that switch S_1 is opened and switch S_2 is closed. At the time when V_{out} turns high, switch S_4 is opened, and switch S_3 is closed. If the capacitor voltages of the two capacitors C_1 and C_s are assumed zero, a charge balance equation for a closed surface which is passed between the bottom plate of C_1 and the top plate of C_s in such a way that it is not crossed by any conductors can be written as

$$V_+ C_s + (V_+ - \frac{1}{2} V_{ref}) C_1 = 0 \tag{5.5}$$

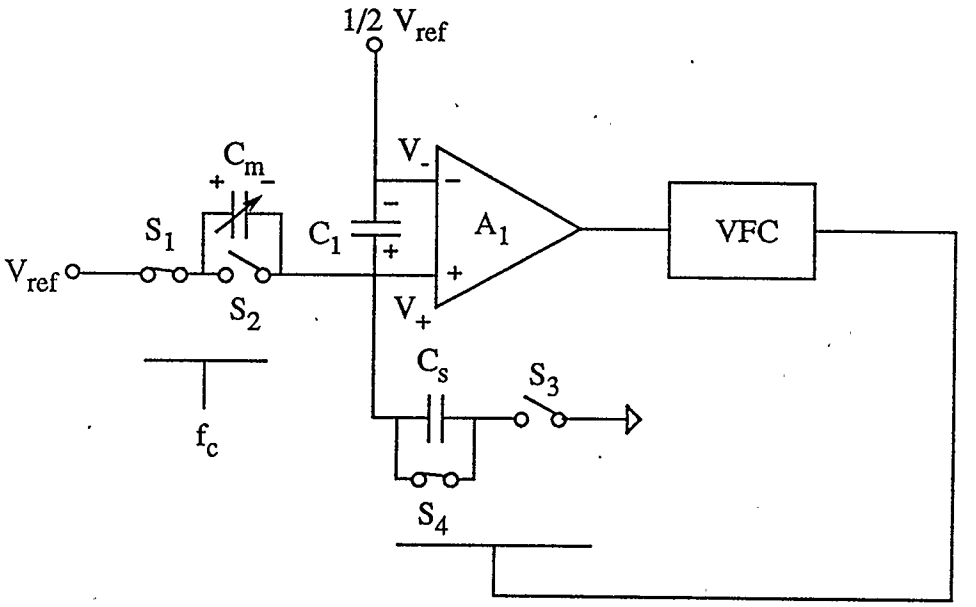
where V_+ is the potential at the non-inverting terminal of A_1. V_+ can be obtained by solving above equation, and the result is of the form

$$V_+ = \frac{1}{2} V_{ref} \frac{C_1}{C_1 + C_s}. \tag{5.6}$$

The charge stored on the bottom plate of C_1 is $-\frac{1}{2} V_{ref} \frac{C_1 C_s}{C_1 + Cs}$ and the charge stored on the top plate of capacitor C_s is $+\frac{1}{2} V_{ref} \frac{C_1 C_s}{C_1 + Cs}$, as shown in Fig. 5.3. At the negative edge of V_{out}, switch S_4 is closed so that the charge stored on the top plate of C_s is transferred through switch S_4 to the bottom plate of C_s resulting in



(a)



(b)

Fig.5.3 (a) The circuit when the f_o waveform is high and the f_c waveform is low

(b) The circuit when the f_o waveform is low and the f_c waveform is high

these two kinds of charge cancelling each other out so that the voltage across capacitor C_s changes to zero. In the meantime, the charge stored on both of the two plates of the capacitor C_1 remains fixed as long as V_{out} remains low. When the positive edge of V_{out} appears, the switches changes their states, i.e., S_4 is opened and S_3 is closed. Capacitors C_1 and C_s are charged from the power supply V_{ref}, and the charge balance equation for the same closed surface as above gives

$$V_+ C_s + (V_+ - \frac{1}{2} V_{ref}) C_1 = q_1 \tag{5.7}$$

where q_1 is the charge accumulated on the bottom plate of capacitor C_1 before the switches change their states, and is equal to $-\frac{1}{2} V_{ref} \frac{C_1 C_s}{C_1 + C_s}$. This time the total charge stored on the bottom plate of C_1, q_2, can be found by substituting V_+ which is obtained from Eq.(5.7) into the following equation.

$$q_2 = (V_+ - \frac{1}{2} V_{ref}) C_1$$

$$= -\frac{1}{2} V_{ref} \frac{C_1 C_s}{C_1 + C_s} - \frac{1}{2} V_{ref} \frac{C_1 C_s}{C_1 + C_s} \frac{C_1}{C_1 + C_s}. \tag{5.8}$$

It can be seen from Eq.(5.8) that the charge accumulated on the bottom plate of C_1 contains two parts. The first part is the new charge obtained from the present switching of capacitor C_s, while the second part comes from the redistribution of the old charge stored on the bottom plate of C_1 before the present switching of capacitor C_s. In the charge redistribution, a small portion of the charge stored on the bottom plate of C_1 is taken away by the capacitor C_s, and therefore, the second term of Eq.(5.8) is multi-

plied by a factor $\frac{C_1}{C_1+C_s}$ which is dependent on the ratio of $\frac{C_1}{C_s}$ and is less than 1.0. Therefore, after every switching of capacitor C_s, the total charge stored on the bottom plate of C_1 is the sum of the new charge obtained from the present switching and the old charge before the present switching multiplied by factor $\frac{C_1}{C_1+C_s}$.

In order to simplify the analysis, it is assumed that the capacitance ratio $\frac{C_m}{C_s}$ is an integer. After $\frac{C_m}{C_s}$ switching cycles of capacitor C_s, the total charge stored on the bottom plate of C_1, $q_{c_1}^-$, is given by

$$q_{c_1}^- = -\frac{1}{2} V_{ref}\, C_s \left[\frac{C_1}{C_1+C_s} + \left(\frac{C_1}{C_1+C_s}\right)^2 + \ldots\ldots + \left(\frac{C_1}{C_1+C_s}\right)^{\frac{C_m}{C_s}}\right]. \qquad (5.9)$$

When the f_c clock waveform turns high, switch S_1 is closed and switch S_2 is opened. Capacitor C_1 obtains some charge from the power supply through the capacitor C_m. As shown in Fig.5.3, this time the charge received by the bottom plate of capacitor C_1 is positive charge which is opposite to the charge obtained by the switching of capacitor C_s. The charge received by capacitor C_1 when f_c is high is

$$q_{c_1}^+ = \frac{1}{2} V_{ref}\, \frac{C_1 C_m}{C_1+C_m}. \qquad (5.10)$$

By considering charge balance for the closed surface,

$$\frac{1}{2} V_{ref}\, \frac{C_1 C_m}{C_1+C_m} = \frac{1}{2} V_{ref}\, C_s \left[\frac{C_1}{C_1+C_s} + \left(\frac{C_1}{C_1+C_s}\right)^2 + \ldots\ldots + \left(\frac{C_1}{C_1+C_s}\right)^{\frac{C_m}{C_s}}\right]. \qquad (5.11)$$

From Eq.(5.11), the output frequency f_o for the case where the effect of the size of capacitor C_1 is considered can be expressed as

$$f_o = k f_c \frac{C_m}{C_s} \tag{5.12}$$

where the factor k is

$$k = \frac{\frac{C_m}{C_s}}{\frac{C_1+C_m}{C_s}\left[1-\left(\frac{C_1}{C_1+C_s}\right)^{\frac{C_m}{C_s}}\right]}. \tag{5.13}$$

Compared with the output frequency for the ideal case, there is a factor k in Eq.(5.12), and it is dependent on the capacitance ratio C_1/C_m and capacitance ratio C_m/C_s. The relationship of factor k to the capacitance ratio C_m/C_s for different capacitance ratios C_1/C_m is plotted in Fig. 5.4. Fig.5.4 indicates that the larger the capacitance ratio C_1/C_m, the smaller the difference between the factor k and 1.0 and the closer the capacitance ratio C_m/C_s approach 1, the smaller the difference between factor k and 1.0. Therefore, to reduce the error, the capacitance ratio C_1/C_m has to be chosen as large as possible.

5.4 Modification of the Basic Circuit

As seen in the discussion of the effects of capacitor C_1, the capacitance variation of the capacitor C_m can not be very large, because the error in the output frequency will increase with an increase of the capacitance ratio C_m/C_s. The basic circuit can be modified by adding a second standard capacitor C_r and two other switches S_5 and S_6

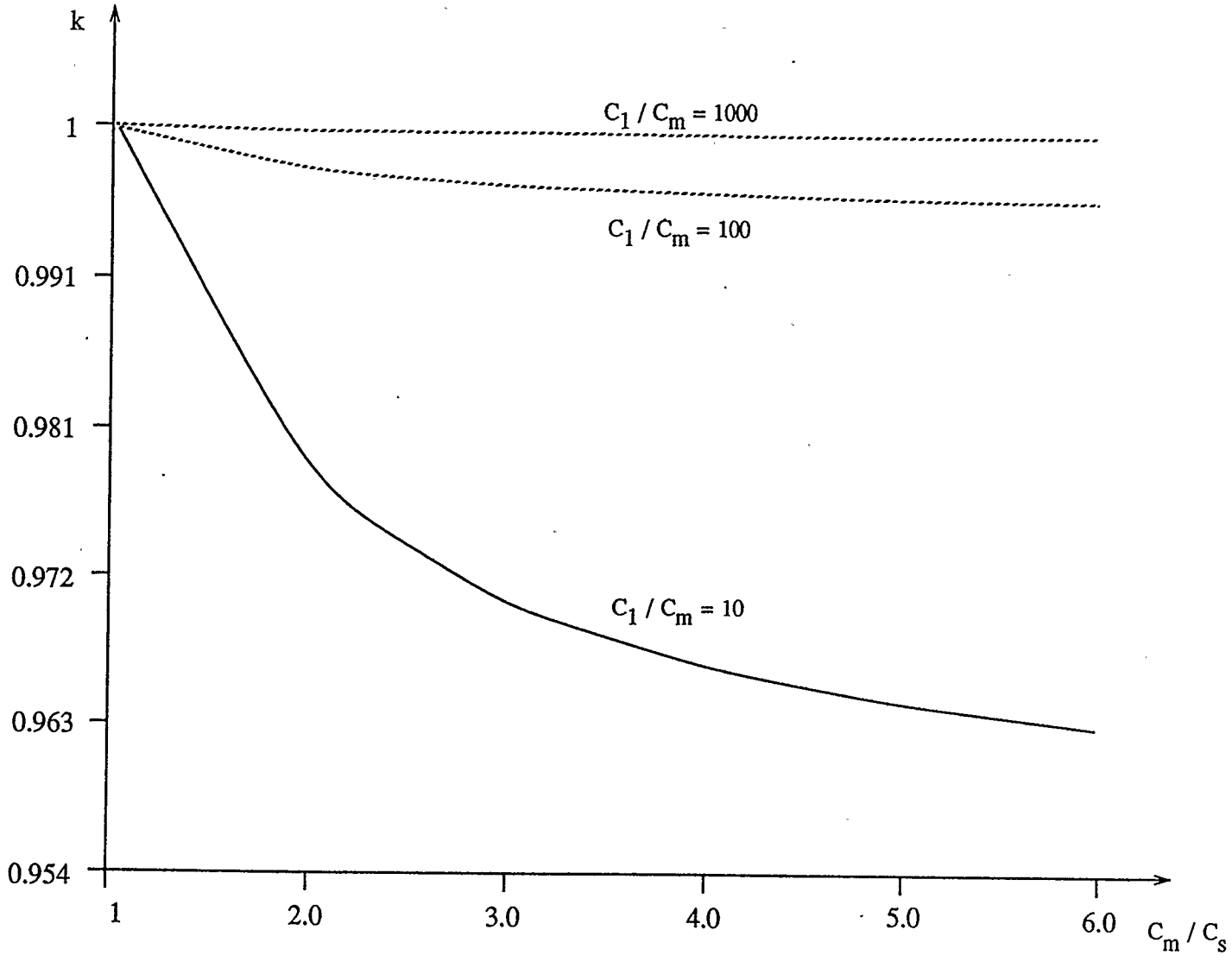


Fig. 5.4 The relationship between factor k and the capacitance ratio C_m / C_s for different capacitance ratios C_1 / C_m

to offset the value of capacitor C_m for the purpose of enhancing capacitance changes and reducing the output frequency error. In the modified circuit shown in Fig. 5.5, the switching of the capacitor C_r is controlled by the clock frequency f_c. Every time when the f_c clock waveform goes high, the switching of capacitor C_m and capacitor C_r pumps charge of amount $(V_{ref} - V_+)C_m - V_+ C_r$ into capacitor C_1 and every time when the output of this circuit V_{out} turns high, the switching of capacitor C_s removes charge of amount $V_+ C_s$ from the capacitor C_1. If the operational amplifier A_1 is ideal and the capacitance of C_1 is much larger than the capacitance of C_m, the output frequency of the modified circuit can be easily obtained by writing down the charge balance equation for capacitor C_1 as follows

$$f_c\,[(V_{ref} - V_+)C_m - V_+ C_r\,] = f_o\,V_+ C_s\,, \tag{5.14}$$

where V_+ is the potential at the non-inverting terminal of A_1 and it is equal to $\frac{1}{2}V_{ref}$ here. So the output frequency of the modified circuit is

$$f_o = f_c\,\frac{C_m - C_r}{C_s}\,. \tag{5.15}$$

The output frequency of the modified circuit is affected by the component nonidealities in the same way as discussed in the basic circuit, and the conclusions drawn in above section can be applied directly to the modified circuit.

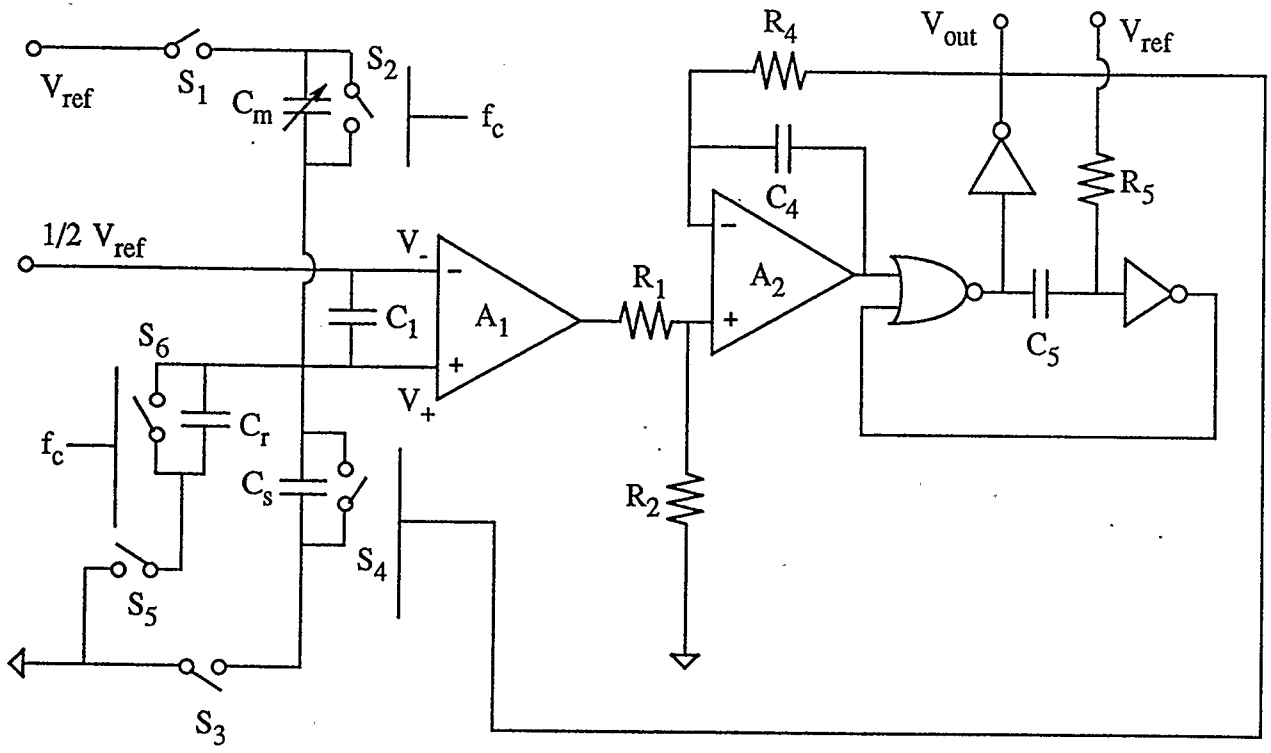


Fig. 5.5 Schematic diagram of the modified two-capacitor pumped capacitance-to-frequency conversion circuit

5.5 Implementation and Testing

The stability and the temperature characteristics of the two-capacitor pumped circuit were tested by implementing the circuit shown in Fig. 5.5. The stability was tested at constant temperature by using an oil bath with a temperature control accuracy of about 0.01 Celsius degree, and the temperature characteristic was tested for various temperatures in the range from 25 degrees Celsius to 175 degrees Celsius. The operational amplifiers and switches used in the implementation were HA5142 and LTC1043, respectively. Capacitors C_m, C_s and C_1 were chosen to be 100pF, 200pF and 0.1μF, respectively, and the temperature coefficients of these capacitors are +140 ppm ± 25 ppm per Celsius degree. The power supply voltage V_{ref} of 5 volts and an external clock frequency of 250 kHz were selected for this circuit.

Test results are listed in Table 5.1. The output frequency was measured by using an HP5316 universal counter using different gate times, and the temperature was set to be 27 degrees Celsius. As shown in Table 5.1, the maximum ppm standard deviation of the average frequency is about 2.4.

Gate Time	Average Frequency (HZ)	Standard Deviation (HZ)	ppm of Average Frequency
100ms	130349.7	0.3	2.4
200ms	130349.7	0.2	1.8
500ms	130349.8	0.1	1.1
800ms	130349.98	0.11	0.87
1.0s	130349.98	0.10	0.79

Table 5.1 *Test Results for Two-capacitor Pumped Converter*

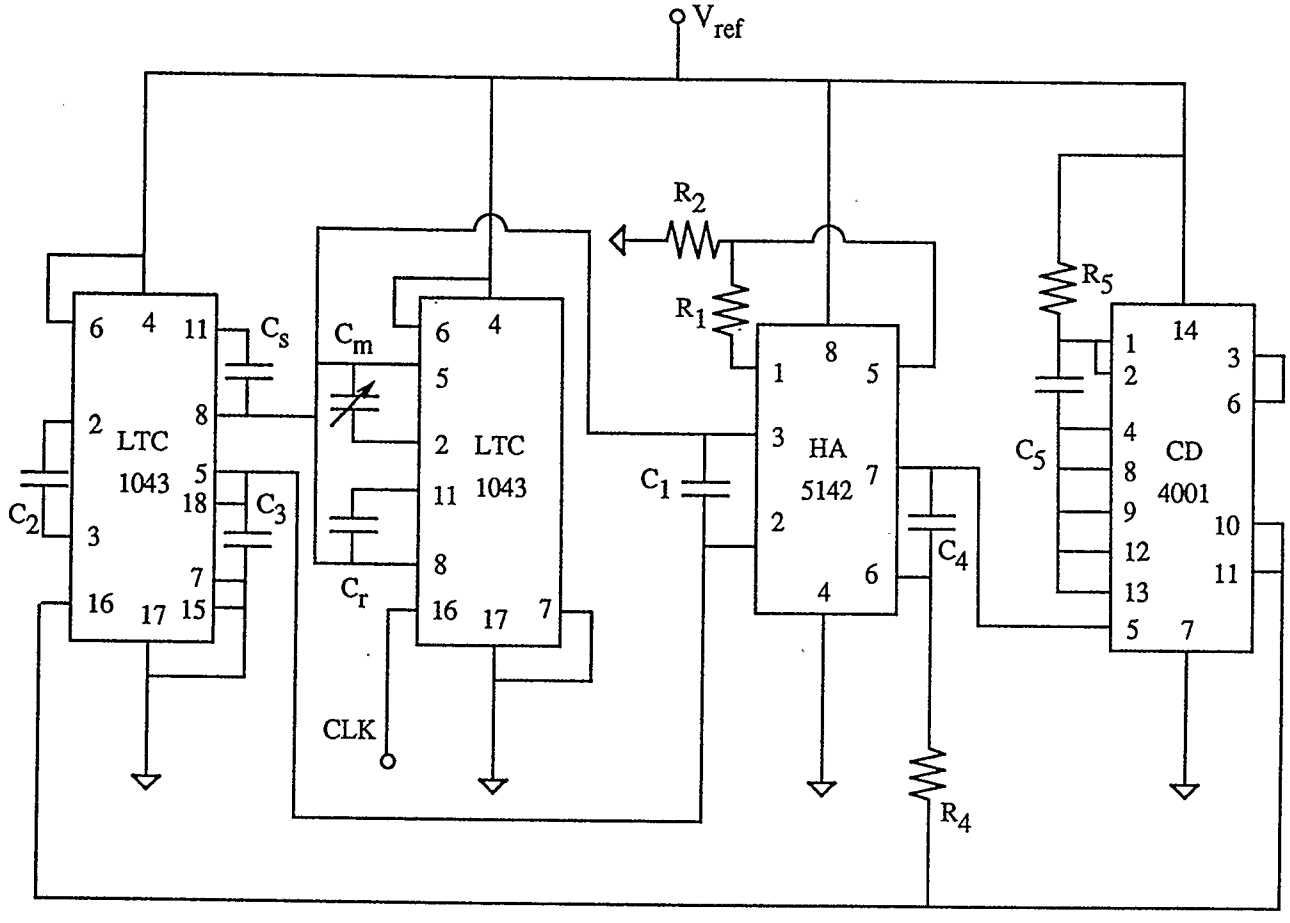


Fig. 5.6 Practical implementation for the modified two-capacitor pumped capacitance-to-frequency converter

The test results for the temperature characteristic of the conversion circuit are plotted in Fig. 5.7 with a comparison of the temperature characteristic of the capacitor C_m and C_s. Theoretically, the temperature coefficient of the output frequency should be zero if the temperature coefficients of capacitor C_m and C_s match and cancel out each other completely. However, there is a mismatch of about 25 ppm / per Celsius degree in the capacitor temperature coefficients and this results in the temperature coefficient of output frequency deviating from zero. When compared with the temperature characteristics of the RC free-running oscillator and the R-pumped capacitance-to-frequency converter, it appears that the output frequency of the two-capacitor pumped capacitance-to-frequency circuit is insensitive to the ambient temperature variation if the temperature characteristics of the capacitor to be measured and the standard capacitor can match each other very well.

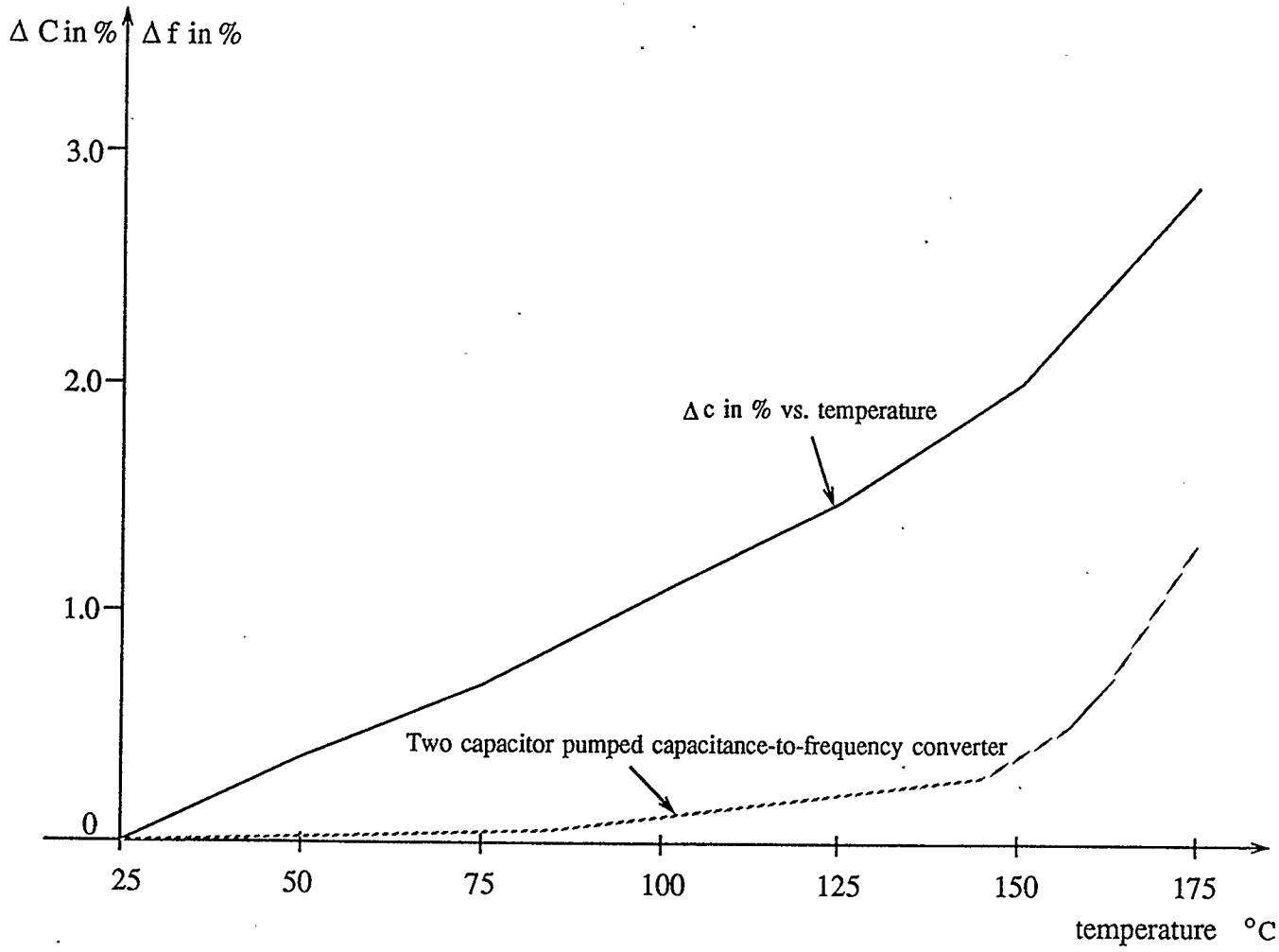


Fig.5.7 % capacitance change and % frequency change vs. temperature

Chapter 6

Simulation of the Noise Characteristics

6.1 Introduction

Because of the fact that all of the circuits discussed previously are effected by resistor and amplifier noise and this noise places a limitation on the achievable resolution, the evaluation of the noise performance is one of the important design considerations of these circuits. SPICE, a widely used simulation program, has been used to evaluate the effects of noise sources on the standard deviation of the output frequency. It is well known that SPICE is a useful circuit simulator at the device level, and is suitable for the simulation of analog circuits. However, the capacitance-to-frequency conversion circuits are hybrid analog / digital circuits which contain a large numbers of bipolar transistors or MOSFET's and diodes, so some special attention must be paid to the simulation of the noise characteristics. In this chapter, the noise models used in the simulation of noise characteristics are introduced, and a macromodel of the operational amplifier, which is developed for improving the simulation speed and reducing the circuit complexity, is described. Finally some simulation results are presented.

6.2 The Noise Source and Modelling

Noise existing in the circuits discussed in this thesis comes from three phenomena: (1) thermal noise in resistive material of both passive or active devices, caused by the random motion of electrons due to thermal agitation; (2) shot noise in

semiconductor devices, which is due to the discrete particle nature of carriers in current carrying devices; (3) flicker noise or $1/f$ noise, which refers to several phenomena that display a power spectral density that is approximately inversely proportional to frequency [15].

Thermal noise and shot noise are both approximately white in nature, that is, the power spectral density is constant and independent of frequency. The spectral density of thermal noise is proportional to both the temperature and the device resistance. The spectral density of shot noise is proportional to the dc current level. Flicker ($1/f$) noise is the dominant noise source at low frequency. The $1/f$ phenomena is characterized by a power spectral density that follows a $\frac{1}{f^{\alpha}}$ law.

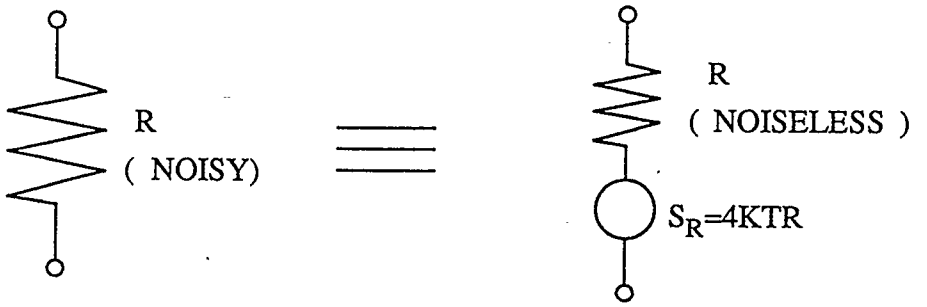
It is possible to predict the actual noise performance of a particular circuit by modelling the theoretical noise sources as equivalent noise voltage and noise current generators. If the noise generators can be assumed to be uncorrelated, the total noise output of the circuit can be estimated.

The equivalent noise model for a resistor with a resistance R is illustrated in Fig. 6.1(a), and the noise spectral density of a resistor is defined as

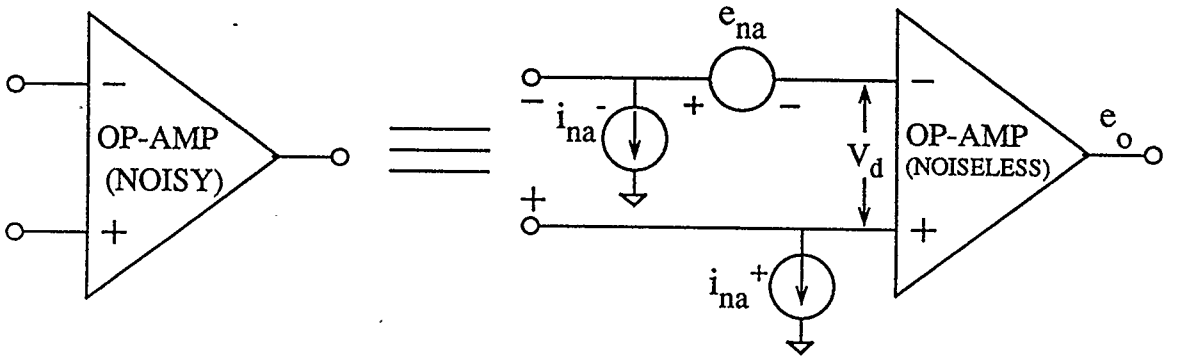
$$S_R = 4kTR; \tag{6.1}$$

where k is Boltzman's constant and T is the absolute temperature [16]. The power spectral density is normally expressed in $volts^2/HZ$.

An equivalent noise model for an operational amplifier is shown in Fig. 6.2(b) [17]. In this case, all of the noise sources internal to the device are referred to the



(a)



(b)

Fig. 6.1 (a) Noise model for resistor (b) Noise model for operational amplifier

amplifier inputs and are represented as two noise current generators and a single noise voltage generator. The spectral density of each generator depends on the type of device (bipolar, JFET, or MOSFET) and the amplifier design. For the purpose of analysis , these generators are modelled as follows:

(a) input noise voltage generator (e_{na}), $S_{ena} = S_e$;

(b) negative input noise current generator (i_{n-}), $S_{i-} = S_i$;

(c) positive input noise current generator (i_{n+}), $S_{i+} = S_i$;

where S_e and S_i are the respective spectral density functions of the noise sources.

In MOSFET amplifiers, the output noise contribution due to the input noise current sources is extremely small in comparison to the contribution due to the input noise voltage source, and therefore can usually be neglected. Similarly, thermal noise generated in small resistors ($R < 100K\ \Omega$) will be small in comparison to the op-amp input noise voltage, and in general can also be neglected [18]. This two assumptions are used throughout the simulation of the noise characteristics.

6.3 The Macromodel of Operational Amplifier

SPICE, a well known simulation program, originally was developed in the early 1970's for the purpose of integrated circuit design simulations in order to avoid difficult breadboarding. Since then, it has evolved into a far more widespread analog design tool and has been widely used on different types of computers, from main-frames to PC's. However, if transient analysis of SPICE is utilized to evaluate the noise characteristics of these capacitance-to-frequency conversion circuits discussed in chapter 2, 3, 4, several problems must be solved. It is known that each conversion

circuit to be simulated is generally composed of two operational amplifiers, one nor gate, several analog switches and several inverters, and the whole circuit consists of a large number of semiconductor devices such as bipolar transistors, MOSFET's and diodes. Because SPICE models semiconductor devices at the p-n junction and two-terminal element level, when a large circuit, such as the capacitance-to-frequency conversion circuit is simulated, one problem is that the simulation may exceed the simulator circuit-size capability established by memory limitations and convergence problem could arise. Even though an adequate simulator and computer are available, the required simulation time may make the simulation impractical. This problem can be solved by using a macromodel of the operational amplifier to significantly reduce the circuit complexity compared to the actual circuit, and therefore improve the simulation speed. In fact, the macromodel simulation approach may be the only practical way to simulate large circuits.

The term macromodel is most commonly used to represent a model which "simplifies" a more complex circuit function. The primary reason to create and use a macromodel is to decrease the circuit complexity and thereby increase the simulation speed when compared to the full device level transistor model. Many macromodels have been proposed both for analog and digital circuits. Some have been moderately successful, but perhaps the most successful has been the macromodel for bipolar operational amplifiers developed by G.R.Boyle, B.M.Cohn, D.O.Pederson, and J.E.Solomon [19].

The macromodel proposed in reference 19 is a good equivalent circuit for the 741 class of operational amplifiers with a bipolar NPN input stage. It accurately models the

input and output characteristics, differential- and common-mode gain versus frequency characteristics, quiescent dc characteristics, offset characteristics, and large-signal characteristics such as slew rate, output voltage swing, and short-circuit current limiting. This amplifier macromodel can be used for small-signal frequency response, dc operating point, and transient simulations. The only limitation of this class of models is that it can only model operational amplifiers used with both positive and negative supplies. This is due to the internal ground reference within the model.

A circuit diagram of this macromodel is given in Fig. 6.2. Indicated in this figure are the input, interstage and output stages of the macromodel. The model parameters are also noted in this figure. The circuit elements contained in the macromodel are those available in SPICE.(i.e. resistors, capacitors, dependent current sources, independent sources, diodes and bipolar transistors) All the circuit element values and the transistor parameters for this model can be calculated from information obtained from manufacturer's data sheets. Detailed equations with example are given in reference 19.

One important point for fully understanding this model is that the input differential pair $Q1$ and $Q2$ are operated at an input-output gain of unity, i.e., the output of the differential pair V_a is equal to input V_{in}. This primary factor allows considerable flexibility in implementing different but related models of the basic Boyle structure. In fact, any differential transconductance pair can in principle be substituted in the front end after suitable transconductance adjustments.

The complexity of this macromodel has reduced an 81-node circuit with 193 branches to a 16-node circuit with 28 branches. The speed improvement is between 6

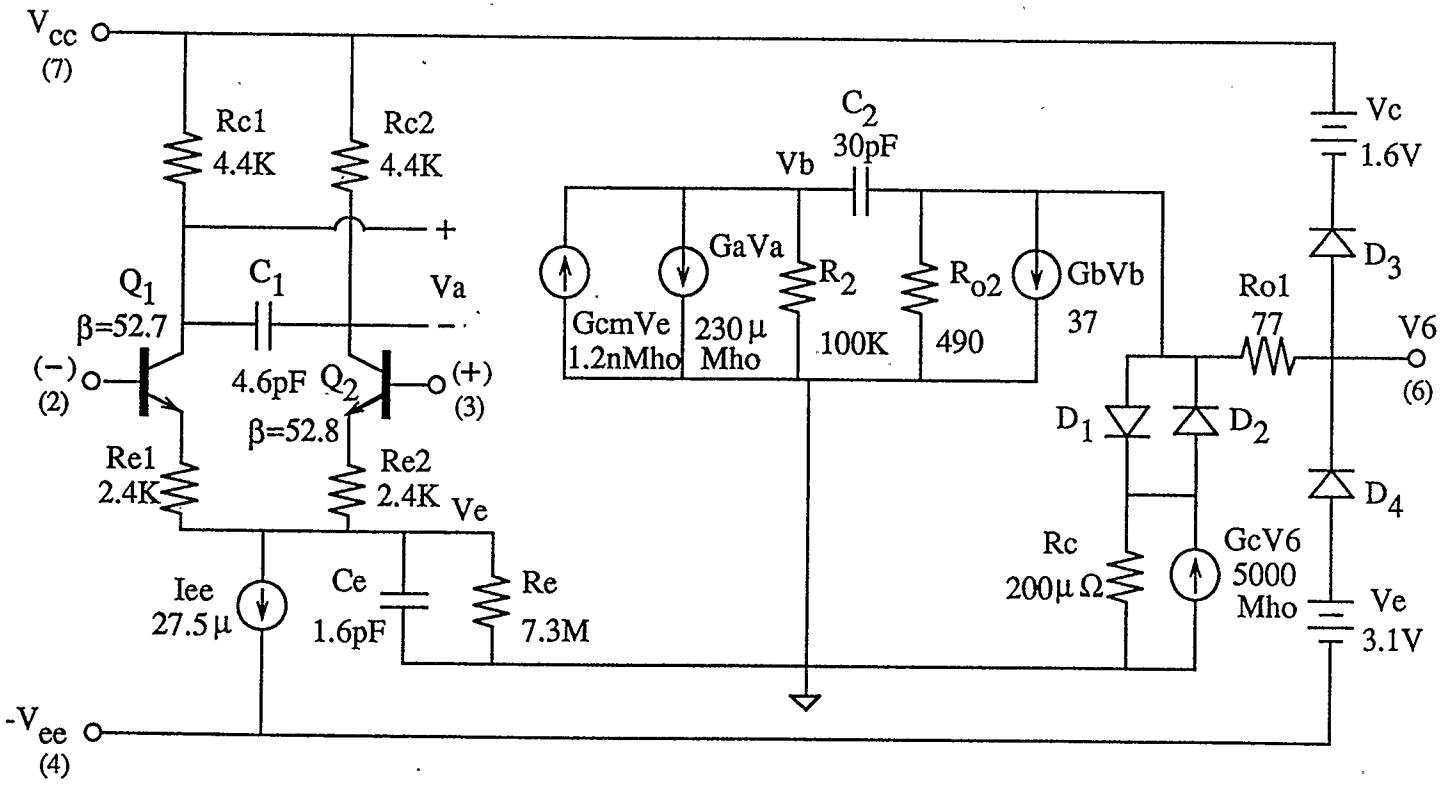


Fig. 6.2 A 741 operational amplifier macromodel

and 10 to 1.

With the replacement of the NPN input transistors shown in the basic Boyle model with PNP bipolar types, or alternatively, with JFET or MOSFET types, four separate macromodel types, which are supported by the above mentioned basic Boyle topologies, can be used to emulate many device specific conditional details. For example, with PMOS input transistors used in the front end, the low input bias currents and low input offset voltage chopper-stabilized operational amplifier as well as the single supply CMOS amplifier can be modelled.

The macromodel for the CMOS operational amplifier is shown in Fig. 6.3. The numerical value of the model elements can be obtained from the manufacturer's data sheets or from the experimental measurements of the operational amplifier characteristics. Except for the input stage, the technique which was used in the basic Boyle model can still be utilized to determine the macromodel parameters. A complete derivation of all the macromodel parameters can be found in reference 19. Here, only some important equations for the input stage are discussed.

The absolute values of the input MOS transistor parameters can be chosen arbitrarily. The input offset voltage V_{os} can be modelled by specifying different threshold voltages for the two transistors, so that the offset voltage is

$$V_{os} = |V_{T1} - V_{T2}| \tag{6.2}$$

The input bias and offset currents are modelled by two current sources I_{G1} and I_{G2}, and the values of I_{G1} and I_{G2} are chosen in such a way that the average value of these two current sources is equal to the input bias current of the operational amplifier

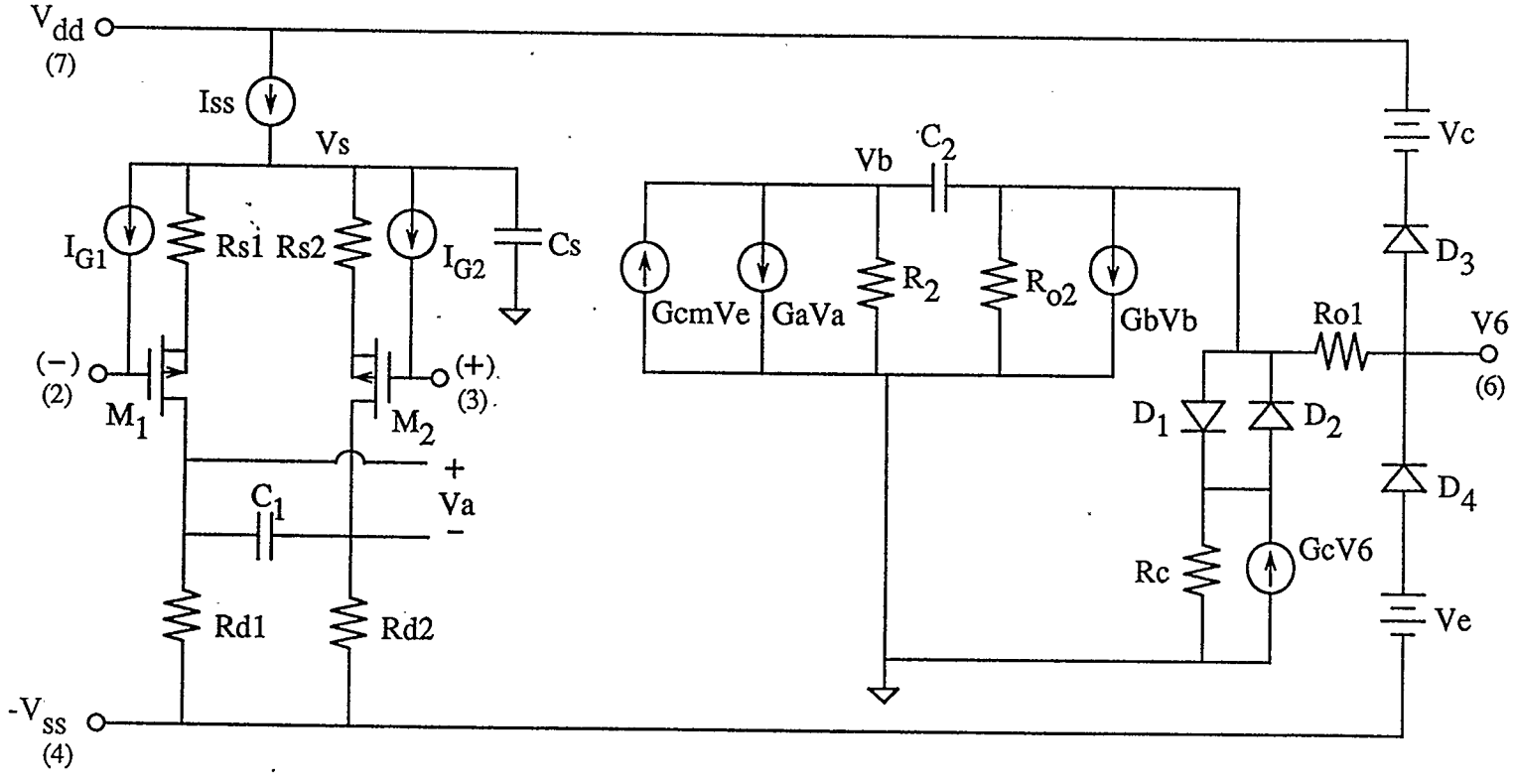


Fig. 6.3 Macromodel with MOSFET input stage for TSC913.

and the difference $(I_{G1}-I_{G2})$ is equal to the input offset current. Two equal resistances R_{s1} and R_{s2} are introduced in the input stage to provide a degree of freedom for independent control of slew rate and zero db frequency, and their values can be found from the differential mode voltage gain, which for convenience is taken to be unity. Thus,

$$\frac{V_a}{V_{in}} = \frac{g_m R_{d1}}{1 + g_m R_{s1}} = 1 \tag{6.3}$$

where g_m is the transconductance of the input transistors. The value of g_m in the above equation can be determined from

$$g_m = \sqrt{2 I_{D1} \beta} \tag{6.4}$$

where β is the transconductance constant for the MOSFET defined by

$$\beta = \mu C_0 \frac{W}{L}. \tag{6.5}$$

In the above equation, μC_0 is the product of the channel surface carrier mobility and the oxide capacitance per unit area, and W/L is the ratio of channel width to channel length. In order to maintain the voltage gain at unity, when a different value of β is assumed for these two MOS transistors, a different value for resistor R_s would have to be selected.

The equations used to calculate the parameters of the macromodel with MOSFET input stage are summarized in Table 6.1 and the values of these macromodel parameters for the TSC913 operational amplifier are given in Table 6.2 [20].

Design Equations for the Operational Amplifier Macromodel

$$V_T = \frac{kT}{q} = 25.85 \text{ mV for } 300K$$

$$I_{sd3} = I_{sd4} = 8 \cdot 10^{-16} \text{ A}$$

$$R_2 = 100 \text{ K}\Omega$$

$$I_{d1} = I_{d2} = \frac{C_2}{2} S_R^+$$

$$C_S = \frac{2 I_{d1}}{S_R^-} - C_2$$

$$I_{G1} = \frac{I_B + I_{BOS}}{2}$$

$$I_{G2} = \frac{I_B - I_{BOS}}{2}$$

$$V_{os} = V_{TH1} - V_{TH2}$$

$$\frac{1}{g_m} = \sqrt{2 I_{d1} \beta}$$

$$R_{d1} = \frac{1}{2\pi f_{odb} C_2}$$

$$Rs1 = R_{d1} - \frac{1}{g_m}$$

$$C_1 = \frac{C_2}{2} \tan \Delta\varphi$$

$$Ga = 1/ R_{d1}$$

$$G_{cm} = \frac{1}{R_{d1} (CMRR)}$$

$$R_{01} = R \text{ o-ac}$$

$$R_{02} = R_{out} - R_{01}$$

$$G_b = \frac{a_{VL} R_{d1}}{R_2 R_{02}}$$

$$I_x = (2 I_{d1}) G_b R_2 - I_{sc}$$

$$I_{sd1} = I_{sd2} = I_x \exp - \frac{R_{01} + I_{sc}}{V_T}$$

$$R_c = \frac{V_T}{100 I_x} \ln \frac{I_x}{I_{Sd1}}$$

$$Gc = 1/ R_{d1}$$

$$V_c = V_{dd} - V_{out}^+ + V_T \ln \frac{I_{sc}^+}{I_{Sd3}}$$

$$V_E = V_{ss} + V_{out}^- + V_T \ln \frac{I_{sc}^-}{I_{Sd4}}$$

Table 6.1 The design equations for the operational amplifier macromodel

TSC 913 Data Sheet and Macromodel Parameters

TSC 913 Data Sheet		Macromodel Parameters	
V_{os} (μV)	5.0	T (K)	300
I_B (pA)	90	I_{ds1}(A)	$2.069 \cdot 10^{-31}$
I_{BOS} (pA)	5.0	C_2 (pF)	30
CMRR (db)	116	C_S (pF)	4.6
A_{VL} (db)	120	R_2 (KΩ)	100
SR (V/μS)	2.5	V_{TH1}(V)	1.7
f_{odb}(MHZ)	1.5	Iss (μA)	75
V_{out} (V)	from Vss + 0.3 to V_{dd}- 0.9	V_{TH2}(V)	1.700005
		β_1 (mA/V^2)	0.55
		β_2 (mA/V^2)	0.55
		I_{G1} (pA)	92.5
		I_{G2} (pA)	87.5
		R_{S1}(Ω)	111
		R_{d1}(KΩ)	3.536
		I_{sd3}(A)	$8 \cdot 10^{-16}$
		C_1 (pF)	12
		G_a (μmho)	282.8
		G_{CM}(nmho)	0.448
		R_{01}(Ω)	76.8
		R_{02}(Ω)	489.2
		G_b (mho)	72.28
		I_x (A)	542.1
		R_c(Ω)	0.03669
		G_C (mho)	27253
		V_d (V)	1.704
		V_S (V)	0.504

Table 6.2 The data sheet and macromodel parameters of TSC913

HA5142 Data Sheet and Macromodel Parameters

HA-5142 Data Sheet		Macromodel Parameters	
V_{os}(mV)	2.0	T (K)	300
I_B (nA)	45	I_{s1}(A)	$8 \cdot 10^{-16}$
I_{BOS}(nA)	0.3	I_{s2}(A)	$8.619 \cdot 10^{-16}$
CMRR (db)	105	C_2 (pF)	30
A_{VL} (db)	100	C_E(pF)	7.5
SR (V/μS)	1.5	R_2 (KΩ)	100
f_{odb}(MHZ)	0.5	I_{EE} (μA)	45.1
		R_E (mΩ)	9.442
		β_1	498.3
		β_2	501.6
		I_{B1} (nA)	45.15
		I_{B2} (nA)	44.85
		R_{E1}(KΩ)	9.442
		R_{c1}(KΩ)	10.61
		I_{sd3}(A)	$8 \cdot 10^{-16}$
		I_{sd1}(A)	$3.7 \cdot 10^{-32}$
		C_1 (pF)	8.66
		G_a (μmho)	94.25
		G_{CM}(nmho)	0.53
		R_{01}(Ω)	76.8
		R_{02}(Ω)	489.2
		G_b (mho)	21.69
		I_x (A)	97.58
		R_c(Ω)	0.204
		G_C (mho)	4906.8
		V_S (V)	1.604
		V_d (V)	0.104

Table 6.3 The data sheet and macromodel parameters of HA5142

The macromodel of the bipolar operational amplifier used with single supply can be obtained by replacing the NPN input transistors of the basic Boyle model with the PNP transistors. The values of the macromodel parameters for the HA5142 are calculated by using the equations in reference 19 and are summarized in Table 6.3 [21].

6.4 The Generation of Noise Voltage Source

In the simulation of the noise characteristics of the capacitance-to-frequency conversion circuits, an assumption that the spectra of the input noise voltage sources are all white was made in order to simplify the simulation.

In SPICE, no white noise voltage source is available. Therefore, the white noise voltage source was generated by using the SPICE piecewise linear source function [22] in such a way that the noise voltage is essentially a straight line interpolation of a Gaussian distributed random sequence.

To generate a white noise voltage source, the following procedure should be followed [23]. First, a random sequence generation program is used to produce a real uncorrelated Gaussian distributed random sequence with zero mean and specified standard deviation. The length of this sequence is determined by the time duration at which the SPICE transient analysis is made and the sampling time, i.e., the time interval between two interpolation points. For example, if the SPICE transient analysis is made from zero to 400 microseconds and the sampling time is chosen to be 0.2 microseconds, the sequence length will be 2000.

For a real random sequence $X = X(k)$, $k = 0,1,2,...n$, where the elements are uncorrelated with each other, and with $E\,X(k) = 0$ and $D\,X(k) = \sigma^2$, it is easy to show that its autocorrelation sequence is:

$$EX(k)X(l) = \begin{cases} \sigma^2, & k = l \\ 0 & k \neq l \end{cases}. \tag{6.6}$$

The power spectral density function of this random sequence is the Fourier transform of autocorrelation sequence of Eq.(6.6) and can be expressed as

$$X(\omega) = \sigma^2. \tag{6.7}$$

As shown in Fig. 6.4, the spectrum of the random sequence is an ideal white noise spectrum.

Secondly, an interpolating function should be chosen for the interpolation operation. If the random sequence discussed above can be considered to be a uniformly sampled signal and sampled at a rate of 1/T Hz, where T is the sampling time, the reconstructed noise voltage source can be given by

$$x_I(t) = \sum_{k=0}^{\infty} x(kT)\, g(t - kT). \tag{6.8}$$

In Eq.(6.8), $x(kT)$; $k = 0,1,2,...$ is the random sequence and g(t) is the interpolating function.

Eq.(6.8) is the convolution of the random sequence and the interpolating function in the time domain so that its Fourier transform can be transformed into a product operation in the frequency domain and yields

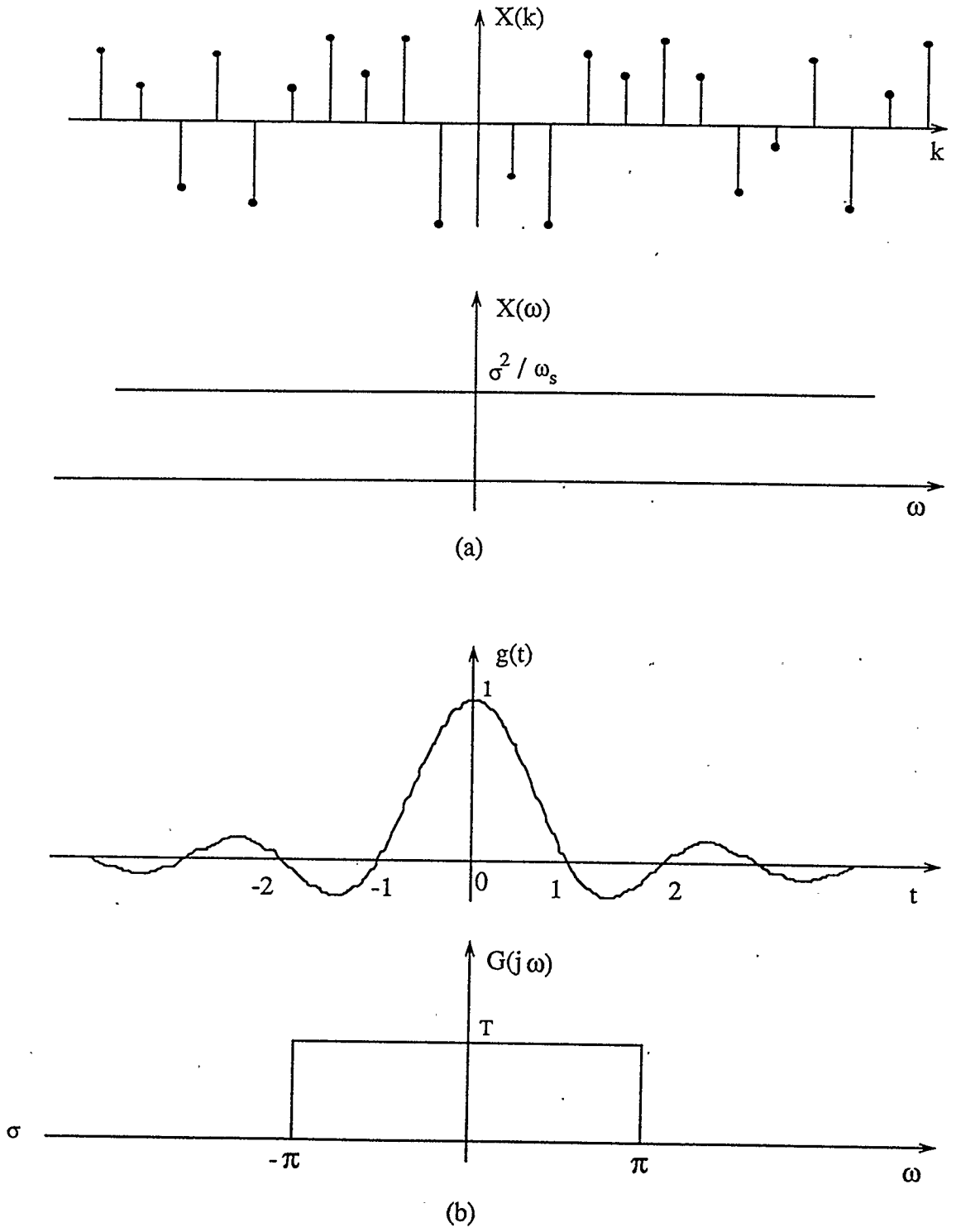


Fig. 6.4 (a) Random sequence and its power spectrum
(b) Sinc(t) function and its frequency spectrum

$$X_I(\omega)=X(e^{j\omega T})G(j\omega), \tag{6.9}$$

where $X(e^{j\omega T})$ is the spectrum of the random sequence and $G(j\omega)$ is the spectrum of interpolating function $g(t)$.

The interpolation operation can be viewed as a filtering operation. As such, interpolation design becomes a low pass filter design, and the interpolation problem is converted to a problem of choosing a suitable interpolating function which possesses ideal low pass filter characteristics [23]. It is desirable to use a sinc(t) function whose definition is $sinc(t)=\frac{sint}{t}$ as the interpolating function. Because, as shown in Fig. 6.4, in the frequency domain the Fourier transform of the sinc(t) function is a rectangular pulse, which is often called a gate function and the gate function possesses an ideal low pass filter characteristic. Unfortunately, it is impossible to use the sinc(t) function as an interpolating function in SPICE. The best approach to generating a white noise voltage source is to utilize a SPICE piecewise linear source function, and it is, in essence, the straight line interpolation of the Gaussian distributed random sequence discussed above.

The straight line interpolation can be shown in Fig. 6.5. As shown in Fig. 6.5, the interpolating function of straight line interpolation is a triangle in the time domain. The triangle interpolating function in Fig. 6.5 has the analytic expression given by

$$g(t)=\begin{cases}1-\frac{|t|}{T} & |t|<T\\ 0 & |t|>T\end{cases}, \tag{6.10}$$

where T is the sampling time. The Fourier transform of the triangle in Eq.(6.10) can

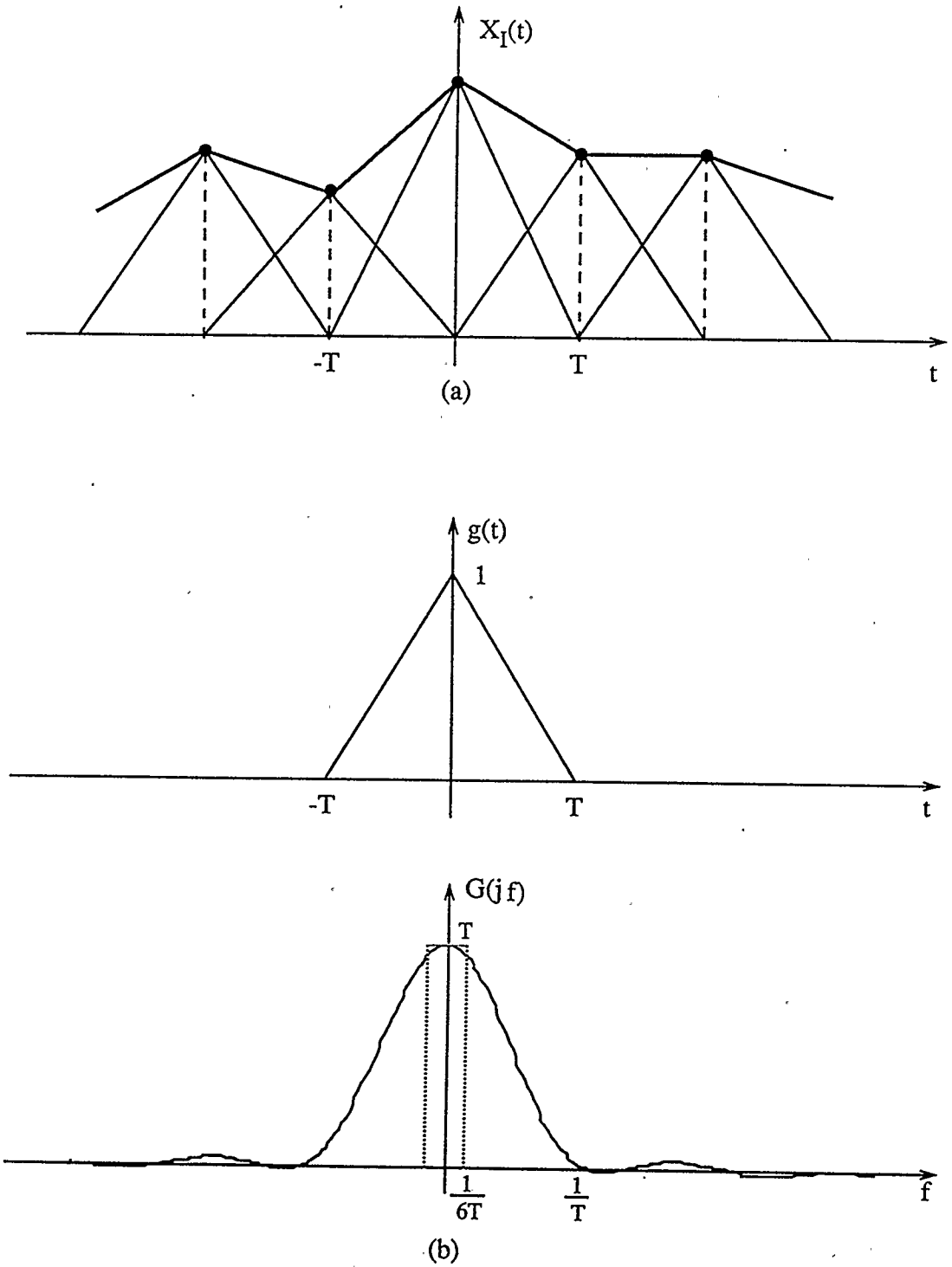


Fig. 6.5 (a) Straight line linear interpolation

(b) Triangle interpolation function and its spectrum

be calculated by use of the definition, as follows

$$G(j\omega)=\int_{-\infty}^{\infty} g(t)e^{-j\omega t}\,dt, \tag{6.11}$$

Substituting Eq.(6.10) into above equation and calculating the integration yields the transform as

$$G(j\omega)=T\,sinc^2(\frac{\omega T}{2}). \tag{6.12}$$

In this case, the frequency spectrum of the triangle interpolating function is the square of the sinc(t) function and can be plotted as shown in Fig. 6.5. The first zero crossing of the spectrum occurs at a frequency $f=1/T$ Hz, and as the sampling time T is decreased, this first zero crossing moves up in frequency.

In order to obtain a close approximation of the white noise spectrum in a specified frequency range, the spectrum of the noise voltage source produced using straight line interpolation has to be constant in the specified frequency range. As discussed above, the shape of the spectrum of the noise voltage source is determined by the shape of the spectrum of the interpolating function and the shape of the spectrum of the random sequence. However, the spectrum of the random sequence is an ideal white noise spectrum, so the shape of the spectrum of the noise voltage source is only dependent on the shape of the interpolating function, and in this case, is only dependent on the shape of the spectrum of the triangle.

Although the spectrum of the triangle interpolating function is not an ideal gate function, its magnitude spectrum can be thought of as constant in a narrow frequency range [23]. For example, the magnitude spectrum is decreased from its peak value to

90% of its peak value from the frequency of zero to the frequency of $1/6T$. The narrower the frequency range, the more constant is the magnitude of the spectrum. Therefore, the quality of spectrum of the noise voltage source can be controlled by chosing the sampling time T such that the magnitude spectrum can keep constant in the specified frequency range. It is better to select the sampling time as small as possible, however, there is a tradeoff between the quality of the noise voltage source, the CPU time needed to run the simulation program and the memory needed for the storage of data.

In our simulation, the sampling time is chosen in such a way that the frequency of $1/6T$ is equal to the ten times of the output frequency of the simulated circuit. For example, if the output frequency of the circuit is $f_o = 83.333\,KHZ$, the sampling time is selected to be $0.2\,\mu s$.

6.5 The Simulation Results

Three capacitance-to-frequency converter circuits including the resistance-capacitance free-running relaxation oscillator, R-pumped switched capacitor capacitance-to-frequency converter and two-capacitor pumped capacitance-to-frequency converter were simulated by using the Meta-software 1990 HSPICE simulation program. The simulation was mainly concentrated on the evaluation of the noise characteristics of these circuits.

The noise models used for the two operational amplifiers of the simulated circuits in the simulation consist of a noise-free operational amplifier with a white noise voltage source in series with the inverting input terminal. These two white noise voltage

sources are uncorrelated and are generated by using straight line interpolation of a Gaussian distributed random sequence. The effects of the noise voltage of the resistors can be ignored because the resistances of all of the resistors in these simulated circuits are less than $100k\ \Omega$. In the simulation only the effects of the noise voltage source of the operational amplifier were simulated.

It is very important to pay attention to the selection of appropriate value of the initial state of the simulated circuits to assure convergence. When a very long time transient analysis is needed to obtain the steady state of these circuits, it is better to divide the whole time interval into a couple of short time intervals and to do the simulation for a short time and store all of the node voltages and use them as the initial state for next simulation. By doing so, the difficulty of exceeding the memory of the system in a long time simulation can be easily overcome.

The simulation results of the noise characteristics for the RC oscillator, R-pumped converter and two-capacitor converter are shown in Fig. 6.6, Fig. 6.7 and Fig. 6.8, respectively. It is seen from these diagrams that the standard deviations of output frequency have an approximately linear relationship with the input noise voltage spectral density of noise voltage source. The noise characteristics of the circuits at actual noise levels can be obtained by extrapolating the simulation data to the lower noise levels. For example, from Fig. 6.7, the standard deviation when the noise voltage is about $1\text{mv}/\sqrt{Hz}$ is equl to 0.0011 and the standard deviation when the noise voltage is about $10\text{mv}/\sqrt{Hz}$ is equal to 0.0073, therefore, the standard deviation for the actual R-pumped converter with noise level at $2.5\mu v/\sqrt{Hz}$ can be obtained by extrapolation to be about 0.0004. This value is very close to the test results of Table 3.3 in chapter 3

where the standard deviation can be found to be $0.57 \cdot 10^{-6} \sqrt{1.0 \cdot 91575.2} = 0.00015$.

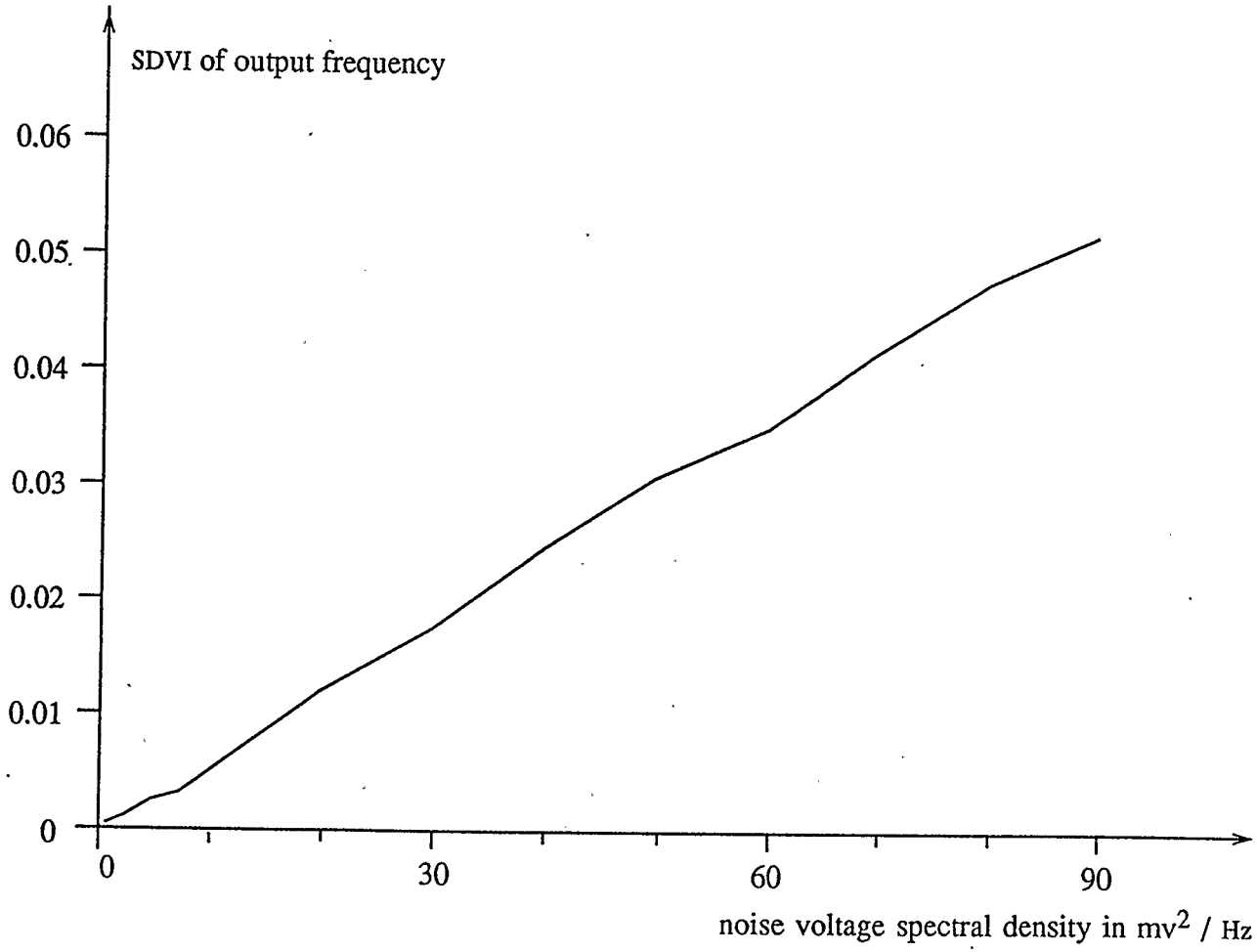


Fig. 6.6 Simulated noise characteristic for RC free-running oscillator

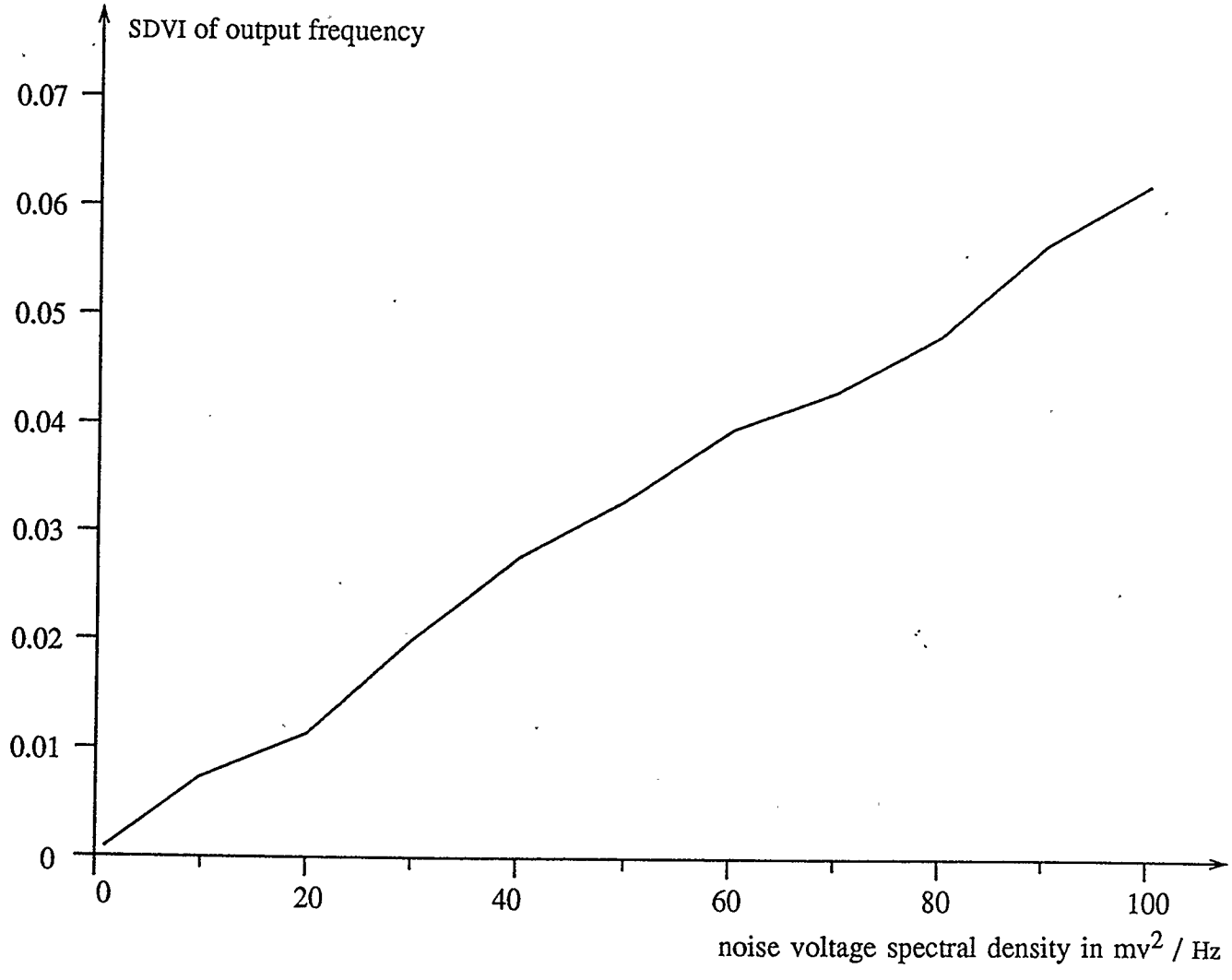


Fig. 6.7 Simulated noise characteristic for R-pumped converter

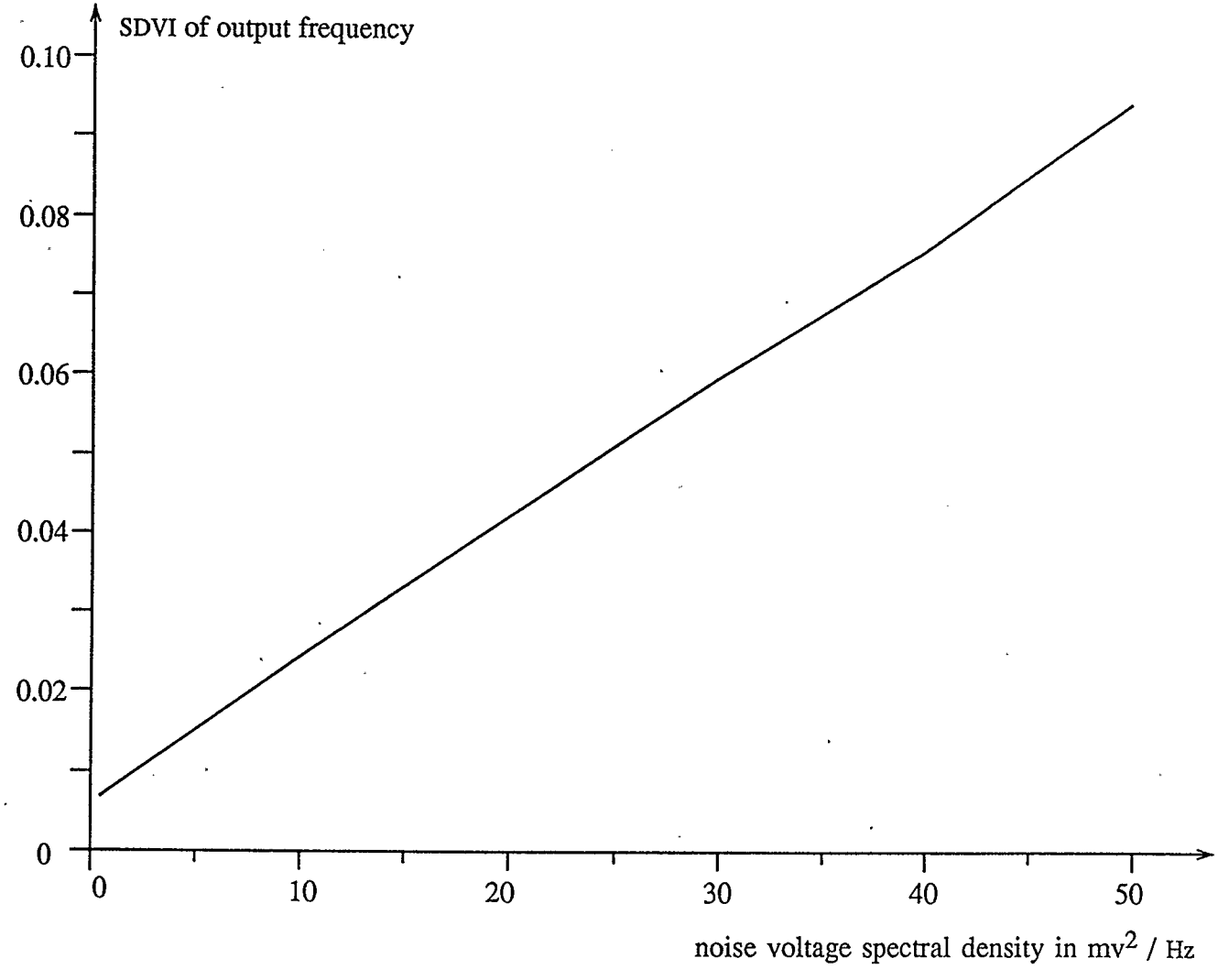


Fig. 6.8 Simulated noise characteristic for two-capacitor pumped converter

Chapter 7

Conclusions and Suggestions for Further Studies

In this thesis, a number of capacitance-to-frequency conversion circuits for interfacing capacitive transducers with digital systems have been described. These circuits include an RC free-running relaxation oscillator, an R-pumped switched capacitor capacitance-to-frequency converter and a two-capacitor pumped capacitance-to-frequency converter. Because of their low parts count, single power supply operation and high stability, these circuits should be useful in industrial applications.

The RC free-running oscillator generates an output pulse train with a frequency which is dependent on the capacitance to be measured, one resistance and three resistance ratios. The disadvantage of this oscillator is that its stability depends on the stability of five resistors and a stable time base is needed for accurate frequency measurement.

The R-pumped switched capacitor converter uses the switched capacitor method to create a simulated resistor containing the capacitor to be measured and two switches. One end of this simulated resistor is voltage driven and the other end is connected to a large capacitor which is used as a charge reservoir. The effective value of the simulated resistor is automatically adjusted by the output frequency until it is approximately equal to the resistance of a normal resistor. An implementation of this circuit using discrete components has been tested. Test results show that this circuit

has the best stability in terms of ppm standard deviation from average output frequency among the studied circuits and it is less than 1 ppm and that the long term stability is almost entirely dependent on one resistor. The test results also indicate that this circuit can work well over the temperature range of 0 degrees Celsius to 175 degrees Celsius. The error introduced by the open-loop amplifier nonidealities can be eliminated by either choosing a low offset voltage and low input bias current operational amplifier or by using the technique of interchanging the position of the normal resistor and simulated resistor. The error caused by the limited size of the capacitive charge reservoir can be reduced by selecting the capacitance ratio C_1/C_m as large as possible. This circuit shows that the use of a switched capacitor simulated resistor formed using the capacitor to be measured and two switches is a very useful approach in instrumentation applications.

In the design and implementation of the two-capacitor pumped converter, the concept of using capacitance ratioing, i.e., comparing the measured capacitor to a standard capacitor, in the capacitance-to-frequency conversion circuit was examined. The output frequency of this circuit is proportional to the clock frequency and the capacitance ratio C_m to C_s. The stability of this converter depends on neither resistance nor the time base if the same clock is used to measure the output frequency. The circuit has been tested and the test results show that the stability of this circuit in terms of ppm standard deviation from average output frequency is about 2.0. As for the temperature characteristics, the test results indicate that the output frequency will be basically free from the effect of ambient temperature if the temperature characteristics of the capacitor to be measured and the standard capacitor match each other very well. Therefore,

this circuit should find applications in a high temperature environment such as oil and gas reservoirs. From the advantages discussed above, it appears that the use of capacitance ratioing is the best approach to the design of capacitance-to-frequency conversion circuits and it can be directly applied to the design of capacitive sensors.

The two designs of R-pumped converter and two-capacitor pumped converter can be applied directly to the design of silicon capacitive sensors so that the sensor and the signal conditioning circuit can be fully integrated on the same silicon wafer. By doing so, low cost and ease of interfacing with digital systems can be realized.

In the practical implementation of both the R-pumped converter and the two-capacitor pumped converter, the stray capacitances from the MOS switches introduce an error in the output frequency. Techniques which can eliminate the effects of stray capacitances of the MOS switches on the output frequency need to be studied in further work.

Possible further research work might involve investigation of the design of a filtering circuit. In practical applications, after the frequency signal from these interfacing circuits is transmitted to the central control unit, an analog signal which is representative of the measured capacitance is sometimes needed. The design and implementation of such a filtering circuit would be useful.

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