# 1 Introduction

This document details the board developed to test fabicated SECD chips.[2] The board also serves as the mother-board for the chip's use. This paper attempts to justify the approach taken in the board's implementation and explain its functionality with respect to its two tasks.

# 2 The SECD Chip

SECD is a specialised architecture to run a purely functional version of Lisp (LispKit).[3] There are three functional blocks making up the architecture: control unit, data path and shift-registers.

- The *control unit* interprets SECD instructions. They are broken down into micro-instructions that the data path executes in sequence. The control unit is a finite-state machine.
- The *data path* executes micro-instructions. It is composed of functional components (registers, arithmetic unit and memory) communicating over a shared 32-bit bus.
- The *shift-register* exists to ease the testing of the chip. The state of the chip can be examined and test vectors asserted using the shift-register.

A more detailed description of these blocks and other architectural issues can be found in [2].

Two sets of external clocks are used to control the flow of information within the chip. One set operates the shift-register the other is the system clock. A two-phase non-overlapping scheme is used. Control signals for the data-path are from the micro-instruction pointed to by the MPC (**M**icro-**P**rogram **C**ounter). These signals are valid sometime following the loading of hte micro-instruction address into the MPC (rising edge of $\Phi_B$). This initiates a data-path computation, terminated by the falling $\Phi_A$ edge when the result is stored into some register or memory location. Computation proceeds in a lock-step fashion. The shift-register clocks work in a similar fashion except the adjacent output signals becomes valid on the rising edge of $\Phi_B$ and is latched on the falling edge of $\Phi_A$.

Other signals are also external to the chip. They can be separated into four categories:[4]

[2] For a detailed description of the development and design of the SECD chip see[1][3].

[3] SECD is an abstract machine invented by Landin.[6] The implemented version is based on Henderson's variant.[4]

[4] This excludes the obligtory power/ground and the clocks as they have been previously mentioned. A complete pin-out can be found in [3].

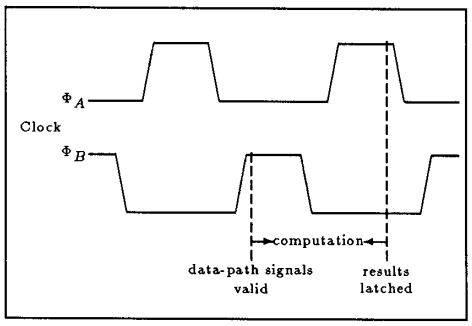



Figure 1: Clocking scheme of the SECD chip with regard to the data-path.

- *Memory* - SECD has no internal memory to store the programs that it runs. Commercially avaliable memories are cheap and readily avaliable allowing the conservation of chip landscape. SECD addresses 16K ($2^{14}$) 32 bit words. The signals required to access memory have been exported: read memory, write memory, 14 bit *address bus* and a 32 bit bi-directional *data bus*. Most commercial memories require only one signal to reflect the bus access. SECD uses two signals as it was tailored to AM99C88/AM99CL88 8k x 8 static RAM memory. Either type can be accomodated.
- *Status* - SECD can be in one of four states: idle, top of instruction cycle, error or in transistion between the other three states. The state is reflected by two flags.
- *Flow* - is concerned with the overall operation of the chip. Two signals are involved. The first is *reset*. This resets the internal state of the machine (when held during an entire system clock cycle). It puts the chip into a known state (idle). Once a forced reset has been done, *button* can be asserted to initiate computation. Computation carries on until execution has been completed (*i.e.* returns to the idle state) or an error occurs.
- *Shift register* - is controlled by two signals and has an external input and output. The shift register sits between the control unit and the datapath. One of the control signals (*test*) determines whether the signals come from the test value contained in the register or from the control signals passed between the datapath and control unit. The other shift-register control signal (*shift*) effectively chains together the latches into a shift-register. Its normal mode of operation is to pass the signals through without latching them. The other two signals (*shin* and *shout*) allows information to be entered and viewed.

The function of the board is to control these signals as required.

# 3 The Board

The board is the means of testing and controlling SECD's operation. It is made up of descreet TTL logic elements. These have been wire-wrapped according to the schematics that accompany this document. Once the hardware has been demeed to be correct and complete, PCBs can be made. The description of the board will be based on the schematics. The nuances of each will be detailed.[5]

| Section | Number(s) | Title |
|---|---|---|
| 3.1 | 1 | 6809 |
| 3.2 | 2 | Communication |
| 3.3 | 3 | Address Decoding |
| 3.4 | 4 | Program Memory |
| 3.5 | 5 | SECD Control Signals |
| 3.6 | 6&7 | SECD Memory |
| 3.7 | 8 | SECD |

[5]See the accompanying specification sheets for the board's components.

## 3.1 Schematic 1: 6809

The 6809 $\mu$processor plays a major role in the testing and operation of the SECD chips. It is responsible for the configuration and control of the other programmable components on the board, the processing and execution of user commands, accessing SECD memory and the setting up and monitoring of signals to/from the SECD.

The 6809 was choosen not because it was ideally suited to the task. Rather:

- it is a simple (but powerful) micro.
- we have a 6809 cross-assembler to EPROM code (see the next section).
- the technical support group has built boards using the 6809 before. This reduced the up-to-speed time.

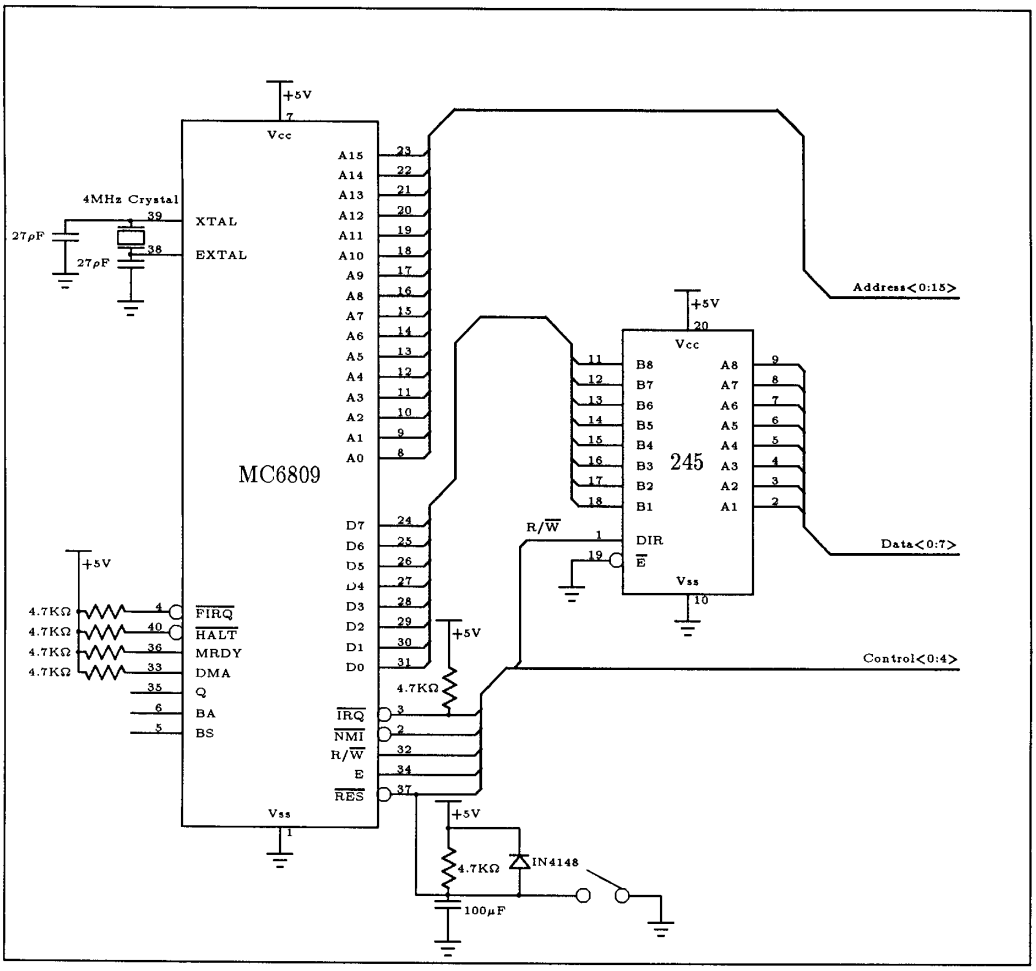
It is clocked by a 4Mhz crystal but operates at 1Mhz (the crystal's signal is divided down and separated into two phases internally). It is possible to get better performance by using either the 1.5MHz or 2MHz versions of the 6809 (MC68A09 and MC68B09 respectively).

Five of the 6809 control signals are used throughout the board: *reset*, $E$ (a slight misnomer as $E$ is really $\Phi_2$ of 6809's system clock), *read/write* and the two interupt lines (*NMI* and *IRQ*). Those 6809 control signals that are not used are either left floating, or, if they by picking up stray noise might affect the operation of the program, tied high through a pull-up resistor.

The 6809 has been set up so that it can be reset by a push-button. The required circuitry is the normal resistor/capacitor system but with a current limiting diode. On reset all other programmable components on the board, including SECD, are put in their initial state.

The 6809 has an 8 bit data bus with an address space of 64K ($2^{16}$).[6]. The breakdown of the address space is shown in Figure 2. Due to the large number of chips accessing the data bus, it is buffered and the direction is controlled by the read/write signal of the 6809.

[6]It is necessary for the 6809 to bank-switch SECD's memory when it access it. This will be elaborated on in §3.6.




Schematic 1: 6809

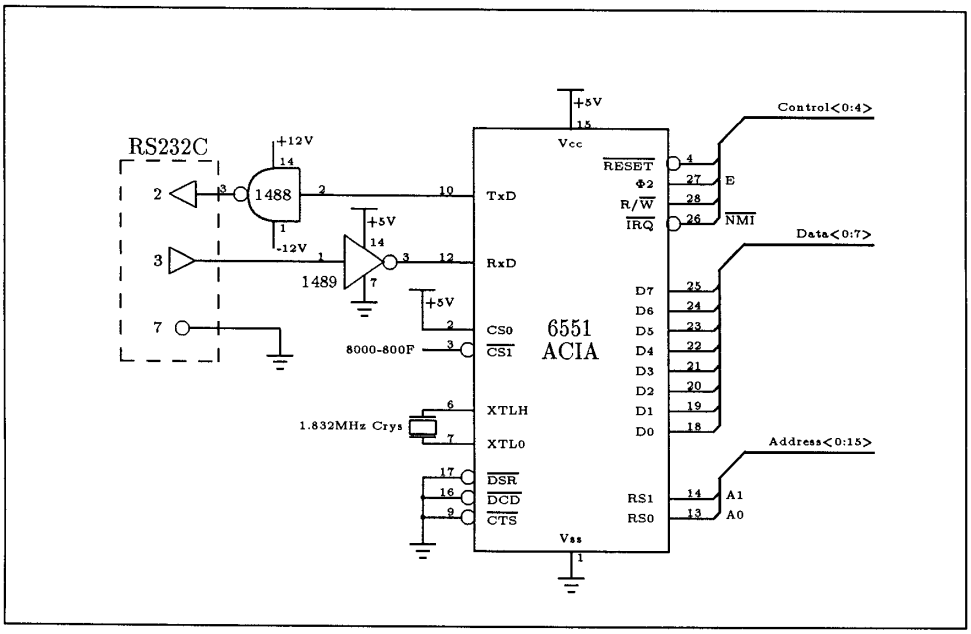
## 3.2 Schematic 2: Communication

Communications to and from the board is accomplished by using the RS232C protocol. Three of the possible seven signals are used: ground, transmit data and receive data. The other signals are not required as handshaking is done in software. Data is exchange in byte streams.

The packaging of data on the board side of the serial line is handled by an ACIA (**A**synchronous **C**ommunications **I**nterface **A**dapter). The 6551 ACIA is fully programmable. It is configured to run at 4800 baud on reset by the 6809. As specified, a 1.832 MHz crystal is used as the baud rate generator.

The RS232 protocol specifies that signals operate at $\pm 12V$. Two adapter chips are required to adjust the signals to the operating voltages of the rest of the board $(0 - 5V)$. The outgoing data is stepped-up by the 1488 chip and incoming signals are reduced by the 1489.

The ACIA is the only peripheral chip that uses the NMI (**N**on-**M**askable **I**nterrupt) line. This allows a seperate interrupt handler to process the communications and perform command interpretation. A rudimentary "processor" handler can be developed that allows the suspending of a SECD program execution to occur. The NMI must take precedence over the IRQ for this to work so the incomming request can be processed.




Schematic 2: Communications

### 3.3 Schematic 3: Address Decoding

The 6809 is able to address 64K words of 8 bits. This space is broken down into 8K blocks as all the major memory components are made up of one (or more) 8K block. The 6809 assembly code resides in the top block. On reset, the 6809 jumps to the address stored in the top two bytes of memory ($FFFE-$FFFF). The block below contains the user and system stack for the 6809 as well as any temporary storage required by the code. The bottom half of the addressable space is reserved for accessing SECD's memory. The top 16K of this is inaddressable by SECD as SECD can only address $2^{14}$ words so it is left unused. 8K has been allocated to addressing peripheral chips. This control block is further sub-divided into 16 byte blocks of which many are unused. There is plenty of space for future expansion should it be required.

The addressing is only required when the data bus might be accessed. This occurs during the $\Phi_2$ phase of the 6809 clock. Hence the decoding is enabled by the $E$ control line.

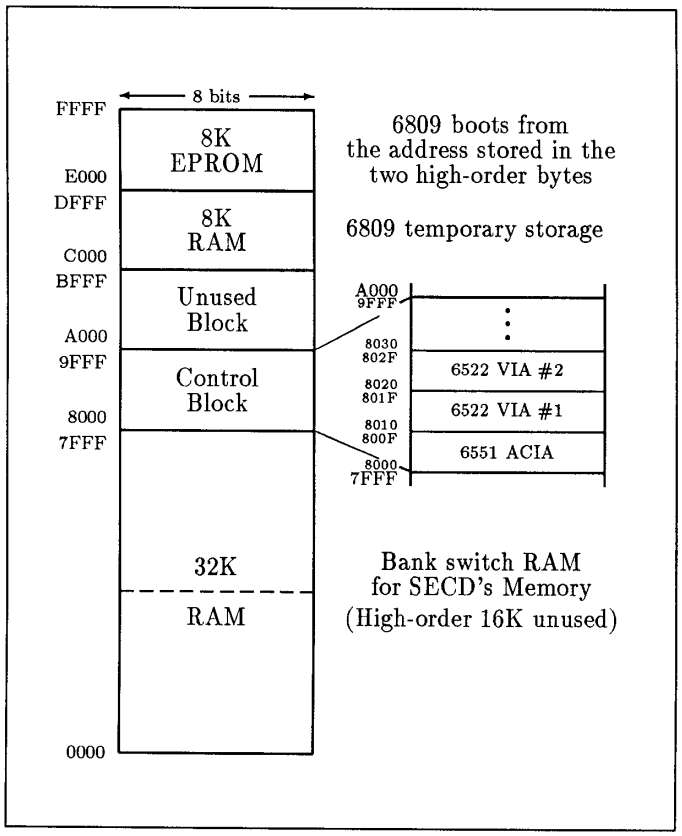
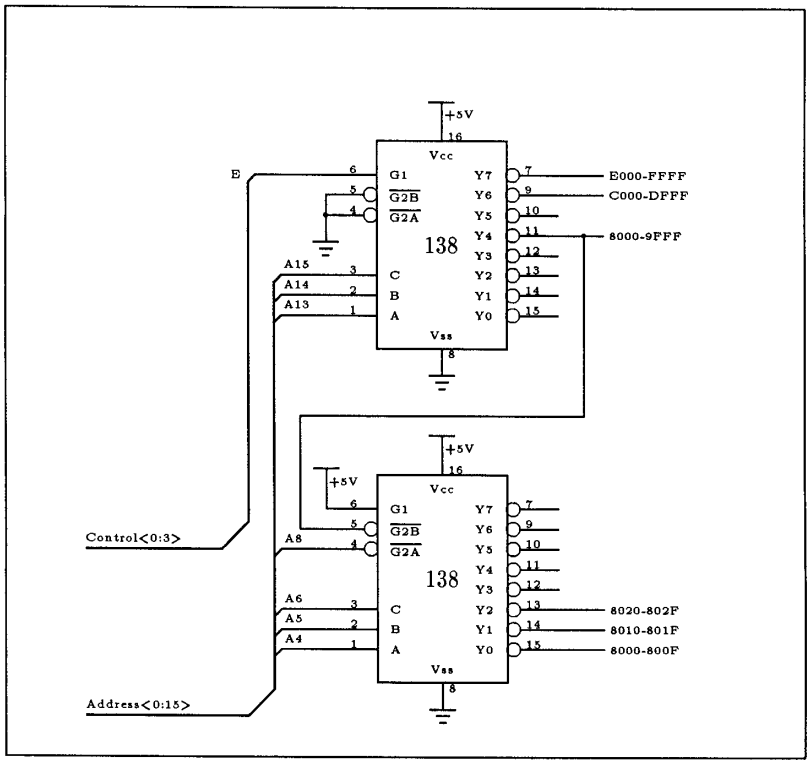



Figure 2: Microprocessor Memory Addressing Map

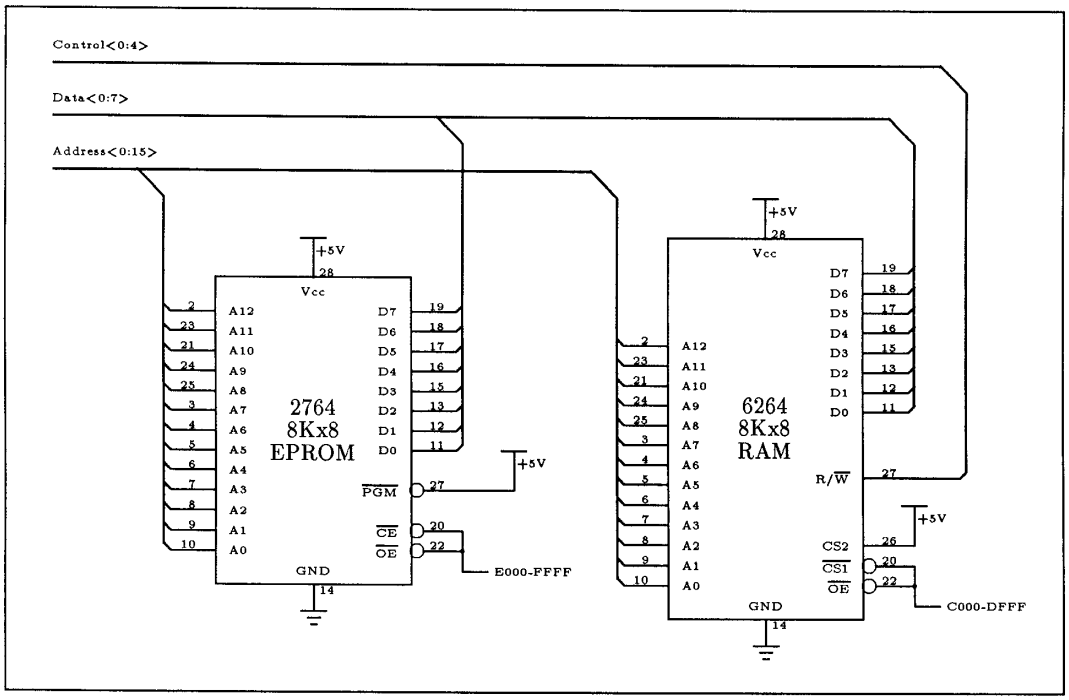



Schematic 3: Address Decoding

## 3.4 Schematic 4: Program Memory

This section describes the program memory once the development and testing of the board and the system have been completed. Up until that time a monitor program residing in EPROM is used. The use of a monitor aids in debugging the board. Any code developed is executed from RAM.

The 6809 program memory consists of two 8K blocks: one EPROM the other RAM. As mentioned above the assembly code resides in EPROM and the RAM serves as a general storage area for the $\mu$processor. They are enabled only when they are being addressed. The low order 13 bits access the required address and the data bus either reflects the contents of that address or in the case of the RAM if the *read/write* line is low the contents on the data bus gets stored at that address.




Schematic 4: Program Memory

## 3.5 Schematic 5: SECD Control Signals

Only two VIAs (**V**ersatile **I**nterface **A**dapter) are required for the control of the board and the manipulation of the SECD control signals. The VIAs are also used to read the address bus value.

VIAs were choosen over PIAs (**P**arallel **I**nterface **A**dapter) as they have built in timers. The timers count the number of $\Phi_2$ pulses of the 6809 clock. They provide a very flexible means of producing the clocks for SECD. During the testing stage the clocks need to be finely controlled. It is necessary to both cycle the clocks once and many times. The use of VIA handles this nicely.

SECD clocks can be produced on board by using either the VIAs or by a clock generation chip. There is space in the 6809 memory map to access a clock generation chip. A VIA has two built in timers. *T1* can either operate in one-shot or continuous mode. T1 affects pin seven of port B (*PB7*). PB7 can also be manually set by disenabling T1 and treating it as an output. The other timer, *T2*, only operates in one-shot mode.[7]

*PB7* of both VIAs are used as the source of SECD clocks. A two-phase non-overlapping sequence is achieved by using *T2* as a stepping clock. On each time-out of T2 the *PB7* port is manually set to a new value. It thus takes five iterations to get one clock cycle.

| | | | | | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | $\Phi_A$ |
| 0 | 1 | 0 | 0 | 0 | $\Phi_B$ |
| $T_n$ | $T_{n+1}$ | $T_{n+2}$ | $T_{n+3}$ | $T_{n+4}$ | |

This method is appropriate for single stepping SECD but requires too much overhead to be used when SECD is executing a program. A similar principle can be used. Instead of T2 acting as an interval timer in which the values of the clocks are manual set, it is used as a delay to ensure that a non-overlapping clock is achieved. Both T1s would be set to continuous mode with the same duration. One of the two clocks would be started. The other clock wouldn't be started until T2 had timed out indicating that it enough time had elapsed to ensure a correct clocking scheme.

Apart from controlling the appliction of the SECD clocks, the VIAs also controls/monitors the other SECD signals. It asserts values on the inputs and provides the means of viewing SECD's outputs. On a reset the control signals are set to their non-active state:

[7] This is not strictly true. It could also be used to count the transistions on *PB6*. We are not interested in this aspect of the T2.

| Signal | Default |
|---|---|
| Button | 0 |
| $\overline{\text{Reset}}$ | 1 |
| Test | 0 |
| Shift | 0 |
| Shin | X[8] |

They are asserted as required by the 6809 code to achieve the desired operation and control of SECD.

The VIAs also provide the means of viewing the information SECD provides to the outside world. This includes the state of SECD, the current memory access state and the value of the *shout* of the shift-register.

The flow of information in the board is also controlled by the 6809 asserting values on five of the VIAs pins. Two pins are used by the 6809 to select which bank of SECD memory is being accessed. It also provides the means of selecting the source and destination of SECD's clocks.

| ClkSrcSel | Source |
|---|---|
| 0 | Crystal |
| 1 | VIA Port |

| ClkDestSel | Destination |
|---|---|
| 0 | Shift-registers |
| 1 | System |

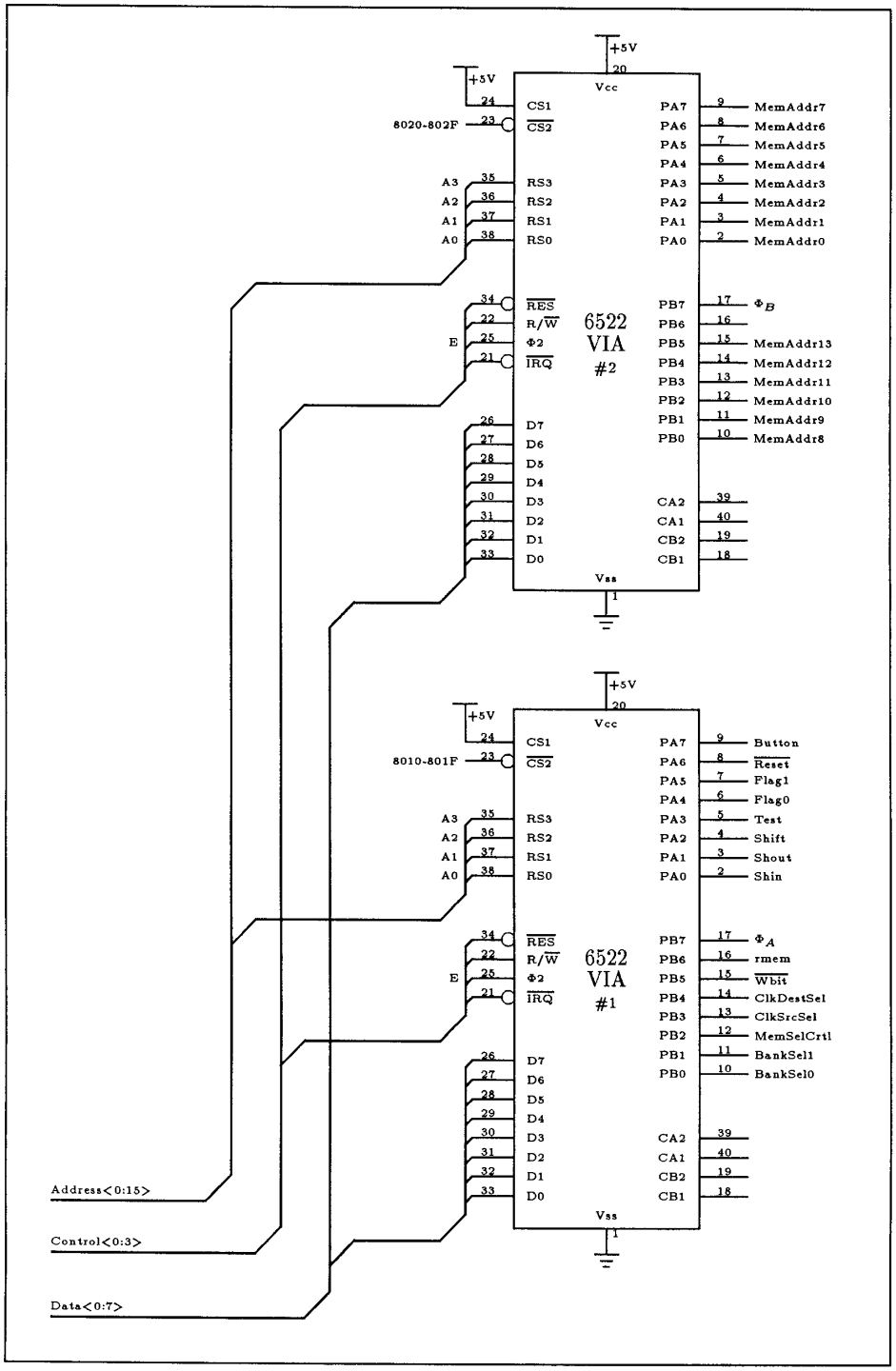
The last of the five pins controls whether the 6809 or SECD has control of SECD's memory.

| MemSelCtrl | Owner |
|---|---|
| 0 | SECD |
| 1 | 6809 |

During the testing of the SECD chips it is useful to know what address SECD is at. SECD's address can be read from the ports by stopping SECD's system clock, setting SECD to control memory (*MemSelCtrl*) and then reading the (address) value on the port.

Even though the (Motorola) 6809 provides the right clocking scheme to be used with the (Rockwell) VIA, *aka* the *E* signal, they are known not to work well in conjunction. The VIA requires a clean clocking signal. So if the 6809 *E* signal is used extensively or a large distance separates the 6809 and the VIA using the signal then the signal might not be clean enough for the VIA to work properly.

[8] It doesn't matter what value is asserted on the shin (shift-in) pin as the accessing of the shift-registers has been disabled with the above two patterns.




Schematic 5: SECD Control Signals

## 3.6 Schematic 6 & 7: SECD Memory

As mentioned before, SECD has no capacity to store its own programs. Programs are run from an external memory of 16Kx32bit RAM. The 6809 is responsible for the down-loading and up-loading of programs and results respectively. The memory must be shared by multiplexing the required signals and choosing whether the 6809 or SECD has control.

This process is further complicated by the differing word size between the two. SECD has a 32 bit data bus while the 6809 has only an 8 bit data bus. In order for the 6809 to access the memory the data must be broken into 8 bit segments. This is acheived by having *four* banks of 8 bit memories. When the 6809 accesses the memory only one of the banks is enabled. That is one of the memories and the coresponding bus driver as the output from the selected bank is tri-stated onto the 8 bit data bus. This is known as bank selecting.

SECD accesses the memory, in 32-bit words, enabling all memory banks (and tri-stated drivers). This is achieved by having SECD's control lines for the bank select signals grounded. SECD accesses the information at a different point. It must be taken before the buffers as the information after the buffer is tri-stated together (the 32 bit value is split into four groups of replicated eight signals).

The access of memory is only enabled when the 6809 is addressing SECD memory (*i.e.* when it is addressing its bottom 32K of space) or when SECD is reading or writing. The function is:

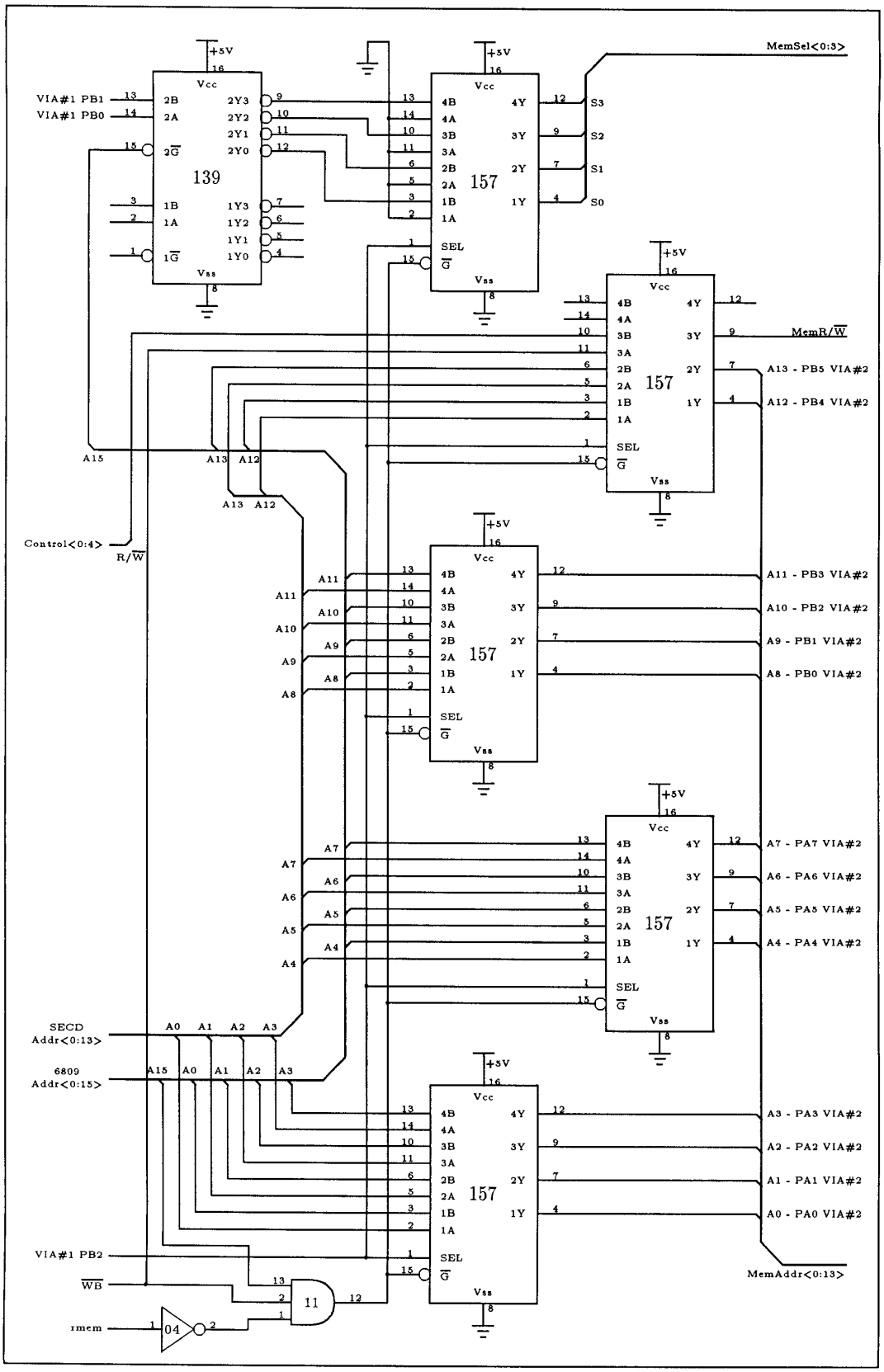
$$\mathrm{rmem} + \overline{(\overline{\mathrm{WBit}})} + \overline{\mathrm{A15}}$$

The memory and drivers enable signals are low:

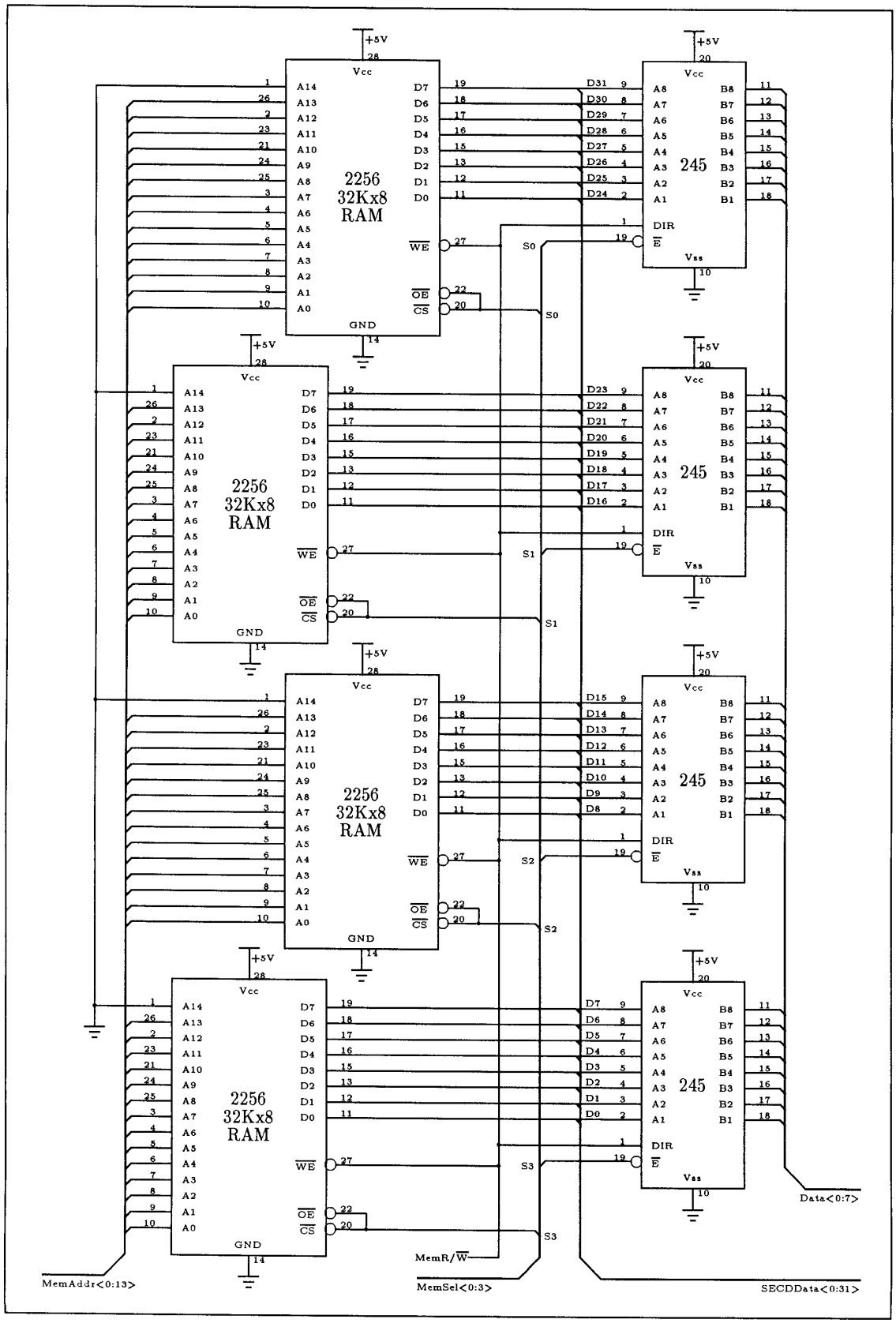
$$\overline{\mathrm{rmem} + \overline{(\overline{\mathrm{WBit}})} + \overline{\mathrm{A15}}}$$

so the implemented function is:

$$\overline{\mathrm{rmem}} \cdot \overline{\mathrm{WBit}} \cdot \mathrm{A15}$$




Schematic 6: Mulitplexing SECD's Memory

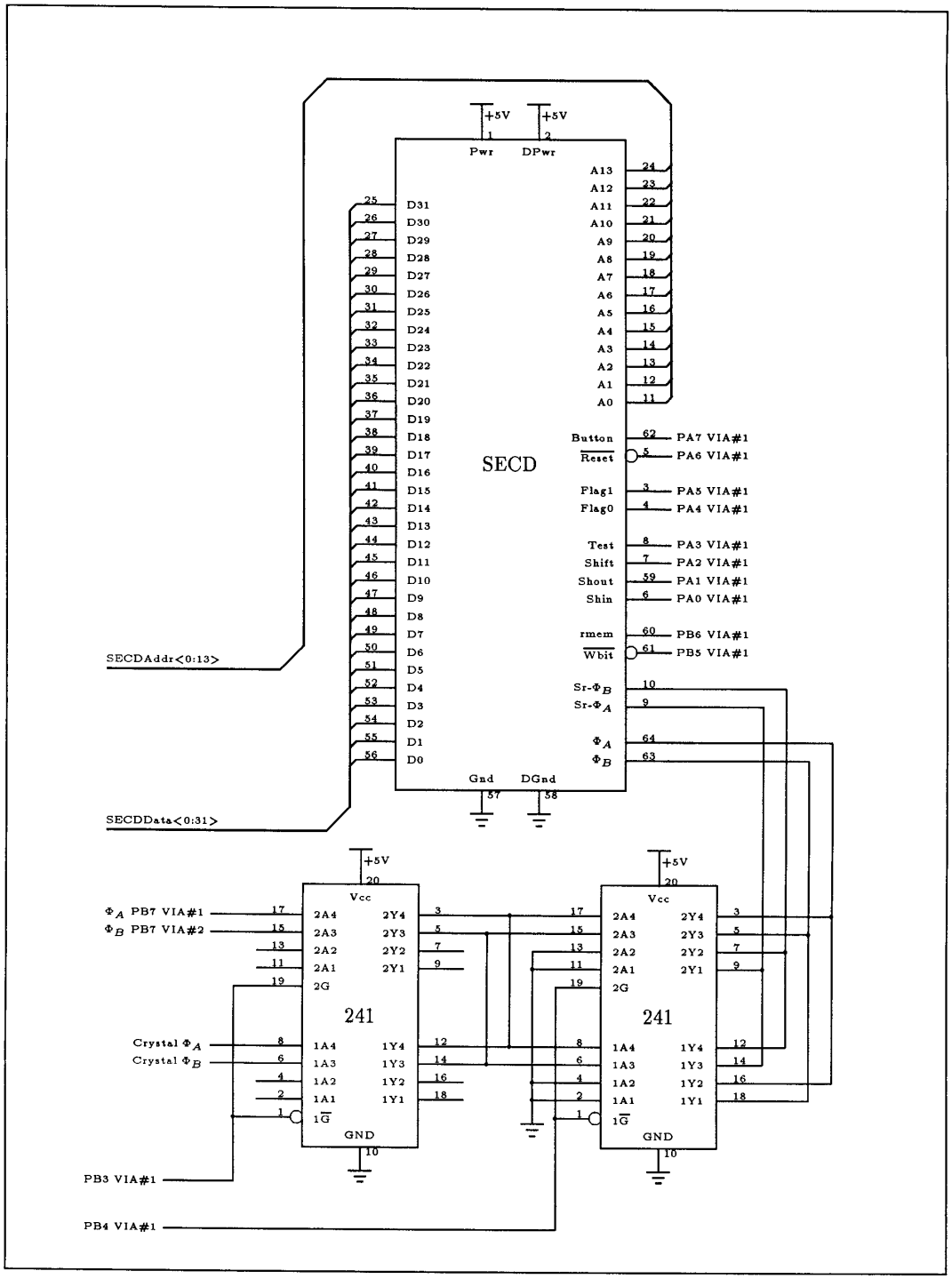



Schematic 7: SECD's Memory

## 3.7 Schematic 8: SECD

Much of this figure has been dealt with in the description of the signals that the VIAs handle.

The control circuit for the clocks is displayed in this portion of the board. Two sources of four clock lines are multiplexed onto a common pair. This is then demultiplexed to either the shift-register or system clocks of SECD. The two select signals come from a VIA port. Two buffer drivers were used to implement this system as less components are required than using multiplexers/demultiplexers. The *ClkSrcSel* determines the which source for the clock is put on the interconnected tristated output lines of the buffer. These signals are fed into the other buffer. The destination is controlled by the *ClkDestSel* signal. The other inputs are grounded to ensure that the clock signals that are not active are not floating. This is done by interconnecting opposite pairs of signals on the output lines.




Schematic 8: SECD

## 4 Conclusion

As a design exercise in both hardware verification and chip fabrication a specialised architecture to run compiled Lispkit code (from a system developed in the Computer Science Department of the University of Calgary). To validate the design a development board has been implemented. This document details the nuances of this board with respect to its two tasks: chip testing and usage.

## 5 Acknowledgements

I am pleased to acknowledge the many people have had a hand in this project, wittingly or otherwise. Jeff Joyce, Rick Schediwy and Glen Stone provided a ready example of a test board in their 1986 work on the Tamarack chip tester. Glen Stone had the first cut at designing this SECD test system in 1988 and his sound design and documentation work formed a solid and reliable platform for my work. Brian Graham patiently explained the SECD clocking scheme and many other details. Simon Williams helped enormously in developing test sequences and in discussing various development strategies and options. Mike Hermann was also very helpful in suggesting and discussing possible approaches. Gerald Vaselenak, Karen Ritchie and Tim Bliek, the departmental Technical Support team did most of the board testing, and provided continual help in its debugging. Dave Hankinson wrote the Sun side of the communication channel.

Without their help things wouldn't have gone so smoothly and I am deeply indebted to them all. Thanks, guys.

## References


[1] G. Birtwistle, B. Graham, J. Joyce, S. Williams, M. Brinsmead, M. Keefe, W. Kroeker, B. Liblong, and W. Vollmerhaus. The SECD MACHINE on a CHIP. Research report 89/354/16, Computer Science Department, University of Calgary, 1989. to be published in the Proc. Int. Conf. on CAD and CG, Beijing,1989.

[2] B. Graham, S. Williams, G. Birtwistle, J. Joyce, and B. Liblong. The Mossim Specification of the SECD DESIGN. Research report 89/341/03, Computer Science Department, University of Calgary, 1989.

[3] B. Graham, S. Williams, and G. Stone. Operating Specification for the SECD Chip. Research report 89/353/15, Computer Science Department, University of Calgary, 1989.

[4] Peter Henderson. *Functional Programming Application and Implementation.* Prentice/Hall International, 1980.

[5] M. J. Hermann, G. Birtwistle, B. Graham, and T. Simpson. The Architecture of Henderson's SECD Machine. Research report 89/340/02, Computer Science Department, University of Calgary, 1989.

[6] P. J. Landin. The mechanical evaluation of expressions. *The Computer Journal*, 6(4):308–320, 1964.

[7] T. Simpson, G. Birtwistle, B. Graham, and M. J. Hermann. A Compiler for Lispkit Targetted at Henderson's SECD machine. Research report 89/339/01, Computer Science Department, University of Calgary, 1989.

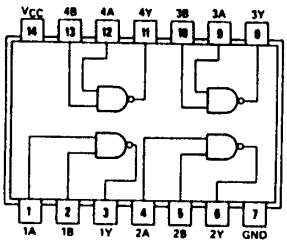
## PIN ASSIGNMENTS (TOP VIEWS)

**QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

# 03

positive logic:
$Y = \overline{AB}$

See page 6-4




SN5403 (J)
SN54L03 (J)
SN54LS03 (J, W)
SN54S03 (J, W)

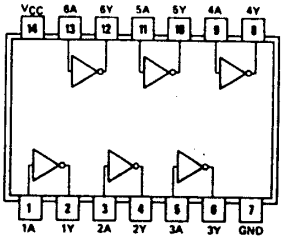
SN7403 (J, N)
SN74L03 (J, N)
SN74LS03 (J, N)
SN74S03 (J, N)

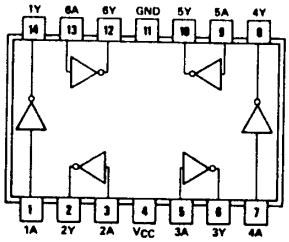
**HEX INVERTERS**

# 04

positive logic:
$Y = \overline{A}$

See page 6-2




SN5404 (J)
SN54H04 (J)
SN54L04 (J)
SN54LS04 (J, W)
SN54S04 (J, W)

SN7404 (J, N)
SN74H04 (J, N)
SN74L04 (J, N)
SN74LS04 (J, N)
SN74S04 (J, N)

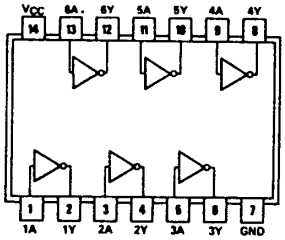
SN5404 (W)
SN54H04 (W)
SN54L04 (T)

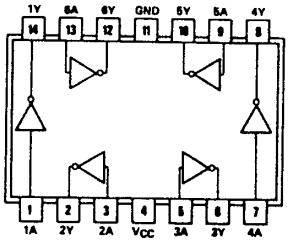
**HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

# 05

positive logic:
$Y = \overline{A}$

See page 6-4




SN5405 (J)
SN54H05 (J)
SN54LS05 (J, W)
SN54S05 (J, W)

SN7405 (J, N)
SN74H05 (J, N)
SN74LS05 (J, N)
SN74S05 (J, N)

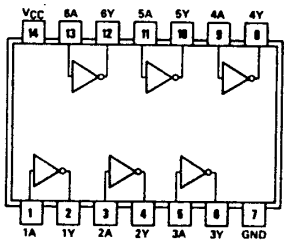
SN5405 (W)
SN54H05 (W)

**HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS**

# 06

positive logic:
$Y = \overline{A}$

See page 6-24




SN5406 (J, W)
SN7406 (J, N)

5

076

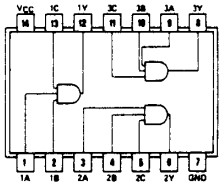
## PIN ASSIGNMENTS (TOP VIEWS)

**TRIPLE 3-INPUT POSITIVE-AND GATES**

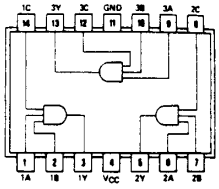
**11**

positive logic:
Y = ABC

See page 6-10



SN54H11 (J) SN74H11 (J, N)
SN54LS11 (J, W) SN74LS11 (J, N)
SN54S11 (J, W) SN74S11 (J, N)



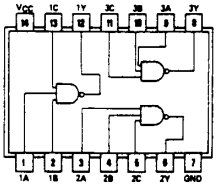
SN54H11 (W)

**TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

**12**

positive logic:
$Y = \overline{ABC}$

See page 6-4



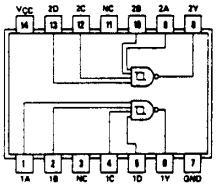
SN5412 (J, W) SN7412 (J, N)
SN54LS12 (J, W) SN74LS12 (J, N)

**DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS**

**13**

positive logic:
$Y = \overline{ABCD}$

See page 6-14



SN5413 (J, W) SN7413 (J, N)
SN54LS13 (J, W) SN74LS13 (J, N)

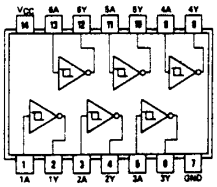
NC—No internal connection

**HEX SCHMITT-TRIGGER INVERTERS**

**14**

positive logic:
$Y = \overline{A}$

See page 6-14



SN5414 (J, W) SN7414 (J, N)
SN54LS14 (J, W) SN74LS14 (J, N)

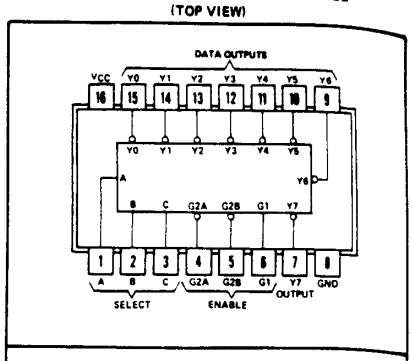
# TYPES SN54LS138, SN54LS139, SN54S138, SN54S139, SN74LS138, SN74LS139, SN74S138, SN74S139 DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7611804, DECEMBER 1972–REVISED OCTOBER 1976

- Designed Specifically for High-Speed:
  - Memory Decoders
  - Data Transmission Systems
- 'S138 and 'LS138 3-to-8-Line Decoders Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Reception
- 'S139 and 'LS139 Contain Two Fully Independent 2-to-4-Line Decoders/Demultiplexers
- Schottky Clamped for High Performance

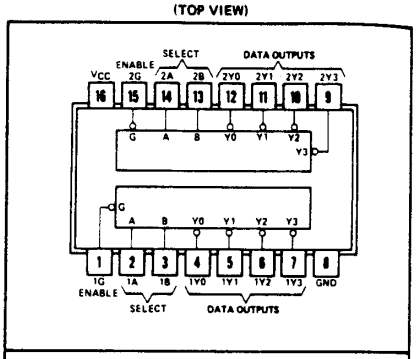
| TYPE | TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC) | TYPICAL POWER DISSIPATION |
|---|---|---|
| 'LS138 | 22 ns | 32 mW |
| 'S138 | 8 ns | 245 mW |
| 'LS139 | 22 ns | 34 mW |
| 'S139 | 7.5 ns | 300 mW |

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . J OR N PACKAGE
(TOP VIEW)




positive logic: see function table

SN54LS139, SN54S139 . . . J OR W PACKAGE
SN74LS139, SN74S139 . . . J OR N PACKAGE
(TOP VIEW)




positive logic: see function table

## description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 'LS139 and 'S139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs each of which represents only one normalized Series 54LS/74LS load ('LS138, 'LS139) or one normalized Series 54S/74S load ('S138, 'S139) to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design. Series 54LS and 54S devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74LS and 74S devices are characterized for 0°C to 70°C industrial systems.



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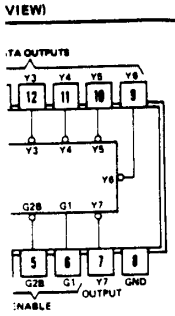
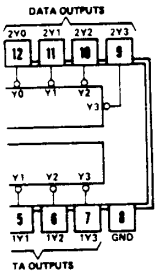
3 . . . J OR W PACKAGE
3 . . . J OR N PACKAGE
VIEW)




ee function table

. . J OR W PACKAGE
. . J OR N PACKAGE
IEW)




function table

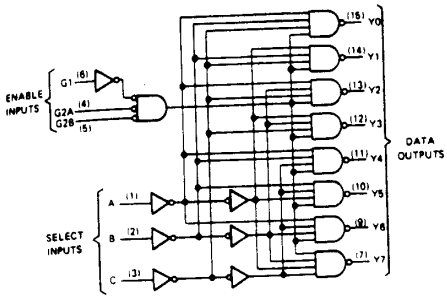
ckage. The active-low enable

s only one normalized Series
9) to its driving circuit. All
mplify system design. Series
range of −55°C to 125°C;

# TYPES SN54LS138, SN54S138, SN54LS139, SN54S139 SN74LS138, SN74S138, SN74LS139, SN74S139 DECODERS/DEMULTIPLEXERS

## functional block diagrams and logic

'LS138, 'S138

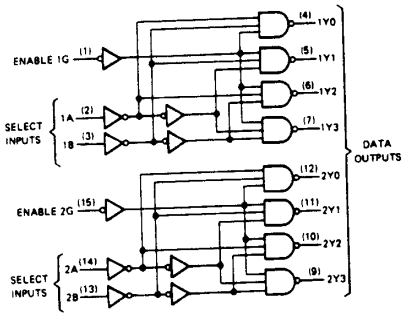



'LS138, 'S138
FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ENABLE | | SELECT | | | | | | | | | | |
| G1 | G2* | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

'LS139, 'S139



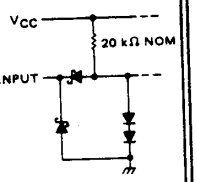

'LS139, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| ENABLE | SELECT | | | | | |
| G | B | A | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

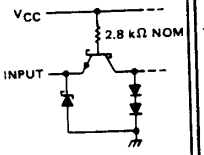
H = high level, L = low level, X = irrelevant

## schematics of inputs and outputs

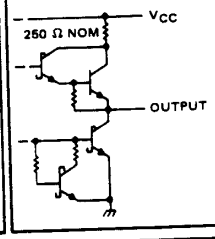
EQUIVALENT OF EACH INPUT OF 'LS138, 'LS139



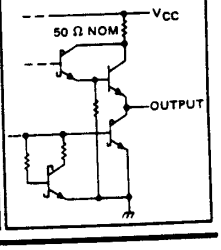

EQUIVALENT OF EACH INPUT OF 'S138, 'S139




TYPICAL OF OUTPUTS OF 'LS138, 'LS139




TYPICAL OF OUTPUTS OF 'S138, 'S139



S

| 54LS156 | | SN74LS156 | | | UNIT |
|---|---|---|---|---|---|
| NOM | MAX | MIN | NOM | MAX | |
| 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| | 5.5 | | | 5.5 | V |
| | 4 | | | 8 | mA |
| | 125 | 0 | | 70 | °C |

range (unless otherwise noted)

| 4LS156 | | SN74LS156 | | | UNIT |
|---|---|---|---|---|---|
| TYP‡ | MAX | MIN | TYP‡ | MAX | |
| | | 2 | | | V |
| | 0.7 | | | 0.8 | V |
| | −1.5 | | | −1.5 | V |
| | 100 | | | 100 | μA |
| .25 | 0.4 | | 0.25 | 0.4 | V |
| | | | 0.35 | 0.5 | |
| | 0.1 | | | 0.1 | mA |
| | 20 | | | 20 | μA |
| | −0.4 | | | −0.4 | mA |
| .1 | 10 | | 6.1 | 10 | mA |

ating conditions.

ts grounded.

| | SN54LS156 SN74LS156 | | | UNIT |
|---|---|---|---|---|
| | MIN | TYP | MAX | |
| | | 25 | 40 | ns |
| | | 34 | 51 | ns |
| | | 31 | 46 | ns |
| | | 34 | 51 | ns |
| | | 32 | 48 | ns |
| | | 32 | 48 | ns |

# TYPES SN54157, SN54L157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74L157, SN74LS157, SN74LS158, SN74S157, SN74S158 QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7711847, MARCH 1974–REVISED AUGUST 1977

## features

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

| TYPES | TYPICAL AVERAGE PROPAGATION TIME | TYPICAL POWER DISSIPATION |
|---|---|---|
| '157 | 9 ns | 150 mW |
| 'L157 | 18 ns | 75 mW |
| 'LS157 | 9 ns | 49 mW |
| 'S157 | 5 ns | 250 mW |
| 'LS158 | 7 ns | 24 mW |
| 'S158 | 4 ns | 195 mW |

## applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

## description

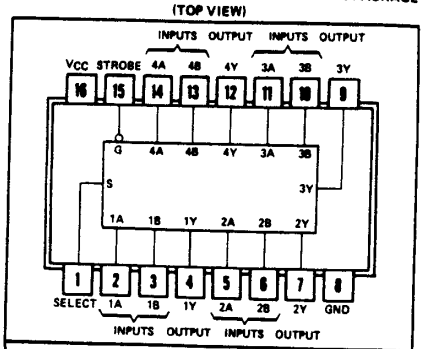
These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

| INPUTS | | | | OUTPUT Y | |
|---|---|---|---|---|---|
| STROBE | SELECT | A | B | '157, 'L157, 'LS157, 'S157 | 'LS158 'S158 |
| H | X | X | X | L | H |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

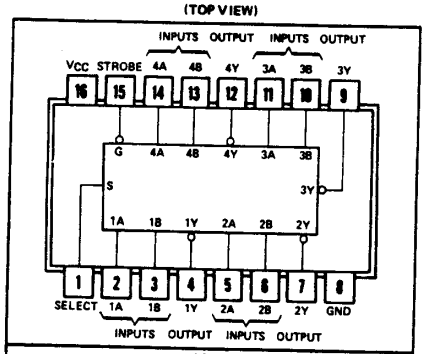
H = high level, L = low level, X = irrelevant

SN54157, SN54LS157, SN54S157 . . . J OR W PACKAGE
SN54L157 . . . J PACKAGE
SN74157, SN74L157, SN74LS157, SN74S157 . . . J OR N PACKAGE
(TOP VIEW)




positive logic:
Low level at S selects A inputs
High level at S selects B inputs

SN54LS158, SN54S158 . . . J OR W PACKAGE
SN74LS158, SN74S158 . . . J OR N PACKAGE
(TOP VIEW)




positive logic:
Low level at S selects A inputs
High level at S selects B inputs

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: '157, 'L157, 'S158 . . . . . 5.5 V
'LS157, 'LS158 . . . . . 7 V
Operating free-air temperature range: SN54', SN54L', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

# TYPES SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241
# OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

| | Typical $I_{OL}$ (Sink Current) | Typical $I_{OH}$ (Source Current) | Typical Propagation Delay Times | | Typical Enable/ Disable Times | Typical Power Dissipation (Enabled) | |
|---|---|---|---|---|---|---|---|
| | | | Inverting | Noninverting | | Inverting | Noninverting |
| SN54LS' | 12 mA | −12 mA | 10.5 ns | 12 ns | 18 ns | 130 mW | 135 mW |
| SN74LS' | 24 mA | −15 mA | 10.5 ns | 12 ns | 18 ns | 130 mW | 135 mW |
| SN54S' | 48 mA | −12 mA | 4.5 ns | 6 ns | 9 ns | 450 mW | 538 mW |
| SN74S' | 64 mA | −15 mA | 4.5 ns | 6 ns | 9 ns | 450 mW | 538 mW |

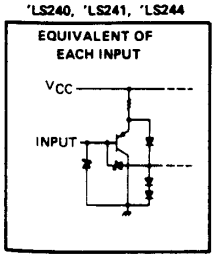
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

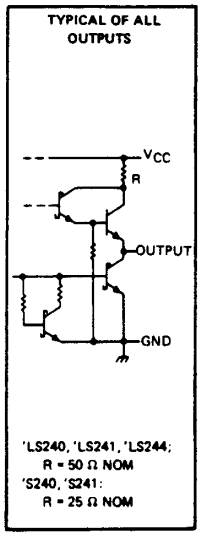
## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

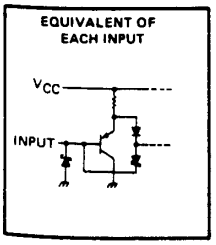
## schematics of inputs and outputs

'LS240, 'LS241, 'LS244

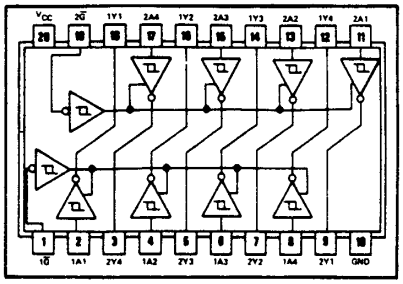


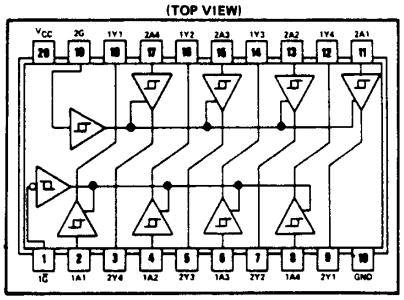

'S240 'S241



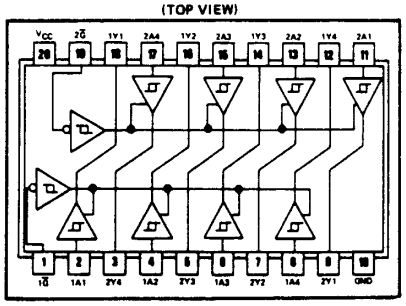

SN54LS240, SN54S240 . . . J
SN74LS240, SN74S240 . . . J OR N
(TOP VIEW)




SN54LS241, SN54S241 . . . J
SN74LS241, SN74S241 . . . J OR N
(TOP VIEW)




SN54LS244 . . . J
SN74LS244 . . . J OR N
(TOP VIEW)



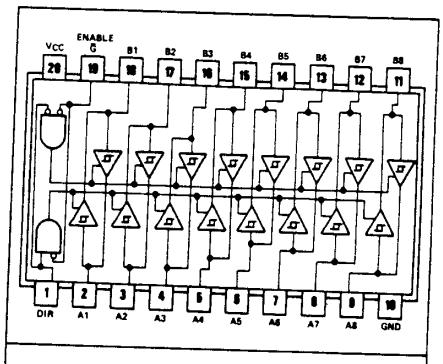
# TYPES SN54LS245, SN74LS245
# OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12471, OCTOBER 1976—REVISED FEBRUARY 1979

- Bi-directional Bus Transceiver in a High-Density 20-Pin Package
- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce D-C Loading on Bus Lines
- Hysteresis at Bus Inputs Improve Noise Margins
- Typical Propagation Delay Times, Port-to-Port . . . 8 ns
- Typical Enable/Disable Times . . . 17 ns

| TYPE | $I_{OL}$ (SINK CURRENT) | $I_{OH}$ (SOURCE CURRENT) |
|---|---|---|
| SN54LS245 | 12 mA | −12 mA |
| SN74LS245 | 24 mA | −15 mA |

SN54LS245 . . . J PACKAGE
SN74LS245 . . . J OR N PACKAGE
(TOP VIEW)




positive logic: see function table

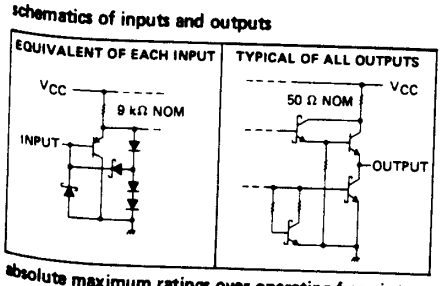
## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54LS245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS245 is characterized for operation from 0°C to 70°C.

## schematics of inputs and outputs




FUNCTION TABLE

| ENABLE $\overline{G}$ | DIRECTION CONTROL DIR | OPERATION |
|---|---|---|
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

H = high level, L = low level, X = irrelevant

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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# Line Drivers/Receivers

NATIONAL

## DS1488 quad line driver

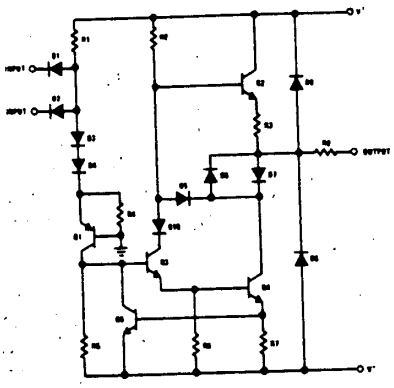
### general description

The DS1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V. 24.

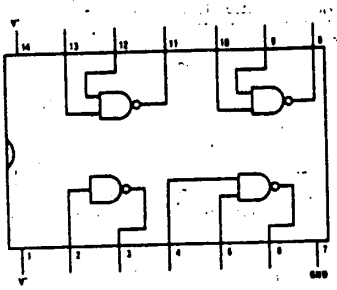
### features

- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

### schematic and connection diagrams



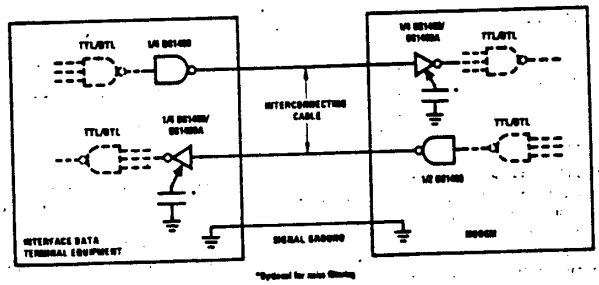
Dual-In-Line Package



Order Number DS1488J

### typical applications

RS232C Data Transmission



NATIONAL

# Line Drivers/Receivers

## DS1489/DS1489A quad line receiver

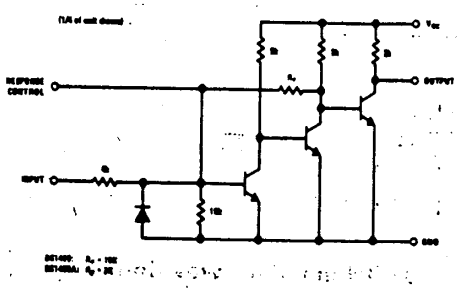
### general description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements. The DS1489/DS1489A are available in 14-lead ceramic dual-in-line package.

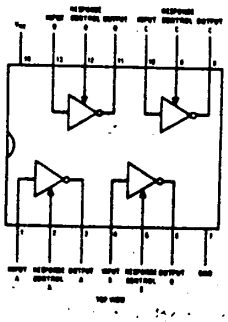
### features

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

### schematic and connection diagrams

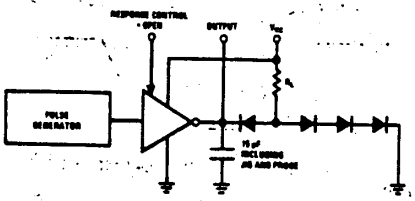


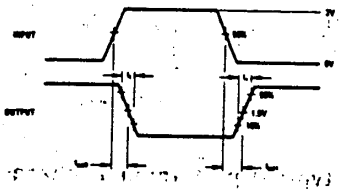
Dual-In-Line Package



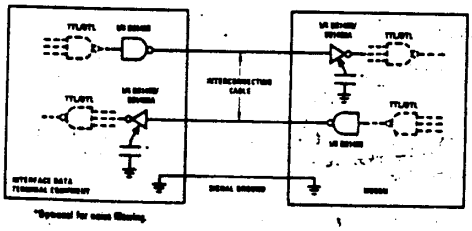
Order Number DS1489J or DS1489AJ

### ac test circuit and voltage waveforms

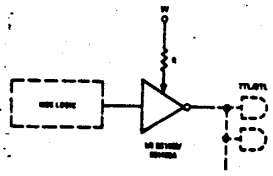




### typical applications



RS232C Data Transmission



MOS to TTL/DTL Translator

SHARP

Sharp Electronics Corporation
Sharp Plaza
Mahwah, New Jersey 07430
(201) 529-8757

# LH52256-55/-70/-90/-12/-15

## MOS 262144-Bit Static Random Access Memory

### Description

The LH52256/LH52256L are fully static RAMs organized as 32,768×8-bit by using silicon-gate CMOS process technology.

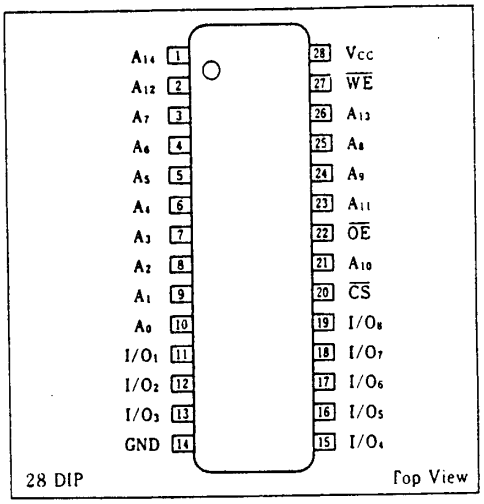
### Features

Access time (MAX.)
- LH52256-55····· 55ns
- LH52256-70····· 70ns
- LH52256-90····· 90ns
- LH52256-12·····120ns
- LH52256-15·····150ns

Low power consumption (MAX.)
- Operating mode:
  - LH52256-55/-70·····80mA
  - LH52256-90/-12/-15·····70mA
- Standby mode: LH52256 ·····2mA
- Low power type
  - Standby mode: LH52256L·····0.1mA

- Single +5V power supply
- Fully static operation
- All inputs and outputs TTL compatible
- Three-state output
- 28-pin dual-in-line package

### Pin Connections

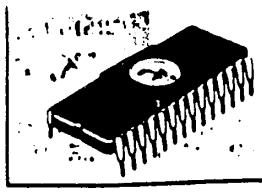



### Pin Description

| Signal | Pin name |
|---|---|
| $A_0 \sim A_{14}$ | Address inputs |
| $\overline{CS}$ | Chip select |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| $I/O_1 \sim I/O_8$ | Data inputs and outputs |
| $V_{CC}$ | Power supply |
| GND | Ground |

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Mode | $I/O_1 \sim I/O_8$ |
|---|---|---|---|---|
| H | X | X | Deselect | High Z |
| L | H | L | Read | $D_{OUT}$ |
| L | H | H | Read | High Z |
| L | L | L | Write | $D_{IN}$ |

Sharp Electronics





# M5L2764K, -2

## 65536-BIT (8192-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

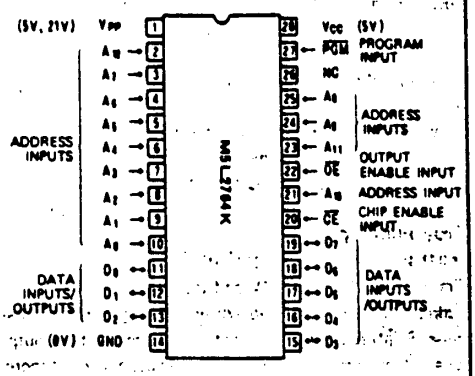
## DESCRIPTION

The Mitsubishi M5L2764K is a high-speed 65536-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L2764K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIL package with a transparent lid.

## FEATURES

- 8192 Word x 8-bit Organization
- Access Time M5L2764K-2 200 ns (Max)
  M5L2764K 250 ns (Max)
- Two Line Control $\overline{OE}$, $\overline{CE}$
- Low Power Current ($I_{CC}$) Active .....150 mA (Max)
  Standby .... 35 mA (Max)
- Single 5V Power Supply
- 3-State Output Buffer
- Input and Output TTL-Compatible in Read and Program Mode
- Standard 28-pin DIL Package
- Single Location Programming with One 50 ms Pulse
- Fast programming algorithm
- Interchangeable with INTEL 2764

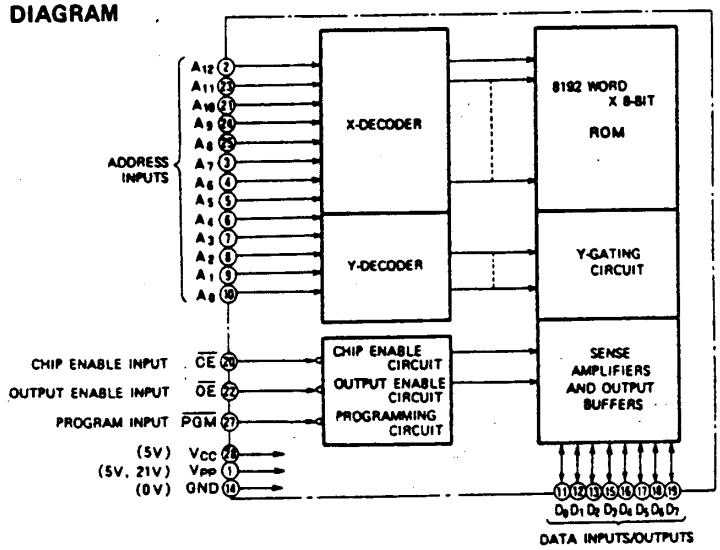
## PIN CONFIGURATION (TOP VIEW)




NC : NO CONNECTION

Outline 28K1

## BLOCK DIAGRAM

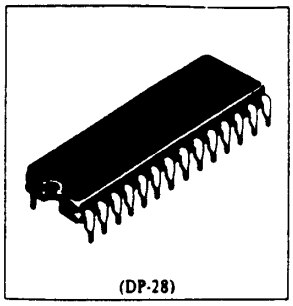


# HM6264LP-10, HM6264LP-12, HM6264LP-15
# 8192-word × 8-bit High Speed Static CMOS RAM

HITACHI

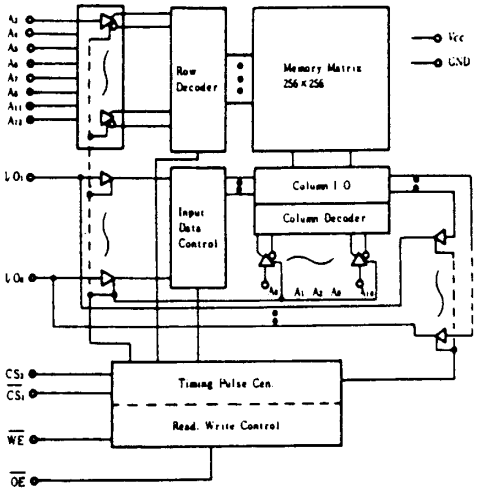
## ■ FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.01mW (typ.)
  Low Power Operation — Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory..... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

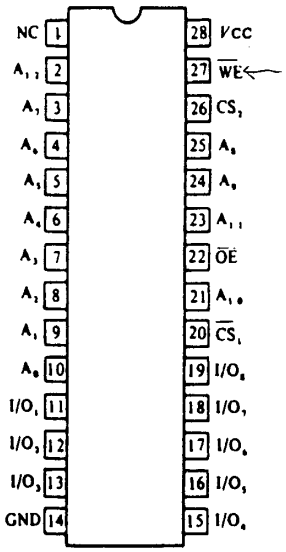


(DP-28)

## ■ BLOCK DIAGRAM




## ■ PIN ARRANGEMENT




(Top View)

## ■ ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Terminal Voltage * | $V_T$ | −0.5 ** to +7.0 | V |
| Power Dissipation | $P_T$ | 1.0 | W |
| Operating Temperature | $T_{opr}$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +125 | °C |
| Storage Temperature (Under Bias) | $T_{bias}$ | −10 to +85 | °C |

* With respect to GND. ** Pulse width 50ns: −3.0V

## ■ TRUTH TABLE

| $\overline{WE}$ | $\overline{CS_1}$ | $CS_2$ | $\overline{OE}$ | Mode | I/O Pin | $V_{CC}$ Current | Note |
|---|---|---|---|---|---|---|---|
| X | H | X | X | Not Selected (Power Down) | High Z | $I_{SB}$, $I_{SB1}$ | |
| X | X | L | X | | High Z | $I_{SB}$, $I_{SB2}$ | |
| H | L | H | H | Output Disabled | High Z | $I_{CC}$, $I_{CC1}$ | |
| H | L | H | L | Read | Dout | $I_{CC}$, $I_{CC1}$ | |
| L | L | H | H | Write | Din | $I_{CC}$, $I_{CC1}$ | Write Cycle (1) |
| L | L | H | L | | Din | $I_{CC}$, $I_{CC1}$ | Write Cycle (2) |

X: H or L


HITACHI AMERICA, LTD. Semiconductor and IC Sales and Service Division
2210 O'Toole Avenue, San Jose, CA 95131 • (408) 942-1500
TELEX: 17-1581 TWX: 910-338-2103

Rockwell

# R6522 VERSATILE INTERFACE ADAPTER (VIA)

## DESCRIPTION

The R6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bidirectional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting exter-nally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

## FEATURES

- Two 8-bit bidirectional I/O ports
- Two 16-bit programmable timer/counters
- Serial data port
- TTL compatible
- CMOS compatible peripheral control lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices.
- Latched output and input registers
- 1 MHz and 2 MHz operation
- Single +5V power supply

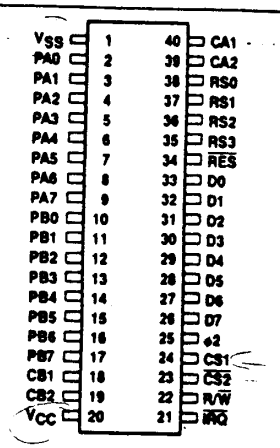
## ORDERING INFORMATION

Part Number:
R6522

Temperature Range
Blank = 40°C to +70°C
E = 40°C to +85°C

Package
C = Ceramic
P = Plastic

Frequency
No Letter = 1 MHz
A = 2 MHz



R6522 Pin Configuration

# R6551
# ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

## DESCRIPTION

The Rockwell R6551 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at $^1/_{16}$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $^1/_{16}$ times the external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R6551's operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receiver circuits.

## ORDERING INFORMATION

Part No.: R6551

- Temperature Range ($T_L$ to $T_H$):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range:
  - 1 = 1 MHz
  - 2 = 2 MHz
- Package:
  - C = Ceramic
  - P = Plastic

## FEATURES

- Compatible with 8-bit microprocessors
- Full duplex operation with buffered receiver and transmit
- Data set/modem control functions
- Internal baud rate generator with 15 programmable b rates (50 to 19,200)
- Program-selectable internally or externally controlled rece rate
- Programmable word lengths, number of stop bits, and pa bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 2 or 1 MHz operation
- 5.0 Vdc ± 5% supply requirements
- 28-pin plastic or ceramic DIP
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 mic processors

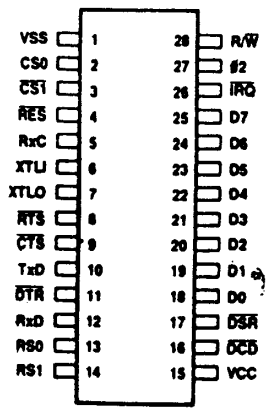



Figure 1. R6551 ACIA Pin Configuration

MOTOROLA

# MC6809
(1.0 MHz)
# MC68A09
(1.5 MHz)
# MC68B09
(2.0 MHz)

## HMOS

(HIGH DENSITY N-CHANNEL, SILICON-GATE)

8-BIT
MICROPROCESSING
UNIT

### 8-BIT MICROPROCESSING UNIT

The MC6809 is a revolutionary high-performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the M6800 family has major architectural improvements which include additional registers, instructions, and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The MC6809 has the most complete set of addressing modes available on any 8-bit microprocessor today.

The MC6809 has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications.

**MC6800 COMPATIBLE**
- Hardware – Interfaces with All M6800 Peripherals
- Software – Upward Source Code Compatible Instruction Set and Addressing Modes

**ARCHITECTURAL FEATURES**
- Two 16-bit Index Registers
- Two 16-bit Indexable Stack Pointers
- Two 8-bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

**HARDWARE FEATURES**
- On-Chip Oscillator (Crystal Frequency = 4XE)
- $\overline{\text{DMA}}/\overline{\text{BREQ}}$ Allows DMA Operation on Memory Refresh
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- MRDY Input Extends Data Access Times for Use with Slow Memory
- Interrupt Acknowledge Output Allows Vectoring By Devices
- SYNC Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle $\overline{\text{RESET}}$
- Single 5-Volt Supply Operation
- $\overline{\text{NMI}}$ Inhibited After $\overline{\text{RESET}}$ Until After First Load of Stack Pointer
- Early Address Valid Allows Use With Slower Memories
- Early Write-Data for Dynamic Memories

**SOFTWARE FEATURES**
- 10 Addressing Modes
  - 6800 Upward Compatible Addressing Modes
  - Direct Addressing Anywhere in Memory Map
  - Long Relative Branches
  - Program Counter Relative
  - True Indirect Addressing
  - Expanded Indexed Addressing:
    - 0-, 5-, 8-, or 16-bit Constant Offsets
    - 8-, or 16-bit Accumulator Offsets
    - Auto-Increment/Decrement by 1 or 2
- Improved Stack Manipulation
- 1464 Instructions with Unique Addressing Modes
- 8 × 8 Unsigned Multiply
- 16-bit Arithmetic
- Transfer/Exchange All Registers
- Push/Pull Any Registers or Any Set of Registers
- Load Effective Address

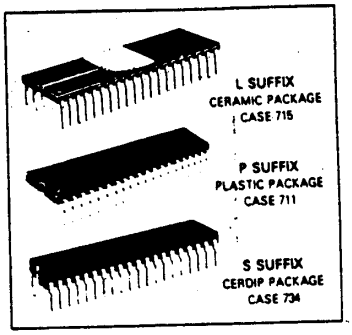
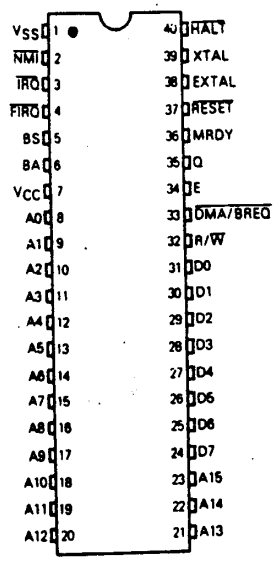



FIGURE 1 – PIN ASSIGNMENT



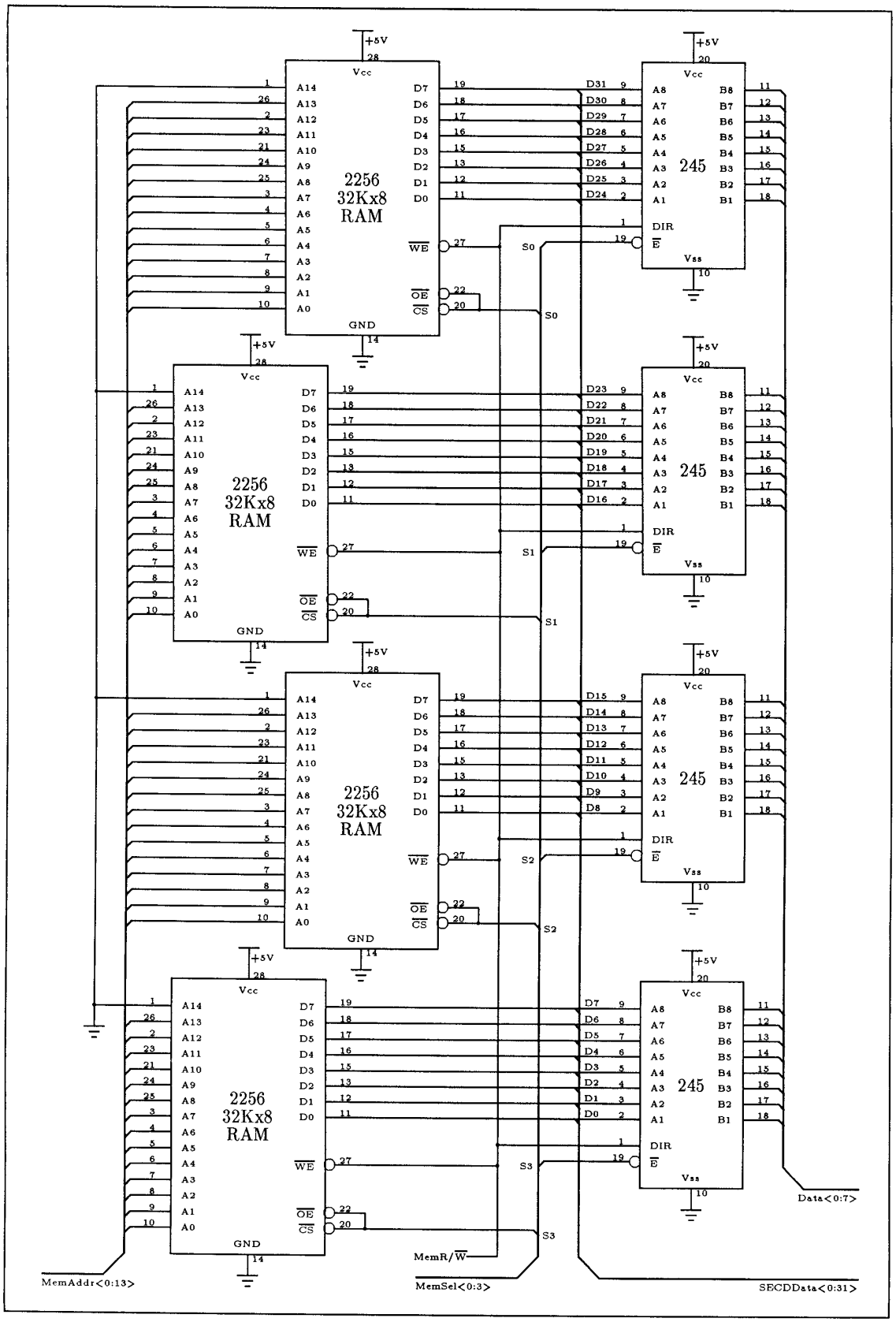



Figure 7: SECD's Memory

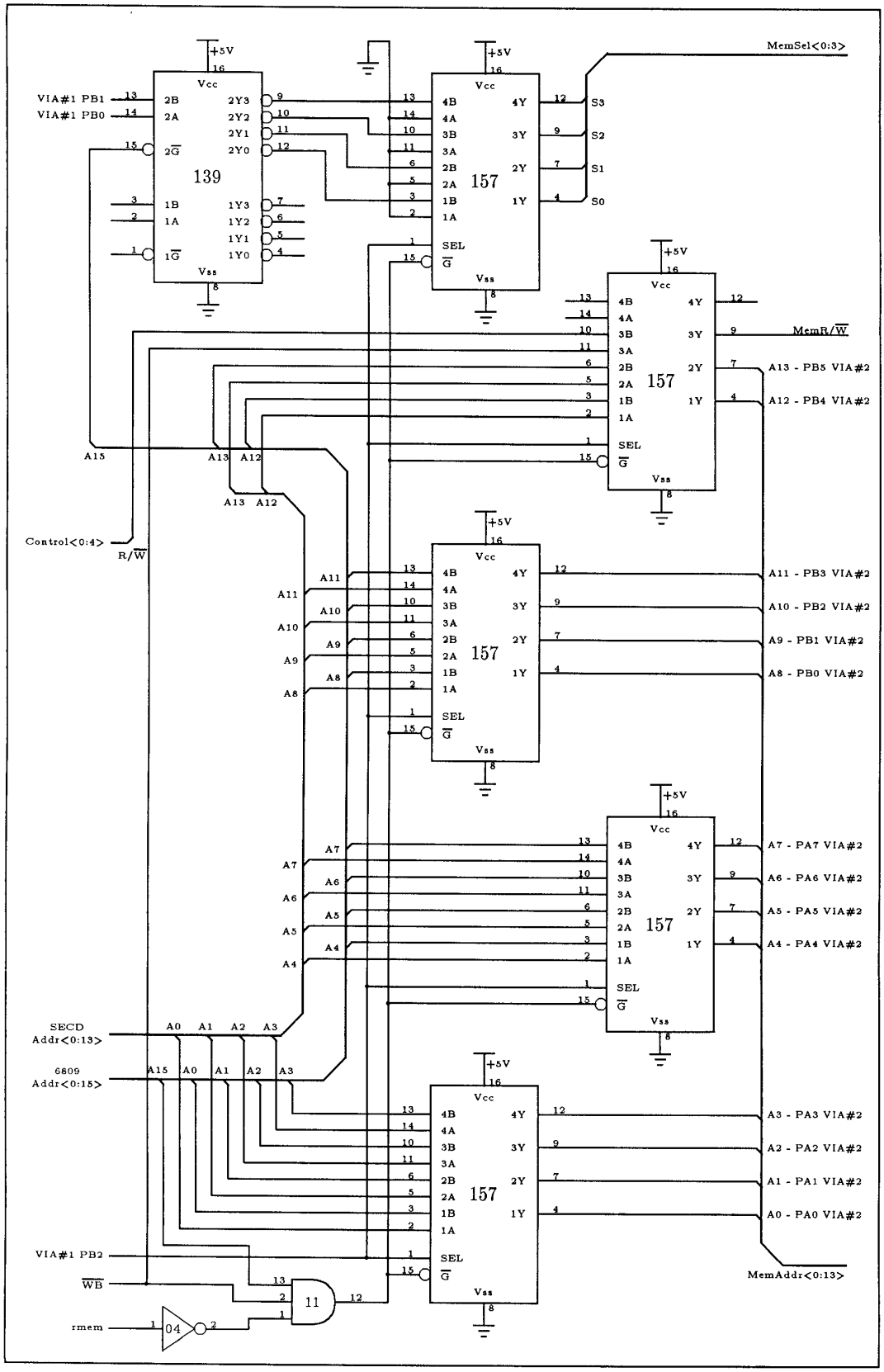



Figure 6: Mulitplexing SECD's Memory

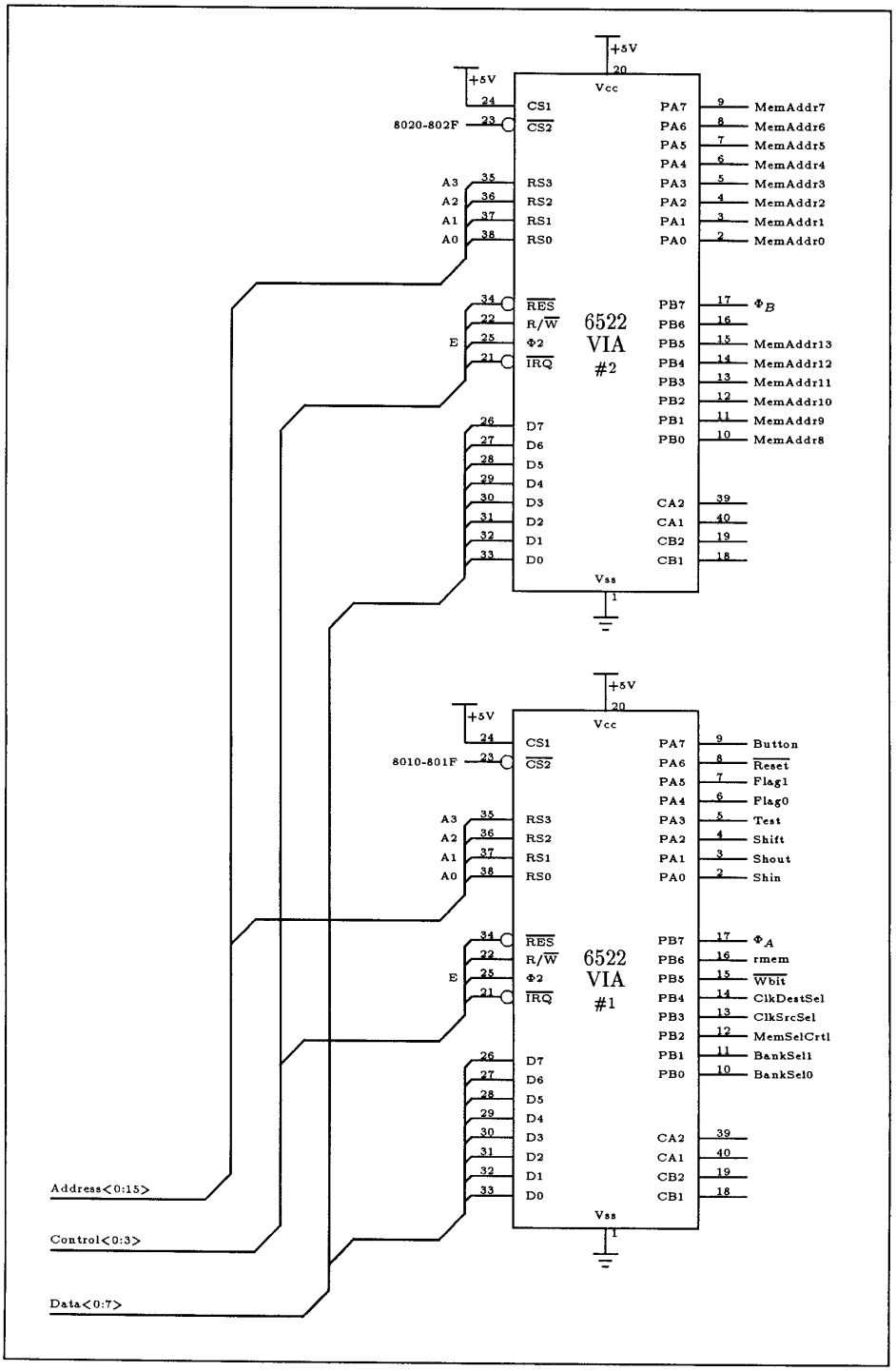



Figure 5: SECD Control Signals

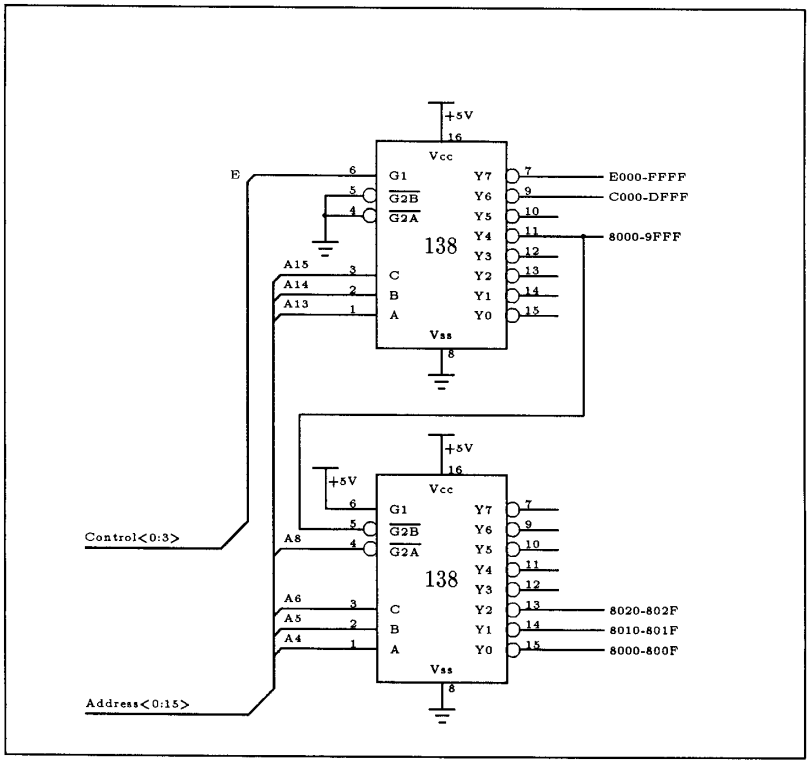



Figure 3: Address Decoding

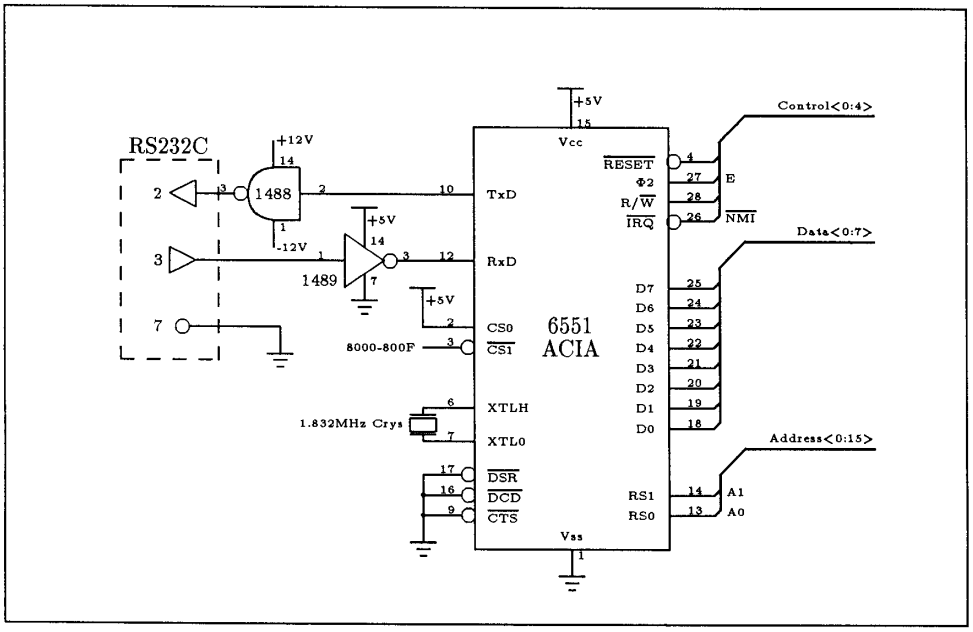



Figure 2: Communications

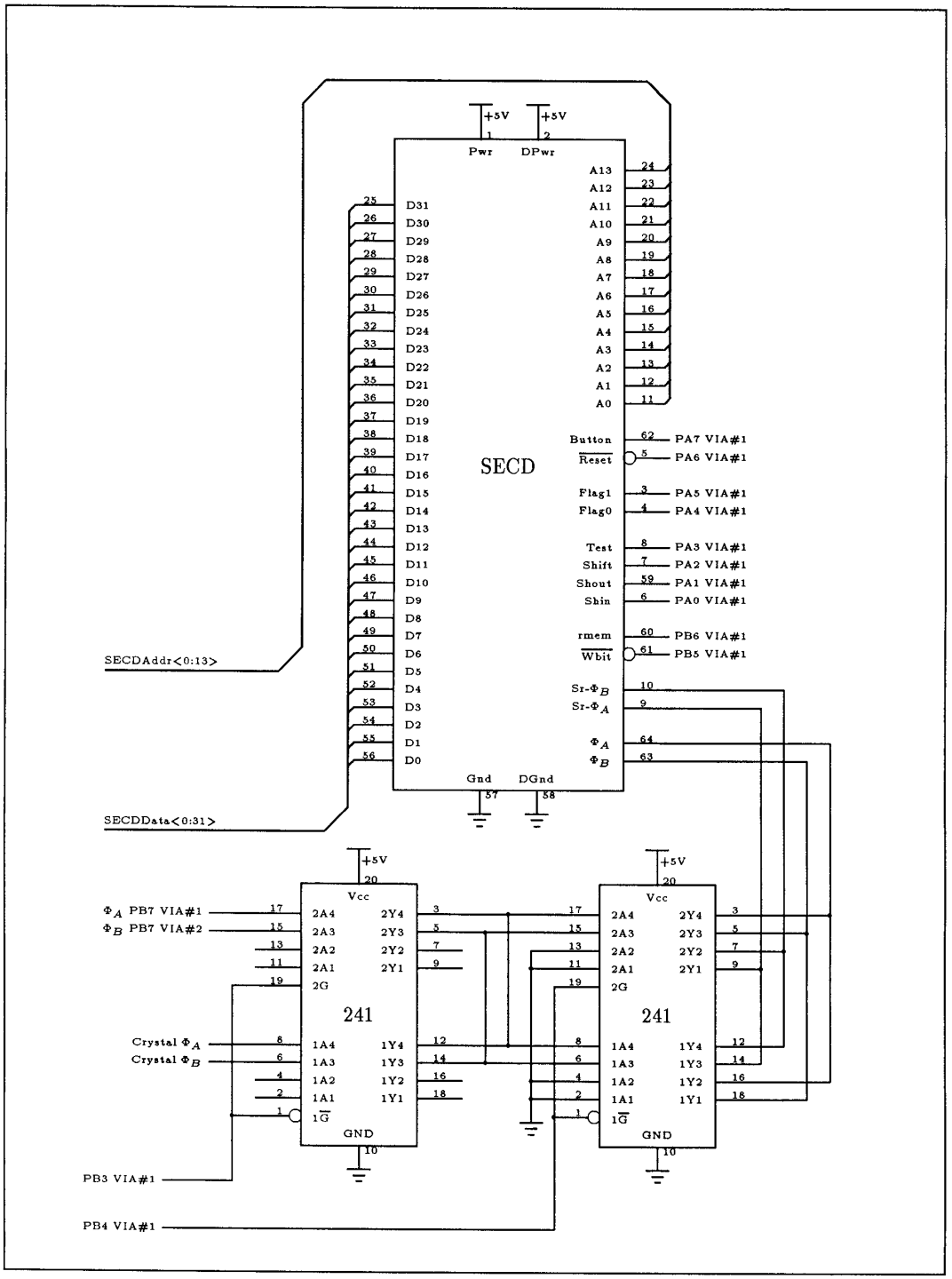



Figure 8: SECD

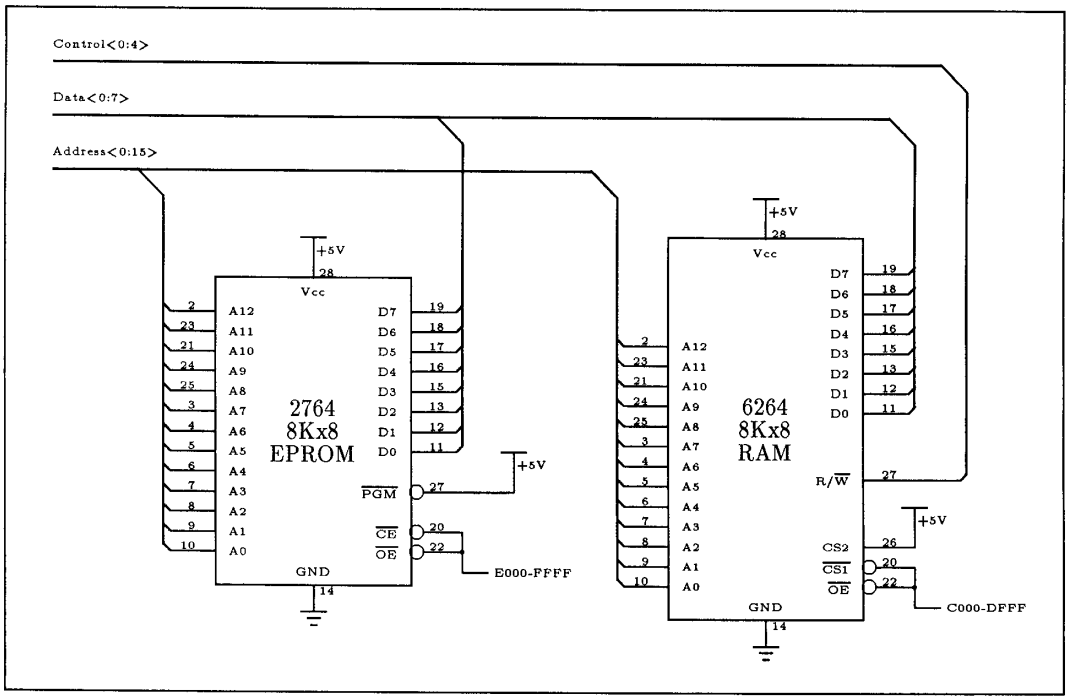



Figure 4: Program Memory

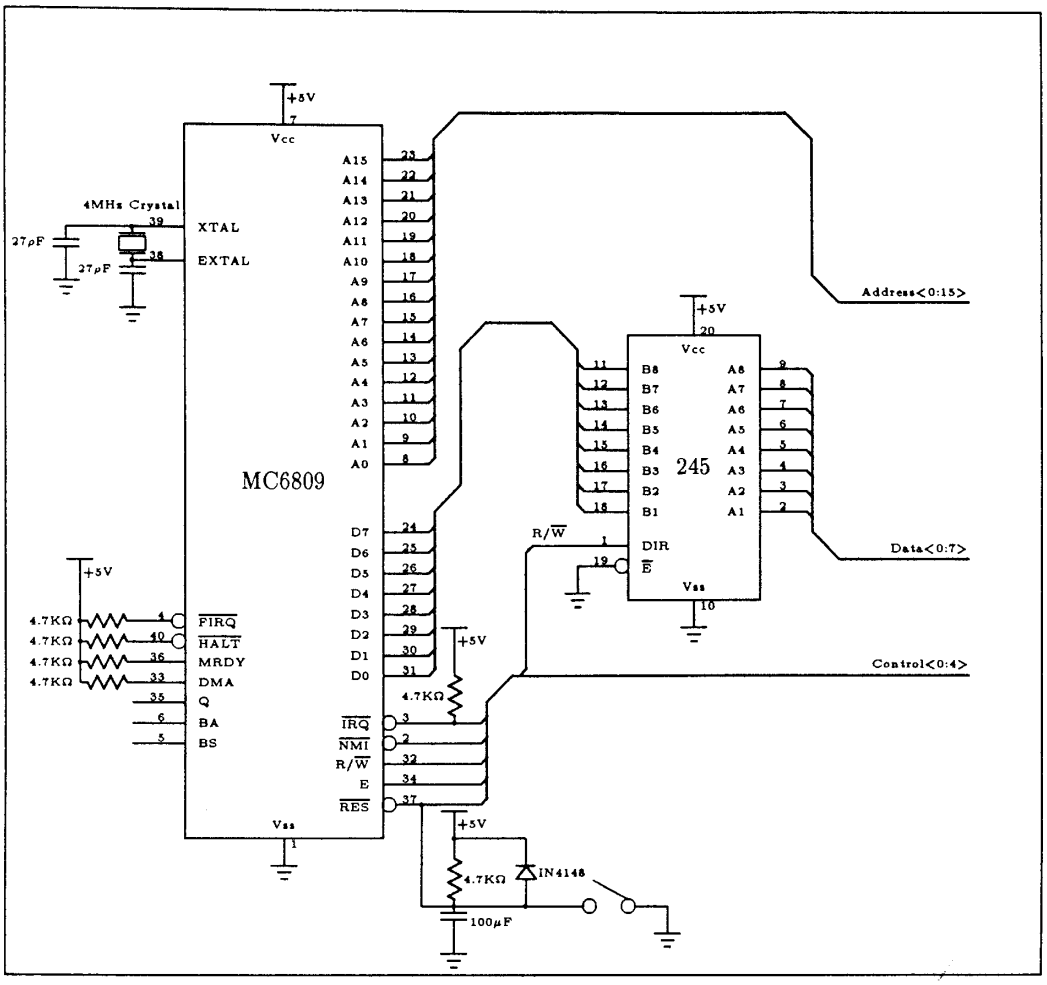



Figure 1: 6809