400-to-800MHz Low-Noise Amplifier for Radio Astronomy

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master thesis

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400-to-800 MHz Low-Noise Amplifier for Radio Astronomy

by

Thisara Navindika Kulatunga

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES IN PARTIAL
FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF
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Abstract

The Dominion Radio Astrophysical Observatory is interested in investigating the possibility of replacing 408 MHz narrow-band feed antennas with wide-band antennas. Such change would require low-noise amplifiers (LNAs), which would operate over a wider frequency band. This thesis explores the feasibility of using GaAs p-HEMT transistors to implement a wide-band low-noise amplifier for the 400 MHz to 800 MHz frequencies for use in a wide-band antenna array.

In order to demonstrate the feasibility, a three-stage cascaded low-noise amplifier was developed and experimentally verified. The GaAs p-HEMT LNA achieves a sub-0.36dB noise figure in the 390 MHz to 810 MHz frequency region and a beam-equivalent receiver noise temperature of 17.8 K to 28.3 K within the 390 MHz-to-810 MHz frequency region. The LNA demonstrates $S_{21} > 41.1$ dB within the 400 MHz-to-800 MHz frequency region while consuming 406 mW of power. This LNA has $P_{1dB} > -32.9$ dBm and $IIP3 > -22.5$ dBm within the frequency region.
Acknowledgements

I would like to offer my sincere gratitude to my supervisor, Dr. Leonid Belostotski for his guidance throughout my masters studies during the past two years. I appreciate his knowledge in RF circuits and I was able to develop insight into the RF circuit field through his teaching. I would also like to thank my co-supervisor, Dr. Jim Haslett, for his support of my research work.

I would like to thank the Dominion Radio Astrophysical Observatory, Herzberg Institute of Astrophysics, National Research Council of Canada for providing necessary data required for the thesis work. I would also like to thank the University of Calgary for providing financial support and facilities required for my work.

I would like to thank CMC Microsystems for providing the necessary design and simulation software tools required for my thesis work.

I would also like to offer my gratitude to the Micro/Nano Technologies (MiNT) Laboratory for providing the facilities and measurement equipment required for building and testing of the design proposed in the thesis.

I owe a great debt of gratitude to everybody in the Micro/Nano Technologies (MiNT) research group for providing advice, guidance for my work and teaching me how to use software tools and measurement equipment.

Finally, I would like to thank my parents, wife, extended family and friends for their support and encouragement throughout my life.
Dedicated to my beloved parents, wife and brothers.

Thank you for your encouragements.
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<tr>
<td>ADS</td>
<td>Advanced Design Systems</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>HEMT</td>
<td>High-Electron-Mobility Transistor</td>
</tr>
<tr>
<td>LNA</td>
<td>Low-Noise Amplifier</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal-Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>MODFET</td>
<td>Modulation-Doped Field-Effect Transistor</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium Arsenide</td>
</tr>
<tr>
<td>p-HEMT</td>
<td>Pseudomorphic High-Electron-Mobility Transistor</td>
</tr>
<tr>
<td>InP</td>
<td>Indium Phosphide</td>
</tr>
<tr>
<td>IP3</td>
<td>Third order intercept point</td>
</tr>
<tr>
<td>IIP3</td>
<td>Input referred IP3</td>
</tr>
<tr>
<td>OIP3dB</td>
<td>Output referred IP3</td>
</tr>
<tr>
<td>P1dB</td>
<td>1 dB compression point</td>
</tr>
<tr>
<td>IP1dB</td>
<td>Input referred P1dB</td>
</tr>
<tr>
<td>OP1dB</td>
<td>Output referred P1dB</td>
</tr>
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<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field-Effect Transistor</td>
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<td>PMOS</td>
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<tr>
<td>DRAO</td>
<td>Dominion Radio Astrophysical Observatory</td>
</tr>
<tr>
<td>NRC</td>
<td>National Research Council of Canada</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>RFIC</td>
<td>Radio Frequency Integrated Circuit</td>
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<td>VNA</td>
<td>Vector Network Analyzer</td>
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Chapter 1

Introduction

Since the dawn of history, the innate quality of curiosity possessed by humans has driven them to observe and study the surrounding environment. This curiosity also focused them towards the objects visible in the sky as well. At first, they were only capable of performing these observations within the visible light portion of the electromagnetic spectrum. These observations were performed using the naked eye. Later, with the development of science and technology, astronomers were able to perform visual observations with the help of telescopes with lenses. These observations were able to provide necessary evidence to disprove the prevailing concept of earth centered universe at the time, providing the foundation for gravitational theories of Newton, and providing proof for Kepler’s laws of planetary motion.

Later in the 19th century, with the discovery of electricity and establishing the theoretical foundation for electromagnetic waves through Maxwell’s equations, new windows to observe the universe were opened. With the discovery of other portions of the electromagnetic spectrum such as radio waves, Infra-red waves, Ultra-violet waves, X-rays, and Gamma rays, acquiring additional information about space was possible for the astronomers. Especially the observations in radio and optical spectra were helpful in formulating the prevailing cosmological model for the creation and expansion of the universe, the Big Bang theory.

The radio telescope is the instrument used for observations of the universe in the radio-wave portion of the electromagnetic spectrum. The developments of electromagnetism and electronics in the 20th century have led to many improvements of the capabilities of the radio telescopes allowing for faster surveying speed, lower noise in measurements, wide-band frequency spectrum observations, and beam steering through antenna arrays.
1.1 The Dominion Radio Astrophysical Observatory and the Synthesis Radio Telescope

The Dominion Radio Astrophysical Observatory (DRAO) hosts multiple antennas, which perform observations in the radio-wave spectrum. DRAO is located near Penticton, British Columbia, Canada. The DRAO is operated by the Herzberg Institute of Astrophysics of the National Research Council of Canada (NRC). The Synthesis Radio Telescope is among the antennas hosted by DRAO and performs radio astronomy observations at 408 MHz and 1420 MHz. Currently, the Synthesis Radio Telescope consists of 7, 8.5 m parametric antennas, which are computer controlled. This telescope uses an aperture synthesis technique to simulate an antenna with large aperture to create radio images. This requires moving the antennas along a railway track.

The primary use of the Synthesis radio telescope [7] is to perform galactic (in the Milky Way galaxy) interstellar medium (ISM) studies [8], although this radio telescope has been used for solar system and extra-galactic studies as well. Interstellar medium (ISM) studies is a branch of astronomy, which is devoted to studying the gas and plasma that lies between astronomical objects in space. Since the ISM contains the physical and chemical traces of past and current astronomical objects and the source of future astronomical objects, the objective of studying ISM is to understand the evolution process of galaxies.

The Synthesis telescope performs ISM studies by performing measurements in two narrow frequency bands near 408 MHz and 1420 MHz. The telescope is capable of performing measurements in both right-hand (R) and left-hand (L) circular polarization at 1420 MHz, and in R-circular polarization at 408 MHz.

The data extracted by the Synthesis telescope at frequency 1420 MHz have a great significance in galactic astronomy because it is the frequency of the spin-flip spectral line of atomic hydrogen gas (H1 line). By extracting the Doppler shifts caused by relative motion between Earth and selected points in the galactic-ISM, velocity of those points and the
distance to those points in the galaxy can be determined [9–11]. Furthermore, atomic hydrogen concentration levels can be mapped using the 1420 MHz frequency measurements.

In addition to spin-flip spectral line observations at 1420 MHz, the Synthesis telescope is also used to extract thermal continuum emission spectra [10, 12] generated by ionized gas in ISM near 408 MHz and 1420 MHz frequencies. The synchrotron emission spectrum is also observed using the Synthesis telescope [12, 13] near 408 MHz and 1420 MHz frequencies. The synchrotron emission spectrum is generated by charged particles moving in curves through magnetic fields at velocities near the speed of light. Hence, studying magnetic fields and ionized gas levels in the ISM is possible using the measurements from the frequency bands near 408 MHz and 1420 MHz.

1.2 The Purpose of the Thesis

The DRAO is currently interested in replacing the existing narrow-band feed antennas of the Synthesis radio telescope with wide-band antenna arrays. This modification would increase the frequency coverage while allowing for forming multiple beams, which increases the surveying speed. The increase of bandwidth can allow for observations of 21 cm (1420 MHz) spin-flip spectral lines of atomic hydrogen at cosmological red-shifts $z = 0.8$ to 2.5 such as in a telescope described in [14, 15]. Furthermore, it would allow astronomers to perform observations of thermal continuum emission and synchrotron emission spectra in a larger bandwidth. These observations would help deepen the understanding of the evolution of the universe by allowing the scientists to probe the expansion history of the universe. This thesis contributes to this task by proposing a wide-band LNA for the antenna arrays.

The specifications of some alternative LNA designs available in the literature, which partially cover the frequency band of interest are shown in Table 1.1. It can be observed that CMOS-technology-based designs consume less power than GaAs technologies, which is an advantage. But cost savings cannot be realized by lower power consumption alone.
Table 1.1: Specifications of Published LNA Designs.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[17]</th>
<th>[18]</th>
<th>[19]</th>
<th>[20]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.2 mm GaAs process of OMMIC, Philips.</td>
<td>GaAs off the shelf</td>
<td>CMOS 0.18µm</td>
<td>CMOS 90 nm</td>
</tr>
<tr>
<td>Frequency</td>
<td>0.6-1.6 GHz</td>
<td>0.7-1.4 GHz</td>
<td>0.7-1.4 GHz</td>
<td>0.7-1.4 GHz</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>0.5 dB max.</td>
<td>0.34 dB max.</td>
<td>0.56 dB max.</td>
<td>0.35 dB max.</td>
</tr>
<tr>
<td>Input $S_{11}$</td>
<td>-12 dB max.</td>
<td>-5 dB max.</td>
<td>-11 dB max.</td>
<td>-15 dB max.</td>
</tr>
<tr>
<td>Power Gain</td>
<td>21 dB min.</td>
<td>28 dB min.</td>
<td>17 dB min.</td>
<td>16 dB min.</td>
</tr>
<tr>
<td>P1dB</td>
<td>-15 dBm min.$^a$</td>
<td>-17 dBm min.$^b$</td>
<td>-10 dBm min.</td>
<td>-25 dBm$^c$</td>
</tr>
<tr>
<td>DC Power</td>
<td>852 mW</td>
<td>500 mW</td>
<td>50 mW</td>
<td>45 mW</td>
</tr>
</tbody>
</table>

$^a$Estimated based on OIP3.
$^b$Estimated based on IIP3.
$^c$Measured at 1 GHz.

if large numbers of LNAs are not used in the end of the design process as in the case of the Square Kilometer Array (SKA) radio telescope project [16]. All designs shown in the Table 1.1 do not require cryogenic cooling to realize the low-noise figures obtained. Nevertheless, none of those designs cover the frequency band of interest completely which justifies the work in this thesis. Furthermore, the published designs shown in Table 1.1 are not specifically optimized to reduce the noise when the LNAs are installed in an antenna array. Hence, the main purpose of the research described in this thesis to describe an LNA optimized for low noise operation when the LNAs are installed in an antenna array.

The LNA design proposed in this thesis will enable capturing of radio signals within the 400 MHz-to-800 MHz frequency band received by the antenna array. The noise of the LNA is to be the lowest possible while operating at ambient temperatures. Based on the designs shown in Table 1.1, it is reasonable to expect a noise figure close to 0.34 dB. The gain in the range of 30-to-50 dB is acceptable to reduce noise contributed by the following stages. A DC power consumption of 500 mW is a reasonable expectation for an LNA with transistors of GaAs technology. A summary of target specifications is shown in Table 1.2.

In addition to the Synthesis radio telescope, DRAO hosts the Canadian Hydrogen Intensity Mapping Experiment (CHIME) radio interferometer [14], which could also potentially
### Table 1.2: Target LNA Specification.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>0.4-0.8 GHz</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>~0.34 dB</td>
</tr>
<tr>
<td>Power Gain</td>
<td>30-50 dB</td>
</tr>
<tr>
<td>DC Power</td>
<td>500 mW</td>
</tr>
</tbody>
</table>

benefit from the design proposed in this thesis work. The CHIME radio interferometer operates in the 400 MHz-to-800 MHz frequency band as well.

### 1.3 Thesis Layout

The rest of the thesis is divided into 4 chapters.

In Chapter 2, GaAs-transistor noise-modeling techniques are reviewed and small-signal transistor parameters and noise parameters are derived for the transistors. Then, various LNA topologies are reviewed and their advantages and drawbacks are discussed. Techniques available to extend the bandwidth of LNA topologies are also discussed. Furthermore, noise cancellation techniques are also reviewed. The rest of the chapter is devoted to evaluation of available topologies to identify the potential candidate topology for the first stage of the LNA design considered in this thesis.

Chapter 3 presents the complete design of the three-stage LNA circuit. This chapter begins by evaluating different GaAs transistors available for use in the candidate LNA topology and comparing their simulation results. Then, this chapter proceeds to evaluation of bandwidth-extension techniques with simulations and comparison of the results. Furthermore, topologies available for the final (buffer) stage are discussed and evaluated through simulations. Finally, the complete LNA design is evaluated by considering simulation results, which consist of scattering parameters, voltage gain, noise parameters, stability metrics, and linearity metrics.

Chapter 4 presents the measurement results of the proposed LNA circuit from Chapter 3. Noise parameters, scattering parameters, linearity metrics, and stability metrics are
considered in this chapter.

Chapter 5 summarizes the thesis.
2.1 Introduction

The main objective of Chapter 2 is to identify potential candidates for the first stage of the low-noise-amplifier design proposed in this thesis. The purpose of Sections 2.2-2.6 is to lay down background information required for understanding LNA architectures discussed in Section 2.7. This chapter starts with a review of noisy two-port networks in Section 2.2. The subsequent Sections 2.3 and 2.4 are about basic information regarding MESFETs (Metal-Semiconductor Field Effect Transistors) and HEMTs (High-Electron-Mobility Transistors). The Statz model, which can be used to model the behavior of GaAs HEMTs, is discussed in Section 2.5. A widely used noise model for GaAs HEMTs is described in Section 2.6. Section 2.7 introduces various low-noise amplifier topologies. This section provides the basic information for selecting a proper topology for the first stage of the proposed design in this thesis. The discussion section summarizes the findings of this chapter.

2.2 Noisy Two-Port Networks

The noise factor is an important metric for determining the performance of an LNA. The noise factor is defined as

\[
F = \frac{SNR_{in}}{SNR_{out}} = \frac{P_{in}}{P_{out}} \frac{N_{in}}{N_{out}} = \frac{P_{in}}{N_{in}} \frac{G_{A}P_{in}}{G_{A}(N_{in}+N_{N})} = 1 + \frac{T_{N}}{T_{0}},
\]

(2.1)

where \(SNR_{out}\) and \(SNR_{in}\) are the available signal-to-noise ratios at the output and input of the device, \(P_{in}\) and \(P_{out}\) are the input and output signal powers, \(N_{in}\) and \(N_{out}\) are the input and output noise powers, \(N_{N}\) is the noise power component added by the circuit, \(G_{A}\) is the available power gain of the circuit, \(T_{N}\) is the equivalent noise temperature of
the component, and \( T_0 \) is the reference temperature, typically 290K. With (2.1), the noise figure is expressed as

\[
NF = 10\log_{10}(F). \tag{2.2}
\]

It is well known that the electrical parameters of a two-port network can be represented using Z, Y, S, or ABCD parameters [21]. In the same manner, it is possible to represent noise characteristics of a two-port network using noise-correlation matrices as outlined in [22, 23] from which the concept of noise parameters follows. For example, the noise-correlation matrix for a chain two-port representation, i.e. ABCD representation, is given as

\[
C_{ABCD} = \frac{1}{2\Delta f} \begin{vmatrix} v_n v_n^* & v_n i_n^* \\ v_n^* i_n & i_n^* i_n \end{vmatrix} \equiv 2kT_0 \begin{vmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{vmatrix}, \tag{2.3}
\]

where \( i_n \) is a current noise source and \( v_n \) is a voltage noise source as shown in Figure 2.1, \( \Delta f \) is the noise bandwidth, \( k \) is Boltzmann’s constant, and \( C_{i,j} \) identify matrix elements. This representation is used to define noise parameters [22, 23], which are: the minimum noise factor \( (F_{\text{min}}) \), the equivalent noise resistance \( (R_n) \), and the optimum admittance for minimum noise \( (Y_{\text{opt}}) \).

The equations for ABCD-parameter noise representation based on Figure 2.1 are

\[
V_1 - v_n = AV_2 + BI_2 \tag{2.4}
\]

\[
I_1 - i_n = CV_2 + DI_2, \tag{2.5}
\]
where $A$, $B$, $C$, and $D$ are the ABCD parameters, $V_1$ and $V_2$ are the voltages between the two terminals of Port 1 and 2 of the noisy two-port network, $I_1$ is the current entering Port 1, and $I_2$ is the current exiting Port 2 of the noisy two-port network. Obtaining $v_n$ and $i_n$ using above equations is not possible since it is necessary to set both $V_2 = 0$ and $I_2 = 0$ at the same time. Instead of trying to directly determine the chain noise-correlation matrix, an alternative way to expressing the network noise properties is based on $Z$ parameters, which results in a system of equations such as

\begin{align}
V_1 - v_n &= Z_{11} (I_1 - i_n) + Z_{12} I_2 \tag{2.6} \\
V_2 &= Z_{21} (I_1 - i_n) + Z_{22} I_2, \tag{2.7}
\end{align}

where $V_1$, $V_2$, $i_n$, $v_n$, $I_1$ have the same meaning as in the case of equations (2.4) and (2.5) while $I_2$ would be the current entering Port 2 of the noisy two-port network. By setting $I_1 = 0$ and $I_2 = 0$ at the same time, it is possible to calculate noise sources of chain representation $v_n$ and $i_n$ as given by

\begin{align}
v_n &= v_{n1} - \frac{Z_{11}}{Z_{21}} v_{n2} \tag{2.8} \\
i_n &= -\frac{v_{n2}}{Z_{21}} \tag{2.9}
\end{align}

where

\begin{align}
v_{n1} &= V_1\|_{I_1,I_2=0} \tag{2.10} \\
v_{n2} &= V_2\|_{I_1,I_2=0}. \tag{2.11}
\end{align}

When a system consists of more than one cascaded two-port network, the relationship between the system $C_{ABCD}$ matrix and the individual $C_{ABCD}$ matrices of each two-port network would be useful in calculations. The $C_{ABCD}$ matrix of a cascade of two two-port networks,
i.e. $C_{ABCD,\text{tot}}$, can be calculated with the knowledge of the ABCD parameters of the first network and the $C_{ABCD}$ matrices of both networks as

$$
C_{ABCD,\text{tot}} = C_{ABCD,1} + ABCD_1 \times C_{ABCD,2} \times ABCD_1^+,
$$

where $^+$ denotes Hermitian conjugation (Transpose of complex conjugate), $ABCD_1$ denotes ABCD parameters of the first two-port network, $C_{ABCD,1}$ and $C_{ABCD,2}$ denote $C_{ABCD}$ matrices of the first and second two-port networks.

### 2.3 Metal-Semiconductor FETs (MESFETs)

MESFETs utilize a metal-semiconductor Schottky junction. MESFETs can be used in high-frequency applications because the Schottky junction allows for fast operation of the device. Particularly manufactured MESFETs using group III-V compounds, such as GaAs or InP, provide higher-frequency operation due to their higher carrier mobilities and drift velocities compared to Si transistors [24]. Furthermore, GaAs devices can be operated at high temperatures similar to materials, such as Si, GaN, SiC, which are used in high-power applications [25–28]. MESFETs also exhibit low noise figures [29–33], which makes them an attractive choice for low-noise-amplifier applications.

Figure 2.2 depicts a simple diagram of a GaAs MESFET. The substrate (semi-insulating GaAs)
GaAs) has a high resistivity ($\sim 10^8 \Omega \text{cm}$) because its Fermi energy level is located near the center of the GaAs bandgap. A thin layer of lightly doped n-type GaAs is grown on top of this substrate using an epitaxial growth process to form the channel of the FET. Defining metal contacts for source and drain ohmic contacts and for the Schottky barrier gate in the metal layer are performed using photolithographic processes. Alternatively ion implantation can be used to create an n-type layer and contacts.

2.4 High-Electron-Mobility Transistors (HEMTs)

High-electron-mobility transistors (HEMTs), or alternatively known as modulation-doped field-effect transistors (MODFETs), are another suitable device for low-noise operation [34–37]. HEMTs are built with a junction between two different materials with different bandgaps, i.e. a heterojunction, as the channel instead of a doped region. HEMTs are mostly manufactured using a combination of elements from groups III and V of the periodic table. Most of the HEMTs are primarily n-channel devices although p-channel HEMTs [38, 39] have also been manufactured successfully. Nevertheless p-channel devices are not used in high-frequency circuits, because their carrier (hole) mobility is lower compared to the electron mobility in n-channel devices and source/drain resistances are high compared to the n-channel devices.

HEMTs are developed as a high-performance solution when the device is scaled down to smaller dimensions. When MESFETs are scaled down, channel length approaches the depletion-layer width causing short-channel effects. Although these effects can be removed by increased channel doping levels, high concentration of dopant atoms results in lower electron mobility due to impurity scattering. This issue was avoided in HEMTs by physically separating donor atoms and mobile charges using selectively doped heterostructure.

A cross section of a GaAs/AlGaAs HEMT is shown in Figure 2.3. This device has a semi-insulating GaAs substrate as the foundation, an undoped GaAs layer, a modulation-doped n-type $Al_xGa_{1-x}As$ layer and a heavily doped n-type GaAs layer in the given se-
Figure 2.3: AlGaAs/GaAs HEMT structure.

quence from bottom to top. The $x$ value of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ compound at the n-type AlGaAs-undoped GaAs interface is 0.23 in which the lattice constants of both materials are matched and a quality heterojunction is formed. The channel is formed in the undoped GaAs layer using the electrons donated by the AlGaAs layer. A thin layer of undoped AlGaAs is placed on top of the junction in order to reduce the scattering between free electrons and donor atoms in AlGaAs. The heavily doped n-type GaAs layer provides low-resistance ohmic contacts to source and drain terminals. The gate terminal is directly in contact with the n-type AlGaAs modulation-doped layer by removing the heavily doped n-type GaAs layer to ensure a Schottky contact between the gate and the AlGaAs layer.

GaAs and AlGaAs layers have a very slight mismatch at the heterojunction causing deep level traps and reducing the performance. By using a sufficiently thin layer of one material, this issue can be eliminated because the lattice constant of the thin layer adjusts to the lattice constant of the other material and improves the performance. This type of HEMT is called a pseudomorphic HEMT (p-HEMT).

The capability to have large electron density within a very thin layer while avoiding ionized impurity scattering is an advantage in HEMTs. Additionally, HEMTs have higher electron mobility and higher drift velocity as well.

GaAs p-HEMT devices are used in the design proposed in the thesis due to the availability of those devices as off-the-shelf components in the open market. Additionally, avail-
Figure 2.4: Simplified small-signal Statz GaAs FET model without gate, source, and drain terminal resistances.

ability of transistor models provided by the manufacturer is another positive attribute of this choice.

2.5 Statz Model for GaAs FETs

The Statz small-signal model [40] is widely used for modeling the behavior of GaAs FETs in simulators such as Keysight’s Advanced Design System (ADS). The small-signal model is shown in Figure 2.4.

The necessity to have a different model for GaAs devices than for Si FETs is because the velocity of electrons traveling in GaAs devices approaches its saturation velocity value at a lower electric field as opposed to Si devices [40]. Hence, saturation of the drain current
with the increasing drain-to-source voltage is caused by the velocity saturation of electrons in GaAs devices as opposed to the channel-pinchoff phenomenon that causes the saturation of the drain current with the increase of the drain-source voltage in Si FETs. Considering \( V_{to} \) as the threshold voltage of transistor, \( \alpha \) as a parameter, which determines the voltage of drain current saturation, B as doping tail extending parameter, \( \lambda \) as a parameter related to drain-source conductance, \( \beta \) as a parameter related to transconductance [40], the drain current \( I_{ds} \) is expressed as

\[
I_{ds} = \frac{\beta V_{ov}^2}{1 + BV_{ov}} (1 + \lambda V_{ds}) X
\]

where

\[
V_{ov} = V_{gs} - V_{to},
\]

and

\[
X = \begin{cases} 
0 & \text{for } V_{ds} < 0 \\
1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3 & \text{for } 0 < V_{ds} < \frac{3}{\alpha} \\
1 & \text{for } V_{ds} \geq \frac{3}{\alpha}.
\end{cases}
\]

The gate current \( I_{gs} \) can be given as

\[
I_{gs} = \begin{cases} 
I_{ds} \left[ e^{\left(\frac{V_{gs}}{N_e V_{to}}\right)} - 1 \right] & V_{gs} > -10N_eV_{to} \\
I_{ds} \left[ e^{-10} - 1 \right] + g_{gs} (V_{gs} - 10N_eV_{to}) & -V_{br} + 50V_{to} < V_{gs} \leq -10N_e V_{to} \\
-I_{ds} e^{\left(-\frac{V_{br}+V_{gs}}{N_e V_{to}}\right)} + I_{ds} \left[ e^{-10} - 1 \right] + g_{gs} (V_{gs} - 10N_eV_{to}) & V_{gs} \leq -V_{br} + 50V_{to}
\end{cases}
\]

where \( N_e \) is the gate junction emission coefficient, \( V_{br} \) is gate junction reverse bias breakdown voltage and

\[
g_{gs} = I_{ds} \frac{e^{-10}}{N_e V_{to}}.
\]
2.6 Noise Model of the HEMT

The characterization of noise properties of HEMTs in this work would be different from physics-based approaches such as in [41] where the underlying principles of physics are investigated in order to derive equations for noise in the devices under consideration. These approaches have the benefit of providing an insight into the noise generation mechanisms of the considered device and their relative contribution to the total noise power. The alternative approach is to use empirical equations based on experiments to predict the noise performance [1, 42–44]. This approach is very widely used for modeling noise performances although it does not give an insight into the underlying noise generating mechanisms. Applying the approach in [41] to the HEMTs is not possible directly because the noise generation mechanism of HEMTs cannot be physically modeled in the same way. Hence, the method proposed by Pospieszalski [1] is used in this work.

The equivalent noisy-HEMT small-signal model as proposed in [1] is given in Figure 2.5.

The Johnson-Nyquist expressions for mean-squared gate-noise voltage and mean-squared
The noise sources $i_n$ and $v_n$ in the ABCD matrix can be calculated using the equations in Section 2.2.

The equivalent noise resistance $R_n$ and the equivalent noise conductance $g_n$ [45] for the noisy two-port network shown in Figure 2.1 can be expressed as

$$R_n = \frac{|v_n|^2}{4kT_0\Delta f}$$

(2.20)

and

$$g_n = \frac{|i_n|^2}{4kT_0\Delta f},$$

(2.21)

where $\Delta f$ denotes the noise bandwidth and $T_0$ denotes the reference temperature (290 K).

Noise parameters [45] for the circuit in Figure 2.5 can be given as [1]

$$R_{opt} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{r_{gs} T_g}{g_{ds} T_d} + r_{gs}^2},$$

(2.22)

$$X_{opt} = \frac{1}{\omega C_{gs}},$$

(2.23)

$$T_{min} = 2\frac{f}{f_T} \sqrt{g_{ds} r_{gs} T_g T_d + \left(\frac{f}{f_T}\right)^2 \frac{r_{gs}^2 g_{ds}^2 T_d^2}{2} + 2 \left(\frac{f}{f_T}\right)^2 r_{gs} g_{ds} T_d},$$

(2.24)

and

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{ds} T_d}{T_0}.$$
\[ N = \frac{T_{\min}}{2T_0 \left( 1 + \frac{r_{gs}}{R_{opt}} \right)}, \quad (2.26) \]

\[ R_n = \frac{T_{e}}{T_0} r_{gs} + \frac{T_d g_{ds}}{T_0 g_m} \left( 1 + \omega^2 C_{gs}^2 r_{gs}^2 \right), \quad (2.27) \]

where the unity-current-gain frequency \( f_T \) is given by

\[ f_T = \frac{g_m}{2\pi C_{gs}}. \quad (2.28) \]

The frequency is denoted by \( f \) and angular frequency \( \omega \) is related to \( f \) by

\[ \omega = 2\pi f. \quad (2.29) \]

Correlation coefficient \( \rho \) between \( v_n \) and \( i_n \) is defined as

\[ \rho = \frac{v_n^* i_n}{\sqrt{|v_n|^2 \cdot |i_n|^2}}. \quad (2.30) \]

### 2.7 LNA Architectures

#### 2.7.1 Common-Source Amplifier

This is one of the basic, but, at the same time, one of the lowest-noise amplifier configurations available to use as a foundation for an LNA design. A simplified schematic of this amplifier is shown in Figure 2.6. The element shown as \( Z_L \) could be a resistor or an inductor or some other load network.

#### 2.7.1.1 Design Equations

The expressions derived in this section were based on the simplified equivalent small-signal circuit shown in Figure 2.7. The input impedance of this circuit is
Figure 2.6: Common-source amplifier. Source voltage and resistance denoted by \( v_s, R_s \) respectively.

Figure 2.7: Common-source small-signal model. \( i_s \) is the noise current of \( R_s \).

\[ Z_{in} = \frac{V_{in}}{I_{in}} \approx \frac{1}{j\omega C_{gs}}, \]  

(2.31)

assuming \( r_{gs} \ll \left| \frac{1}{j\omega C_{gs}} \right| \).

The equation B.4 in Appendix B for a voltage gain is transformed to

\[ Gain = \frac{V_{out}}{V_{in}} \approx -g_m Z_L, \]  

(2.32)

assuming \( g_{ds} \ll \left| \frac{1}{Z_L} \right| \).
The noise factor equation for the common-source amplifier is derived in Appendix B and is rewritten here for convenience as

\[
F = 1 + \frac{T_g r_{gs}}{T_0 R_s} + \frac{T_d g_{ds}}{g_m^2 R_s T_0} \left[ 1 + \omega^2 C_{gs}^2 (R_s + r_{gs})^2 \right].
\]  

(2.33)

It can be observed that increasing the bias current reduces the noise figure because of its dependency on \(g_m\).

From (2.31), it can be seen that the input impedance is reactive and frequency-dependent for this amplifier. Furthermore real and imaginary components of optimal input impedance for this amplifier are given by (2.22) and (2.23), if \(Z_L\) doesn’t introduce noise into the circuit shown in Figure 2.7. Hence, achieving a reasonable balance between power match and noise match is not straightforward. Additionally, the opportunity to adjust \(Z_m\) is not available because \(C_{gs}\) does not change considerably by changing biasing conditions. Using a resistor as the load gives an advantageous frequency-independent voltage gain at frequencies at which parasitic capacitances have insignificant effect. However, the resistor adds noise and introduces a voltage drop across its terminals. Based on (2.24), \(F_{min}\) of the common-source amplifier can be expressed as

\[
F_{min} = 1 + \frac{T_{min}}{T_0} = 1 + \frac{2 \omega C_{gs}}{g_m T_0} \sqrt{g_{ds} r_{gs} T_k T_d} + \left( \frac{\omega C_{gs}}{g_m} \right)^2 r_{gs}^2 g_{ds}^2 T_d^2 + 2 \left( \frac{\omega C_{gs}}{g_m} \right)^2 r_{gs} g_{ds} T_d. \]  

(2.34)

It can be observed that by increasing \(g_m\) (by increasing bias current) both \(F_{min}\) and \(F\) can be reduced. Furthermore, the noise figure increases rapidly with the frequency according to (2.33) and (2.34).
2.7.2 Common-Gate Amplifier

A basic schematic and a simplified small-signal model of a common-gate amplifier are shown in Figures 2.8a and 2.8b.

The equations derived in Appendix C can be simplified assuming $r_{gs} \ll \left| \frac{1}{j\omega C_{gs}} \right|$ and
\[ g_{ds} \ll \left| \frac{1}{Z_L} \right| . \] The input impedance of this amplifier is given by

\[ Z_{in} \approx \frac{1}{g_m + sC_{gs}}. \] (2.35)

The overall voltage gain is given by

\[ \text{Gain} \approx g_mZ_L. \] (2.36)

When angular frequency \( \omega \ll \frac{g_m}{C_{gs}} = \omega_t \), \( Z_{in} \) can be approximated by \( \frac{1}{g_m} \) where \( \omega_t \) is unity-current-gain angular frequency. Hence since \( g_m \) is a function of biasing current, the input impedance of this amplifier can be adjusted by changing biasing conditions.

Based on the circuit shown in Figure 2.8b, the noise factor can be given as

\[
F = 1 + \frac{T_g r_{gs} \left( g_m^2 + \omega^2 C_{gs}^2 g_{ds}^2 R_s^2 \right)}{T_0 R_s \left[ (g_m + g_{ds})^2 + \omega^2 C_{gs}^2 g_{ds}^2 r_{gs}^2 \right]} + \frac{T_d g_{ds}}{\left[ (g_m + g_{ds})^2 + \omega^2 C_{gs}^2 g_{ds}^2 r_{gs}^2 \right]} R_s T_0 \left[ 1 + \omega^2 C_{gs}^2 (r_{gs} + R_s)^2 \right]. \] (2.37)

A simplified noise-factor equation, where \( g_{ds} \) is sufficiently small, i.e \( g_m \gg g_{ds} \), and \( g_m^2 \gg \omega^2 C_{gs}^2 g_{ds}^2 R_s^2 \) is given as

\[
F = 1 + \frac{T_g r_{gs}}{T_0 R_s} + \frac{T_d g_{ds}}{g_m^2 R_s T_0} \left[ 1 + \omega^2 C_{gs}^2 (r_{gs} + R_s)^2 \right]. \] (2.38)

According to (2.38), the noise factor is a function of \( g_m \). The equation predicts a lower noise factor (figure) for a higher \( g_m \). However, the requirement for low noise factor works against achieving power match since, as is shown in (2.35), the input impedance also depends on \( g_m \). By comparing (2.33) and (2.38), it can be observed that the noise factors of the common-source and common-gate amplifiers are equal under the same biasing conditions, with the same source resistance, signal frequency, and under the same temperature conditions.
Table 2.1: Simulation results for the selected transistors.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Bias Voltage (V)</th>
<th>Noise Figure (dB)</th>
<th>$S_{21}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATF-33143 [46]</td>
<td>0.90</td>
<td>0.68-0.70</td>
<td>2.24-2.29</td>
</tr>
<tr>
<td>ATF-34143 [47]</td>
<td>0.86</td>
<td>1.32-1.35</td>
<td>1.83-1.88</td>
</tr>
<tr>
<td>ATF-35143 [48]</td>
<td>0.76</td>
<td>1.10-1.11</td>
<td>2.26-2.29</td>
</tr>
<tr>
<td>ATF-38143 [49]</td>
<td>0.69</td>
<td>1.45-1.47</td>
<td>2.22-2.27</td>
</tr>
</tbody>
</table>

Figure 2.9: Circuit used for simulation.

conditions.

Since model parameters $T_g$, $T_d$, and $r_{gs}$ are unknown for candidate transistors, which were preselected for this work based on their manufacturer specifications, calculated values are not provided in this section. Instead simulated noise figure values using ADS for the selected transistors are given in Table 2.1. Those values were obtained for circuits biased such that $|S_{11}| < -10$ dB within a 400 MHz-to-800 MHz frequency range. The circuit used for the simulation is shown in Figure 2.9.

As can be seen in Table 2.1, the noise figure is not sufficiently low to meet requirements of this project. In addition, the gain is also not very high, which requires the following stage to be very low noise.

2.7.3 Inductive-Source-Degenerated Amplifier

In Section 2.7.2, it was shown that the noise figures for both common-source and common-gate amplifiers are nearly equal for same circuit elements and biasing conditions. But achieving input power match while maintaining the low noise figure with the original form
of those circuits would be difficult because parameters available to adjust the circuits are limited. In the case of a common-source amplifier, it has a capacitive input impedance, while a common-gate amplifier has a resistive input impedance, which only depends on $g_m$. Changing $g_m$ also changes the noise figure in the case of the common-gate amplifier. Thus both choices are not attractive for the design pursued in this thesis, which requires both low noise figure and input power match.

Inductive-source-degeneration [50, 51] is a technique, which generates an adjustable resistive input impedance by the choice of source and gate inductors and, if required, by employing an external capacitor between the gate and source terminals. The schematic of an inductive-source-degenerated amplifier is given in Figure 2.10. Detailed derivations of gain, input impedance, and noise factor are shown in Appendix D.

The minimum noise factor, $F_{\text{min}}$, which is derived for the selected design in Appendix E using noise parameters, is valid for a single-stage source-degenerate amplifier due to the assumption of no significant noise contribution from subsequent stages. The equation is

**Figure 2.10:** Schematic of an inductive-source-degenerated amplifier.
derived in Appendix E and repeated here in (2.39).

\[
F_{\text{min}} = 1 + \frac{2\omega C_{\text{gs}}}{T_0 (g_m + \omega^2 C_{\text{gs}} L g_{\text{ds}})} \left\{ \omega C_{\text{gs}} R_g T_d g_{\text{ds}} + \sqrt{T_d g_{\text{ds}} \left[ (T_g r_{\text{gs}} + T_0 R_g) (g_m + \omega^2 C_{\text{gs}} L g_{\text{ds}})^2 + \omega^2 C_{\text{gs}}^2 R_g^2 T_d g_{\text{ds}} \right]} \right\}. \tag{2.39}
\]

The Noise factor of the circuit can be obtained for a power matched condition based on (D.13) as

\[
F = 1 + \frac{T_g r_{\text{gs}}}{T_0 R_s} + \frac{R_g}{R_s} + \frac{T_d g_{\text{ds}} \left[ C_{\text{gs}}^2 (R_s + R_g + r_{\text{gs}})^2 + \omega^2 \right]}{T_0 R_s (g_m + g_{\text{ds}} L_s C_{\text{gs}} \omega^2)^2}. \tag{2.40}
\]

It can be observed that the resistance of the inductor has a significant effect on noise factor because of the term \(R_g R_s\) in (2.40). Hence, using high-quality-factor inductors for gate inductors is vital for achieving a low noise factor.

By assuming \(r_{\text{gs}} = 0, g_{\text{ds}} = 0\), an approximation can be made to the input impedance equation derived in Appendix D for the purpose of gaining analytical insight to obtain

\[
Z_{\text{in}} = \frac{g_m L_s}{C_{\text{gs}}} + j \omega (L_g + L_s) + \frac{1}{j \omega C_{\text{gs}}}. \tag{2.41}
\]

A typical LNA design with this topology would have parameter values chosen to ensure that the imaginary part of the input impedance vanishes at the required frequency, i.e. \(\omega^2 C_{\text{gs}} (L_g + L_s) = 1\), and that \(\frac{g_m L_s}{C_{\text{gs}}} = R_s\) to get an input power match. Nevertheless, this topology provides a narrow-band impedance match, which can be either problematic or desirable depending on the application.

The effect of parasitic capacitance \(C_{\text{gd}}\) is not considered in the calculations in Appendix D as the basic Pospieszalski model [1] does not contain a \(C_{\text{gd}}\) capacitor. This lack of \(C_{\text{gd}}\) in Pospieszalski’s model is due to the model focusing on modeling the noise behavior of the transistor as opposed to modeling the complete small-signal behavior of the transistor. Including \(C_{\text{gd}}\) in the calculations in Appendix D would increase the complexity of the
calculations. The existence of this capacitor between input and output also lowers the gain of an amplifier at high frequencies, via what is known as Miller effect, compared to a circuit based on Pospieszalski’s model [1]. The Miller effect is the increase of equivalent input capacitance caused by a capacitor (parasitic or external) connected between input and output terminals of any voltage amplifying circuit. The circuits shown in Figure 2.11a and Figure 2.11b are variations of standard source degeneration circuits to mitigate the Miller effect by lowering the load impedance seen by the $M_1$ transistor.

The topology in Figure 2.11a was demonstrated in a CMOS amplifier for a GPS receiver [52] achieving 3.5 dB noise figure while only consuming 30 mW. Additionally, various versions of cascode and folded-cascode source-degeneration topology can be found in the literature [19, 53–55]. For example, a modification to the cascode source-degeneration amplifier was introduced in [19] where a low-noise amplifier was designed in a 0.18 $\mu$m CMOS technology. This amplifier operates in a 0.7 GHz-to-1.4 GHz frequency range with 0.35 dB noise figure.
Furthermore, a similar topology shown in Figure 2.12a, in which an RF choke and a capacitor are introduced between the cascode connection of the drain and source terminals, was implemented using a 90 nm CMOS technology in [55], which achieved 0.2 dB noise figure for a 0.7 GHz-to-1.4 GHz frequency range. The RF choke provides a path for DC current while blocking AC currents and the capacitor provides an independent parameter to adjust the input power match profile. The work by Witvers et al. [56] also utilizes the same architecture as in the case in [54] for a GaAs LNA and obtained 0.15 dB noise figure in a 1 GHz-to-2 GHz frequency range.

In the circuit topology from [55], the existing parasitic $C_{gd}$, $g_{ds}$ and the added capacitor $C_L$ work with the source inductor $L_s$ to establish a second resonant structure as shown in Figure 2.12b, which can be used to widen the operating frequency band. The equivalent circuit given in Figure 2.12b takes $C_{gs}$ and $g_{ds}$ into consideration while neglecting $r_{gs}$. It is possible to design a wideband LNA by tuning circuit parameters to fix resonances of $RLC_1$ and $RLC_2$. 

**Figure 2.12:** Modified cascode LNA with input bandwidth enhancement.
to the upper frequency edge and $RLC_2$ to the lower frequency edge.

A variation of a standard source-degenerated amplifier for operation at a 91-cm wavelength was demonstrated in the work of Korolev et al. [57]. A commercially available GaAs p-HEMT ATF-33143 was used in this design and was able to achieve $12.8 \pm 1.5$ K noise temperature at ambient temperature operation (293 K) within a 315 MHz-to-340 MHz frequency band.

### 2.7.4 Resistive Shunt-Feedback Amplifier

A resistive shunt-feedback amplifier is a wide-band amplifier topology [58]. The main issue with the common-source amplifier is the high input impedance. The high input impedance property makes achieving power match over a broad frequency range a difficult task. The resistive shunt feedback lowers the input impedance and allows for a wide-band power match while inevitably compromising the noise figure.

The schematic of a single-transistor resistive shunt-feedback amplifier is shown in Figure 2.13. In this circuit, the impedance $Z_L$ is selected as an inductor in order to increase the drain current without the dc voltage drop across $Z_L$. 

![Figure 2.13: Classic resistive shunt-feedback amplifier.](image)
Figure 2.14: Resistive shunt-feedback amplifier small-signal model. $i_s$ and $i_f$ denote the noise generated by $R_s$ and $R_f$. $e_{gs}$ and $i_{ds}$ are standard noise generators in Pospieszalski’s model [1].

A simplified small-signal model for this amplifier is shown in Figure 2.14. A first-order approximation of the input impedance of the amplifier when connected to a load is given by

$$Z_{\text{in}} = \frac{(g_{ds}Z_L R_f + R_f + Z_L)}{[sC_{gs}(g_{ds}Z_L R_f + R_f + Z_L) + g_{ds}Z_L + g_m Z_L + 1]}.$$  \hspace{1cm} (2.42)

where $Z_L$ is a large-impedance load. The voltage gain of such an amplifier is

$$\text{Gain} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{Z_L (1 - g_m R_f)}{g_{ds}Z_L R_f + R_f + Z_L}.$$ \hspace{1cm} (2.43)

The noise-factor equation derived in Appendix F and repeated here is

$$F = 1 + \frac{R_f \left\{ (1 + g_m R_s)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{R_s (1 - g_m R_f)^2} + \frac{T_g r_{gs} \left\{ g_m^2 (R_s + R_f)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{T_0 R_s (1 - g_m R_f)^2} + \frac{T_d g_{ds} \left\{ (R_s + R_f)^2 + \omega^2 C_{gs}^2 R_s^2 R_f^2 \right\}}{T_0 R_s (1 - g_m R_f)^2}.$$ \hspace{1cm} (2.44)
Table 2.2: Simulation results for resistive-feedback circuit.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Bias Voltage (V)</th>
<th>Bias Current (mA)</th>
<th>$R_f$ (Ω)</th>
<th>Noise Figure (dB)</th>
<th>$S_{11}$(dB)</th>
<th>$S_{21}$(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATF-33143</td>
<td>1.0</td>
<td>801</td>
<td>260</td>
<td>1.06-1.07</td>
<td>-12.9 to -8.4</td>
<td>13.5-13.8</td>
</tr>
<tr>
<td>ATF-34143</td>
<td>1.0</td>
<td>411</td>
<td>400</td>
<td>1.03-1.04</td>
<td>-13.5 to -10.2</td>
<td>14.5-14.7</td>
</tr>
<tr>
<td>ATF-35143</td>
<td>1.0</td>
<td>199</td>
<td>400</td>
<td>1.24-1.25</td>
<td>-10.5 to -10.1</td>
<td>12.7-12.8</td>
</tr>
<tr>
<td>ATF-38143</td>
<td>1.1</td>
<td>461</td>
<td>490</td>
<td>0.78-0.79</td>
<td>-13.5 to -10.3</td>
<td>16.6-16.9</td>
</tr>
</tbody>
</table>

The circuit given in Figure 2.13 was simulated for selected transistors and achieved the results shown in the Table 2.2 for the 400 MHz-to-800 MHz frequency range.

These results show relatively high noise figures, which are similar to the results in Table 2.1, but with higher gain.

The shunt-feedback amplifier can be used as a part of a noise-canceling circuit. The circuit shown in Figure 2.15 illustrates a resistive-feedback noise-canceling LNA, which has an unbalanced differential output [2]. The capability of giving a lower noise figure compared to a conventional resistive-feedback amplifier circuit without additional components is an advantage in this topology. This characteristic can be observed by comparing the noise factor equations derived in Appendices F and G for conventional resistive-feedback circuits and the topology proposed in [2], whose noise factor is

$$
F = 1 + \frac{\left\{ \left(1 + g_{ds}R_s + g_mR_s \right)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{R_f R_s (g_m + g_{ds})^2} + \frac{T_{ggs} \left\{ g_m^2 + \omega^2 C_{gs}^2 R_s^2 g_{ds}^2 \right\}}{T_0 R_s (g_m + g_{ds})^2} + \frac{T_{dgsd} \left\{ 1 + \omega^2 C_{gs}^2 R_s^2 \right\}}{T_0 R_s (g_m + g_{ds})^2}. \quad (2.45)
$$

By analyzing (2.44) and (2.45), it can be seen that the drain noise contribution is always higher in the case of the conventional topology. Furthermore, the gate noise contribution is also higher in the conventional circuit for sufficiently high feedback resistance or when $\omega \ll \omega_r$. If $g_{ds}$ is very small compared to $g_m$, the noise contribution from the feedback resistor is also higher in the conventional circuit.
**Figure 2.15:** Resistive-feedback circuit proposed in [2].

**Table 2.3:** Simulation results for noise-canceling resistive-feedback topology.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Bias Voltage (V)</th>
<th>Bias Current (mA)</th>
<th>$R_f$ (Ω)</th>
<th>Noise Figure (dB)</th>
<th>$S_{11}$(dB)</th>
<th>$S_{21}$(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATF-33143</td>
<td>1.0</td>
<td>801</td>
<td>260</td>
<td>0.95</td>
<td>-2.2 to -2.0</td>
<td>3.5-3.6</td>
</tr>
<tr>
<td>ATF-34143</td>
<td>1.0</td>
<td>411</td>
<td>400</td>
<td>0.85-0.87</td>
<td>-2.9 to -2.7</td>
<td>3.7-3.8</td>
</tr>
<tr>
<td>ATF-35143</td>
<td>1.0</td>
<td>199</td>
<td>400</td>
<td>0.99</td>
<td>-4.1 to -4.0</td>
<td>3.2</td>
</tr>
<tr>
<td>ATF-38143</td>
<td>1.1</td>
<td>461</td>
<td>490</td>
<td>0.63-0.64</td>
<td>-2.3 to -2.2</td>
<td>4.1-4.2</td>
</tr>
</tbody>
</table>

Simulation results for a noise-canceling resistive feedback LNA are shown in Table 2.3 for the same biasing conditions as in Table 2.2. By comparing Table 2.2 and Table 2.3, it can be seen that for the same biasing conditions and similar component parameters, resistive feedback amplifiers with differential output have a lower noise figure but also lower gain. It can be seen that output port impedance $Z_L$ and feedback resistance $R_f$ are parallel to each other, which reduces the input impedance as compared to the standard resistive-feedback amplifier. This results in shifting the $S_{11}$ values to the short circuit side of the Smith chart. Hence, it has given worse $S_{11}$ results for given bias conditions.

Figure 2.16 shows a resistive-feedback common-gate hybrid amplifier [3], which is a wide-band differential amplifier circuit. Based on [3], the voltage gain of the circuit is
Figure 2.16: Differential resistive-feedback circuit proposed in [3].

Given as

\[
\text{Gain} = \frac{2 (g_{m1} + g_{m2}) R_f - 1 + \frac{R_f}{r_0} + sR_f (C_{ds} - C_{gd})}{1 + \frac{R_f}{r_0} + sR_f (C_{gd} + C_{ds})}
\] (2.46)

where \(g_{m1} = g_{m3}\) and \(g_{m2} = g_{m4}\). The input impedance is given by

\[
Z_{in} = \frac{r_0 + R_f}{2 ((g_{m1} + g_{m2}) r_0 + 1)}.
\] (2.47)

The approximate noise factor is

\[
F \approx 1 + \frac{\gamma}{\alpha} \frac{1}{2 (g_{m1} + g_{m2}) R_s} + \frac{8R_s}{R_f}.
\] (2.48)

In the equations given above, \(R_s\) is signal generator resistance and \(r_0\) is drain-source small-signal resistance.

Wang et al. [3] demonstrated this topology using a 0.13 µm CMOS technology with a noise figure of 4 dB within 100 MHz to 930 MHz. The implemented LNA draws 0.6 mA from a 1.2 V voltage source while maintaining the input match for the frequency range of
interest. Nevertheless, the noise contribution from the common-gate transistors $M_2$ and $M_4$ as demonstrated in (2.38) increases the overall noise figure of this topology as compared to the conventional resistive-feedback amplifier.

A noise-canceling resistive-feedback circuit was proposed in [59] as shown in Figure 2.17. In this circuit, transistor $M_2$ and resistor $R_1$ add the phase inverted and amplified noise signal to the gate of $M_1$ and work to partially cancel out the noise of the $M_1$ transistor. The circuit shown in Figure 2.17 was utilized in [59] to build a differential wide-band LNA and to achieve 7 GHz bandwidth, 17 dB voltage gain, and 2.4 dB noise figure at 3 GHz with 0.13 µm CMOS technology.

While there were many implementations of resistive shunt-feedback amplifiers, their noise figures do not approach that of source-degenerated amplifiers discussed in Subsection 2.7.3.

Figure 2.17: Noise-canceling resistive-feedback amplifier.
Figure 2.18: Noise-canceling circuits proposed in [4]

2.7.5 Noise-Canceling LNA Topologies

The noise reduction in LNA topologies discussed in Sections 2.7.1-2.7.4 is achieved by tuning the transistor parameters, bias conditions, and attached component parameters to get close to the noise match condition. But, there are some other techniques, which can be used to cancel the noise generated in the amplifiers.

Figures 2.18a and 2.18b illustrate noise-canceling circuits proposed in [4]. In the topology shown in Figure 2.18a, $M_a$ provides the input power match while drain noise of $M_a$ is canceled via the noise-canceling path. This topology is only capable of low gain. The LNA realized by Bruccoleri et al. [4] based on Figure 2.18a in a 0.35 $\mu$m CMOS technology had only 6.2 dB-to-11 dB gain and was able to achieve 4.3 dB-to-4.9 dB noise figure in a 400 MHz-to-900 MHz band.

An alternative noise-canceling technique was introduced in [5] and the circuit is illustrated in Figure 2.19. This circuit was implemented using 0.25 $\mu$m technology and was able to achieve 2.4 dB noise figure in a 0.01 GHz-to-2 GHz band, with 13.7 dB voltage gain, while drawing 14 mA current at 2.5 V. This circuit cancels the drain noise generated by $M_1$ with an amplifier circuit and an adder.

Blaakmeer et al. [6] introduced a wide-band noise-canceling circuit topology, which
Figure 2.19: Noise-canceling technique presented by Bruccoleri et al. [5]

Figure 2.20: Common-gate common-source topology proposed in [6]

is shown in Figure 2.20. This circuit is a combination of common-source-and common-gate-connected transistors and provides a differential output. The common-gate-connected transistor provides the input power match. This circuit cancels the drain noise generated in the common-gate-connected transistor. The expressions for voltage gain and noise factor for this topology are derived in Appendix H. The work in [6] demonstrated a sub-3.5 dB noise figure and 15 dB gain in a 65 nm technology at a 1.2 V supply voltage.

It is clear by observing the noise figures achieved using noise-canceling techniques described above that these techniques cannot achieve the very low noise figures with source-degenerated amplifier topologies and their variants. Hence, these techniques are not considered as viable options in this thesis.
2.8 Discussion

Several low-noise amplifier topologies were reviewed in this chapter for consideration as potential candidates for the first stage of the LNA investigated in this thesis. Observing (2.33) and (2.38), it can be seen that noise factor values for common-gate and common-source amplifiers are nearly equal for the same biasing currents and voltages. Additionally, the noise factor expression given in (2.40) for a source-degenerated amplifier is close to the noise factor of common-source amplifiers for the same biasing conditions if high-quality-factor inductors are chosen. The noise factor of resistive-feedback amplifier topologies is higher than that of common-gate, common-source, or source-degenerated amplifiers according to (2.44) and (2.45) due to the noise contribution from the feedback resistance.

Source-degenerated amplifiers are advantageous over common-gate and common-source amplifiers because they have multiple parameters for adjusting their input impedance. For example, biasing points and discrete components $L_g$, $L_s$, and $C_{ext}$ can be used for adjustment of the input impedance. Furthermore, multiple techniques exist as discussed in Section 2.7.3 to widen the operating frequency of the amplifier. The existence of multiple variants, such as folded cascode, for the source-degenerated amplifier topology allows for flexibility in optimizing the targeted LNA design as well.

2.9 Conclusion

The inductive source-degenerated amplifier and its variants are identified as the most suitable candidates for this research project due to their capability of achieving low noise figures and control of their input impedance via adjusting biasing points and values of $L_g$, $L_s$, and $C_{ext}$. Furthermore, the possibility of widening the operating frequency range by utilizing the techniques demonstrated in [19, 53–55, 57] is an added advantage as wideband low-noise match is necessary to achieve low noise figure in the 400 MHz-to-800 MHz frequency region.
The design of the first stage and selection of topologies for subsequent stages and design of the complete LNA are discussed in detail in Chapter 3. Simulation results of the final design are also presented in Chapter 3. Chapter 4 demonstrates the experimental performance of the final design based on selected topologies and comparison between simulations and collected experimental data.
Chapter 3

Low-Noise Amplifier Design for 400 MHz-to-800 MHz Frequency Range

3.1 LNA Architecture

The proposed LNA design architecture block diagram is shown in Figure 3.1.

The front end of the amplifier should consist of a very-low-noise amplifier circuit. This is expected to have a single-ended input and single-ended output. The single-ended input can be considered connected to a 50 Ω port for design purposes although in reality it will be connected to the antenna element. The effect of the antenna array will be considered and corrected in the later stage of the design process. The second stage of the design should be able to maintain the low-noise operation while increasing the gain of the circuit. As explained in Section 2.7.3, wideband source-degenerated amplifier topologies such as a folded-cascode circuit [53], cascode-amplifier topology [54], and modified-cascode amplifier [19, 55] topology utilize the second stage, which in combination with the front-end stage increases the bandwidth of the design. Hence, it would be an added advantage for the design if such a topology is used in the design. This stage is also a circuit with a single-ended input/output. The third stage is a buffer stage, which increases the gain while providing a single-ended output match to a 50 Ω port.

The subsequent sections of this chapter explain the design process of the three stages of the LNA.

![Figure 3.1: LNA block diagram. In this diagram, $A_f$, $A_s$, $A_b$ denote the first, second, and third stages of the LNA, respectively.](image-url)
Table 3.1: Key parameters of GaAs p-HEMT transistors.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Nominal Noise Figure (dB)&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Gate width (µm)</th>
<th>Power Gain (dB)&lt;sup&gt;b&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATF-33143 [46]</td>
<td>0.5</td>
<td>1600</td>
<td>15.0</td>
</tr>
<tr>
<td>ATF-34143 [47]</td>
<td>0.5</td>
<td>800</td>
<td>17.5</td>
</tr>
<tr>
<td>ATF-35143 [48]</td>
<td>0.4</td>
<td>400</td>
<td>18.0</td>
</tr>
<tr>
<td>ATF-38143 [49]</td>
<td>0.4</td>
<td>N/A</td>
<td>16.0</td>
</tr>
<tr>
<td>ATF-531P8 [60]</td>
<td>0.6</td>
<td>N/A</td>
<td>20.0</td>
</tr>
<tr>
<td>ATF-54143 [61]</td>
<td>0.5</td>
<td>800</td>
<td>16.6</td>
</tr>
<tr>
<td>ATF-58143 [62]</td>
<td>0.5</td>
<td>N/A</td>
<td>16.5</td>
</tr>
<tr>
<td>ATF-55143 [63]</td>
<td>0.6</td>
<td>400</td>
<td>17.7</td>
</tr>
<tr>
<td>ATF-551M4 [64]</td>
<td>0.5</td>
<td>400</td>
<td>17.5</td>
</tr>
</tbody>
</table>

<sup>a</sup>noise figure at the conditions defined in the data sheets of the transistors.<br>
<sup>b</sup>available power gain at the conditions defined in the datasheets of the transistors.

3.2 Transistors

Low-noise amplifier designs require transistors as active elements to provide sufficient gain. In this work, GaAs pseudomorphic High-electron-mobility transistors (p-HEMTs) are used since they are available in the open market as off-the-shelf components with low-noise properties. Table 3.1 depicts the important parameters of a group of GaAs transistors available in the market.

In this work, only simulations performed with ATF-33143, ATF-34143, and ATF-35143 transistors are shown because they were deemed to have lower-noise properties within the 400 MHz-to-800 MHz frequency band compared to other transistors shown in Table 3.1 based on criteria used in Subsection 3.2.1.

3.2.1 Comparison of ATF-33143, ATF-34143, and ATF-35143 using Standard Inductive-source-degenerated Amplifier Circuit

ADS simulations were performed using selected ATF-series transistors to compare their performance based on their noise figure and S-parameters. A standard inductive-source-degenerated amplifier was used to create the circuits used for parameter extractions. The circuits used are shown in Figures 3.2a, 3.2b, and 3.2c. Both the input and output of the
Figure 3.2: Circuits for simulation of standard inductive-source-degenerated amplifiers with GaAs transistors.

The amplifier are connected to 50 Ω ports. The circuit parameters are chosen to have a noise match at 800 MHz.

Noise performance simulation results comparison between ATF-33143, ATF-34143, and ATF-35143 LNA circuits is shown in Figure 3.3. By observing Figure 3.3, it can be seen that both noise figure and the minimum noise figure, \( NF_{\text{min}} \), are higher by 0.1 dB in the circuit with the ATF-34143 transistor compared to the circuit with the ATF-33143 transistor despite Table 3.1, which shows that nominal noise figures of the two transistors should be equal. Nevertheless, the noise-figure results obtained in simulations for the desired frequency range appear lower than nominal noise figures as given in the corresponding...
Figure 3.3: Minimum noise figure, $NF_{min}$, and noise figure, $NF$, of LNA circuits with ATF-33143, ATF-34143, and ATF-35143.

data sheets of the selected transistors. Additionally it can be seen that the $NF_{min}$ of the circuit with ATF-35143 is lower than both of the other circuits, although the noise figures of this circuit at lower frequencies are much higher compared to circuits with ATF-33143 and ATF-34143 transistors. The reason for this can be observed from the Smith chart in Figure 3.4 and from the plot for equivalent noise resistance of the circuits in Figure 3.5. According to the Smith chart, optimum noise reflection coefficient $\Gamma_{opt}$ values at lower frequencies for the circuit with ATF-33143 are slightly farther away from the center of the Smith chart compared to the other two circuits. According to Figure 3.5, the equivalent noise resistance for the circuit with ATF-35143 is significantly higher than other circuits. Hence, it can be deduced that the noise figure of the circuit with ATF-35143 should have a higher noise figure at lower frequencies based on (A.3).

S-parameters for the circuits are shown in Figure 3.6a and 3.6b. It can be observed that the circuit with ATF-34143 has a greater -10dB input bandwidth ($S_{11}$) than the other two circuits, although a part of that bandwidth falls outside the desired frequency region of 400MHz-to-800MHz. According to Figure 3.6b, $S_{21}$ parameters of the circuits are in the range of 18dB to 21dB within the frequency region.

40
Figure 3.4: $\Gamma_{opt}$ of LNA circuits with ATF-33143, ATF-34143, and ATF-35143.

Since the front-end of the LNA circuit should generate the lowest noise possible across the 400MHz-to-800MHz frequency region, it seems that the ATF-33143 transistor is the most suitable candidate for the front-end stage. This is despite the fact that the ATF-35143 transistor gives better noise at higher frequencies compared to ATF-35143. Since the -10dB input bandwidth is about 250MHz for the circuit with the ATF-33143 transistor, it indicates that subsequent stages should assist in increasing the bandwidth by using wide-band LNA topologies [19,53–55] .

3.3 Front-end Stage

Inductive-source-degenerated amplifier topologies were identified in Chapter 2 as suitable candidates for the first stage of the circuit. A standard inductive-source-degenerated amplifier, a cascode amplifier circuit [54], a modified wide-band-cascode circuit [19,55], and
Figure 3.5: $R_n$ of LNA circuits with ATF-33143, ATF-34143, and ATF-35143.

A folded-cascode circuit [53] are shown in Figure 3.7a, 3.7b, 3.7c and 3.7d, respectively. Among those topologies, the folded-cascode topology has a special characteristic of having a second stage, which contributes to improving the bandwidth of the overall LNA. But standard folded-cascode topology [53] cannot be implemented using GaAs HEMT transistors available as off-the-shelf components because there are no suitable p-channel versions of the HEMT capable of performing as well as the n-channel version. However, it is possible to implement this topology using two n-channel versions of p-HEMT transistors by slightly modifying the standard folded-cascode topology as shown in Figure 3.8. In this modification, the original p-channel transistor in the second stage is replaced by an n-channel transistor whose terminals are connected in the same way as in the original topology. Then, the power and ground terminals connected to second-stage transistor source and drain terminals are interchanged to establish the suitable power supply arrangement for a common-gate connected n-channel transistor.

Cascode and modified cascode amplifier topologies also have the potential of providing wider bandwidths while generating low noise although they are single-stage topologies as explained in Section 2.7.3.

The merits of aforementioned topologies for an LNA design for 400MHz-to-800MHz
Figure 3.6: S-parameters of the circuits shown in Figures 3.2a, 3.2b, and 3.2c.

using ATF-33143 transistors was evaluated using the ADS software simulations. The noise figure and S-parameter values are the focus of these simulations in order to determine the most suitable topology. ATF-33143 was the choice as the transistor due to the low noise figure demonstrated in Section 3.2.1 for a wider frequency range compared to other transistors. Since the standard inductive source-degenerated-amplifier topology was already evaluated in Section 3.2.1, the cascode-amplifier topology, the modified-cascode-
(a) Standard inductive-source-degenerated amplifier.

(b) Cascode amplifier topology.

(c) Modified wideband-cascode amplifier topology [54].

(d) Folded-cascode amplifier topology [53].

Figure 3.7: Variants of inductive-source-degenerated amplifiers.
amplifier topology, and the modified folded-cascode-amplifier topology are evaluated in Section 3.3.1.

3.3.1 Evaluation of Variants of Inductive-source-degenerated Amplifier Topologies

It was demonstrated in Section 3.2.1 that the standard inductive-source-degenerated amplifier topology cannot give the required wide -10dB input bandwidth, although it has a low noise figure across the 400MHz-to-800MHz frequency region. Additionally, by the observation of Figure 3.6b, it can be seen that the gain of the circuit drops significantly in the high frequency region.

Hence, it is necessary to evaluate variants of the cascode topology to determine the best topology for the design. Another benefit of choosing variants of the cascode circuit is that those circuits incorporate both the front and the second stages of the LNA, which give higher gain than the standard inductive-source-degenerated amplifier.

The evaluation of each topology was done by performing ADS simulations on the three topologies shown in Figures 3.9a, 3.9b and 3.9c. All of these circuits are noise matched at 800 MHz and all the external components to the ATF-33143 transistor are ideal compo-
Noise performances of the circuits are illustrated in Figure 3.10. It can be seen that both the cascode amplifier and the modified-cascode circuit have a slightly lower noise figure and $NF_{\text{min}}$ values (~0.01dB) than the modified folded-cascode circuit. However, by observing Figure 3.11a, it can be observed that the -10dB input bandwidth of the cascode circuit is at higher frequencies than the required frequency region. The -10dB input bandwidth of the modified-cascode circuit is at 390MHz-to-860MHz frequencies, while it is at 320MHz-to-920MHz frequencies for the modified folded-cascode circuit. Hence in that regard, the modified folded-cascode circuit shown in Figure 3.9c has an advantage over the other two circuits. Moreover, as illustrated in Figure 3.11b, $S_{21}$ for the modified folded-cascode circuit is relatively flat in the required frequency region while the other two circuits have rapidly decreasing $S_{21}$ with increasing frequency.

Based on simulation results, it was decided to choose the modified folded-cascode circuit as the starting point for the front-end and the second stages of the LNA design. This is due to the capability of getting better than -10dB input match and having a relatively flat $S_{21}$ profile while achieving 0.13dB to 0.19dB noise figure from 400MHz-to-800MHz.

### 3.4 Buffer Stage/ Output Stage of the LNA

All of the combined front-end/second-stage topologies discussed in Section 3.3.1 have the problem of unmatched output to a 50Ω port. By analyzing the $S_{22}$ graphs for those circuits, this issue can be identified as shown in Figure 3.11a. It can be seen that the output is highly mismatched to 50Ω in the desired 400MHz-to-800MHz frequency region. This issue can be resolved by adding another stage to the LNA design to act as a buffer between the second stage and the 50Ω output port. One drawback of this strategy is that it would increase the noise figure of the entire circuit by some amount. The equation (3.1) (Friis’s equation) depicts the relation between noise factors of each stage ($F_1$, $F_2$, $F_3$), the available gains of each stage ($G_1$, $G_2$, $G_3$), and the noise factor $F$ of the entire system shown in Figure 3.12.
Figure 3.9: Test circuit for variants of cascode-amplifier topologies.

\[
F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2}.
\]  

(3.1)

According to (3.1), it can be seen that although each stage adds more noise to the system, the added noise is reduced if the gain prior to the considered stage is sufficiently high. Hence, trading off noise figure to have a matched output to \( 50 \, \Omega \) is an acceptable choice. The potential candidates for the buffer stage amplifier circuit are described in Section 3.4.1.
**Table 3.2:** Amplifier circuit topologies

<table>
<thead>
<tr>
<th></th>
<th>Common Source</th>
<th>Common Source with Feedback</th>
<th>Source Follower</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain</td>
<td>$-g_mZ_L$</td>
<td>$\frac{Z_L\left[1-g_mR_f\right]}{Z_L+R_f}$</td>
<td>$\frac{g_mZ_L}{g_mZ_L+1}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\frac{-g_mZ_LR_f}{Z_L+R_f}$ if $g_mZ_L \gg 1$</td>
<td>1 if $g_mZ_L \gg 1$</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>$\infty$</td>
<td>$\frac{Z_L+R_f}{g_mZ_L+1}$</td>
<td>$\infty$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\frac{1}{g_m} + \frac{R_f}{g_mZ_L}$ if $g_mZ_L \gg 1$</td>
<td></td>
</tr>
<tr>
<td>Output Impedance</td>
<td>$Z_L$</td>
<td>$\frac{Z_LR_f}{Z_L+R_f}$</td>
<td>$\frac{Z_L}{g_mZ_L+1}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\frac{1}{g_m}$ if $g_mZ_L \gg 1$</td>
<td></td>
</tr>
</tbody>
</table>

**3.4.1 Comparison of Common-source Circuit, Resistive-feedback Circuit & Source-follower Circuit**

Simplified small-signal diagrams for a common-source resistive-feedback circuit and source-follower circuits are shown in Figures 3.13a, 3.13b, and 3.13c. Input/output impedances and voltage gains of each circuit are shown in Table 3.2.

It can be seen that the common-source amplifier has the highest gain while the source follower circuit has nearly a unity gain. Although high gain can be beneficial for the buffer
Figure 3.11: S-parameters of variants of a cascode circuit.

stage, it could cause instability in the complete LNA design. It can be also seen that both common-source and source-follower circuits have a high input impedance compared to the common-source circuit with resistive feedback. Typically, the buffer stage is expected to have high impedance at the input if the trace leading to the input of the buffer stage is sufficiently short (trace length < wavelength/20). However input impedance can be adjusted by setting the length of the trace leading to the input or placing a suitable shunt resistor, induc-
Figure 3.12: Friis equation block diagram for LNA design. Input-referred noise of each stage is denoted as $F_1$, $F_2$ and $F_3$. $G_1$, $G_2$ and $G_3$ denote the available voltage gain of each stage. $F$ is the input-referred noise of entire system.

Figure 3.13: Small-signal diagrams for various amplifier topologies.

In this work, the common-source circuit was selected for its adjustable output impedance, high input impedance, and high gain. Selection of a transistor with the proper gate width helps in achieving the output match because increasing the gate width reduces the drain-source resistance. This in turn reduces the gain and output impedance because both gain
Figure 3.14: Circuit for simulation of the S-parameters of the buffer stage.

Figure 3.15: $S_{21}$ parameters for the circuit in Figure 3.14.

and output impedance of the common-source amplifier are proportional to the term $Z_L$ as shown in Table 3.2. An $S_{21}$ (dB) graph and Smith chart of $S_{22}$ parameters for the circuit, shown in Figure 3.14, are illustrated in Figure 3.15 and Figure 3.16. It can be observed that $S_{22}$ values of large gate-width transistor (ATF-33143) fall in a lower impedance area compared to the other two transistors with lower gate width. In Figure 3.15, it can be seen that transistors with higher gate width have higher gain compared to other transistors. This can be due to increased $g_m$ contribution overshadowing the decreased drain-source resistance effect on the gain. ATF-34143 was selected as the output stage transistor since it is the most suitable transistor to have a good match to a $50\,\Omega$ port based on the results shown
in Figure 3.16.

3.5 Complete LNA Circuit

The final amplifier topology is shown in Figure 3.17.

The noise parameters of the complete circuit can be derived as shown in Appendix E and repeated here as

\[
R_n = \frac{1}{T_0} \left\{ \frac{\kappa}{(g_{m1} + \omega^2 C_{g1} L_s g_{ds1})^2} \right\} \tag{3.2}
\]

\[
B_{s,\text{opt}} = -\frac{\omega C_{g1}}{\kappa} \left[ 1 - \omega^2 C_{g1} (L_g + L_s) \right] T_{d1} g_{ds1} \tag{3.3}
\]
Figure 3.17: Complete LNA topology

where

\[ \kappa = \left( T_{g1} r_{g1} + T_0 R_g \right) \left( g_{m1} + \omega^2 C_{gs1} L_{s1} R_{ds1} \right)^2 \]

\[ + \left\{ \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right]^2 + \omega^2 C_{gs1}^2 R_g^2 \right\} T_{d1gds1}, \quad (3.4) \]

\[ G_{s, opt} = \psi \sqrt{T_{d1gds1} \left( \kappa - T_{d1gds1} \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right] \right)}, \quad (3.5) \]

where

\[ \psi = \frac{\omega C_{gs1}}{\kappa}, \quad (3.6) \]

and

\[ F_{\text{min}} = 1 + \frac{2 \omega C_{gs1} T_{d1gds1} \tau}{T_0 \left( g_{m1} + \omega^2 C_{gs1} L_{s1} R_{ds1} \right)^2}, \quad (3.7) \]

where

\[ \tau = \omega C_{gs1} R_g + \sqrt{\frac{\kappa}{T_{d1gds1}}} - \left\{ \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right]^2 \right\}. \quad (3.8) \]
3.5.1 Simulation Results of the Complete Design

The final LNA topology used for the simulation purposes is shown in Figure (3.17). Keysight Advanced Design System (ADS) software was used for obtaining the results shown in this section. The simulated power consumption of the complete circuit is \( P_{\text{input}} + P_{\text{cascode}} + P_{\text{output}} = 179.2\text{mW} + 329\text{mW} + 131\text{mW} = 639.2\text{mW} \). It was found out in Chapter 4, that the actual power consumption is much less than (<70%) of the simulated power consumption. The DC gate biasing voltages \( V_{b1} \) and \( V_{b2} \) for \( M_1 \) and \( M_3 \) transistors are provided by voltage dividing an external negative voltage source. \( V_{dd} \) is set to 1.4V in the simulation. Characteristics of the PCB were obtained by using an EM-simulation tool available in ADS software.

Transistor models provided for ATF-33143 and ATF-34143 by the manufacturer are based on a Statz Raytheon GaAsFET model [40].

3.5.1.1 Noise Performance

Simulated noise performance of the circuit is presented in Figure 3.18. It can be observed that a very low noise figure (<0.3dB) is obtained with the simulated circuit in the 400MHz-to-800MHz frequency region. Nevertheless, this result was obtained while using ideal components for \( C_1 \), \( C_2 \), \( C_3 \), and \( C_5 \) below 400 MHz. Unavailability of S-parameter values below 400MHz is the reason for not using the S-parameter files provided by the manufacturer for the aforementioned components below 400 MHz. Hence, it is justified to expect an increase in noise figure especially due to the thermal noise generated by the thermodynamic variations of number of charges on the capacitors. The simulated equivalent noise resistance and optimum noise reflection coefficient are also presented in Figures 3.19 and 3.20 in order to provide a complete description of noise parameters of the LNA.

Noise contributors to the circuit, which were extracted through the simulation at selected frequencies, are presented in Table 3.3. It can be observed that \( M_1 \) gate noise, \( M_1 \) drain noise, \( L_g \) gate inductor noise, \( L_1 \) biasing inductor noise, \( C_1 \) noise, and the PCB noise...
Figure 3.18: Simulated noise figure ($NF$) and minimum noise figure ($NF_{min}$) of LNA.

Figure 3.19: Simulated equivalent noise resistance ($R_n$) of LNA.

are the major contributors of input-referred noise across the frequency spectrum. Another important observation is that the flicker noise contributions from both $M_1$ and $M_2$ transistors are negligible even at 200MHz compared to drain and gate noise.

### 3.5.1.2 Noise Performance in the Antenna Array

Noise performance when both input and output of the LNA circuit are connected to 50 Ω ports were considered in Section 3.5.1.1. However the noise performance of the LNA cir-
cuit when installed in an antenna array would be different from the results shown in the previous section due to two factors. The first factor is that impedance looking into the antenna side from the input side can be different from $50 \Omega$. However, it can be easily corrected if that impedance is known. The second factor is more difficult to account for and is the result of noise emerging from an input of the LNA which couples with neighboring antennas in an antenna array if those antennas are closely placed. This coupled noise propagates through the neighboring LNAs towards their outputs. If beamformer coefficients are used to steer the beam direction, they further complicate the estimation of the noise performance of the array because both the coupling effect and the beamformer coefficients affect the final output noise.

There are multiple strategies available in the literature [65–67] to model the noise performance of an antenna array. In this work, the beam-equivalent receiver noise temperature
Table 3.3: Simulated input-referred noise voltages at selected frequencies by contributor.

<table>
<thead>
<tr>
<th>Noise Contributor</th>
<th>200 MHz&lt;sup&gt;a&lt;/sup&gt;</th>
<th>450 MHz</th>
<th>600 MHz</th>
<th>750 MHz</th>
<th>1000 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_1(M_1$ biasing inductor)</td>
<td>71.9 pV</td>
<td>45.8 pV</td>
<td>37.4 pV</td>
<td>28.4 pV</td>
<td>17.4 pV</td>
</tr>
<tr>
<td>$C_{b2}$ noise</td>
<td>33.3 pV</td>
<td>22.6 pV</td>
<td>7.4 pV</td>
<td>5.7 pV</td>
<td>2.8 pV</td>
</tr>
<tr>
<td>$C_1$ noise</td>
<td>N/A</td>
<td>17.5 pV</td>
<td>22.9 pV</td>
<td>17.2 pV</td>
<td>20.7 pV</td>
</tr>
<tr>
<td>$M_1$ gate noise</td>
<td>54.8 pV</td>
<td>37.3 pV</td>
<td>33.9 pV</td>
<td>36.0 pV</td>
<td>46.7 pV</td>
</tr>
<tr>
<td>$M_1$ drain noise</td>
<td>59.7 pV</td>
<td>48.9 pV</td>
<td>50.3 pV</td>
<td>57.4 pV</td>
<td>58.5 pV</td>
</tr>
<tr>
<td>$L_g$ gate inductor noise</td>
<td>34.7 pV</td>
<td>23.5 pV</td>
<td>25.1 pV</td>
<td>32.0 pV</td>
<td>48.0 pV</td>
</tr>
<tr>
<td>$C_{b1}$ noise</td>
<td>15.9 pV</td>
<td>9.1 pV</td>
<td>2.8 pV</td>
<td>2.1 pV</td>
<td>1.5 pV</td>
</tr>
<tr>
<td>PCB noise</td>
<td>18.2 pV</td>
<td>17.6 pV</td>
<td>19.7 pV</td>
<td>23.6 pV</td>
<td>30.1 pV</td>
</tr>
<tr>
<td>$M_1$ source terminal resistance noise</td>
<td>13.9 pV</td>
<td>9.4 pV</td>
<td>8.3 pV</td>
<td>7.9 pV</td>
<td>8.0 pV</td>
</tr>
<tr>
<td>Input connector</td>
<td>8.6 pV</td>
<td>10.3 pV</td>
<td>11.6 pV</td>
<td>14.4 pV</td>
<td>17.0 pV</td>
</tr>
<tr>
<td>$L_{s1}$</td>
<td>6.8 pV</td>
<td>4.9 pV</td>
<td>4.8 pV</td>
<td>5.0 pV</td>
<td>6.0 pV</td>
</tr>
<tr>
<td>$C_2$</td>
<td>N/A</td>
<td>3.5 pV</td>
<td>4.5 pV</td>
<td>5.7 pV</td>
<td>5.9 pV</td>
</tr>
<tr>
<td>$L_{s2}$</td>
<td>6.5 pV</td>
<td>5.4 pV</td>
<td>5.2 pV</td>
<td>5.4 pV</td>
<td>6.5 pV</td>
</tr>
<tr>
<td>$M_1$ flicker noise</td>
<td>3.7 pV</td>
<td>2.3 pV</td>
<td>2.0 pV</td>
<td>2.0 pV</td>
<td>1.6 pV</td>
</tr>
<tr>
<td>$M_1$ drain resistance noise</td>
<td>0.8 pV</td>
<td>2.0 pV</td>
<td>3.0 pV</td>
<td>4.5 pV</td>
<td>6.2 pV</td>
</tr>
<tr>
<td>$L_{2}$</td>
<td>1.7 pV</td>
<td>1.0 pV</td>
<td>0.9 pV</td>
<td>0.8 pV</td>
<td>0.3 pV</td>
</tr>
<tr>
<td>$M_2$ drain noise</td>
<td>3.4 pV</td>
<td>6.6 pV</td>
<td>9.5 pV</td>
<td>13.5 pV</td>
<td>18.5 pV</td>
</tr>
<tr>
<td>$M_2$ gate noise</td>
<td>2.8 pV</td>
<td>5.5 pV</td>
<td>8.0 pV</td>
<td>11.7 pV</td>
<td>16.6 pV</td>
</tr>
<tr>
<td>$M_2$ source terminal resistance noise</td>
<td>0.8 pV</td>
<td>1.5 pV</td>
<td>2.2 pV</td>
<td>3.1 pV</td>
<td>4.4 pV</td>
</tr>
<tr>
<td>$R_1$</td>
<td>0.8 pV</td>
<td>2.1 pV</td>
<td>3.6 pV</td>
<td>4.7 pV</td>
<td>3.3 pV</td>
</tr>
<tr>
<td>$R_2$</td>
<td>1.2 pV</td>
<td>2.6 pV</td>
<td>3.6 pV</td>
<td>3.7 pV</td>
<td>1.3 pV</td>
</tr>
</tbody>
</table>

<sup>a</sup>Input-referred noise at 200 MHz was extracted with ideal input capacitors for $C_1$, $C_2$, $C_3$ and $C_5$.

concept introduced in [67] is used to obtain the simulated noise performance of the LNA used with the antenna array. In this method, the noise performance of the entire system, consisting of antennas, LNAs, and beamformer coefficients, is represented by a noise temperature. S-parameters of the antenna array, S-parameters of the LNA circuit, and noise parameters of the LNA circuit are required to calculate the beam-equivalent receiver noise temperatures of the system. For the purpose of calculating beam-equivalent receiver noise temperatures, the antenna array was considered to have 41 metallic Vivaldi elements which are arranged as shown in Figure 3.21. Simulated S-parameters were used to characterize the antenna array. The beamformer coefficients for the antenna array elements 9-11, 20-22 and 31-33 were considered to be 1, since it was assumed that the outputs of LNAs attached
to those elements are combined with equal weights. The beamformer coefficients of rest of elements were assigned to 0.0001 since the outputs of those LNAs are terminated with 50Ω loads and function as active cold loads [68, 69].

Figure 3.22 shows the simulated beam-equivalent receiver noise temperatures ($T_{\text{rec}}$) for the system within the 310MHz-to-890MHz frequency region. According to Figure 3.22, $T_{\text{rec}}$ is 14.7K to 21.6K within the 390MHz-to-810MHz frequency region.
3.5.1.3 S-parameters and Voltage Gain

Simulated $S_{11}$ and $S_{22}$ for the LNA circuit are shown in Figure 3.23. The input match is better than -8.2 dB and output match is better than -13.5 dB within the 400 MHz-to-800 MHz frequency region.

The voltage gain (with 50 Ω output load) and $S_{21}$ obtained in the simulation are presented in Figure 3.24. It can be seen that simulated voltage gain is 38.6 dB to 41.0 dB while $S_{21}$ is 41.1 dB to 42.1 dB within the 400 MHz-to-800 MHz frequency region.

3.5.1.4 Linearity Metrics

Simulated IP1dB and IIP3 levels are shown in the Figure 3.25a and 3.25b. The minimum IP1dB level is -30.4 dBm while the minimum IIP3 level is -9.8 dBm within the 400 MHz-to-800 MHz frequency region. It can be observed that IP1dB values are improving in both lower and higher end of the considered frequency spectrum. This can be explained by noting that according to Figure 3.24, the voltage gain and $S_{21}$ are decreasing at lower and higher frequencies.

The relationship between simulated input power and output power of the designed LNA
Figure 3.24: Simulated $S_{21}$ and voltage gain of the LNA.

Figure 3.25: Simulated linearity metrics.

at 600 MHz is shown in Figure 3.26.

3.5.1.5 Stability Analysis

The $\mu$ and $\mu'$ test introduced in [70] is used in the thesis to determine the stability of the design. The $\mu$ test determines the stability from the load side while the $\mu'$ test determines the stability from the source side. In both cases if $\mu, \mu' > 1$, the circuit is unconditionally stable, while it is conditionally stable in other scenarios. Larger values of $\mu$ and $\mu'$ mean
**Figure 3.26:** Simulated input power vs. output power of the LNA at 600 MHz.

**Figure 3.27:** Simulated values of $\mu$ and $\mu'$.

greater stability.

Simulated $\mu$ and $\mu'$ values for the 200 MHz-to-1 GHz frequency region are shown in Figure 3.27. It can be seen that the circuit is unconditionally stable within the considered frequencies and remains stable over wider range.
3.6 Conclusion

The design of a low-noise amplifier for the 400MHz-to-800MHz frequency region is presented in this chapter.

The final LNA design has three cascaded stages. An inductive-source-degenerated amplifier was previously chosen to be the first stage in Chapter 2 after evaluating several LNA topologies. In this chapter, the selection of GaAs p-HEMT transistors was evaluated using ADS simulations to determine the most suitable transistor for the first stage. It was determined that ATF-33143 is suitable for the first stage transistor due to its better noise performance and better $S_{11}$ -10dB bandwidth.

Then, after evaluating several bandwidth extension techniques, it was decided that the modified folded-cascode topology is the most suitable topology, which also serves as the second stage. Better noise figure and -10dB input bandwidth were the advantages of this choice.

Suitable topologies for the output stage were reviewed, and it was determined that a common-source amplifier would be the best choice due to its high voltage gain. Then ATF-34143 was selected as the suitable transistor based on simulation results obtained. This choice allowed to achieve a better output match to a 50Ω port.

Finally, simulation results are presented for the complete design. Scattering parameters, noise simulation results, and linearity metrics were obtained for the complete design.
Chapter 4

Experimental Performance of the LNA

The LNA circuit designed in Section 3.5 was laid out and mounted on a Rogers 4003C substrate. The LNA circuit, the fabricated PCB, and the metal assembly are shown in Figure 4.1.

4.1 Measurement Methodology

The S-parameters, noise parameters, and linearity measurements were conducted in order to experimentally determine the performance of the designed LNA circuit. The stability condition of the design was also derived based on the measured S-parameters as well.

S-parameters and linearity measurements were conducted using an Agilent N5242A vector network analyzer (VNA). The noise measurement system was a combination of VNA, Agilent N8975A noise figure analyzer, noise source, and an impedance tuner. Three Agilent N4000A noise sources (MY44420504, MY44420729, MY44420986) were used for the noise measurement hereby denoted as noise sources 1, 2, and 3. The tuner, noise

Figure 4.1: Complete LNA circuit, PCB and the assembly.
sources and PCBs were contained within an aluminum box to reduce the interference from external signals. Then the measurement equipment and the aluminum box were placed in a metallic shielded room in order to further isolate the system from outside interference. The modified Y-factor measurement technique explained in [71] was used to extract the noise parameters from the measurements taken with the noise figure analyzer.

4.2 Experimental Performance of the LNA Circuit

The experimental results obtained with the measurement system are presented in this section. Total measured power consumption of the LNA circuit is power supply voltage × drawn current = 290×1.4 = 406 mW. This is only 63.5% of the value obtained in the simulations as shown in the Section 3.5.1. It was observed that the models provided by the manufacturer for the transistors do not give the correct drain-source currents for given biasing conditions.

4.2.1 S-parameter Measurements

Two LNAs were built and measured. These are denoted by PCB 1 and PCB 2. $S_{21}$ measurement results for PCB 1 and 2 are shown in Figure 4.2. It can be seen that $S_{21}$ results from 250 MHz-to-1 GHz agree with the simulation within ±2dB. But it can be observed that the results at lower frequencies seem to slightly deviate from the simulation results. This deviation has most likely occurred due to transistor modeling inaccuracies in the low frequency region. Slight differences exist between the measurements likely caused by the tolerances of the components used on the PCBs. According to the results shown in Figure 4.2, $S_{21}$ is 41.1 dB - 43.3 dB within 400 MHz-to-800 MHz frequency region.

$S_{11}$ and $S_{22}$ measurement results are shown in Figure 4.3. The input match is better than -7.3 dB and output match is better than -9.5 dB within the 400 MHz-to-800 MHz frequency region. It can be observed that there are significant differences between the measured and simulated $S_{11}$ and $S_{22}$. But considering $S_{11}$, simulations agree with the mea-
Figure 4.2: $S_{21}$ measurement results for PCB 1 and 2. $S_{21,1}$, $S_{21,2}$ and $S_{21,s}$ denote the results of PCB 1, 2 and simulation.

measurements within the 400 MHz-to-800 MHz frequency region. Slight differences existing within 400 MHz-to-800 MHz frequencies would be caused by the tolerances of the components used for assembling the PCBs. But it can be observed that a local minimum of $S_{11}$ seen at 300 MHz in simulations has shifted to 240 MHz-260 MHz while a local minimum at 820 MHz shifted to 790 MHz-810 MHz. These local minimums can be adjusted by changing the $g_m/g_{ds}$ of input transistor $M_1$, $L_s$, $L_g$ and $C_2$. Hence, the reasons behind these deviations are likely due to transistor modeling inaccuracies, lack of modeling of interaction of $L_s$, $L_g$, and $C_2$ components with the PCB metal and substrate or device tolerances.

$S_{22}$ measurements somewhat deviated from the simulation results with local minimums shifted to lower and higher frequency.

4.2.2 Voltage Gain

The voltage gain measurements for the LNA circuit are shown in Figure 4.4. The voltage gain is 39.2 dB-41.4 dB within the 400 MHz-to-800 MHz frequency region.
Figure 4.3: $S_{xx}$ measurement results for PCB 1 and 2. $S_{xx,1}$, $S_{xx,2}$ and $S_{xx,s}$ denote the results of PCB 1, 2, and simulation.

Figure 4.4: Voltage gain (dB) measurements for PCB 1 and 2.

4.2.3 Linearity Measurements

Measurement results for the linearity metrics IP1dB and IIP3 for PCB 1 and 2 are shown in Figure 4.5a and 4.5b. It can be observed that IIP3 values are lower than the expected based on the simulation. IP1dB values agree with the simulation in frequencies beyond 800 MHz.
although when the frequency decreases below 800 MHz, simulation results and measured values deviate from each other. The cause for this deviation is likely due to the transistor models used in the simulation not modeling the non-linearity effects well. Furthermore, higher than expected $S_{21}$ values at lower frequencies cause IP1dB to deteriorate in lower frequencies. The minimum IP1dB level is -32.9 dBm while the minimum IIP3 level is -22.5 dBm within the 400 MHz-to-800 MHz frequencies.

### 4.2.4 Noise Measurements

Three different sets of noise measurements were taken using 3 calibrated noise sources for each LNA circuit.

Measurement results of the minimum noise figure $NF_{min}$, are shown in Figure 4.6a, 4.6b and 4.6c. It can be seen with all 3 measurement sets that $NF_{min}$ measurements mostly agree with the simulation up to 430 MHz frequency. Then they gradually deviate from the simulation results until reaching a maximum around 650 MHz. Then the difference between simulation results and measurements decreases until around 750 MHz where it can be observed that this difference starts to increase. Overall by considering all 3 measurement sets, the average $NF_{min}$ falls within 0.2 dB-0.33 dB for the 350 MHz-to-850 MHz frequency range.
Measurements of \( NF_{\text{min}} \) with noise source 1.

Measurements of \( NF_{\text{min}} \) with noise source 2.

Measurements of \( NF_{\text{min}} \) with noise source 3.

**Figure 4.6:** Minimum noise figure \( NF_{\text{min}} \) measurements from 3 noise sources. \( NF_{\text{min},1} \), \( NF_{\text{min},2} \) denote \( NF_{\text{min}} \) of PCB 1 and 2. \( NF_{\text{min,s}} \) denotes simulation result. Error bars represent values within single standard deviation from the average value.

The measurement results of the equivalent noise resistance \( R_n \) are shown in Figures 4.7a, 4.7b and 4.7c. It can be observed that there is an increase in equivalent noise resistance for all frequencies in all 3 measurement sets compared to the simulation. This deviation gradually increases with the frequency except around 650 MHz where there is an anomaly. Furthermore, it can be observed that with all 3 noise sources, standard deviations of \( R_n \) measurements increase with decreasing frequency. The possible reason for this phenomenon would be that the impedance tuner used for measurements can only provide impedance...
points around the Smith chart above 800 MHz. This issue would introduce errors in measurements below 800 MHz.

Deviations in measurements from the simulation results can occur due to a combination of multiple reasons. Firstly, the actual temperature of GaAs p-HEMT transistors during its operation was not used in the simulation. It was observed that the temperature of the PCB (measured on the side with no components) was 310K which means GaAs transistor temperatures would be higher than 310 K. Additionally, the negative voltages required for biasing of transistors were supplied externally using a power supply, which introduces its
own noise to the PCB. Finally, inaccuracies in transistor models and systematic errors in the measurement system would also cause deviations as well.

Measured $\Gamma_{opt}$ results are shown in Figures 4.8a, 4.8b, 4.8c, 4.8d, 4.8e and 4.8f. It can be observed that with all 3 noise sources, standard deviations of $|\Gamma_{opt}|$ and $\angle \Gamma_{opt}$ decrease with increasing frequency as in the case of $R_n$ measurements; it is caused by the same reason.

The noise figures when the circuit is connected to 50 $\Omega$ input and output ports are shown in Figures 4.9a, 4.9b and 4.9c. Average noise figure falls within 0.25 dB-0.36 dB for the 390 MHz-to-810 MHz frequency region. Furthermore, it can be observed that simulated noise figure agrees with measured noise figure results until 490 MHz. Then, these two sets gradually deviate from each other until 850 MHz.

4.2.5 Estimated Beam-equivalent Receiver Noise Temperature in Antenna Array

Estimated beam-equivalent receiver noise temperatures based on measurements in Section 4.2.4 are shown in Figure 4.10a, 4.10b and 4.10c. The beamformer coefficient arrangement explained in Section 3.5.1.2 and simulated antenna array S-parameters were used for the calculation of beam-equivalent receiver noise temperatures. According to estimation, beam-equivalent receiver noise temperature [67] of the LNA circuit is 17.8 K-28.3 K within the 400 MHz-to-800 MHz frequency region.

4.2.6 Stability Analysis

$\mu$ and $\mu'$ test results for the 2 PCBs are presented in Figure 4.11. Both measurement results from the 2 PCBs indicate that the designed LNA circuit is unconditionally stable in the considered frequency region.
Figure 4.8: Optimum noise reflection coefficient ($\Gamma_{opt}$) measurements with 3 noise sources. $\Gamma_{opt,1}, \Gamma_{opt,2}$ denote the $\Gamma_{opt}$ of PCB 1 and 2. $\Gamma_{opt,s}$ denotes the simulation result. Error bars represent values within the single standard deviation from the average value.
Figure 4.9: Noise figures, $NF$, obtained with from 3 noise sources. $NF_1$, $NF_2$ denote $NF$ of PCB 1 and 2. $NF_s$ denotes the simulation result. Error bars represent values within the single standard deviation from the average value.

4.3 Conclusion

The LNA topology proposed in this thesis experimentally demonstrated a sub-0.36dB noise figure within the 390 MHz-to-810 MHz when the circuit was connected to 50Ω ports. Estimated beam-equivalent receiver noise temperature of the LNA circuit is 17.8 K-to-28.3 K within the 390 MHz-to-810 MHz frequency region. The input match $|S_{11}| < -7.3$ dB and output match $|S_{22}| < -9.5$ dB within the 390 MHz-to-810 MHz frequencies. $|S_{21}|$ values of the circuits are 41.1 dB to 43.3 dB within the 400 MHz-to-800 MHz frequency region. The
Figure 4.10: Estimated beam-equivalent receiver noise temperature ($T_{\text{rec}}$) within the 350 MHz-to-850 MHz frequency region. Error bars represent values within single standard deviation from the average value.

Linearity metrics were: IP1dB > -32.9 dBm while IIP3 > -22.5 dBm within the 400 MHz-to-800 MHz frequency region.
Figure 4.11: $\mu$ and $\mu'$ stability test for PCB 1 and 2. $\mu_1$ and $\mu'_1$ denote stability tests for PCB 1 while $\mu_2$ and $\mu'_2$ denote stability tests for PCB 2.
Chapter 5

Conclusions and future work

5.1 Thesis Summary

The design of a low noise amplifier operating in the 400 MHz-to-800 MHz frequency range is presented in this thesis.

The literature review for the theories related to LNA design was given in Chapter 2. Small-signal models for the GaAs p-HEMTs were reviewed and the noise contributors in the transistor were identified in Section 2.6. In Section 2.7, available low-noise amplifier topologies were reviewed, and their performance was evaluated based on their scattering parameters and noise-figure simulation results. Noise-canceling LNA topologies were reviewed in Section 2.7.5. It was identified that the inductive-source-degenerated low-noise amplifier topology and its variants are the best choice as the front end for the LNA.

Chapter 3 presented the three-stage amplifier design. In Section 3.2, the available GaAs p-HEMT transistors were evaluated, and the best transistor for the front end of the LNA circuit was identified. Bandwidth extension techniques were evaluated using the selected transistor, and the best topology for the combined front end and the second stage in Section 3.3 was identified. In Section 3.4, suitable topologies for the buffer stage were reviewed from which the best topology was selected. The complete LNA circuit was presented and evaluated through simulations in Section 3.5. The schematic representation of the LNA circuit is shown in Figure 3.17.

Chapter 4 presented the experimental performance of the designed LNA. Noise parameters, scattering parameters, linearity metrics, and expected noise performance within the array were shown in that chapter. A summary of measurement results is shown in Table 5.1.
Table 5.1: Measurement summary.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>This design (400 MHz - 800 MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Consumption</td>
<td>406 mW</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>&lt; 0.36 dB</td>
</tr>
<tr>
<td>Beam-equivalent receiver noise temperature</td>
<td>17.8 K - 28.3 K</td>
</tr>
<tr>
<td>$</td>
<td>S_{11}</td>
</tr>
<tr>
<td>$</td>
<td>S_{22}</td>
</tr>
<tr>
<td>$</td>
<td>S_{21}</td>
</tr>
<tr>
<td>IP1dB</td>
<td>&gt; -32.9 dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>&gt; -22.5 dBm</td>
</tr>
</tbody>
</table>

5.2 Future Work

This thesis successfully demonstrates the feasibility of using GaAs p-HEMT transistors in a design of a low-noise amplifier for the 400 MHz-to-800 MHz frequency region. Nevertheless, there are a few points, which can be further investigated. This thesis did not explore the effect of reducing the power supply voltage on the amplifier for its performance in relation to its noise figure. Investigating this matter is worthwhile because reducing power consumption could be a preferred option, if the noise figure increase is tolerable. Additionally, due to spacing constraints in the current PCB layout, it was not possible to use a better biasing inductor $L_1$ in Figure 3.17. By rearranging the PCB layout, it would be possible to accommodate an inductor with better quality factor and improve the noise figure. Furthermore, it is possible to improve the linearity metrics by increasing the power supply voltage of the output stage of the LNA design.
Bibliography


[38] H. Tian, K. W. Kim, M. A. Littlejohn, and U. K. Mishra, “Characteristics of In0.52Al0.48As/In0.53Ga0.47As/InP HEMT’s with n- and p-channel doping,” IEEE Transactions on Electron Devices, vol. 40, pp. 2362–2365, December 1993. (Cited on page 11.)


Appendix A

Important Equations

The relationship between minimum noise figure $F_{\text{min}}$, equivalent noise resistance $R_n$, optimal noise reflection coefficient $\Gamma_{\text{opt}}$ and noise figure $F$ is given by

$$F = F_{\text{min}} + \frac{4R_n |\Gamma_s - \Gamma_{\text{opt}}|^2}{Z_0 \left(1 - |\Gamma_s|^2 \right) \left|1 + \Gamma_{\text{opt}}\right|^2},$$  \hspace{1cm} (A.1)

where $Z_0$ is the characteristic impedance and $\Gamma_s$ is source reflection coefficient.

Let $\Gamma_{\text{opt}} = |\Gamma_{\text{opt}}| (\cos(\theta) + j \sin(\theta))$ and $\Gamma_s = |\Gamma_s| (\cos(\alpha) + j \sin(\alpha))$. Then (A.1) can be rearranged to

$$F = F_{\text{min}} + \frac{4R_n |\Gamma_{\text{opt}}|^2 + |\Gamma_s|^2 + 2|\Gamma_{\text{opt}}| |\Gamma_s| \cos(\theta) \cos(\alpha)}{1 + |\Gamma_{\text{opt}}|^2 + 2|\Gamma_{\text{opt}}| \cos(\theta)}.$$  \hspace{1cm} (A.2)

If $\Gamma_s = 0$, then equation (A.2) reduces to

$$F = F_{\text{min}} + \frac{4R_n}{Z_0} \frac{1}{1 + \frac{2 \cos(\theta)}{|\Gamma_{\text{opt}}|} + \frac{1}{|\Gamma_{\text{opt}}|^2}}.$$  \hspace{1cm} (A.3)
Appendix B

Derivation of Gain, Input Impedance and Noise Factor of a GaAs-transistor

Common-source Amplifier

The LNA schematic is presented in Figure B.1 and the small-signal model in Figure B.2. Based on Figure B.2, the input impedance $Z_{in}$ and voltage gain are

$$Z_{in} = r_{gs} + \frac{1}{sC_{gs}}$$

(B.1)
Gain = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-g_mZ_L}{(1 + g_{ds}Z_L)(1 + sC_{gs}r_{gs})}.
\text{(B.2)}

For \( r_{gs} \| sC_{gs} \ll 1 \),

\[ Z_{\text{in}} = \frac{1}{sC_{gs}} \quad \text{(B.3)} \]

Gain = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-g_mZ_L}{(1 + g_{ds}Z_L)}.
\text{(B.4)}

Based on Figure B.2, the noise contribution from each noise source to \( V_{\text{out}} \) i.e. \( V_{\text{out},i_s}, V_{\text{out},e_{gs}}, V_{\text{out},i_{ds}} \) are expressed in equations (B.5), (B.6) and (B.7) as

\[ V_{\text{out},i_s} = \frac{-Z_Lg_m i_s R_s}{(1 + g_{ds}Z_L)(1 + sC_{gs}R_s + sC_{gs}r_{gs})} \quad \text{(B.5)} \]

\[ V_{\text{out},e_{gs}} = \frac{Z_Lg_m e_{gs}}{(1 + g_{ds}Z_L)(1 + sC_{gs}R_s + sC_{gs}r_{gs})} \quad \text{(B.6)} \]

\[ V_{\text{out},i_{ds}} = \frac{-Z_Li_{ds}}{(1 + g_{ds}Z_L)} \quad \text{(B.7)} \]

The noise factor for this amplifier is derived as

\[ F = \frac{|V_{\text{out},i_s} + V_{\text{out},e_{gs}} + V_{\text{out},i_{ds}}|^2}{|V_{\text{out},i_s}|^2} = 1 + \frac{|V_{\text{out},e_{gs}}|^2}{|V_{\text{out},i_s}|^2} + \frac{|V_{\text{out},i_{ds}}|^2}{|V_{\text{out},i_s}|^2}, \quad \text{(B.8)} \]

where \( V_{\text{out},e_{gs}} \) and \( V_{\text{out},i_{ds}} \) are not correlated in Pospieszalski’s noise model. Based on (B.6), (B.7) and (B.5), the ratios between mean square noise voltages \( \frac{|V_{\text{out},e_{gs}}|^2}{|V_{\text{out},i_s}|^2}, \frac{|V_{\text{out},i_{ds}}|^2}{|V_{\text{out},i_s}|^2} \) are derived as

\[ \frac{|V_{\text{out},e_{gs}}|^2}{|V_{\text{out},i_s}|^2} = \frac{e_{gs}^2}{i_s^2 R_s^2} = \frac{T_g r_{gs}}{T_0 R_s} \quad \text{(B.9)} \]

\[ \frac{|V_{\text{out},i_{ds}}|^2}{|V_{\text{out},i_s}|^2} = \frac{i_{ds}^2}{i_s^2 g_m R_s^2} \left[ 1 + \omega^2 C_{gs}^2 (R_s + r_{gs})^2 \right] = \frac{T_d g_{ds}}{g_m^2 R_s^2 T_0} \left[ 1 + \omega^2 C_{gs}^2 (R_s + r_{gs})^2 \right] \quad \text{(B.10)} \]

Substituting (B.9), (B.10) into (B.8) results in the following

\[ F = 1 + \frac{T_g r_{gs}}{T_0 R_s} + \frac{T_d g_{ds}}{g_m R_s T_0} \left[ 1 + \omega^2 C_{gs}^2 (R_s + r_{gs})^2 \right]. \quad \text{(B.11)} \]
Appendix C

Derivation of Gain, Input Impedance, and Noise Factor of a GaAs-transistor

Common-gate Amplifier

Figure C.1 depicts the schematic of the common-gate amplifier, and the small-signal model for the common-gate amplifier is shown in Figure C.2. The voltage gain and input
impedance of the circuit are

\[
Gain = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{[g_m + g_{ds} + sC_{gs}r_{gs}g_{ds}]Z_L}{(1 + g_{ds}Z_L) (1 + sC_{gs}r_{gs})}
\]  
(C.1)

\[
Z_{\text{in}} = \frac{(1 + g_{ds}Z_L) (1 + sC_{gs}r_{gs})}{[g_m + g_{ds} + sC_{gs} (r_{gs}g_{ds} + Z_Lg_{ds} + 1)]}.
\]  
(C.2)

Assuming \( r_{gs} \ll |Z_L| \) and \( r_{gs} |sC_{gs}| \ll 1 \) results in

\[
Gain = \frac{[g_m + g_{ds}]Z_L}{(1 + g_{ds}Z_L)}
\]  
(C.3)

\[
Z_{\text{in}} = \frac{(1 + g_{ds}Z_L)}{[g_m + g_{ds} + sC_{gs} (Z_Lg_{ds} + 1)]}.
\]  
(C.4)

Based on the small-signal model in Figure C.2, noise contributions to the output \( V_{\text{out}} \) from each noise source i.e. \( V_{\text{out},i_s}, V_{\text{out},e_{gs}}, V_{\text{out},i_{ds}} \) can be calculated (assume \( V_{\text{in}} \approx V \)) as given below:

\[
V_{\text{out},i_s} = \frac{Z_L (g_m + g_{ds} + sC_{gs}r_{gs}g_{ds}) R_s i_s}{(1 + g_{ds}Z_L) (1 + sC_{gs}R_s) + R_s (g_m + g_{ds}) + sC_{gs}r_{gs} (1 + g_{ds}Z_L + g_{ds}R_s)}
\]  
(C.5)

\[
V_{\text{out},e_{gs}} = \frac{Z_L (g_m - g_{ds}R_s sC_{gs}) e_{gs}}{(1 + g_{ds}Z_L) (1 + sC_{gs}R_s) + R_s (g_m + g_{ds}) + sC_{gs}r_{gs} (1 + g_{ds}Z_L + g_{ds}R_s)}
\]  
(C.6)

\[
V_{\text{out},i_{ds}} = \frac{-Z_L i_{ds} (1 + sC_{gs}R_s + sC_{gs}r_{gs})}{(1 + g_{ds}Z_L) (1 + sC_{gs}R_s) + R_s (g_m + g_{ds}) + sC_{gs}r_{gs} (1 + g_{ds}Z_L + g_{ds}R_s)}
\]  
(C.7)

Based on (C.6), (C.7) and (C.5), the ratios between mean-square noise voltages \( |V_{\text{out},e_{gs}}|^2, |V_{\text{out},i_{ds}}|^2 \) and \( |V_{\text{out},i_s}|^2 \) are derived as
\[
\left| \frac{V_{\text{out},es}}{V_{\text{out},is}} \right|^2 = \frac{e_{gs}^2 (g_m^2 + \omega^2 C_{gs}^2 g_{ds}^2 R_s^2)}{i_{ds}^2 R_s^2 (g_m + g_{ds})^2 + \omega^2 C_{gs}^2 g_{ds}^2 r_{gs}^2} \\
= \frac{T_g r_{gs} (g_m^2 + \omega^2 C_{gs}^2 g_{ds}^2 r_{gs}^2)}{T_0 R_s [(g_m + g_{ds})^2 + \omega^2 C_{gs}^2 g_{ds}^2 r_{gs}^2]},
\]  
(C.8)

\[
\left| \frac{V_{\text{out},is}}{V_{\text{out},ds}} \right|^2 = \frac{\overline{i_{ds}^2}}{i_{ds}^2 R_s (g_m + g_{ds})^2 + \omega^2 C_{gs}^2 g_{ds}^2 r_{gs}^2} \frac{R_s^2}{R_s R_s} \left[ 1 + \omega^2 C_{gs}^2 (r_{gs} + R_s)^2 \right] \\
= \frac{T_d g_{ds}}{(g_m + g_{ds})^2 + \omega^2 C_{gs}^2 g_{ds}^2 r_{gs}^2} R_s T_0 \left[ 1 + \omega^2 C_{gs}^2 (r_{gs} + R_s)^2 \right].
\]  
(C.9)

By substitution of (C.8) and (C.9) into (B.8) the following is obtained:

\[
F = 1 + \frac{T_g r_{gs} (g_m^2 + \omega^2 C_{gs}^2 g_{ds}^2 R_s^2)}{T_0 R_s [(g_m + g_{ds})^2 + \omega^2 C_{gs}^2 g_{ds}^2 r_{gs}^2]} \\
+ \frac{T_d g_{ds}}{(g_m + g_{ds})^2 + \omega^2 C_{gs}^2 g_{ds}^2 r_{gs}^2} R_s T_0 \left[ 1 + \omega^2 C_{gs}^2 (r_{gs} + R_s)^2 \right]
\]  
(C.10)
Appendix D

Derivation of Gain, Input Impedance & Noise Factor of a GaAs-transistor

Source-degenerated Amplifier

The schematic and the small-signal model are shown in Figure D.1 and D.2.

Figure D.1: Schematic of inductive-source-degeneration amplifier

Figure D.2: The small-signal model for source-degeneration amplifier
Neglecting the effects of small inductor resistance, the voltage gain and input impedance of the LNA are

\[ \text{Gain} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{Z_L \left(s^2 g_{ds} C_{gs} L_s - g_m\right)}{\beta} \quad (D.1) \]

\[ Z_{\text{in}} = \frac{\beta}{s C_{gs} \left(s L_g g_{ds} + Z_L g_{ds} + 1\right)} \quad (D.2) \]

where

\[
\beta = s C_{gs} \left[s g_{ds} (L_s (s L_g + r_{gs}) + Z_L (L_g + L_s)) + s (L_s + L_g) + r_{gs} (1 + g_{ds} Z_L)\right] \\
+ s L_s (g_{ds} + g_m) + g_{ds} Z_L + 1. \quad (D.3)
\]

Assuming voltage drop across \( C_{gs} \) is very large compared to voltage drop across \( r_{gs} \), then noise contributions to the output \( V_{\text{out}} \) from each noise source i.e. \( V_{\text{out}, i_s} \), \( V_{\text{out}, e_{gs}} \), \( V_{\text{out}, i_d} \), \( V_{\text{out}, i_g} \) can be calculated as given below:

\[ V_{\text{out}, i_s} = \frac{R_s i_s Z_L \left(C_{gs} L_s s^2 g_{ds} - g_m\right)}{d} \quad (D.4) \]

\[ V_{\text{out}, i_g} = \frac{R_g i_g Z_L \left(C_{gs} L_s s^2 g_{ds} - g_m\right)}{d} \quad (D.5) \]

\[ V_{\text{out}, e_{gs}} = \frac{-e_{gs} Z_L \left(C_{gs} L_s s^2 g_{ds} - g_m\right)}{d} \quad (D.6) \]

\[ V_{\text{out}, i_d} = \frac{-Z_L i_d \left[1 + s C_{gs} (R_s + R_g + r_{gs}) + s^2 C_{gs} (L_g + L_s)\right]}{d}, \quad (D.7) \]

where

\[
d = C_{gs} \left[s^3 L_g L_s g_{ds} + s^2 g_{ds} (L_g Z_L + L_s R_s + L_s R_g + L_s Z_L + L_s r_{gs}) + s^2 (L_g + L_s) + \\
s (R_g + R_s + r_{gs}) (1 + g_{ds} Z_L)\right] + s L_s (g_{ds} + g_m) + Z_L g_{ds} + 1. \quad (D.8)
\]

Based on (D.4), (D.5), (D.6) and (D.7), the ratios between mean-square noise voltages

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\[ \left| V_{\text{out},e_{gs}} \right|^2, \left| V_{\text{out},i_s} \right|^2, \left| V_{\text{out},i_{ds}} \right|^2 \text{ and } \left| V_{\text{out},i_g} \right|^2 \text{ are derived as.} \]

\[
\frac{\left| V_{\text{out},e_{gs}} \right|^2}{\left| V_{\text{out},i_s} \right|^2} = \frac{e_{gs}^2}{i_s^2 R_s^2} = \frac{T_g r_{gs}}{T_0 R_s} \tag{D.9}
\]

\[
\frac{\left| V_{\text{out},i_s} \right|^2}{\left| V_{\text{out},i_s} \right|^2} = \frac{i_s^2 R_s^2}{i_s^2 R_s^2} = \frac{g}{R_s} \tag{D.10}
\]

\[
\frac{\left| V_{\text{out},i_{ds}} \right|^2}{\left| V_{\text{out},i_s} \right|^2} = \frac{R_{ds}^2}{i_s^2 R_s^2} \left| 1 + s C_{gs} (R_s + R_g) + s^2 C_{gs} (L_g + L_s) \right|^2
\]

\[
= T_d g_{ds} \left[ \frac{1 - C_{gs} \omega^2 (L_g + L_s)}{1 - C_{gs} \omega^2 (L_g + L_s)} \right]^2 + C_{gs}^2 (R_s + R_g + r_{gs}) \left| \omega^2 \right|^2 \frac{T_0}{T_0 R_s (g_m + g_{ds} L_s C_{gs} \omega^2)} \tag{D.11}
\]

Noise factor can be defined for a source-degenerated amplifier as

\[
F = \frac{\left| V_{\text{out},i_s} + V_{\text{out},e_{gs}} + V_{\text{out},i_{ds}} + V_{\text{out},i_g} \right|^2}{\left| V_{\text{out},i_s} \right|^2} = 1 + \frac{\left| V_{\text{out},e_{gs}} \right|^2}{\left| V_{\text{out},i_s} \right|^2} + \frac{\left| V_{\text{out},i_{ds}} \right|^2}{\left| V_{\text{out},i_s} \right|^2} + \frac{\left| V_{\text{out},i_g} \right|^2}{\left| V_{\text{out},i_s} \right|^2}. \tag{D.12}
\]

For sub-GHz frequencies, the noise factor can be approximated as given in equation (D.13) by substitution of (D.9), (D.10) and (D.11) to (D.12).

\[
F = 1 + \frac{R_g}{R_s} + \frac{T_g r_{gs}}{T_0 R_s} + T_d g_{ds} \left[ \frac{1 - C_{gs} \omega^2 (L_g + L_s)}{1 - C_{gs} \omega^2 (L_g + L_s)} \right]^2 + C_{gs}^2 (R_s + R_g + r_{gs}) \left| \omega^2 \right|^2 \frac{T_0}{T_0 R_s (g_m + g_{ds} L_s C_{gs} \omega^2)} \tag{D.13}
\]
Appendix E

Derivation of Noise Parameters for the Proposed Circuit

The small-signal diagram for the complete design is given in Figure E.1. For the ease of mathematical calculations, the complete design can be split into three cascade-connected 2-port networks as shown in Figure E.1. Based on the equations given in Section 2.2, noise sources of cascade representation $I_n$ and $V_n$ can be calculated as given below.

\begin{equation}
V_n = e_{gs1} - i_g R_g - \left[ \frac{1 - \omega^2 C_{gs1} (L_g + L_s) + j \omega C_{gs1} R_g}{\omega^2 C_{gs1} g_{ds1} L_s + g_m} \right] i_{ds1}
\end{equation}
(E.1)

\begin{equation}
I_n = \frac{-j \omega C_{gs1} i_{ds1}}{\omega^2 C_{gs1} g_{ds1} L_s + g_m}
\end{equation}
(E.2)

where

\begin{equation}
\overline{i_{ds1}^2} = 4kT_{ds1} g_{ds1} \Delta f
\end{equation}
(E.3)

\begin{equation}
\overline{e_{gs1}^2} = 4kT_{g1} r_{gs1} \Delta f
\end{equation}
(E.4)

\begin{equation}
\overline{i_g^2} = \frac{4kT_0 \Delta f}{R_g}.
\end{equation}
(E.5)

Then the following is found:

\begin{equation}
\frac{\overline{I_n I_n^*}}{\overline{V_n V_n^*}} = \frac{\omega^2 C_{gs1}^2 \overline{i_{ds1}^2}}{(g_m + \omega^2 C_{gs1} L_s g_{ds1})^2} = \frac{4kT_{ds1} g_{ds1} \Delta f \omega^2 C_{gs1}^2}{(g_m + \omega^2 C_{gs1} L_s g_{ds1})^2}
\end{equation}
(E.6)

\begin{equation}
V_n V_n^* = e_{gs1}^2 + i_g^2 R_g + \left\{ \frac{\left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right]^2 + \omega^2 C_{gs1}^2 R_g^2}{(g_m + \omega^2 C_{gs1} L_s g_{ds1})^2} \right\} \overline{i_{ds1}^2}
= 4k \Delta f \left\{ T_{g1} r_{gs1} + T_0 R_g + \left\{ \frac{\left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right]^2 + \omega^2 C_{gs1}^2 R_g^2}{(g_m + \omega^2 C_{gs1} L_s g_{ds1})^2} \right\} T_{ds1} g_{ds1} \right\}
\end{equation}
(E.7)
Figure E.1: Small-signal diagram for complete design.
\[
V_n^*T_n = 4k\Delta f \left\{ \frac{j\omega C_{gs1}}{(g_m1 + \omega^2 C_{gs1} L_d g_{ds1})^2} \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) + j \omega C_{gs1} R_g \right] T_{d1g_{ds1}} \right\} \quad (E.8)
\]

\[
V_n^*T_n = 4k\Delta f \left\{ \frac{j\omega C_{gs1}}{(g_m1 + \omega^2 C_{gs1} L_d g_{ds1})^2} \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) - j \omega C_{gs1} R_g \right] T_{d1g_{ds1}} \right\} \quad (E.9)
\]

The \( C_{ABCD} \) matrix would be

\[
C_{ABCD} = 2kT_0 \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} = \frac{1}{2\Delta f} \begin{bmatrix} V_n V_n^* & V_n T_n^* \\ V_n^* T_n & T_n T_n^* \end{bmatrix} \quad (E.10)
\]

Based on the equation (E.10), the parameters \( C_{11}, C_{12}, C_{21} \) and \( C_{22} \) can be calculated as given below.

\[
C_{11} = \frac{V_n V_n^*}{4kT_0 \Delta f} = \frac{1}{T_0} \left\{ T_{g1} r_{gs1} + T_0 R_g + \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right]^2 + \omega^2 C_{gs1}^2 R_g^2 \right\} T_{d1g_{ds1}} \right\} \quad (E.11)
\]

\[
C_{12} = \frac{V_n^* T_n}{4kT_0 \Delta f} = \frac{1}{T_0} \left\{ \omega C_{gs1} \left\{ \omega C_{gs1} R_g - j \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right] \right\} T_{d1g_{ds1}} \right\} \quad (E.12)
\]

\[
C_{21} = \frac{V_n^* T_n}{4kT_0 \Delta f} = \frac{1}{T_0} \left\{ \omega C_{gs1} \left\{ \omega C_{gs1} R_g + j \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right] \right\} T_{d1g_{ds1}} \right\} \quad (E.13)
\]

\[
C_{22} = \frac{T_n T_n^*}{4kT_0 \Delta f} = \frac{T_{d1g_{ds1}} \omega^2 C_{gs1}^2}{T_0 \left( g_m1 + \omega^2 C_{gs1} L_d g_{ds1} \right)^2} \quad (E.14)
\]

Based on equation 2.12, it can be determined that the noise correlation matrix of the complete circuit is equal to the noise correlation matrix of the first stage since noise correlation matrices of two later stages can be considered as a null matrix if the gain of the first stage is sufficiently high. The relationship between noise parameters noise resistance i.e. \( R_n \),
minimum noise factor \( F_{\text{min}} \), and optimal source admittance \( Y_{\text{opt}} (G_{\text{opt}} + jB_{\text{opt}}) \) as defined in [22, 23] can be calculated as given below.

\[
R_n = C_{11}
\]

\[
= \frac{1}{T_0} \left\{ T_{g1} r_{g1} + T_0 R_g + \left[ \frac{\left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right]^2 + \omega^2 C_{gs1}^2 R_g^2}{(g_{m1} + \omega^2 C_{gs1} L_s g_{ds1})^2} \right] T_{d1g_{ds1}} \right\}
\]

\[
= \frac{1}{T_0} \left\{ \frac{\kappa}{(g_{m1} + \omega^2 C_{gs1} L_s g_{ds1})^2} \right\},
\]

(E.15)

\[
B_{s,\text{opt}} = \frac{\text{Im}(C_{12})}{C_{11}} \frac{-\omega C_{gs1} \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right] T_{d1g_{ds1}}}{(g_{m1} + \omega^2 C_{gs1} L_s g_{ds1})^2}
\]

\[
= \frac{T_{g1} r_{g1} + T_0 R_g + \left[ \frac{\left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right]^2 + \omega^2 C_{gs1}^2 R_g^2}{(g_{m1} + \omega^2 C_{gs1} L_s g_{ds1})^2} \right] T_{d1g_{ds1}}}{\kappa}
\]

\[
= \frac{-\omega C_{gs1} \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right] T_{d1g_{ds1}}}{\kappa},
\]

(E.16)

where

\[
\kappa = \left( T_{g1} r_{g1} + T_0 R_g \right) \left( g_{m1} + \omega^2 C_{gs1} L_s g_{ds1} \right)^2
\]

\[
+ \left[ \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right]^2 + \omega^2 C_{gs1}^2 R_g^2 \right] T_{d1g_{ds1}},
\]

(E.17)

\[
G_{s,\text{opt}} = \varphi \sqrt{T_{d1g_{ds1}} \left\{ \kappa - T_{d1g_{ds1}} \left[ 1 - \omega^2 C_{gs1} (L_g + L_s) \right] \right\}}
\]

(E.18)

where

\[
\varphi = \frac{\omega C_{gs1}}{\kappa}
\]

(E.19)
\[ G_{s,\text{opt}} C_{11} = \sqrt{C_{11} C_{22} - [\text{Im}(C_{12})]^2} \]

\[ = \frac{1}{T_0} \sqrt{R_n C_{22} T_0^2 - \left( \frac{\omega C_{gsl} \left[ 1 - \omega^2 C_{gsl} (L_g + L_s) \right] T_{d1} g_{ds1}}{(g_{m1} + \omega^2 C_{gsl} L_s g_{ds1})^2} \right)^2}, \quad (E.20) \]

\[ \Re(C_{12}) = \frac{1}{T_0} \left( \frac{\omega C_{gsl} \left[ \omega C_{gsl} R_g \right] T_{d1} g_{ds1}}{(g_{m1} + \omega^2 C_{gsl} L_s g_{ds1})^2} \right)^2, \quad (E.21) \]

and

\[ F_{\text{min}} = 1 + \frac{2 \omega C_{gsl} T_{d1} g_{ds1} \tau}{T_0 \left( g_{m1} + \omega^2 C_{gsl} L_s g_{ds1} \right)^2}, \quad (E.22) \]

where

\[ \tau = \omega C_{gsl} R_g + \sqrt{\frac{\kappa}{T_{d1} g_{ds1}}} - \left\{ \left[ 1 - \omega^2 C_{gsl} (L_g + L_s) \right] \right\}^2. \quad (E.23) \]
Appendix F

Derivation of Gain, Input Impedance and Noise Factor of a GaAs-transistor

Resistive-feedback Amplifier

The amplifier schematic is presented in Figure F.1 and the small-signal model shown in Figure F.2. The voltage gain and input impedance of the circuit are

\[
Gain = \frac{V_{out}}{V_{in}} = \frac{Z_L (1 - g_m R_f + s C_{gs} r_{gs})}{(s C_{gs} r_{gs} + 1) (g_{ds} Z_L R_f + R_f + Z_L)} \tag{F.1}
\]

\[
Z_{in} = \frac{(s C_{gs} r_{gs} + 1) (g_{ds} Z_L R_f + R_f + Z_L)}{[s C_{gs} (g_{ds} Z_L R_f + g_{ds} Z_L r_{gs} + R_f + Z_L + r_{gs}) + g_{ds} Z_L + g_m Z_L + 1]} \tag{F.2}
\]

Considering \( s C_{gs} r_{gs} + 1 \approx 1 \) for sub-GHz frequencies and \( R_f + r_{gs} \approx R_f \) results in

\[
Gain \approx \frac{V_{in}}{V_{out}} = \frac{Z_L (1 - g_m R_f)}{g_{ds} Z_L R_f + R_f + Z_L} \tag{F.3}
\]

\[
Z_{in} \approx \frac{(g_{ds} Z_L R_f + R_f + Z_L)}{[s C_{gs} (g_{ds} Z_L R_f + R_f + Z_L) + g_{ds} Z_L + g_m Z_L + 1]} \tag{F.4}
\]

Figure F.1: Schematic diagram of a resistive-feedback amplifier.
Based on the small-signal model depicted in Figure F.2, the noise contribution from each noise source to the output noise $V_{out}$ i.e. $V_{out,i_s}, V_{out,e_{gs}}, V_{out,i_{ds}}, V_{out,i_f}$ can be given as below, assuming voltage drop across $r_{gs}$ is negligible compared to $V$:

$$V_{out,i_s} = \frac{Z_L \left(1 - g_mR_f\right) R_s i_s}{d} \quad (F.5)$$

$$V_{out,i_f} = \frac{Z_L (1 + g_mR_s + sR_sC_{gs}) R_f i_f}{d} \quad (F.6)$$

$$V_{out,e_{gs}} = \frac{Z_L (g_mR_s + g_mR_f + sC_{gs}R_s) e_{gs}}{d} \quad (F.7)$$

$$V_{out,i_{ds}} = -\frac{Z_L i_{ds} \left(R_f + R_s + sC_{gs}R_sR_f\right)}{d} \quad (F.8)$$

where

$$d = sC_{gs}R_s \left(g_{ds}Z_LR_f + R_f + Z_L\right) + Z_L \left(g_{ds}R_f + g_{ds}R_s + g_mR_s\right) + R_f + R_s + Z_L \quad (F.9)$$
Based on (F.5), (F.6), (F.7) and (F.6), the ratios between mean square noise voltages \( \frac{|V_{out,i_s}|^2}{|V_{out,i_d}|^2} \) and \( \frac{|V_{out,i_s}|^2}{|V_{out,i_d}|^2} \) are derived as.

\[
\frac{|V_{out,i_f}|^2}{|V_{out,i_s}|^2} = \frac{i_f^2 R_f^2 \left\{ (1 + g_m R_s)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{i_s^2 R_s^2 \left( 1 - g_m R_f \right)^2} = \frac{R_f \left\{ (1 + g_m R_s)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{R_s \left( 1 - g_m R_f \right)^2} \tag{F.10}
\]

\[
\frac{|V_{out,e_{gs}}|^2}{|V_{out,i_s}|^2} = \frac{e_{gs}^2 \left\{ g_m^2 (R_s + R_f)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{i_s^2 R_s^2 \left( 1 - g_m R_f \right)^2} = \frac{T_{g r_{gs}} \left\{ g_m^2 (R_s + R_f)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{T_0 R_s \left( 1 - g_m R_f \right)^2} \tag{F.11}
\]

\[
\frac{|V_{out,i_d}|^2}{|V_{out,i_s}|^2} = \frac{i_d^2 \left\{ (R_s + R_f)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{i_s^2 R_s^2 \left( 1 - g_m R_f \right)^2} = \frac{T_{d g_{ds}} \left\{ (R_s + R_f)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{T_0 R_s \left( 1 - g_m R_f \right)^2} \tag{F.12}
\]

The noise factor for this topology can be defined as

\[
F = \frac{|V_{out,i_s} + V_{out,e_{gs}} + V_{out,i_d} + V_{out,i_f}|^2}{|V_{out,i_s}|^2} = 1 + \frac{|V_{out,e_{gs}}|^2}{|V_{out,i_s}|^2} + \frac{|V_{out,i_d}|^2}{|V_{out,i_s}|^2} + \frac{|V_{out,i_f}|^2}{|V_{out,i_s}|^2} \tag{F.13}
\]

Substituting equations (F.10), (F.11) and (F.12) into (F.13) gives

\[
F = 1 + \frac{R_f \left\{ (1 + g_m R_s)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{R_s \left( 1 - g_m R_f \right)^2} + \frac{T_{g r_{gs}} \left\{ g_m^2 (R_s + R_f)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{T_0 R_s \left( 1 - g_m R_f \right)^2} + \frac{T_{d g_{ds}} \left\{ (R_s + R_f)^2 + \omega^2 C_{gs}^2 R_s^2 \right\}}{T_0 R_s \left( 1 - g_m R_f \right)^2} \tag{F.14}
\]
Appendix G

Derivation of Gain, Input Impedance & Noise Factor of a GaAs-transistor Partial Noise-cancellation Resistive-feedback Amplifier

The small-signal model for this topology is shown in Figure G.1. Assuming voltage drop across \( r_{gs} \) is small compared to the voltage across \( C_{gs} \) for sub-GHz frequencies, the differential voltage gain and input impedance of the circuit are found as

\[
Gain = \frac{V_{out} - V_{in}}{V_{in}} = \frac{- (R_f Z_L g_m - R_f - Z_L)}{(R_f Z_L g_{ds} + R_f + Z_L)} \tag{G.1}
\]

\[
Z_{in} = \frac{R_f Z_L g_{ds} + R_f + Z_L}{[sC_{gs} (g_{ds} Z_L + R_f + Z_L) + g_{ds} Z_L + g_m Z_L + R_f g_m + R_f g_{ds}]} \tag{G.2}
\]

The noise voltage contribution to the differential voltage output \( V_{out} - V_{in} \) i.e. \( V_{diff,i_s}, V_{diff,e_{gs}}, V_{diff,i_{ds}}, V_{diff,i_f} \) from the noise sources can be given as below.

\[
V_{diff,i_s} = \frac{-(g_{ds} + g_m) Z_L R_s R_f i_s}{d} \tag{G.3}
\]

Figure G.1: Small-signal model for the circuit proposed in [2]
Then the ratios between mean-square noise voltages

\[ V_{\text{diff},if} = \frac{(1 + g_m R_s + g_{ds} R_s + s R_s C_{gs}) Z_{L} R_f i_f}{d} \]  

(G.4)

\[ V_{\text{diff},egs} = \frac{(g_m - s C_{gs} R_s g_{ds}) Z_{L} R_f e_{gs}}{d} \]  

(G.5)

\[ V_{\text{diff},ids} = \frac{-(1 + s C_{gs} R_s) Z_{L} R_f i_{ds}}{d} \]  

(G.6)

where

\[ d = s C_{gs} R_s (g_{ds} Z_{L} R_f + R_f + Z_L) + R_f R_s (g_{ds} + g_m) + Z_L (g_{ds} R_f + g_{ds} R_s + g_m R_s) + R_f + Z_L. \]  

(G.7)

Then the ratios between mean-square noise voltages \( \frac{|V_{\text{diff},egs}|^2}{|V_{\text{diff},ifs}|^2} \), \( \frac{|V_{\text{diff},if}|^2}{|V_{\text{diff},g}|^2} \), \( \frac{|V_{\text{diff},ids}|^2}{|V_{\text{diff},ifs}|^2} \) and \( \frac{|V_{\text{diff},ifs}|^2}{|V_{\text{diff},ifs}|^2} \) are derived based on (G.3), (G.4), (G.5) and (G.6).

\[ \frac{|V_{\text{diff},if}|^2}{|V_{\text{diff},ifs}|^2} = \frac{\frac{7}{2} \{ (1 + g_{ds} R_s + g_m R_s)^2 + \omega^2 C_{gs}^2 R_s^2 \}}{\frac{7}{2} R_s^2 (g_m + g_{ds})^2} = \frac{\{ (1 + g_{ds} R_s + g_m R_s)^2 + \omega^2 C_{gs}^2 R_s^2 \}}{R_f R_s (g_m + g_{ds})^2} \]  

(G.8)

\[ \frac{|V_{\text{diff},egs}|^2}{|V_{\text{diff},ifs}|^2} = \frac{e_{gs}^2 \{ g_m^2 + \omega^2 C_{gs}^2 R_s^2 g_{ds}^2 \}}{\frac{7}{2} R_s^2 (g_m + g_{ds})^2} = \frac{T_{g r gs} \{ g_m^2 + \omega^2 C_{gs}^2 R_s^2 g_{ds}^2 \}}{T_0 R_s (g_m + g_{ds})^2} \]  

(G.9)

\[ \frac{|V_{\text{diff},ids}|^2}{|V_{\text{diff},ifs}|^2} = \frac{\frac{7}{2} \{ 1 + \omega^2 C_{gs}^2 R_s^2 \}}{\frac{7}{2} R_s^2 (g_m + g_{ds})^2} = \frac{T_{d g ds} \{ 1 + \omega^2 C_{gs}^2 R_s^2 \}}{T_0 R_s (g_m + g_{ds})^2} \]  

(G.10)

Substitution of (G.8), (G.9), and (G.10) into equation (F.13) gives

\[ F = 1 + \frac{\{ (1 + g_{ds} R_s + g_m R_s)^2 + \omega^2 C_{gs}^2 R_s^2 \}}{R_f R_s (g_m + g_{ds})^2} + \frac{T_{g r gs} \{ g_m^2 + \omega^2 C_{gs}^2 R_s^2 g_{ds}^2 \}}{T_0 R_s (g_m + g_{ds})^2} \]

\[ + \frac{T_{d g ds} \{ 1 + \omega^2 C_{gs}^2 R_s^2 \}}{T_0 R_s (g_m + g_{ds})^2} \]  

(G.11)
Appendix H

Derivation of Common-gate- and Common-source-hybrid Amplifier Gain, Noise Factor

The following equations are derived based on the criterion in [6]. In [6], only the drain noise current is considered for noise-figure calculation. The voltage gain is found as

$$A_v = \frac{V_{out}^+ - V_{out}^-}{V_{in}} = g_{m1}R_{cg} + g_{m2}R_{cs}. \quad (H.1)$$

The noise voltage contribution to the differential voltage output $V_{out} - V_{in}$ i.e. $V_{diff,i_s}$, $V_{diff,i_{d1}}$, $V_{diff,i_{d2}}$, $V_{diff,ig_c}$, $V_{diff,ig_s}$, $V_{diff,if}$ from the noise sources can be given as below.

$$V_{diff,i_s} = \frac{i_sR_sZ_L(g_{m1}R_{cg} + g_{m2}R_{cs})}{(R_{cg} + R_{cs} + Z_L)(1 + g_{m1}R_s)}, \quad (H.2)$$

Figure H.1: Small-signal diagram for common-gate and common-source hybrid amplifier.
\[ V_{\text{diff.}d1} = \frac{-i_{d1}Z_L(R_{cg} - g_m2R_s)}{(R_{cg} + R_{cs} + Z_L)(1 + g_m1R_s)}, \]  

(H.3)

\[ V_{\text{diff.}d2} = \frac{i_{d2}Z_LR_{cs}}{(R_{cg} + R_{cs} + Z_L)}, \]  

(H.4)

\[ V_{\text{diff.}r_{cg}} = \frac{-i_{r_{cg}}Z_LR_{cg}}{(R_{cg} + R_{cs} + Z_L)}, \]  

(H.5)

\[ V_{\text{diff.}r_{cs}} = \frac{i_{r_{cs}}Z_LR_{cs}}{(R_{cg} + R_{cs} + Z_L)}. \]  

(H.6)

The ratios between mean-squared noise voltages \( |V_{\text{diff.}d1}|^2, |V_{\text{diff.}d2}|^2, |V_{\text{diff.}r_{cg}}|^2, |V_{\text{diff.}r_{cs}}|^2 \) and \( |V_{\text{diff.}i_s}|^2 \) are derived as

\[ \frac{|V_{\text{diff.}d1}|^2}{|V_{\text{diff.}i_s}|^2} = \frac{T_{d1}g_{ds1}(R_{cg} - R_{cs}R_s^2g_m2)^2}{R_sT_0A_v^2}, \]  

(H.7)

\[ \frac{|V_{\text{diff.}d2}|^2}{|V_{\text{diff.}i_s}|^2} = \frac{T_{d2}g_{ds2}R_{cs}^2(1 + g_m1R_s)^2}{T_0R_sA_v^2}, \]  

(H.8)

\[ \frac{|V_{\text{diff.}r_{cg}}|^2}{|V_{\text{diff.}i_s}|^2} = \frac{R_{cg}(1 + g_m1R_s)^2}{R_sA_v^2}, \]  

(H.9)

\[ \frac{|V_{\text{diff.}r_{cs}}|^2}{|V_{\text{diff.}i_s}|^2} = \frac{R_{cs}(1 + g_m1R_s)^2}{R_sA_v^2}. \]  

(H.10)

The noise factor for the circuit considered would be defined as

\[ F = 1 + \frac{|V_{\text{diff.}d1}|^2}{|V_{\text{diff.}i_s}|^2} + \frac{|V_{\text{diff.}d2}|^2}{|V_{\text{diff.}i_s}|^2} + \frac{|V_{\text{diff.}r_{cg}}|^2}{|V_{\text{diff.}i_s}|^2} + \frac{|V_{\text{diff.}r_{cs}}|^2}{|V_{\text{diff.}i_s}|^2}. \]  

(H.11)
Substitution of (H.7), (H.8), (H.9), and (H.10) into (H.11) would give the following expression:

\[
F = 1 + \frac{T_{d1}g_{d1}(R_{cg} - R_{cs}R_{s}g_{m2})^2}{T_{0}R_{s}A_v^2} + \frac{T_{d2}g_{d2}R_{cs}^2(1 + g_{m1}R_{s})^2}{T_{0}R_{s}A_v^2} + \frac{R_{cg}(1 + g_{m1}R_{s})^2}{R_{s}A_v^2}
+ \frac{R_{cs}(1 + g_{m1}R_{s})^2}{R_{s}A_v^2}. \quad \text{(H.12)}
\]