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GaN Monolithic Microwave Integrated Amplifiers for Space and Wireless Applications

by

Ahmed Mohammed Elelimy Ramadan Abounemra

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

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Abstract

In modern communication systems, such as the fourth generation (4G) and fifth-generation (5G), the frequency spectrum needs to be fully utilized to support broadband applications and keep up with increasing user demand for high data rates. As an important component of the RF front-end in the transmitter, the power amplifier (PA) is used to convert the DC supply power into RF power. As the PA consumes most of the power in the transmitter, minimizing the power dissipation of the PA would have a significant effect on the efficiency of the whole transceiver. Doherty power amplifiers (DPAs) based on gallium nitride (GaN) transistors are poised to play a leading role in wireless base stations and repeaters in achieving high power efficiency and in meeting the linearity requirements set by wireless network standards. Although DPAs are widely utilized in field-deployed 4G base stations, they still suffer from many limitations. These limitations are mainly related to hardware imperfections in the RF blocks of the Doherty PA, such as narrow bandwidth and the gain imbalance between the main and the peak branches. Also, the large size of the circuit, because of the use of $\lambda/4$ transformers in the output combining network, is considered a critical problem for broadband DPA design.

To adequately overcome the limitations of the Doherty PA, a new design methodology for Doherty architecture based on three-port input and output networks topology is proposed in the first part of this thesis. The output three-port network performs the impedance matching from any load impedance to the optimum loads, for both main and peak transistors and combines the power delivered from the two devices at any power ratio. The input splitting network is proposed for matching the input impedances of the two transistors to the source impedance. The freedom in choosing the power division ratio of the input network, enables us to achieve a tradeoff between efficiency and linearity. An asymmetric two-stage broadband

Doherty amplifier is implemented using a 0.25-um GaN HEMT MMIC process to validate the proposed topology.

The second part of the thesis concerns the study and the design of a wide-band harmonic controlling network (HCN) based DPA, using a new output combining network to achieve higher power efficiency over the broadband operating frequency range. In this design, the frequency sensitivity of the impedance inverters was compensated to minimize the efficiency degradation across the designed bandwidth.

In many microwave systems, like radar and satellite applications, unwanted high input power levels such as jamming and interfering signals, affect LNAs. One of the characteristics of LNAs, designed using GaN technology, is the ability to endure these power levels with no need for using a limiter in front of the LNA. The third part of this dissertation presents a survivability study of wideband GaN HEMT LNA. It was concluded that GaN LNA can sustain relatively very high input power overdrive before device performance degradation or failure.

Keywords: Broadband Doherty power amplifier, harmonic controlling network (HCN), high efficiency, wide-band low noise amplifier, survivability.

Preface

This thesis is submitted to the Faculty of Graduate Studies in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering. It reports the work that I have conducted at the University of Calgary's Intelligent RF Radio Technology Laboratory (iRadio Lab) from January 2017 to December 2020. This thesis has been solely written by me and revised by my supervisor, Dr. Fadhel M. Ghannouchi. Most of the text in Chapters 3-5 is based on publications that have arisen from my research work. The following is a list of publications resulted from the work carried out for this thesis:

Journal Papers:

P1: **A. M. Elelimy Abounemra**, Wenhua Chen, Fei Huang, Mohammad Maktoomi, Mohamed Helaoui, and Fadhel M. Ghannouchi, "Systematic Design Methodology of Broadband Doherty Amplifier Using Unified Matching/Combining Networks with an Application to GaN MMIC Design", IEEE Access, DOI: 10.1109/ACCESS.2020.3046706, accepted, Dec. 14th, 2020**.**

P2: **A. M. Elelimy Abounemra**, Mohamed Helaoui, and Fadhel M. Ghannouchi, "A Systematic Topology for Efficiency Improvement of a Broadband Doherty Power Amplifier Using Harmonically Control Networks ", Submitted to IEEE Transactions on Industrial Electronics.

P3: **A. M. Elelimy Abounemra**, Mohamed Helaoui, and Fadhel M. Ghannouchi, "Analytical Design of a Robust MMIC Broadband Cascode Low Noise Amplifier Using RLC Feedback Network" **in preparation to be submitted to an IEEE Journal**.

P4: **A. M. Elelimy Abounemra**, Mohamed Helaoui, and Fadhel M. Ghannouchi, "Survivability Analysis of a Robust MMIC LNAs Under Gate Stress" **in preparation to be submitted to an IEEE Journal**.

Conference Papers:

P5: **A. M. Elelimy Abounemra**, Mohamed Helaoui, and Fadhel M. Ghannouchi, "A Highly Survivable C-band GaN HEMT LNA with Resistive Feedback Technique," *19th Mediterranean Microwave Symposium*,DOI:10.1109/MMS48040.2019.9157323, Oct. 2019.

P6: **A. M. Elelimy Abounemra**, Mohamed Helaoui, and Fadhel M. Ghannouchi, "A High Gain and High Linear 0.25μm GaN HEMT Based Monolithic Integrated C-band Low Noise Amplifier," *IEEE International Electromagnetics and Antenna Conference (IEMANTENNA)*, DOI: 10.1109/IEMANTENNA.2019.8928801, Oct. 2019.

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Finally, this work would not have been possible without the never-ending love of my beloved family; my parents, my patient wife, my inspiring children Fatima, Habiba, and Maryam. I love you all so much!

To my parents

To my wife

And to my lovely Fatma, Habiba, and

Maryam.

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List of Symbols, Abbreviations, and Nomenclature

5G	Fifth Generation
Symbol	Definition
MIMO	Multiple Input Multiple Output
SISO	Single Input Single Output
PA	Power Amplifier
CMOS	Complementary Metal Oxide Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
OPBO	Output Power Back Off
PAPR	Peak to Average Power Ratio
PAE	Power Added Efficiency
HEMT	High Electron Mobility Transistor
CCA	Current Conduction Angle
VCCS	Voltage Controlled Current Source
ZVS	Zero-voltage Switching
ZVDS	Zero-voltage Derivative Switching
ET	Envelope Tracking
DPA	Doherty Power Amplifier
DE	Drain Efficiency
LNA	Low Noise Amplifier
CS	Common Source
CG	Common Gate
FET	Field Effect Transistor
IIN	Impedance Inverting Network
OMCN	Output Matching Combining Network
IMSN	Input Matching Splitting Network
LTE	Long Term Evolution
ACPR	Adjacent Channel Power Ratio
DPD	Digital Predistortion
LMN	Load Modulation Network
HCN	Harmonic Controlling Network
SHIIC	Second Harmonic Impedance Inverter Network
THSN	Third Harmonic Suppression Network
FTCS	Frequency Tuned Coupling Structure
PMTN	Post-Matching Tuning Network
GaN	Gallium Nitride
GaAs	Gallium Arsenide
CW	Continuous Wave
MAG	Maximum Available Gain
MSG	Maximum Stable Gain
OIP3	Output Third-Order Intercept Point
UMS	United Monolithic Semiconductors
SRF	Self-Resonance Frequency

Chapter 1 Introduction

1.1. Motivation

Recently, the evolution of the wireless communication systems from 4G to 5G networks has accelerated significantly, opening the door to many opportunities for scientific research. The 5G networks are destined to become the core of future commercial communications and infrastructure applications. The 5G for wireless communication is expected to deliver services to about 150 million subscribers by 2021 [1].

In 5G wireless networks, massive multiple-input multiple-output (MIMO) systems play a significant role because they achieve higher data rates than the single-input, single-output (SISO) systems. This improvement in the data rate will require more complex modulation schemes, and also, larger instantaneous signal bandwidths (more than 200 MHz) [2]. These challenges will drive the demand for small, efficient, and cost-effective power amplifiers (PAs) that can be integrated with 64-, or even 128-elements MIMO active array antennas for wireless base station applications or even with 5G handheld devices. One solution is to use integrated technologies such as the complementary metal oxide semiconductor (CMOS) and monolithic microwave integrated circuit (MMIC), which offer high reliability, excellent repeatability, high yield, as well as, low cost. With the development of advanced wireless communication networks, it is highly desirable to operate across multiple standards using different frequency bands that can be handled by a single radio operating over a wide frequency band. Also, the complexity of the modulation schemes used in 5G networks will require efficient power amplifiers and must remain highly efficient at output power back-off (OPBO).

For PA design, several strategies can allow the achievement of efficiency enhancement at the output power back-off region, such as bias modulation, out-phasing technique, and envelope

tracking technique. Among these topologies, DPA is one of the most well-established methods used in commercial base stations for its ability to achieve a high peak-to-average power ratio (PAPR). Most of the DPA designs focus on fundamental load tuning. However, the harmonic load terminations have a great effect on the power efficiency performance. Thus, by controlling the harmonic load terminations, along with tuning the fundamental load, enhancement of the efficiency can be achieved.

For LNA design, the low power handling capabilities of GaAs and InP technologies requires the integration of a limiting circuit at the LNA input, which results in higher NF. GaN HEMT technology has been considered a promising technology for radar, electronic countermeasure (ECM), and wireless communication applications. This interest in GaN technology is due to its properties, like higher operating channel temperature and high breakdown voltage. Moreover, the high cut-off frequency of GaN technology is ideal for wideband applications [3]. LNA that has been designed and fabricated using GaN technology can survive under very high power levels, without using an input limiter which adds more noise to the receiver chain.

1.2. Objectives

The main objectives of this thesis are to develop innovative theories and methodologies for high-efficiency DPA designs, along with bandwidth extension and/or efficiency enhancement techniques. In addition, the thesis explores the development of methodologies for designing wideband LNAs with improved noise figure, high reliability, and robustness against high-level input drives.

1) *Design of broadband MMIC DPA.* Due to the ever-increasing data capabilities and complex modulation schemes in 5G applications, compact PAs that can handle large

PAPR up to 10 dB are required. Despite the abundance of design challenges of a high power MMIC broadband Doherty amplifier, it warrants the attention of researchers to devise cost-effective and high performing architectures and topologies that can be suitable for wireless base stations and handheld terminals. Furthermore, it can be used as a building block for an active massive MIMO transmitter.

2) *Design of high-efficiency DPA with bandwidth extension.* Although the conventional DPAs can be extended into broadband DPAs with the continuous-mode technique, only one harmonic load termination can be tuned independently. The other harmonic load terminations must be fixed to a specific reflective load. In this thesis, both the second and the third harmonics have been considered and manipulated to obtain enhanced efficiency, while broadening the design space for a more comprehensive operational bandwidth.

3) *Design of high-reliability broadband LNAs.* Due to the high breakdown voltage of the GaN HEMT, the device can survive in severe RF environments and, by applying high input powers, without the need for any additional protection circuitry. Furthermore, as a result of this inherent robustness of the device, the low noise amplifiers (LNAs), designed using GaN technology, can endure higher power levels without using an input limiter and, hence, degrading the noise figure of the receiver chain. Basically, with this ruggedness, one can eliminate the limiter in front of the LNA, which reduces losses and, therefore, improves the overall noise figure and also improves the reliability of the RF front-end.

1.3. Research methodologies and contributions

To reach the thesis objectives, several theories and methods are presented in this dissertation. They are summarized as follows:

1) Three-port DPA. An adopted analysis and a stream out design methodology of the three-port input and output networks are developed and adopted throughout this thesis to enhance the bandwidth of the Doherty amplifier design and reduce its size to make it appropriate for MMIC implementation. Also, for the first time, the implementation of the three-port matching and combining networks topology was realized, based on MMIC technology to fulfill the integration requirements. Since the designed DPA is composed of two cascaded stages and involves five transistors, 1600-time post-layout Monte Carlo simulations, with the consideration of both the mismatch and process variations, were carried out to investigate the robustness of the proposed technique.

2) *Harmonically tuned Doherty power amplifier with extended bandwidth*. Narrow bandwidth is a significant problem for conventional DPAs due to the presence of device output capacitance (C_{ds}) and a high impedance transformation ratio of the quarter-wavelength impedance inverter, the drain efficiency (DE) at the OBO region degrades away from the center frequency. To address this issue, a systematic topology for efficiency enhancement for a broadband DPA, based on an output harmonic control network associated with post-matching topology, was investigated. This topology ensures that the main and auxiliary optimum load impedances are maintained for the transistor's output. By manipulating the harmonic impedances as seen by the transistors in the DPA, the bandwidth and efficiency enhancement can be achieved.

3) *Highly rugged LNAs.* One of the essential aspects of GaN LNA is its ability to afford substantial RF input power. One of the contributions of this work is to design LNAs based on different topologies and assess the circuit's performance under overdrive input power. Along with the design of a rugged LNA, a systematic testing methodology to assess the performance of the LNA under stress, in terms of recoverable and non-recoverable performance degradation, is proposed. The fabricated GaN MMIC LNA was tested with high over-drive input power levels.
4) *Ultra-wideband LNA.* To achieve this objective, the LNA is designed based on cascode topology with a series inductive source, and using an RLC frequency-dependent feedback network. The RLC frequency-dependent feedback network in this configuration is used to achieve the required broadband frequency operation. It is designed to obtain excellent wideband frequency response with a flat gain over the frequency range from 2 to 11 GHz.

1.4. Thesis Outline

This dissertation is composed of several chapters as described in the following:

Chapter 2 gives a brief introduction of different power amplifier design techniques and topologies, and low noise amplifier topologies.

Chapter 3 illustrates the research work on the broadband MMIC DPA using unified matching-combining networks. This work includes a review of the conventional DPA principle, the theory of the three-port topology, and the generic design methodology of the proposed DPA.

Chapter 4 proposes a topology suitable for the design of harmonically tuned broadband DPA. The systematic analytical topology of a new harmonic controlling network is presented in

this chapter. The design procedure of the broadband DPA is illustrated in detail. The simulated and measured results are discussed and analyzed.

Chapter 5 presents the designs of a robust broadband LNA based on different topologies. The overdrive test was performed on the single-stage LNAs to check their ruggedness. Also, in this chapter, a new design analysis of an UWB LNA was studied theoretically and verified. Simulated and measured results are presented and discussed for each design.

Chapter 6 gives the conclusion and contributions of this research work.

Chapter 2 Architectures of front-end modules

2.1. Introduction

Most of today's GaAs MMIC PAs in T/R modules have output power levels in the range of 5 W to 10 W. To meet the future requirements for wireless and satellite communications using highly varying envelop signals and complex modulation schemes, higher output power levels, and increased power added efficiency (PAE), which are prime design parameters for such systems. The higher breakdown voltage of GaN, compared to GaAs, enables GaN devices to handle very high powers and makes GaN devices very promising for these applications [4]. Another important consideration for these T/R modules is the input power survivability for the low noise amplifiers (LNA), besides its noise factor (NF). The LNA's receiver is subject to high to power input signals (1-5 W) that might result from unwanted blockers and interferers, as well as, leakage from the high power amplifier (PA), due to limited isolation between the transmit and receive paths in the T/R module. These high-power input signals may permanently damage the LNA and the full receiver chain if not protected adequately. A widely used method to protect against these aggressors is to use high-power limiter PIN diodes in front of the GaAs LNA. However, this limiter can increase the NF of the receiver path, and generally, it cannot be integrated into the same substrate, which increases the system size and cost.

2.2. Power amplifier

The power amplifier is a critical component of any microwave transmission system. The performance of the power amplifier module has a significant impact on the final system architecture. Its role is to magnify the power of the transmitted signal, without adding undesirable distortion signals generated by the non-linearity of PAs. Simultaneously, the power amplifier should be efficient in terms of its capability to convert the DC supply power into RF power.

2.2.1. Operating conditions of power amplifiers

The power amplifier classification is based on classes of their operation, which refers to several features. This includes selecting a quiescent (Q) biasing point and current conduction angle (CCA) θ, which is defined as the fraction of the RF signal period, where a non-zero current is flowing through the device. The PA's classes are Class-A, AB, B, and C, related to the Q biasing point and CCA. Another classification is related to the device dynamic operating conditions [6].

An alternative PA classification is related to the device dynamic operating conditions, and consequently, matching network terminations. In this classification, three categories are identified: the current-mode, switching-mode, and the waveform engineered PAs. In these modes, the active device behaves as a voltage-controlled current source (VCCS), whereas the switch-mode PAs use the device output capacitance to perform a current switching behavior. Waveform engineered PAs use the harmonic terminations to shape the drain voltage and current waveform to maximize output power and efficiency [7].

2.2.1.1. Linear mode power amplifiers

In the linear mode, the active device is conducting at the full cycle of the input sinusoidal signal. The Q biasing point is selected at the center of the device current (I) and voltage (V) domain, such that the transistor is biased halfway between the turn-on (V_T) and cut-off point [8].

The input-output characteristic of the transistor is modeled as follow [7]:

$$i_{ds} = \begin{cases} 0 & v_{gs} \leq V_p \\ g_m(v_{gs} - V_p) & v_{gs} \geq V_p \end{cases} \tag{2-1}$$

where g_m is the transconductance of the transistor.

When the input voltage is larger than the pinch-off voltage V_p, the current starts following through the transistor. Figure 2-1 shows the input voltage and output current waveforms when the transistor is driven by a sinusoidal signal under the given biasing condition as:

$$v_{in} = V_b + V_m \cos(\omega t) \tag{2-2}$$

where V_b is the gate dc bias voltage, and V_m is the magnitude of the sinusoidal signal.

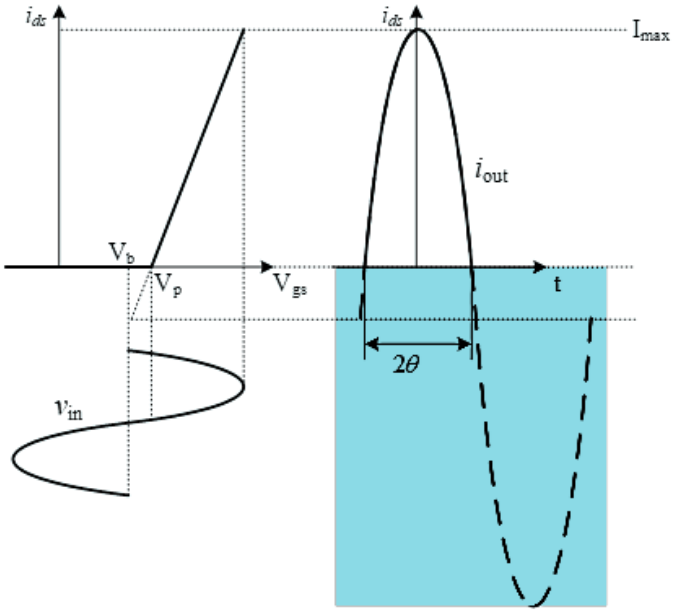

Figure 2-1 Input voltage and output current waveforms

The output current i_{out} only exists during the conduction angle 2θ, which can be represented as:

$$i_{out} = \begin{cases} 0 & \theta \leq \omega t \leq 2\pi - \theta \\ g_m V_m(\cos(\omega t) - \cos\theta) & -\theta \leq \omega t \leq 2\pi \end{cases} \tag{2-3}$$

where,

$$\theta = arccos\left(\frac{V_b - V_p}{V_m}\right) \tag{2-4}$$

The conduction angle and the load topology identify the operation classes of the power amplifier as shown in Figure 2-2.

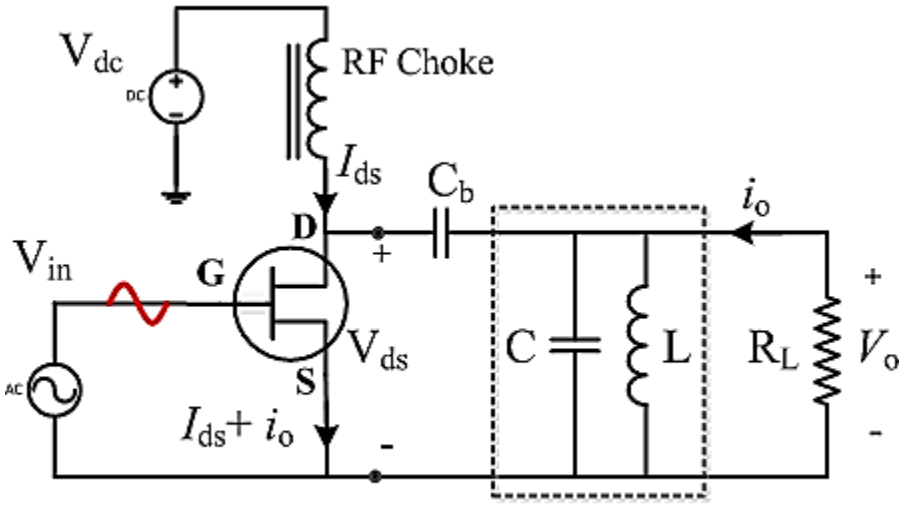

Figure 2-2 Circuit topology of the power amplifier

When conduction angle $\theta = \pi$, the output current is expressed as:

$$i_{out} = g_m V_m (1 + \cos \omega t) \tag{2-5}$$

Such voltage and current waveforms determine an operation class, Class-A. The drain efficiency can be calculated as:

$$\eta = 1 - \frac{\int_{\omega t=0}^{\omega t=2\pi} v_{out} i_{out} d\omega t}{g_m V_m V_{CC}} = \frac{1}{2} \frac{V_R}{V_{CC}} \tag{2-6}$$

When the magnitude V_R is equal to dc supply voltage V_{CC}, the efficiency of Class-A reaches the maximum value of 50%.

2.2.1.2. Waveform engineered power amplifiers with harmonic controlling

In a more advanced mode of operation, the harmonics can be manipulated in such a way to shape the drain voltage/current waveforms. This technique is called waveform engineering [9]. Only the manipulation of the second and third harmonics are considered to reduce the circuit complexity in high RF and microwave applications. Another reason is that, above the third

harmonic, the active device's output capacitance will effectively short higher harmonics [6]. In general, the efficiency of a harmonic-tuned power amplifier is expressed as:

$$\eta = \frac{P_{out,f_o}}{P_{diss}+P_{out,f_o}+P_{out,2f_o}+P_{out,3f_o}} \quad (2\text{-}7)$$

The power amplifier efficiency can be optimized by maximizing the fundamental output power, and by minimizing the dissipated power, and the second and third harmonics powers. This can be achieved by using appropriate harmonic loading conditions to tune the harmonics, such that the harmonic components are added to the fundamental signal in the correct phases to properly shape the current and voltage waveforms.

One of the most common waveforms' engineered power amplifiers is Class-F/F^{-1} PAs. They are designed like Class-AB/B PAs, except that multiple resonators are integrated with the output matching network to control the second and third harmonics and shape the drain voltage/current waveforms [6]. Ideally, for Class-F PAs, all even harmonics are short-circuited to reproduce a half sine-wave current waveform, while the odd harmonics are open-circuited to shape the output voltage to a square wave, thus reducing the overlap between the current and voltage waveforms.

One of the significant differences between Class-B and Class-F PAs, is that Class-B current waveform does not have odd harmonics. These odd harmonics are generated in Class-F PA as a result of the overdriven condition [7]. In this situation, the load-line hits the knee region because of the high-level input power. The circuit diagram of Class-F topology is shown in Figure 2-3 [6]. The L_3 - C_3 resonator provides an open circuit at the third harmonic frequency and, combined with L_1 - C_1 resonator, achieves a short-termination to the 2nd harmonic. Figure 2-4 depicts the drain voltage and current waveforms of Class-F PA.

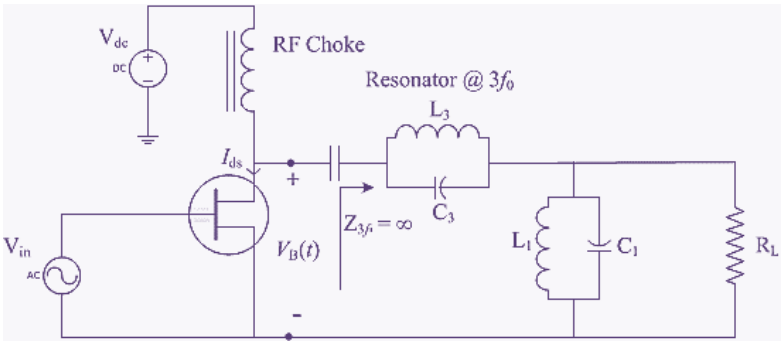

Figure 2-3 Circuit topology of Class-F PA

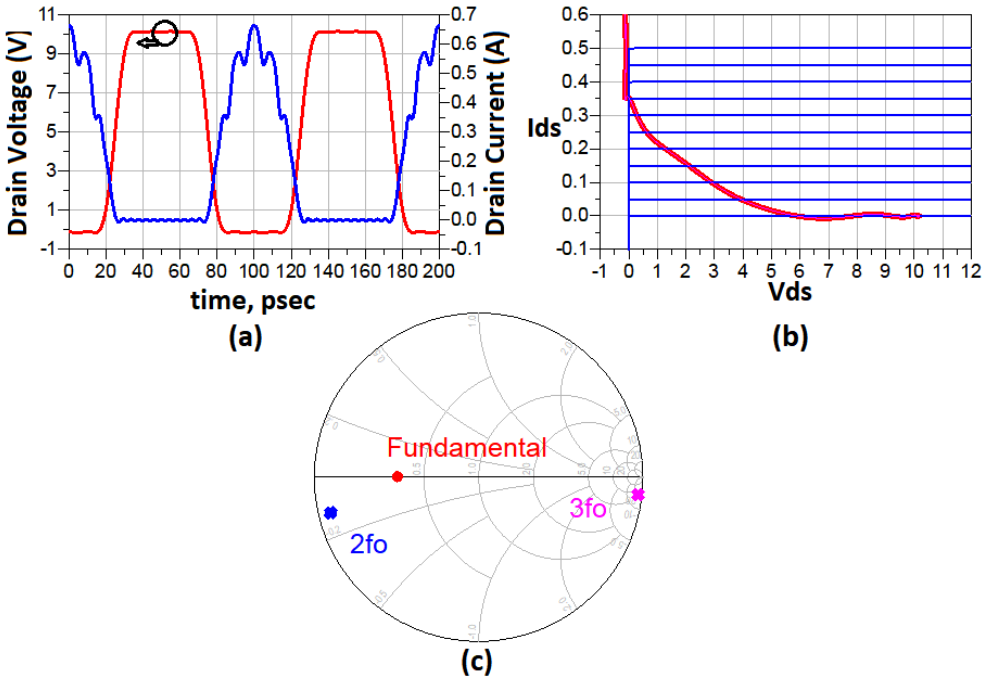

Figure 2-4 Class-F PA (a) waveforms, (b) load-line, and (c) fundamental and harmonic impedances

2.2.1.3. Switched-mode power amplifiers

The transistor operates as a switch in this operation mode [8] and has a very low ON resistance and very high OFF resistance. In such a case, the voltage and current waveforms at the device output show a 180◦ phase shift. If the ON-state resistance is negligible, no power is dissipated in the device; similarly, if the OFF resistance is very high, no current will flow through

it. Theoretically, an ideal switching PA can achieve 100% drain efficiency. Class-D is defined when the load is purely resistive. In Class-D PAs, the even harmonics are short-circuited, and the odd harmonics are open-circuited. Practically, the transistor has a finite ON resistance, and there is a significant transition time from the ON to the OFF state, which leads to reduced efficiency.

To reduce the harmonic dissipated energy in the resistive load, a Class-E is proposed as shown in Figure 2-5. A Class-E PA has a high Q tuned circuit at the device's output to provide reactive load at the fundamental frequency and open termination at the second and third harmonics. All the harmonic energy is stored in the shunt capacitor C. Two special conditions, zero voltage switching (ZVS) and zero derivative voltage switching (ZDVS) are assumed as shown in the following:

$$v(\omega t)\big|_{\omega t=2\pi} = 0 \tag{2-8}$$

$$\frac{dv(\omega t)}{d\omega t}\Big|_{\omega t=2\pi} = 0 \tag{2-9}$$

The voltage and current waveforms are obtained at these conditions as shown in Figure 2-6. The theoretical efficiency of the Class-E is 100%, as all the dc energy is converted to fundamental frequency energy. The components' values can be calculated as:

$$C = \frac{I_0}{V_0}\frac{1}{2\pi^2 f_0} \tag{2-10}$$

$$R = \frac{V_0}{I_0}\frac{8}{\pi^2 + 4} \tag{2-11}$$

$$L = \frac{V_0}{I_0}\frac{\pi^2 - 4}{\pi^2 + 4}\frac{1}{4 f_0} \tag{2-12}$$

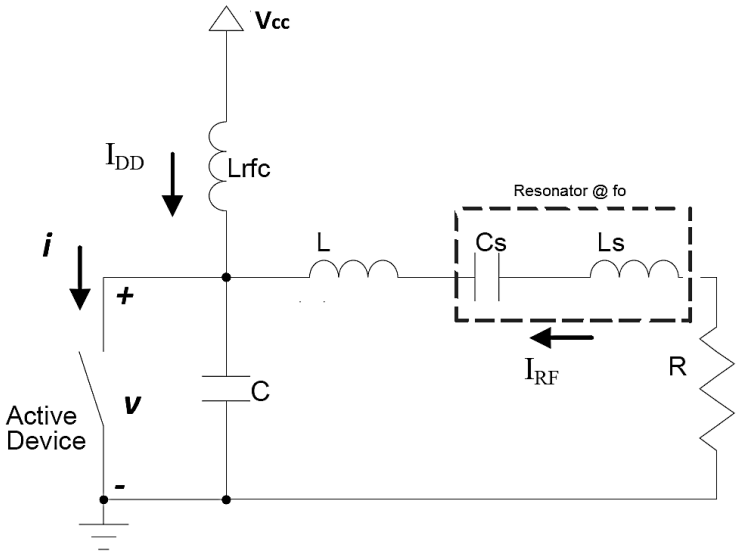

Figure 2-5 Circuit topology of Class-E PA

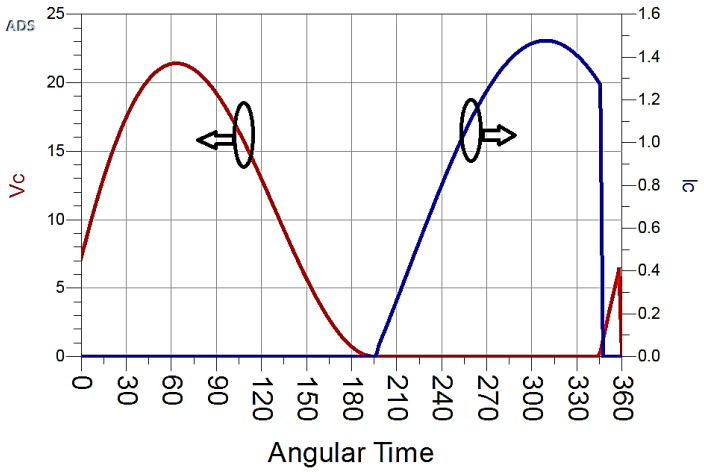

Figure 2-6 Voltage and current waveforms for Class-E circuit

2.2.1.4. Continuous mode power amplifiers

The concept of the continuous mode PA was first proposed by S. Cripps [9]. The new PA mode of operation, namely the Class-J, assumes some voltage waveforms, which, when combined with the baseline half sine-wave current waveform, results in the same overall power and

efficiency of Class-B PA. These voltage waveforms correspond to different fundamental and second harmonic load impedances.

Unlike the Class-B PA, a Class-J PA allows for a wide range of second harmonic reactive components, but simultaneously, requires a paired reactive component at the fundamental to keep the voltage waveform above zero, as shown in Figure 2-7. The mathematical analysis of the Class-J PA is presented in [9].

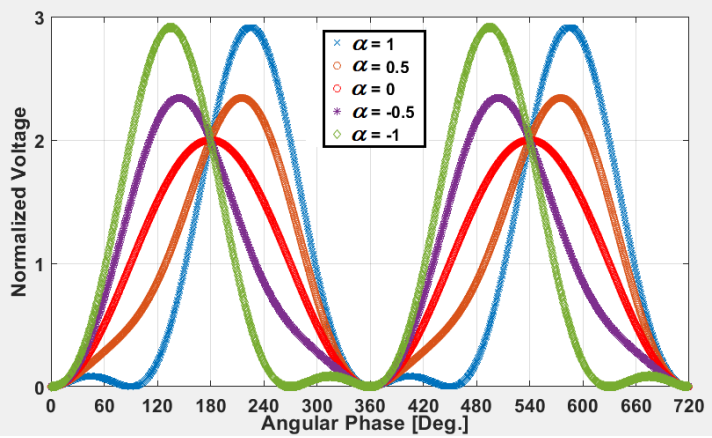

Figure 2-7 Class-J PA voltage waveforms

More recent work by S. Cripps has introduced a much broader design space for Class-F PAs, namely the continuous Class-F [10]. The concept is extended in [11]. This operation mode provides the ability to design high-efficiency broadband PAs, resulting in an over-octave in bandwidth (BW) [12]. The key to engineering this new PA mode lies in changing the reactive component of the fundamental load, while varying the phase of the second harmonic impedance as in (2-13).

$$V(\omega t) = (1 - \gamma \sin \omega t)\left(1 + \frac{1}{\sqrt{3}}\cos \omega t\right)\left(1 - \frac{2}{\sqrt{3}}\cos \omega t\right)^2 \qquad (2\text{-}13)$$

A set of voltage and current waveforms can be generated by following this method, which coincides with the conventional Class-F requirements. The required impedances are shown in Figure 2-8, with γ changing from (-1 to 1), to generate a second harmonic reactance that varies around the Smith chart's edge, while the fundamental impedance varies on a circle of constant resistance.

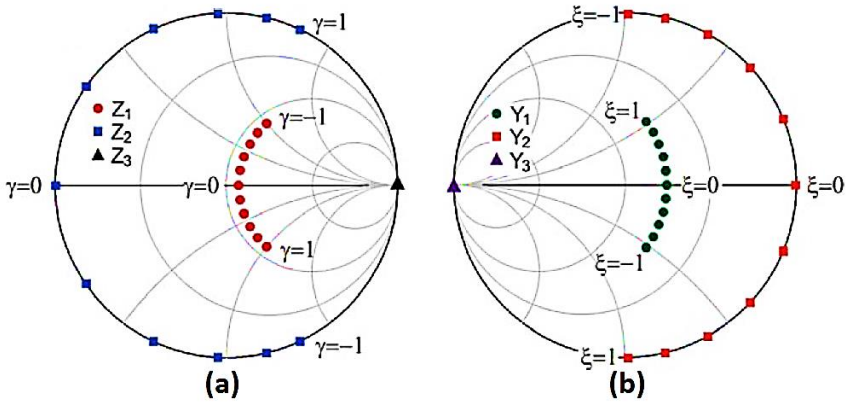

Figure 2-8 Fundamental and harmonic loading conditions: (a) continuous Class-F PA, and (b) continuous Class-F^{-1} PA

2.2.2. Efficiency enhancement techniques of power amplifiers

Different techniques are used to maintain the maximum efficiency at output power back-off levels (OPBO). First, preserving the optimum load impedance over the entire power range enables enhancement in the power amplifier's efficiency; the variation of the drain supply voltage as a function of the input drive level is used to perform the same role. The load impedance seen by the transistor is modulated to maintain the maximum voltage swing and efficiency. Correspondingly, various techniques are proposed in the literature to enhance PA's efficiency over a range of output power back off (OPBO) levels. These techniques can be classified into three

main categories: drain supply modulation techniques, current biasing techniques, and load modulation techniques, as shown in Figure 2-9 [13].

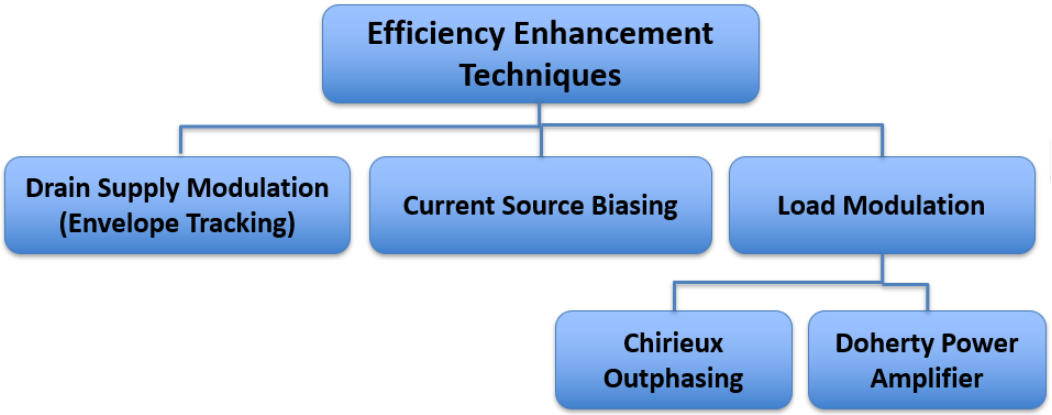

Figure 2-9 Efficiency enhancement techniques

2.2.2.1. Envelope Tracking (ET)

The envelope tracking PA consists of three main components: the envelope detector, envelope amplifier (modulator), and a linear RF PA [14], as shown in Figure 2-10. The envelope detector follows the input signal amplitude and passes it to the envelope amplifier, magnifying the signal and transferring it to the drain of the PA, as depicted in Figure 2-11.

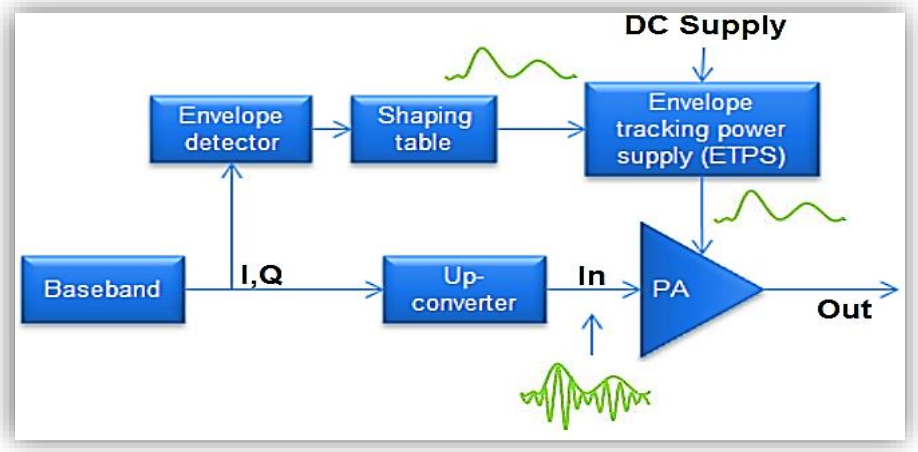

Figure 2-10 Block diagram of the envelope tracking PA

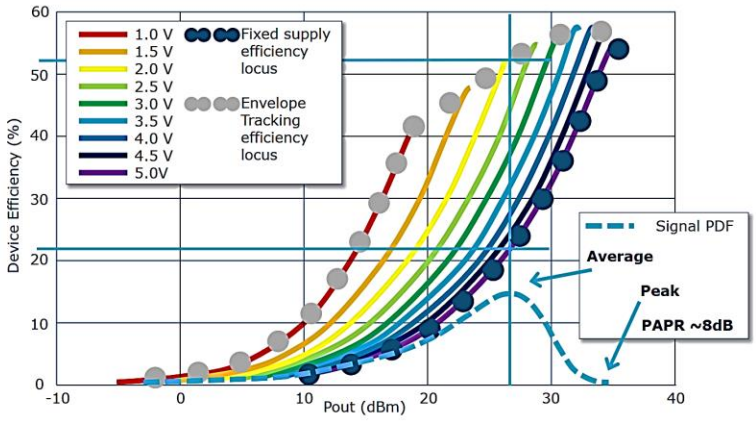

Figure 2-11 The envelope tracking PA efficiency enhancement concept

On the other hand, one of the drawbacks of the ET technique is that the bandwidth and efficiency of the envelope amplifier are very limiting factors; the system's overall efficiency is highly dependent on the efficiency of the envelope amplifier [15]. The efficiency of an ET PA is lower at a higher envelope power than that of the conventional PAs, with constant supply voltage due to the envelope modulator's inefficiency.

2.2.2.2. Current source biasing technique

In this technique, a constant current biasing topology scheme is proposed for the main transistor of the two branches [16]. By using the current biasing scheme, the transistor presents completely different behaviors, compared to the conventional voltage biasing scheme. One of these behaviors is reversed load modulation. Due to this behavior, the power amplifier can be implemented to obtain a broadband extended high efficiency at power back-off without using the impedance inverters at the output network. The structure of the current biased technique is shown in Figure 2-12, while the simulation results are shown in Figure 2-13.

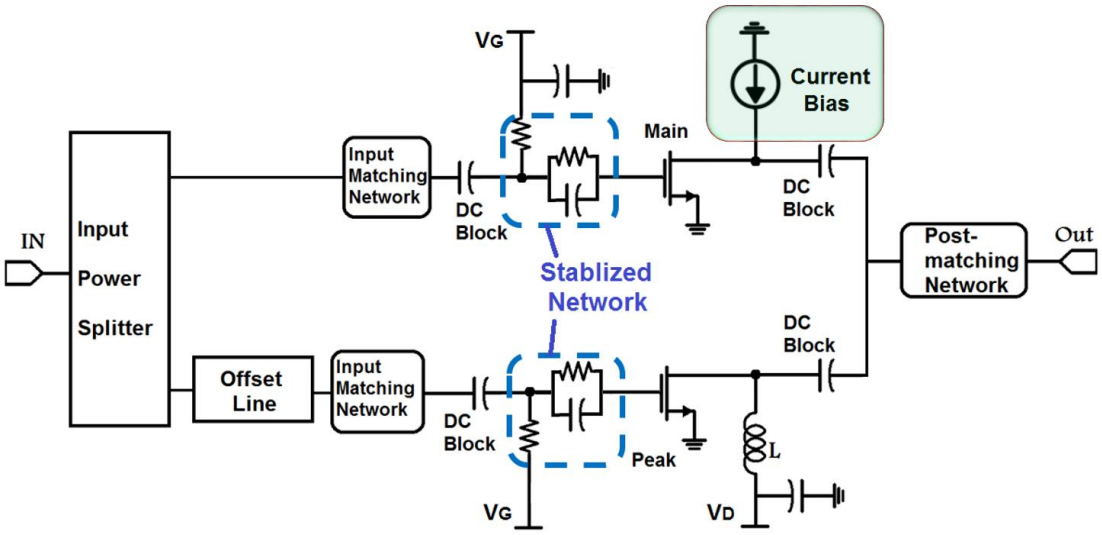

Figure 2-12 Block diagram of the power amplifier based on current source biasing topology

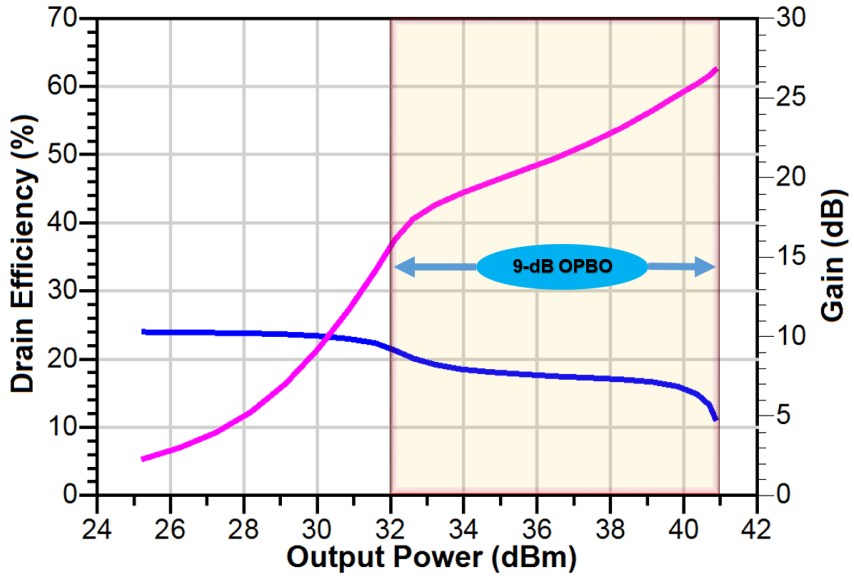

Figure 2-13 The drain efficiency and gain simulation results

2.2.2.3. Chireix outphasing technique

The concept of the outphasing PA was first introduced by Chireix in the 1930s to improve the efficiency and linearity of AM broadcast transmitters [17]. This invention's primary purpose

was to resolve the isolating combiner drawbacks in the LINC transmitters, mainly to add up the outphasing signals. Chireix introduced a non-isolating combiner design, resulting in improved average efficiency, as shown in Figure 2-14.

Outphasing architectures provide high operating efficiency over a wide range of output power levels [18]. The major limitation in the outphasing approach is the need for signal component separation of the desired RF signal into multiple phase amplitude-modulated signals driving the branch PAs.

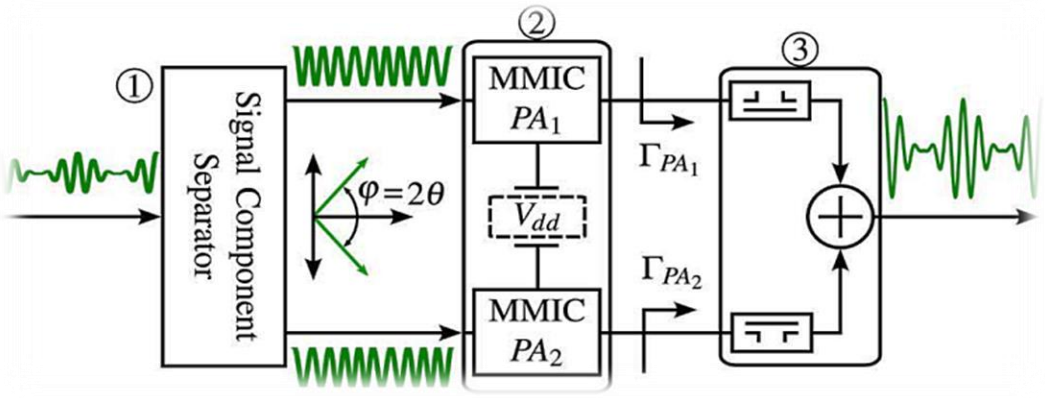

Figure 2-14 Schematic diagram of the outphasing PA

2.2.2.4. Doherty power amplifier

The concept of a conventional Doherty power amplifier (DPA) has been discussed in many previous works [19-22]. In a Doherty PA, the main device conducts at a low power level, up to a preselected average power level, while the auxiliary device conducts when the power surpasses the preselected power level, which is often fixed at 6-dB OPBO. The impedance modulation in DPA is enacted using λ/4 transformers [20]. In the conventional Doherty amplifier design shown in Figure 2-15, the matching networks of the main and auxiliary amplifiers are usually designed separately from the input-splitting and output-combining networks.

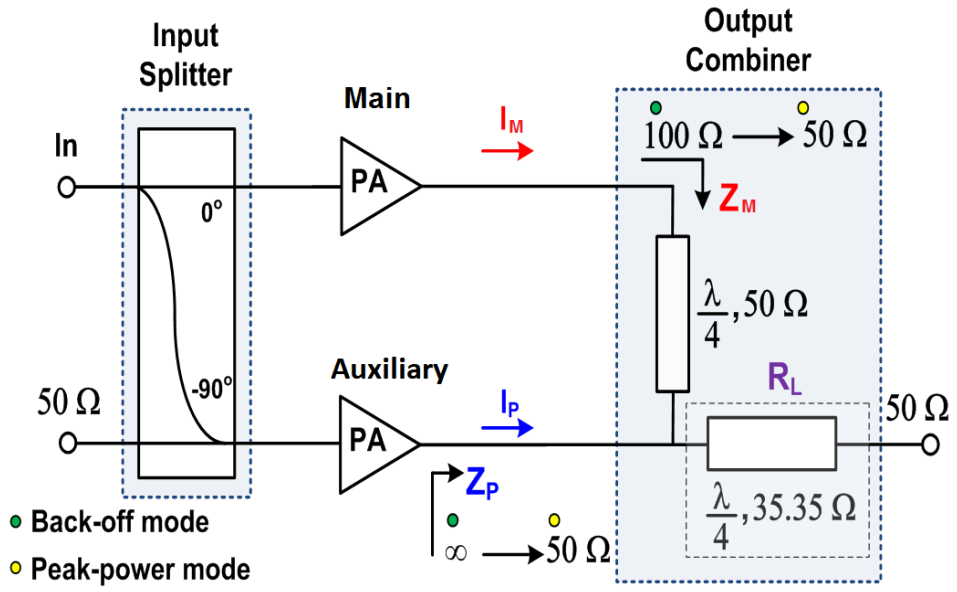

Figure 2-15 Conventional Doherty power amplifier architecture

The drain efficiency (η) of an ideal DPA in which the main amplifier is biased at Class-B is given by [23].

$$\eta = \begin{cases} \frac{\pi}{2} \times 10^{\frac{OPBO}{20}} & OPBO \leq -6 \\ \frac{\pi}{4} \times \left(\frac{10^{\frac{OPBO}{10}}}{1.5 \times 10^{\frac{OPBO}{20}} - 0.5} \right) & -6 \leq OPBO \leq 0 \end{cases} \tag{2-14}$$

Figure 2-16 shows the theoretical efficiency curve of a Class-B based Doherty PA and that of a balanced Class-B PA. The Doherty PA has higher efficiency at output power back-off levels, which is highly desirable to fulfill the requirements of the communication systems with high peak to average power ratio (PAPR) signal.

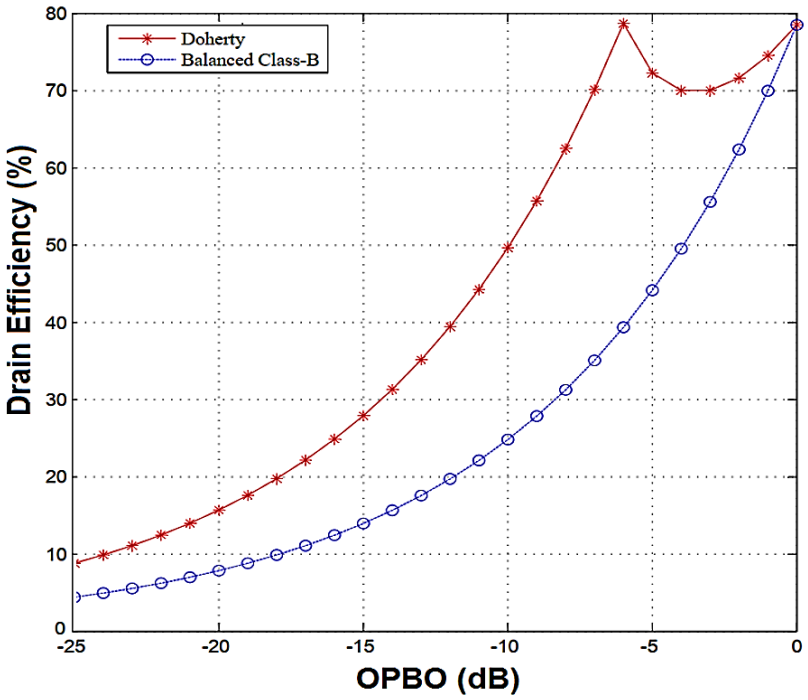

Figure 2-16 The drain efficiency of Doherty and class-B balanced PAs

2.3. Low noise amplifier

Low noise amplifiers (LNA) are the first stage in the RF front-end receiver system. The LNA's primary purpose is to amplify the desired signal received from the antenna with minimum degradation of the signal-to-noise ratio. Thus, a LNA is an essential component in the receiver chain, because its noise performance directly dominates the noise performance of the receiver chain. LNA design considerations are low noise figure, good input-output matching performance, operating frequency range, stability, and linearity.

2.3.1. Low noise amplifier topologies

Most LNA topologies are single-ended, the use of differential LNAs being limited by performance impairments. The main difficulty in the differential LNA's design is accomplishing a very low common-mode rejection ratio (CMRR) [24]. They also have drawbacks, like consuming

a lot of power, having higher NF, and requiring more chip area than single-ended LNAs. The NF of LNAs is better for single-ended devices than for differential devices [25].

2.3.1.1. Common source low noise amplifier

The common source (CS) topology is the most common LNA topology in use. It includes a single transistor whose source is grounded which results in a high current gain, high input impedance, and low output impedance. Common source LNA has high gain and good noise performance, compared to common gate topology (CG). Due to Miller effect, the bandwidth of the amplifier tends to be low [26]. A common source configuration may be used in wideband applications, using appropriate feedback or matching circuits [27]. Also, because the common source amplifier includes one transistor compared to cascode topology, as shown in Figure 2-17, it occupies less space on the chip and has a smaller noise figure.

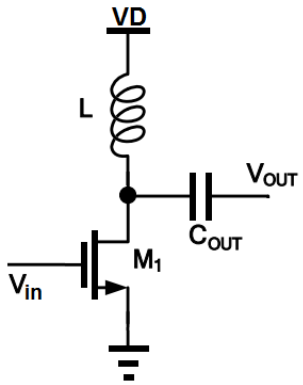

Figure 2-17 Common source LNA topology

2.3.1.2. Common gate low noise amplifier

In common-gate amplifier topology, the input signal is applied to the transistor source, and output is taken from the drain port, as shown in Figure 2-18. Wideband input matching is possible for common gate configuration, and, hence, this configuration is widely used in broadband LNA

circuits [28]. Common-gate low noise amplifiers achieve a broadband impedance match, superior reverse isolation, and stability due to the absence of Miller effect. Common gate feedback amplifiers aim at decoupling the noise and power (input) match trade-off, without degrading other relevant LNA parameters.

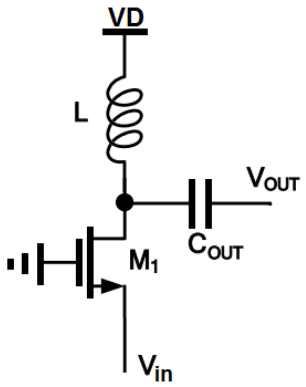

Figure 2-18 Common gate LNA topology

2.3.1.3. Cascode low noise amplifier

The cascode LNA topology is shown in Figure 2-19. Using this topology has many benefits, like improving the LNA's voltage gain and output impedance [29]. The gate-drain capacitive feedback between the output and the input was canceled, resulting from the common-gate configuration of the second transistor. So, due to Miller effect elimination, much higher bandwidth can be achieved. However, in this topology, the supply voltage is relatively high, and the second transistor impairs the LNA's noise performance [30].

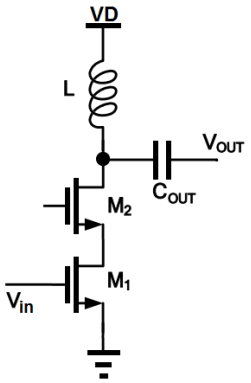

Figure 2-19 Cascode LNA topology

2.3.1.4. A common source topology with resistive feedback

Using the feedback topology, the LNA can achieve a wideband matching, low power consumption, and high gain. As compared to the other topologies, a smaller chip area can be obtained by using a feedback LNA configuration, since fewer inductors are usually needed. A simplified circuit of the common-source amplifier with a feedback network is illustrated in Figure 2-20.

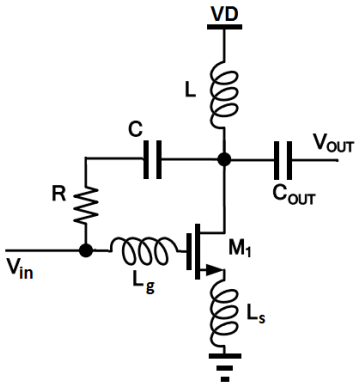

Figure 2-20 Common source topology with a feedback network

Chapter 3 MMIC broadband Doherty power amplifier using unified matching/combining networks

3.1.Introduction

Different techniques were studied previously to improve the performance of the DPA by broadening the operating bandwidth and extending the efficiency range. In [31], [32], the efficiency performance was improved over a wide power range by using a digitally controlled input power scheme, which minimizes the power waste into the peaking branch at the back-off power levels. The bandwidth limitation was mitigated in the Doherty region by using different optimized characteristic impedances for λ/4 transformers at the output combiners as in [33]-[36]. In [37] and [38] a modified power combining network with an L-C tank and compensating reactance C-R was used, respectively, to maintain the back-off impedance seen by the main transistor over a frequency band to obtain a higher bandwidth.

The frequency response of the output-combining network of the Doherty amplifier with an arbitrary back-off level configuration was reported in [39]-[41]. Furthermore, post-matching networks were employed in [42]-[44] to achieve improved bandwidth and efficiency. In [45], an asymmetric GaN MMIC Doherty PA was designed using a reversed uneven power splitting network to improve the linearity performance, and it included a two-section λ/4 transformer to obtain a uniform frequency response. Since the main obstacles in obtaining a DPA, with wideband performance, are the use of output impedance inverters and offset lines, a transformer-less load-modulation network was reported in [46], which resulted in a wideband DPA. A single RF-input modified MMIC Doherty amplifier, with reconfigurable efficiency, was proposed in [47], showing the effect of the input network and the bias voltages on the amplifier frequency response.

Most of the studies rely on discrete GaN devices to design high power Doherty PAs and only a few of them use MMIC technology. Despite the abundance of challenges and difficulties in designing a high power MMIC Doherty amplifier, it deserves a great deal of research attention as it can help fulfill the requirements of small-cell base stations. Furthermore, it can be used as a building block for an active MIMO transmitter. An alternative Doherty design topology was reported in [48], which examined the performance of the three-port matching and combining networks. Inspired by [48], an adopted analysis and a stream out design methodology of the three-port input and output networks were developed and adopted throughout this chapter to enhance the bandwidth of the Doherty amplifier design and reduce its size to make it appropriate for MMIC implementation. Also, for the first time, the implementation of the three-port matching and combining networks topology was realized based on MMIC technology to fulfill the integration requirements.

In this chapter, a compact GaN MMIC two-stage DPA design based on a new and comprehensive design methodology suitable for MMIC design is presented. This methodology was employed to optimize the DPA behavior, not only for performance such as efficiency, back-off range, and frequency bandwidths, but also to optimize MMIC design constraints such as circuit size, the process variability, and limitations. The three-port technique has been used to synthesize the DPA matching and splitting input/output networks. A detailed procedure of the broadband Doherty design is given in the paper. Consideration is given to the degree of freedom for implementation of the networks, which provides high flexibility to the design of input/output networks with minimal sensitivity to the process variation, and broadband frequency response. Also, we sought a compact size that would be suitable for integration with MIMO active antennas.

3.2.Conventional Doherty Operating Principle

Figure 3-1 shows the conventional schematic of the Doherty power amplifier (DPA). The DPA architecture consists of two sub-amplifiers; the main amplifier is biased as Classes-AB/B while the auxiliary amplifier is modeled in the Class-C mode of operation. In the DPA operation, the main device conducts at a low power level, up to a preselected average power level, while the auxiliary device conducts when the power surpasses the preselected power level, which is often fixed at 6-dB OPBO. Typically, the DPA architecture includes an input power splitter that independently distributes the same power into the main and auxiliary paths. The impedance modulation in the conventional DPA is established using quarter-wave (λ/4) transformers in the output combiner network, which consists of a single λ/4 impedance inverting network (IIN) and a single λ/4 impedance transforming network (ITN).

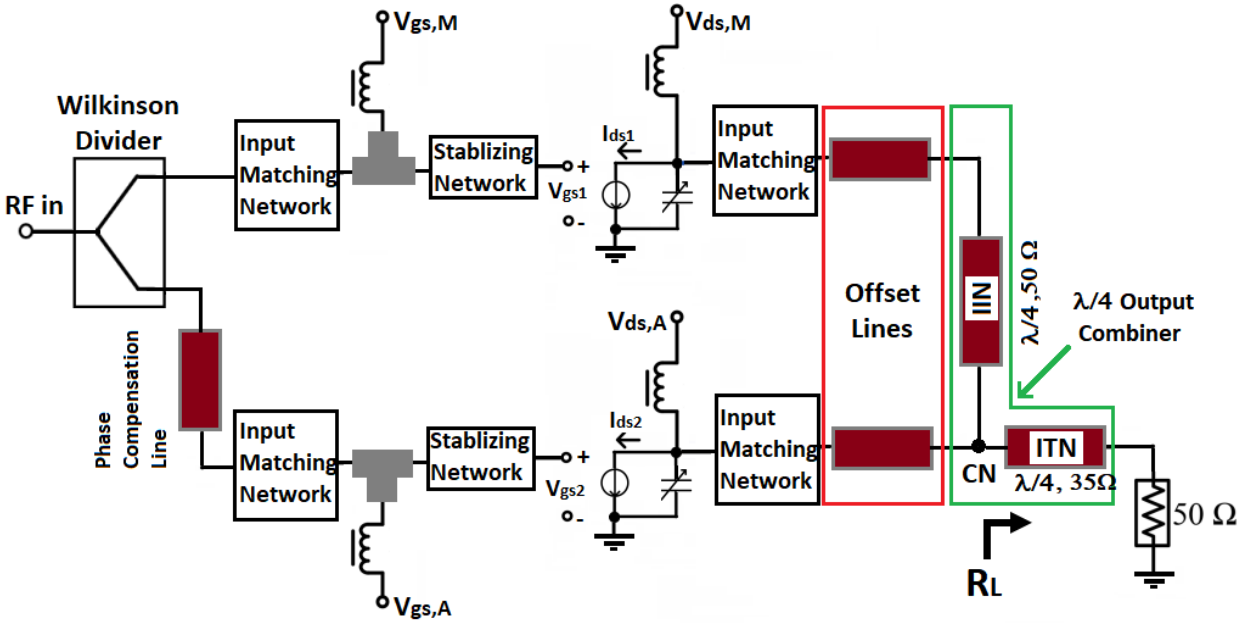

Figure 3-1 The circuit diagram of the conventional Doherty PA

To start the design, the designer needs to fix the ratio $\alpha = Z_{PK}/Z_{BO}$, which is equal to 0.5 in most cases, with the impedance seen by the main amplifier at peak power, $Z_{PK} = 50\Omega$, and the

impedance seen by the main amplifier at 6-dB back-off power level, Z_{BO} = 100Ω. The characteristic impedance of $\lambda/4$ transformer equals $Z_{\lambda/4} = \alpha\ Z_{PK}$. Also, the designer needs to fix the value of the power-dividing factor of the input-splitting network, which commonly equals 3 dB. To equalize the phase between the main and auxiliary branch of the Doherty amplifier, a 90-degree delay line cascaded to an in-phase splitter or else a quadrature hybrid is used. The second $\lambda/4$ transformer has no impact on the load-modulation, and it is inserted between the combining junction and the output of the DPA to be used only for impedance matching purpose to transform Z_{PK} /2 to Z_{PK}.

3.3.Generic design methodology of the proposed DPA

The proposed design methodology unifies and merges the concurrent design of the input matching networks of the main and auxiliary amplifiers with the input-splitting network. Also, the output matching networks of the main and auxiliary amplifiers are merged with the output combining network, without using an additional impedance transformer for impedance matching at the output network. Furthermore, by selecting the two appropriate transistors for the main and auxiliary amplifiers, and knowing through simulations or source-pull/load-pull characterization, their respective complex gain, optimum source, and load matching impedances, and their respective peak power capabilities when they are entirely driven, one can define:

- First, the voltage ratio α of the output matching-combining network needed to equalize the magnitude and phase of the two signals outputted by the two amplifiers at the combining junction.
- Second, the complex voltage splitting ratio γ of the input matching-combining network is needed to properly drive both the main and auxiliary amplifiers to equalize the gain's magnitude and phase in both branches of the Doherty amplifier.

The optimum source and load matching impedances for both amplifiers and the output impedance of the auxiliary amplifier have to be found through simulations or source-pull/load-pull characterization at an arbitrary back-off power level, (not necessarily 6 dB) where only the main amplifier is active, and the auxiliary amplifier biased in Class-C is in the turn-off mode. The values of α , γ and the source and load optimum impedances for the main and auxiliary amplifiers at the back-off level and the full drive level, will be sufficient to determine the S-parameters of the input and output three-port networks needed to design the Doherty power amplifier. This approach can be applied over a broader frequency band, since no transformer or offset lines are required. It is also anticipated that it will lead to a smaller form-factor and substantial gain in the surface area and cost when MMIC technology is selected for fabrication.

The block diagram structure of the proposed MMIC Doherty amplifier is shown in Figure 3-2. The amplifier configuration is composed of two stages. The first one is the driver stage, which consists of a single transistor biased at Class-AB. For the second power stage, i is like the Doherty amplifier operation, as the main transistor operates at the Class-AB biasing conditions, while the auxiliary transistor is biased at Class-C. The two transistors can deliver different output powers to achieve the desired back-off performance. The first step in designing a three-port Doherty PA is to obtain the parameters of the output matching-combining network (OMCN). The function of the OMCN is to combine the output powers from both the main and auxiliary transistors and to match the impedances of the two devices, at peak power and back-off power, to the required loaded impedances by the load modulation scheme taking place in the Doherty amplifier. The input matching-splitting network (IMSN) affects the Doherty back-off performance based on the splitting ratio selected and serves to equalize the phase and gain between the two branches of the Doherty amplifier, in addition to the input matching of the transistors. Inspired by the design

criteria reported in [48], a generalized design procedure was developed below to realize a broadband performance for the Doherty amplifier design.

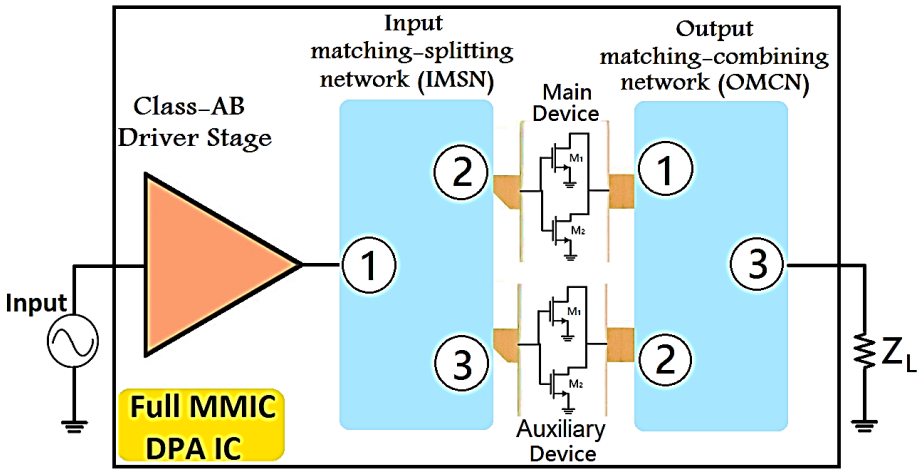

Figure 3-2 Proposed two-stage GaN MMIC Doherty PA with input/output networks

3.3.1. Output matching-combining network (OMCN)

The first step in designing a three-port DPA is to get the parameters of the OMCN. This nonsymmetrical OMCN is employed as a non-isolated power combiner network, that combines the output powers from both main and auxiliary transistors. Moreover, it is used to match the reference load impedance to the optimum impedance of the two transistors at output peak power, and keep the optimal response at output power back-off (OPBO). The reference impedances are defined as shown in Figure 3-3. The complex conjugate of the optimum impedance at the maximum output power of the main transistor $Z^*_{L,M,P}$ is the impedance for Port 1, while the complex conjugate of the optimum impedance at the maximum output power of the auxiliary transistor $Z^*_{L,A,P}$is the reference impedance for Port 2. The reference impedance for Port 3 is Z_L = 50Ω. The output-combining network, assumed to be a lossless and reciprocal network, combines

the output powers from the two transistors with an arbitrary ratio. We define the output power ratio (α) between the powers of the auxiliary and the main amplifiers as a function of the frequency by:

$$\alpha(f) = \frac{S_{32}a_2(f)}{S_{31}a_1(f)} \tag{3-1}$$

where S_{ij} are the S-parameters of the three-port network in 50Ω characteristic impedance. In case of indicating the phase of the S_{ij}-parameters to be (θ_{ij}), then based on [48], the general S-parameters matrix can be written as in:

$$S = \begin{bmatrix} -\frac{\alpha(f)e^{j(\theta_{21}(f)+\theta_{31}(f)-\theta_{32}(f))}}{1+\alpha(f)} & \frac{\sqrt{\alpha(f)}}{1+\alpha(f)}e^{j\theta_{21}(f)} & \frac{e^{j\theta_{31}(f)}}{\sqrt{1+\alpha(f)}} \\ \frac{\sqrt{\alpha(f)}}{1+\alpha(f)}e^{j\theta_{21}(f)} & -\frac{e^{j(\theta_{21}(f)-\theta_{31}(f)+\theta_{32}(f))}}{1+\alpha(f)} & \sqrt{\frac{\alpha(f)}{1+\alpha(f)}}e^{j\theta_{32}(f)} \\ \frac{e^{j\theta_{31}(f)}}{\sqrt{1+\alpha(f)}} & \sqrt{\frac{\alpha(f)}{1+\alpha(f)}}e^{j\theta_{32}(f)} & 0 \end{bmatrix} \tag{3-2}$$

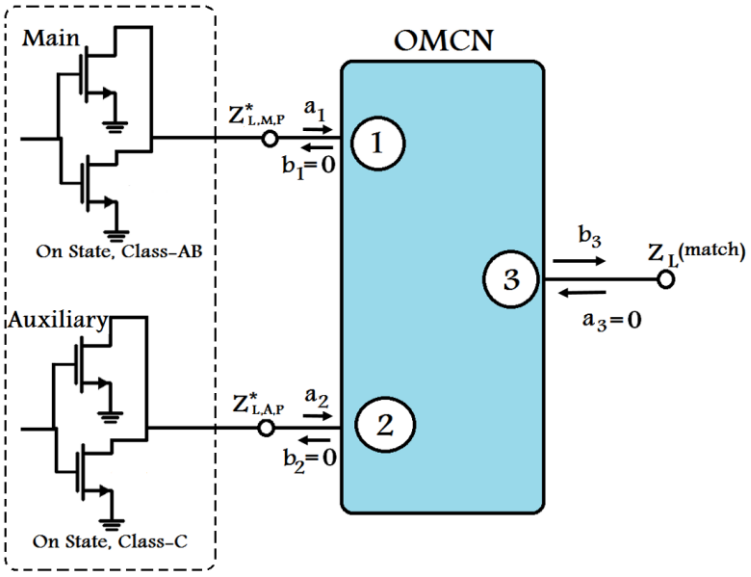

Figure 3-3 Output matching-combining network with three-port reference impedances (@ Peak Power)

From the S-matrix, the difference of the three phases in the three-port network $\theta_{21}(f)$, $\theta_{31}(f)$, $\theta_{32}(f)$ are used mainly to optimize the performance of the DPA in term of efficiency over the frequency bandwidth. The choice $\theta_{21}(f)$, will impact the impedance seen by the main transistor at the back-off state, and hence, the efficiency in the back-off region. As well, the choice of $\theta_{31}(f)$ and $\theta_{32}(f)$ will impact the phase balance between the two branches and, hence, the efficiency at peak power. This will depend mainly on the output reflection's coefficient of the auxiliary transistor and $\theta_{21}(f)$. Figure 3-4 shows the OMCN configuration at the back-off state. At output power back-off, Port 3 is connected to its reference impedance 50Ω, so the load reflection coefficient, seen by the main transistor, was calculated based on [48], [49], as shown in:

$$\Gamma_{L,M,BO}(f) = -\frac{\alpha(f)\, e^{j(\theta_{21}(f)+\theta_{31}(f)-\theta_{32}(f))}}{(1+\alpha(f)+|\Gamma_{t,A,BO}(f)|e^{j(\theta_{t,A,BO}(f)+\theta_{21}(f)+\theta_{32}(f)-\theta_{31}(f))}} \tag{3-3}$$

$\Gamma_{L,M,BO}(f)$ is the output reflection of the auxiliary transistor in the back-off state at different frequencies. At back-off, the auxiliary transistor is turned off, and the value of $\Gamma_{t,A,BO}(f)$ is calculated with the reference impedance of Port 2 ($Z^*_{L,A,P}$) as:

$$\Gamma_{t,A,BO}(f) = \frac{Z_{t,A,BO}(f)-Z^*_{L,A,P}(f)}{Z_{t,A,BO}(f)+Z_{L,A,P}(f)} \tag{3-4}$$

and,

$$\Phi_0(f) = \theta_{t,A,BO}(f) + \theta_{21}(f) + \theta_{32}(f) - \theta_{31}(f) \tag{3-5}$$

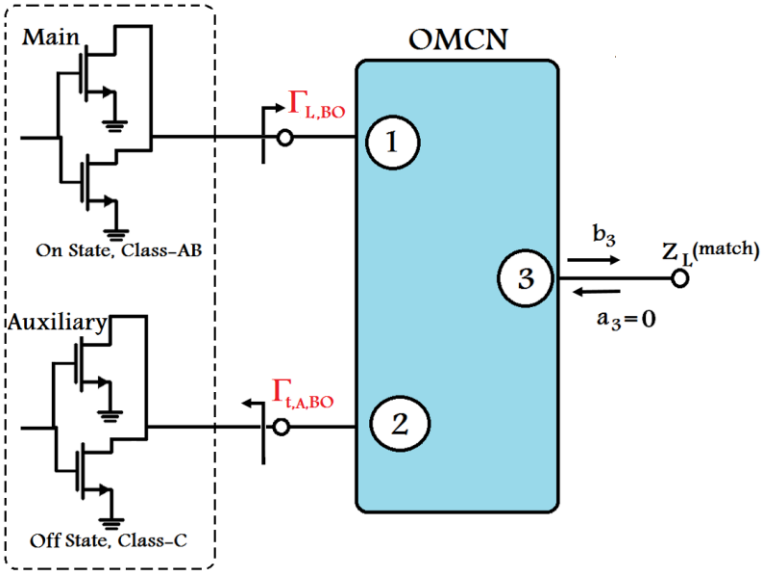

Figure 3-4 Three-port output matching-combining network at OPBO

and, the phase value of $\Gamma_{L,M,BO}(f)$ is deduced as:

$$\angle\left|\Gamma_{L,M,BO}(f)\right| = \pm\pi + \left(\theta_{21}(f) - \theta_{32}(f) + \theta_{31}(f)\right) - \Theta_D \tag{3-6}$$

where,

$$\Theta_D = tan^{-1}\left(\frac{\left|\Gamma_{t,A,BO}(f)\right| sin(\Phi_0(f))}{1+\alpha(f)+\left|\Gamma_{t,A,BO}(f)\right| cos(\Phi_0(f))}\right) \tag{3-7}$$

Using the above equations, one can get the value of $\Phi_0(f)$ as:

$$\Phi_0(f) = \pm cos^{-1}\left(\frac{\alpha(f)^2}{2(1+\alpha(f))\left|\Gamma_{t,A,BO}(f)\right|\left|\Gamma_{L,BO}(f)\right|^2} - \frac{1+\alpha(f)}{2\left|\Gamma_{t,A,BO}(f)\right|} - \frac{\left|\Gamma_{t,A,BO}(f)\right|}{2(1+\alpha(f))}\right) \tag{3-8}$$

The steps to find the optimum $\Gamma_{L,M,BO}(f)$, at the desired back-off output power are as follows:

1- Perform load-pull simulation for the main device at the desired output power back-off level.

2- Obtain the dc power consumption and the delivered output power in the $\Gamma_{L,M,BO}(f)$ plane, with $Z^*_{L,M,P}$ as the reference impedance.

3- Estimate the values of efficiency at the back-off level from the delivered power to the load and the dc power consumption.

4- Then plotting the efficiency contours to get the optimum load impedance for the main transistor at the back-off region.

Furthermore, from (3-6) and (3-8) we can deduce that:

$$\theta_{21}(f) = \frac{\angle|\Gamma_{L,M,BO}(f)| + \Phi_D(f) + \Phi_0(f) - \theta_{t,A,BO}(f) \pm \pi}{2} \tag{3-9}$$

and,

$$\theta_{31}(f) - \theta_{32}(f) = \frac{\angle|\Gamma_{L,M,BO}(f)| + \Phi_D(f) - \Phi_0(f) + \theta_{t,A,BO}(f) \pm \pi}{2} \tag{3-10}$$

Equation (3-9) is the direct analytical relationship giving the phase value between Port 1 and Port 2 of the OMCN $\theta_{21}(f)$, as a function of the phase of $\Gamma_{L,M,BO}(f)$ and $\Gamma_{t,A,BO}(f)$**,** which should be known in advance from load-pull simulation or characterization. The value of $\alpha(f)$, models the peak power ratio between the auxiliary and the main transistors, and it is known, as well, once the transistors are selected and characterized. The selection of the value of $\theta_{21}(f)$ can be used to tune the actual impedance presented by the auxiliary branch to the main transistor to make

it as close as possible to an open circuit. Furthermore, this phase controls the level of leakage of the signal from the main branch to the auxiliary branch at back-off mode, and hence, it can be used to optimize the efficiency of the DPA in the back-off region.

Equation (3-10) is the direct analytical relationship, given the phase difference value $\theta_{31}(f) - \theta_{32}(f)$ as a function of the phases of $\Gamma_{L,M,BO}(f)$, $\Gamma_{t,A,BO}(f)$ and the value of $\alpha(f)$, which should be known in advance from simulation or characterization. The proper selection of $\theta_{31}(f) - \theta_{32}(f)$ will ensure that the signal from the auxiliary transistor and the signal from the main transistor, which are not necessarily identical, will be in-phase and, hence, maximize the efficiency at peak power. Also, $\theta_{21}(f)$ can have four possible solutions according to the signs in the equations (3-8) and (3-9). Additionally, the phase difference $\theta_{31}(f) - \theta_{32}(f)$ can have multiple solutions, as well, based on the selected signs in (3-8) and (3-10). Based on the optimum $\Gamma_{L,M,BO}(f)$, $\Gamma_{t,A,BO}(f)$, and the value of $\alpha(f)$, we selected the appropriate values for $\theta_{21}(f)$ and $\theta_{31}(f) - \theta_{32}(f)$, using equations (3-9) and (3-10). Since only $\theta_{31}(f) - \theta_{32}(f)$ is relevant for the design approach, one can select an arbitrary, but adequate value, for $\theta_{31}(f)$ considering the process constraints, and then select $\theta_{32}(f)$, such that their difference satisfies the equation (3-10). Consequently, the degree of freedom in selecting the value of $\theta_{31}(f)$ will lead to a realizable OMCN, with much lower sensitivity and wideband characteristics.

3.3.2. Input matching-splitting network (IMSN)

The three-port input matching-splitting network (IMSN) proposed here is a non-isolated, nonsymmetrical power splitter. It also matches the source impedance to the input impedance of the two transistors. The IMSN provides any arbitrary phase difference between the two transistors, which means there is no need to offset lines in the DPA design. A set of reference impedances was selected for the input three-port network, as shown in Figure 3-5, and using these reference

impedances, we can obtain the S-parameters for the IMSN. The IMSN parameters are chosen based on the analysis of the main and auxiliary transistors input impedances to obtain an optimized broadband performance of the Doherty amplifier. The input-splitting network is assumed to be a lossless and a reciprocal network, and it splits the input powers into the two branches with an arbitrary complex ratio. At peak input power, the input signal to the main transistor is different in amplitude and phase from the one applied to the input of the auxiliary transistor. This can be expressed as follows:

$$\left.\frac{b_3(f)}{b_2(f)}\right|_{peak-power} = S_o = \gamma(f)e^{j\theta_o(f)} \tag{3-11}$$

where $\theta_0(f)$ is the phase difference between the main and the auxiliary input signals, and $\gamma(f)$ indicates the ratio between the power feeding the auxiliary and main amplifiers at peak power.

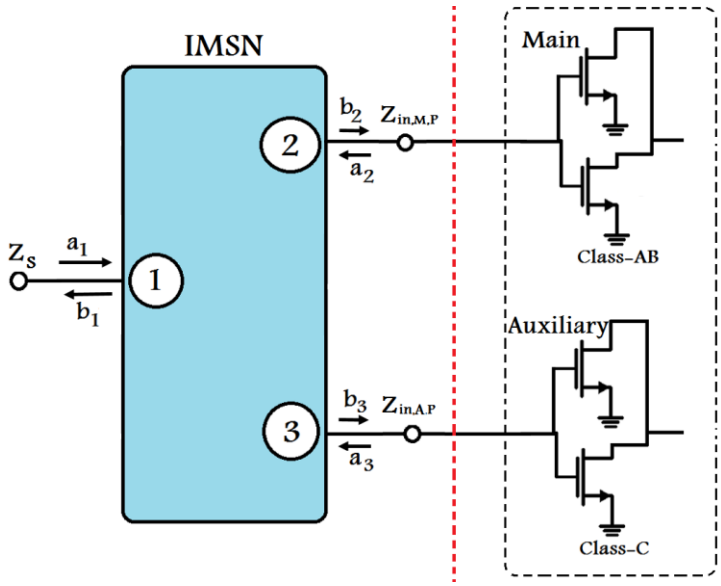

Figure 3-5 Input matching-splitting network with three-port reference impedances

At peak power, the main and auxiliary transistor's large-signal input impedances are equal to the impedances $Z_{in,M,P}(f)$ and $Z_{in,A,P}(f)$ at Ports 2 and 3, respectively. This means that the loads at Ports 2 and 3 have no reflection ($a_2 = a_3 = 0$), then according to (3-11) and based on the network lossless condition, one can deduce that the IMSN S-parameters matrix can be driven as:

$$S = \begin{bmatrix} 0 & \frac{1}{\sqrt{1+\gamma^2(f)}} e^{j\theta_{21}^*(f)} & \frac{\gamma(f)}{\sqrt{1+\gamma^2(f)}} e^{j(\theta_{21}^*(f)+\theta_0(f))} \\ \frac{1}{\sqrt{1+\gamma^2(f)}} e^{j\theta_{21}^*(f)} & \frac{\gamma^2(f)}{1+\gamma^2(f)} e^{j(\theta_{33}^*(f)-2\theta_0(f))} & -\frac{\gamma(f)}{1+\gamma^2(f)} e^{j(\theta_{33}^*(f)-\theta_0(f))} \\ \frac{\gamma(f)}{\sqrt{1+\gamma^2(f)}} e^{j(\theta_{21}^*(f)+\theta_0(f))} & -\frac{\gamma(f)}{1+\gamma^2(f)} e^{j(\theta_{33}^*(f)-\theta_0(f))} & \frac{1}{1+\gamma^2(f)} e^{j\theta_{33}^*(f)} \end{bmatrix} \quad (3\text{-}12)$$

From (3-12), the phase parameters $\theta_{21}^*(f)$ and $\theta_{33}^*(f)$ can be used to adjust the performance of the IMSN at power back-off. The input impedances of the transistors are dependent on the input power. These impedances can be used to adjust the amplifier's performance at power back-off. Theorizing that the large-signal input impedances at peak power and power back-off are $Z_{in,M,P}(f)$ and $Z_{in,M,BO}(f)$, respectively. For the auxiliary transistor, the large-signal input impedances are $Z_{in,A,P}(f)$, and $Z_{in,A,BO}(f)$ at peak power and back-off state, respectively.

At peak power, the proposed IMSN function is to divide the power with an appropriate ratio to both branches of the Doherty, such that both the auxiliary and main amplifiers will deliver the same in-phase current at the combining junction of the OMCN. At back-off mode, we will obtain the input reflection coefficient of the main transistor $\Gamma_{in,M,BO}(f)$ and the input reflection coefficient of the auxiliary transistor $\Gamma_{in,M,BO}(f)$. These input reflection coefficients $\Gamma_{in,M,BO}(f)$ and $\Gamma_{in,A,BO}(f)$ are obtained, either from load-pull /source-pull simulation or characterization of the main, and the auxiliary transistors are:

$$\Gamma_{in,M,BO}(f) = \frac{a_2(f)}{b_2(f)} = \frac{Z_{in,M,BO}(f)-Z_{in,M,P}(f)}{Z_{in,M,BO}(f)+Z_{in,M,P}^*(f)} \quad (3\text{-}13)$$

$$\Gamma_{in,A,BO}(f) = \frac{a_3(f)}{b_3(f)} = \frac{Z_{in,A,BO}(f) - Z_{in,A,P}(f)}{Z_{in,A,BO}(f) + Z^*_{in,A,P}(f)} \tag{3-14}$$

The ratio of powers delivered to the two transistors at OPBO state can be derived as:

$$\left|\frac{b_2(f)}{b_3(f)}\right|^2_{back-off} = \frac{1}{\gamma^2(f)} \left| \frac{1 - \Gamma_{in,A,BO}(f) e^{j\theta^*_{33}(f)}}{e^{j\theta_0(f)} - \Gamma_{in,M,BO}(f) e^{j(\theta^*_{33}(f) - \theta_0(f))}} \right|^2 \tag{3-15}$$

From equation (3-15), one can conclude that the value of the phase difference between the main and auxiliary input signals $\theta_0(f)$ is used to balance the over-all phases between the auxiliary and main branches of the DPA at peak power. Also, the power dividing ratio at OPBO is a function of $\theta^*_{33}(f)$, $\Gamma_{in,M,BO}(f)$, $\Gamma_{in,A,BO}(f)$ and $\theta_0(f)$. Since all the parameters in (3-13) are preferably fixed or known from characterization or simulation, we can expect the value of $\theta^*_{33}(f)$, this can later be used to set the splitting power factor of the IMCN at power back-off.

The selection of $\theta^*_{33}(f)$ will impact the broadband performance and the DPA behavior at the back-off state. Afterward, using the values of $\theta_0(f)$ and $\theta^*_{33}(f)$, we can obtain the S-matrix parameters. In (3-12), the non-constrained variable $\theta^*_{21}(f)$ can be selected, such that the IMCN design satisfies the constraints of the MMIC fabrication process, the frequency response, and yield performance.

3.3.3. Realization of the three-port network

The parameters of the three-port networks were driven based on the analysis in Sections 3.3.1 and 3.3.2 for the OMCN, and the IMSN can be realized using six elements circuit structure. It is a simple implementation for these parameters using circuit elements. This structure is suitable

for MMIC design to get a compact layout for the final amplifier. This network may be adopted and developed to be with more elements to get a broader frequency response, but will affect the circuit size and the insertion loss. This three-port network is shown in Figure 3-6, while the admittance matrix of this network can be written as:

$$Y = \begin{bmatrix} Y_1 + Y_4 + Y_5 & -Y_4 & -Y_5 \\ -Y_4 & Y_2 + Y_4 + Y_6 & -Y_6 \\ -Y_5 & -Y_6 & Y_3 + Y_5 + Y_6 \end{bmatrix} \tag{3-16}$$

we obtained the elements of the matching network by using the Y-parameters as:

$$\begin{aligned} Y_4 &= -y_{21} \\ Y_5 &= -y_{31} \\ Y_6 &= -y_{32} \end{aligned} \tag{3-17}$$

$$\begin{aligned} Y_1 &= y_{11} + y_{12} + y_{13} \\ Y_2 &= y_{21} + y_{22} + y_{32} \\ Y_3 &= y_{31} + y_{32} + y_{33} \end{aligned}$$

In (3-17), y_{ij} are the elements of the Y-matrix shown in (3-16). We can obtain the Y-parameters matrix from the S-parameters matrices (3-2) and (3-12), using the conversion criteria which is illustrated in [50]. Based on the obtained networks, we can select the most reliable network considering the foundry process limitations, yield requirements, and broadband performance. The new generalized design methodology is described in detail by the flowchart reported in Table 3-1 and is based on the theory presented in the previous sections.

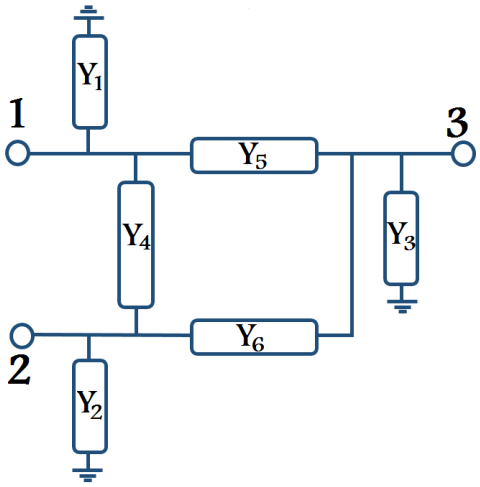

Figure 3-6 Three-port realization network based on circuit elements

Table 3-1 Design flowchart of the proposed DPA

1 - Specification of the Doherty Amplifier in terms of peak power, gain, efficiency, turn-on level of auxiliary amplifier, frequency bandwidth.
2 - Selection of the transistors for the main & peak amplifiers.
3 - Load-pull/source pull characterization @ peak power at several frequency points within the bandwidth.
4 - Knowledge of $Z_{L,M,P}$, $Z_{in,M,P}$, $Z_{L,A,P}$, $Z_{in,A,P}$, $P_{out,A,Peak}$, $P_{out,M,Peak}$, $G_{M,Peak}$ and $G_{A,Peak}$ for conjugate input matches over the frequency bandwidth.
5 - Determine $\alpha(f) = \frac{P_{out,A,Peak}}{P_{out,M,Peak,}}$.
6 – Determine the ratio of complex gains for the main and peaking amplifiers $\gamma(f) = \frac{G_{M,Peak}}{G_{A,Peak}}$.
7 - Load-pull/source-pull characterization @ Back-off power across the operating bandwidth.
8 - Knowledge of $Z_{in,M,BO}$, $Z_{in,A,BO}$, $Z_{L,M,BO}$ and $Z_{t,A,BO}$.
9 - Convert the three-port S-parameter to the Y-parameter matrix.
10 - From the four sets of Y-parameters for the output matching-combining network, select the appropriate values that suit wideband design.
11- In the range of Y-parameters, which meet the foundry process limits, perform yield analysis considering the process variation.
12- Converting three-port networks Y-parameters to circuits elements (L, C, and transmission lines (TL)).
13- Synthesize the two three-port networks and assess the Doherty amplifier performance.

3.4.Broadband MMIC two-stage DPA prototype

The GaN MMIC DPA was designed using the WIN Semiconductors Foundry GaN HEMT process. This technology is based on a 250 nm gate length process on GaN/SiC substrates. In this paper, the Doherty amplifier was designed based on two power bars, which consisted of two GaN HEMT cells to achieve a high-power density and enhance the power performance, compared to the single device. This improvement is due to the higher output resistance (R_{ds}) and lower gate to drain capacitance (C_{gd}). As well, using the power bar can enhance the performance of the breakdown voltage. Moreover, as per the load-pull power simulation, the RF maximum output power increases from 12 Watts to 16.8 Watts at 3.5 GHz operating frequency for eight-finger devices with 250 um gate width. Figure 3-7(a) shows DC–IV data for both single-gate (8-fingers and 250 um width) and power bars with 16-fingers and 250 um gate width. The gate bias range is from -4 to -1.5 V with 0.25 V step for both single-gate and the power bar. A microscopic image of the power bar device with 16-fingers is shown in Figure 3-7(b).

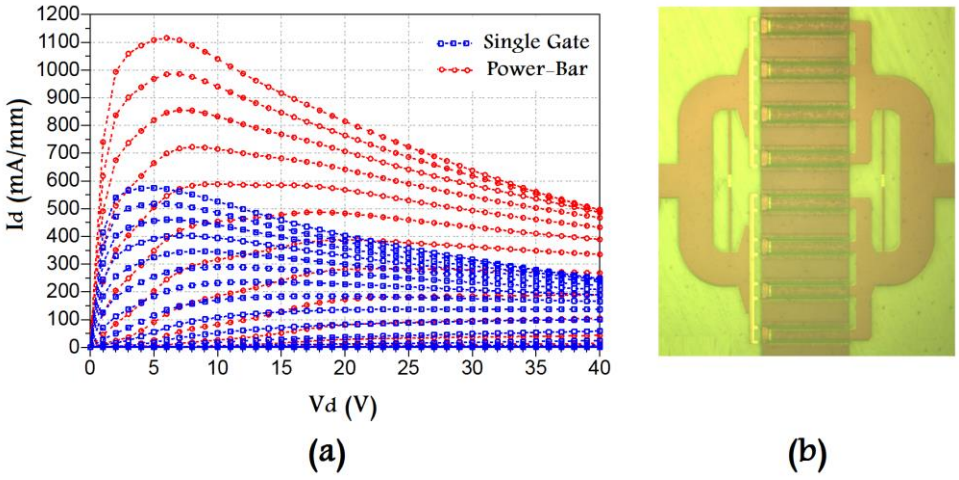

Figure 3-7 (a) Typical DC–IV of GaN single-gate and power bar devices, (b) Layout of the power bar

The Doherty power amplifier is designed based on the proposed amplifier topology to validate the analysis shown in Section 3.3. The power bar device was used for both the main and auxiliary branches. The design center frequency is 3.5 GHz. The design procedure was repeated for different frequencies, targeting a frequency band of 400 MHz bandwidth (3.3 – 3.7 GHz) to achieve the best input and output circuit parameters. The bias point of the main transistor is set to a quiescent current of 300 mA and a drain voltage of 30 V (Class-AB operation), while the Class-C auxiliary transistor is biased at the drain voltage of 30 V and the gate voltage of -5.3 V.

A parallel R-C network is added to the input of the transistors to stabilize the amplifier and prevent any oscillations, and then the optimum load impedance for each transistor was obtained using load-pull simulations. Figure 3-8 shows that, at the center operating frequency 3.5 GHz, the optimum load impedance at the maximum output power was $Z_{L,M,P}$ = 8.25 + j 12.6 Ω and $Z_{L,A,P}$ = 6.5 + j 12 Ω for the main and auxiliary transistors, respectively. The maximum output power was 41.7 dBm from the main device, while it was 40.85 dBm from the auxiliary transistor, and this means that α = 0.82. At back-off, the auxiliary transistor's small-signal output impedance was $Z_{t,A,BO}$ = 0.58 - j 22.26 Ω. At 3.4 GHz, the main transistor optimum load impedance was $Z_{L,M,P}$ = 7.8 + j 12.9 Ω and for the auxiliary transistor $Z_{L,A,P}$ = 5.5 + j 12.5 Ω at maximum output power. The maximum output power was 41.8 dBm from the main device, while it was 41 dBm from the auxiliary transistor, and this means that α = 0.83. At back-off the auxiliary transistor's small-signal output impedance was $Z_{t,A,BO}$ = 0.58 - j 24.413 Ω. Moreover, at 3.6 GHz, $Z_{L,M,P}$ = 8.7 + j 12.1 Ω for the main transistor and $Z_{L,A,P}$ = 6 + j 11 Ω for the auxiliary transistor, at this frequency the maximum output power was 41.65 dBm from the main device, but for the auxiliary transistor it was 40.7 dBm. According to these values, the power ratio coefficient α = 0.81. The small-signal output impedance was $Z_{t,A,BO}$ = 0.58 - j 22.6 Ω for the auxiliary transistor at output power back-

off. Based on these optimum load impedances at different frequencies, we obtained the load reflection coefficients seen by the auxiliary transistor $\Gamma_{t,A,BO}$. According to the characterization of the IMSN, the input power splitting ratio, γ = 1.1 was selected for the input network at 3.5 GHz, γ = 1.09 at 3.4 GHz, and γ = 1.1 at 3.6 GHz at output peak power.

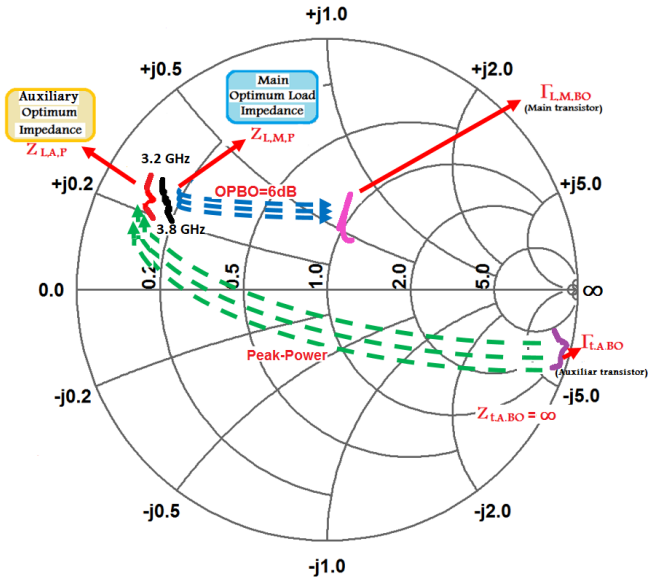

Figure 3-8 Load impedances seen by the main and auxiliary transistors at peak power and back-off states, and the load-modulation effects

The source and load reference impedances for the designed amplifier was 50 Ω, based on the reference impedances and by following the step procedures in Section 3.3.1. Afterward, using equations (3-7) and (3-8), the values of $\Theta_D(f)$ and $\Phi_0(f)$ can be obtained, and then by substituting into equation (3-9), we can estimate the possible four values of the phase θ_{21}. The values of these phases for the OMCN, at the targeting frequency range, were mentioned in Table 3-2. By sweeping θ_{31}, we can get the available admittance values Y_1 to Y_6 at a given frequency. These procedures were repeated at frequencies 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, and 3.8 GHz to get the best output parameters. By comparing the admittance parameters, we found that the shaded third and fourth

phase parameters in Table 3-2 lead to symmetrical admittance values across the desired operating frequency band from 3.3 to 3.7 GHz. In this Doherty design, we select the third phase parameter from Table 3-2. For a selected value of θ_{21}, Figure 3-9 displays the possible admittance values at these frequencies as a function of θ_{31}, it is noted that for some values of θ_{31} the admittance parameters have the same values for a certain range of frequencies. On the other hand, at other values of θ_{31}, the admittance parameters show large differences within the design frequency band. Based on the parameters from Figure 3-9, one can select a value of θ_{31} that suits a wideband design.

In addition, a yield analysis was performed to obtain the convenient matching network with low sensitivity to the process variation and, of course, meeting the process limitations of the foundry. Based on this analysis, the output network parameters were chosen from Figure 3-9 at the phase values of $\theta_{31} = 240^{o}$. It can be noted that $\theta_{31} = 120^{o}$ can be a good choice as well.

Table 3-2 θ_{21} as a function of the frequency

Frequency (GHz)	$\theta_{21}(f)$			
	1st value	2nd value	3rd value	4th value
3.3	151.35 °	-34.61 °	155.6 °	-27.63 °
3.35	154.76°	-25.23°	148.3°	-31.7°
3.4	156.33°	-23.66°	150.42°	-29.58°
3.45	173.22 °	-6.77 °	143.34 °	-36.65 °
3.5	189.55 °	9.55 °	139.3 °	-40.72 °
3.55	183 °	3 °	140.24 °	-39.75 °
3.6	177.9 °	-2.1 °	138 °	-42 °
3.65	182 °	1.88 °	132.4 °	-47.6 °
3.7	185.63 °	3.42 °	132.65 °	-49.8 °

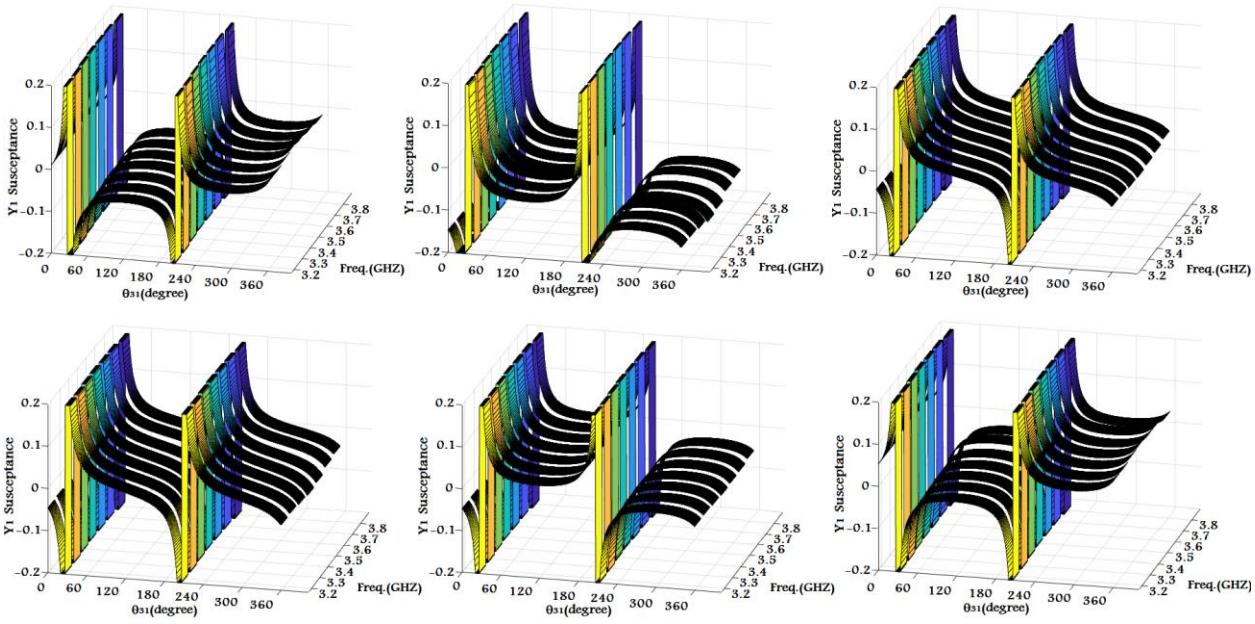

Figure 3-9 Possible output matching-combining network admittance values as a function of θ_{31} form pre-selected values of θ_{21} over the frequency range 3.2-3.8 GHz

By using the obtained OMCN, and performing source–pull simulation, at the center frequency of 3.5 GHz, the main transistor's large-signal input impedance at peak power was $Z_{in,M,P}$ = 2 - j 15.8 Ω, while at the power back-off, it was found to be $Z_{in,M,BO}$ = 1.9 - j 15.5 Ω. For the auxiliary transistor, the large-signal input impedances were found to be $Z_{in,A,P}$ = 2.24 - j 21.7 Ω and $Z_{in,A,BO}$ = 4 - j 23.8 Ω at peak power and the power back-off, respectively.

To design the IMSN, the complex input splitting factor was found as γ = 1.1, and the required phase difference between the main and the auxiliary input signals was determined to be θ_0 = 60° degree based on the design methodology presented in Table 3-1. From load-pull/source-pull simulation, we indicated the input reflection coefficients $\Gamma_{in,M,BO}(f)$ and $\Gamma_{in,A,BO}(f)$ of the main and the auxiliary transistors, respectively. Then, to obtain the value of $\theta_{33}^{*}(f)$, the power splitting factor at the power back off from 3.2 to 3.8 GHz is plotted in Figure 3-10, using equation (3-13). The value of θ_{33}^{*} = 250° turns out to be an appropriate choice over the desired frequency band, and

also, it provides a higher gain of the DPA at OPBO and minimizes the power dissipated in the input resistance of the auxiliary amplifier, when it is off.

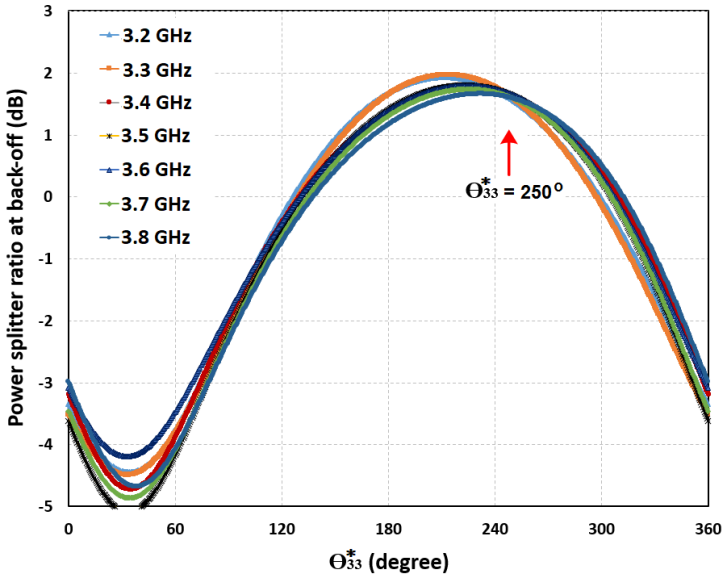

Figure 3-10 IMSN input power ratio of the main transistor to the auxiliary transistor at back-off region versus θ_{33}^{*}

Using the selected θ_{33}^{*} , the values of the admittance Y_1 to Y_6 as a function of $\theta_{21}^{*}(f)$ are plotted for the target frequency band as shown in Figure 3-11. To obtain an input-splitting network, with reasonable element values, θ_{21}^{*} = 45^{o} was selected because the admittance values at different frequencies fall around the same value. This means that using these parameters at this selected phase will suit a broadband design at the input network of the DPA. As a result, the elements of the input and output networks (Y1 to Y6) were obtained based on the proposed design methodology, which optimizes the DPA performance such as efficiency, back-off range, and frequency response, and also deals with the MMIC design constrains like circuit's sizes and yield as shown in Table 3. These values were obtained from Figure 3-9 and Figure 3-11, respectively. We transformed these values using combined distributed and lumped elements considering the derating's processes limits and to improve the yield dispersion.

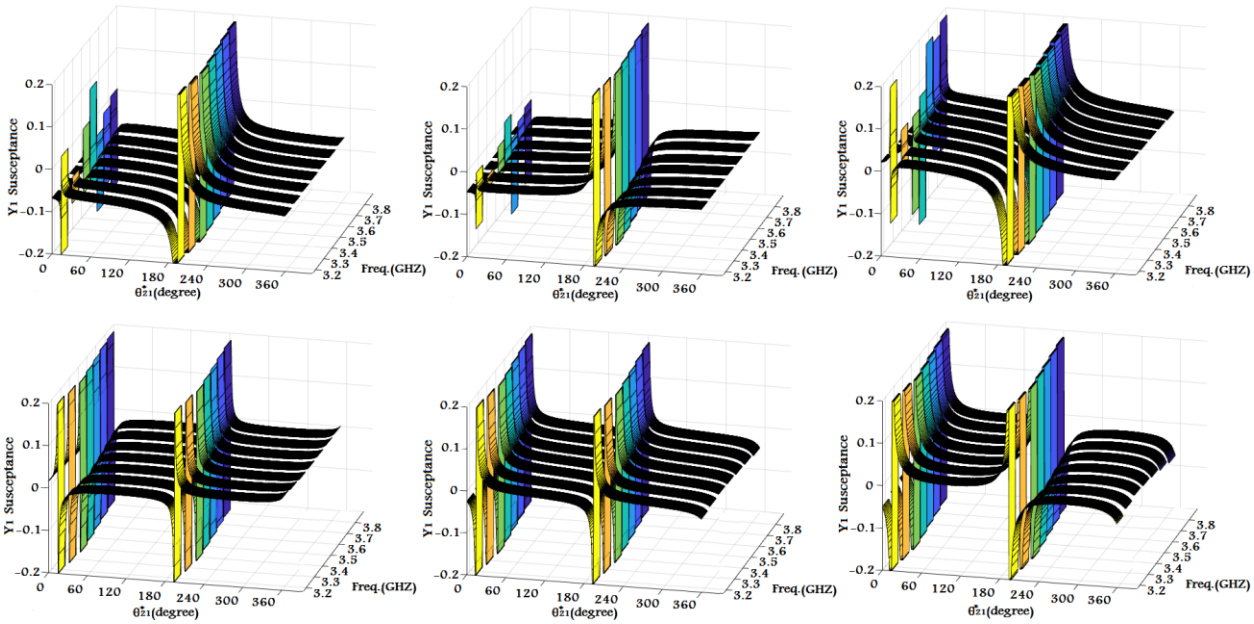

Figure 3-11 Input matching-splitting network admittance values from 3.2 - 3.8 GHz for (θ_{33}^{*} = 250º)

Table 3-3 Admittance values Y_1 to Y_6 for the OMCN and IMSN

Y-Pars.	Pass-yield		Fail-yield	
	OMCN Susceptance (S) (θ_{21}=139^o & θ_{31}=240^o)	IMSN Susceptance (S) (θ_{33}^{*}= 250^o & θ_{21}^{*}=45^o)	OMCN Susceptance (S) (θ_{21}=-40.7^o & θ_{31}=80^o)	IMSN Susceptance (S) (θ_{33}^{*}= 230^o & θ_{21}^{*}=180^o)
Y_1	-0.02	-0.054	-0.023	0.08
Y_2	-0.13	-0.058	-0.076	0.04
Y_3	0.02	0.015	-0.04	0.04
Y_4	0.04	-0.015	-0.03	0.025
Y_5	-0.035	0.018	0.025	0.028
Y_6	0.046	0.035	0.03	-0.01

In Table 3-3, we also reported another possible three-port network combination. The first one (shaded red) passed the yield analysis, according to the foundry's processing limits and design requirements which were used in the DPA implementation, while the second solution (shaded blue) failed in the yield performance. The specific yield analysis variations are illustrated in Table 3-4. After modifying the designed circuit, and adding the physical variable standard deviations and

the yield requirements, a Monte Carlo analysis was performed on the full MMIC Doherty circuit. A performance histogram of gain, PAE, and output power using 1600 trials, was calculated at the operating frequency band, as displayed in Figure 3-12, to obtain the accurate deviation. The Monte Carlo analysis shows that the yield of a gain greater than 26 dB, is 75%, while the yield of PAE greater than 50% at saturation power level, is 97%.

Table 3-4 Yield analysis of output power and PAE across the frequency of operation

Yield	1st Solution			2nd Solution		
	Max. Output power	PAE @ Peak Power	PAE @ 6-dB OPBO	Max. Output power	PAE @ Peak Power	PAE @ 6-dB OPBO
Peak-Peak variation	41-44 dBm	46-58 %	35-53 %	40-44 dBm	40-56 %	30-48 %
Yield process	75% Yeild>42 dBm	97% Yeild>50 %	90% Yeild>40 %	70% Yeild>42 dBm	50% Yeild>50 %	50% Yeild>40 %

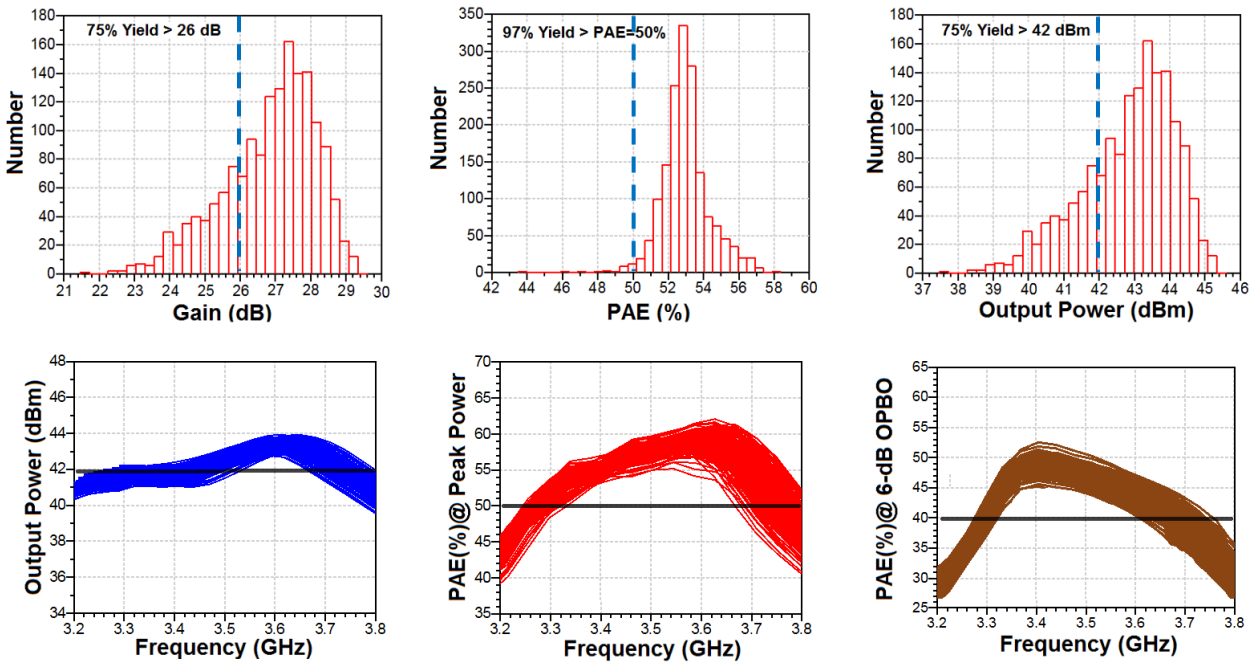

Figure 3-12 Variations, due to the yield process dispersion of gain, PAE, and output power of the MMIC DPA across the operating bandwidth

To verify the new design methodology, two DPAs, based on the three-port network are designed using the reference topology as in [48], and the new analysis proposed in this chapter. Figure 3-13 shows the detailed circuit parameters of the reference topology DPA, while the parameters in the proposed DPA are shown in Figure 3-14. The simulated large-signal performance of the referenced and proposed DPAs were plotted from 3.2 to 3.8 GHz, as in Figure 3-15. For the proposed DPA, wideband Doherty behavior can be observed from 3.3 to 3.7 GHz. The PAE is 42.5%–52% and 52%–59.4% for the 6 dB OPBO and saturation power level over this frequency band, respectively. For reference DPA, the operating bandwidth is narrow (3.45–3.6 GHz). However, the corresponding PAE is 38%–54% and 52%–60% for the 6 dB OPBO and saturation regions. Compared with the reference case, the proposed DPA can achieve broadband behavior with better large-signal performance. The full schematic of the proposed two-stage three-port network DPA is presented in Figure 3-16

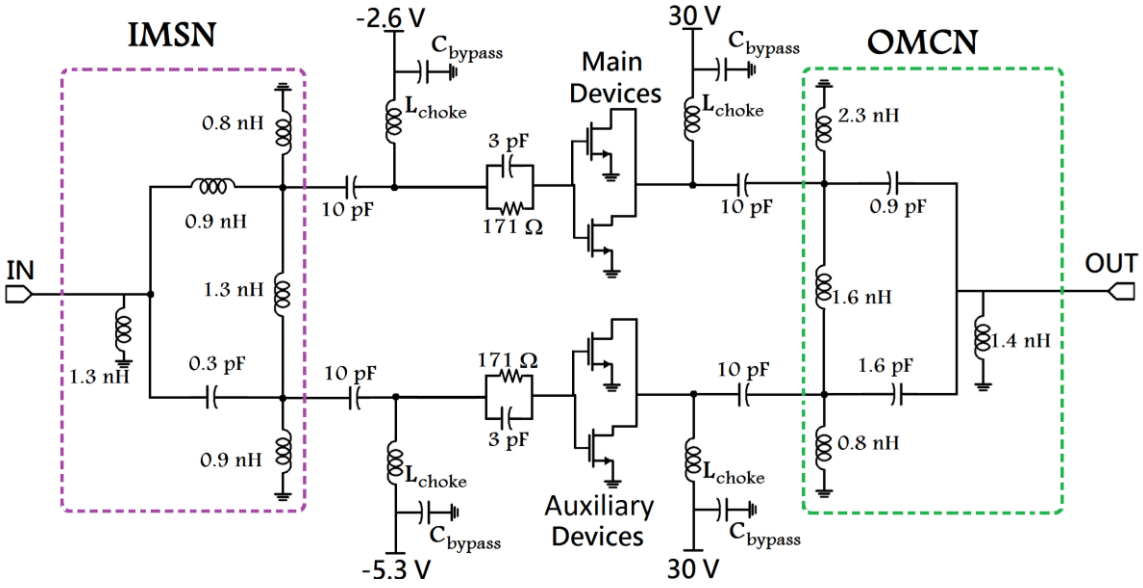

Figure 3-13 The reference DPA circuit

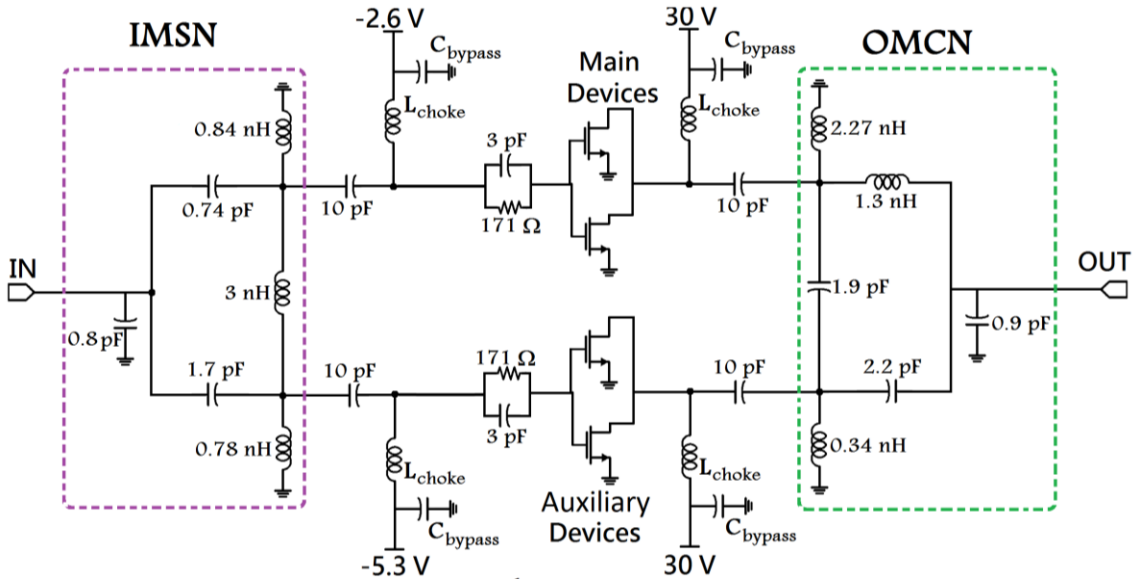

Figure 3-14 The proposed DPA circuit

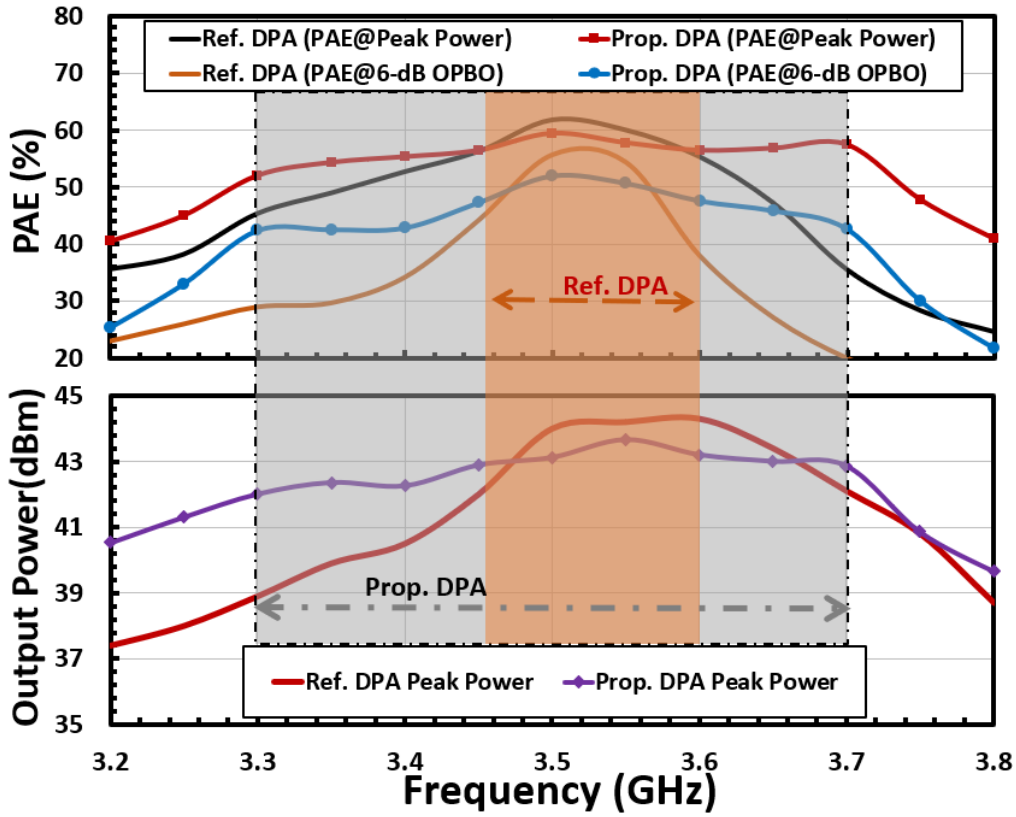

Figure 3-15 Simulation comparison between the reference and the proposed DPA circuits

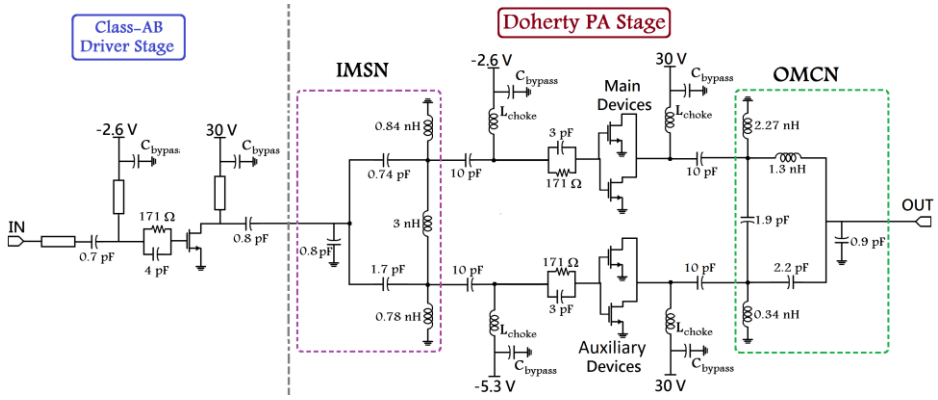

Figure 3-16 Complete schematic of the two-stage GaN MMIC three-port DPA

3.5.Fabrication and experimental characterization

The two-stage MMIC Doherty amplifier was designed and fabricated using a 0.25 um GaN-HEMT process. The carrier amplifier operates under a Class-AB condition with a quiescent current of 300 mA, and the auxiliary amplifier is biased to the Class-C condition. Both amplifiers have a drain supply voltage of 30V. A microscopic photo of the fabricated DPA IC on a package is displayed in Figure 3-17(a). In the design work, a compact layout was tailored, resulting in a chip size of 4.4 mm × 3.5 mm. Figure 3-17(b) shows a photograph of the implemented evaluation board. The DPA IC was mounted on a 7 mm × 7 mm QFN package. As shown in Figure 3-17(b), a few bypass capacitors were added to the evaluation board.

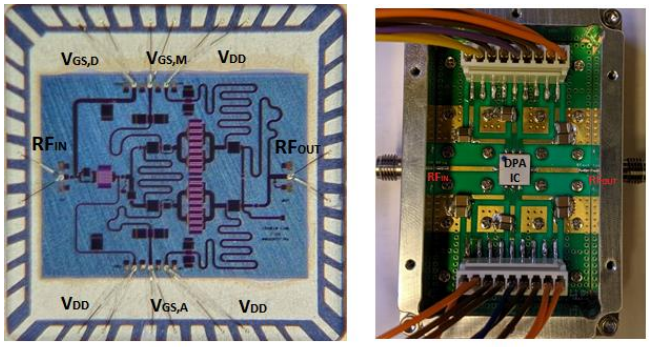

Figure 3-17 Microscope image of the fabricated GaN-HEMT DPA, (a) DPA IC on a QFN package, (b) Evaluation board

3.5.1. Measurement with pulsed and CW signals

The fabricated DPA has been experimentally characterized using pulsed-RF and CW signals. In the pulsed-RF setup, the gate quiescent voltage for the first stage and the main amplifier is varied from on state (Vg = −2.6 V) to a large negative voltage (Vg = −5 V) covering voltages at which a HEMT operates with RF pulsed driving signal. The pulse width is 5 µsec, and the pulse period is 200 µsec. The peak power of the pulsed-RF signal was estimated by sensing the average power of the pulse, and then dividing it by the duty cycle of the pulse [51]. Figure 3-18 illustrates the detailed components of the full setup used in the Doherty PA measurements, while the actual measurement bench is depicted in Figure 3-19.

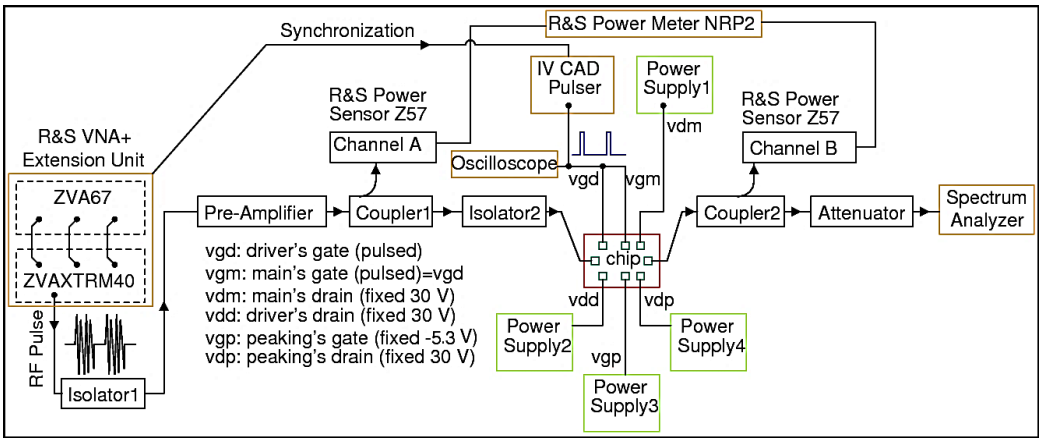

Figure 3-18 Block-diagram of the measurement setup

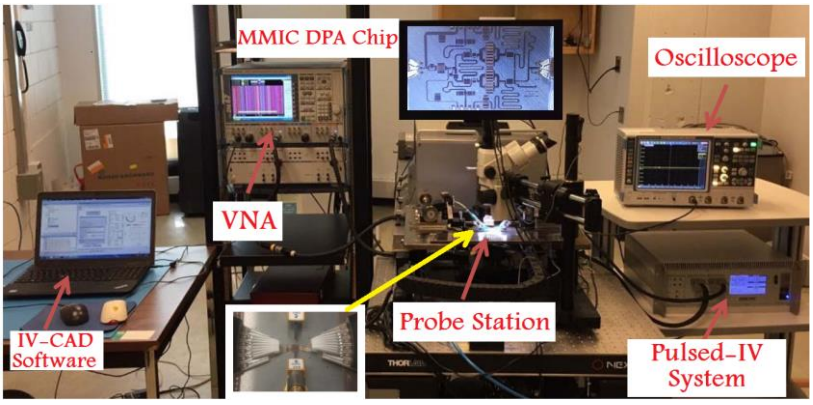

Figure 3-19 The actual measurement setup for the MMIC DPA characterization

Six samples of the MMIC PA have been characterized, to determine the process performance uniformity, and thus, verify the robustness of the design strategy. Figure 3-20 shows the measured power added efficiency (PAE) and the gain of the fabricated DPA as a function of output power at different frequencies within the band. Drain efficiency of 51% – 59.2% and 38.6% – 51.5% is achieved at the peak output power and 6-dB output power back-off region, respectively. The measured maximum output power is more than 42 dBm. The CW measurement results verify that the designed MMIC amplifier shows excellent performance at the frequency band from 3.3-3.7 GHz. To better present, the outcome broadband performance of the proposed DPA, the measured PAE, peak output power, and gain at 6-dB output power back-off, for the six samples of the fabricated MMIC DPA are plotted versus frequency as depicted in Figure 3-21. The plotted data shows that the PAE is in excess of 50.8% and 38% is obtained at peak output power and 6-dB OPBO, respectively, over the targeting frequency band. In addition, the saturated output power across the band is in order of 41.8 dBm with an associated gain in the range of 27.4 dB to 30.6 dB.

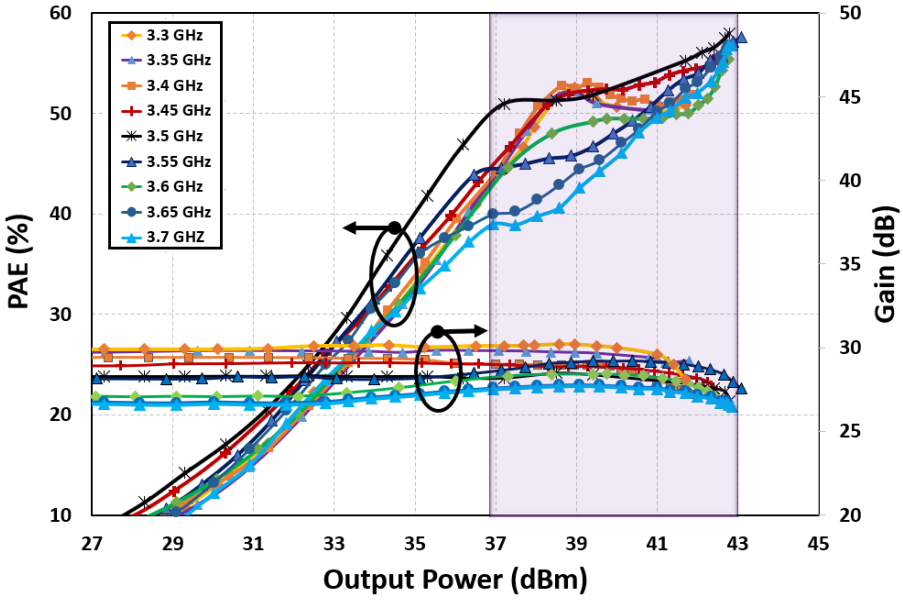

Figure 3-20 Measured gain and power-added efficiency versus output power

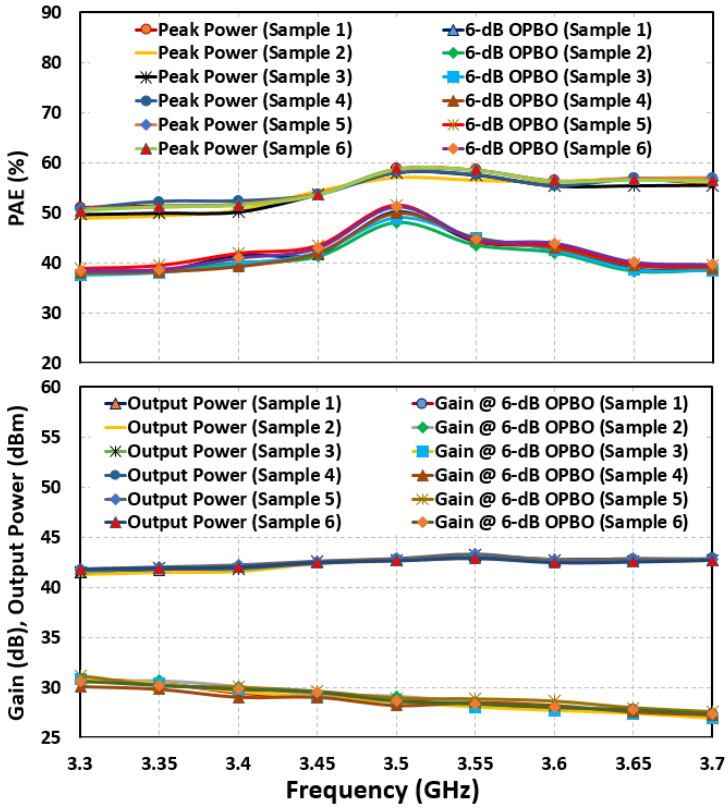

Figure 3-21 Measured power added efficiency, peak output power, and gain at OPBO versus frequency

3.5.2. Measurement with modulated signal

To evaluate the performance of the fabricated MMIC DPA when driven by a modulated signal, a long-term evolution (LTE) signal having 7.5 dB of PAPR and 20 MHz of bandwidth was employed to test the DPA at 3.5 GHz. The power of the LTE signal was swept and the values of the average drain efficiency (DE) and adjacent channel power ratio (ACPR) for the designed DPA were obtained and plotted versus output power, as displayed in Figure 3-22. The measured ACPR at an average output power of 36.5 dBm, changed from -27 dBc to -22.4 dBc. Meanwhile, the measured average drain efficiency of the amplifier was between 36.5% and 46.4% across the whole working frequency band. Digital pre-distortion (DPD), consisting of the lookup table and memory polynomial, was performed to linearize the implemented DPA. Figure 3-23 displays the output

spectrum with, and without, DPD linearization of the DPA under a 20 MHz signal at 3.5 GHz. It is clear from the results in Figure 3-23 that the ACPR, after performing DPD, was improved to better than -47 dBc. These results confirm that the fabricated MMIC DPA achieves consistent power and efficiency performance, across the frequency of operation, and relatively excellent performance compared with the other published studies, as listed in Table 3-5.

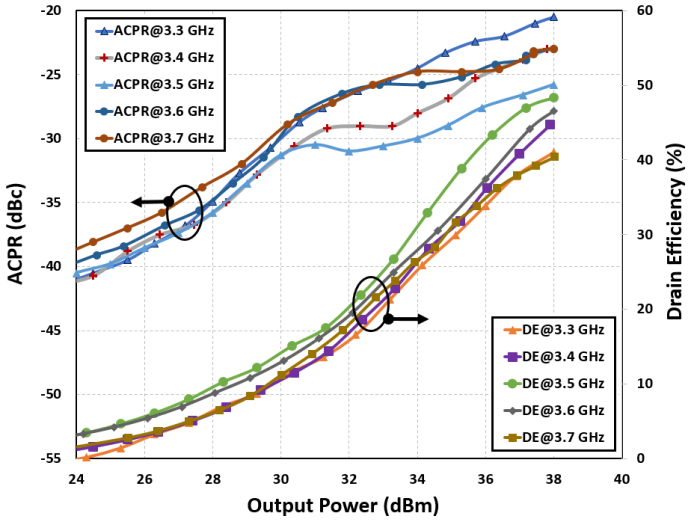

Figure 3-22 Measured ACPR and the average drain efficiency of the modulated signal versus average output power

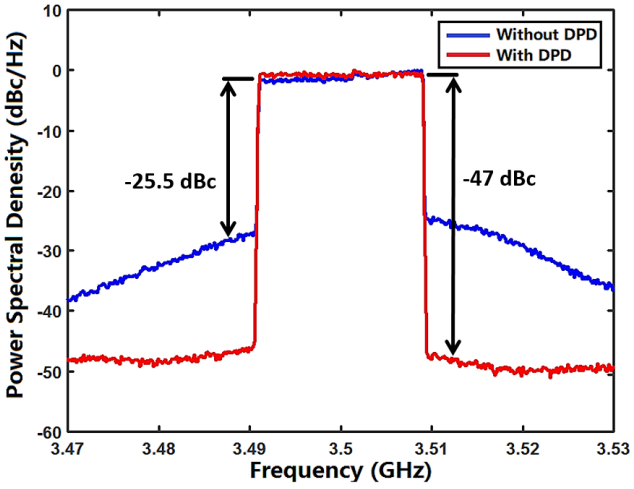

Figure 3-23 Measured normalized power spectral density of a 20 MHz LTE signal at 3.5 GHz with and without digital pre-distortion

Table 3-5 Comparison with recently reported DPAs

Ref.	Freq. (GHz)	Maximum output power (dBm)	Gain at peak power (dB)	PAE at peak power (%)	PAE at 6-dB OPBO (%)	Technology
[52] one-stage	6.5-8.5	35	6-14	32-53	30-43	GaN HEMT 0.25 um
[53] one-stage	2.1-2.7	41	12-14	-	-	GaN HEMT 0.25 um
[48] one-stage	0.95	41	15	58	54	GaN Cree
[54] one-stage	5.5-6.5	44	9	37-43	32-36	GaN HEMT 0.25 um
[55] one-stage	2.14	42	135	63	55	GaN HEMT 0.25 um
[56] one-stage	5.1-5.9	38.7	15	43-47	31.6-49.5	GaN HEMT 0.25 um
[57] two-stage	1.7	38.6	16	45.8	35	GaN HEMT 0.25 um
[58] two-stage	2.41	41.2	19	56.2	43.4	GaN HEMT 0.25 um
[59] two-stage	7	38	14	57	41	GaN HEMT 0.25 um
This Work (two-stage)	3.35-3.65	42	27	52-60	40-51	GaN HEMT 0.25 um

3.6.Conclusion

This chapter demonstrates the general broadband design methodology for Doherty architecture based on three-port input and output combining and matching networks. For broadband operation, a new design methodology with a detailed theoretical parameter for both input and output networks was used to alleviate the bandwidth limitations. For the first time, the three-port matching and combining networks were implemented using MMIC technology. The non-isolated output network performs as a power combiner, and it matches the reference load

impedance to the optimum impedance of the two transistors at output peak power, and keeps the optimal response at the back-off region. Moreover, the input-splitting network is proposed for matching the input impedances of the two transistors to the source impedance. According to the measured results, the proposed DPA achieves the desired Doherty operation, resulting in a high PAE and high output power across the targeting operation band. These results show superior performance compared to other reported MMIC Doherty PAs.

4. High-efficiency broadband DPA using harmonically tuned network

4.1.Introduction

Green communications aim at creating more environmentally friendly systems by exploring sustainability, energy recycling, and the enhancement of power efficiency in telecommunication systems. Within telecommunication systems, there are many challenges to be addressed, such as operating energy consumption [60]-[62], wide bandwidth [63], high peak-to-average power ratio (PAPR) [64], [65], and good linearity [67]. Reducing energy consumption will be one of the most significant challenges for the base station infrastructures of the next generation of telecommunication systems [68]. Since the power amplifier (PA) is the most critical subsystem of the radio transmitter, the development of power-efficient and broadband PAs, that simplifies hardware complexity and meets the requirements of fifth-generation (5G) and beyond in industrial applications is essential. These developments would also provide higher reconfigurability as a precursor in the deployment of the modern wireless communication infrastructure [69]. A Doherty PA, which was proposed by W.H. Doherty in 1936 [19], is one of the most efficient methods, due to its high back-off efficiency and easy realization.

The DPA can be designed over broad bandwidth using different techniques, such as integrated compensating reactance [70], post-matching architecture [71]–[72], complex combining loads [73], [74], and reciprocal gate bias [75]. These techniques can improve the impedance matching condition of the DPA at peak power conditions. However, the impedance mismatch still exists in the back-off region due to limitations of their load modulation network (LMN) structures, which causes degradation in the efficiency performance at the output power back-off (OPBO) region. Accordingly, it is desirable to explore a new harmonic control network (HCN) associated with the post-matching topology, which provides a more precise impedance matching at power

back-off within a wide frequency range, while maintaining the Doherty load modulation operation at the same time. The main function of the HCN is to shape the voltage and current waveforms at the device's current generation plane, leading to efficiency enhancement of the DPA across the entire operating frequency.

In this chapter, a novel HCN is proposed for designing a high-efficiency broadband DPA. This HCN employs a second harmonic impedance inverter circuit (SHIIC) and a third harmonic suppression network (THSN) to provide a second harmonic short termination and third harmonic open termination. Concurrently, enhancing bandwidth and efficiency can be achieved by maintaining the fundamental frequency load modulation with this technique.

4.2.Analysis of the proposed Doherty PA

In the proposed DPA, the output topology consists of an appropriate harmonic control network to tune the second and third harmonics at the current generator planes of the two active devices to achieve a back-off and peak power efficiency enhancement. This output network topology ensures that the main and auxiliary optimum load impedances are maintained for the transistor's respective outputs. The main and auxiliary branch's drain impedances are designated as Z_M and Z_A, respectively, while R_L is the impedance at the joining point as shown in Figure 4-1. The load-pull simulation results of GaN transistors operating in the Doherty region, indicate that the real part of optimal impedances at the saturation and back-off level is almost unchanged. In contrast, the value of the imaginary part decreases and moves toward the real axis as the output power increases. Table 4-1 shows the optimal impedances of Cree's CGH40010F at saturation and back-off power levels across the frequency of operation 1 – 2 GHz.

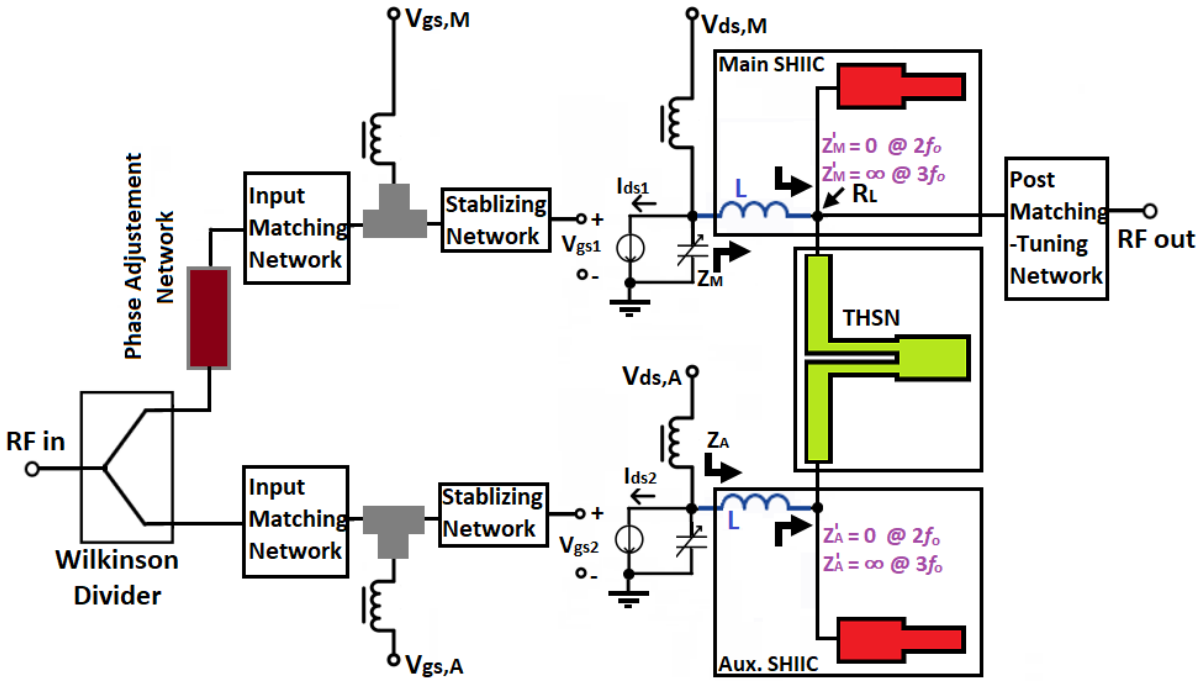

Figure 4-1 Proposed Doherty power amplifier architecture with second and third harmonic controlling network

Table 4-1 Optimal impedances for the active device at different input power levels

Frequency (GHz)	$Z_{Opt}(\Omega)$ @SATURATION	$Z_{Opt}(\Omega)$ @OPBO
1	27.5 - j*1.5	26.8 + j*19
1.2	25.4 - j*2.7	24.8+ j*16.8
1.4	24.2 - j*4.8	23.6 + j*17
1.6	23.9 - j*5.7	22.8 + j*17.4
1.8	23.4 - j*6.2	22.3 + j*18.2
2	22.8 - j*6.8	21.7 + j*18.6

The load conditions of the proposed DPA at the back-off power region can be expressed as:

$$Z_M = \begin{cases} Z_{M,Opt} & @ \quad f_o \\ 0 & @ \quad 2f_o \\ \infty & @ \quad 3f_o \end{cases} \tag{4-1}$$

and,

$$Z_A = \infty \quad @ \quad f_o \tag{4-2}$$

where $Z_{M,Opt,}$ and $Z_{A,Opt}$ are the optimal impedance of the main and auxiliary devices, respectively. With an increase in output power, the auxiliary device then turns on and the proposed DPA enters the Doherty region. At peak power level, the load conditions can then be presented as:

$$Z_M = \begin{cases} Z_{M,Opt} & @ \quad f_o \\ 0 & @ \quad 2f_o \\ \infty & @ \quad 3f_o \end{cases} \tag{4-3}$$

and,

$$Z_A = \begin{cases} Z_{A,Opt} & @ \quad f_o \\ 0 & @ \quad 2f_o \\ \infty & @ \quad 3f_o \end{cases} \tag{4-4}$$

4.2.1. Operating principle of the proposed DPA at the fundamental and second harmonic frequency (main branch)

In the conventional DPA, λ/4 transmission lines are used to realize the impedance inverter at the main branch. For the post-matching structure, the λ/4 transmission line is often considered inappropriate for the following reasons. First, using Quarter-wave transmission lines as impedance inverters restricts the operating bandwidth of the Doherty amplifier. Second, the crucial function of the impedance inverters in the proposed DPA is to provide the proper matching at the fundamental frequency, as well as, controlling the second-harmonic frequencies in the main and auxiliary branches.

The configuration of the second-harmonic shorted circuit (SHSC) can be achieved in the proposed Doherty power amplifier by adding a shunt resonant circuit as a part of the impedance inverters of the main and auxiliary branches to control the second-harmonic impedance at the device's current generation planes. The impedance inverter circuit is composed of a series inductor with a shunt *L*-*C* resonator as shown in Figure 4-2. However, there are some constraints when employing the shunt SHSC into the load matching network (LMN). First, the degradation in the Doherty amplifier operating bandwidth can be attributed to the mismatch introduced by the SHSC. Second, the *L*-*C* resonance of the SHSC in the DPA requires a large inductor value of L_{SH} at low power and a relatively small L_{SH} in the Doherty region. This is because the imaginary term for the optimal impedance of the GaN transistor will move toward the real axis, while the real part remains unchanged with an increase in the output power. The resonant frequency of the shunt SHSC can be written as:

$$Z_{SH}(2f_o) = j4\pi f_o L_{SH} + \frac{1}{j4\pi f_o C_{SH}} \tag{4-5}$$

Consequently, the relationship between L_{SH} and C_{SH} can be derived as:

$$L_{SH} = \frac{1}{16\pi^2 f_o^2 C_{SH}} \tag{4-6}$$

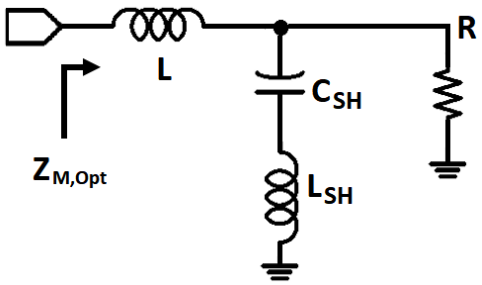

Figure 4-2 Circuit schematic of a normalized low-pass impedance inverter with second harmonic LC resonator

Based on the impedance inverter circuit shown in Figure 4-2, the presented impedance to the main device is expressed as:

$$Z_{M,Opt} = j\omega L + \frac{1}{\left(\frac{1}{j\omega L_{SH} + \frac{1}{j\omega C_{SH}}}\right) + \frac{1}{R}} \tag{4-7}$$

$$R = \begin{cases} R_L, & Back-off \\ 2R_L, & Saturation \end{cases} \tag{4-8}$$

The real and imaginary parts of $Z_{Opt,M}$ can be represented in term of the normalized frequency $\boldsymbol{\omega'}$ as:

$$real\left(Z_{M,Opt}\right) = \frac{R\left(1-\left(\frac{\omega'}{2}\right)^2\right)^2}{\left(1-\left(\frac{\omega'}{2}\right)^2\right)^2 + \frac{C_{SH}}{L_{SH}}\left(\frac{R\omega'}{2}\right)^2} \tag{4-9}$$

$$imag\left(Z_{M,Opt}\right) = \frac{\omega'}{2\sqrt{L_{SH}C_{SH}}}\left(L - \frac{R^2C_{SH}\left(1-\left(\frac{\omega'}{2}\right)^2\right)}{\left(1-\left(\frac{\omega'}{2}\right)^2\right)^2 + \frac{C_{SH}}{L_{SH}}\left(\frac{R\omega'}{2}\right)^2}\right) \tag{4-10}$$

From Table 4-1, the real part of the optimal impedance of GaN CGH40010F is almost unchanged at the OPBO and saturation regions, while the imaginary part moves towards the real axis with an increase in the output power. As a result, the shunt *L*-*C* resonator values of SHSC were chosen from Figure 4-3 to meet these requirements and satisfy the broadband conditions for the Doherty operation. We select the L_{SC} value to be 1.3nH, while the C_{SC} value equals 2.5pF in the main branch.

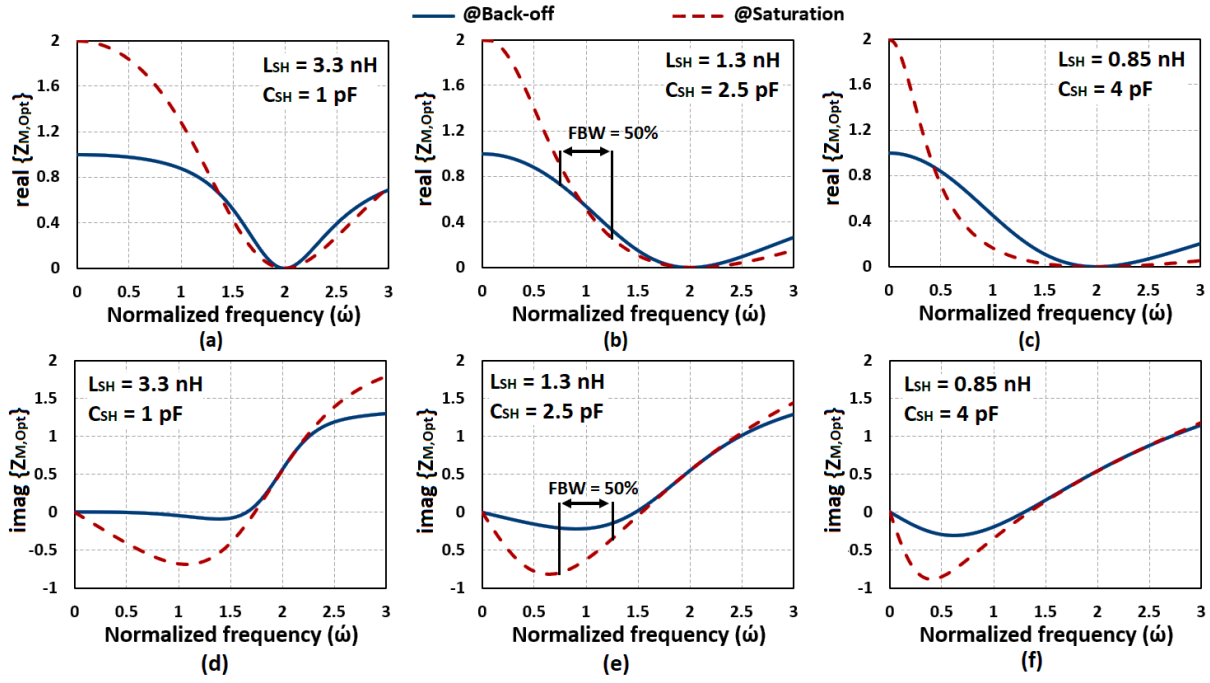

Figure 4-3 The transformed impedance to the main branch in different load conditions and different SHSC configurations

4.2.2. Third harmonic suppression network (THSN)

The third harmonic suppression network consists of two sections: the frequency-tuned coupling structure (FTCS) unit and two feeding transmission lines. The FTCS is the key section that provides the harmonic suppression property. The structure of FTCS is composed of an anti-coupled line terminated with a capacitive load, realized by a low impedance stub. An FTCS unit's structure, with an equivalent characteristic impedance Z_c and an equivalent electrical length Φ is shown in Figure 4-4(a). The even- and odd-mode equivalent circuits are shown in Figure 4-4(b) and (c), respectively. The harmonic suppression network is designed to maintain the optimum impedance at the auxiliary branch over the entire operating frequency. This behavior leads to proper matching at the fundamental frequencies, which enhances frequency operation bandwidth.

The method of even- and odd-mode analyses can be used for studying the characteristic of the FTCS unit. The even- and the odd-mode input impedance of the circuit can be derived as:

$$Z_{ie} = Z_{Le}\frac{Z_{me}+jZ_{Le}\tan\theta}{Z_{Le}+jZ_{me}\tan\theta} \tag{4-11}$$

$$Z_{io} = jZ_{Lo}\tan\theta \tag{4-12}$$

$$Z_{me} = 2Z_m = \frac{2Z_r}{j\tan\theta} \tag{4-13}$$

where Z_{Le} and Z_{Lo} are the coupled line even- and odd-mode characteristic impedances, respectively, while Z_r is the open-circuited stub characteristic impedance. The harmonic suppression band of the THSN is indicated, based on the electrical length θ, which is a function of

the even and odd-mode impedances. The harmonic suppression band can be assessed by making the transmission coefficient S_{21} equal to zero, which is given by [76] as:

$$S_{21} = \frac{\Gamma_e - \Gamma_o}{2} = \frac{Z_0}{Z_{Lo}+Z_0} - \frac{Z_0}{Z_{Le}+Z_0} \tag{4-14}$$

The equivalent characteristic impedance Z_c of the harmonic suppression section can be calculated as:

$$Z_c = \sqrt{|Z_{Lo}Z_{Le}|} \tag{4-15}$$

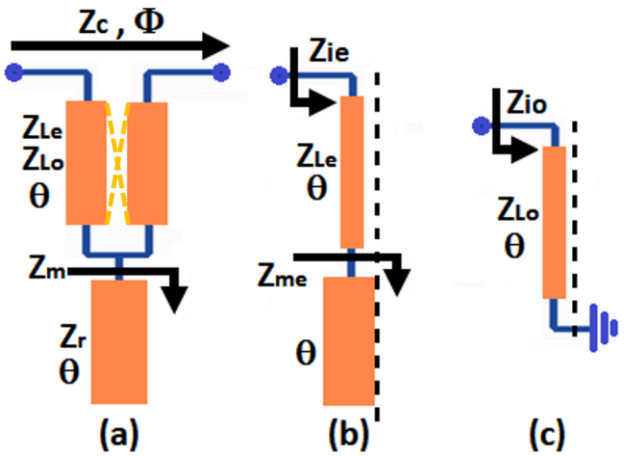

Figure 4-4 (a) The structure of FTCS unit, (b) Even-mode excitation, (c) Odd-mode excitation

The harmonic suppression unit is designed using the following steps:

1- Select the appropriate values for Z_{Le}, $Z_{Lo,}$ and Z_r. In this paper, Z_{Le}, $Z_{Lo,}$ and Z_r are set as 115, 60, and 45 Ω, respectively.

2- Plot the equivalent characteristic impedance Z_c versus the electrical length θ as shown in Figure 4-5. The middle part of the plot indicates the stopband region of the FTCS unit.

3- Determine the value of θ_o which represents the operating frequency of the proposed DPA.

4- Calculate the center frequency of the stopband of the FTCS unit f_s by:

$$f_s = \frac{\pi f_o}{2\theta_o} \tag{4-16}$$

5- Then, all obtained values can be converted into their physical counterparts.

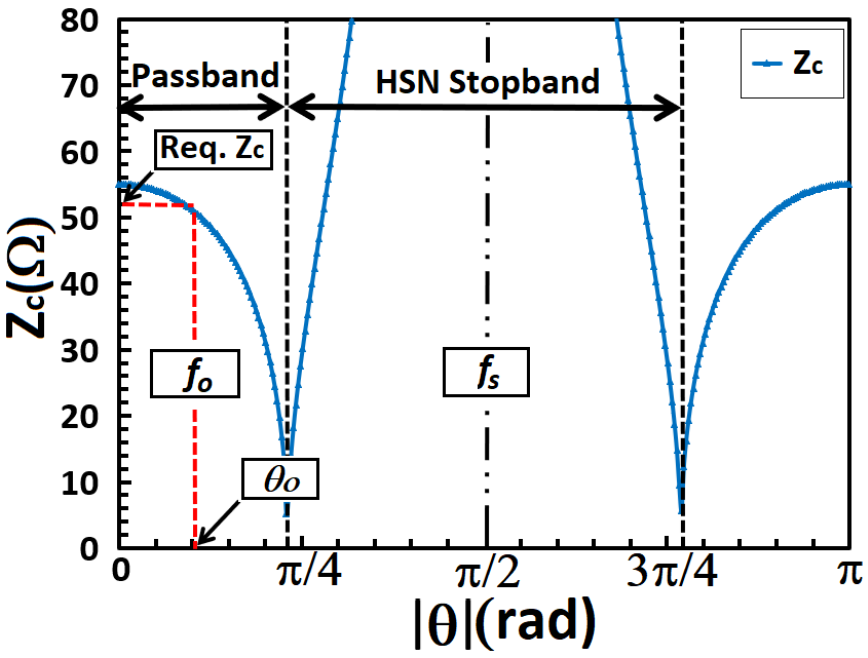

Figure 4-5 The calculated equivalent characteristic impedance of FTCS as a function of the electrical length

4.2.3. Operating principle of the proposed DPA at the fundamental and second harmonic frequency (auxiliary branch)

In this section, a full analysis of the fundamental optimal load of the inverter circuit and the SHIIC, seen by the auxiliary device, is carried out. The equivalent circuit of the harmonic control network (HCN) is shown in Figure 4-6. This equivalent circuit was generated based on the illustrated analysis of the FTCS in the previous section. Two feeding inductors L_f are realized by the symmetric two feeding transmission lines, while the FTCN is synthesized using two coupling

inductors L_e, two substrate's capacitors C_a, and the magnetic paralleled capacitor C_m. The two coupling inductors are mutually cumulatively coupled in a series, and the total inductance of coupled inductors can be calculated as:

$$L_t = 2(L_e + L_m)\ ,\quad L_m = k_m\, L_e \tag{4-17}$$

$$L_t = 2L_e(1 + k_m) \tag{4-18}$$

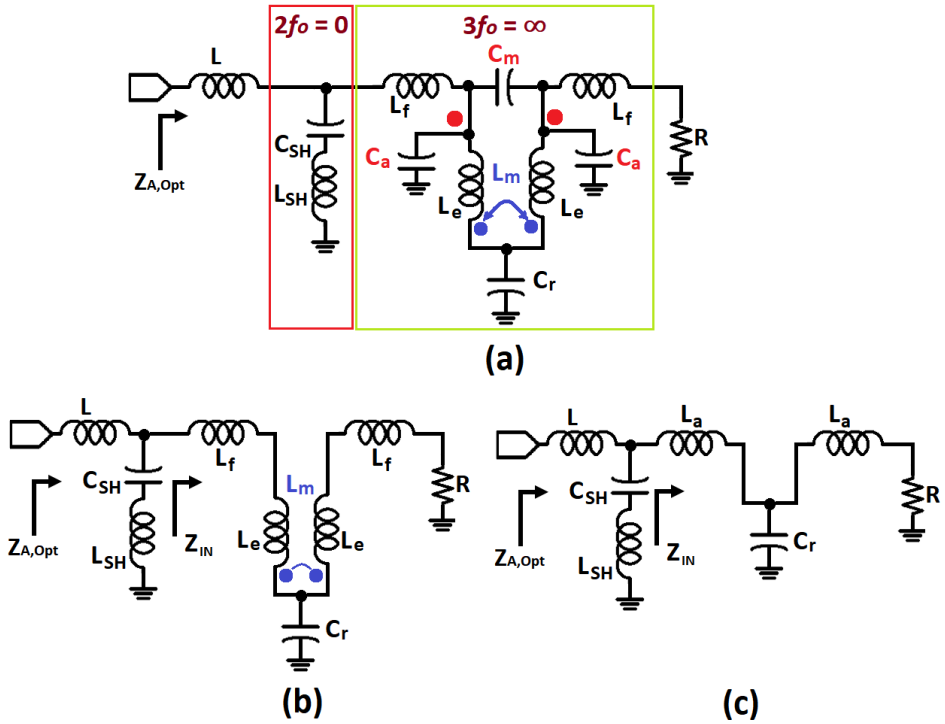

Figure 4-6(a) Full equivalent circuit of HCN, (b) equivalent circuit of HCN without CL substrate capacitances, (c) simplified equivalent circuit of HCN.

The two capacitors C_a are mutually coupled, and their coupled capacitance can be calculated as:

$$C_m = k_e\, C_a \tag{4-19}$$

where k_m and k_e are the magnetic and electric coupling coefficients [86]. An inductor L_a was proposed as a function of L_e in (4-20) to simplify the analysis of the HCN. The value of $2(C_a - C_m)$ is generated by the coupled line's (CL) substrate capacitances and has little effect on the actual design. Therefore, one can neglect its value in the analysis of the HCN's transformed impedance. Then, the capacitor of $C_r + 2(C_a - C_m)$ is simplified to C_r, as shown in Figure 4-6 (b) to avoid highly complex calculations.

$$L_a = L_f + L_t/2 \tag{4-20}$$

$$L_a = L_f + L_e(1 + k_m) \tag{4-21}$$

Consequently, the simplified equivalent circuit of the proposed HCN, as seen by the auxiliary transistor, is a T-type impedance inverter circuit, as in Figure 4-6 (c). The proposed HCN has a wider operating bandwidth than the conventional T-type impedance inverter, due to the magnetic coupling C_m generated by C_a from the coupled line. The input impedance is derived as:

$$Z_{A,Opt} = j\omega L + \frac{1}{\left(\frac{1}{j\omega L_{SH} + \frac{1}{j\omega C_{SH}}}\right) + \frac{1}{Z_{IN}}} \tag{4-22}$$

where,

$$Z_{IN} = j\omega L_a + \frac{1}{\left(j\omega C_r + \frac{1}{R + j\omega C_r}\right)} \tag{4-23}$$

Figure 4-7 and Figure 4-8 show the real and imaginary parts of the transformed impedance to the auxiliary device with different SHSC values at peak power. These figures show that the harmonic load terminations would affect the optimum fundamental load trajectory for the auxiliary device. Consequently, the shunt L-C resonator values of SHSC were chosen from Figure 4-7 and

Figure 4-8 to match the optimum fundamental load trajectory and satisfy the Doherty region's broadband conditions. In the proposed DPA design, the L_{SC} value was selected to be 1.6 nH, while the C_{SC} value was selected to be 2 pF. The values of the harmonic controlling network equivalent circuit are shown in Figure 4-9.

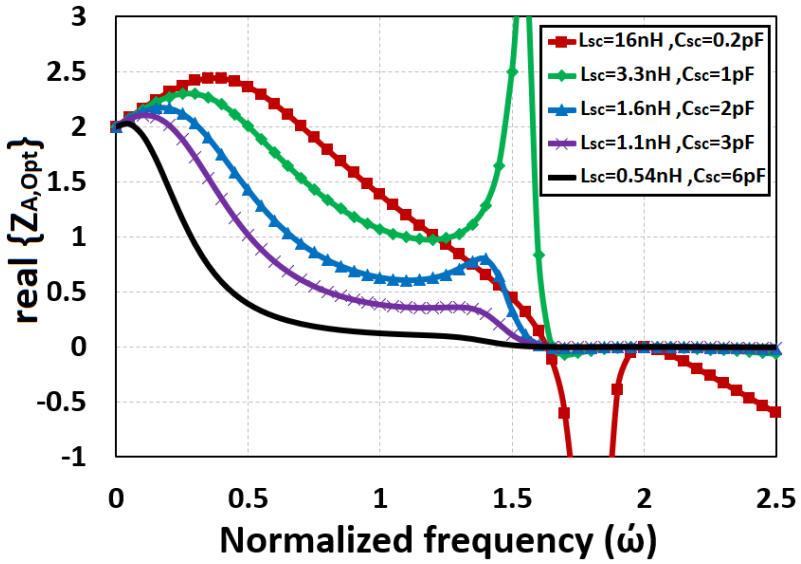

Figure 4-7 The real part of the transformed impedance to the auxiliary transistor with different SHSC configurations at the saturation power level

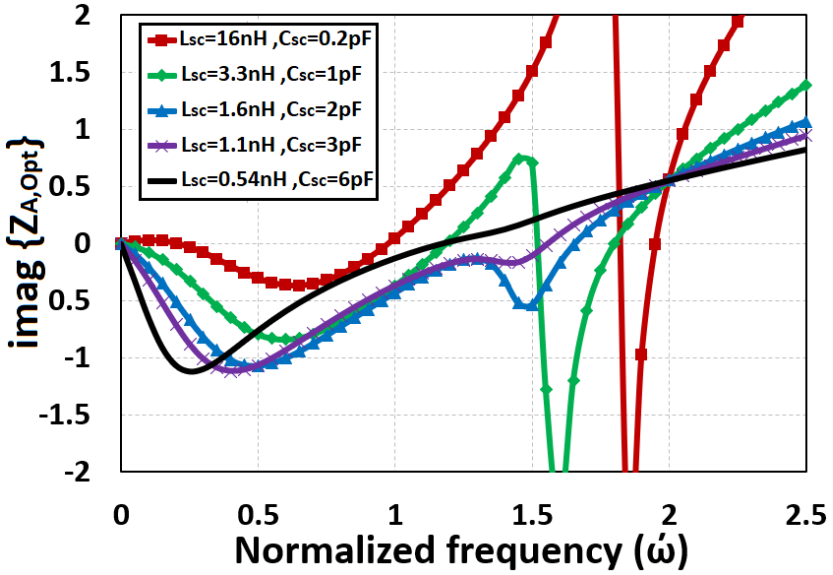

Figure 4-8 The imaginary part of the transformed impedance to the auxiliary transistor with different SHSC configurations at the saturation power level

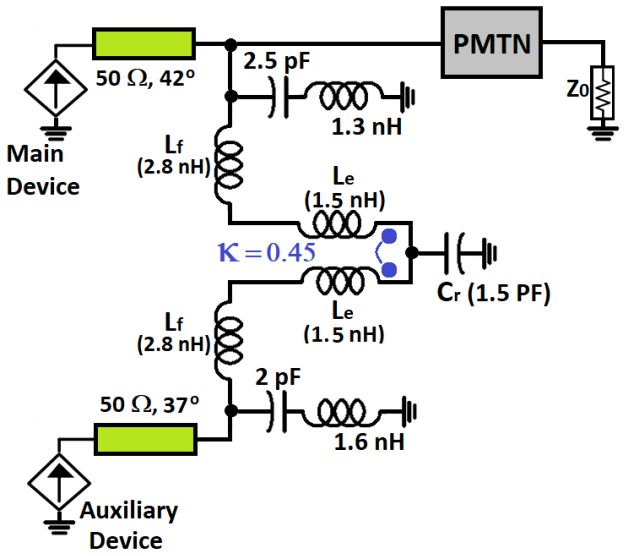

Figure 4-9 The components' values of the HCN equivalent circuit

4.2.4. Synthesis of the post-matching tuning network

The post-matching tuning network (PMTN) can be synthesized to implement the impedance transformation in order to achieve the desired 25Ω fundamental impedance, while simultaneously exhibiting a relatively high impedance at the third harmonics ($3f_o$). The synthesized PMTN and its S_{11} response are shown in Figure 4-10. According to the S_{11} response, it can be concluded that the PMTN can perform the desired impedance matching across the operating bandwidth at fundamental frequencies. Meanwhile, the PMTN controls the third harmonic impedances of the deigned DPA to prevent harmonic power leakage.

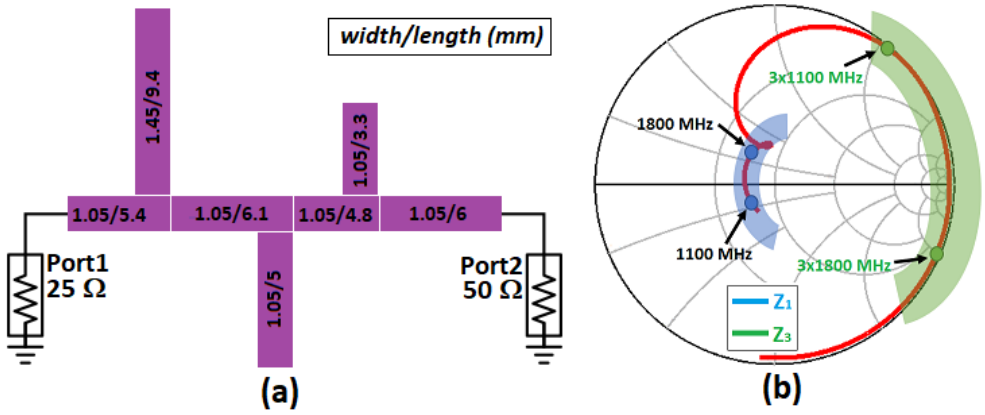

Figure 4-10 (a) Synthesized PMTN, (b) S_{11} of the PMTN on a Z_0 = 25Ω Smith chart

4.3.Prototype Design and Demonstration

In this section, we briefly discuss the design and simulation results of the proposed Doherty amplifier. The theory proposed in Section 4.2 is applied to design the broadband harmonically tuned DPA, working across the frequency band from 1.1 GHz to 1.8 GHz, with a saturation power of 43 dBm and an output power back-off (OPBO) of 6 dB. The DPA is designed using the device model of the packaged gallium nitride (GaN) high-electron-mobility-transistors (HEMTs) CGH40010F from Wolfspeed. The overall circuit schematic of the proposed broadband DPA is displayed in Figure 4-11. The proposed DPA is designed and simulated using the transistor's nonlinear model in Keysight's ADS software. The gate bias voltage of the main transistor was set to -2.8 V (Class AB mode) with a drain current of 86 mA, while the auxiliary transistor bias voltage was set to -5.6 V (Class C mode), and their drain voltages were set to 28 V.

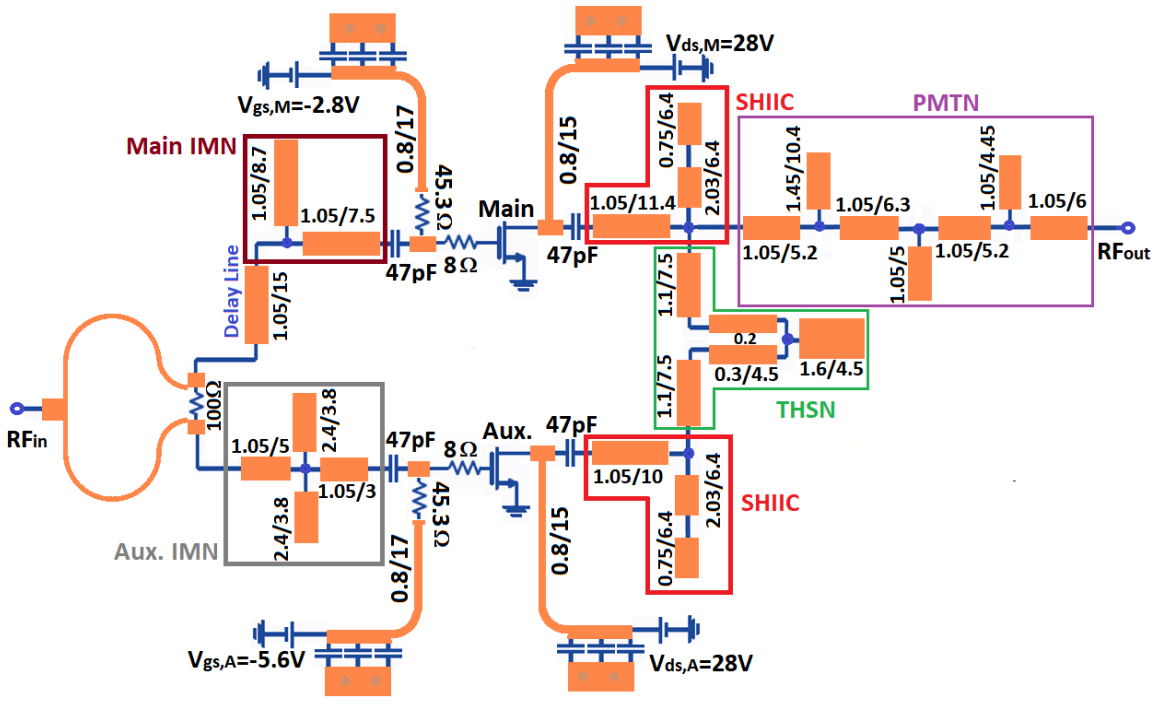

Figure 4-11 Full circuit schematic of the implemented DPA on Rogers 6006 substrate with ε_r = 6.45, the thickness of 0.635 mm and tanδ = 0.0027

The procedures used to design the output harmonic controlling network of the proposed DPA are described in Section 4.2.1. Initially, the design of the SHIIC for the main transistor is carried out, followed by the design of the THSN, and then by the design of the SHIIC for the auxiliary transistor. The above networks are realized using a transmission line (TL) and anti-coupled transmission line structures. The load resistor R_L can further be transformed to 50 Ω using the designed post-matching-tuning network (PMTN), as mentioned in Section 4.2.4.

The input matching network provides a conjugated match by observing the input load conditions with the output combiner attached. For the main and the auxiliary branches, the same transistor is used, so as a result, their stabilization networks are the same. At the input section of the main PA, an additional phase adjustment line is added to compensate for the phase difference between the main and auxiliary branches. The large-signal model of the parasitic and package parameters was presented in [77]. The values of the parasitic and package parameters were used to access the transistors' intrinsic current generator plane, as shown in Figure 4-12.

The designed SHIIC for the main transistor, along with the post-matching-tuning network (PMTN) ensure a short termination of the second harmonic component, and reflects the third harmonic component to the main device drain for waveform shaping purposes, at both the saturation region and back-off region. Moreover, the designed SHIIC associated with the third harmonic suppression network is employed to shape the waveform at the output of the auxiliary device drain. The shaping of the voltage and current waveforms at the current generation plane of the main and auxiliary devices at three frequencies of 1.2 GHz, 1.4 GHz, and 1.6 GHz, within the band is shown in Figure 4-13. From this figure, one can notice that the waveform follows the expected and simulated waveforms of the broadband DPA at the saturation power level and the back-off region corresponding to 36.8-37.5 dBm. The simulated drain voltage waveform appears

as a quasi-square waveform, and the drain current is like a half-sinusoidal waveform. The output drain-source capacitance and package parasitic cause small waveform ripples at the higher-order harmonic components. Furthermore, since the leakage of the third harmonic signal into the PMTN cannot be avoided entirely, the third harmonic load impedance of the main device cannot remain near an open-circuit load condition throughout the entire operating bandwidth.

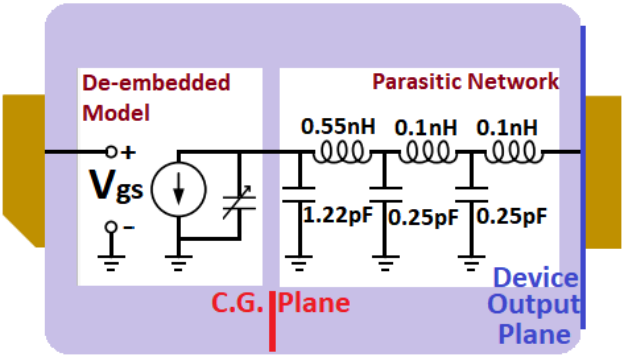

Figure 4-12 large-signal circuit model of CGH40010F device

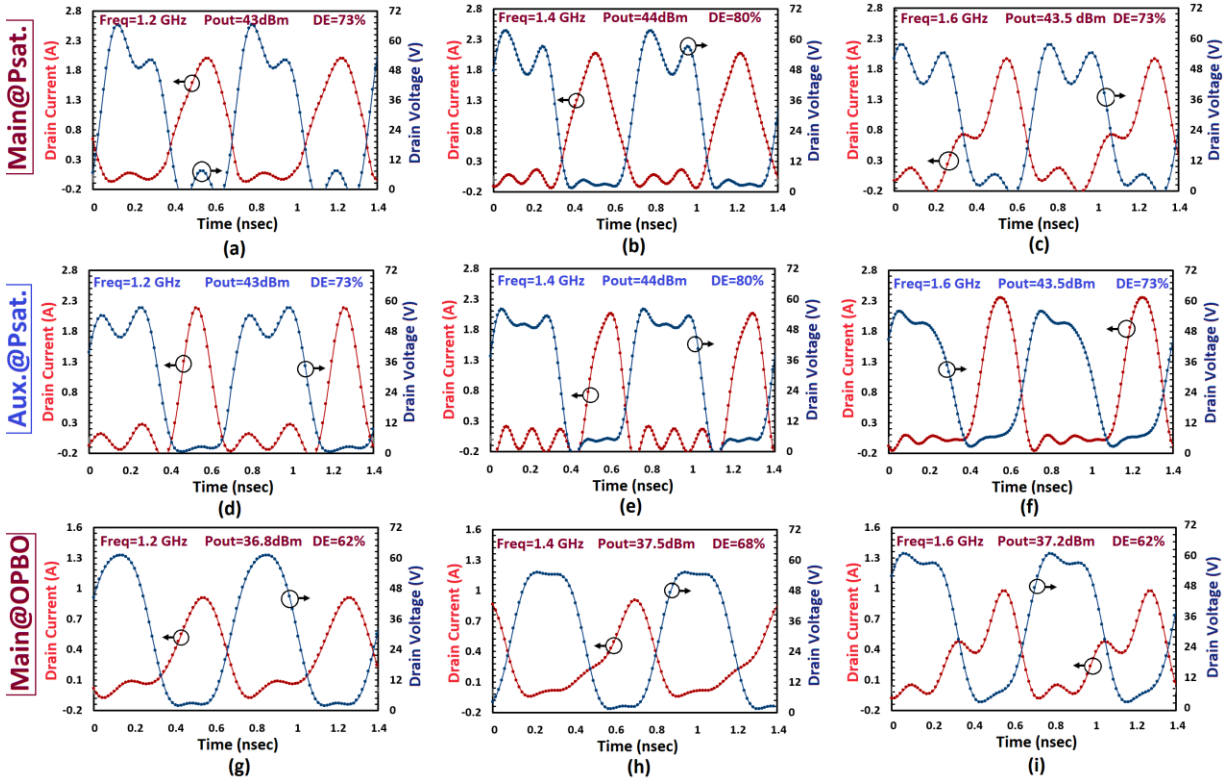

Figure 4-13 Simulated time-domain waveforms of drain voltage and current at the intrinsic current source plane of the main and auxiliary devices

The EM simulation of the entire DPA was performed using ADS Momentum from Keysight. The gate bias of the main device was set to -3 V with the quiescent current 70 mA, while the gate biasing of the auxiliary device was set to -5.6 V. Figure 4-14 presents the simulated drain efficiency and the gain of the proposed DPA, versus the output power. The drain efficiency (DE) at 6 dB back-off is higher than 56% across the targeted frequency band. Moreover, 70% to 82% DE can be obtained at the saturation power level. Also, the DPA achieves gain compression of 2.3 dB to 3.8 dB at saturation.

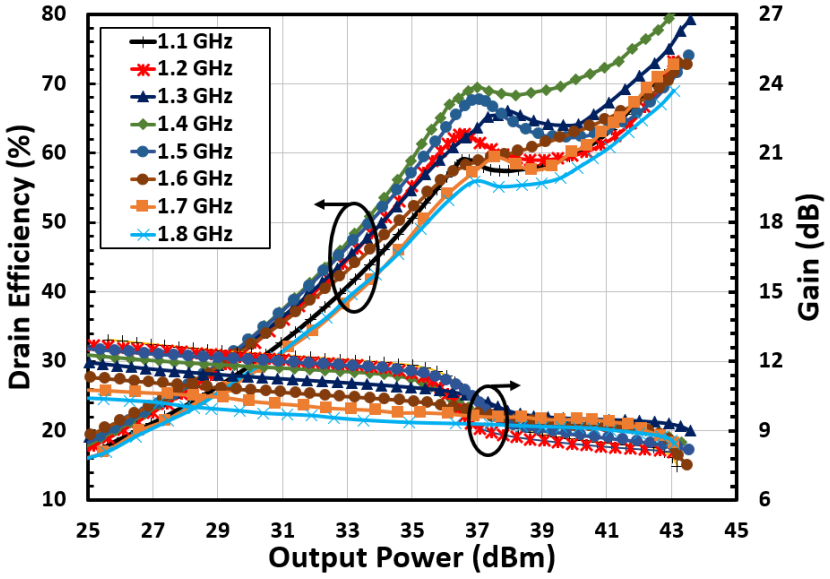

Figure 4-14 Simulated drain efficiency and gain performance of the designed DPA versus delivered output power

4.4.Experimental Results

The photograph of the fabricated DPA, with the measurement setup, is shown in Figure 4-15. The DPA was measured under both continuous wave (CW) and modulated signal at different operating frequencies. Some of the designed frequencies, with a high back-off efficiency shifted slightly from the simulation due to fabrication process variations. The final measured operation

bandwidth was from 1.1 to 1.8 GHz. To show the broadband feature of the implemented DPA, performance at a saturation power level and back-off region were measured across the operating frequency band with a 0.1 GHz step. In the measurements, the DPA had a drain bias of 28 V and the main quiescent current was set to 80 mA, while the auxiliary gate bias was set to −6.3 V.

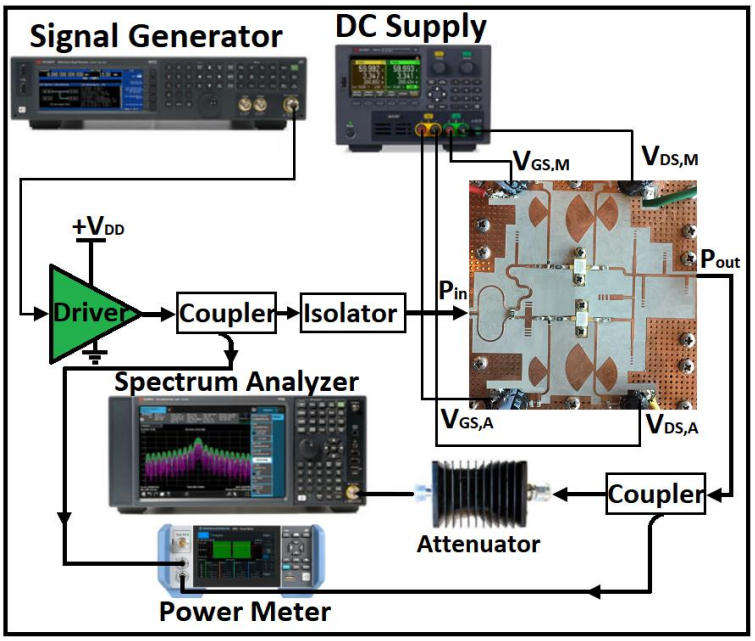

Figure 4-15 DPA fabricated circuit and the measurement setup

4.4.1. Measurement with CW signal

The simulated and measured small-signal gain of the proposed DPA, from 1 to 2 GHz is presented in Figure 4-16, where the behavior of broadband operation can be observed. The measured small-signal gain changes from 8.3 to 11.5 dB in the frequency band from 1.1 to 1.8 GHz. A comparison between the simulated and measured input return loss is also given in Figure 4-16, showing a good matching performance within the operating band.

The measured drain efficiency and the gain of the designed DPA versus output power are shown in Figure 4-17. Drain efficiencies of 65.5% – 78.2% and 52.5% – 67.5% are achieved at

the peak output power and the 6-dB output power back-off region, respectively. The measured maximum output power is more than 43 dBm. From the above CW measurement results, we can state that the designed DPA performs as expected over a wideband operation. The Doherty operation is not obvious at some frequencies around the edge of the operating frequency band. This might be caused by several factors, such as the fundamental impedance mismatch and non-perfect harmonic control. Also, the variation of the DPA gain at different frequencies may lead to an early turn-on of the auxiliary amplifier. In this situation, the main PA has not been driven to voltage saturation at back-off, while the auxiliary PA already begins to generate power. Thus, the back-off efficiency will be reduced to some extent, and the Doherty behavior will become not obvious. Nevertheless, the achieved back-off efficiency is still comparable with other reported broadband DPAs. To better illustrate, the consistency between the simulated and measured broadband performance of the proposed DPA, the drain efficiency (DE), the peak output power, and the gain at 6-dB output power back-off are plotted versus frequency as given in Figure 4-18.

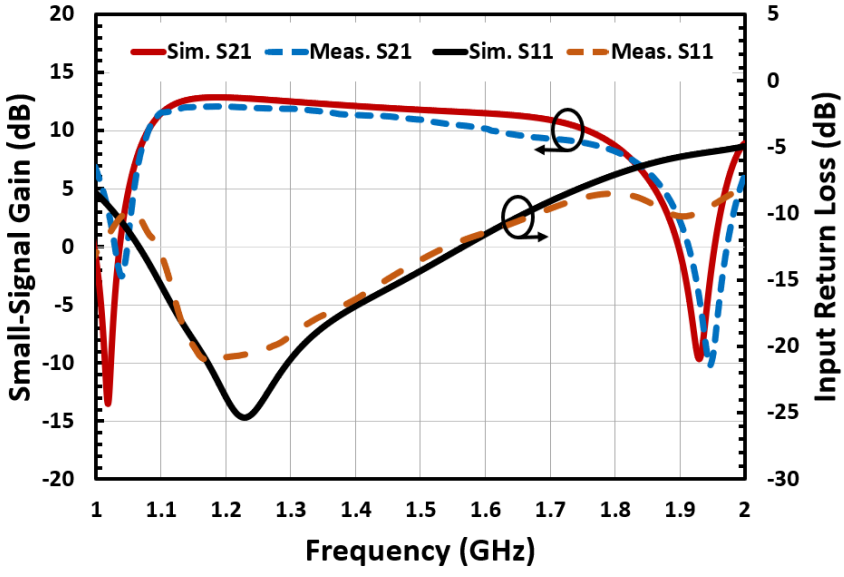

Figure 4-16 Simulated and measured small-signal performance of the fabricated DPA versus operation frequency

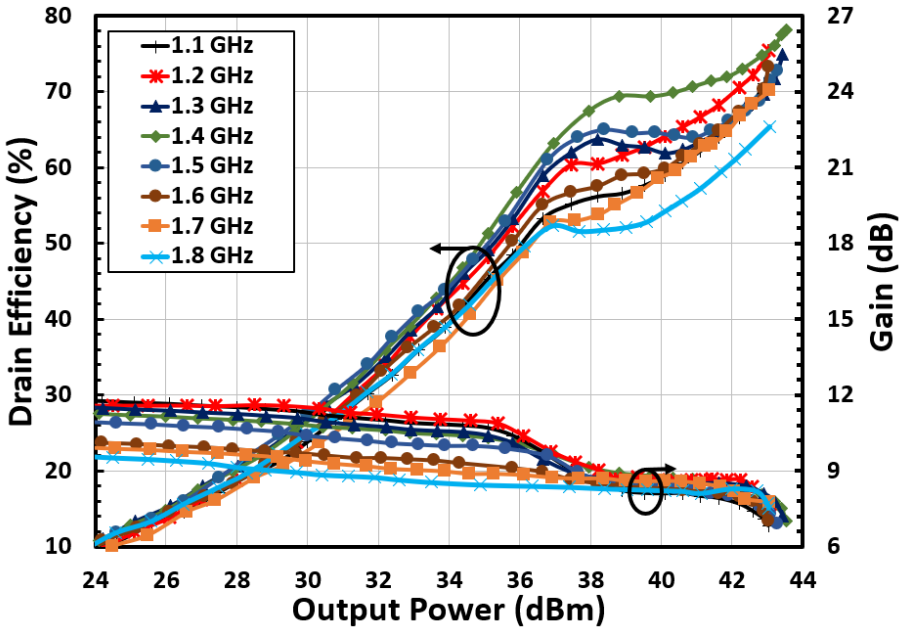

Figure 4-17 Measured drain efficiency and gain performance of the fabricated DPA versus the delivered output power

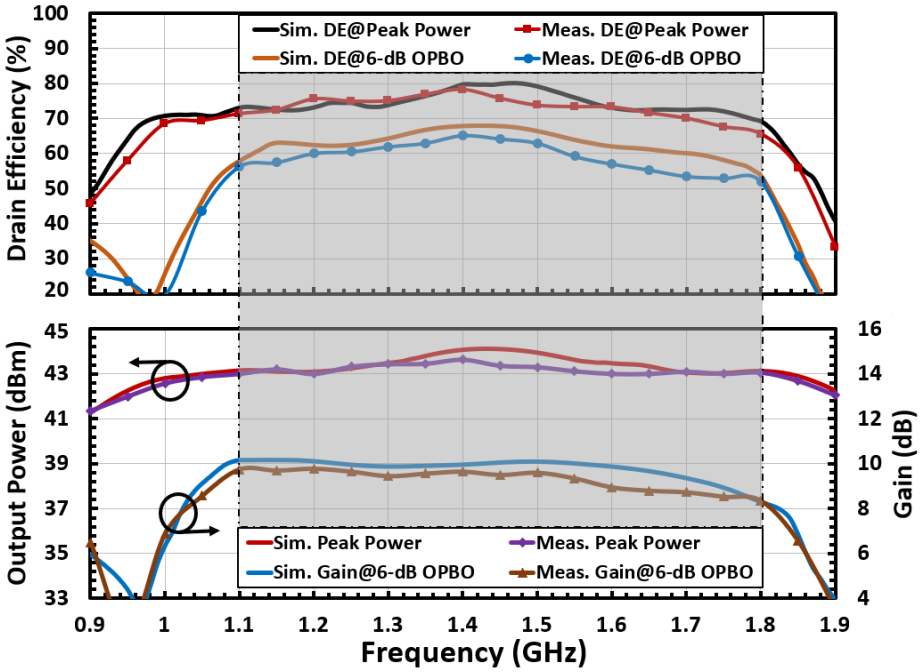

Figure 4-18 Measured drain efficiency and gain performance of the fabricated DPA versus the operation frequency

4.4.2. Measurement with modulated signal

To evaluate the performance of the fabricated Doherty amplifier when driven by a modulated signal, a long-term evolution (LTE) signal having 7.5 dB of PAPR and 20 MHz of bandwidth was employed to test the DPA at 1.2/1.4/1.7GHz, respectively. The power of the LTE signal was swept and the values of the average drain efficiency and adjacent channel power ratio (ACPR) for the designed DPA were obtained and plotted versus output power as displayed in Figure 4-19. The measured ACPR at the average output power of 36.5 dBm changes from –32 dBc to −25.5 dBc. Meanwhile, the measured average drain efficiency of the amplifier was between 48.7% - 59.4% across the whole working frequency band.

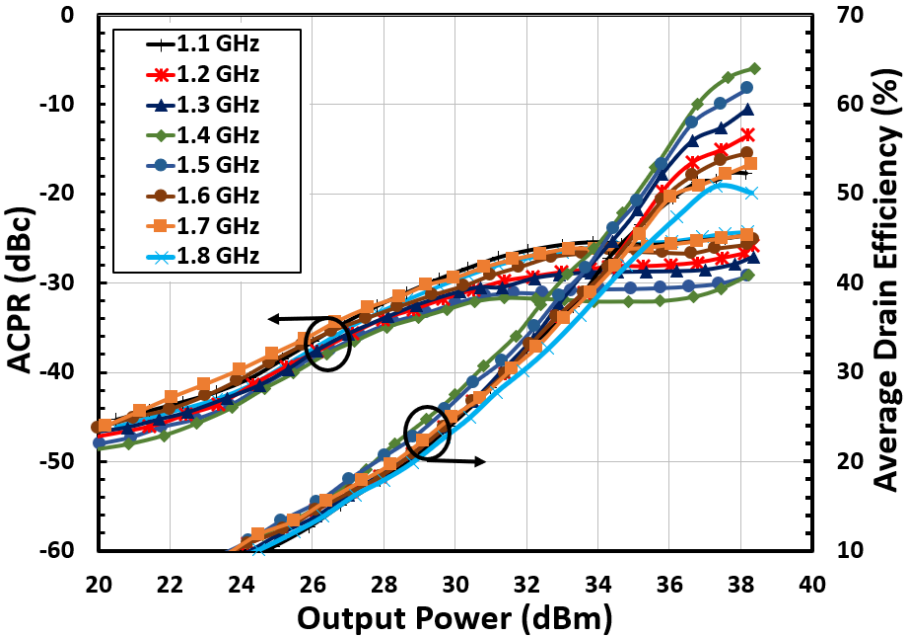

Figure 4-19 Measured average drain efficiency and ACPR versus the output power of the implemented DPA under LTE signal excitation

A digital pre-distortion (DPD) consisting of a lookup table and memory polynomial was performed to linearize the Doherty amplifier. Figure 4-20 displays the output spectrum with, and without, DPD linearization of the DPA under a 20 MHz signal at 1.2, 1.4, and 1.7 GHz. It is clear

from the results in Figure 4-20 that the ACPR, after performing DPD, was improved to more than −49 dBc. Furthermore, the proposed DPA was also measured under a 40 MHz signal with 7.5 dB PAPR at the center frequency. The corresponding output spectrum is shown in Figure 4-21. The measured average drain efficiency under 40 MHz was 54.3%, with 36 dBm average output power. The ACPR was improved from -25.8 dBc to -47.6 dBc. The performance comparison of some recently reported broadband DPAs is summarized in Table 4-2.

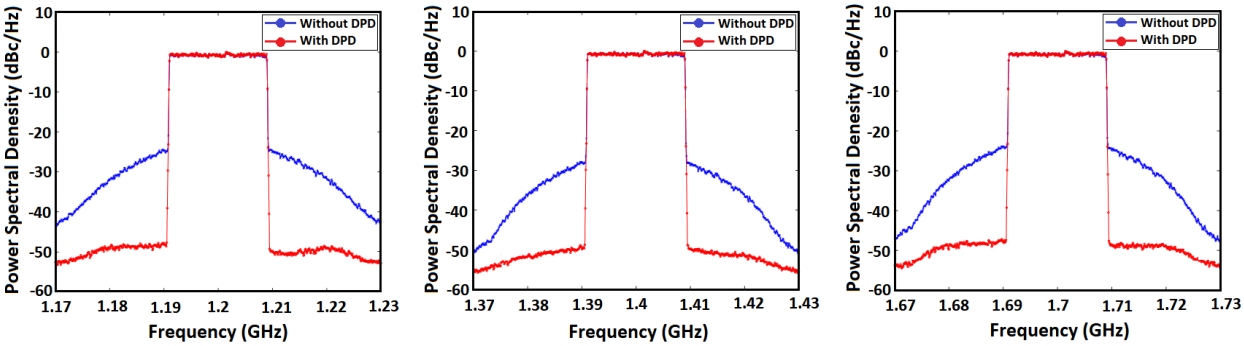

Figure 4-20 Measured output PSD before and after DPD under a 20 MHz LTE signal at 1.2 & 1.4 & 1.7 GHz

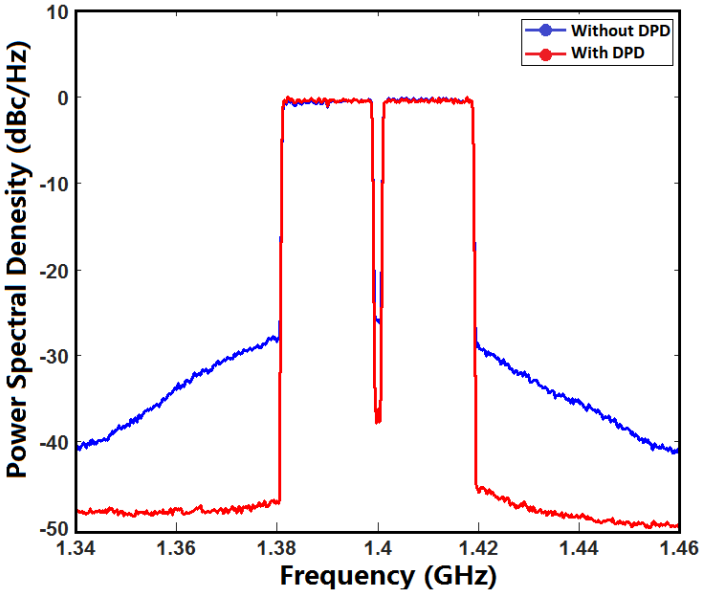

Figure 4-21 Measured output PSD under a 40 MHz LTE signal at 1.4 GHz

Table 4-2 The performance comparison of the proposed and recently reported broadband DPA

Ref.	Freq. (GHz)	OPBO (dB)	CW Signal Measurement Results			Modulated Signal Measurement Results						
			Psat. (dBm)	DE @ OPBO (%)	DE @ Psat. (%)	Signal	Test Freq. (GHz)	Mod. BW (MHz)	PAPR (dB)	Average DE (%)	ACPR without DPD (dBc)	ACPR after DPD (dBc)
[70]	1.5-3.8	6	42.3-43.4	29-49	42-63	WiMax	2.6	7	9	33	-42	-48
[78]	1.7-2.8	6	44-44.5	40	57-71	LTE	1.96-2.14-2.35-2.65	20	6.5	45-54	-34	-50
[71]	1.6-2.7	6	43.8-45.2	46-63	56-75	LTE	2.2	20	7.4	41.5-57.4	-31.7/-26.5	-50.1
[72]	1.8-2.7	6	41	47-54	57-73	WCDMA	1.8-2.7	5	6.5	-	-23/-30	-
[79]	1.7-2.25	6	48.2-49.6	53-65	65-77	LTE	1.85	5	7.3	50	-33	-43
[80]	1.65-2.7	6	43.1-45.2	35-45	56-72	WCDMA	2	5	8.6	37-50	-25/-37	-46
[81]	1.6-2	6	31-34	20-50	47-64	WCDMA	1.73	5	9	40-45	-30/-20	-
This Work	1.1-1.8	6	43-43.6	52-65.2	65.5-78	LTE	1.2 -1.4 - 1.7	20	7.5	50.3-56.6-48.6	-32 / -25.5	-49
						LTE	1.4	40	7.5	54.3	-25.8	-47.6

4.5.Conclusion

In this chapter, a new harmonic control network (HCN) is proposed to design a broadband Doherty power amplifier (DPA). The originality in the DPA design is reflected in the manipulation of the harmonic loading conditions using a new HCN to improve the bandwidth and efficiency. The proposed HCN is an integration between a second harmonic impedance inverter circuit (SHIIC) and a third harmonic suppression network (THSN). The configuration of the SHIIC, with the help of a properly designed post-matching tuned network (PMTN), creates a short-circuit

condition for the second harmonic component for the main transistor. It also reflects the third harmonic component to the main device drain at the saturation condition and back-off region. As well, the modified SHIIC is combined with the THSN to realize a short termination of the second harmonic component and open-circuit load condition for the third harmonic component, as viewed by both the main and auxiliary devices. Hence, a series of highly efficient DPA modes can be created in the entire Doherty region, over a continuous frequency band, leading to a broadband DPA. Based on the proposed topology, an example of a broadband DPA working from 1.1 to 1.8 GHz (48% FBW) was designed. The fabricated DPA exhibits a measured drain efficiency of 52.5–67.5 % at 6-dB output power back-off (OPBO) and 43–43.7 dBm saturated power within the designed bandwidth. When driven by a 7.5-dB peak-to-average power ratio (PAPR) of 40-MHz long-term evolution (LTE) signal, the implemented DPA exhibits 48.7%–59.4% average efficiency. The adjacent channel power ratio (ACLR) was improved from -25.8 dBc to -47.6 dBc after performing digital pre-distortion (DPD).

5. GaN MMIC Low Noise Amplifiers

5.1.Introduction

AlGaN/GaN HEMTs have been considered as a magnet technology for high power microwave electronics. This interest in AlGaN/GaN technology is due to many different reasons. First, the outstanding properties of its material, such as high breakdown voltage and high peak and saturation carrier velocity are of interest. Moreover, the AlGaN/GaN material has good thermal conductivity. In addition to its high-power handling capability, GaN HEMTs are promising for low noise applications, while the noise figure of the GaN process is almost like the GaAs process [82]. LNAs in radar and satellite applications are affected by high input power levels, such as jamming, interferer, or blocker signals. One of the characteristics of LNAs designed using GaN technology is the ability to endure strong power levels compared to GaAs technology. The GaN process has more than a 10 dB increase in power surge survivability, which is better than the GaAs process. In this case, there is no need for limiters to be placed in front of the LNAs due to the inherent robustness of the device [83]. Basically, with this ruggedness, one can eliminate the limiter in front of the LNA, which reduces the losses, and therefore, improves the overall noise figure of the receiving chain and improves the reliability of the RF front-end. These LNAs offer exciting possibilities for a simplified receiver front-end design, since there is no need for any protection circuit that will inherently add noise of 0.5 to 2 dB to the system, as shown in Figure 5-1. From the transceiver design's point of view, the GaN MMIC LNA design simplifies the transceiver design and improves its spurious-free dynamic range (SFDR).

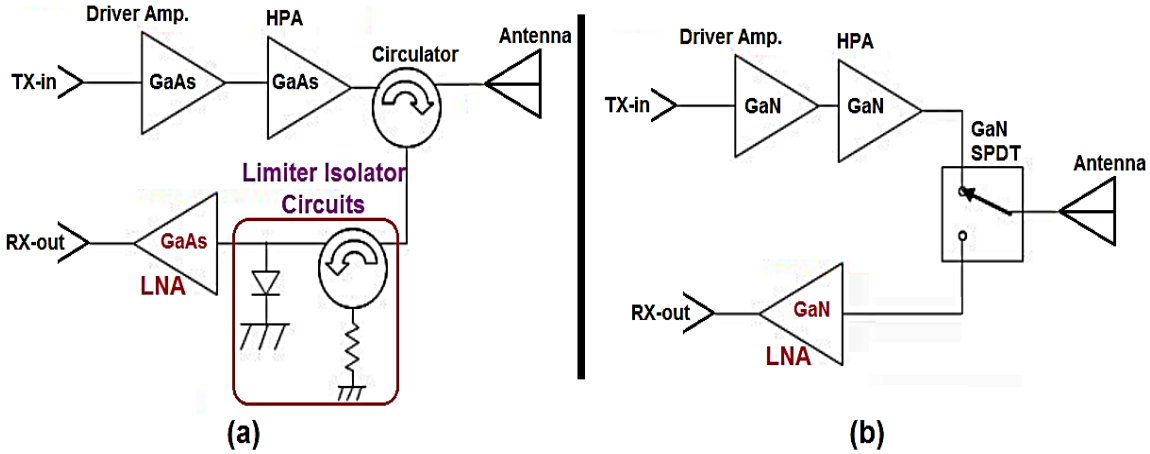

Figure 5-1 Simplified example of (a) GaAs, and (b) GaN-based front-end modules.

5.2.Technology

The GaN MMIC LNA was designed using the UMS MMIC foundry GaN HEMT process. This technology is based on AlGaN/GaN high electron mobility transistors of 250 nm gate length with a slanted profile. Two metallization layers can be used for wiring, metal-insulator-metal capacitors, thin-film resistors, and inductors. The second metallization layer also provides air bridges to overcome topologies and to cross previous structures with low parasitic capacitance. The technology targets the design of monolithic integrated, robust, low power MMICs, and multi-stage high power high-efficiency amplifiers up to 20 GHz. The AlGaN/GaN material is formed by a metal-organic chemical vapor deposition (MOCVD) active layer on four semi-insulating SiC substrates with high uniformity.

5.3. Single-stage LNA design

The LNA is designed based on common-source topology, with a series inductive source, and using R-C feedback network. First, the LNA is designed based on a linear noise model from the United Monolithic Semiconductors (UMS) Process Design Kit (PDK). This model allows simulating and optimizing the LNA design using different transistors sizes with different gate

widths. The most appropriate device size and biasing point were selected to strike a trade-off between the maximum available gain (MAG) and minimum noise figure, such that the specifications of the LNA will meet. Also, we paid special attention to make the design unconditionally stable over the entire frequency band. The Simulated MAG and minimum NF at different transistors' sizes are shown in Figure 5-2.

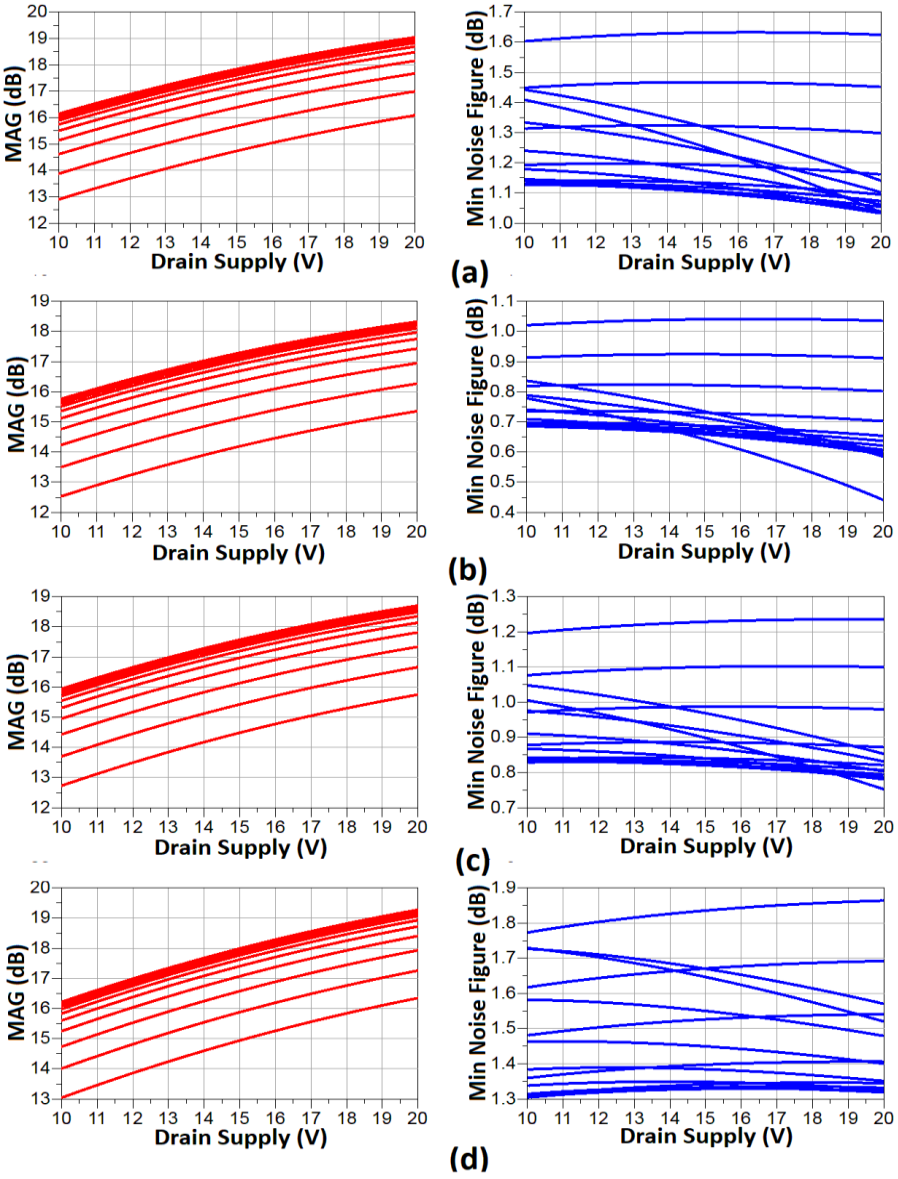

Figure 5-2 Simulated MAG and minimum NF at different transistors' size (a) 2 x 100 um, (b) 4 x 75 um, (c) 6 x 100 um, and (d) 8 x 150 um

Based on the results of Figure 5-2, the single-stage amplifier using a HEMT GaN device of 4-finger of 75 um gate width (300 um total periphery), biased at 16V and 150-mA/mm current density (45 mA total current) was selected. The LNA is designed based on a common-source amplifier topology, with series inductive source feedback at an operating frequency of 5.4 GHz. The R-C feedback function is to maintain the stability of the circuit, in addition to enhancing the gain bandwidth. A simplified circuit schematic of the proposed LNA is shown in Figure 5-3.

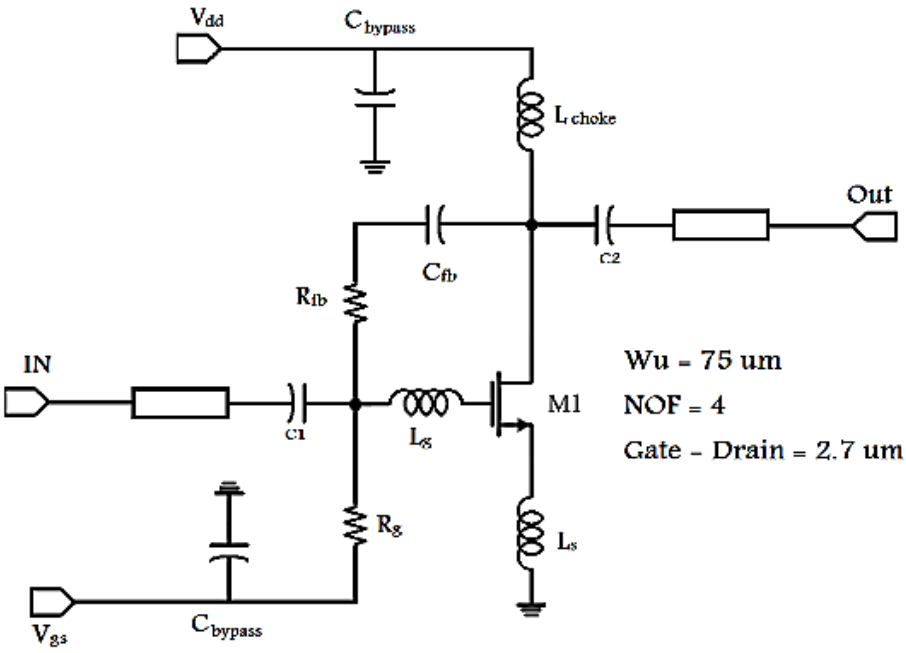

Figure 5-3 Simplified schematic of the GaN MMIC LNA design

An inductive source degeneration technique is used to minimize additional noise generation from the device input parasitics. Also, the use of the gate inductor reduces the effect of the input parasitic capacitance on the noise figure and provides a good matching at the input of the LNA. The optimum noise figure might happen at any input impedance, not necessarily 50 Ω. Also, the input impedance of the transistor is dominated by C_{gs} and contains no real part. The series inductor L_s is placed at the source of the transistor to facilitate the LNA matching. The inductor

appears in series with the C_{gs} and therefore, is directly added to the input impedance. The other effect of the inductor L_s is to provide an effective resistive input without contributing additional noise. The other advantages of adding the inductor are that the noise factor does not change, and the optimum noise impedance is closer to the input impedance of the transistor. The gate inductor L_g is used for both input impedance power matching network and to optimize the noise figure. The inductor L_g, in series with the gate of M1 significantly enhances the bandwidth. Figure 5-4 shows the intrinsic equivalent parameters, gate-source capacitance C_{gs}, and transconductance g_m for the selected transistor with a gate width of 75 μm. At the input network, the device is matched to its optimum noise matching admittance Y_{opt}. This can be expressed as follows:

$$NF = NF_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2 \tag{5-1}$$

where Y_{opt} is the optimum source admittance, Y_S is the source admittance presented to the transistor, and NF_{min} is the minimum noise figure of the device that is accomplished when Y_S equals Y_{opt}. R_N is the equivalent noise resistance of the transistor, and G_S is the real part of the source admittance. The input impedance can be expressed as:

$$Z_{in} = mZ_{fb} \parallel \left(\frac{1}{j\omega C_{gs}} + j\omega\left(L_s + L_g\right) + \frac{g_m L_s}{C_{gs}}\right) \tag{5-2}$$

Where m is Miller's multiplication factors.

$$Z_{fb} = R_{fb} + \frac{1}{j\omega C_{fb}} \tag{5-3}$$

For input matching, the real part of the input impedance should be equal to the source resistance Zo. This can be expressed as:

$$Z_o = real(Z_{in}) \tag{5-4}$$

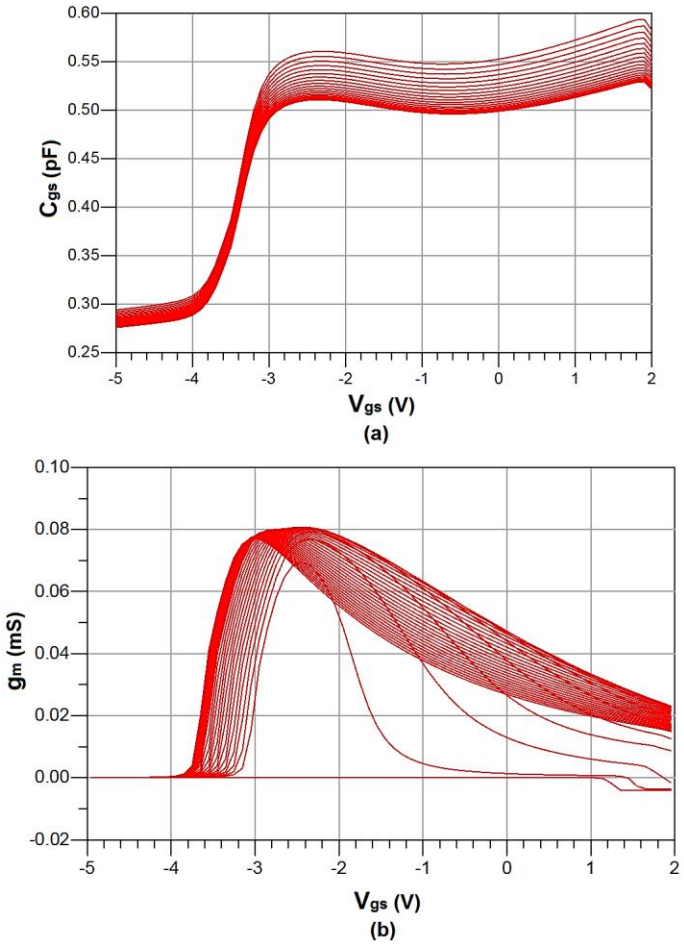

Figure 5-4 Extracted intrinsic equivalent parameters by sweeping V_D from 0 to 30 V: (a) gate-source capacitance C_{gs}, (b) transconductance g_m

To implement the LNA design, the source impedance is chosen for minimum noise factor, and the load impedance is a conjugate match to achieve maximum gain. Both the input matching and output matching networks are based on L–C Circuit. The two capacitors are used in the RF

signal matching to the 50 Ω terminal and as DC blocks, while transmission lines, as a part of the biasing networks, realize the inductors. All the inductors used in the circuit, the input matching network (IMN) and output matching network (OMN) are realized using transmission lines. The bypass capacitor in the biasing networks is replaced by two capacitors in parallel to prevent any resonance in the operating frequency band, and they are also used to filter the RF signals. Figure 5-5 shows the circuit layout of the GaN MMIC LNA. A yield analysis simulation was performed on the full MMIC LNA to check the process performance uniformity and the robustness of the designed LNA. The deviation performance of the gain, flatness across the operating bandwidth, and the noise figure is displayed in Figure 5-6. Using 2500 trials, the circuit analysis shows that the yield for a gain greater than 14 dB, is 70% associated with 75% success yield for gain flatness less than 0.5 dB, while the yield for NF less than 1.6 dB is 85%.

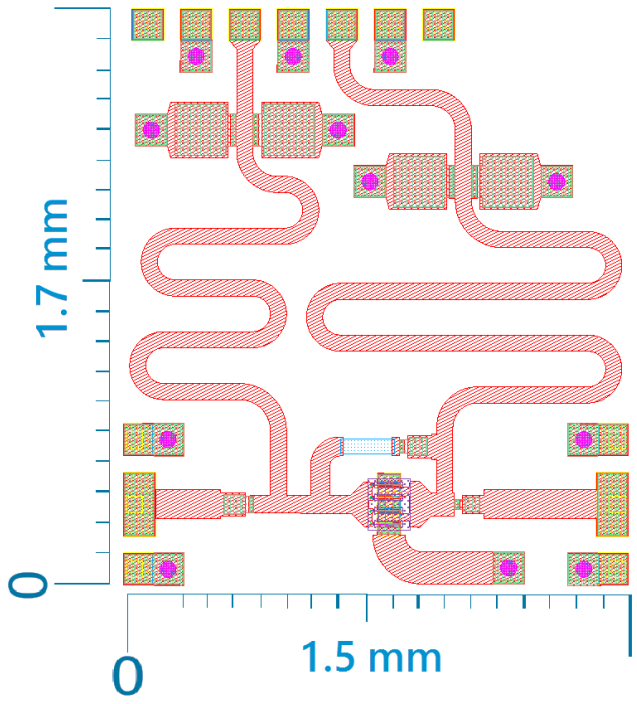

Figure 5-5 Circuit layout of the GaN MMIC LNA

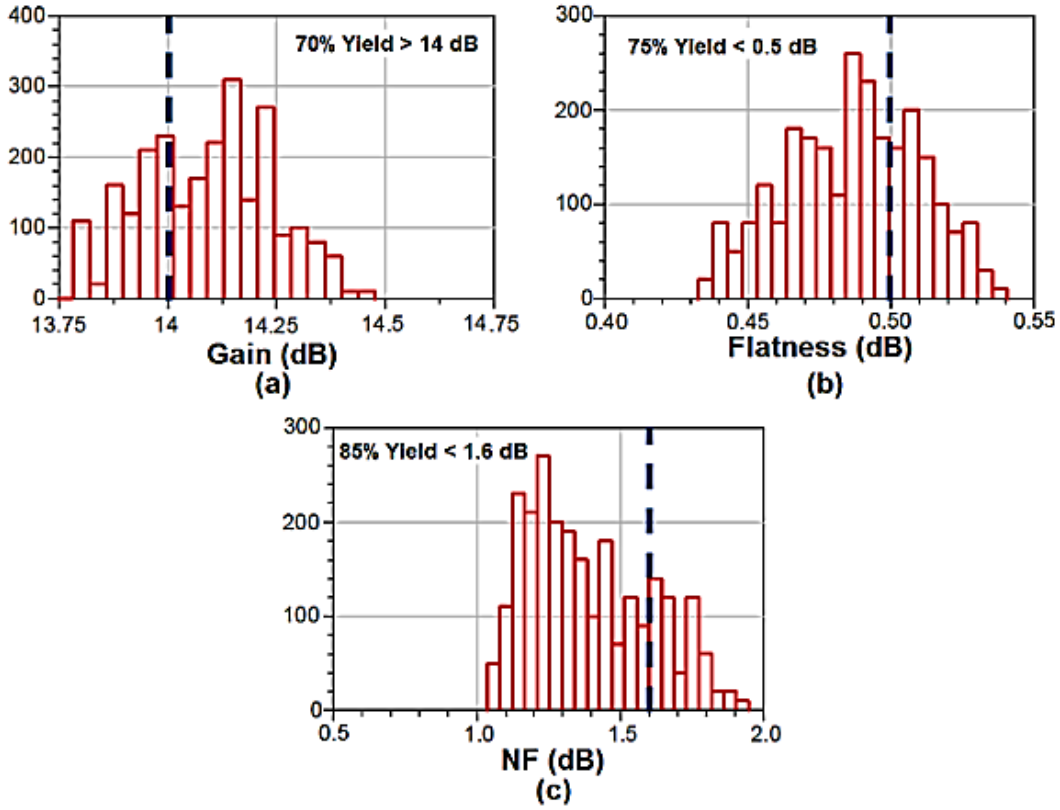

Figure 5-6 MMIC LNA variations, due to the yield process dispersion of (a) gain, (b) flatness, and (c) noise figure

5.4. Single-stage MMIC LNA performance

The single-stage MMIC LNA was designed and fabricated using a 0.25 um UMS GaN-HEMT process. A microscopic photo of the fabricated LNA IC on the wafer is displayed in Figure 5-7. In the design work, a compact layout was tailored, resulting in a chip with full size of 1.5 mm × 1.7 mm.

5.4.1. Gain, matching, and noise performance

As shown in Figure 5-8, the fabricated LNA has a measured noise figure of 0.9 dB at the operating frequency of 5.4 GHz. Figure 5-9 shows that the LNA is unconditionally stable over the entire frequency range from 0 to 7 GHz. Measured S-parameters of the low noise amplifier is

shown in Figure 5-10. For nominal operation at Vds = 16 V and Vgs = -2.8 V, the input return loss is -15 dB, and the output return loss is better than -26 dB within the operating center frequency, with an associated gain of 14 dB. The LNA exhibits a broadband operation from 4.5–6.5 GHz with a noise figure of less than 1.5 dB. The device has an input return loss of -10 dB to -17 dB and an output return loss of -10 to -30 dB. The small-signal gain of 13.4 dB to 14 dB was achieved across the whole frequency band.

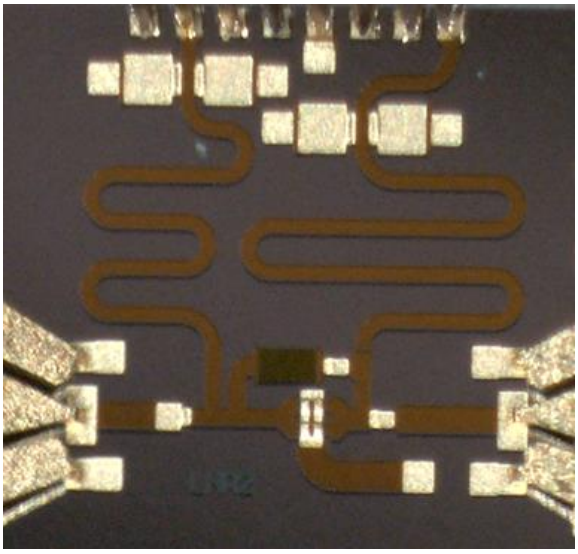

Figure 5-7 Die photograph of the designed LNA

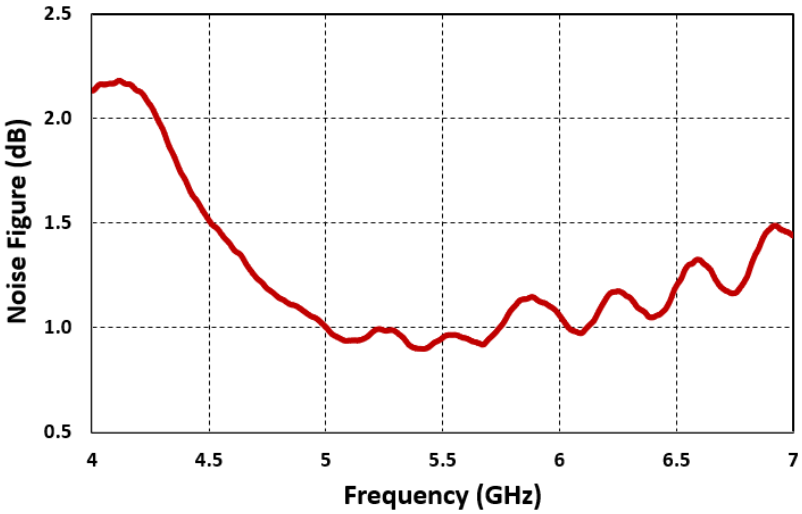

Figure 5-8 Noise figure performance for the proposed LNA

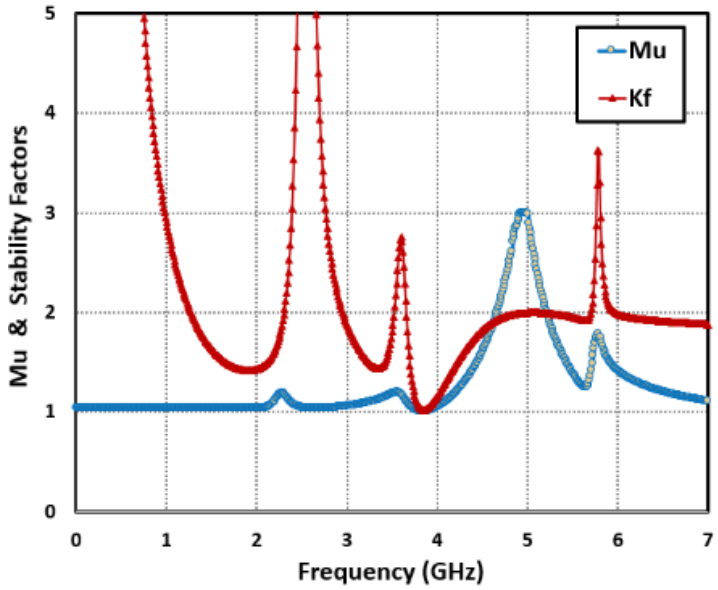

Figure 5-9 Stability behavior of the proposed LNA

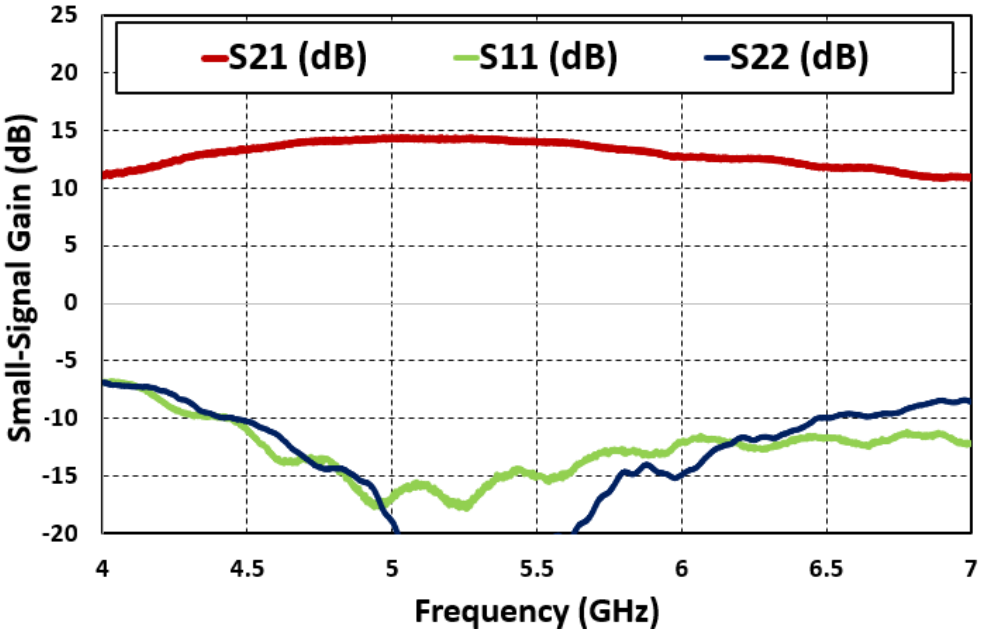

Figure 5-10 S-parameters of the GaN MMIC LNA

5.4.2. Large-signal performance

In this section, the large-signal performances of the proposed LNA are illustrated. These power characteristics are based on the non-linear hot model of the GaN device. Simulated power, gain, and power-added efficiency (PAE) results from the LNA versus the input power are shown in Figure 5-11. The input power sweeps from -5 to 25 dBm at the operating frequency of 5.4 GHz. The maximum power-added efficiency (PAE) for this topology is 41.7 % and it occurs at an output peak power of 28.6 dBm (0.8 Watt). Moreover, it is seen that the P_{1dB} compression point happens at an input power level of 9 dBm, while the P_{3dB} compression occurs at an input power level of 16 dBm for this LNA topology. The measured power sweep curves are shown in Figure 5-12. In this figure, we compare the simulated and measured characterization results.

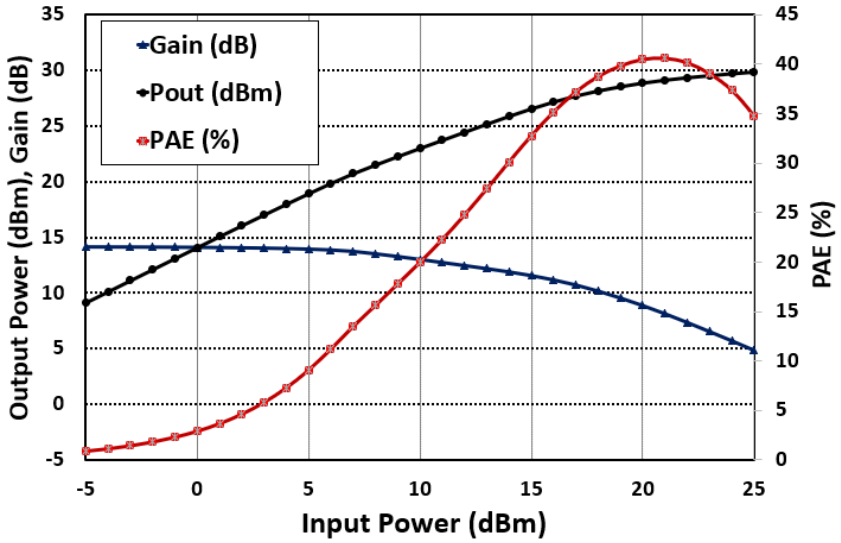

Figure 5-11 Simulated large-signal performance at 5.4 GHz

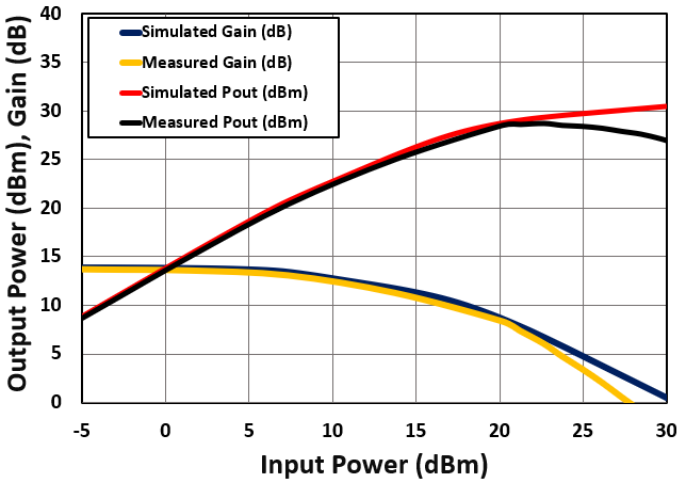

Figure 5-12 Measured large-signal performance at 5.4 GHz

5.4.3. Linearity performance

The IP3 measurement was performed using a two-tone RF signal with a spacing of 10 MHz, where the first tone was fixed at the operating frequency of 5.4 GHz. The biasing conditions remained in the large signal characterization. An outstanding linear performance was obtained, as shown in Figure 5-13. The OIP3 is better than 35 dBm in the linear region, while the input IP3 is 23 dBm. At the P1dB compression point, the OIP3 is about 32.6 dBm as displayed in Figure 5-14. The proposed GaN LNA shows a very high-dynamic range with a high gain and low noise performance.

Figure 5-15 displays the third-order intermodulation difference (IMD3) plotted against the output power of the two-tone test. The plot indicates that the IMD3 of the designed MMIC LNA is -23.5 dBc at the 1dB compression point. It is worth noting that the power in both sidebands (i.e., upper and lower sidebands) is almost equal, which indicates that quasi-no memory effects are generated. Table 5-1 summarizes the comparison of the proposed MMIC LNA with other previously reported LNAs, according to the measured parameters as well as the process technology.

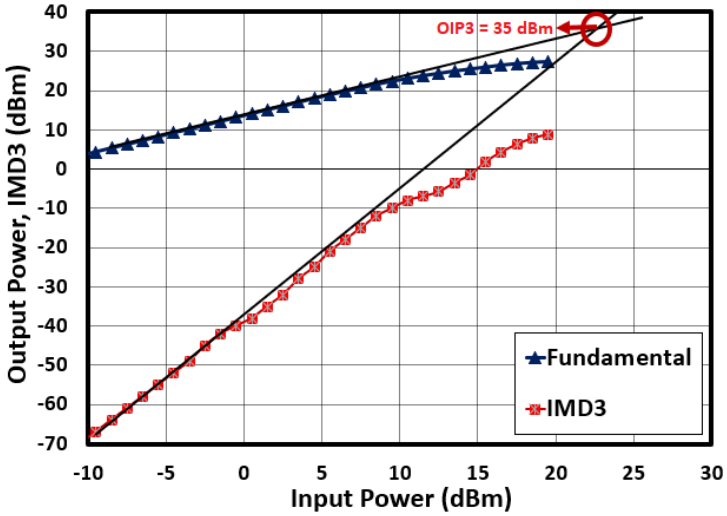

Figure 5-13 Measured linearity performance of the proposed GaN LNA

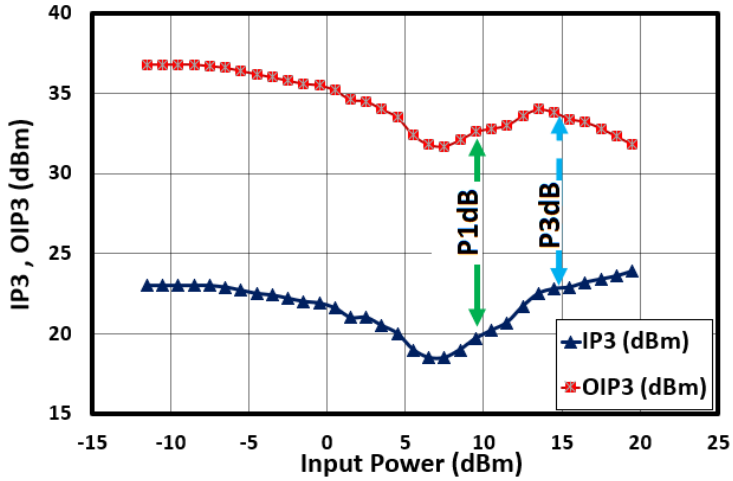

Figure 5-14 Measured IP3 and OIP3 versus power sweep

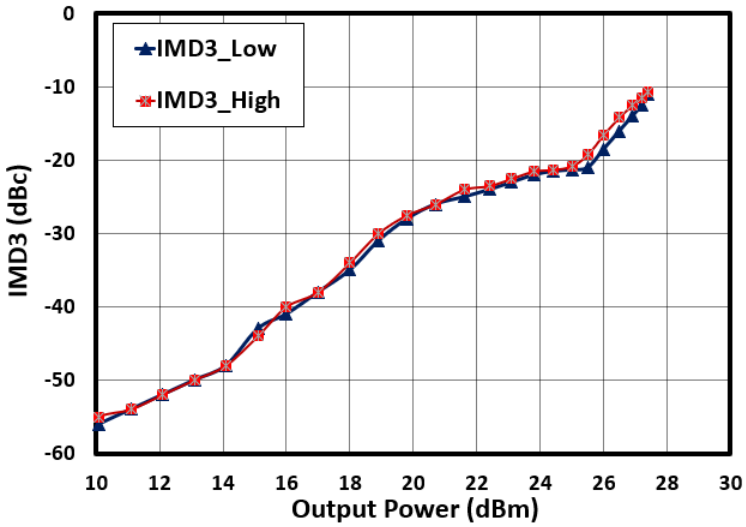

Figure 5-15 Measured IMD3 of the MMIC LNA

Table 5-1 The performance comparison with recently published LNAs

Ref.	Process	Freq. (GHz)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)	P1-dB	OIP3 (dBm)
[84]	GaN HEMT	7 - 11	18	-	-	1.8 – 2.4	-	-
[85]	GaN HEMT	8 - 11	21	10 - 15	10 - 22	1.7 – 2.3	15	-
[86]	GaN HEMT	5 - 6	12	7 - 14	-	5.5	-	-
[87]	GaN HEMT	2 - 5	17.4	7 - 10	15 - 20	1.5 - 2	20	-
[88]	GaN HEMT	8 – 10	18	5 - 10	5 – 20	2.5 - 3	-	37
[89]	SiGe HBT	1.1 – 1.6	13	9 - 11	8 - 12	0.8 – 0.9	-	-
This Work	GaN HEMT	5 – 6	14	12 – 17	14 - 30	0.9 – 1.3	20	35

5.4.4. Overdrive analysis

One of the essential aspects of a GaN low noise amplifier is its ability to sustain substantial RF input power. To assess the circuit performance under overdrive, we apply a CW tone at the operating frequency 5.4 GHz to the LNA from 0 dBm to 40 dBm. According to the technology, the maximum ratings for different transistors under recommended operating rating DC bias conditions are V_{dg} = 80 V and V_{gs} = -20 V. Therefore, under these conditions, an overdrive analysis was done on the designed LNA, and these results are displayed in Figure 5-16. These curves indicate that the proposed LNA can operate normally up to RF input power of 28 dBm.

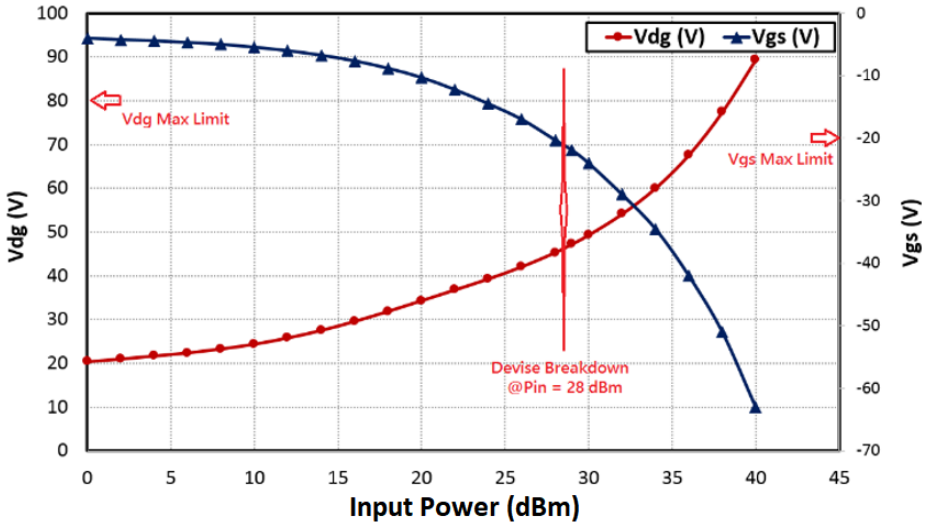

Figure 5-16 Overdrive analysis versus power sweep

5.5. Survivability analysis of the designed LNA die

This section presents a detailed results analysis of the survivability study, stressing the performance degradation of the fabricated GaN MMIC LNA, operated at high over-drive input power levels. The survivability is defined as the input power where LNAs start to demonstrate permanent and non-recoverable damage, in terms of loss of gate control and increased leakage currents. The recovery time is the time the LNA takes to return to its normal performance after stressing the device with high input signal levels. The GaN MMIC LNA was stress-tested to assess the LNA ruggedness behavior. The survivability was characterized under input overdrive conditions with a CW input RF signal at 5.4 GHz. The input power was swept stepwise from 31 dBm to 36 dBm. After each stress, the LNA performance (gain and NF) and dc characteristics (Ig and Id) were measured to check the functionality of the LNA.

Noise figure (NF) and S-parameters of the LNA were measured on-wafer, at room temperature of 21 °C, at a low power drive between 5.0 GHz and 5.8 GHz; the results obtained are used as reference measurements for the stress test results. The LNA die was stress-tested, and their respective S parameters and NF were measured over the frequency range prior, immediately post-stress test, and after a 6-hour recovery time. This stress test was performed by driving continuously, for 16 hours, the LNA under test, with high input CW drive level at a frequency range of 5.4 GHz. First, 31 dBm was applied for 16 hours, followed by 6 hours of recovery time. Then, small-signal gain and noise's performance were measured after the 6-hour recovery period. This process is repeated at input power levels of 32 dBm, 33 dBm, 34 dBm, 35 dBm, and 36 dBm. We assessed the performance of the LNA being tested using its small-signal gain and its noise figure directly after power stress and after a recovery period at each power level. The gate and drain currents were monitored during the stress time, while the LNA was being tested.

The goal of this test was to assess the LNA robustness against overdriving conditions for a relatively long time (16 Hours) and assess the device's small-signal and noise performance after the recovery period. Since the input power level limit for a non-permanent damage operation was determined to be 1-Watt (30 dBm), which was deduced from the previously carried out investigation of the LNA robustness to overdrive conditions, the power range of survivability investigation will cover 31 dB to 36 dBm range with an increasing step of 1 dB. The maximum input power limit is dictated by the maximum power rating of the probes used (Model: ACP40-L-GSG-200) of 38 dBm. Intentionally, a margin of 2 dB was kept, safeguarding the operation and performance of the probes.

5.5.1. Small-Signal gain performance

The small-signal gain of the GaN MMIC LNA was measured on-wafer at room temperature. The LNA was also stress-tested, and its parameters were measured before and post-stress test. This stress test was performed by injecting high input CW powers at a frequency of 5.4 GHz in a 50- system. First, 31 dBm was applied for 16 hours, and then the gain was measured directly after this period. Then, the small-signal gain performance was measured after a 6 hour recovery period. This stressing condition is among the most severe reported in the literature [88], [90], due to its high-power level, long duration, and verification of robustness by post-stress noise measurement. The stress-test process is repeated at input power levels of 32 dBm, - 33 dBm, - 34 dBm, - 35 dBm, - 36 dBm. The small-signal gain results of the fabricated LNA at different power levels are shown in Figure 5-17, Figure 5-18, Figure 5-19, Figure 5-20, Figure 5-21, and Figure 5-22. Table 5-2 illustrates the difference in the measured small-signal gain at different input power and different conditions.

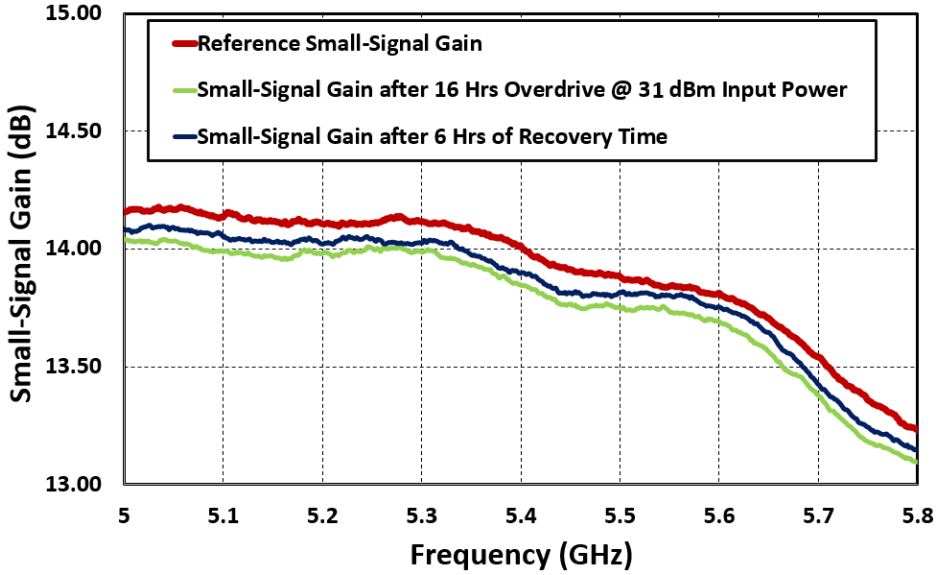

Figure 5-17 Measured small-signal gain : (reference gain, post 16 Hrs @ Pin 31 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA)

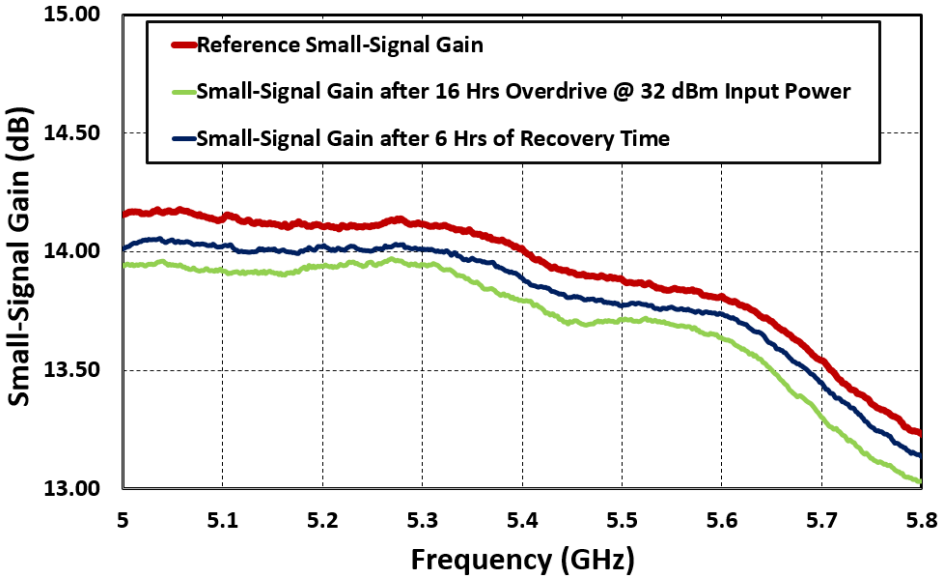

Figure 5-18 Measured small-signal gain : (reference gain, post 16 Hrs @ Pin 32 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA)

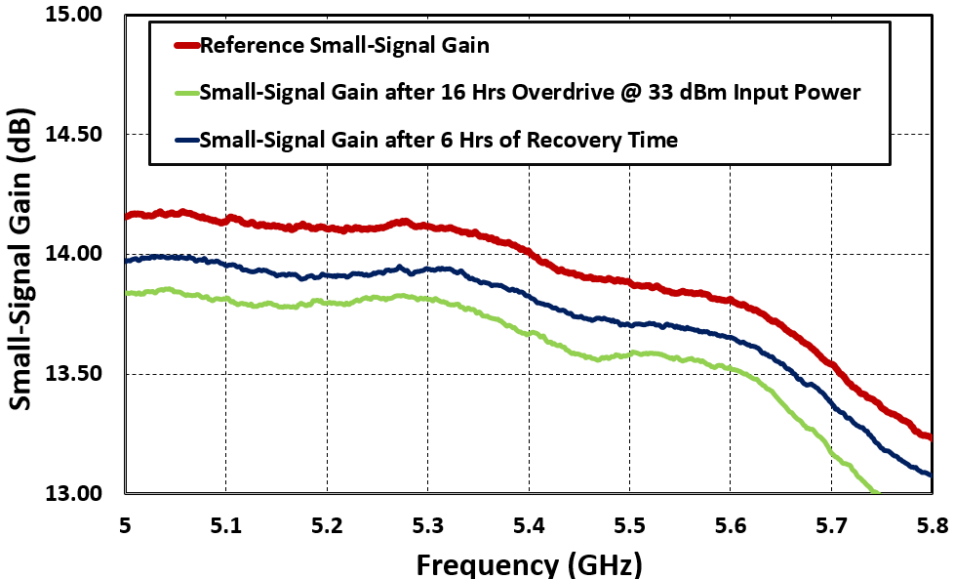

Figure 5-19 Measured small-signal gain : (reference gain, post 16 Hrs @ Pin 33 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA)

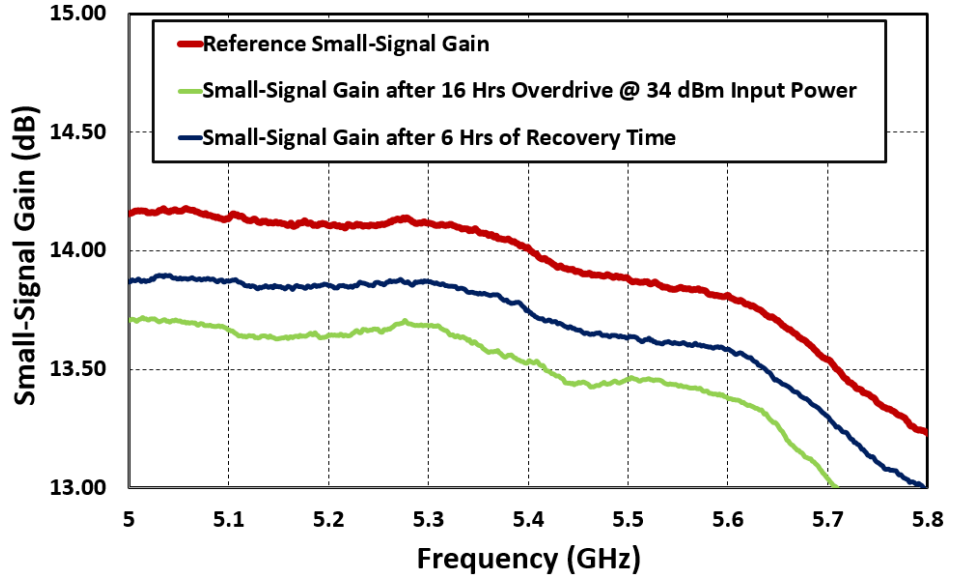

Figure 5-20 Measured small-signal gain : (reference gain, post 16 Hrs @ Pin 34 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA)

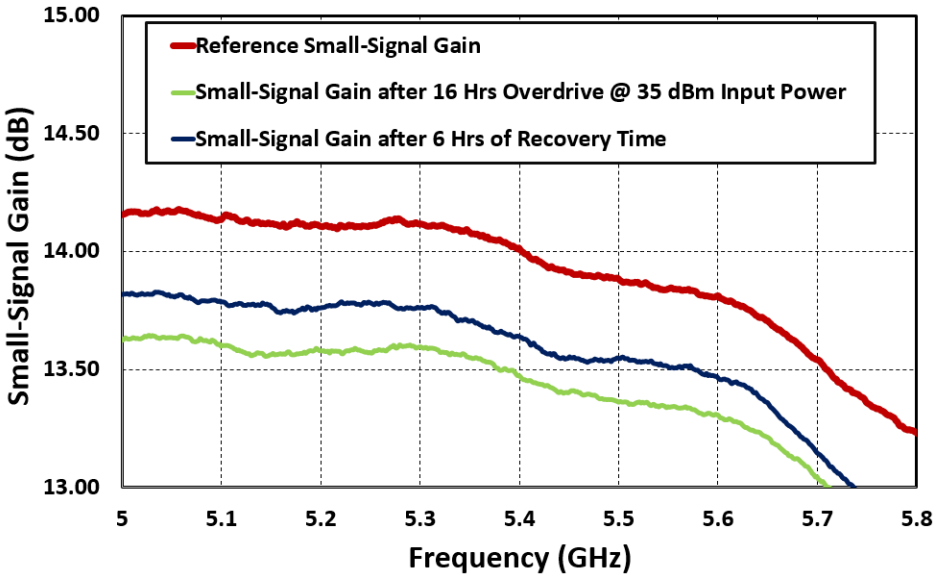

Figure 5-21 Measured small-signal gain : (reference gain, post 16 Hrs @ Pin 35 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA)

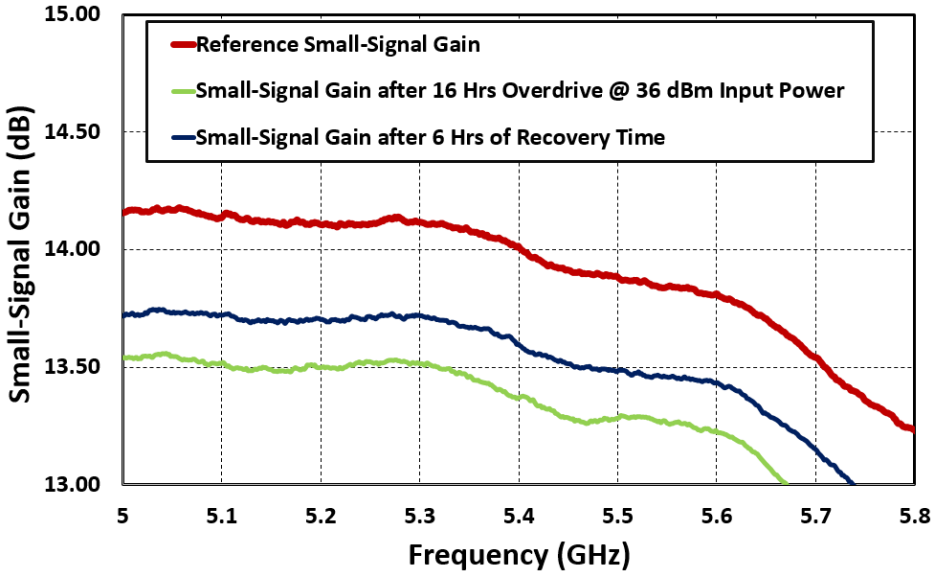

Figure 5-22 Measured small-signal gain : (reference gain, post 16 Hrs @ Pin 36 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA)

Table 5-2 Delta in gain at different input power @ 5.4 GHz.

Input Power	Reference Gain (dB)	Gain after 16 Hrs (dB)	Delta in the Gain after 16 Hrs (dB)	Gain after 6 Hrs recovery (dB)	Delta in the Gain after 6 Hrs (dB)	Gain Compression (dB)
31 dBm	13.98	13.84	-0.14	13.87	-0.11	19.4
32 dBm		13.74	-0.24	13.82	-0.16	21.3
33 dBm		13.67	-0.31	13.76	-0.22	23
34 dBm		13.48	-0.5	13.7	-0.28	24.9
35 dBm		13.41	-0.57	13.67	-0.31	25.6
36 dBm		13.36	-0.62	13.56	-0.42	27

5.5.2. Noise figure performance

Noise figure characterization of the MMIC LNA was performed on the same measurement setup. The reference NF of the LNA was measured in the beginning, as given in Figure 5-8, which is 0.9 –1.3 dB, in the operating frequency band. The noise figure results of the fabricated LNA at different power levels are shown in Figure 5-23, Figure 5-24, Figure 5-25, Figure 5-26, Figure 5-27, and Figure 5-28. Table 5-3 illustrates the difference in the measured noise figure at different input power and different conditions.

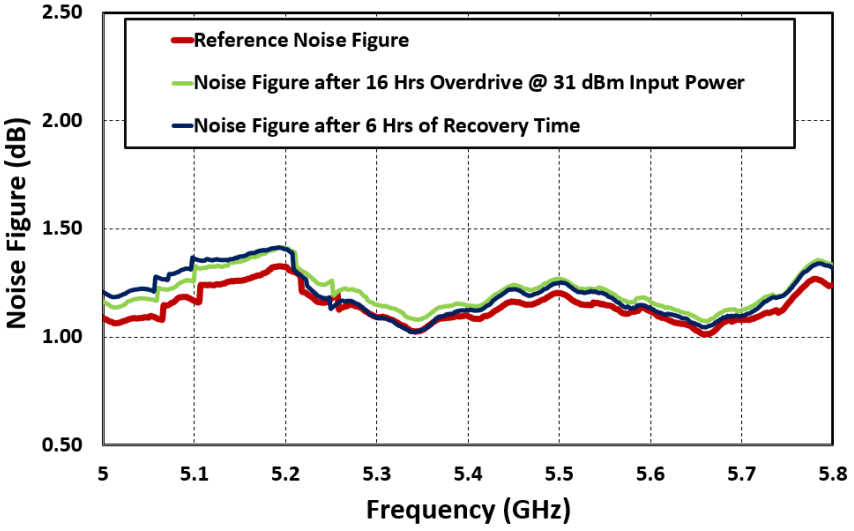

Figure 5-23 Measured noise figure : (reference NF, post 16 Hrs @ Pin 31 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA)

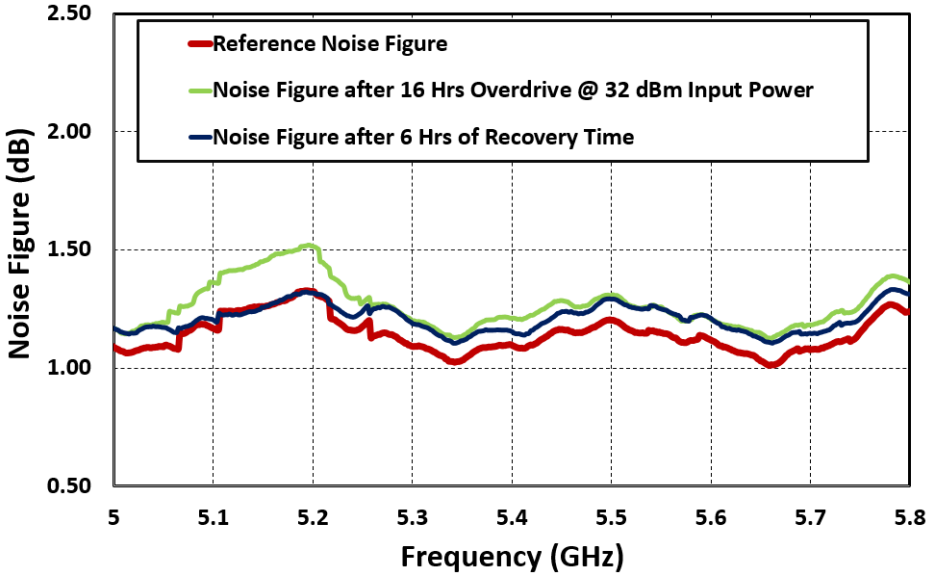

Figure 5-24 Measured noise figure : (reference NF, post 16 Hrs @ Pin 32 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA).

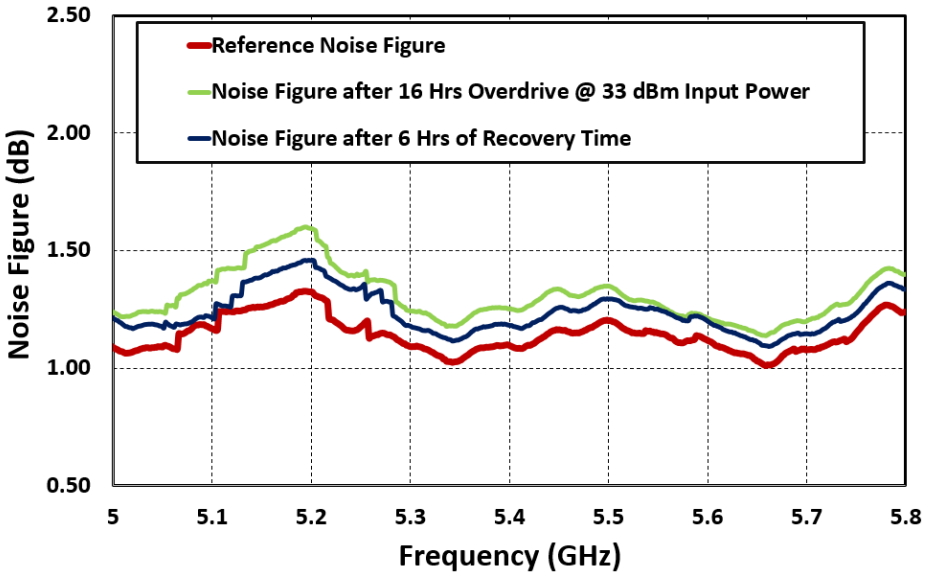

Figure 5-25 Measured noise figure : (reference NF, post 16 Hrs @ Pin 33 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA).

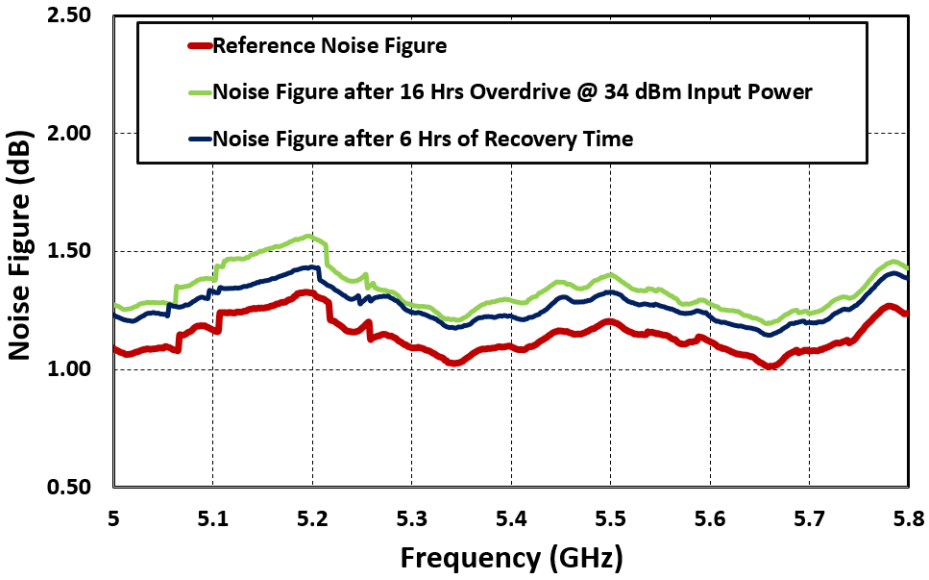

Figure 5-26 Measured noise figure : (reference NF, post 16 Hrs @ Pin 34 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA).

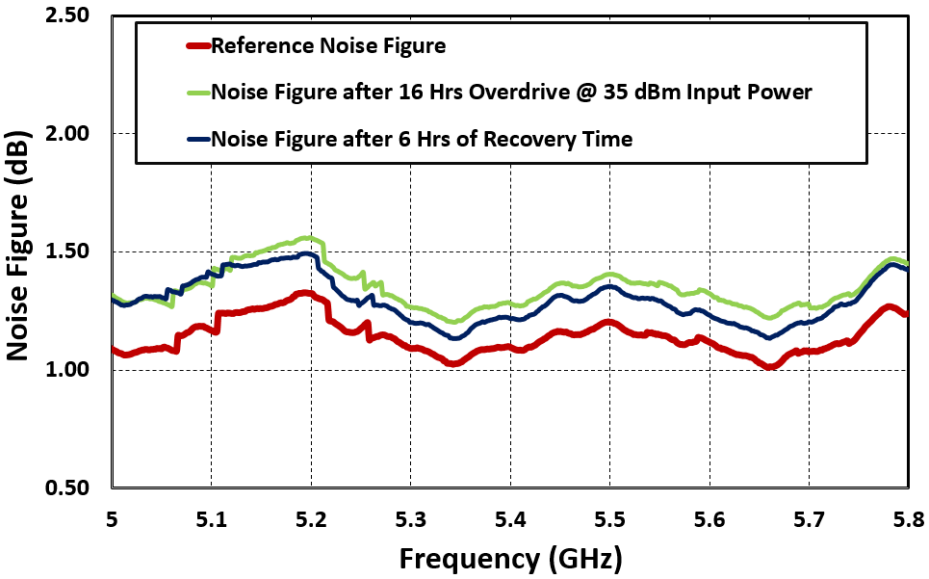

Figure 5-27 Measured noise figure : (reference NF, post 16 Hrs @ Pin 35 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA).

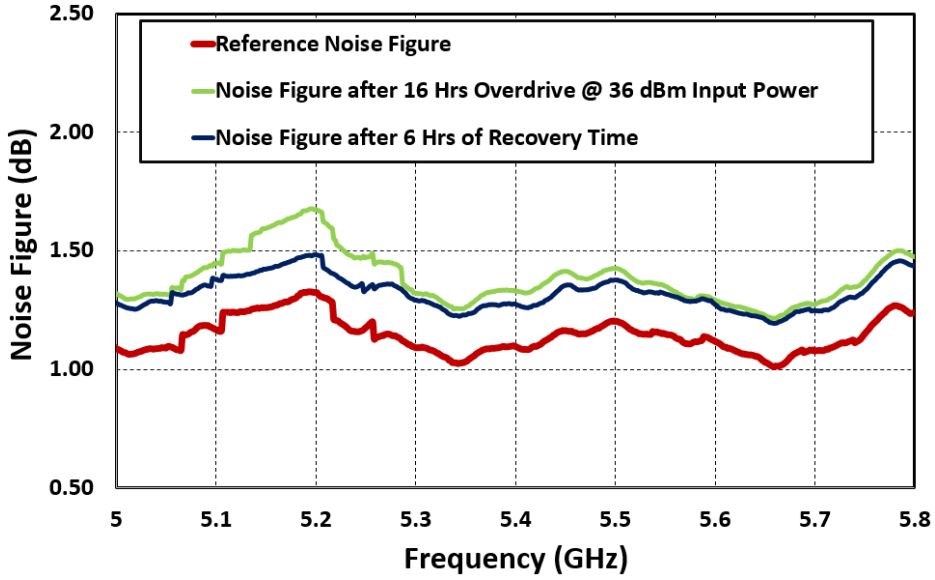

Figure 5-28 Measured noise figure : (reference NF, post 16 Hrs @ Pin 36 dBm and post 6 Hrs recovery at V_D = 16 V and I_D = 36 mA).

Table 5-3 Delta in noise figure at different input power @ 5.4 GHz.

Input Power	Reference Noise Figure (dB)	Noise Figure after 16 Hrs (dB)	Delta in the Noise Figure after 16 Hrs (dB)	Noise Figure after 6 Hrs recovery (dB)	Delta in the Noise Figure after 6 Hrs(dB)
31 dBm	1.1	1.14	+0.04	1.12	+0.02
32 dBm		1.21	+0.11	1.15	+0.05
33 dBm		1.25	+0.15	1.18	+0.08
34 dBm		1.29	+0.19	1.22	+0.12
35 dBm		1.3	+0.20	1.22	+0.12
36 dBm		1.33	+0.23	1.27	+0.17

5.5.3. Gate and drain Currents

During the measurements of the LNA, we monitored the gate, as well as the drain currents at different input power. From the power sweep measurements, the output power and the drain current exhibit monotone increases up to certain saturation points, approximately 30 dBm and 90 mA, respectively. After reaching its peak drain current value, the drain current decreases rapidly, with the increase of the drive level and with a concurrent increase in the gate current. This corresponds to the onset of a dc gate current, as shown in Figure 5-29. This gate current flows if the incident drive level causes large voltage swings high enough to drive the gate into a forward bias state. The curves for the drain current of the LNA are shown in Figure 5-30. Table 5-4 illustrates the variation of the gate and drain currents during the stress conditions at different input power levels.

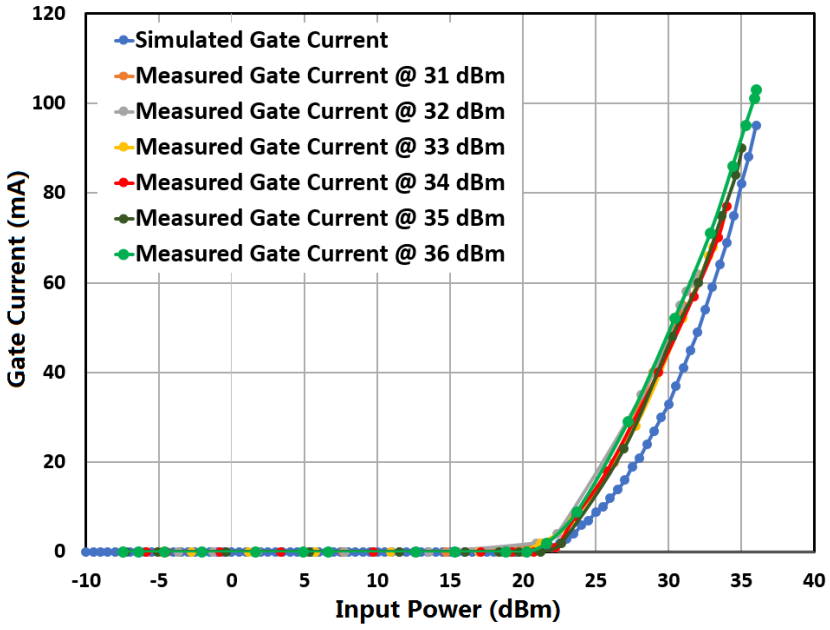

Figure 5-29 Gate currents of the LNA at different power stresses as a function of the input power at 5.4 GHz

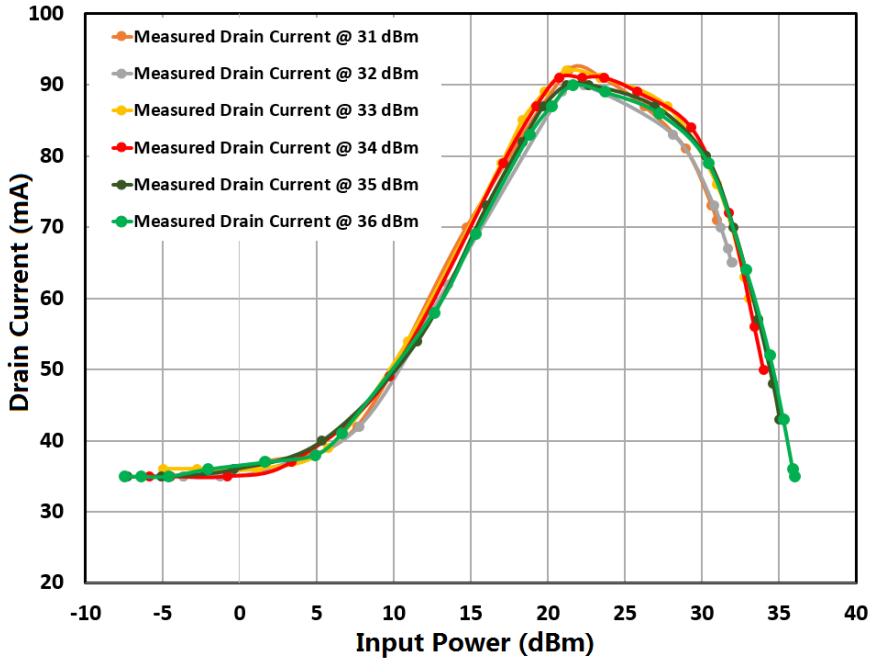

Figure 5-30 Drain currents of the LNA at different power stresses as a function of the input power at 5.4 GHz

Table 5-4 Variation of gate & drain currents versus time at stress conditions of different input power levels.

Input Power	Gate & Drain Currents	Start time	After 16 Hrs	Delta
31 dBm	I_D (mA)	67.2	68.6	+ 2.1 %
	I_G (mA)	58	59.4	+ 2.4 %
32 dBm	I_D (mA)	65	68.3	+ 5.1 %
	I_G (mA)	64.4	66.8	+ 3.7 %
33 dBm	I_D (mA)	61.7	65.5	+ 6.2 %
	I_G (mA)	72	75.2	+ 4.4 %
34 dBm	I_D (mA)	50.9	54.8	+ 7.7 %
	I_G (mA)	77.3	81	+ 4.8 %
35 dBm	I_D (mA)	43.2	46.9	+ 8.6 %
	I_G (mA)	91.1	95.7	+ 5.0 %
36 dBm	I_D (mA)	26.2	29	+ 10.7 %
	I_G (mA)	100.2	106.3	+ 6.1 %

5.6. Two-stage LNA design

In this section, a two-stage LNA, based on inductively source-degenerated topology with R-C feedback network, was designed. Each stage was created separately and then cascaded together, as shown by the block diagram in Figure 5-31, to achieve a maximum gain of higher than 23 dB and low noise characteristics of less than 1.2 dB over a wideband frequency range from 5 to 6 GHz. The noise figure of the first stage overrules the noise figure of the whole system as validated by Frii's equation (5-5).

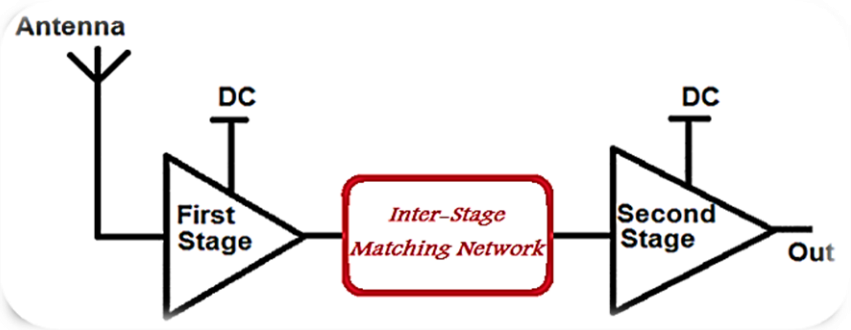

Figure 5-31 Cascaded two-stage LNA

$$NF = NF_1 + \left(\frac{NF_2 - 1}{G_1}\right) + \left(\frac{NF_3 - 1}{G_1 G_2}\right) + \cdots + \left(\frac{NF_n - 1}{G_1 G_2 \cdots G_n}\right) \quad (5\text{-}5)$$

The transistor selection of the first stage is the most important step in designing the LNA. The input and output matching networks of the first stage were designed to achieve a minimum noise figure. At the input network, the device is matched to its optimum noise matching admittance Y_{opt}. The first stage amplifier uses a HEMT GaN device of 4-finger of 75 um gate width (300 um total periphery), biased at 16 V, and 150 mA/mm current density (45 mA total current). The R-C feedback function is to maintain the stability of the circuit besides enhancing the gain bandwidth. An inductive source degeneration technique is used to minimize additional noise generation.

The second stage is designed and matched for maximum gain. This is because the noise figure of the stages preceding the first stage does not contribute to the overall noise figure of the system. The device used in the second stage has 6-fingers with a gate width of 65 um. The matching networks can be designed either to achieve a minimum noise figure, or maximum gain. There is always a trade-off between achieving the minimum noise figure of the device and maximum gain. A full circuit schematic of the designed LNA is depicted in Figure 5-32. Both stages of the designed LNA were biased with a drain bias of 16 V, and the total drain current I_D of both the stages is 80 mA. Figure 5-33 shows the fabricated die of the designed MMIC LNA with a chip size of 1.8 x 2 mm^2 (3.6 mm^2).

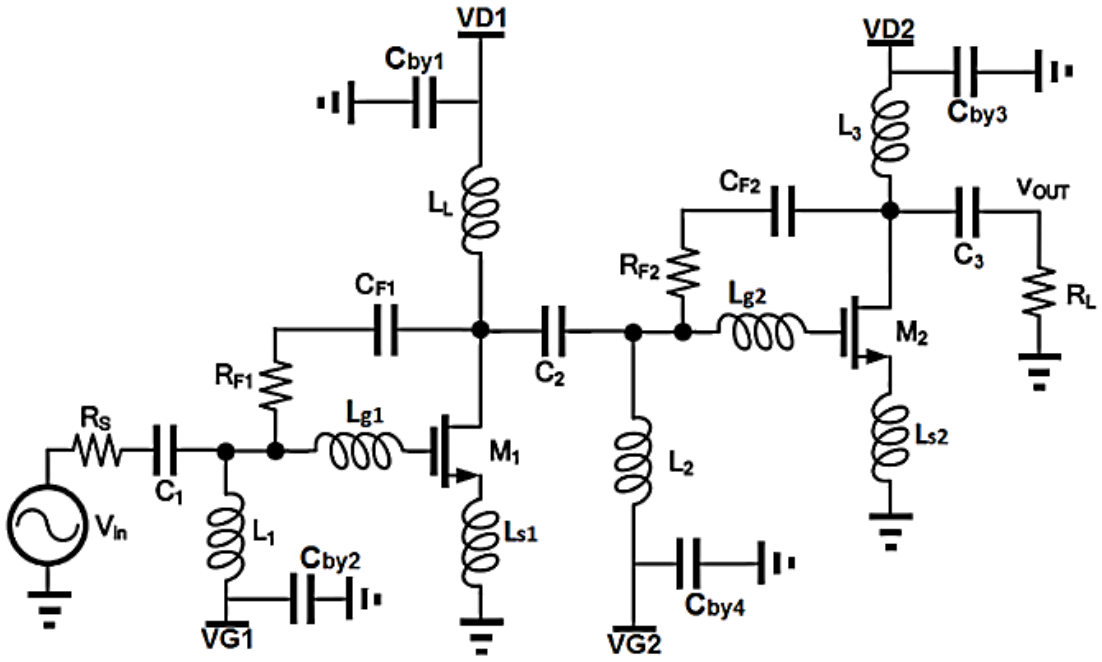

Figure 5-32 Circuit diagram of the designed two-stage LNA

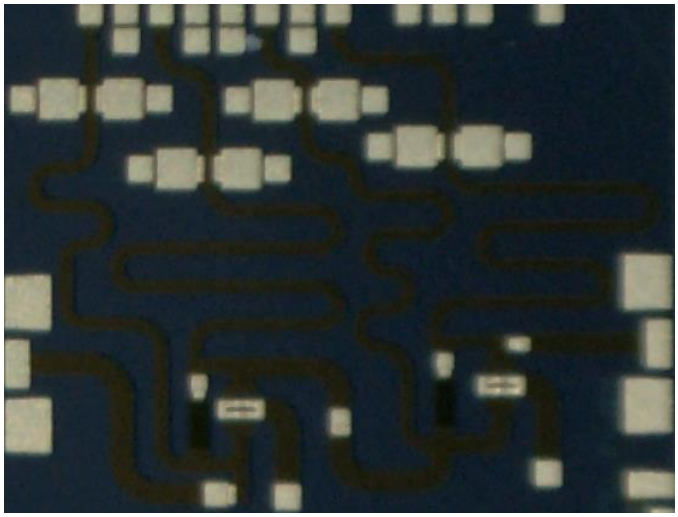

Figure 5-33 Fabricated MMIC die of the two-stage LNA with size 1.8 x 2 mm^2

5.7. Two-stage LNA characterization

5.7.1. Gain, matching, and noise performance

Figure 5-34 shows that the designed LNA has a measured noise figure ranging from 0.9 dB to a maximum of 1.3 dB, in the frequency range of 5 to 6 GHz. Figure 5-35 shows that the device has an input return loss of -10 dB to -12 dB and an output return loss of -9 to -20 dB. The LNA small-signal gain is from 23 dB to 25 dB, in the whole frequency band of 5 GHz to 6 GHz.

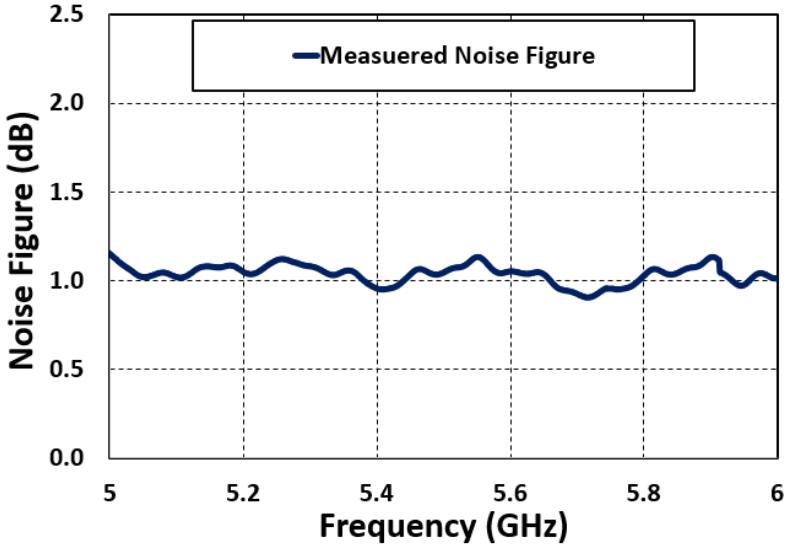

Figure 5-34 Noise figure of the designed two-stage MMIC LNA

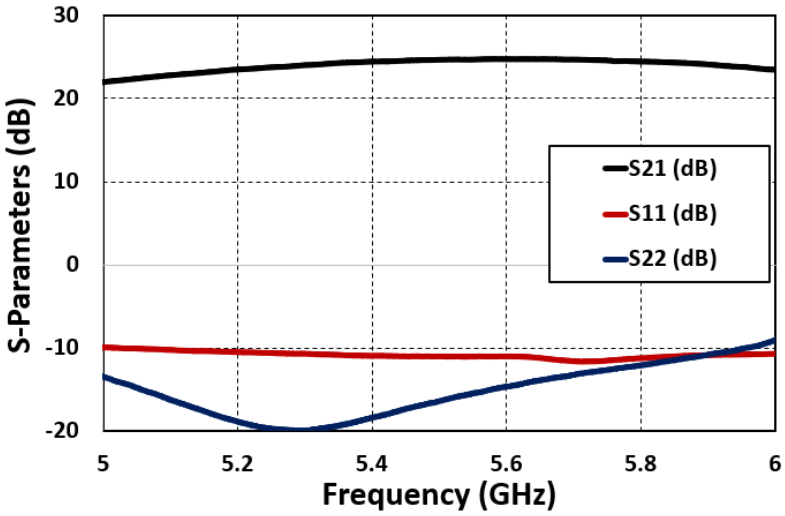

Figure 5-35 S-parameter of the cascaded two-stage LNA

5.7.2. Large-Signal and Linearity Characterization

The large-signal behavior results are shown in Figure 5-36. These results, at 5.4 GHz with V_D = 16 V and V_G = -2.7 V, indicates that the LNA achieves a maximum output power of 29 dBm. It also shows that it has a small signal gain of 25 dB. The two-tone simulation was performed to characterize the LNA's non-linear behavior. The two-tone simulation was carried out at 5.4 GHz with a tone spacing of 10 MHz. The biasing conditions remained the same as in the large-signal characterization. An outstanding linear performance was obtained as shown in Figure 5-37. The OIP3 is better than 35 dBm in the linear region, while the IP3 is 10 dBm. At the P1dB compression point, the OIP3 is about 33 dBm, as displayed in Figure 5-38. These results mean that OIP3 is 11 dB higher than P1dB at the center operating frequency, which indicates the good linearity of the designed MMIC LNA.

Figure 5-39 displays the third-order intermodulation difference (IMD3) plotted against the output power of the two-tone modulation. The plot indicates that the IMD3 of the designed MMIC LNA is -25 dBc at the 1dB compression point.

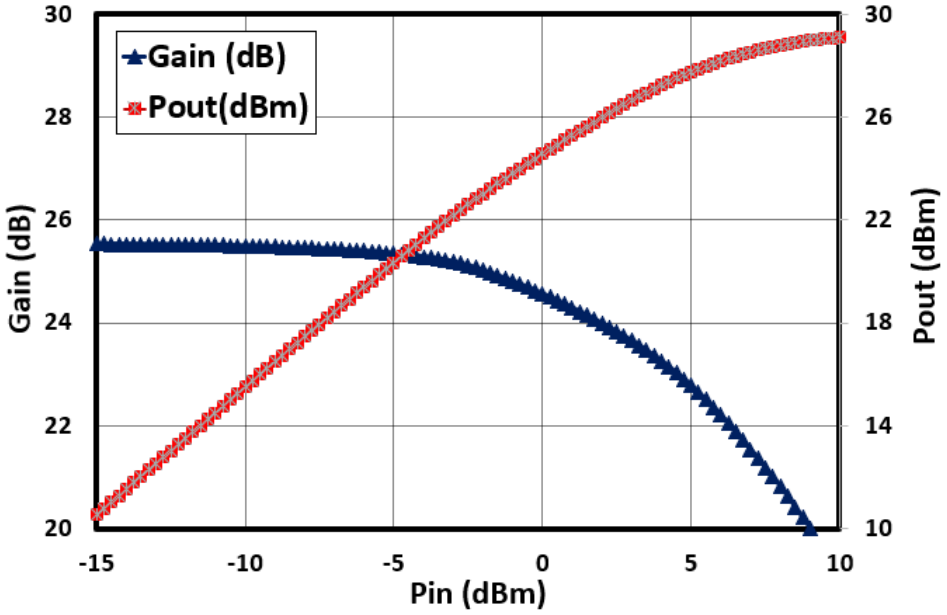

Figure 5-36 Large signal behavior for the cascaded two-stage LNA

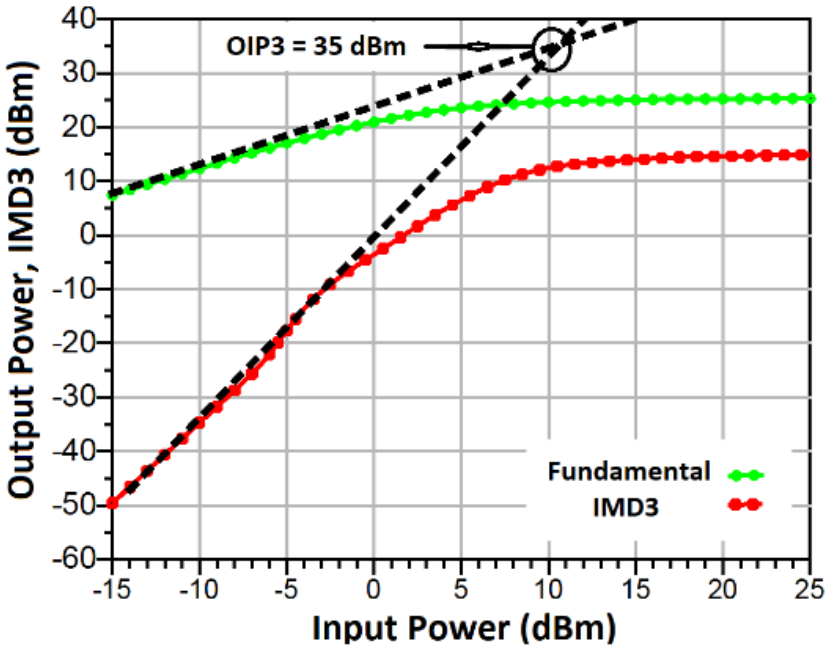

Figure 5-37 Linearity performance of the cascaded two-stage LNA

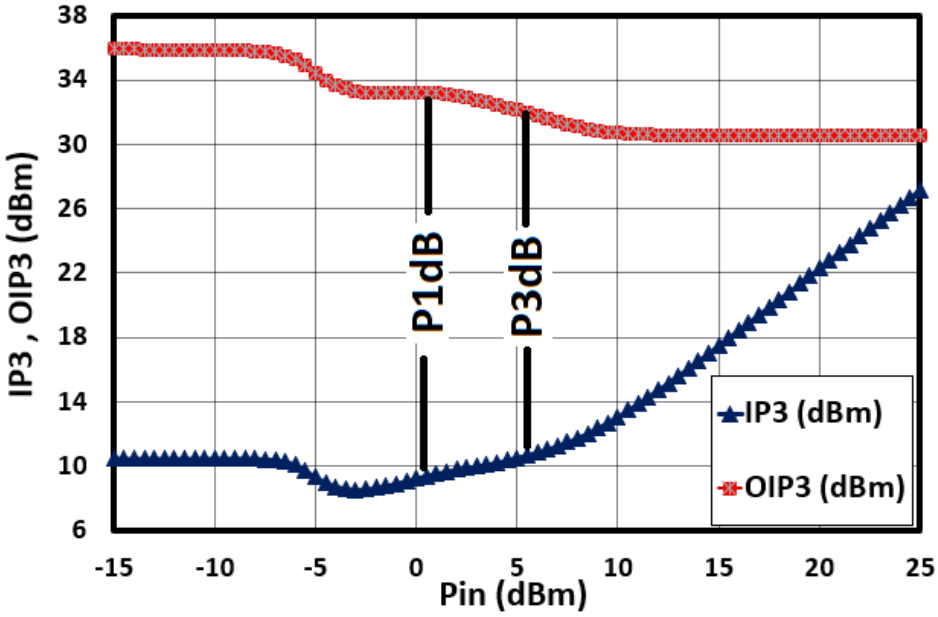

Figure 5-38 OIP3 and IP3 versus input power of the two-stage LNA

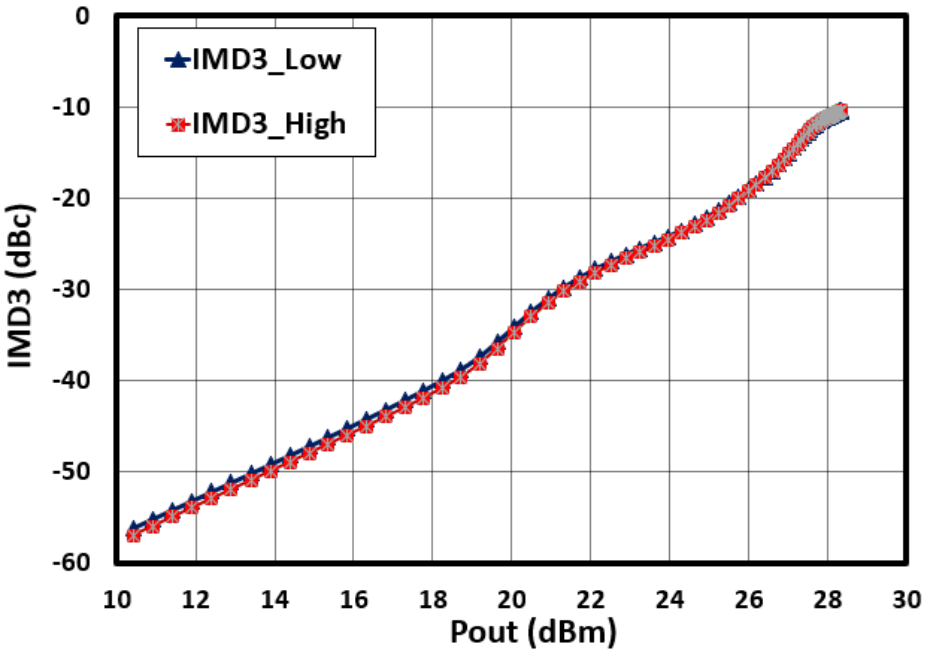

Figure 5-39 IMD3 of the MMIC two-stage LNA

5.8. Design of UWB LNA

The LNA design is based on cascode topology, with a series inductive source and using RLC frequency-dependent feedback network. The proposed LNA's cascode configuration is composed of two-stage; the first stage is based on the degenerated common-source topology, and the second stage performs as a common-gate topology. The common source stage provides a higher gain and a lower NF, while the common gate stage acts as a buffer to reduce the first stage's loading effect. The main advantage of the common gate configuration is that it has good isolation and provides a wideband frequency response. The RLC frequency-dependent feedback network in this configuration is used to achieve the required broadband frequency operation. It is designed to obtain excellent wideband frequency response, with flat gain, and to make the proposed LNA unconditionally stable. Furthermore, an LC-ladder matching network is used in the input matching network to obtain more improvement in both the noise figure and power gain performance of the proposed LNA across the entire frequency range [91].

First, the LNA is designed based on the linear noise model from the UMS PDK. That is because it is better in indicating the noise parameters and accurately estimating the performance of this LNA topology. For the UMS foundry specifications, a typical biasing condition for the cascode configuration is at a drain voltage of 24 V, a second gate bias of 20 V, and a proper first gate bias of -3.5 V. The first stage uses a HEMT GaN device of 4-finger and 65 um gate width (260 um total periphery), while the device of 4-finger and 120 um gate width (480 um total periphery) is used in the common gate stage. A full circuit diagram of the proposed LNA is shown in Figure 5-40. Using a simplified HEMT equivalent circuit model, the small-signal equivalent circuit for the proposed cascode configuration with RLC frequency-dependent feedback network is displayed in Figure 5-41.

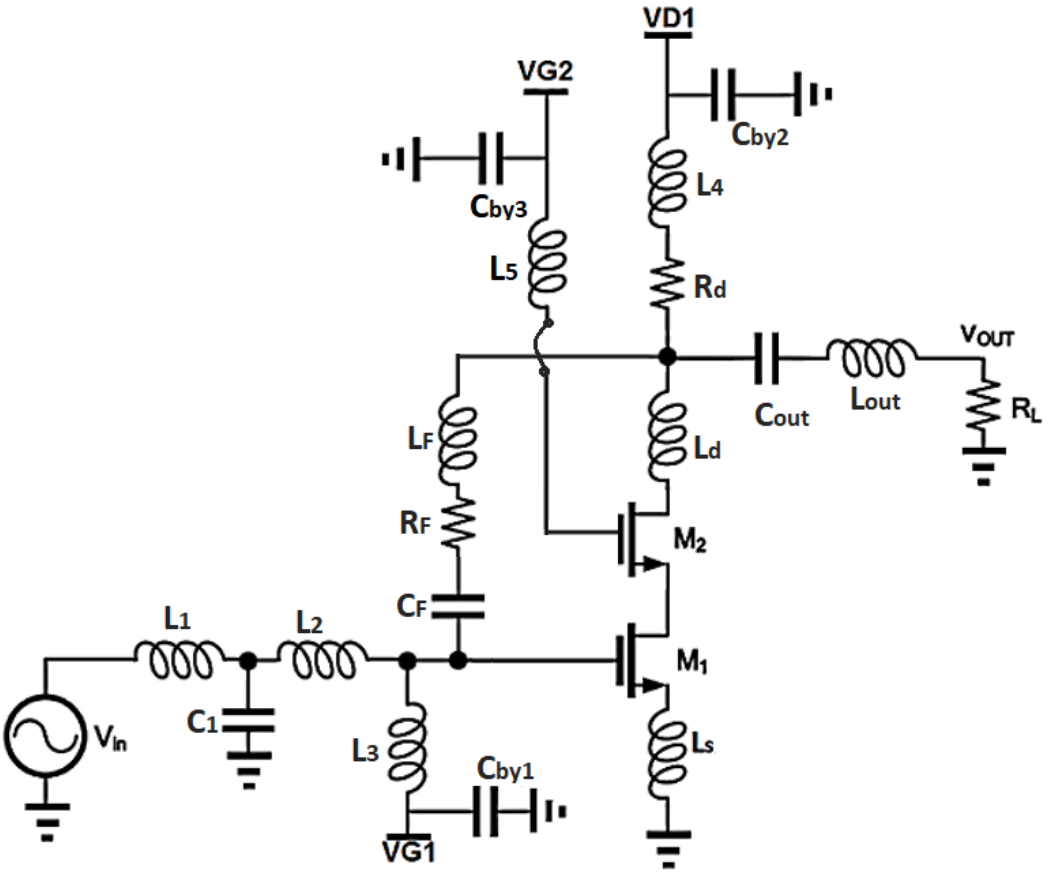

Figure 5-40 Circuit diagram of the UWB LNA

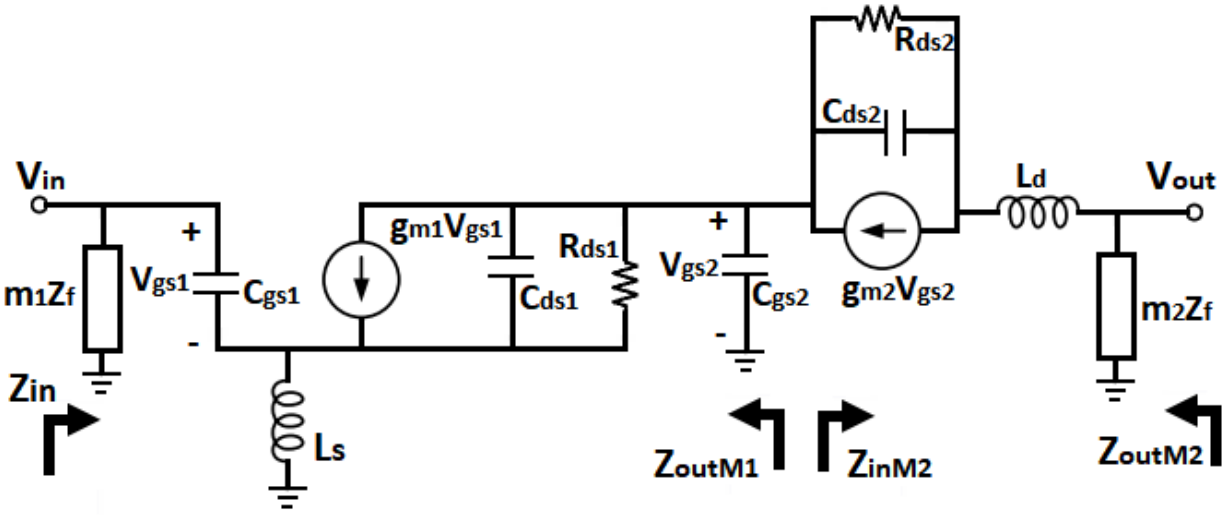

Figure 5-41 The small-signal equivalent circuit of the proposed cascode configuration with RLC frequency-dependent feedback network

The inductive source degeneration technique of the first device is used to minimize additional noise generation. The optimum noise figure might happen at any input impedance, not necessarily 50 Ω. Also, the input impedance of the transistor is dominated by C_{gs} and contains almost a real part. The series inductor L_s is placed at the source of the transistor to ease the LNA matching. The inductor appears in series with the C_{gs} and therefore is directly added to the input impedance. The other effect of the inductor Ls is to provide an effective resistive input without contributing any additional noise. The other advantages of adding the inductor are that the noise factor does not change, and the optimum noise impedance is closer to the input impedance of the transistor. Figure 5-42 shows the intrinsic equivalent parameters for the transistor of the first stage of 4-finger with a gate width of 62 μm while the parameters of the common gate device of 4-finger with a gate width of 120 μm are depicted in Figure 5-43. These devices' intrinsic parameters are obtained by sweeping frequency from 0.5 to 15 GHz and a drain bias of 15 V.

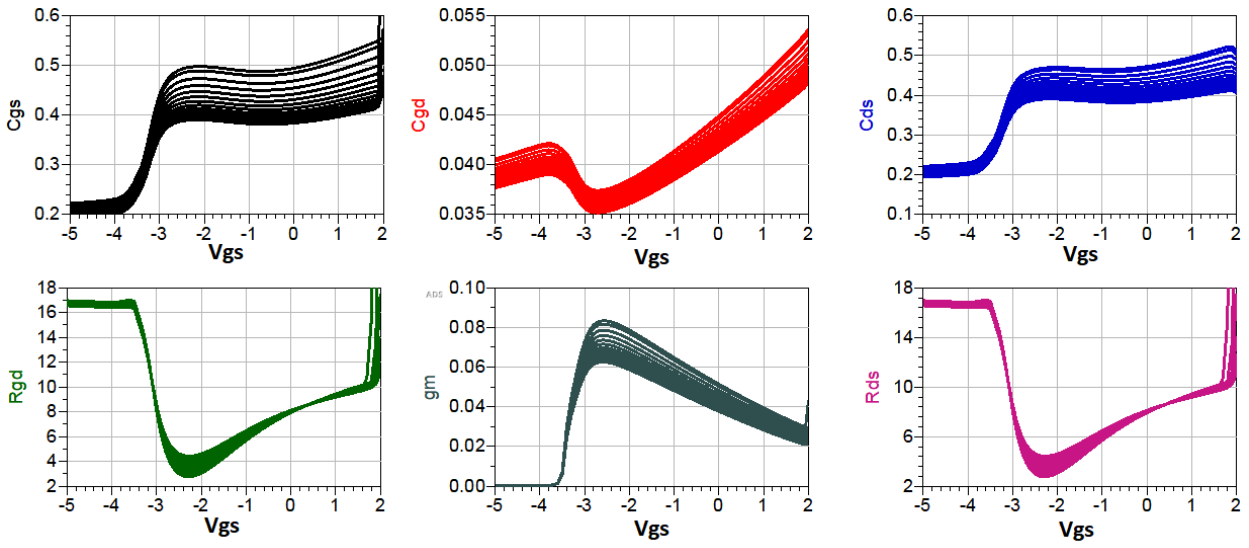

Figure 5-42 Extracted intrinsic equivalent parameters of the device with 4 fingers and 62 um gate width at V_D = 15 V across the frequency band (0.5 – 15 GHz)

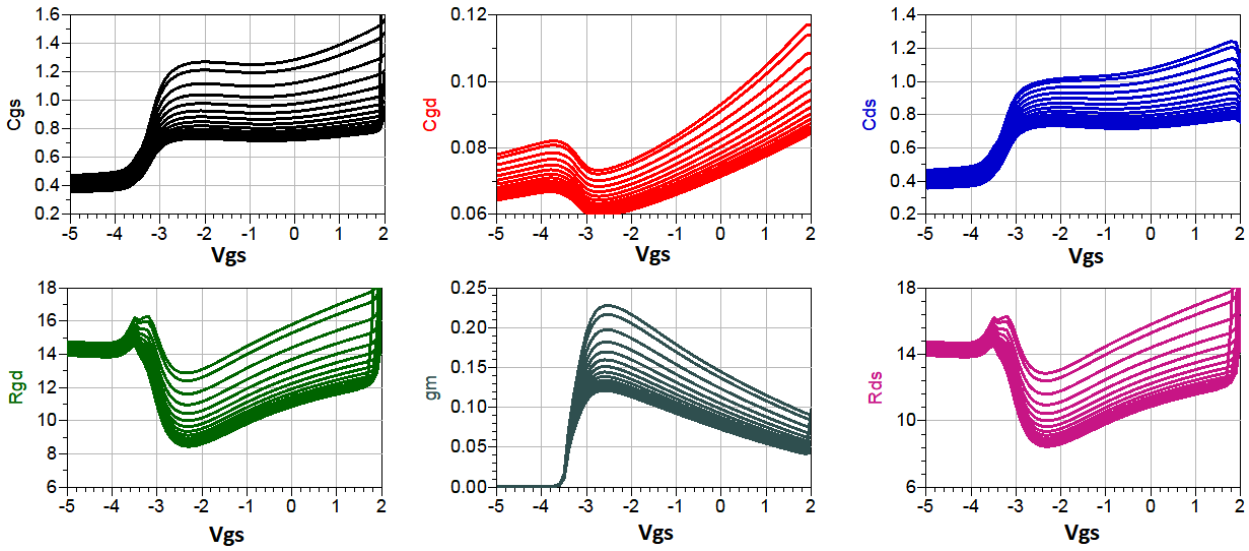

Figure 5-43 Extracted intrinsic equivalent parameters of the device with 4 fingers and 120 um gate width at V_D = 15 V across the frequency band (0.5 – 15 GHz)

Using the circuit in Figure 5-41, the gain from the gate to the drain of the cascode configuration can be formulated as follows:

$$G \approx g_{m1} \times (Z_{outM2} \parallel m_2 Z_f \parallel Z_L) \tag{5-6}$$

where

$$Z_f = R_f + j\omega L_f + \frac{1}{j\omega C_f} \tag{5-7}$$

$$Z_{outM2} = j\omega L_d + (1 + g_{m2} Z_{outM1})(R_{ds2} \parallel \frac{1}{j\omega C_{ds2}}) + Z_{outM1} \tag{5-8}$$

$$Z_{outM1} = R_{ds1} \parallel \frac{1}{j\omega C_{ds1}} \parallel \frac{1}{j\omega C_{gs1}} \tag{5-9}$$

where g_{m1} and g_{m2} are the transconductances, while R_{ds1}, R_{ds2}, $C_{ds1,}$ and C_{ds2} are the parasitic resistances and capacitances of devices M_1 and M_2, respectively. As well, m_1 and m_2 are Miller's multiplication factors. The RLC feedback network has a significant impact on the frequency response of the cascode LNA. The appropriate choice of network values will result in achieving broadband performance, with good gain flatness and unconditional stability. The capacitor C_f is used for dc decoupling, which blocks the dc current from the transistor's drain to the gate. The effect of the inductors L_f and R_f on the gain and noise figure performance can be analyzed. Also, the effect of the inductor, $L_{d,}$ on the gain can be analyzed according to Equation (5-6). To validate this analysis, both maximum stable gain (MSG) and noise figure for different values of L_f, R_f, and L_d are simulated at the schematic level, and the results are presented in Figure 5-44, Figure 5-45, and Figure 5-46. Indeed, the proper choice of L_f, R_f, and L_d values can enhance and extend the gain at high operation frequency, hence improving the gain flatness. Simultaneously, the selected values will impact the noise figure performance across the entire bandwidth.

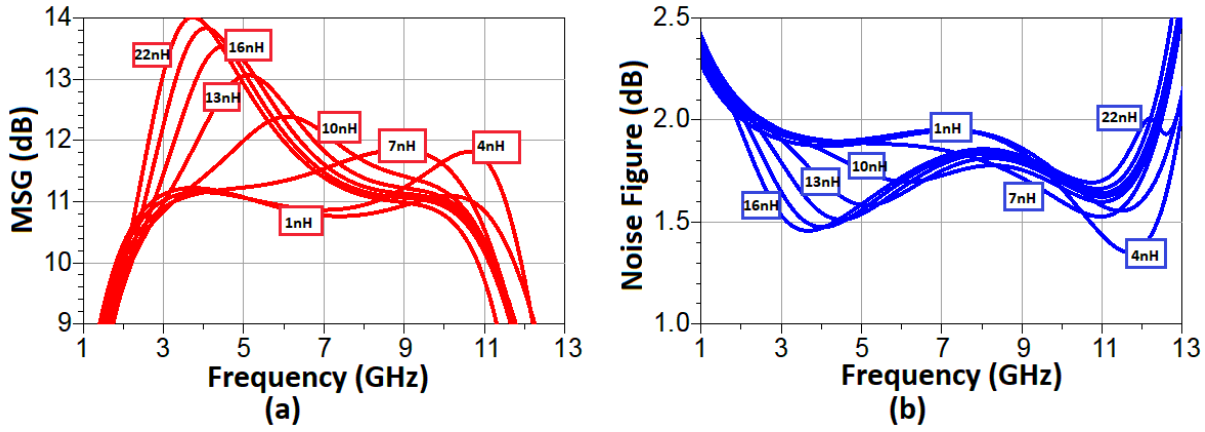

Figure 5-44 The simulated MSG and noise figure for different values of L_f

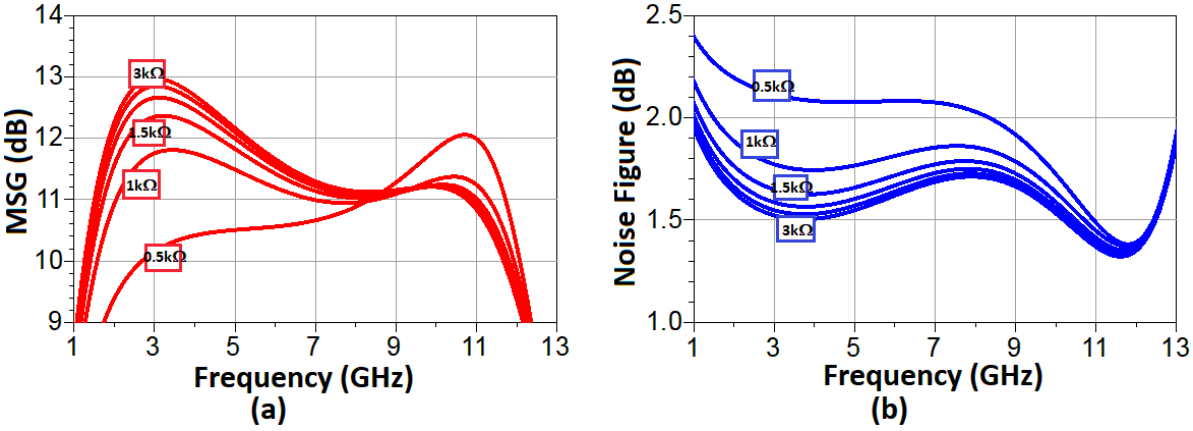

Figure 5-45 The simulated MSG and noise figure for different values of R_f

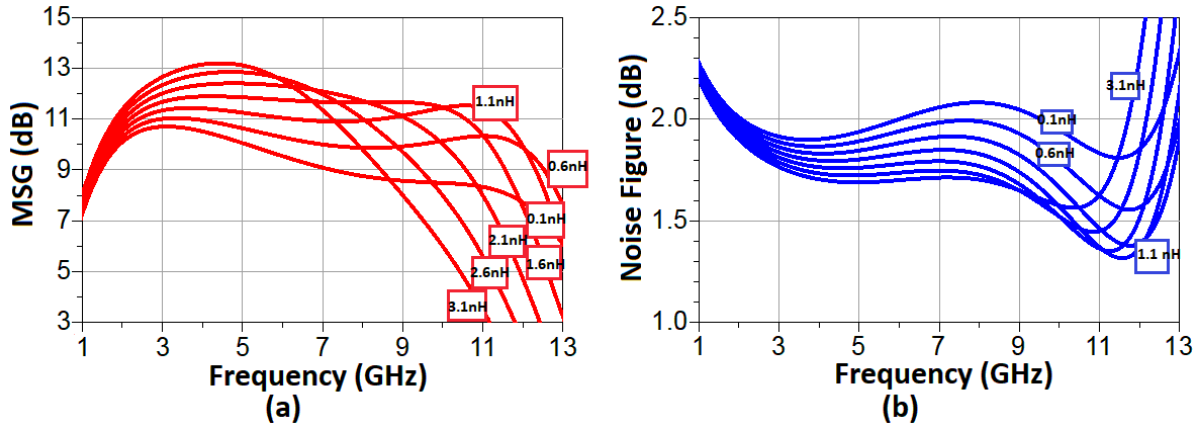

Figure 5-46 The simulated MSG and noise figure for different values of L_d

To implement the LNA design, the source impedance, noise matching point is chosen for minimum noise factor and the load impedance is a conjugate match to achieve maximum gain. Both the input matching and output matching networks are based on L–C circuits. The simplified input impedance Z_{in} can be expressed as:

$$Z_{in} = m_1 Z_f \parallel \left(\frac{1}{j\omega C_{gs1}} + j\omega L_s + \frac{g_{m1} L_s}{C_{gs1}}\right) \tag{5-10}$$

The input impedance in (5-10) can be written as $Z_{in} = R_{eq} + jX_{eq}$. The X_{eq} value is obtained from the complete small-signal equivalent circuit shown in Figure 5-41, and the extracted parameters from Figure 5-42. The simple equivalent input matching circuit is given in Figure 5-

47(a). The input impedance can be absorbed into the LC-ladder topology, based on the matching topology in [91]. This will lead to only real input impedance over a wider frequency band. The real part of the input impedance R_{eq} can be settled close to 50Ω in the desired frequency band by selecting L_S and Z_f proper values.

The initial component values of the input matching LC-ladder network are set as: L_1 = 400 pH, C_1 = 200 fF, L_2 = 700 pH, based on the method described in [91], while selecting L_S = 100 pH and the feedback network is set as: L_f = 3.5 nH, R_f = 800 Ω and C_f = 200 fF based on Figure 5-44 and Figure 5-45. Figure 5-47(b) shows the simulated S11 from 0.1 GHz to 24 GHz, which indicates that the designed LC-ladder matching network achieves a good input matching, with an input return loss of better than 10 dB from 0.2 GHz to 16 GHz. A higher-order LC-ladder matching network can also be utilized to get better matching results. However, the chip area, insertion loss, and noise degradation, must be considered as a result of using more passive components. The bypass capacitor in the biasing networks is used to prevent any resonance in the operating band and to filter the RF signals. Figure 5-48 shows the circuit layout of the GaN MMIC LNA.

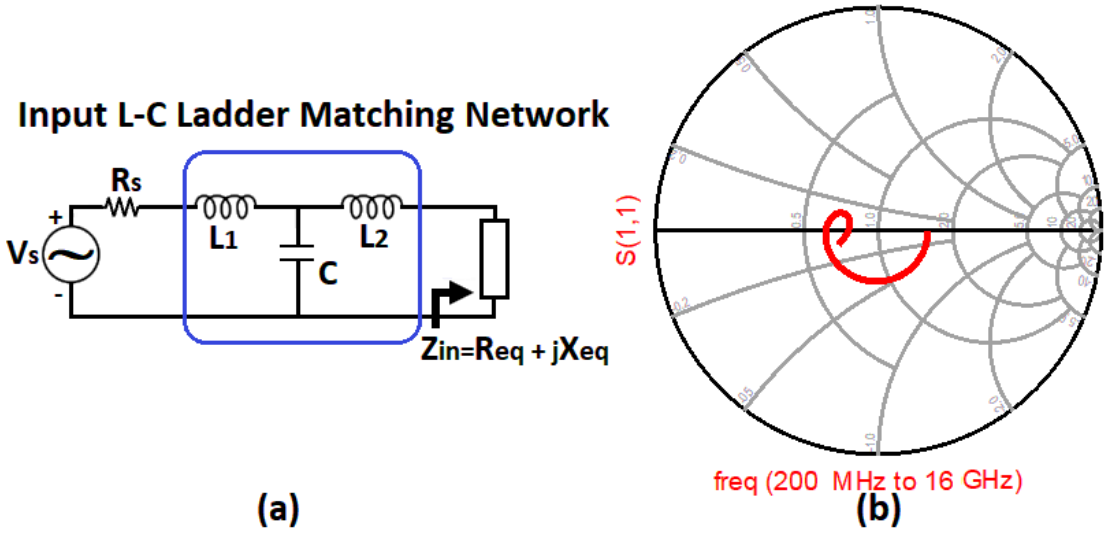

Figure 5-47 (a) The input LC-ladder matching network, (b) S_{11} simulation results

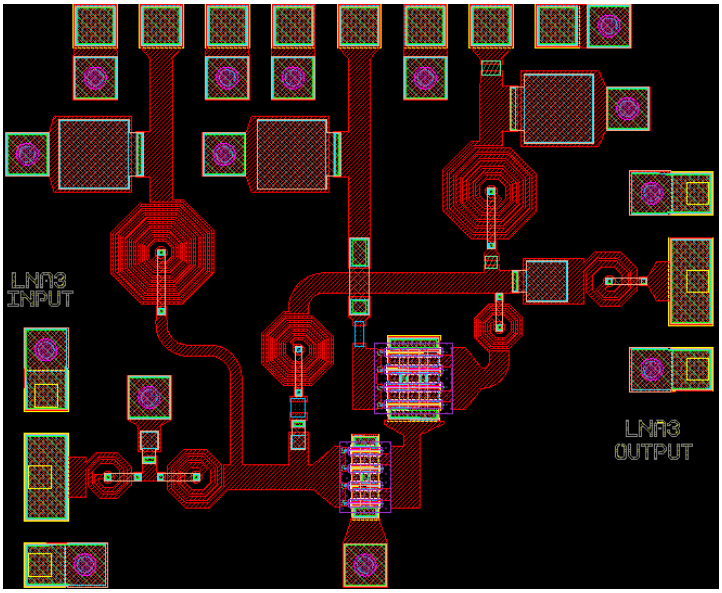

Figure 5-48 Layout of the proposed UWB LNA

5.8.1. UWB LNA characterization

The UWB MMIC LNA was designed and fabricated using a 0.25 um UMS GaN-HEMT process. A microscopic photo of the fabricated LNA IC on the wafer is displayed in Figure 5-49. In the design work, a compact layout was tailored, resulting in a chip with full size of 1.3 mm × 1.6 mm.

5.8.1.1.Gain, matching, and noise figure results

As shown in Figure 5-50, the fabricated LNA has a simulated noise figure of 2.2 to 2.5 dB over the operating frequency band from 2 to 11 GHz. Figure 5-51 shows that the UWB LNA is unconditionally stable over the entire frequency range from 0 to 12 GHz. The post-layout, simulated S-parameters, of the low noise amplifier is shown in Figure 5-52. The UWB LNA exhibits an average gain of 11 dB with ± 1.5-dB variation. The proposed LNA has an output return loss of better than 10 dB, and an input return loss of -9 dB to -15 dB, over frequencies from 2 to 12 GHz.

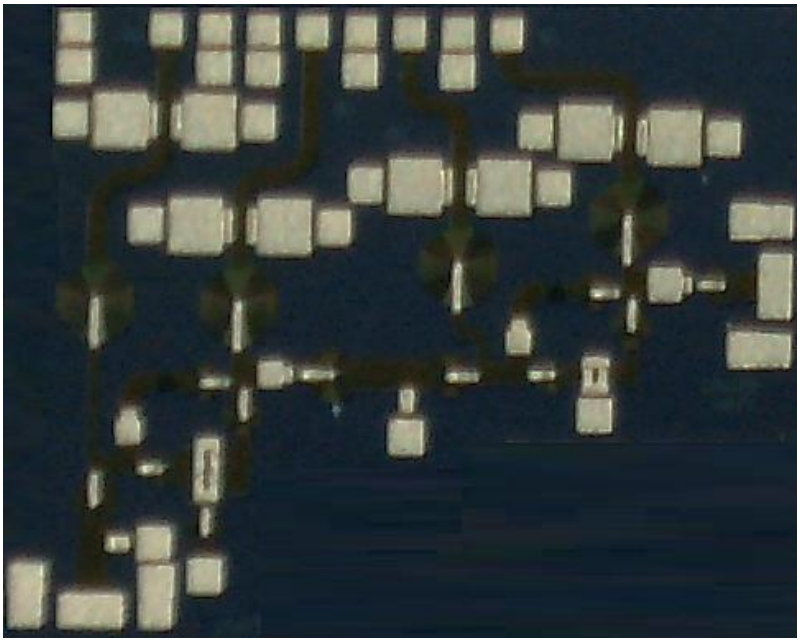

Figure 5-49 The fabricated die of the UWB LNA

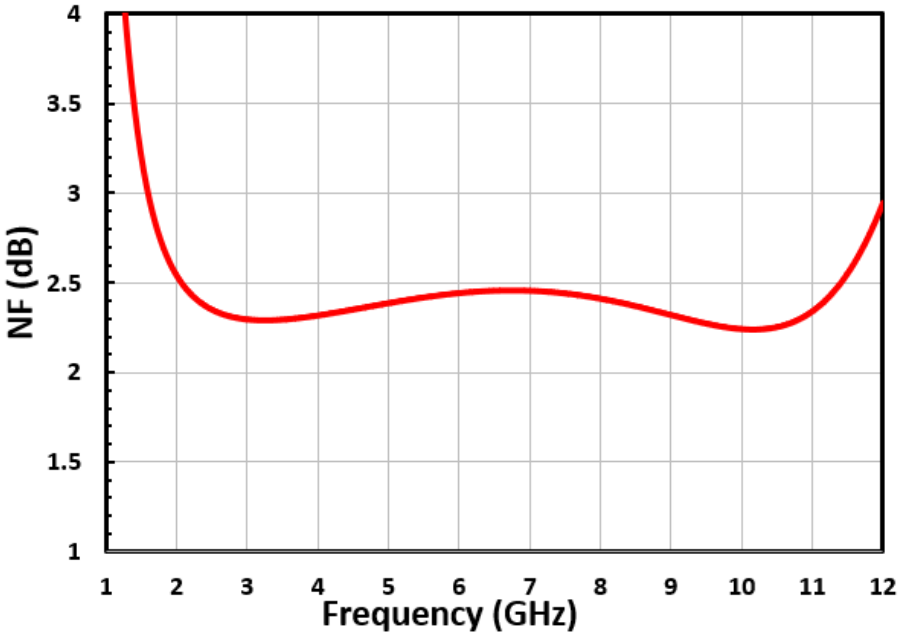

Figure 5-50 Noise figure performance the UWB LNA

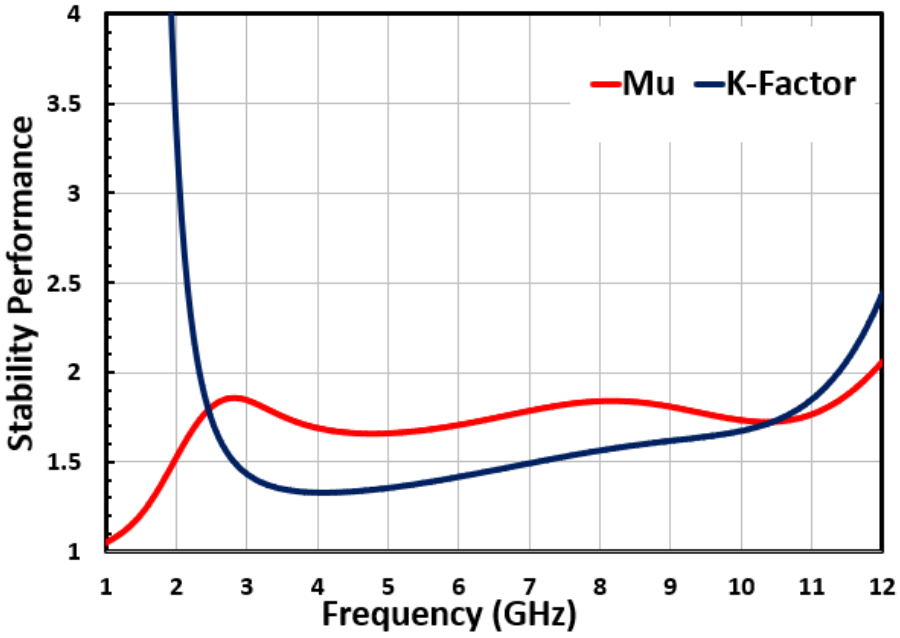

Figure 5-51 Stability condition of the UWB LNA

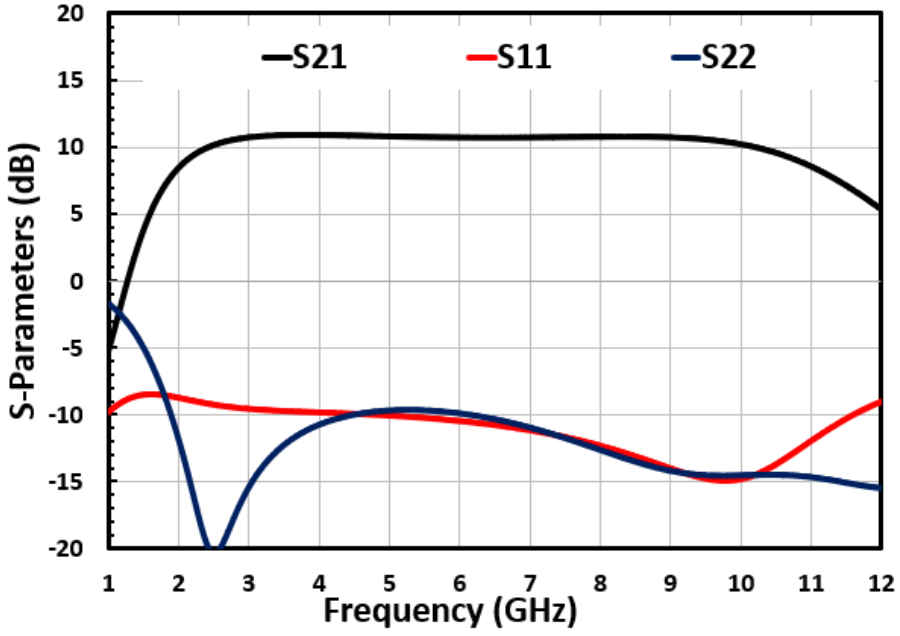

Figure 5-52 S-parameters of the UWB LNA

5.8.1.2. Linearity performance

The IP3 simulation was performed using a two-tone RF signal with a spacing of 10 MHz at different operating frequencies of 3 GHz, 5 GHz, 7 GHz, and 9 GHz. The linearity performances of the proposed UWB LNA are shown in Figure 5-53 to Figure 5-56. The OIP3 is better than 30 dBm in the linear region, while the IP3 is better than 18 dBm.

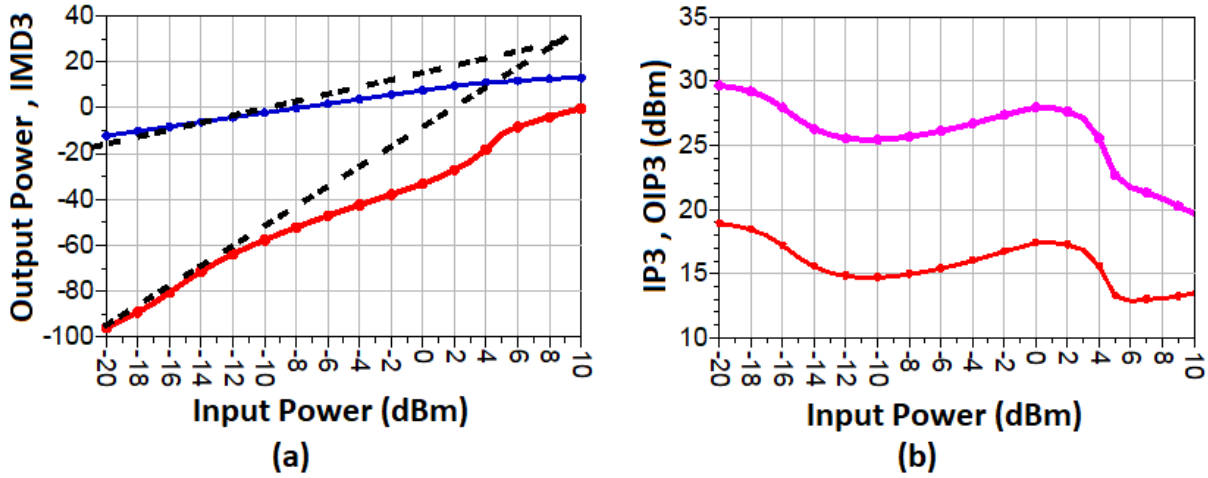

Figure 5-53 Simulated OIP3 and IIP3 of the UWB GaN LNA at 3 GHz with 10 MHz frequency spacing

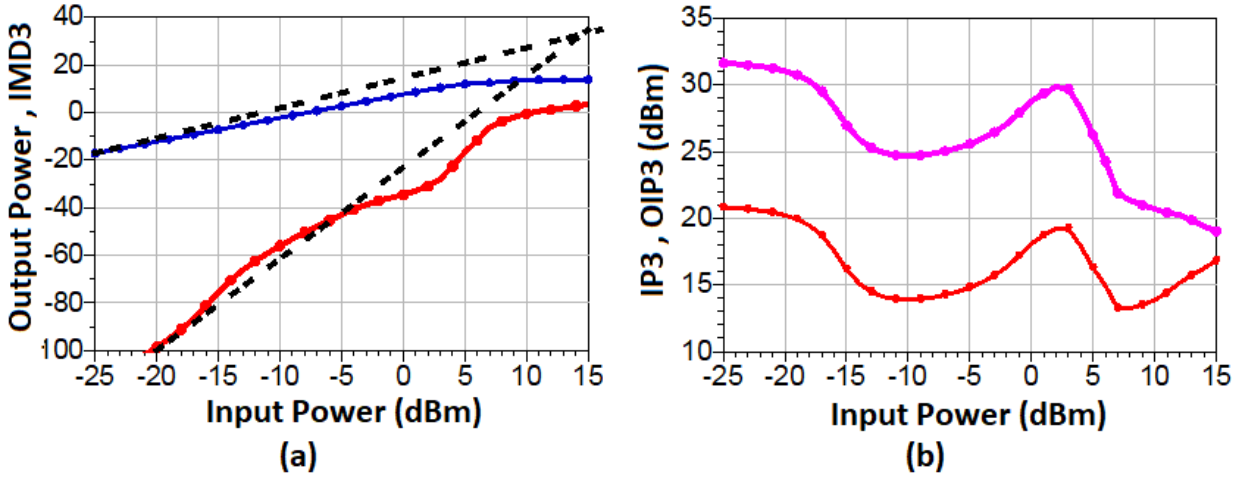

Figure 5-54 Simulated OIP3 and IIP3 of the UWB GaN LNA at 5 GHz with 10 MHz frequency spacing

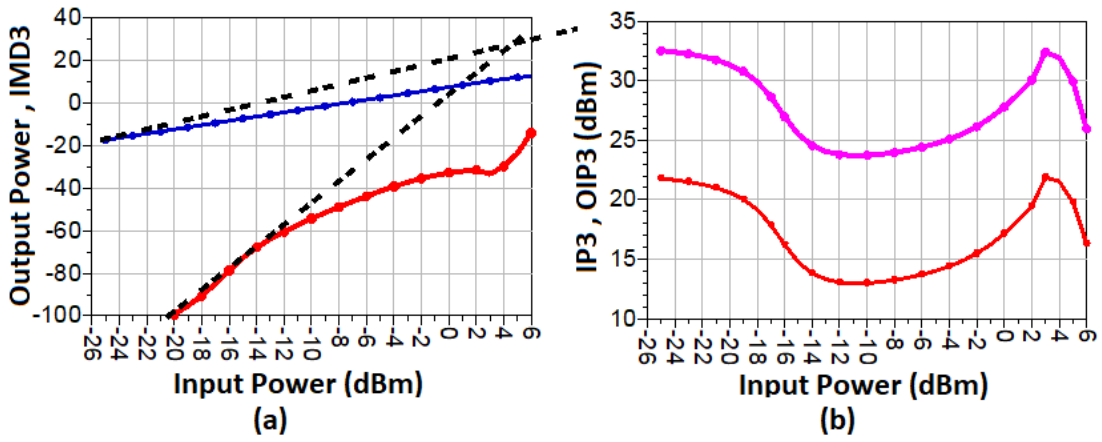

Figure 5-55 Simulated OIP3 and IIP3 of the UWB GaN LNA at 7 GHz with 10 MHz frequency spacing

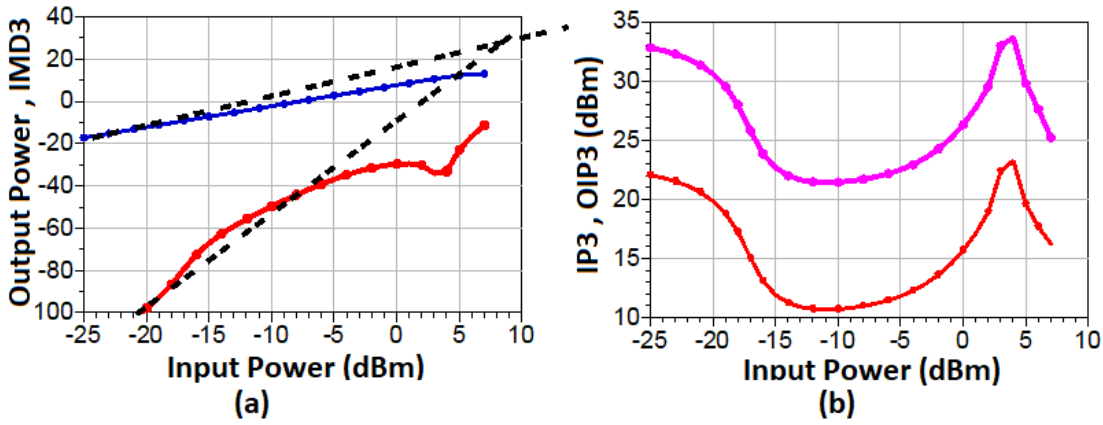

Figure 5-56 Simulated OIP3 and IIP3 of the UWB GaN LNA at 9 GHz with 10 MHz frequency spacing

5.9.Conclusion

In this chapter, three MMIC LNAs, using 0.25 um AlGaN/GaN HEMT technology were presented. The first LNA is designed for C-band space applications, using inductively source-degenerated with R-C feedback topology. The performance of the integrated C-band LNA shows that it offers 0.9-1.2 dB noise figure across the frequency band from 5 – 6 GHz. The MMIC

designed LNA, illustrates a P_{1dB} compression output power of 24 dBm and output third-order intercept point (OIP3) of 35 dBm, which shows a good linearity performance. A survivability study was also conducted on the LNA dies, and an assessment of the performance degradation, in terms of gain and noise figure, was carried out after a stress period of 16 hours and recovery period of 6 hours for an input driving signal level varying between 31-36 dBm. The second LNA is a two-stage design, based on inductively sourced degenerated topology with R-C feedback network. The performance of the designed LNA shows a noise figure of 0.9 ~1.3 dB and a gain of 23 ~ 25 dB at the frequency band from 5 to 6 GHz. The last LNA design is based on cascode configuration with RLC feedback network to achieve an ultra-wideband performance. The designed LNAs showed comparable noise performance with state-of-the-art MMIC LNA's designs, however, they offer better reliability, higher dynamic range, and strong survivability, to high input drives.

6. Conclusions

This Chapter summarizes the research work presented, and the conclusions drawn from this research, lists the contributions that have been achieved in this work, and suggests recommendations for future work.

6.1.Summary

The evolution of wireless communication systems shows that wideband operation must integrate different operating frequencies spectrums into one band. Thus, the transceiver's modules must operate across a broad frequency spectrum. Meanwhile, to be suitable for the multi-standards radio frequency (RF) systems, the power amplifiers and low noise amplifiers must be extended to the wideband operation mode. PAs' efficiency must be improved at power back-off to perform efficiently when driven by high envelope varying signals. These efficiency and bandwidth issues for the PAs were addressed in this dissertation. Several theories and design methods were proposed to improve the efficiency and to extend the bandwidth. The design methodologies, of wideband LNAs immune to high input drive and fabricated on the GaN/SiC substrate, were discussed in this thesis.

Chapter 2 surveys the power amplifier classes, recent trends in broadband, high-efficiency power amplifier modes of operation, and the different LNA topologies in this thesis.

In Chapter 3, a novel general broadband design methodology for Doherty architecture, based on three-port input and output combining and matching networks, is introduced. The approach introduces a systematic design approach for both input and output networks of the DPA. For broadband operation, a new design methodology was used to alleviate bandwidth limitations. For the first time, the three-port matching and combining networks were implemented using

MMIC technology. The proposed Doherty PA delivers 42 dBm peak power with an associated gain of 27.4 dB. Over the design band of 400 MHz, it exhibits PAE of 52% - 60% at peak power and of 38% - 51% at – 6 dB back-off.

Next, a new broadband DPA, based on a harmonic control network, is presented in Chapter 4. The DPA design is focused on manipulating harmonic components to improve bandwidth and efficiency. A proposed second harmonic impedance inverter is combined with a third harmonic suppression network, to realize short termination of the second harmonic component and open-circuit load condition for the third harmonic component, as viewed by both main and auxiliary amplifiers in the load modulation region. This new modified network creates a high-efficiency behavior over the frequency band from 1.1 to 1.8 GHz in the Doherty region. The fabricated DPA achieves a measured drain efficiency of 52.5–67.5 % at 6-dB output power back-off and 43–43.7-dBm saturated power. Measurements are in excellent agreement with simulation results which validates the proposed design methodology.

In Chapter 5, three different MMIC LNAs designs using 0.25 um AlGaN/GaN HEMT technology were carried out. The first one was a design based on common-source, with R-C feedback to operate in C-band. The performance of the integrated C-band LNA shows that it offers a 0.9-1.2 dB noise figure across the frequency band from 5 to 6 GHz. Also, this design topology provides excellent input and output matching response. A survivability study was also performed on the LNA dies, and the assessment of the performance degradation, in terms of the gain and noise figure, was carried out after a signal stress period of 16 hours and a recovery period of 6 hours, for an input driving signal level varying between 31-36 dBm. A non-recoverable

degradation of less than 0.5 dB in the gain, and 0.3 dB in the noise figure, was observed after the tested dies recovery period. The second design was a two-stage LNA, based on inductively source-degenerated topology with R-C feedback network. This design achieved a maximum gain higher than 23 dB and low noise characteristics of less than 1.2 dB, over a wideband frequency range from 5 to 6 GHz. The third one was a UWB LNA, based on cascode topology, with a series inductive source and using RLC frequency-dependent feedback network. The RLC frequency-dependent feedback network in this configuration is used to achieve the required broadband frequency operation with flat gain and minimum noise figure.

The design results in this thesis are cross-validated, comparing the results obtained by analytical simulation and experimental measurements. The simulations are conducted using commercial software, Advanced Design Systems (ADS).

6.2.Recommended Future Works

In this research, some basic theories and methods were proposed. In advance of that, several works can be carried out in the future.

1) Broadband DPA with an extended back-off region. The analysis and new design methodology of the three-port input and output networks can be developed and adopted throughout to enhance further the bandwidth of the Doherty amplifier and extending its back-off region up to (8-10 dB) output power level.
2) Multi-stage broadband DPA. To increase the high-efficiency back-off region in the Doherty power amplifier in order to meet the ever-increasing peak-to-average power ratio of modern waveforms. The use of multi-stage Doherty power amplifiers should be explored

to determine the feasibility of extending the back-off region up to (8-12-dB) output power level.

3) Harmonically tuned DPA with linearity enhancement. To improve the dynamic range and linearity of the DPA, several techniques have been proposed. These techniques can be also applied to the harmonically tuned DPA. This linearity enhancement technique can be realized, based on a third harmonic modulated network, which performing manipulation on the third harmonic component and keeping the fundamental load modulation is needed to achieve a linear Doherty power amplifier.
4) Design of a robust UWB single chip. The theories presented in this dissertation aim to design broadband components (PAs – LNAs), which is the T/R modules platform. One can explore different techniques and methods to design a full MMIC T/R chip that demonstrates an ultra-wideband GaN front-end module, covering most modern wireless applications.

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