Power Electronic Converters for Hybrid Micro-Grids

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doctoral thesis

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Abstract

In this thesis, topologies and control systems of power electronic converters for hybrid micro-grids are presented. In particular, the converters presented in this thesis are single-stage AC/DC and three-port DC/DC converters. These converters are derived from a common structure, which consists of a dual inductor connected to the switch node of two switches. This structure enables high control flexibility and gives rise to providing soft-switching.

A three-port nonisolated DC/DC converter and a new control system are proposed to integrate solar panels and energy storage in a DC micro-grid. The proposed control system utilizes the duty cycle as well as the switching frequency to control the power flow between the three ports. The proposed converter offers a low number of components, low cost, and high reliability.

A system that comprises a totem-pole isolated, non-resonant single-stage AC/DC converter with a variable frequency control system is presented. The proposed system improves the converter’s reliability by ensuring a constant dc-link voltage, which is independent of power flow. The converter uses small output capacitors to regulate the output current tightly. The converter achieves soft-switching at the turn-on of the MOSFETs. Moreover, it can achieve a high power factor and tight output current regulation. A new steady-state model was presented to describe the operation of the converter.

A variable duty cycle control (VDC) system is proposed for totem-pole isolated single-stage AC/DC converters. In the proposed VDC, the switches’ duty cycle is constant over a half mains period but different from each other in the negative and positive half mains periods. This feature allows high power efficiencies at low power operations. In the proposed VDC system, a new synchronization timing method and a new variable frequency modulation (FM) are introduced to mitigate the current surge issue in the transformer current at zero crossings of the mains grid. Furthermore, the time-domain analysis of the converter is presented for the VDC system.
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Abbreviations and Nomenclatures

Cmd command signal
CCM continuous conduction mode
CRM critical conduction mode
D duty cycle
DAB dual active bridge
DBR diode bridge rectifier
DCM discontinuous conduction mode
DERs distributed energy resources
DLI DC-link inductor
EMI electromagnetic interference
ESS energy storage system
EV electric vehicle
FM frequency modulation
HCS half cycle state
LED light-emitting diodes
MPC multi-port converters
MPPT maximum power point tracking
multi-port multiple port
MUX multiplexer
NHC negative half cycle
PF power factor
PCM peak current mode
PFM pulse frequency modulation
PFC power factor correction
PS preliminary signal
PV photo-voltaic
SIMO single-input-multiple-output
swt sawtooth
SISO single-input single-output
SOC state of charge
SR synchronous rectifier
TCM triangular current mode
THD total harmonic distortion
TPC three-port converter
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDC</td>
<td>variable duty cycle control</td>
</tr>
<tr>
<td>ZVS</td>
<td>zero voltage switching</td>
</tr>
<tr>
<td>$T_s$</td>
<td>switching cycle</td>
</tr>
<tr>
<td>$k_\theta$</td>
<td>displacement factor</td>
</tr>
<tr>
<td>$k_P$</td>
<td>distortion factor</td>
</tr>
<tr>
<td>$t$</td>
<td>time</td>
</tr>
<tr>
<td>$f_s$</td>
<td>switching frequency</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>DC-link voltage</td>
</tr>
<tr>
<td>$v_g$</td>
<td>grid/mains voltage</td>
</tr>
<tr>
<td>$i_g$</td>
<td>grid/mains current</td>
</tr>
<tr>
<td>$v_{S1}$</td>
<td>voltage across switch $S_1$</td>
</tr>
<tr>
<td>$v_{S2}$</td>
<td>voltage across switch $S_2$</td>
</tr>
<tr>
<td>$P_m$</td>
<td>input power</td>
</tr>
<tr>
<td>$P_o$</td>
<td>output power</td>
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</table>
Due to the adverse effects of using fossil energy on air pollution and global climate change, there has been a massive movement towards using renewable energy systems and distributed energy resources (DERs). This trend is replacing the conventional centralized power generation scheme with a distributed power generation scheme, in which micro-grids are the main building blocks [1]. A micro-grid is generally considered a small-scale grid that incorporates DERs, energy storage systems (ESSs), and loads [2, 3]. In micro-grids, DERs are typically placed close to the load, whereas, there is usually a long distance between the power source and loads in the centralized scheme. Thus, transmission losses and their costly installation are eliminated in the emerging distributed scheme [4]. Micro-grids can be AC, DC, or a hybrid combination of AC and DC. AC micro-grids utilize an AC distribution and are more compatible to operate in conjunction with the current AC grid infrastructure. They offer several advantages such as grid support, local control of the AC power, and resiliency in case of faults and failures in the AC grid. Therefore, AC micro-grids can enhance the performance and reliability of the current electrical power grid [4].

Due to the rapid change in the landscape of modern loads and sources, DC systems are becoming widely popular [5, 6]. In particular, DC micro-grids have recently gained much attention due to their attractive features. DC micro-grids offer a highly efficient, simple, and reliable solution to provide power for DC loads from DC sources such as solar modules. Thus, they are beneficial when dealing with DC loads such as light-emitting diodes (LED), variable speed drives and batteries (e.g., electric vehicle charging, computers, laptops, mobile phones, servers). However, since the loads are not all DC, and there are many AC loads, DC micro-grids alone are not currently a viable
solution to the distributed generation. Hybrid micro-grids can take advantage of both the AC and DC distributions; thus, enabling a much more efficient, flexible and reliable system than AC micro-grids. Due to its attractive features, many researchers believe that hybrid micro-grids are superior alternatives to AC micro-grids, and they are suitable for the vast implementation of the distributed generation systems. Figure 1.1 depicts an exemplary diagram of a hybrid micro-grid. According to this figure, the hybrid micro-grid includes both AC and DC distributions. Bidirectional power electronic converters are used to enable power transfer between the AC and DC distributions. In the hybrid micro-grid, DERs, ESSs, and loads are connected to the respective distribution rails (AC or DC) via power electronic converters. Power electronic converters are fundamental components to control the power flow between different components of the hybrid micro-grid. Thus, the focus of this thesis is on the design and development of various power electronic converters for hybrid micro-grids.

Power electronic converters are used to perform appropriate power conversions such as DC
to AC (DC/AC), AC to DC (AC/DC) and DC to DC (DC/DC) in hybrid micro-grids. DC/DC converters are used to enable power transfer between DC sources and DC loads. In many cases, multiple port (multi-port) DC/DC converters are needed to allow power transfer between multiple DC sources and loads. In particular, photovoltaic (PV) modules are typically combined with ESSs as a backup source to complement their intermittent nature and deliver power to the loads in a reliable way. Thus, multi-port DC/DC converters are suitable for this application as depicted in Figure 1.1. In addition, AC/DC converters are used as the interface between the micro-grids AC distribution rail and DC loads such as LEDs and electronics. These converters can be categorized into two-stage and single-stage converters. Two-stage converters are the standard method as they offer high reliability and performance, while single-stage converters use fewer components with some compromise on the performance. Thus, high-performance AC/DC and DC/DC power converters play an essential role in realizing hybrid micro-grids.

In this thesis, novel power converters, along with their control systems, will be introduced, which are suited for hybrid micro-grids. A novel multi-port DC/DC converter and a control system are proposed to interconnect two DC sources to the DC distribution of a hybrid micro-grid. In addition, a new high-performance single-stage AC/DC converter, along with its control system, is proposed to provide power for DC loads from the AC distribution. The proposed power electronic converters offer many advantages for this application, such as inherent soft-switching for power semiconductors, simple and reliable control, high efficiency, and high power density.

In this chapter, the general background on some of the types, applications and requirements of multi-port DC/DC converters and AC/DC converters are described. Then, the thesis objectives, contributions, and organization will be explained.
1.1 Background

1.1.1 Multi-Port DC/DC Converters

Multi-port DC/DC converters are mainly used to reduce the number of components in DC/DC converters. These converters are used in applications where multiple DC sources/loads are connected. They are widely used in DC micro-grids, where multiple DC sources need to interact to provide reliable power for the loads. Figure 1.2 depicts an exemplary arrangement of a small scale DC micro-grid. According to this figure, solar energy harvesting systems are generally used with ESSs to complement intermittent solar energy and DC loads. Multi-port power converters are particularly suitable for integrating solar energy harvesting systems and ESSs inside a DC micro-grid. Figure 1.3 depicts the conventional way of using individual single-input single-output DC/DC converters to transfer power between DC micro-grids and other sources/loads. According to this figure, every source/load needs an individual switching leg to interact with the DC rail. That
is, each leg’s switching pattern is designed to control the power flow between one source/load and the DC micro-grid. Therefore, the DC micro-grid is the intermediate link for power flow between the sources and the loads.

### 1.1.2 Single-Stage AC/DC Converters

Single-phase AC/DC converters are widely used to convert AC voltage from the AC micro-grid to DC voltages suitable for DC loads. Figure 1.4 and Figure 1.5 depict two different types of AC/DC converters: single-stage AC/DC converters and two-stage AC/DC converters, respectively. As the name implies, single-stage AC/DC converters convert AC to DC power in one single stage, and it can be isolated or nonisolated. Two-stage AC/DC converters consist of a PFC pre-regulator AC/DC converter followed by a DC/DC converter; these pre-regulators can use nonisolated single-stage AC/DC converters [7–13]. The pre-regulator converts the AC voltage to a DC voltage on an intermediate DC-link bus. The DC/DC converter uses this DC-link bus as input to create a regulated DC voltage suitable for the load. Two-stage AC/DC converters are appropriate for applications that require high performance, such as strict regulation on the output current (negligible output current ripple) and high power factor correction (PFC).

One of the regulatory requirements for grid-connected AC/DC converters is to achieve a PFC and harmonic distortion compliant with grid regulatory standards. AC/DC switch mode-power converters impose non-linearities and draw non-sinusoidal current from the AC grid, which causes an increase in harmonic distortion and reactive power. There are strict regulations that limit the
permitted harmonic distortion on the AC grid. For example, Europe’s EN61000-3-2 code issued by the European power supply manufacturers association imposes limits on the harmonic contents of converters [14]. EN 61000-3-2 applies to all electronic equipment that draws an input current below 16A per phase connected to the low-voltage AC grid distribution network (for equipment exceeding 16 A per phase, EN 61000-3-12 may be applicable). There are four different categories of limitations, depending on the equipment and application:

1. Class A for balanced three-phase equipment (household appliances) excluding equipment identified as class D, tools (excluding portable tools), dimmers for incandescent lamps, audio equipment, and all other equipment except the ones stated in the other classes,

2. Class B for portable tools,

3. Class C for lighting equipment,

4. Class D for PC, PC monitors, radio, switch-mode power supplies. Input power $P \leq 600W$

More stringent total harmonic distortion (THD) regulations, such as JIS 61000-3-2 have also been introduced to regulate the input current drawn by electronic equipment (used in Japan) [15].

The THD of a current waveform is a measurement of its harmonic components and is given
by:

\[
THD = \sqrt{\sum_{n=2}^{\infty} \frac{I_n^2}{I_1}} = \frac{\sqrt{(I_{RMS}^2 - I_1^2)}}{I_1} 
\]  

(1.1)

where \( I_1 \) is the RMS of the fundamental component of the current, \( I_n \) is the RMS of the \( n^{th} \) harmonic of the current and \( I_{RMS} \) is the RMS of the current waveform.

Another measure of harmonic contents is the distortion factor \((k_d)\), which is calculated from:

\[
k_d = \frac{I_1}{I_{RMS}} = \frac{1}{\sqrt{1 + THD^2}} 
\]  

(1.2)

and \( k_d \) is between 0 to 1. When the current waveform is pure sinusoidal \((THD = 0)\), \( k_d = 1 \); \( k_d \) decreases as \( THD \) increases. Therefore, \( k_d \) is directly related to the quality of the current. However, it does not consider the phase-angle between the grid voltage and the current’s fundamental component. Thus, it does not fully capture the quality of the current waveform. Power factor \((PF)\) is a figure of merit that fully realizes the quality of the current drawn from the mains grid. That is, \( PF \) quantifies the net energy carried from the grid to the load and can be expressed as:

\[
PF = \frac{P_{avg}}{|S|} 
\]  

(1.3)

where \( P_{ave} \) is the average power, and \(|S|\) is the apparent power. Equation (1.3) can further be simplified as

\[
PF = \frac{P_{avg}}{|S|} = \frac{V_1 I_1}{V_{1} I_{RMS}} \cos(\theta) = \frac{I_1}{I_{RMS}} \times \frac{\cos(\theta)}{k_\theta} \rightarrow 
\]

\[
PF = k_d \times k_\theta 
\]  

(1.4)

where \( V_1 \) is the RMS value of the AC grid voltage, \( k_\theta \) is the displacement factor, and \( \theta \) is the phase angle.
angle between the current waveform’s fundamental component and the grid voltage (assuming that the grid voltage is purely sinusoidal). Similar to $k_d$, $k_\theta$ also varies from 0 to 1. When the current’s fundamental component is completely in phase with the grid voltage, $k_\theta = 1$.

According to (1.4), $PF$ encapsulates both the distortion factor ($k_p$) and the displacement factor ($k_d$). When $PF$ is equal to one, the current’s quality is at its best, and only real power is present. Otherwise, either the current has harmonic disturbances or the input voltage and the current’s fundamental component are displaced from each other (not synchronized). In either case, the RMS current drawn from the grid has to increase to provide the same amount of real power as when $PF = 1$; thus, resulting in higher conduction losses in the transmission line.

To comply with the harmonic limitations imposed by regulations such as EN61000-3-2 and JIS61000-3-2 and maintain high power-factor performance, PFC has to be incorporated in the design of AC/DC front-end converters.

### 1.2 Thesis Objective

In this thesis, research is conducted to investigate high-performance circuits and control systems for multi-port DC/DC converters and single-stage AC/DC converters.

The following are detailed objectives of this thesis:

1. Design and development of new nonisolated three-port DC/DC converters, which are capable of bidirectional power transfer in two ports and unidirectional in one port. The proposed converter is suitable for integrating a PV module and an ESS into a DC micro-grid. It can also be used to provide power to two loads with high voltage gain from a DC input (e.g., DC power supply). A new control system is proposed that uses the switching frequency and the duty cycle to control the power flow on the three ports.

2. Design and development of a new system that comprises an isolated single-stage AC/DC converter and control system. The system provides the following features:
   
   (a) Constant DC-link voltage over wide operating power.
(b) Tight output current while achieving a near unity power factor
(c) Inherent soft-switching for all the switches.
(d) Reduced reactive current in the transformer winding.

1.3 Thesis Contribution

The major novilites and contributions of this thesis are summarized below:

1. A new three-port DC/DC converter is proposed that uses two active switches. The proposed converter can provide bidirectional power flow in two ports and unidirectional power flow in one port.

2. A mathematical model for the steady-state operation of the three-port DC/DC converter is proposed that captures the power flow. The steady-state model is further used to design converter parameters. The mathematical modelling for the AC large-signal and small-signal models of the DCM operation is provided.

3. A new multi-variable control system is introduced that uses both the duty cycle and the switching frequency to control the power flow between the three ports of the proposed three-port DC/DC converter. In particular, the duty cycle is used to control the power in one of the bidirectional ports and the switching frequency is used to control the power flow in the unidirectional port.

4. A new non-resonant single-stage AC/DC converter, which offers inherently achieve soft-switching for all power semiconductors. Moreover, it can provide constant DC-link voltage on the intermediate dc-bus.

5. A new equivalent circuit and mathematical model for the non-resonant single-stage AC/DC converter is proposed to allow better understanding and precise steady-state operation of the converter. A new large signal and small-signal AC analysis are proposed for DCM operation of the converter when variable frequency control is used to control the power flow.

6. A variable duty cycle control (VDC) system is proposed for totem-pole isolated single-stage
AC/DC converters. The proposed VDC can offer effective reduction of power flow, which allows achieving high power efficiencies at low power operations.

1.4 Thesis Organization

This thesis is organized into five chapters. In Chapter 2, a literature survey is performed on multi-port DC/DC converters and single-stage AC/DC converters. The three-port DC/DC converter is proposed in Chapter 3. This chapter also discusses the AC and DC analysis of the converter and provides component design for the converter. Moreover, a new multivariable control system is introduced to control, which uses the switching frequency and the duty cycle to control the power flow on the three ports. Chapter 4 proposes a new system comprised of an isolated single-stage AC/DC converter and a control system. In this chapter, a new DC modeling is introduced to investigate the DC analysis of the converter. In Chapter 5, a new duty cycle control system is proposed for totem-pole isolated single-stage AC/DC converters for DCM PFC operation. In Chapter 6, a summary of the thesis and relevant future work are presented.

The following journal papers and patents are based on the of this thesis:


- Iman Askarianabyaneh, Nicholas Adam Dohmeier, Majid Pahlevaninezhad, Christopher Jon Botting “Bridgeless single-stage AC/DC converter” U.S. Patent. No. 16576606, Issue date: Dec,2020

Constant DC-link Voltage", minor revision at IEEE Transactions on Industrial Electronics.
2 | Research Review

2.1 Introduction

Power converters are essential components, which are used to facilitate power transfer between elements (e.g., batteries, PV modules, LEDs) inside hybrid micro-grids. AC/DC converters are used to convert AC power from the AC distribution of hybrid micro-grids to DC power for loads such as batteries and LEDs. DC/DC converters are used to convert the DC power on the DC distribution of hybrid micro-grids to DC power compatible with the DC appliances. Multi-port DC/DC converters are used to enable power transfer between three or more sources/loads. These converters are particularly useful for applications that connect PV modules and ESSs to DC loads or in auxiliary applications that require multiple DC voltage levels from a single DC power supply.

This chapter reviews different types of single-phase multi-port DC/DC converters and single-phase AC/DC converters. The challenges related to specific subjects related to this thesis are identified.

2.2 Multi-Port DC/DC Converters

Single-phase multi-port converters (MPC) can be divided into two main categories: isolated and nonisolated. The power circuit of isolated MPCs are typically based on conventional methods such as full-bridge circuit with four switches for each port [16], half-bridge circuit with two switches for each port [17–20], and single-switch circuits with one switch for each port [21]. In the following,
some of the isolated MPCs will be briefly explained [22–43]. [32] proposes a three-port converter (TPC) that interfaces three power ports: a source, a bidirectional storage port, and an isolated load port by using two controlling variables. [33] proposes a topology that interfaces four power ports: two sources, one bidirectional storage port, and one isolated load port is proposed by adding two switches and two diodes to the traditional half-bridge topology. In [34], an isolated three-port bidirectional DC/DC converter is proposed, which manages power flow between multiple energy sources by using LCL resonant circuits. [35] proposes a TPC to enhance efficiencies for a standalone PV system, mainly when the battery operates at discharging mode. The converter utilizes a combined three-port LLC converter to share the PV and the battery load adaptively. In the converter, a shared resonant capacitor is used to couple two LLC resonant tanks and the fixed frequency operation allows an optimized LLC design for the converter. [36] proposes an isolated TPC, which uses a series resonant converter and a dual active bridge (DAB) converter for fast and slow EV charging applications. [38] proposes an isolated three-port LLC resonant converter. The control system uses a combination of pulse-frequency modulation and phase-shift control. The converter has four different operating modes, which offer various gains and different power flow directions between its three ports. Thus, this converter is suitable for applications that use renewable energy sources with an energy storage system. The converter operates with a resonant frequency, which can attain soft-switching for most of its switches and diodes the same ways as conventional LLC resonant converters.

In [37], a TPC is proposed to interconnect RERs with ESSs inside DC micro-grids. The converter is composed of an isolated series-resonance based TPC, which uses a hardware decoupling approach. The control system uses a unified autonomous structure, which is based on minimum value competition logic to manage power flow between the ports and regulate the voltage on the DC micro-grid bus. [39] focuses on investigating the power flow and the ZVS regions of an isolated series-resonant TPC, which operates in DC-transformer mode. [39] presents a mathematical model, which separates the circulating current from the primary currents enabling simple analysis. [40] proposes a system that consists of multiple modules controlled by PWM and phase-shift
control methods. Each input port is connected to a PV panel, which allows achieving MPPT, while the output ports are connected in series to provide a suitable interface with a high-voltage DC bus. [41] proposes an energy management and control scheme for a TPC used to interconnect PVs and ESSs in hybrid distributed power generation systems. The control system is designed to achieve MPPT and enhance the battery charging/discharging management by considering different power flow modes between the three-ports. [42] proposes an isolated MPC for connecting different PV panels. Multiple windings are used in a high-frequency transformer; only one is used for the output port, and the rest are used as input ports. Each of these input ports is connected to a PV panel through a two-quadrant inverter. A diode bridge is used to convert the transformer’s output port to a DC voltage connected to the load. The two-quadrant inverter only allows current to travel from the PV panel towards the transformer. In [43], an isolated MPC is proposed to interconnect PV panels and ESSs with a 380 V DC micro-grid. An isolated DC/DC converter with a high-frequency transformer is used to boost the PV and battery voltage to the DC micro-grid voltage. The ESSs are charged directly from the PV panels without using the high-frequency transformer, which effectively reduces the system’s power flow path. The converter can operate in an islanded or a grid-connected mode. The grid-connected mode can achieve maximum power point tracking (MPPT) for the PV panels while independently controlling the battery’s current. In the islanded mode, the control system regulates the voltage across the loads inside the DC micro-grid.

Non-isolated multi-port converters are given in [22, 23, 44–65]. In the following, some of these nonisolated MPCs will be explained. [52] presents a family of single-input-multiple-output (SIMO) DC/DC converters, which provides one step-up and multiple step-down outputs. The control switch of a conventional boost converter is used to regulate the boost output voltage, and additional switch nodes are implemented to generate step-down DC outputs. This converters advantage is that they utilize fewer switches and are more reliable due to their inherent shoot-through protection. Similar dynamic behaviour as the individual buck and boost converters is illustrated in this converter. Thus, the same control system in separate converters is used in this converter to precisely regulate each output. In [50], a systematic method is proposed to derive a multi-port
Figure 2.1: Multiport DC/DC converter based on DC-link inductor.

Figure 2.2: Schematic diagram of a soft-switched high step-up nonisolated TPC.

A high step-up three-port DC/DC converter is proposed in [49]. This converter employs two active clamp circuits and five power switches. In [53], an integrated multi-port converter is proposed that can achieves multiple regulated buck outputs. This converter can be used in the auxiliary power supply system of EVs, and it offers reduced switches as compared to conventional separate buck con-
In [54], a family of the three-port converter with variable structures is presented. This method’s advantage is that it removes output voltage restrictions because of its variable structures among ports and features a wide operational range. However, this method utilizes a higher number of semiconductors as compared to the previous methods. In [53], the converter uses $N+1$ switches to generate $N$-output voltages with unidirectional power flow for auxiliary power supply systems of electric vehicles (EVs). This converter operates similar to the conventional $N$ separate buck converters with the advantage of reduced switches. [55] presents an integrated three-port converter with single input double buck outputs. The converter uses three switches and two inductors. [56] proposes a nonisolated three-port converter with high voltage conversion ratios.

The converter can achieve zero input current ripple at the low voltage side for a wide range of duty cycles. [57] presents a nonisolated high step-up TPC capable of achieving soft-switching under various operating modes. The converter uses the coupled inductors technique to improve the voltage gain. [58] proposes an integrated TPC by replacing a switch and a diode with a basic cell in conventional single-input single-output (SISO) converters. [59] presents a high step-up TPC,
which can achieve soft-switching. A passive lossless snubber is used to attain a soft-switching without utilizing an additional semiconductor in the power train. [60] presents a high step-up TPC, which is based on a single-ended primary-inductor converter (SEPIC). The converter comprises two switches, which can either achieve zero voltage switching (ZVS) under high voltages. [61] proposes a stacked three-level TPC using GaN switches to interconnect RERs with ESSs to provide power for loads. The converter is derived from the asymmetrical half-bridge converter, which offers a simple control scheme and broad soft-switching region due to its active clamp configuration. The control system uses PWM and phase-shift control methods to control the power flow. [62] presents a buck-boost TPC for EVs. This converter can achieve high voltage gain and can operate with different voltage and current levels. The converter can operate in buck, boost, and buckboost mode with partial bidirectional power flow capability. In [63], a nonisolated high step-up TPC is presented, allowing two different paths of power flow between the input and output ports as depicted in Figure 2.2. The converter shares the same elements for transferring power to the battery and the load. In order to achieve high voltage gain, a coupled inductor technique is used. Two active clamp circuits are used to reduce the effect of the leakage inductance and provide soft-switching. In [64], a nonisolated MPC is proposed, integrating a PWM converter and a phase-shift control capacitor converter in standalone PV systems. The control system uses the duty cycle and the phase-shift angle to regulate the load, PV panel, and battery. Low RMS current can be achieved when the PV panel is not functioning, and the battery is in charging mode, which improves the power efficiency. In [65], a family of MPCs is proposed using pulsating current source cells to replace switches in conventional converters. The converter offers simplicity and a reduced number of switches. The mentioned nonisolated TPCs mostly provide buck output conversions and need three or more active switches to provide bidirectional power flow between at least two ports.

PV panels are typically used in conjunction with ESS to connect to DC micro-grids. The voltage of PV panels are typically lower than the battery and the DC micro-grid voltages. Thus, these applications require a TPC with bidirectional power flow in at least two of its ports and boost
output conversion. The previously mentioned nonisolated TPC converters with such capability use high number of active switches and passives components.

2.3 Single-Stage PFC AC/DC Converters

Figure 2.3 depicts one of the most common AC/DC converters, which consists of a diode bridge and a bulk capacitor. The diode bridge rectifies the grid voltage, and the capacitor \(C_o\) acts as an energy storage element to produce a DC voltage for the load. In this method, the diodes conduct for a short period. That is, the required output power is provided in this short interval, which in turn causes high input current \(i_g\) peaks. These high peak currents create stress on the diodes and affect their life expectancy. Moreover, the high \(THD\) due to the short interval of conduction typically surpasses the permissible harmonic limits enforced by the regulatory standards. Therefore, diode bridge rectifiers (DBRs) are not suitable for applications that require PFC. Passive and active circuitry can be added to DBRs to achieve PFC AC/DC conversion [66–69]. Passive PFC AC/DC converters use capacitors and inductors to reduce the input current’s harmonics and increase the power factor. For instance, one common way to improve the power factor and \(THD\) in DBRs is to use an inductor on the DC-side as depicted in Figure 2.4. In this configuration, the diode bridge will rectify the grid voltage. The inductor and the capacitor will filter out the rectified voltage to provide a dc voltage at the output. Increasing the inductor value stretches out the current and increases the diode commutation interval, which improves the \(THD\) and enhances the converter’s
Figure 2.6: Block diagram of average current mode control for boost converter and the respective input current waveform.

PFC performance. Other methods such as adding AC-side inductor, series resonant bandpass filter, parallel-resonance band stop filter, and harmonic trap filter have been proposed in the literature to achieve near-unity PFC in DBRs [69]. The main problem with passive PFC circuits, in general, is that they require bulky inductors and capacitors, which affect size, volume, and cost. Moreover, passive PFC methods are typically tuned for specific operating conditions. They are not suitable for achieving high power-factor in applications that need to operate over broad operating conditions (wide output current/voltage/power conditions or wide input voltage conditions). Active PFC methods were proposed as a remedy to these problems. Active PFC methods use switching devices such as IGBTs and MOSFETs to shape and control the input line current and perform PFC. One of the most basic active PFC converters is to replace the diodes with thyristors in Figure 2.4. The switching frequency used to control the thyristors are close to line frequency, which is about 50 Hz or 60 Hz. The advantages of this method are that it is simple, reliable and offers control-
Figure 2.7: Block diagram of peak current mode control for boost converter and the respective input current waveform.

lable output voltage regulations. However, the output voltage regulation is slow and bulky passive components such as inductor and capacitor are still required [69]. Active PFC methods with much higher switching frequencies than the line frequency have been proposed to decrease the size of inductors and capacitors. A common way to implement high-frequency active PFC is to use a diode bridge followed by different DC/DC converters. In principle, any DC/DC converter such as boost, buck, flyback, etc. can be used for this purpose.

The boost PFC converter shown in Figure 2.5 is one of the most common PFC AC/DC converter. In this method, a very simple topology is used that allows high $k_\theta$ and $k_d$, with near-unity power factor. This converter can achieve good performance for low power operations. As the power level increases, interleaving of two boost converters is often employed to improve efficiency and reduce the size of inductors and capacitors [70, 71]. Two very common control system structures are single-loop control or a cascade control. In single-loop control, the measured output voltage
Figure 2.8: Block diagram of hysteresis control for boost converter and the respective input current waveform.

is subtracted from a reference to create an error signal. The error signal is passed through a compensator (usually a linear proportional integral (PI) controller) and multiplied by a template of the rectified input voltage to create the control parameter for the input of the modulator. To increase the transient response of the control system, cascade control, which comprises of a slow transient outer loop control and a fast transient inner loop control is used. In the outer loop, the measured output voltage is subtracted from a voltage reference to create an error signal. The error signal is passed through a compensator and multiplied by a template of the input voltage to create the current reference for the inner loop. In the inner loop, the reference current is subtracted from the measured inductor current to create the error signal of the inner loop. The inner error signal is then passed through a compensator (typically fast transient PI controller) to create the input control parameter for the modulation. The modulation scheme is responsible for creating the switching
instants of the MOSFETs based on the control parameter. Depending on the type of the control, the modulator can be of different forms. Some of the common control methods are the average current mode control [72], peak current mode (PCM) control [73, 74], hysteresis control [75], one cycle control [76–78]. The inductor current waveform for positive half line-cycle (i.e. when the grid voltage is positive) and the control block diagram of these control methods are depicted in Figure 2.6, Figure 2.7, Figure 2.8, and Figure 2.9, respectively. The main difference between the average current mode, the peak current mode (PCM) and the hysteresis control are their modulation schemes. In average current mode, the control parameter is compared to a predetermined sawtooth waveform with fixed frequency. The output of the comparator will create the switching pattern of the MOSFET. In PCM, the control parameter will be connected to the negative terminal of a comparator (For control stability a positive ramp is subtracted from the control parameter) and the inductor current will be connected to the positive terminal of the comparator. The output of the comparator will be connected to the reset of a flip-flop. A predetermined clock with fixed frequency will be connected to the set of the flip-flop. The output of the flip-flop creates the switching pattern for PCM control. The structure of the hysteresis control is very similar to the peak current mode; except that in hysteresis control, the set of the flip-flop is determined by another comparator, in which the control parameter is connected to the positive terminal and the inductor current is connected to the negative terminal of the comparator. Therefore, both the peak and minimum of the inductor current can be controlled for every switching cycle. In one cycle control, a rather different approach is taken to control the output. The feedback of the control for this approach is the switch voltage. The switch voltage is passed through an integral. The output of the integral is compared to a voltage reference to create the switching pattern for the MOSFET.

Figure 2.10 depicts an interleaved boost PFC converter. In this method, the current is shared between inductors $L_1$ and $L_2$, which reduces the peak current in the inductors and MOSFETs. Thus, the size of these inductors and the current stress on the MOSFETs are reduced. Moreover, interleaving doubles the switching frequency, which reduces the input/output ripple current, and reduces the size of the electromagnetic interference (EMI) filter and the passive components (i.e.,
Control

Figure 2.9: Block diagram of one cycle control system for boost converter and the respective input current waveform.

Figure 2.10: Schematic diagram of the interleaved PFC converter.

Boost PFC converter has a voltage gain of more than unity. That is, the output DC voltage is higher than the maximum input AC voltage. In order to achieve a wide range of output voltage regulation, other DC/DC topologies such as buck, buck-boost, flyback, etc. were proposed in the literature [79, 80].

One of the most common ways of implementing a buck PFC AC/DC converter is depicted in Figure 2.11. The buck PFC converter can achieve high efficiency for wide input operating conditions, particularly when operated in critical conduction mode (CRM). PFC buck converters...
typically comprise a passive filter and a buck converter, as depicted in Figure 2.11. The output voltage \(V_o\) of the buck converter must be lower than the instantaneous input rectified voltage. Thus, when the input rectified grid voltage is higher than \(V_o\), the buck and the diode bridge conduct, and when the input voltage drops below \(V_o\), both the buck and the diode bridge shut off. In order to reduce the dead angle of the input current, \(V_o\) has to be considerably lower than the grid peak voltage [82–86]. In [87] a nonisolated buck PFC converter was proposed to improve the conduction angle. Figure 2.12 shows a single-stage PFC flyback converter. The converter utilizes only one output switch to perform both PFC and output regulation. The main disadvantage of this converter is large double-line frequency ripple at the output.

One of the major issues with the aforementioned PFC AC/DC converters are the conduction losses associated with the diode bridge rectifiers. To reduce these losses, bridgeless single-stage AC/DC converters were introduced. In [81, 88, 89], bidirectional bridgeless AC/DC and DC/AC converters were proposed, which can be used for EV to grid and grid to EV applications. These converters need many switches and gate drivers. Figure 2.13 depicts the bidirectional bridgeless
AC/DC converter presented in [81]. A current-fed half-bridge converter is used on the AC side and a full-bridge converter is used on the secondary side of a high-frequency transformer. The converter features zero current switching for the switches in the primary side and zero turn-on current for secondary side elements. The bridgeless single-stage PFC converters are mostly based on utilizing bidirectional switch, switch mode capacitors, symmetrical and asymmetrical structures, or totem-pole-based structures [87–104]. Each of these methods introduce a different structure, in which a comprise between the number of components (cost) and performance is made. In particular, there have been many attempts to overcome some of the main drawbacks of bridgeless singles-stage AC/DC converters such as hard switching, part soft-switching, and limited input voltage range. The bridgeless PFC converter with dual boost circuits is shown in Figure 2.14. The converter reduces one low frequency diode in the path for the grid current; hence, improving the efficiency compared with the conventional boost PFC converter [105].

A new bridgeless PFC AC/DC converter is proposed in [103] which is named the Manitoba
Rectifier (depicted in Figure 2.15). The converter can achieve wide range of output voltages by using a bridgeless single-stage topology. An LC filter is used to provide continuous current at the input terminal. [106] proposes a resonant bridgeless PFC AC/DC converter (depicted in Figure 2.16), which can achieve soft-switching for its semiconductors. That is, the converter can achieve zero voltage switching for its switches and zero current switching for its diodes.

Among the bridgeless methods, totem-pole bridgeless PFC converters depicted in Figure 2.17 have gained much attention due to their low common-mode noise interference, high device utilization, and lower number of components [91, 94, 97, 98]. According to Figure. 2.17, the totem-pole bridgeless PFC consists of one high frequency half-bridge switch leg ($S_1$ and $S_2$) and one low frequency half-bridge diode ($D_1$ and $D_2$) [105]. During the positive half line cycle, $D_2$ conducts, $S_2$ is the active switch and $S_1$ behaves as a synchronous rectifier (SR) switch; During the negative half line cycle, $D_1$ conducts, $S_1$ is the active switch and $S_2$ behaves as the SR [105]. That is, the totem-pole converter has one MOSFET and one low frequency diode conducting during each half line cycle; hence, reducing the conduction losses. The totem-pole converter’s conduction losses can further be decreased by replacing the diodes $D_1$ and $D_2$ with switches [107]. The drawback of the converter is that high frequency switches suffer from reverse recovery losses. In order to minimize the switching losses critical conduction mode (CRM) or discontinuous conduction mode (DCM) can be used. These operating modes allow a resonant switching transition between output capacitance of the MOSFETs and the inductor [107]. With proper control over the timing period of the switches reduced switching losses and ZVS can achieved in these modes. In conventional CRM, the SR switch turns off when the inductor current reaches zero. If the input voltage is lower that half of the output voltage, then ZVS can be achieved for the active switch; otherwise ZVS is not achieved and valley switching is used to minimize the switching losses [107]. To extend the ZVS range, triangular current mode (TCM) or quasi-square-wave mode has been introduced [105, 107, 108]. In the TCM, the SR MOSFET turns off when current has reached a required negative value [105, 107, 108]. The negative inductor current provides the storage energy required to discharge the output capacitance of the active switch and allow ZVS. Thus, a dual mode soft-
switching operation is used to achieve ZVS over the entire line cycle as depicted in Figure 2.18. According to this figure, CRM is used when $2v_g < V_o$ and TCM is used when $2v_g > V_o$. The on-time of the active switch can be used to achieve soft-switching for the totem-pole PFC converter. The on-time is determined based on the required average AC current from the grid [105, 107]. Alternatively, hysteresis current control [105] can be used to achieve soft-switching. In this control scheme, the upper and lower current references are used to generate the semiconductors’ switching instants. In this scheme, high speed isolated sensing of the inductor current is required, which could be challenging. To overcome this issue, current sensorless techniques and model predictive methods were introduced in [109–111].

In some applications isolation is a necessity due to user safety. Isolated bridgeless single-stage converters are proposed in [97, 112–115].

In [84] an bidirectional isolated bridgeless single-stage PFC is proposed, which uses four bidirectional switches on the primary of the transformer and four switches on the secondary of the
Figure 2.17: Schematic diagram of bridgeless totem-pole nonisolated AC/DC converter.

transformer. [112] proposes a single-stage interleaved Boost-LLC PFC converter. The converter uses four switches, two input diodes and an output diode bridge. [116] presents a single-stage AC/DC converter that is formed by integrating a boost PFC converter with a two switch clamped flyback converters. The converter uses a cascaded control loop to achieve PFC as well as intermediate bus voltage and output bus voltage regulation. $S^2PFC$ AC/DC converters simplify the two-stage PFC AC/DC converters and the DC/DC converters by sharing a single/pair of common switches. By allowing boost PFC converters to operate in DCM, PFC and fast output voltage regulation can be achieved with a single-loop controller. One of the main disadvantages of single-switch type $S^2PFC$ is the voltage spikes due to the leakage inductance of the transformer, which can cause damage to the switch and create higher losses. Two-transistor clamped isolated converters are used to clamp the switch stresses to the input voltage as well as recycling the energy stored in the leakage inductance back to the source. These converters have the downside of high
In some applications, output ripple-current output ripple current is limited and these single-stage methodologies are not suitable. [113] proposes a bridgeless dual-mode single-stage PFC converter as depicted in Figure 2.19. The converter uses a series-resonant circuit connected to an output voltage doubler. The converter can operate in both DCM and CCM. One of the most attractive structures of bridgeless single-stage converters is based on integrating nonisolated bridgeless totem-pole PFC converters with isolated DC/DC converters. Thus, a DC-link voltage is constructed that connects the two conversions. In these configurations, some of the switches and capacitors are shared between the two conversions causing reduced number of components compared to conventional two-stage AC/DC converters. In [117] a bridgeless single-stage AC/DC converter is presented (depicted in Figure 2.20), which consists of an isolated step-up AC/DC converter and a series-resonance circuit. The boost AC/DC converter operates in CCM while achieving PFC in the AC/DC conversion. The bridgeless configuration reduces the conduction losses and the series-resonance circuit provides zero current turn-on for the diodes and reduces its reverse-recovery losses. The issue with this converter is that it has high current ripple at the output terminal.

One of the main challenges of the bridgeless single-stage AC/DC converter with DC-link buses structure is that they have a variable DC-link voltage. The variable DC-link voltage is dependent on power flow due to a mismatch between input and output powers. Therefore, the voltage stress across power devices such as switches, diodes, and dc-link capacitors may increase under different
load conditions, which affects the reliability in these converters.

2.4 Summary

In this chapter, a literature review on three-port DC/DC converters and single-stage AC/DC converters was performed. It was identified that there is a need for nonisolated three port DC/DC converter that can achieve bidirectional power flow in at least two ports with two step-up outputs while mainlining low number of active switches and passive components.

Among single-stage AC/DC converters, totem-pole nonisolated AC/DC converters have gained much attention due to their low number of components, simple control systems, and high performance. Totem-pole isolated AC/DC converters are constructed by integrating totem-pole nonisolated bridgeless AC/DC converters with isolated DC/DC converters. This structure creates challenges such as variable DC-link voltage, which can affect the reliability in these converters. Although there has been existing research on improving totem-pole nonisolated AC/DC converters’ performance, the totem-pole isolated AC/DC converter still requires new systems and control methods to improve its reliability and power efficiencies.
3 | Three-Port DC/DC Converters

3.1 Introduction

The evaluated converters in this thesis stem from the dual inductor switch-node circuit shown in Figure 3.1. According to this figure, two inductors ($L_1$ and $L_2$) are connected to the switch node of a switch-leg. This structure provides high flexibility in controlling the current passing through the switches ($S_1$ and $S_2$) as there are two paths of current flow for each switch: through $L_1$ and through $L_2$.

As mentioned in the previous chapter, there is a need for nonisolated TPCs that can effectively integrate PV modules and ESS into DC micro-grids. This chapter proposes a nonisolated TPC based on the dual inductor switch-node circuit. Two different variations of the proposed TPC is presented. The proposed TPC can transfer bidirectional power in two ports and unidirectional flow in one port. It can also achieve boost output conversions from the unidirectional port to the bidirectional ports. The proposed TPC uses a new control system, which controls both the duty cycle and switching frequency to perform precise power flow management between these ports. The switching frequency controls the unidirectional power flow, and the duty cycle controls the bidirectional power flow. The proposed converter, along with the multi-variable control system, offers high flexibility in achieving soft-switching.

This chapter is organized as follows. In section 3.2, the proposed topology of the three-port DC/DC converter is given. The equivalent circuit and the steady-state operation of the converter is also investigated in section 3.2. In section 3.3, the AC modelling is presented. In section 3.4,
the proposed control system of the three-port DC/DC converter is given. In section 3.6, simulation and experimental results are provided.

### 3.2 Proposed Nonisolated Three-Port DC/DC Converter

Figure 3.2(a) and Figure 3.2(b) illustrate two different variations of the proposed TPC. According to the figure, the proposed TPC can be used to interconnect a PV module with ESSs inside a DC micro-grid. These two variations are very similar in operation; thus, in the following, the operation of variations 1 shown in Figure 3.2(a) will be discussed. According to Figure 3.2(a), the two ends of the switch-leg are connected to the DC-link (rails) of the DC micro-grid. There are two boost power conversions from the PV module and the battery to the DC-link of the grid. The PV panel boost conversion operates in DCM, while the battery boost conversion operates in CCM. The components of the PV module boost conversion are a boost inductor ($L_p$), a diode ($D$), a filtering capacitor ($C_p$), and two active switches ($S_1$ and $S_2$). The boost conversion components on the battery side boost consist of an inductor ($L_b$), a filtering capacitor ($C_b$), and the two active switches. Therefore, the two conversions share the two active switches. Another applications for the proposed TPC is shown in Figure 3.3, where an input DC power supply is connected to $V_{in}$ to provide power to two individual loads ($Load_1$ and $Load_2$) at two different voltage levels ($V_{o1}$ and $V_{o2}$).

A multi-variable control system is proposed to implement a power management system to control power flow in each port. In this control system, the switching frequency is used to regulate
the current in the PV module and the duty cycle is used to regulate the current in the battery. By using the power provided by the PV module ($P_{PV}$) and the absorbed power in the battery ($P_{bat}$), the power flow from the converter to the DC micro-grid can be determined. Thus, both the duty cycle and the switching frequency determine the power flow to the DC micro-grid.

### 3.2.1 Equivalent Circuit

Figure 3.4 shows the equivalent circuit for the proposed TPC. This figure’s top schematic shows a conventional method for integrating a PV module and battery into a DC micro-grid. This method
involves two distinct power conversion stages. The bottom schematic displays the equivalent circuit of the proposed TPC, which can be derived by sharing the two stages’ switching circuits. The current passing through the diode and the PV side inductor is modeled by the dependent current source ($i_p$). Therefore, $i_p$ models the unidirectional current and power flow from the PV module. In the following, $i_p$ and $i_b$ of the equivalent circuit are determined to perform the converter’s steady-state analysis. When the diode conducts, $i_p(t)$ is calculated as:

$$i_p(t) = \frac{1}{L_p} \int_{t_0}^{t} (V_{PV}(\tau) - v_{S2}(\tau)) d\tau + i_p(t_0) = \frac{1}{L_p} \int_{t_0}^{t} (V_{PV}(\tau) - S(\tau)V_{dc}) d\tau + i_p(t_0) \quad (3.1)$$
Figure 3.5: Illustration of current loops in different operating modes of the converter.

where

\[
S(t) = \begin{cases} 
1, & S_1 \text{ is on or } S_2 \text{ is off} \\
0, & S_1 \text{ is off or } S_2 \text{ is on} 
\end{cases}
\]

\(V_{PV}\) is the PV module voltage, \(v_{s2}\) is the voltage of \(S_2\), and \(V_{dc}\) is the DC micro-grid voltage. \(i_b(t)\) can be calculated in the same way by:
Figure 3.6: Illustration of the key waveform of the proposed converter.

\[
i_b(t) = \frac{1}{L_b} \int_{t_0}^{t} (v_{S2}(\tau) - V_{bat}(\tau)) d\tau + i_b(t_0) = \frac{1}{L_b} \int_{t_0}^{t} (S(\tau)V_{dc} - V_{bat}(\tau)) d\tau + i_b(t_0)
\]  

(3.2)

where \(V_{bat}\) is the voltage of the battery.

Figure 3.5 shows the modes of operation for the proposed TPC and the respective currents. According to this figure, the converter can operate in three different modes:

1. When \(S_1\) conducts (\(S(t) = 1\)), \(i_p\) decreases and \(i_b\) increases.

2. The diode will stop conducting when \(i_p\) goes negative. Thus, it will settle at zero till the next mode of operation. \(i_b\) will maintain its increasing slope similar to mode 1.

3. When \(S_1\) is off (\(S(t) = 0\)), the energy stored in \(i_p\) increases and \(i_b\) decreases. Thus, energy is stored in \(L_p\) and the stored energy in \(L_b\) is spent.

The voltages across \(L_p\) and \(L_b\) determine the behavior and slope of \(i_p\) and \(i_b\), respectively. Figure 3.6 shows the main voltages and current waveforms of \(L_p\) and \(L_b\) for all modes of operation. In the next subsection, the proposed circuit's power flow will be determined by using these waveforms.
3.2.2 Steady-State Operation

This section explains the steady-state operation of the proposed TPC. \( d_1 \) in Fig. 3.6 (the proportion of the required time for \( i_p \) to become zero after reaching its peak value divide by the total time period) can be calculated by using the voltage-second balance of \( L_p \) as:

\[
d_1 = \frac{V_{PV}}{V_{dc} - V_{PV}}(1 - D)
\]

(3.3)

\( D \) is the duty cycle.

In the proposed TPC, \( i_p \) has to operate in DCM; hence \( d_1 \) must be lower than \( D \). Therefore:

\[
V_{PV} < V_{bat} < V_{dc}
\]

(3.4)

The proposed TPC can achieve a unidirectional power flow from the PV module. This power can be derived as:

\[
P_{PV} = V_{PV}\langle i_p \rangle_{T_s}
\]

(3.5)

where

\[
\langle i_p \rangle_{T_s} = \frac{1}{f_s \int_{DT_s}^{(1+d_1)T_s}} i_p(t)dt
\]

(3.6)

by using (3.1), \( i_p(DT_s) = 0 \), and \( S(\tau) = u(\tau - T_s) \), and 3.6, where \( u(t) \) is the unit step function, the
average of $i_p$ for one switching cycle is written as:

$$\langle i_p \rangle_{T_s} = \frac{f_s}{L_p} \int_{DT_s}^{(1+d_1)T_s} \left( \int_{DT_s}^{t} (V_{PV}(\tau) - u(\tau - T_s)V_{dc}) d\tau \right) dt$$  \hspace{1cm} (3.7)

$$= \frac{f_s}{L_p} \int_{DT_s}^{(1+d_1)T_s} (V_{PV}(t - DT_s) - u(t - T_s)(t - T_s)V_{dc}) dt$$  \hspace{1cm} (3.8)

by using (3.3) and the steady-state relation $D = V_{bat}/V_{dc}$ in the above equation, the average of $i_p$ for one switching cycle is calculated as:

$$\langle i_p \rangle_{T_s} = \frac{V_{PV}V_{dc}}{2L_p f_s (V_{dc} - V_{PV})} (1 - D)^2$$  \hspace{1cm} (3.9)

$$\langle i_p \rangle_{T_s} = \frac{1}{2L_p f_s} \frac{V_{PV}(V_{dc} - V_{bat})^2}{V_{dc}(V_{dc} - V_{PV})}$$  \hspace{1cm} (3.10)

and the power provide by the PV module is calculated as:

$$P_{PV} = \frac{1}{2L_p f_s} \frac{V_{PV}^2 (V_{dc} - V_{bat})^2}{V_{dc}(V_{dc} - V_{PV})}$$  \hspace{1cm} (3.11)

Figure 3.7 shows the graph for PV module power versus the switching frequency ($f_s$). According to this figure, $P_{PV}$ has an inverse relation with $f_s$. Thus, it gives an intuitive idea of regulating the PV module’s power by adjusting the switching frequency.

The battery side operates in CCM, and its power can be calculated from:

$$P_{bat} = \frac{1}{T_s} \int_{0}^{T_s} V_{bat}i_b(t) dt = V_{bat} \langle i_b \rangle_{T_s} = V_{bat}I_{bat}$$  \hspace{1cm} (3.12)

where $\langle i_b(t) \rangle_{T_s}$ is the average of $i_b$ over a switching cycle. $\langle i_b(t) \rangle_{T_s}$ can be regulated by changing the duty cycle in transient (in transient, the duty cycle is controlled to change $\langle i_b(t) \rangle_{T_s}$, while at steady-state, the duty cycle is kept at $D = V_{bat}/V_{dc}$).
The transferred power to the DC micro-grid is calculated as:

\[ P_g = -V_{dc} \langle i_{s1} \rangle_{Ts} \quad (3.13) \]

where \( i_{s1} \) is the drain-source current of \( S_1 \) and its average, \( \langle i_{s1} \rangle_{Ts} \), in a lossless conversion is derived as

\[ \langle i_{s1} \rangle_{Ts} = \frac{1}{V_{dc}} \left( V_{bat} \langle i_b \rangle_{Ts} - V_{PV} \langle i_p \rangle_{Ts} \right) \quad (3.14) \]

by using (3.10) and (3.13) and (3.14), \( P_g \) is calculated as:

\[ P_g = V_{PV} \langle i_p \rangle_{Ts} - V_{bat} \langle i_b \rangle_{Ts} \quad (3.15) \]

\[ P_g = \frac{V_{PV}^2(V_{bat} - V_{dc})^2}{2f_s L_p(V_{dc} - V_{PV})} - \langle i_b \rangle_{Ts} V_{bat} V_{dc} \quad (3.16) \]

The currents flowing through the inductors \( L_p \) and \( L_b \) are used to regulate each port’s power. The duty cycle and the switching frequency can be used to control these currents.
3.3 AC Modeling

The DCM conversion with frequency variation control is derived by using the average switch model, and the PWM CCM conversion is derived by state-space averaging. Figure 3.8(a) shows the AC large-signal model for the DCM conversion. The input and output signals for this figure are expressed as:

\[
\langle v_1 \rangle = \langle v_{pv} \rangle \quad (3.17)
\]
\[
\langle v_2 \rangle = \langle v_{dc} \rangle \quad (3.18)
\]
\[
\langle i_1 \rangle = \langle i_b \rangle = \frac{D^2}{2 L_p f_s} \frac{\langle v_1 \rangle \langle v_2 \rangle}{\langle v_2 \rangle - \langle v_1 \rangle} \quad (3.19)
\]
\[
\langle i_2 \rangle = \frac{D^2}{2 L_p f_s} \frac{\langle v_1 \rangle^2}{\langle v_2 \rangle - \langle v_1 \rangle} \quad (3.20)
\]
The nonlinear performance of the AC large-signal model of the DCM conversion can be seen in (3.19) and (3.20). These average current and voltage waveforms are functions of time \( t \), and their averages are provided for one switching period \( T_s \). In order to have simple notations, \( T_s \) and \( t \) are disregarded from the equations.

It can be seen that (3.19) and (3.20) are functions of \( f_s \), \( \langle v_1 \rangle \) and \( \langle v_2 \rangle \). Therefore, they can be written as:

\[
\langle i_1 \rangle = h_1(\langle v_1 \rangle, \langle v_2 \rangle, f_s) \\
\langle i_2 \rangle = h_2(\langle v_1 \rangle, \langle v_2 \rangle, f_s)
\]

These equations can be linearized at one operating point to create the small-signal model. To do this, they are expressed by Taylor series expansion, at a specific operating condition of \( V_1, V_2, \) and \( F_s \). The taylor series expansion of \( \langle i_1 \rangle = h_1(\langle v_1 \rangle, \langle v_2 \rangle, f_s) \) is given as:

\[
I_1 + \hat{i}_1 = h_1(V_1, V_2, F_s) + \frac{1}{r_1} \hat{v}_1 + g_1 \hat{v}_2 + j_1 \hat{f}_s
\]

where

\[
\begin{align*}
\frac{1}{r_1} &= \left. \frac{\partial h_1(\langle v_1 \rangle, V_2, F_s)}{\partial \langle v_1 \rangle} \right|_{\langle v_1 \rangle = V_1} = \frac{D^2}{2L_pF_s} \frac{V_2^2}{(V_2 - V_1)^2} \\
g_1 &= \left. \frac{\partial h_1(V_1, \langle v_2 \rangle, F_s)}{\partial \langle v_2 \rangle} \right|_{\langle v_2 \rangle = V_2} = -\frac{D^2}{2L_pF_s} \frac{V_1^2}{(V_2 - V_1)^2} \\
j_1 &= \left. \frac{\partial h_1(V_1, v_2, f_s)}{\partial f_s} \right|_{f_s = F_s} = -\frac{D^2}{2L_pF_s^2} \frac{V_1V_2}{(V_2 - V_1)}
\end{align*}
\]

Equaling the AC and DC equation of each side of (3.21) results in the following:
\[ I_1 = h_1(V_1, V_2, F_s) = \frac{1}{8L_p F_s} \frac{V_1 V_2}{V_2 - V_1} \quad (3.22) \]

\[ \hat{i}_1 = \frac{1}{r_1} \hat{v}_1 + g_1 \hat{v}_2 + j_1 \hat{f}_s \quad (3.23) \]

The Taylor series expansion of \( \hat{i}_2 = h_2(\langle v_1 \rangle, \langle v_2 \rangle, F_s) \) can be derived in the same way. The AC and DC terms of this expansion are derived as:

\[ I_2 = h_2(V_1, V_2, F_s) = \frac{1}{8L_p F_s} \frac{V_1^2}{V_2 - V_1} \quad (3.24) \]

\[ \hat{i}_2 = -\frac{1}{r_2} \hat{v}_2 + g_2 \hat{v}_1 + j_2 \hat{f}_s \quad (3.25) \]

where

\[
\frac{1}{r_2} = \left. \left( -\frac{\partial h_2(V_1, \langle v_2 \rangle, F_s)}{\partial \langle v_2 \rangle} \right) \right|_{\langle v_2 \rangle = V_2} = \frac{D^2}{2L_p F_s} \frac{V_1^2}{(V_2 - V_1)^2},
\]

\[
g_2 = \left. \left( \frac{\partial h_2(\langle v_1 \rangle, V_2, F_s)}{\partial \langle v_1 \rangle} \right) \right|_{\langle v_1 \rangle = V_1} = -\frac{D^2}{2L_p F_s} \frac{V_1 (V_1 - 2V_2)}{(V_2 - V_1)^2},
\]

\[
j_2 = \left. \left( \frac{\partial h_2(V_1, V_2, \langle f_s \rangle)}{\partial \langle f_s \rangle} \right) \right|_{\langle f_s \rangle = F_s} = -\frac{D^2}{2L_p F_s^2} \frac{V_1^2}{V_2 - V_1}
\]

Figure 3.8(b) shows the small-signal model given in (3.23) and (3.25). In order to validate the small-signal model, first the theoretical derivation of the transfer function for the frequency to output current \( (G_{if}) \) is calculated when an example load shown in Figure 3.9.

\[
G_{if} = \frac{\hat{i}_R(s) | \hat{v}_1 = 0}{\hat{f}(s)} = \frac{D^2 V_1^2 (V_1 - V_2)}{Den(s)} \quad (3.26)
\]
Figure 3.9: Test circuit to validate the small signal modeling given in Figure 3.8(b).

where

\[
\text{Den}(s) = F_s \left( 2F_s L(V_1 - V_2)^2 \left( C_2 s (C_o L R_s^2 + L_s + R_s) + C_o R_s + 1 \right) + D^2 V_1^2 (C_o L R_s^2 + L_s + R_s) \right)
\]

(3.27)

Then, the theoretical expression given in (3.26) is compared with simulation results (achieved by AC sweep in PSIM simulation). The Bode plots for the simulation and theoretical results are shown in Figure 3.10. According to the figure, the theoretical and the simulation results corresponded well.

The PWM control for the CCM small-signal operation can be calculated as [118]:

\[
L_b \frac{d \hat{i}_b}{dt} = D \hat{v}_{dc} + dV_{dc} - \hat{v}_{bat} + R \hat{i}_o
\]

(3.28)

\[
RC_o \frac{d \hat{i}_o}{dt} = \hat{i}_b - \hat{i}_o
\]

(3.29)

By using the Laplace transform, the following equation is derived.

\[
\hat{i}_o(s) = \frac{\hat{d}(s)V_{dc} + D \hat{v}_{dc}(s)}{R + L_b s + C_b L_b R_s^2}
\]

(3.30)

The transfer function \(G_{i_{o,d}}\) is calculated as

\[
G_{i_{o,d}} = \frac{\hat{i}_o(s)|_{\hat{v}_{dc}=0}}{\hat{d}(s)} = \frac{V_{dc}}{R + L_b s + C_b L_b R_s^2}
\]

(3.31)
Figure 3.10: Bode diagrams for the DCM operation of the proposed converter transfer function $G_{if}$: theoretical (line) and simulation (markers).

The theoretical small-signal equations given in (3.31) were verified by comparing them to simulation results (AC sweep in PSIM simulation). The Bode plots for the simulation and theoretical results are depicted in Figure 3.11. The Bode diagrams expressed in (3.11) and the one from the simulation corresponded well.
3.4 Proposed Control System for the Proposed TPC

The proposed control system for the TPC is described in this section. In particular, a two-variable control system is proposed to regulate the three ports’ power flow. When the DC micro-grid is connected, MPPT is performed by the PV module; the current in the battery is determined by the state of charge (SOC). The power in the third port (DC micro-grid) is determined by calculating the difference between the PV module’s supplied power and the charging/discharging power of the battery. When the converter operates in the islanded mode, the DC micro-grid voltage has to be regulated, which can be achieved by using droop control. The block diagram for the control system
is shown in Figure 3.12. There are two control freedoms in the proposed control system: the duty cycle ($D$) and the switching frequency ($f_s$). Two individual feedback loops are used to create these control variables. The initial feedback loop creates $D$, hence, regulating the battery’s power. The other feedback loop creates $f_s$; hence, controlling the power harvested by the PV module. When the DC micro-grid is connected, the MPPT is used to create the PV module’s reference ($i_{ref}^p$), and the SOC is used to create the battery’s reference ($i_{ref}^b$). When the converter is operating in islanded mode, the droop control is used to create the references. The operating mode selection is performed by two multiplexers (MUX), which enables creating the proper $i_{ref}^p$ and $i_{ref}^b$. $D$ and $f_s$ are created using the reference signals and the current feedback from the PV module and the battery.

The mode of operation is determined by the MUXs in Figure 3.12 and their command signal (i.e. $Cmd$). When the converter is operating in islanded, the droop control regulates the bus voltage $V_{dc}$ by changing the reference signal. When the DC micro-grid is connected, the grid regulates $V_{dc}$. In this scenario, maximum power is harvested from the PV module by creating the proper reference
3.5 Performance Analysis

In this section, the impacts of different circuit parameters on the performance of the proposed circuit and the design flexibility for different applications are investigated.

3.5.1 PV-Side Parameters

The components of the PV-side consist of $L_p$ and $C_p$. This subsection describes the designs of $L_p$ and $C_p$. By using (3.11), $L_p$ can be expressed as:

$$L_p = \frac{1}{2(f_p)} \frac{V_{PV}^2(V_{dc} - V_{bat})^2}{V_{dc}(V_{dc} - V_{PV})}$$  \hspace{1cm} (3.32)

where $f_p = P_{PV} f_s$.

$L_p$ can be designed by using Figure 3.13. Figure 3.13 depicts a 3-D plot with the following axes: $L_p$, $P_{PV}$, $f_s$. Figure 3.13(b) depicts the value of $L_p$ with respect to $V_{dc}$ and $f_p$. Figure 3.13(b) shows that $f_p$ is an important parameter in the design of $L_p$. This is because $f_p$ is different for every value of $L_p$ for a constant $V_{dc}$.

The maximum core flux density in $L_p$ is relevant to the peak current $I_{p,max}$ passing through $L_p$. Thus, this parameter is important when designing the core. $I_{p,max}$ is calculated as:

$$I_{p,max} = \frac{2P_{PV}(V_{dc} - V_{PV})}{V_{PV}(V_{dc} - V_{bat})}$$  \hspace{1cm} (3.33)

The RMS of $i_p$ is required to derive the conduction losses in $L_p$. The RMS can be derived from
computing the DC element of $i_p$ and its harmonic contents. The Fourier Series of $i_p$ is given as:

$$i_p = \sum_{n=0,1,2,...}^\infty i_n e^{j\omega_n t}$$

where, $\omega_n = 2\pi nf_s$

$$i_n = \frac{P_{PV} V_{dc} (V_{dc} - V_{PV})}{2\pi^2 n^2 V_{PV}^2 (V_{bat} - V_{dc})^2} \times \left( (V_{PV} - V_{dc}) \cos \left( \frac{2\pi n (V_{bat} - V_{dc})}{V_{dc}} \right) + V_{dc} V_{PV} \cos \left( \frac{2\pi n V_{bat}}{V_{dc}} \right) \right) - V_{dc} V_{PV} \cos \left( \frac{2\pi n V_{bat}}{V_{dc}} \right)$$

(3.34)

The RMS harmonic contents of $i_p$ is calculated as:

$$I_{rms, p,n} = \frac{P_{PV} V_{dc} (V_{dc} - V_{PV})}{\pi^2 n^2 V_{PV}^2 (V_{bat} - V_{dc})^2} \left( V_{dc} (V_{PV} - V_{dc}) \cos \left( \frac{2\pi n (V_{bat} - V_{dc})}{V_{dc}} \right) + V_{dc} V_{PV} \cos \left( \frac{2\pi n V_{bat}}{V_{dc}} \right) \right) + V_{PV} (V_{dc} - V_{PV}) \cos \left( \frac{2\pi n (V_{bat} - V_{dc})}{V_{dc}} \right) + V_{dc}^2 - V_{dc} V_{PV} + V_{PV}^2 \right)^{1/2}$$

(3.35)
Figure 3.14: RMS current of the harmonics of \( i_p \) with respect to various PV panel power levels.

Figure 3.14 shows the RMS of the harmonic components of \( i_p \) versus the PV module’s power. Every individual plain shows the RMS of one of the harmonic components for a unique operating power. At every operating power, \( I_{p,max} \) and \( I_{p,n}^{rms} \) are dependent on the three ports’ voltages. (i.e., this can be seen from (3.33) and (3.35)). Therefore, the peak, average and RMS of the harmonic components in \( i_p \) are not impacted by \( L_p \) (due to variation in \( f_s \)).

\( C_p \) is designed to ensure minimal ripple current passing through the PV module. Thus, \( C_p \) has to be designed such that it approximately filters all the ripple from \( i_p \). This can be achieved by choosing sufficiently large capacitance as follows:

\[
C_p = \frac{L_p(I_{p,max} - \langle i_p \rangle T_s)^2}{2 \Delta V_{p,pp}} \left( \frac{V_{dc}}{V_{PV}(V_{dc} - V_{PV})} \right)
\]

\[
C_p = \frac{V_{PV}(V_{bat} - V_{dc})^2(V_{bat} - V_{PV})^2}{2 \Delta V_{p,pp} f_s^2 L_p V_{dc}(V_{dc} - V_{PV})^3}
\]

where \( \Delta V_{p,pp} \) is the peak-to-peak voltage ripple across \( C_p \).

### 3.5.2 Battery-Side Components

The main elements of the battery portion are \( L_b \) and \( C_b \). The current flowing through \( L_b \) (\( i_b \)) comprises a DC component and a small ripple (i.e., since it operates in CCM). The RMS of \( i_b \) (\( I_{b}^{rms} \)) is required to calculate the conduction losses, which can be used to choose the appropriate
The high frequency contents of $i_p$ are filtered by $C_b$, where $C_b$ is calculated as:

$$C_b = \frac{1}{8\Delta V_{b,pp}L_b f_s} \frac{V_{bat}(V_{dc} - V_{bat})}{V_{dc}}$$ (3.38)

where $\Delta V_{b,pp}$ is the peak-to-peak voltage across $C_b$.

### 3.5.3 DC-Bus Filtering Capacitor ($C_{dc}$)

The high frequency contents of $i_{s1}$ are filtered by the DC bus capacitor ($C_{dc}$). The current in $C_{dc}$ ($i_{C_{dc}}$) is shown in Figure 3.15. $C_{dc}$ can be calculated as:

$$C_{dc} = \frac{(I_{ng} + I_{p,max} - I_{b,min})^2}{2\Delta V_{n,pp}(m_p + m_b)}$$ (3.39)

where,

$$m_p = \frac{V_{dc} - V_{PV}}{L_p},$$

$$m_b = \frac{V_{dc} - V_{bat}}{L_b},$$

and $\Delta V_{n,pp}$ is the desired peak-to-peak voltage across $C_{dc}$. 

![Figure 3.15: Current waveform of $C_{dc}$](image)
By substituting \( I_{ng} = \frac{P_g}{V_{dc}} \), (3.33) and \( I_{b,\text{min}} = I_{bat} - \frac{D_{mb}}{2f_s} \), \( C_{dc} \) can be calculated as:

\[
C_{dc} = \frac{L_b L_p}{2\Delta V_{pp} (L_b (V_{dc} - V_{PV}) + L_p (V_{dc} - V_{bat})))} \times \\
\left(\frac{V_{bat} (V_{dc} - V_{bat})}{2 f_s L_b V_{dc}} + \frac{P_{PV} - P_{bat}}{V_{dc}} - \frac{P_{bat}}{V_{bat}} + \frac{2 P_{PV} (V_{dc} - V_{PV})}{V_{PV} (V_{dc} - V_{bat})}\right)^2
\]

(3.40)

3.6 Simulation and Experimental Results

This section provides the simulations and experimental results for the proposed TPC. The specifications of the converter are given in TABLE 3.1. Figure 3.16 depicts the simulation results for \( i_p, i_b, \) and \( v_s2 \). According to this figure, \( i_p \) is operating in DCM while \( i_b \) is operating in CCM. Figure 3.17 shows the key waveforms of the converter, \( v_s2, i_p, \) and \( i_b, \) when the PV panel and the battery are providing power to the DC micro-grid. Figure 3.18 depicts the current passing through switches \( S_1 \) and \( S_2 \) with respect to their gate-source voltage. According to this figure, the switch current is negative at the turn-on instant of both the switches; hence, enabling ZVS. Figure 3.19 depicts the transient response's simulation results for a positive and negative step change in the reference of the battery current. During this transient, the duty cycle changes to alter \( i_b, \) and at steady-state, the duty cycle settles at 0.28. Figure 3.20 depicts the transient response for a positive and negative step change in the reference current of the PV module. According to this figure, during transient \( f_s \) changes to regulate \( I_{pv} \) and at steady-state, the frequency settles at different values for different \( I_{pv}. \)
Table 3.1: Specifications & parameters of the experimental prototype.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_p$</td>
<td>PV inductor</td>
<td>28 $\mu H$</td>
</tr>
<tr>
<td>$L_b$</td>
<td>Battery inductor</td>
<td>5 $mH$</td>
</tr>
<tr>
<td>$C_{bat}$</td>
<td>Battery-side capacitor</td>
<td>10 $\mu F$</td>
</tr>
<tr>
<td>$C_{dc}$</td>
<td>DC-bus capacitor</td>
<td>33 $\mu F$</td>
</tr>
<tr>
<td>$C_{PV}$</td>
<td>PV-side capacitor</td>
<td>47 $\mu F$</td>
</tr>
<tr>
<td>$P_{PV}$</td>
<td>PV power</td>
<td>50 – 250 W</td>
</tr>
<tr>
<td>$V_{bat}$</td>
<td>Battery voltage</td>
<td>48 V</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>DC micro-grid voltage</td>
<td>170 V</td>
</tr>
</tbody>
</table>

Figure 3.16: Simulation results for the high frequency current waveforms with respect to the drain-source voltage across switch $S_2$. 
Figure 3.17: Simulation results of $v_s2$, $i_b$, and $i_p$ when the PV panel and the battery are providing power.

Figure 3.18: Simulation results for switch current with respect to the gate-source voltages.
Figure 3.19: Simulation results of transient response for a positive and negative step change of reference battery current.
An experimental prototype is built to validate the proposed TPC’s practicability and verify the claims mentioned in this chapter. The experimental prototype is depicted in Figure 3.21 along with the diagrams for the power stage and the control system. 170 V
An Intel Field-Programmable Gate Array (FPGA) is used to realize the digital control system. The digital control system shown in Figure 3.21 is performed inside the FPGA by using VHSIC Hardware Description Language (VHDL) as the programming language. A variable duty cycle and frequency modulation is the basis of the proposed control system. Two feedback loops are used to create these control variables. The initial feedback loop creates $f_s$, and the second feedback loop creates $D$. The PV module’s current is adjusted by varying $f_s$. This is achieved by changing the reference current of the PV module inside the control system. According to Figure 3.21, MPPT segment takes the PV modules’ voltage and current; thus, producing the reference for the PV module. A compensator is then used to create a sawtooth waveform with a variable switching period ($T_s$).

The energy supplied/absorbed by the battery is controlled by $D$. According to Figure 3.21, the loop including the SOC segment creates a reference for the battery current. This reference signal is then used to change the duty cycle. At the final stage, a PWM signal is created by comparing the sawtooth waveform with $D$, which is shown in Figure 3.21.
The voltage across the diode ($v_D$) and the current passing through $L_p$ ($i_p$) are shown in Figure 3.22(a). When $v_d = 0$ (diode conducts), then $i_p$ is positive. $v_d$ oscillates after the zero crossing of $i_p$. The resonance between $L_p$ and the diode’s junction capacitance is the underlying reason for this oscillation. In practice, the next switching state begins before allowing the oscillation to settle (i.e., given enough time, $v_D$ will settle at $v_D = V_{dc} - V_{PV}$, which results in $V_L = 0$). The voltage across $S_1$ ($v_{s1}$) and $i_p$ are shown in Figure 3.22(b). According to this figure, when $S_1$ is off ($S_2$ is on), $i_p$ has a negative slope and when $S_1$ is on ($S_2$ is off), $i_p$ has a positive slope. The unchanged shape $v_{s2}$ at steady-state can be modeled as a voltage source that divides the PV side elements from the other side.

Figure 3.23(a) depicts the current waveform of the battery inductor, $i_b$, and $v_{s1}$. The waveforms
Experimental waveforms for $i_b$ and $v_{s1}$.

(a) Experimental waveforms for $i_b$ and $v_{s1}$.

(b) Experimental key waveforms for different modes of operation.

Figure 3.23: Experimental results of (a) battery waveforms and (b) all the key waveforms.

for the battery current ($i_b$), $v_{s1}$ are shown in Figure 3.23(a). $i_b$ shows a continuous current operation.

When $v_{s1} = 0$ then $S_1$ is on and $i_b$ has a positive slope; when $v_{s1} = V_{dc}$ then $S_1$ is off and $i_b$ has a negative slope. Therefore, the mode of $S_1$ (and $S_2$) and their respective voltages across the switches greatly influence $i_b$. That is, $i_b$ is determined by the voltage across $S_1$ and $S_2$. $i_p$ is also determined by the voltage across $S_1$ and $S_2$. Therefore, $v_{s2}$ acts as a voltage source model that separates the PV from the battery side. Figure 3.23(b) shows the behavior of $i_p$ and $i_b$ versus $v_{s1}$ on the same graph. According to this figure, when $v_{s1} = 0$, $i_b$ increases and $i_p$ decreases (Mode 1). That is, the currents illustrate reverse slopes to each other. When $i_p$ reaches zero, the diode stops to conduct; hence, $i_p$ remains zero (Mode 2). In this interval, $i_b$ will continue its increasing trend since the boost conversion operates in CCM. When $v_{s1} = V_{dc}$, $i_p$ increases and $i_b$ decreases; hence, they
(a) ZVS is achieved for $S_1$ at turn-on.

(b) ZVS is achieved for $S_2$ at turn-on.

Figure 3.24: Experimental results for gate-source voltage and drain-source current of $S_1$ and $S_2$. show reverse trends to one another (Mode 3). The gate-source voltage and the switches’ current are shown in Figure 3.24. The gate-source voltage of $S_1$ ($v_{gs1}$) and the current in $S_1$ ($i_{s1}$) are depicted in Figure 3.24(a). It can be seen that at turn-on switching of $S_1$, the current passing through it is negative. The negative current discharges the output capacitor of $S_2$ in deadtime. Then, the body diode of $S_1$ conducts after the output capacitance of $S_1$ is fully discharged. The gate source voltage of $S_2$ ($v_{gs2}$) and the current in $S_2$ ($i_{s2}$) are shown in Figure 3.24(b). According to this figure, at turn-on instant of $S_2$, the current passing through $S_2$ is negative ($i_{s2} = -3.2\ A$). Thus, ZVS is achieved for both switches.
Figure 3.25: Experimental results of the PV-side and battery-side waveforms for medium PV power.

The experimental results for medium power ($P_{PV} = 150 \text{ W}$) is shown in Figure 3.25. Figure 3.25(a) shows $i_p$ and $v_{s1}$. When $v_{s1} = V_{dc}$, $i_p$ has a positive trend and when $v_{s1} = 0$, $i_p$ has a negative trend. $i_b$, and $v_{s1}$ are shown in Figure 3.25(b). The behavior of $i_p$ and $i_b$ versus $v_{s1}$ are shown in Figure 3.25(c).

The experimental results for low power ($P_{PV} = 85 \text{ W}$) is shown in Figure 3.26. Figure 3.26(a)
shows $i_p$ and $v_{s1}$; $i_b$, and $v_{s1}$ are shown in Figure 3.26(b). The behavior of $i_p$ and $i_b$ versus $v_{s1}$ are shown in Figure 3.26(c). Figure 3.26 and Figure ?? demonstrate the behavior and feasibility of the proposed converter and control system at various operating points.

Figure 3.26: Experimental results of the PV-side and battery-side waveforms for low PV power.
3.7 Summary

This chapter proposed a new nonisolated three-port DC/DC converter that can be used to interconnect a PV panel and a battery inside a DC micro-grid. The proposed converter can achieve a low number of elements and high reliability. The conversions from the PV panel to the battery and the DC-microgrid form two boost output conversions, where bidirectional power flow can be achieved for the battery and the DC micro-grid. A new control system was proposed to regulate the power harvested from the PV module and the absorbed/supplied power in the battery and the DC micro-grid.
4 | Totem-Pole Non-Resonant Isolated AC/DC Converter

4.1 Introduction

As mentioned in chapter 2, totem-pole isolated AC/DC converters have reliability and efficiency issues that need to be addressed. This chapter proposes a system that improves reliability of the converter while achieving high performance. In particular, a system is proposed that comprises a totem-pole isolated non-resonant AC/DC topology with variable frequency control. The active circuitry of the topology is based on the dual inductor switch-node circuit shown in Figure 3.1. The converter is capable of providing tight output current regulation while achieving a high power factor. Furthermore, it can provide soft-switching for all the switches. In the proposed system, the input and output power curves completely match each other, which causes the DC-link voltage to remain constant for all power levels; hence, improving the reliability of the system.

This section is organized as follows: Subsection (4.2) describes the isolated, non-resonant converter with variable frequency control. In section (4.3), the stability of the DC-link voltage is investigated. Section (4.4) presents the proposed control system. The qualitative performance of the converter is given in section (4.5). In section (4.6), simulation and experimental results are provided.
4.2 Totem-pole Isolated, Non-Resonant AC/DC Converter with Variable Frequency Control

4.2.1 Circuit & Operation

The schematic diagram of the totem-pole isolated, non-resonant AC/DC converter is shown in Figure 4.1. A boost AC/DC converter and an isolated nonresonant DC/DC converter are combined to create the converter shown in Figure 4.1. Thus, the conversion shares two power switches ($S_1$ and $S_2$) and two capacitors ($C_1$ and $C_2$) between the two conversions. The boost AC/DC comprises the two power switches, the two capacitors, an inductor ($L_b$), and two general-purpose diodes ($D_1$ and $D_2$). The isolated nonresonant DC/DC converter comprises a high-frequency transformer (turns-ratio of $n : 1 : 1$), a high-frequency inductor ($L_d$) (i.e., the leakage inductance of the transformer could be used for $L_d$), magnetizing inductance ($L_m$), the two capacitors, the two power switches, output capacitors ($C_o$), and output diodes ($D_{o1}$ and $D_{o2}$). $C_1$ and $C_2$ are not used for resonance and are only used to block DC current going through the transformer.

Figure 4.2 shows the steady-state operating modes of the converter for positive and negative half-cycles. The current loops of inductor boost current ($i_b$), transformer current ($i_s$), and output rectified current ($i_{rec}$) are drawn for each mode. Figure 4.2(a) shows seven different modes for one switching period ($T_s$) when the converter is operating in positive half cycle ($v_g > 0$).
Figure 4.2: Steady-state operating modes: boost inductor current ($i_b$), transformer primary current ($i_p$), and output rectified current ($i_{rec}$) are shown for each mode.
These modes are briefly elaborated below:

- At the beginning of mode 1, $S_1$ is turned on; hence, $v_p = \frac{1}{2}V_{dc}$. Diode $D_{o2}$ conducts. $i_b$ has a positive but decreasing value during this interval.

- Mode 2: In this mode, $S_1$ is still on, and $i_b$ continues to decrease till it reaches zero. However, the diode $D_{o1}$ starts to conduct in this interval.

- In mode 3, $S_1$ is still on but, $i_b$ has reached zero and stays at zero for the rest of this interval (in practice $i_b$ will have small oscillation around zero due to the junction capacitance of $D_1$ and $D_2$).

- Mode 4 is the deadtime interval. At the beginning of this mode, $S_1$ is turned off, while $i_s$ is positive. Thus, the output capacitor of $S_1$ is charged up to $V_{dc}$ and the body diode of $S_2$ conducts. This enables soft-switching for the turn-on of $S_2$ at the beginning of mode 5.

- At the beginning of mode 5, $S_2$ is turned on; hence, $v_p = -\frac{1}{2}V_{DC}$. $i_b$ is positive and increasing in this mode.

- Mode 6: the switch $S_2$ is still on, and $i_b$ continues to increase. However, the diode $D_{o2}$ starts to conduct in this interval.

- In mode 7, $S_2$ is turned off, and the switches enter deadtime interval. At the beginning of this mode, $i_b - i_p$ is positive. Thus, the output capacitor of $S_2$ is charged up to $V_{dc}$ and the body diode of $S_1$ conducts. This enables soft-switching for turning on $S_1$ at the beginning of mode 1.

The operating modes of the negative half cycle ($v_g < 0$) are depicted in Figure 4.2(b). These modes are similar to the ones in the positive half cycle.

### 4.2.2 Equivalent Circuit

A new equivalent circuit model for the proposed system is shown in Figure 4.3. According to the equivalent circuit, a voltage source ($v_{s2}$) can be used to break the AC/DC from the DC/DC conversion, where $v_{s2}$ models the voltage across switch $S_2$. $v_{s2}$ can be derived from $v_{s2}(t) = S(t)V_{dc}$, where $S(t)$ is the state of the switch for $S_1$. That is, when $S_1$ is on, $S(t) = 1$ and when
Figure 4.3: Equivalent circuit of the totem-pole isolated, non-resonant AC/DC converter.

$S_1$ is off then $S(t) = 0$. Therefore, $v_{s2}$ intuitively shows effective sharing of the two switches and the capacitors between the AC/DC conversion and the nonresonant isolated DC/DC conversion. Figure 4.3 shows that the AC/DC conversion comprises a current source ($i_{b,rec}(t)$), a grid voltage ($v_{g,rec}$), and $v_{s2}$. $i_{b,rec}(t)$ is derived from:

$$i_{b,rec}(t) = \frac{1}{L_b} \int_{t_0}^{t} (v_{g,rec}(\tau) - S(\tau)V_{dc})d\tau + i_{b,rec}(t_0) \quad (4.1)$$

According to Figure 4.3, the DC/DC isolated nonresonant converter is modeled by a voltage source ($V_{dc}/2$), the leakage inductance $L_s$, the magnetizing inductance ($L_m$), and a voltage source ($sgn(i_p(\tau))nV_o$). $i_p$, which is the current passing in the voltage source $sgn(i_p(\tau))nV_o$ is derived as:

$$i_p(t) = \frac{1}{L_s} \int_{t_0}^{t} \left( (S(\tau) - \frac{1}{2})V_{dc} - sgn(i_p(\tau))nV_o \right) d\tau + i_p(t_0) - \frac{1}{L_m} sgn(i_p(\tau))nV_o \quad (4.2)$$

where

$$sgn(i_p(t)) = \begin{cases} 1, & i_p(t) > 0 \\ 0, & i_p(t) < 0 \end{cases}$$

The converter’s key waveforms are shown in Figure 4.4 (modes of operation for different periods are shown). It can be seen that $i_p$ has a constant slope at each period, and $i_b$ is operating at DCM.
Since zero current switchings are achieved for the output diodes, the polarity of the transformer’s secondary voltage ($v_{s2}$) changes with the polarity of $i_p$.

### 4.2.3 Power

The input power for $v_{g,rec}$ ($P_{in}$) and the output power for $\text{sgn}(i_p(t))nV_o$ ($P_o$) in Figure 4.3 are calculated in this subsection. $P_{in}$ can be calculated as:

$$P_{in} = \langle v_{g,rec}i_{b,rec} \rangle T_g \quad (4.3)$$
where \( T_g \) is one main period. Eq. 4.3 can be written as:

\[
P_{\text{in}} = 2 \frac{f_s}{f_g} \sum_{n=1}^{N/2} \langle P[n] \rangle_T \tag{4.4}
\]

where \( \langle P[n] \rangle_T \) is the average power for one switching period, \( f_s \) is the switching frequency, \( f_g \) is the mains frequency (i.e. 50Hz or 60Hz), and \( N \) is the number of switching periods in one main period; therefore,

\[
N = \frac{T_g}{T_s} = \frac{f_s}{f_g} \tag{4.5}
\]

where \( T_s \) is the switching period.

\( \langle P[n] \rangle_T \) is calculated as:

\[
\langle P[n] \rangle_T = \frac{1}{T_s} \int_0^{T_s} v_{g, \text{rec}}(t) i_{b, \text{rec}}(t) \, dt = v_g[n] f_s \int_0^{T_s} i_{b, \text{rec}}(t) \, dt \tag{4.6}
\]

By using (4.1) and (4.6), \( \langle P[n] \rangle_T \) is derived as:

\[
\langle P[n] \rangle_T = \frac{1}{8 L_b f_s} \frac{v_g[n]^2}{1 - \frac{v_g[n]}{V_{dc}}} \tag{4.7}
\]

By using (4.7) and (4.4), the average of the input power is derived as

\[
P_{\text{in}} = 2 \frac{f_s}{f_g} \sum_{n=1}^{N/2} \frac{1}{8 L_b f_s} \frac{v_g[n]^2}{1 - \frac{v_g[n]}{V_{dc}}}
\]

\[
P_{\text{in}} = \frac{1}{4 L_b \pi f_s} \int_0^{\pi/2} \frac{v_g(t)^2}{1 - \frac{v_g(t)}{V_{dc}}} \, dt \tag{4.8}
\]

where \( v_g(t) = V_g \sin(t) \). Due to the capacitors, \( i_p \) does not have a DC value. Therefore, the output
power ($P_o$) consumed by the voltage source ($\text{sgn}(i_p)nV_o$) in Figure 4.3 can be derived from:

\[ P_o = \langle nV_o i_p \text{sgn}(i_p(t)) \rangle \tau_s = \frac{1}{T_s} \int_0^{T_s} nV_o i_p(t) \text{sgn}(i_p(t)) dt = nV_o f_s \int_0^{T_s} i_p(t) \text{sgn}(i_p(t)) dt \]

\[ P_o = \frac{nV_o (2nV_o(L_m - L_s) + L_m V_{dc})(2nV_o(L_m + L_s) - L_m V_{dc})}{16 f_s L_m L_s (2nL_s V_o - L_m V_{dc})} \]  \hspace{1cm} (4.9)

### 4.3 Stability of DC-Link Voltage

In this subsection, the output and input powers are used to investigate the DC-bus voltage. This can be achieved by $P_o = P_{in}$ (by assuming lossless conversion). By substituting (4.8) and (4.9) in $P_o = P_{in}$, $V_{dc}$ is given in an implicit equation:

\[ \frac{nV_o (2nV_o(L_m - L_s) + L_m V_{dc})(2nV_o(L_m + L_s) - L_m V_{dc})}{4L_m L_s (2nL_s V_o - L_m V_{dc})} = \frac{1}{L_b \pi} \int_0^{\pi/2} \left( \frac{v_g(t)}{V_{dc}} \right)^2 dt \]  \hspace{1cm} (4.10)
Equation (4.10) shows that $V_{dc}$ is not dependent on the operating power and $f_s$. Therefore, the converter’s reliability enhances since $V_{dc}$ does not vary with power. In similar totem-pole isolated resonant AC/DC converters, $V_{dc}$ is dependent on operating power; hence, as the power changes, $V_{dc}$ changes with it. The change in $V_{dc}$ and power in these converters is not necessarily linear, making it difficult to predict the highest potential $V_{dc}$. Therefore, high voltage stress can happen across elements such as the switches and the capacitors, affecting their life expectancy or damage them.

The steady-state operations of the two conversions are shown in Figure 4.5. The solid lines represent $f_s$ versus $V_{dc}$ for a given operating power, which are based on (4.8); the dotted lines represent $f_s$ versus $V_{dc}$ for a given operating power, which are based on (4.9). The converter’s operating point for a given $P$, $V_o$, and $V_{rms}$ can be determined by finding the crossing of a dotted and solid line for that $P$. Figure 4.5 shows that the three crossings for $P = 90$ W, $P = 150$ W, and $P = 250$ W all have the same voltage across the DC-bus. The main reason of variation in $V_{dc}$ for varying power is the mismatch between $P_{in}$ and $P_o$. Figure 4.6 shows that $P_{in}$ and $P_o$ in the proposed system (comprising of a totem-pole isolated, non-resonant AC/DC converter with variable frequency control) agree with one another, which allows $V_{dc}$ to maintain a steady value.
4.4 Variable Frequency Control System

According to (4.8) and (4.9), $P_{in}$ and $P_o$ are both inversely proportional to $f_s$. Therefore, $f_s$ can be used to control these powers simultaneously. That is, the output voltage ($V_o$) and the output current ($I_o$) are used as feedback for the control system. This reference is subtracted from the output power (calculated from $V_o$ and $I_o$) to create an error. The compensator (comp.) uses this error to create the switching frequency ($f_s$). $f_s$ is then passed to the variable frequency control (VFC) to create the switching instants of $S_1$ and $S_2$. In the following, an accurate AC modelling of the totem-pole isolated non-resonant AC/DC converter with the proposed variable frequency control is given.

AC Modeling

Figure 4.7 depicts the large-signal AC model of the converter. The large-signal AC model is constructed by using DCM averaged model of the switching circuit for the PFC conversion and state-space averaging for the PWM DC/DC conversion. The large-signal equations for the DCM averaged model of the switching circuit can be written as:

$$\langle v_1 \rangle = \langle v_{g,RMS} \rangle$$  \hspace{1cm} (4.11)

$$\langle v_2 \rangle = \langle v_{dc} \rangle$$ \hspace{1cm} (4.12)

$$\langle i_1 \rangle = \langle i_b \rangle = \frac{1}{8L_b f_s} \frac{\langle v_1 \rangle \langle v_2 \rangle}{\langle v_2 \rangle - \langle v_1 \rangle}$$ \hspace{1cm} (4.13)

$$\langle i_2 \rangle = \frac{1}{8L_b f_s} \frac{\langle v_1 \rangle^2}{\langle v_2 \rangle - \langle v_1 \rangle}$$ \hspace{1cm} (4.14)

These input and output signals are averaged over one switching cycle ($T_s$), and they are functions of time ($t$). In the proposed control scheme (for non-resonant), $f_s$ is the controlling variable. Therefore, $f_s$ is also a function of time ($t$). For simplicity of notation, $T_s$ and $t$ are omitted from the equations.

Equations (4.13) and (4.14) show that the large-signal average signals are nonlinear. The small-
signal equivalent model can be achieved by perturbation about a quiescent point and linearization of the large-signal switch network. Equations (4.13) and (4.14) are functions of the switching frequency ($f_s$) and terminal voltages ($\langle v_1 \rangle$ and $\langle v_2 \rangle$). That is

$$\langle i_1 \rangle = h_1(\langle v_1 \rangle, \langle v_2 \rangle, f_s).$$

This expression can be expanded by using Taylor series, about the quiescent operating point $(V_1, V_2, F_s)$, as follows:

$$I_1 + \hat{i}_1 = h_1(V_1, V_2, F_s) + \frac{1}{r_1} \hat{v}_1 + g_1 \hat{v}_2 + j_1 \hat{f}_s$$  \hspace{1cm} (4.15)

where

$$\frac{1}{r_1} = \frac{\partial h_1(\langle v_1 \rangle, V_2, F_s)}{\partial \langle v_1 \rangle} \bigg|_{\langle v_1 \rangle=V_1} = \frac{1}{8L_bF_s} \frac{V_2^2}{(V_2 - V_1)^2},$$

$$g_1 = \frac{\partial h_1(V_1, \langle v_2 \rangle, F_s)}{\partial \langle v_2 \rangle} \bigg|_{\langle v_2 \rangle=V_2} = -\frac{1}{8L_bF_s} \frac{V_1^2}{(V_2 - V_1)^2},$$

$$j_1 = \frac{\partial h_1(V_1, v_2, f_s)}{\partial f_s} \bigg|_{f_s=F_s} = -\frac{1}{8L_bF_s} \frac{V_1V_2}{V_2 - V_1}.$$

The DC and AC terms on both sides of (4.15) must be equal. Therefore,
\[ I_1 = h_1(V_1, V_2, F_s) = \frac{1}{8L_bF_s} \frac{V_1V_2}{V_2-V_1} \quad (4.16) \]

\[ \hat{i}_1 = \frac{1}{r_1} \hat{v}_1 + g_1 \hat{v}_2 + j_1 \hat{f}_s \quad (4.17) \]

Similarly, the DC and small-signal AC variations of \( i_2 = h_2(\langle v_1 \rangle, \langle v_2 \rangle, f_s) \) can be derived as:

\[ I_2 = h_2(V_1, V_2, F_s) = \frac{1}{8L_bF_s} \frac{V_1^2}{V_2-V_1} \quad (4.18) \]

\[ \hat{i}_2 = \frac{-1}{r_2} \hat{v}_2 + g_2 \hat{v}_1 + j_2 \hat{f}_s \quad (4.19) \]

where

\[ \frac{1}{r_2} = \frac{1}{8L_bF_s (V_2-V_1)^2} \]

\[ g_2 = \frac{-1}{8L_bF_s (V_2-V_1)^2} \]

\[ j_2 = \frac{-1}{8L_bF_s V_2-V_1} \]

The small-signal averaged switch model representing (4.17) and (4.19) can be estimated by writing the state-space of the dc-bus capacitors as follows:

\[ C_1 || C_2 \frac{d\langle v_{dc} \rangle}{dt} = j_2 \hat{f}_s - \frac{1}{r_2} \hat{v}_{dc} - \hat{i}_{dc} \quad (4.20) \]

The output capacitance state-space equation is written as:

\[ C_o \frac{d\langle v_o \rangle}{dt} = \langle i_{rec} \rangle - \frac{\langle v_o \rangle}{R} \quad (4.21) \]

By using voltage-second balance principle in \( L_s \), the magnitudes of the maximum current
(\(i_{p,max}\)) and minimum current (\(i_{p,min}\)) of the transformer primary current are derived as:

\[
i_{p,max} = |i_{p,min}| = \frac{1}{8L_s\langle v_{dc}\rangle f_s(t)} \left( \langle v_{dc}\rangle^2 - 4n^2\langle v_o\rangle^2 \right)
\]

(4.22)

and

\[
\langle i_{rec} \rangle = \frac{1}{2}i_{p,max}
\]

(4.23)

By using (4.21)-(4.23), \(\hat{v}_o(s)\) can be derived as:

\[
\hat{v}_o(s) = \frac{\alpha}{C_o s - \beta} \hat{v}_{dc}(s) - \frac{\zeta}{C_o s - \beta} \hat{f}_s(s)
\]

(4.24)

where

\[
\alpha = \frac{1}{16L_s f_s} + \frac{n^2V_o^2}{2L_s f_s V_{dc}^2}
\]

\[
\beta = -\frac{n^2V_o}{2L_s f_s V_{dc}}
\]

\[
\zeta = -\frac{1}{16L_s f_s V_{dc}^2} (V_{dc}^2 - 4n^2V_o^2)
\]

The control-to-output transfer function \(G_{v_o,f_s}(s)\) can be calculated by using (4.19)-(4.24) and letting \(\hat{v}_g = 0\) as follows:

\[
G_{v_o,f_s}(s) = \frac{\hat{v}_o(s)}{\hat{f}_s(s)} = \frac{\zeta (C_1||C_2)s + \zeta m + \alpha j_2}{(C_1||C_2)C_o s^2 + (mC_o - \beta (C_1||C_2))s - m\beta + \frac{2\alpha V_o}{RV_{dc}}}
\]

(4.25)

where

\[
m = \frac{1}{r_2} - \frac{V_o^2}{RV_{dc}^2}
\]

(4.26)

Equation (4.25) represents a minimum-phase system since all its poles and zeros are in the left
half of the s-plane. Thus, the design of the control system is not complex and can be achieved by simple digital/analog circuitry.

### 4.5 Qualitative Performance

In this section, the input power factor and output regulation will be analyzed.

#### 4.5.1 Input Power Quality

Power factor quantifies the net energy that is transmitted from the grid to the load, which depends on $k_d$ and $k_\theta$. To find $k_d$, the RMS and fundamental components of $i_g$ are needed.

The peak boost inductor current $i_{b\text{peak}}(t)$ can be calculated from:

$$i_{b\text{peak}}(t) = \frac{1}{2L_b f_s} v_g(t) \quad (4.27)$$

And the average current in each switching cycle can be calculated as:

$$\langle i_b \rangle_{T_s}(t) = \frac{V_{dc}}{4L_b f_s} \frac{v_g(t)}{V_{dc} - v_g(t)} \quad (4.28)$$

When $V_{dc}$ is much larger than the amplitude of the grid voltage ($V_g$), (4.28) can be simplified to:

$$\langle i_b \rangle_{T_s}(t) = \frac{1}{4L_b f_s} v_g(t) \quad (4.29)$$

In this scenario, $\langle i_b \rangle_{T_s}(t)$ is a pure sinusoidal waveform. Thus, the power factor will be at near unity. That is, $PF = k_d = 1$. Since the high-frequency (kHz range) ripple in $i_b$ can easily be filtered out using differential Electromagnetic Interference (EMI) filters, the general form of $PF$ can be
Figure 4.8: Graphs for power factor and THD versus $\lambda = \frac{V_g}{V_{DC}}$.

Estimated as:

$$\text{PF} = k_d = \frac{\langle i_{b1}\rangle_{T_s}^{\text{RMS}}}{\langle i_b \rangle_{T_s}^{\text{RMS}}}$$  \hspace{1cm} (4.30)$$

where $\langle i_{b1}\rangle_{T_s}^{\text{RMS}}$ is the RMS value of the fundamental component of (4.28) and $\langle i_b \rangle_{T_s}^{\text{RMS}}$ is the RMS value of (4.28). $\langle i_{b1}\rangle_{T_s}^{\text{RMS}}(t)$ can be calculated as:

$$\langle i_{b1}\rangle_{T_s}^{\text{RMS}} = \frac{\sqrt{2} \left( \pi \left( \frac{1}{\sqrt{1-\lambda^2}} - 1 \right) + \frac{2\sin^{-1}(\lambda)}{\sqrt{1-\lambda^2}} - 2\lambda \right)}{\pi \lambda^2}$$  \hspace{1cm} (4.31)$$
where \( \lambda = \frac{V_g}{V_{dc}} \). \( \langle i_b \rangle_{T_s}^{RMS} \) is derived as:

\[
\langle i_b \rangle_{T_s}^{RMS} = \frac{1}{\sqrt{\pi \lambda (1 - \lambda^2)^{3/4}}} \times \left( 2 \sqrt{1 - \lambda^2} \lambda + \pi \left( - \left( \sqrt{1 - \lambda^2 - 2} \lambda^2 + \sqrt{1 - \lambda^2 - 1} \right) + (4 \lambda^2 - 2) \sin^{-1}(\lambda) \right) \right)^{-1/2}
\] (4.32)

Figure 4.8(a) is drawn based on (4.30), (4.31), and (4.32). As \( V_{dc} \) decreases and gets closer to \( V_g \), power factor slightly decreases. According to Figure 4.8(a) near unity \( PF \) can be achieved for all operating conditions.

Total harmonic distortion (THD) of the current can be calculated from:

\[
THD = \sqrt{\frac{1}{L_d^2} - 1} = \sqrt{1 - \frac{1}{PF^2}} - 1
\] (4.33)

Figure 4.8(b) depicts the graph for \( THD \) versus \( \lambda \). When \( \lambda \) is near zero, \( THD = 0 \). As \( \lambda \) increases, THD increases slightly.

### 4.5.2 Output Regulation

In this subsection, the output current ripple of the converter is investigated. The difference between the instantaneous input and output power causes output current ripple at twice the line frequency (100 Hz or 120 Hz). The double-line frequency ripple initially appears on the DC-link voltage (\( \Delta V_{dc} \)), which is then reflected in the output. The double-line frequency current ripple (\( \Delta I_o \)) is calculated as:

\[
\Delta I_o = \frac{2 f_s L_s \Delta V_{dc}}{n^3 R_o^2} \left( -1 + \sqrt{1 + \frac{n^4 R_o^2}{16 f_s^2 L_s^2}} \right)
\] (4.34)

Adopting energy storage capacitors at the DC-link compensates for the instantaneous power difference between the input and output powers, which consequently reduces the double-line frequency output current ripple.
Figure 4.9: Drain to source current waveforms of $S_1$ and $S_2$ at switching instants, which shows ZVS for all the switches.

4.6 Simulation and Experimental Results

Simulation and experimental results for the proposed system are given in this section. The current passing through $S_1$ ($i_{S1}$) and $S_2$ ($i_{S2}$) for positive and negative main periods are depicted in Figure 4.9 at $I_o = 5.2$ A. According to this figure, when $S_1$ turns on, $i_{S1}$ is negative; similarly, when $S_2$ turns on, $i_{S2}$ is negative. Due to this negative current, the output capacitance of the switch that is turning on is discharged during deadtime. Thus, the voltage of the switch reaches zero before the turn-on instant, and ZVS is provided.

Figure 4.10 shows the experimental prototype for the proposed system. Table 4.1 provides the
Table 4.1: Specifications and parameters of the single-stage AC/DC converter.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_o )</td>
<td>Output Power</td>
<td>90-250 W</td>
</tr>
<tr>
<td>( v_g )</td>
<td>Input Voltage</td>
<td>90-130 ( V_{RMS} )</td>
</tr>
<tr>
<td>( V_o )</td>
<td>Nominal Output Voltage</td>
<td>48 ( V_{DC} )</td>
</tr>
<tr>
<td>( f_s )</td>
<td>Switching Frequency</td>
<td>50-250 kHz</td>
</tr>
<tr>
<td>( L_s )</td>
<td>Series Inductance</td>
<td>29 ( \mu H )</td>
</tr>
<tr>
<td>( L_b )</td>
<td>Input Boost Inductor</td>
<td>80 ( \mu H )</td>
</tr>
<tr>
<td>( n )</td>
<td>Transformer Turns-Ratio</td>
<td>20:8:8</td>
</tr>
<tr>
<td>( C_o )</td>
<td>Output Capacitor</td>
<td>10 ( \mu F )</td>
</tr>
<tr>
<td>( S_1 ) and ( S_2 )</td>
<td>MOSFETs</td>
<td>FCP11N60</td>
</tr>
<tr>
<td>( D_1 ) and ( D_2 )</td>
<td>Input diodes</td>
<td>MUR860G</td>
</tr>
</tbody>
</table>

parameters and the specifications of the prototype. The control system is implemented inside an Intel FPGA. \( I_o \) is measured using a shunt-resistor is utilized to measure \( I_o \). A 10-bit analog-digital converter (PN:ADS7884) is used to pass the measured value from \( I_o \) to the FPGA (PN:ADS7884). A digital linear compensation is used to create the switching period signal inside the FPGA. This signal is then passed to the modulator. The modulator uses the switching period signal to create a counter up limit (CUL) of a sawtooth signal; it will also create a constant signal of CUL/2 (for 50% duty cycle). The sawtooth signal is compared with the CUL/2 signal to generate the pulses for the switches.

The steady-state behavior of the DCM AC/DC converter in the positive half mains is shown in Figure 4.11. This figure shows that when \( v_{S1} = V_{dc} \), \( i_b \) rises and when \( v_{S1} = 0 \), \( i_b \) reduces. When
$i_p$ is positive, $D_2$ is conducting; hence, $v_{D2}$ is zero (theoretically). After the zero crossings of $i_b$, resonance occurs between the boost inductor and the junction capacitances of the input diodes. This resonance causes oscillation in $v_{D2}$ and $i_b$ waveforms. The waveforms $v_{D2}$, $i_b$, and $v_{S2}$ for the steady-state operation of the DCM boost PFC in negative half mains is shown in Figure 4.12. The steady-state behavior of the isolated nonresonant DC/DC converter is shown in Figure 4.13. The behavior of the isolated nonresonant DC/DC converter does not depend on the half mains periods and is the same in both of them. When $v_{S1} = 0$ rises and when $v_{S1} = V_{dc}$, $i_p$ reduces ($L_m$ is designed large; thus $i_s \approx i_p$). Since the output diodes have zero current switchings, the polarity of $i_p$ determines the polarity of $v_{S2}$. When $i_p > 0$, $D_{o1}$ conducts and $v_{s2} = V_o$; when $i_p < 0$, $D_{o2}$ conducts and $v_{s2} = -V_o$. Therefore, the slope and polarity of $i_p$ changes at the zero crossing of $i_p$. 

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Figure 4.13: Experimental results of $i_p$ and $v_{S1}$ when $V_o = 48$ V and $I_o = 5.2$ A.

Figure 4.14: Experimental results of $i_p$, $i_b$, and $v_{S1}$ for different operating modes.

The steady-state behavior of $i_b$, $i_p$, and $v_{S1}$ for negative half mains are shown in Figure 4.14. This figure shows that in mode 1, $v_{S1} = V_{dc}$, which results in the decrease of $i_p$ and $i_b$. Mode 2 shows that after the zero crossing of $i_p$, the slope of $i_p$ changes. In mode 3, the converter begins deadtime as $S_2$ switches off. During the deadtime, the output capacitance of $S_1$ discharges and $v_{S1}$ reaches zero; hence, ZVS is provided when $S_1$ switches on. In mode 4, $v_{S1} = 0$, which causes $i_p$ and $i_b$ to rise. In mode 5, $i_p$ is positive and the trend of $i_p$ changes. In mode 6, $i_b$ becomes zero; after the zero crossing resonance between $L_b$ and the junction capacitances of $D_1$ and $D_2$ occurs. In mode 7, $V_{S1} = 0$ and deadtime begins. During deadtime, the output capacitance of $S_2$ discharges and its voltage reaches zero. Thus, ZVS is provided at the turn-on instant of $S_2$.

The steady-state behavior of the grid current ($i_g$), $v_g$, output current ($I_o$), and output voltage ($V_o$)
are shown in Figure 4.15. The harmonic contents of $i_g$ and the maximum permissible harmonic current (in mA) based on JIS C-61000-3-2 and IEC 61000-3-2 for output power at 250 W are depicted in Fig. 4.16. This figure shows that the harmonic components of the $i_g$ are bellow the permissible limits. depicts The efficiency of the converter is shown in Fig. 4.17 from 250 W to 90 W. According to this figure, high efficiency is achieved for the proposed system.

The measured DC-link voltage for various powers is shown in Figure 4.18. This figure shows that the DC-link voltage is steady over the complete range of power. Thus, the converter’s operating power does not vary the voltage stress across switches, the diodes, and the input capacitors. This allows a reliable operation for the converter over wide power levels.
The proposed system comprising the totem-pole isolated, non-resonant AC/DC converter with variable frequency control has omitted half-bridge capacitors’ energy imbalance problem and the associated losses. The half-bridge capacitors’ imbalance problem happens when totem-pole isolated, nonresonant AC/DC converters (with phase-shift full-bridge) implement PWM \((D \neq 0.5)\) control system. Due to this imbalance, current spikes occurs in the transformer windings At zero-crossings of \(v_g\) as shown in Figure 4.19. These current spikes generate losses for the switches and the high-frequency transformer. They also affect the longevity of the output diodes and the switches. Another adverse effect of the current spike issue is that large capacitors are required at the output terminal. These capacitors filter out these spikes to provide a smooth output current for the load. The behavior of the proposed system when the converter uses the variable frequency control scheme is shown in Figure 4.20. This figure shows that \(i_p\) has fixed the capacitor’s energy imbalance issue and has provided a stable operation for the transformer current. Thus, the switching frequency contents of \(i_{rec}\) are only filtered by the output capacitor \((C_o)\). In this prototype, \(C_o = 10\mu F\) is used. To construct \(C_o = 10\mu F\), three 3.3 \(\mu F\) capacitors (PN: B32562J1335K189) are utilized in parallel to the output port.
Figure 4.18: Measured DC-link voltage.

Figure 4.19: Steady-state waveforms of grid voltage and the transformer primary current when PWM control is used for totem-pole, isolated, non-resonant single-stage AC/DC converter. Current surge occurs at zero crossing of the grid voltage.

Figure 4.20: Steady-state waveforms of grid voltage and the transformer primary current of the proposed control for the totem-pole isolated, non-resonant single-stage AC/DC converter.
4.7 Summary

This chapter proposed a system consisting of a totem-pole isolated, non-resonant AC/DC converter with a variable frequency control system. The proposed system enhances the converter’s reliability by allowing a constant DC-link voltage that is not dependent on the operating power. Small output capacitors are required to regulate the output current tightly while achieving high power factor. At the turn-on instants of the MOSFETS, soft-switching is achieved. A new steady-state equivalent circuit was given to explain the behavior of the converter and provide precise expressions for the input and output powers.
Control Systems for Totem-Pole Isolated AC/DC Converters

5.1 Introduction

A variable duty-cycle control (VDC) system is proposed for the totem-pole isolated single-stage AC/DC converters in this chapter. The proposed VDC’s control variable is the duty cycle; hence, the duty cycle regulates the operating power of the converter. The duty cycle shows a quasi-square-waveform with a fundamental frequency of the mains frequency (50Hz or 60Hz). A new time-domain expression is given for the totem-pole single-stage AC/DC converter when the proposed VDC scheme is used. The proposed VDC enables the addition of control freedom, which can be utilized to improve the power efficiency at low power.

This chapter is organized as follows. In section 5.2, the conventional PFM control for totem-pole single-stage AC/DC converters is given. In section 5.3, the proposed VDC is presented. In section 5.4, the time-domain expression is provided. In section 5.5, experimental results are provided to verify the performance of the proposed control system.
Figure 5.1: Schematic and block diagram of Totem-pole isolated AC/DC converter when PFM is used.

5.2 Totem-Pole Isolated AC/DC Converter

The diagram of a totem-pole isolated single-stage AC/DC converter when operating under conventional PFM control system is shown in Figure 5.1. This figure shows that a totem-pole nonisolated AC/DC converter is combined with a half-bridge isolated DC/DC converter. This is achieved by sharing the capacitors ($C_1$ and $C_2$), and the two switches ($S_1$ and $S_2$). The input AC voltage ($v_g$) is converted to a DC-link voltage ($V_{dc}$) by using the totem-pole nonisolated AC/DC converter, which comprises the two switches, boost inductor ($L_b$), and two diodes ($D_1$ and $D_2$). The DC-link is used as the input for the half-bridge isolated DC/DC converter to provide a suitable output condition for loads such as LEDs or batteries. The half-bridge isolated DC/DC converter comprises two switches, a transformer, a series inductor ($L_p$), magnetizing inductance ($L_m$), two input capacitors ($C_1$ and $C_2$), and a center-tapped or diode bridge rectifier ($D_{o1}$ and $D_{o2}$), and the output capacitor ($C_o$). Since $S_1$ and $S_2$ are shared, the control system is responsible for performing both the AC/DC and DC/DC conversions. One of the common control methods is the PFM, which is shown in Figure 5.1. This figure shows that a current compensator controls the switching frequency ($f_s$), and the duty cycle ($D$) is constant $D = 0.5$. $f_s$ is given to a PFM block; the PFM block then changes the time period by altering the sawtooth ($swt$) width. The switching pulses for $S_1$ and $S_2$, the half cycle state ($HCS$) signal, and the $swt$ signal near the zero crossings of $v_g$ is shown in Figure 5.2. The polarity of $v_g$ is shown with $HCS$. That is, When $v_g \geq 0$, $HCS = 1$ and when $v_g < 0$, $HCS = 0$. 

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Figure 5.2: Illustration of switching pattern when using PFM.

Figure 5.2 shows that HCS does not affect \( swt \) and the switching pulses (i.e., HCS is \( swt \) and the switching pulses are not dependent on HCS). Thus, one of the PFM control’s main benefits is that it doesn’t need sensing at the input side \( v_g \). One of the main drawbacks of PFM is that efficiency is affected at low power. This is mainly because of the high switching frequency at light load since \( f_s \) is inversely related to the power flow.

### 5.3 Proposed Variable Duty Cycle Control (VDC)

The block diagram of the totem-pole isolated single-stage AC/DC converter with the proposed VDC is shown in Figure 5.3. In the proposed VDC, The duty cycle \( D \) is varied to control the output power, where \( D \) is defined as the interval of on-time for \( S_1 \) over the switching period. The converter’s main waveforms when utilizing the proposed VDC system are shown in Figure
Figure 5.3: Schematic and block diagram of the proposed VDC for the totem-pole isolated single-stage AC/DC converter.

5.4 during steady-state (The waveforms are shown using PSIM simulation). According to this figure, in the positive half cycle (PHC) (when $v_g$ is positive), $D$ is constant and equal to $D = D_p$; $D_p \geq 0.5$. In the negative half cycle (NHC) (when $v_g$ is positive), $D$ is constant and equal to $D = D_n$; $D_n \leq 0.5$. Therefore, $D$ shows a quasi-square-waveform with a fundamental frequency of the mains frequency (60 Hz or 50 Hz). The switch of $D$ between the $D_p$ and $D_n$ is necessary in order to prevent DC component in the grid current. To prevent this DC current, the summation of $D_p$ and $D_n$ has to equal to one ($D_p + D_n = 1$). According to Figure 5.4, $D$ changes its state near the zero crossings. This causes the transformer primary current $i_p$ to show symmetric waveform at this point (This can be seen in Figure 5.4). Due to the shape of $i_p$, in the NHC, $D_{o1}$ is mostly on and in the PHC, $D_{o2}$ mostly conducts (i.e., each output diode mostly conducts in one half mains period). The current in $D_{o2}$ ($i_{D_{o2}}$) in the NHC has similar behavior to the current in $D_{o1}$ ($i_{D_{o1}}$) in the PHC (section V provides experimental waveforms of $i_{D_{o1}}$ and $i_{D_{o2}}$). Therefore, output delivered power to the load is the same in PHC and NHC (i.e., the converter achieves symmetric power flow versus $D$ at $D = 0.5$).

Figure 5.3 shows that the current error is generated by subtracting the current reference ($I_{ref}$)
Figure 5.4: Simulation result illustrating the VDC operation, which illustrates the semi-square-waveform shape of the duty cycle and the symmetric shape of $i_p$ in positive and negative half cycles.

from the output current ($I_o$). A compensator (cmp) uses this error and outputs a signal, which is passed to a limiter (with a maximum limit of 0.5). The output of the limiter is the value of the $D$ in NHC ($D_n$). Therefore, the control system varies $D_n$ to control $I_o$. It is worth noting that with the given control structure in Fig. 5.3, $D_n$ cannot surpass 0.5; otherwise, instability could occur in the control system. A comparator is used to compare $D_n$ with $swt$, which creates a preliminary signal ($PS$). Two multiplexers (MUX) are used with inputs as $PS$ and the inverse of the $PS$ signal. These MUXes use $HCS$ as the control signal and create the switching pulses of $S_2$ and $S_1$. Therefore, these MUXes enable the switch in $D$ at the zero crossings. That is, if $HCS = 0$, inverse of $PS$ is passed to $S_2$, and $PS$ is given to $S_1$; when $HCS = 1$, inverse of $PS$ is passed to $S_1$, and $PS$ is given to $S_2$. In the proposed VDC system, a timing synchronization method is presented to define $HCS$, and a variable frequency modulation ($FM$) is given to make the $swt$ signal zero when $HCS$ switches between two states. To find $HCS$, initially, a ZCD signal is created using a zero-crossing detection (ZCD). The ZCD signal presents the polarity of $v_g$. However, when the ZCD signal is directly passed to $HCS$, a current surge occurs in $i_p$ due to unsynchronized timing and abrupt change in $D$. The experimental results in Figure 5.5(a) demonstrate a high current surge happening in $i_p$ when $HCS$ switches its state from $PHC$ to $NHC$ and vice versa. The time in which this surge
Current surge of $i_p$ is illustrated at turn over instants of HCS (NHC to PHC and vice versa).

(a) Current surge of $i_p$ is illustrated at turn over instants of HCS (NHC to PHC and vice versa).

(b) Smooth transition of $i_p$ from NHC to PHC and vice versa is illustrated.

Figure 5.5: Experimental results for $i_p$ with and without the proposed variable frequency synchronization method.

...happens may be a short interval (a couple of switching periods); this time is dependent on the saved energy in $C_1$ and $C_2$. However, this current surge can exceed twice the normal steady-state current of $i_p$. This can damage and affect the diodes, capacitors, and switches’ life expectancy; thereby, affecting the converter’s reliability. As a remedy to this issue, a D-flip-flop is utilized in order to synchronize the ZCD signal with the switching pulses. The synchronization is implemented by connecting the PS signal and the ZCD signal to the D-flip-flop clock and input, respectively; the output of the D-flip-flop is the HCS signal (which is shown in Figure 5.3). HCS is used to control the MUXes and to reset $swt$ in between the switching period. The instant of resetting the $swt$ signal by HCS is depicted in Figure 5.6. This figure shows that $swt$ resets to zero when HCS changes its state. Therefore, $swt$ resets in between the switching period, which causes the switching frequency to vary for one switching cycle. Figure 5.6(a) shows that at the falling instant of $S_2$ HCS changes its state from PHC to NHC. This instant coincides with the rising instant of the inverse of PS when $HCS = PHC$; Figure 5.6(b) shows that at the falling instant of $S_2$ HCS changes its state from NHC to PHC. This instant coincides with the rising instant of the inverse of PS when...
$HCS = NHC$. Thus, the inverse of the $PS$ signal can be used for the clock of the D-flip-flop. The experimental results in Figure 5.5(b) show a stable operation of $i_p$ by using the FM block and the timing synchronization method. According to this figure, $i_p$ has a smooth transition from $PHC$ to $NHC$ and vice versa.

### 5.4 Time-domain Expression

The time-domain expression for the proposed VDC system is provided in this section. Figure 5.7 shows the key waveforms of the steady-state operation for $PHC$ and $NHC$ when using the proposed VDC system. When $S_2$ is off ($S_1$ is on), the voltage of switch $S_2$ ($v_{s2}$) is equal to $v_{s2} = V_{dc}$ and when $S_2$ is on ($S_1$ is off), $v_{s2} = 0$. Figure 5.7 shows that when operating in $PHC$, $i_b$ rises linearly when $v_{s2} = 0$ and decreases linearly to zero when $v_{s2} = V_{dc}$; in $NHC$, when $V_{dc} = 0$, $i_b$ descends.
Figure 5.7: Key waveforms of VDC.

linearly and when \( v_{s2} = 0 \), \( i_b \) linearly rises till it reaches zero. The time-domain expression for \( i_b \) is given as:
\[
\begin{align*}
  i_b &= \frac{v_g}{L_{bf}} I_t & t < d_1 T_s \\
  i_b &= \frac{v_g - V_{dc} \text{sgn}(v_g)}{L_{bf}} - i b_1 u(t - d_3 T_s) & d_1 T_s < t < T_s
\end{align*}
\]

where \( d_3 = \frac{|v_g(t)|}{V_{dc} - |v_g|} d_n \), \( u \) is the unit step function and \( \text{sgn}(v_g) \) is the sign of \( v_g \), and \( i b_1 = \frac{v_g(t) d_1}{L_{bf}} \). \( P_n \) can be derived as

\[
p(t) = \frac{1}{T_g} \int_0^{T_g} v_g(t) \langle i_b \rangle_T_s(t) dt = \frac{D_n^2}{\pi L_{bf} f_s} \int_0^{\pi/2} \frac{V_g^2 \sin^2(t)}{1 - \frac{V_c \sin(t)}{V_{dc}}} dt
\]

where \( V_g \) is the amplitude of \( v_g \), and \( T_g \) is the mains period.

The state-space expressions of the half-bridge isolated DC/DC conversion can be derived from:

\[
\begin{align*}
  \frac{d i_p}{dt} &= \frac{1}{L_p} (v_{c2} - v_c - v_m) \\
  \frac{d v_c}{dt} &= \frac{1}{C_p} i_p(t) \\
  \frac{d i_m}{dt} &= \frac{1}{L_m} v_m
\end{align*}
\]

where \( C_p = \frac{C_1 C_2}{C_1 + C_2} \), and \( v_{c2} \) is the voltage across \( C_2 \).

\[
\begin{align*}
  v_c &= v_{c1} & \text{when } S_1 \text{ is on.} \\
  v_c &= v_{c2} & \text{when } S_2 \text{ is on.}
\end{align*}
\]

The time-domain expressions of the half-bridge isolated DC/DC conversion can be obtained for three modes:

**Interval 1:** \( 0 < t < d_1 T_s \):

From (5.2), the time-domain expression is calculated as:
\[
\begin{align*}
    i_p(t) &= i_p0 \cos(\omega_0 t) - \frac{\sin(\omega_0 t)(v_c0 - v_{s2} + v_m)}{z_0} \\
    v_c(t) &= i_p0 z_0 \sin(\omega_0 t) + \cos(\omega_0 t)(v_c0 - v_{s2} + v_m) + V_{dc} - v_m \\
    i_m(t) &= \frac{1}{L_m} v_m t + i_p0
\end{align*}
\]

where \(v_c0\) and \(i_p0\) and the initial points of \(v_c2\) and \(i_p\) of interval 1, respectively, and

\[
\omega_0 = \frac{1}{\sqrt{L_p C_p}}
\]

(5.4)

\[
z_0 = \sqrt{\frac{L_p}{C_p}}
\]

(5.5)

\[
C_p = \frac{C_1 C_2}{C_1 + C_2}
\]

(5.6)

The time-domain expressions are different in negative and positive half cycles. The time-domain expressions in \(PHC\) are calculated using (5.3) and

\[
\begin{align*}
    v_c &= v_c2 \\
    v_{s2} &= 0 \\
    v_m &= -V_o
\end{align*}
\]

In \(PHC\), the final value of the state-variables in interval (1) is derived from

\[
\begin{align*}
    i_p1 &= i_p0 \cos(d_1 T_s \omega_0) - \frac{\sin(d_1 T_s \omega_0)(v_c0 - V_o)}{z_0} \\
    v_c1 &= i_p0 z_0 \sin(d_1 T_s \omega_0) + \cos(\omega_0 d_1 T_s)(v_c0 - V_o) + V_o \\
    i_m1 &= -\frac{1}{L_m} V_o d_1 T_s + i_p0
\end{align*}
\]

(5.7)
where \( v_c1 = v_c2(d_1T_s) \), \( ip1 = i_p(d_1T_s) \), and \( im1 = i_m(d_1T_s) \).

The time-domain expressions in \( NHC \) is calculated by using (5.3) and

\[
\begin{align*}
\begin{cases}
    v_c &= v_{c1} \\
    v_s2 &= V_{dc} \\
    v_m &= V_o
\end{cases}
\end{align*}
\]

In \( NHC \), the values of the state-variables at the end of interval 1 are calculated from

\[
\begin{align*}
\begin{cases}
    ip1 &= ip0 \cos(\omega_0 d_1 T_s) - \frac{\sin(\omega_0 d_1 T_s)(vc0 - V_{dc} + V_o)}{z_0} \\
    vc1 &= ip0 z_0 \sin(\omega_0 d_1 T_s) + \\
         &\quad \cos(\omega_0 d_1 T_s)(vc0 - V_{dc} + V_o) + V_{dc} - V_o \\
    im1 &= \frac{1}{L_m} V_o d_1 T_s + ip0
\end{cases}
\end{align*}
\]

(5.8)

**Interval 2:** \( d_1T_s < t < d_2T_s \):

From (5.2), time-domain expressions when \( d_1T_s < t < d_2T_s \) is calculated from:

\[
\begin{align*}
\begin{cases}
    i_p(t) &= ip1 \cos(\omega_0 (t - d_1 T_s)) - \\
         &\quad \frac{\sin(\omega_0 (t - d_1 T_s))(V_{dc} - vc1 - v_s2 + v_m)}{z_0} \\
    v_c(t) &= ip1 z_0 \sin(\omega_0 (t - d_1 T_s)) + \cos(\omega_0 (t - d_1 T_s)) \\
         &\quad \times (V_{dc} - vc1 - v_s2 + v_m) + v_s2 - v_m \\
    i_m(t) &= \frac{1}{L_m} v_m t + ip0
\end{cases}
\end{align*}
\]

(5.9)

The time-domain expressions in interval 2 vary between \( PHC \) and \( NHC \). The time-domain expressions in \( PHC \) is calculated by using (5.9) and
In PHC, the final state-variables of interval (2) are derived from

\[
\begin{align*}
\frac{v_c}{v_{c2}} &= v_{c1} \\
\frac{v_s}{v_{s2}} &= V_{dc} \\
\frac{v_m}{v_m} &= -V_o
\end{align*}
\]

The time-domain expressions in NHC is calculated by using (5.9) and

\[
\begin{align*}
ip_2 &= ip_1 \cos(\omega_0(d_2 - d)T_s) - \\
&\quad \frac{\sin(\omega_0(d_2 - d)T_s)(-vc1 - V_o)}{z_0} \\
v_{c2} &= ip_1z_0 \sin(\omega_0(d_2 - d)T_s) + \\
&\quad \cos(\omega_0(d_2 - d)T_s)(-vc1 - V_o) + V_{dc} + V_o \\
im_2 &= -\frac{1}{L_m}V_o d_2 T_s + ip_0
\end{align*}
\]

where \(im_2 = i_m(d_2 T_s)\), \(vc_2 = v_{c2}(d_2 T_s)\), and \(ip_2 = i_p(d_2 T_s)\).

The time-domain expressions in NHC is calculated by using (5.9) and

\[
\begin{align*}
\frac{v_c}{v_{c2}} &= v_{c2} \\
\frac{v_s}{v_{s2}} &= 0 \\
\frac{v_m}{v_m} &= V_o
\end{align*}
\]

In NHC, the values of the state-variables at the end of interval 2 are derived from
\[
\begin{align*}
\frac{ip_2}{ip_1} = & \cos(\omega_0(d_2 - d)T_s) - \\
& \sin(\omega_0(d_2 - d)T_s)(V_{dc} - vc_1 + V_o) \\
& z_0
\end{align*}
\]

\[
vc_2 = ip_1z_0 \sin(\omega_0(d_2 - d)T_s) + \\
\cos(\omega_0(d_2 - d)T_s)(V_{dc} - vc_1 + V_o) - V_o
\]

\[
im_2 = \frac{1}{L_m} V_o d_2 T_s + ip_0
\]

**Interval 3: \(d_2 T_s < t < T_s\):**

From (5.2), the time-domain expressions when \(d_2 T_s < t < T_s\) are calculated as:

\[
\begin{align*}
\frac{i_p(t)}{ip_2} = & \cos(\omega_1(t - d_2 T_s)) - \\
& (v_{s2} - vc_2) \sin(\omega_1(t - d_2 T_s)) \\
& z_1
\end{align*}
\]

\[
vc(t) = v_{s2} + ip_2 z_1 \sin(\omega_1(t - d_2 T_s)) + \\
(vc_2 - v_{s2}) \cos(\omega_1(t - d_2 T_s))
\]

\[
im(t) = i_p(t)
\]

where

\[
\omega_1 = \frac{1}{\sqrt{(L_p + L_m)C_p}}
\]

\[
z_1 = \sqrt{\frac{L_p + L_m}{C_p}}
\]
The time-domain expressions in this interval vary between PHC and NHC. The time-domain expressions in PHC is calculated by using

\[
\begin{align*}
v_c &= v_{c1} \\
v_{s2} &= V_{dc}
\end{align*}
\]

and (5.12). In PHC, the final values of the state-variables in interval (3) are derived from

\[
\begin{align*}
\begin{align*}
    ip^3 &= ip_2 \cos(\omega_1((1 - d_2)T_s)) - \\
    &\quad \left(\frac{V_{dc} - v_{c2}}{z_1}\right) \sin(\omega_1((1 - d_2)T_s)) \\
    vc^3 &= V_{dc} + ip_2z_1 \sin(\omega_1(1 - d_2)T_s) + \\
    &\quad (vc2 - V_{dc}) \cos(\omega_1((1 - d_2)T_s)) \nonumber
\end{align*}
\end{align*}
\]

(5.15)

where \( vc2 = v_{c2}(T_s) \), and \( ip^3 = i_p(T_s) \).

The time-domain expressions in NHC is calculated by using

\[
\begin{align*}
v_c &= v_{c2} \\
v_{s2} &= 0
\end{align*}
\]

and (5.12). In NHC, the values of the state-variables at the end of interval 3 are derived from

\[
\begin{align*}
\begin{align*}
    ip^3 &= ip_2 \cos(\omega_1((1 - d_2)T_s)) + \frac{vc2 \sin(\omega_1((1 - d_2)T_s))}{z_1} \\
    vc^3 &= ip_2z_1 \sin(\omega_1(1 - d_2)T_s) + vc2 \cos(\omega_1((1 - d_2)T_s)) \nonumber
\end{align*}
\end{align*}
\]

(5.16)

where \( vc3 = v_{c2}(T_s) \), and \( ip^3 = i_p(T_s) \).

At steady-state, the final and beginning values of \( i_p(t) \) and \( v_{c2}(t) \) of the switching period are equal to each other. thus,
\[
\begin{align*}
ip3 &= ip0 \\
vc3 &= vc0
\end{align*}
\] (5.17)

In NHC, \(ip0\) and \(vc0\) can be calculated by using (5.17), (5.16), (5.11), and (5.8); in the PHC, \(ip0\) and \(vc0\) are found by using (5.17), (5.15), (5.10), and (5.7).

5.5 Experimental Results

The behavior of the proposed control system is tested and validated using experimental results in this section. Table 5.1 provides the parameters and specification of the prototype.

The behavior of the converter when using PFM control scheme is shown in Figure 5.8. According to this figure, \(D\) is constant and equal to \(D = 0.5\) for the complete mains cycle. \(i_b\) and \(i_p\), and \(v_{s2}\) are depicted for PHC in Figure 5.8(a). This figure shows that when \(v_{s2} = V_{dc}\) (switch \(S_2\) is off), \(i_b\) reduces, and when \(v_{s2} = 0\), \(i_b\) rises with a constant slope. After \(i_b\) crosses zero, oscillation will occur, which is due to the resonance between \(L_b\) and the diodes’ junction capacitance \((D_1, D_2)\). \(i_p\) has a resonant operation, which is because \(C_1\) and \(C_2\) are chosen to demonstrate resonance in the half-bridge DC/DC conversion. External electrolytic capacitors are used at the DC-link voltage for energy storage purposes. \(i_p\), \(v_{s2}\), and \(i_b\) are shown for NHC in Figure 5.8(b). The operation of \(i_p\) in NHC and PHC are the same; however, the operation of \(i_b\) have some dissimilarities in NHC and PHC.

Table 5.1: Converter specifications and parameters.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(v_g)</td>
<td>Input Grid Voltage</td>
<td>110 (V_{RMS})</td>
</tr>
<tr>
<td>(V_o)</td>
<td>Nominal Output Voltage</td>
<td>48 (V_{DC})</td>
</tr>
<tr>
<td>(f_{sw})</td>
<td>Switching Frequency</td>
<td>90-200 kHz</td>
</tr>
<tr>
<td>(L_p)</td>
<td>Series Inductance</td>
<td>170 (\mu H)</td>
</tr>
<tr>
<td>(L_b)</td>
<td>Input Boost Inductor</td>
<td>75 (\mu H)</td>
</tr>
<tr>
<td>(n)</td>
<td>Transformer Turns-Ratio</td>
<td>4.57</td>
</tr>
<tr>
<td>(C_o)</td>
<td>Output Capacitor</td>
<td>30 (\mu F)</td>
</tr>
<tr>
<td>(C_1)</td>
<td>Resonant Capacitors</td>
<td>8.2 (nF)</td>
</tr>
<tr>
<td>(D_{o1}) and (D_{o2})</td>
<td>Output Schottky Diode</td>
<td>MBR20200CTG</td>
</tr>
</tbody>
</table>
Figure 5.8: Experimental results for $i_p$ and $i_b$ with respect to $v_{s2}$ when operating with PFM in (a) PHC and (b) NHC.

Figure 5.9: Experimental results for $i_{D01}$ and $i_{D02}$ with respect to $v_{s2}$ in PFM.

Figure 5.10: Experimental results for $i_{D01}$ and $i_{D02}$ with respect to HCS when operating in VDC.

**PHC.** In NHC, when $v_{s2} = V_{dc}$ ($S_1$ is on), $i_b$ reduces linearly to reach zero; when $v_{s2} = V_{dc}$ ($S_2$ is on), $i_b$ rises linearly.

The current passing in $D_{o2}$ ($i_{D_{o2}}$), the current passing in $D_{o1}$ ($i_{D_{o1}}$), and $v_{s2}$ in PFM is shown
Figure 5.11: Experimental results for $i_{D_{o1}}$ and $i_{D_{o2}}$ with respect to $v_{s2}$ when operating with VDC in (a) PHC and (b) NHC.

in Figure 5.9. This figure shows that when $v_{s2} = V_{dc}$, $D_{o1}$ operates $v_{s2} = 0, D_{o2}$ operates. The operation of $i_{D_{o1}}$ and $i_{D_{o2}}$ are not different in PHC and NHC. Thus, in both the half cycles, when PFM is used, $D_1$ and $D_2$ participate evenly to transfer energy to the output. This is not correct for the proposed VDC. The operation of $i_{D_{o2}}$ and $i_{D_{o1}}$ and HCS under the proposed VDC is shown in Figure 5.10. The enlarged graphs of Figure 5.10 for PHC and NHC are shown in Figure 5.11(a) and Figure 5.11(b), respectively. These figures show that in NHC, $i_{D_{o1}}$ has much high value than $i_{D_{o2}}$; hence, $D_{o1}$ has much greater contribution in delivering the power in NHC. In PHC, $i_{D_{o2}}$ has much high value than $i_{D_{o1}}$; hence, $D_{o2}$ is dominant in delivering the power in PHC.

In Figure 5.12, the key waveforms of the converter while using the proposed VDC is shown. In this operating condition, $D$ alters between $D_n = 0.45$ and $D_p = 0.55$ in PHC and NHC, respectively. Figure 5.12(a) shows $i_p, i_b,$ and $v_{s2}$ for PHC. According to this figure, when $v_{s2} = V_{dc}$ (switch $S_2$ is off), $i_b$ increases and it decreases when $v_{s2} = 0$ (switch $S_2$ is on) until it reaches zero. $i_p, v_{s2},$ and $i_b$ for NHC are shown in Figure 5.12(b). This figure shows that when $v_{s2} = 0$ (switch $S_2$ is on) $i_b$ decreases to zero and when $v_{s2} = V_{dc}$ (switch $S_1$ is on), $i_b$ rises.
Figure 5.12: Experimental results for $i_p$ and $i_b$ with respect to $v_{s2}$ when operating with VDC in (a) PHC and (b) NHC.

Figure 5.13: Experimental results of VDM operation for $i_b$ with respect to (a) $v_{D2}$ in PHC and (b) $v_{D1}$ in NHC.

In Figure 5.13, $i_b$ and the voltages of the input diodes are shown for PHC and NHC. $i_b$ and the voltage of $D_2$ ($v_{D2}$) are depicted in Figure 5.13(a). This figure shows that when $D_2$ is operating in
forward biased, $v_{D2} = 0$ and $i_b$ is positive. When $i_b$ crosses zero, it can enter an oscillation mode or linear mode. In oscillation mode, the resonance between the input diodes’ junction capacitance and $L_b$ cause resonance in $v_{D2}$ and $i_b$. In linear mode, $v_{D2}$ is fixed at $v_{D2} = V_{dc}$; hence, $D_1$ conducts in this mode and thus, in this prototype, the frequency is constrained to 200 kHz, and the proposed VDC is used to regulate the output at low power. $i_b$ rises with a constant slope. The operation of input diodes in $NHC$ and $PHC$ are similar.

The proposed VDC system offers additional control freedom for the control system. This can be used to enhance power efficiency at light load. The graph for efficiency of the converter is shown in Figure 5.14. It can be seen that high power efficiency is achieved when using PFM (in this prototype, high power refers to $P<115 \, W<250 \, W$). In PFM, high switching frequencies are expected at low power due to the inverse relationship between the switching frequency and the operating power. This causes high losses in the switches and the magnetic components. In Figure 5.14, the dotted curve demonstrates the speedy drop in power efficiency when $f_s$ goes over 200 kHz. Therefore, for low power operations ($50 \, W < P < 150 \, W$), the proposed VDC is used, in which the switching frequency remains at 200 kHz. The green line in Figure 5.14 represents the power efficiencies at low power when the proposed VDC is used. This figure shows a notable increase in power efficiency when using the proposed VDC for power levels lower than 115 W when compared to the PFM control system.
5.6 Summary

This chapter proposed a variable duty cycle control (VDC) system for totem-pole isolated AC/DC converters. The duty cycle is the main control variable that is used in the proposed VDC to regulate the output power. The steady-state operation of the duty cycle shows a quasi-square-waveform with a fundamental component frequency of grid frequency (60 Hz or 50 Hz). In each half mains period, mostly one of the output diodes contributes to delivering power to the load ($D_{o2}$ is dominant in PHC, and $D_{o1}$ is dominant NHC). New time-domain expressions were provided for the proposed VDC system. The proposed VDC allows an added control freedom, which can be used to enhance the converter’s efficiency. An experimental prototype was built to implement the proposed VDC system and validate its performance and increase power efficiencies at low powers.
6 | Conclusion and Future Work

6.1 Conclusion

In this thesis, the challenges of nonisolated multi-port DC/DC converters and isolated integrated AC/DC converters used in hybrid micro-grids were identified. New topologies and control systems were presented to overcome these challenges. Three-port DC/DC and single-stage AC/DC solutions derived from a dual inductor switch-node circuit were proposed. This structure enables high control flexibility over the currents in the switches. The main novelties and contributions of the thesis are given as follows:

1. A three-port DC/DC topology was proposed, which is capable of providing bidirectional power flow for two ports and a unidirectional power flow for one port. The proposed converter offers a low number of components and high reliability. It can be used to integrate solar panels and energy storage in a DC grid. It also can be used in applications that need to power two loads with boost output voltages from a single DC input source. An experimental prototype was built to show the operation of the converter for powers bellow 250 W.

2. A new control system was proposed for the three-port DC/DC converter, which controls the power flow between the ports by modifying the switching frequency and the duty cycle. The switching frequency controls the power flow in the DCM operation of the unidirectional port, and the duty cycle controls the current and power in the CCM operation of one of the bidirectional ports. Thus, the other bidirectional port’s power is determined by subtracting the power in the DCM from the CCM operation.
3. A mathematical model of the three-port DC/DC converter was presented that captures the steady-state and transient operation. The steady-state model was further used to design converter parameters. The mathematical modelling for the AC large-signal and small-signal models of the DCM operation was provided.

4. A new system comprised of a totem-pole isolated, nonresonant single-stage AC/DC converter with variable frequency control was proposed. The converter can achieve a stable DC-link voltage independent of power flow, which improves the reliability of the system. Moreover, it eliminates the capacitor imbalance issue when using pulse width modulation (PWM) control in totem-pole, isolated AC/DC converters. A minimal output capacitance is needed to tightly regulate the output current in low output voltage applications while achieving a high power factor. The proposed system shows high flexibility in controlling the current waveforms, which enables soft switching for all turn-on instants of the switches. An experimental prototype was built to the the operation of the proposed system for powers bellow 250 W.

5. A new equivalent circuit for totem-pole isolated, nonresonant single-stage AC/DC converters with variable frequency control was introduced. The proposed equivalent circuit allows a better understanding and precise steady-state analysis of the converter. In particular, a new and exact mathematical modelling of the steady-state power flow is derived for both AC/DC and DC/DC conversion stages using the new equivalent circuit. A new AC analysis involving new average modelling and small-signal modelling was proposed for DCM operation of totem-pole AC/DC converters. The large-signal AC model of the converter was derived by using the average switch model.

6. A new variable duty cycle control system was proposed for totem-pole isolated single-stage AC/DC converters. The proposed control system offers an additional control variable, which can be used to improve the performance of the converter. In particular, it can be used in hybrid conjunction with pulse frequency method to drastically improve power efficiencies at light load. Furthermore, a new time-domain analysis was presented for the VDC to capture
the behavior of the converter under the proposed control system. An experimental prototype was built to show the efficiency improvement at light load when using the proposed VDC.

6.2 Future Work

Possible future work of this research is outlined as follows:

- **Multi-port DC/DC converter**
  Controllable switches can have the potential to add more ports to the proposed three DC/DC converter. Thus, applications that require multiple PV panels and batteries can benefit from this multi-port structure.

- **High power operation for the proposed three-port DC/DC converter**
  The three-port DC/DC converter can be extended to operate in higher power levels. One method to approach this is to investigate the interleaved variation of the proposed three-port DC/DC converter.

- **Isolated three-port DC/DC converter**
  The three-port DC/DC converter can be extended to have single or multiple isolated ports by adding a transformer and rectifiers.

- **High power single-stage AC/DC converter**
  The proposed system for totem-pole single-stage isolated AC/DC converter operates in DCM to perform PFC. Thus, they are suitable for low power operations. The proposed system’s operation for the single-stage AC/DC converter can be extended to higher power levels by using two controllable switches instead of the two input diodes.

- **Bidirectional single-stage AC/DC converter**
  Optimized performance and bidirectional power flow of the proposed single-stage AC/DC solution can be achieved using two controllable switches instead of the input diodes and a synchronous rectifier at the output. This can be used in applications such as vehicle-to-grid (V2G) and grid-to-vehicle (G2V).
Bibliography


[15] “SA - JIS C 61000-3-2,” *Electromagnetic compatibility (EMC) - Part 3û2: Limits - Limits for harmonic current emissions (equipment input current Less than or equal to 20 A per phase)*.


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