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Fully Integrated GaN MMIC Power Amplifier Design for Sub-6 GHz 5G Applications

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Fully Integrated GaN MMIC Power Amplifier Design for Sub-6 GHz 5G Applications

by

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A THESIS

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Abstract

Power amplifiers (PAs) are the most power-hungry component of the transmit chain in a base transceiver system (BTS). Efficiency of the PA thus plays a significant role in the overall efficiency of the transmitter. Today's modern wireless communications networks need high data rates and low power consumption. Given that the bandwidth is limited, and frequency bands are expensive, therefore, spectral efficiency is of high importance. This is mainly achieved by varying the modulation techniques to accommodate higher data rates. Consequently, with the modern modulation techniques, there is a generation of high peak-to-average ratio power levels. This poses a challenge for the traditional PAs to have high efficiency not only at the peak power but also at back-off power levels.

Although there are several techniques to enhance the efficiency at back-off such as envelope tracking, pulse modulation, Doherty PA (DPA) etc., however, there are certain limitations associated with these architectures especially bandwidth restrictions and the complex designs. In this work, an unconventional design architecture for Radio Frequency (RF) PAs is implemented which is based on reverse load modulation technique. The Reverse Modulated Dual-Branch (RMDB) PA uses a constant current-biased transistor in the carrier branch to realize optimal load modulation without using the impedance transformer at the output of the PA, unlike in conventional Doherty. A proof-of-concept monolithic microwave integrated circuit (MMIC) PA is designed using 0.25um Gallium Nitride (GaN) high-electron-mobility transistor (HEMT) and process from United Monolithic Semiconductor (UMS) for sub-6 gigahertz (GHz) wireless applications, centered at 3.6 GHz.

This first ever fully integrated RMDB PA MMIC provides excellent gain flatness 10.5 dB (±0.5 dB) across 3.4 to 4.0 GHz bandwidth (BW) and delivers an output power of 39 decibel-milliwatt (dBm), (~ 8 watts), at saturation with drain efficiency of greater than 52% while maintaining greater than 38% at 10-dB back-off under continuous wave (CW) signal. This performance makes this design a promising candidate for future 5G and beyond applications.

Acknowledgments

I am deeply thankful to almighty for giving me strength and mercy to pursue a scientific research career in my life.

I take this opportunity to place on record my deep sense of gratitude to my supervisor, Prof. Mohamed Helaoui for his guidance, several encouragements and endless support he has provided throughout my research work. A special thank you to Prof. Fadhel Ghannouchi for his constructive technical insights and illuminating discussions throughout my grad studies.

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I would also like to extend my gratitude to my thesis oral examination committee members for their time and efforts to review my thesis.

A sincere gratitude to my family, my parents and my sister for their moral support and wisdom through this journey. And lastly, a big thank you to Dr. Tushar Sharma, who has always been a true friend, guide and supporter throughout.

Finally, I would like to thank Recon-RF inc. and Mitacs scholarship for providing me an opportunity to gain industrial exposure during my graduate studies and elevate my professional skills. A big thank you to the Faculty of Graduate Studies for providing scholarships and the entire University of Calgary professors, students and staff who have inspired me in ways beyond words can describe.

Dedication

Dedicated to my father, Akshay Tangri, my mother, Rekha Tangri

and my sister, Aastha Tangri

Table of Contents

List of Tables

List of Figures and Illustrations

List of Symbols, Abbreviations and Nomenclature

Symbol/Abbreviation	Definition
4G	Fourth Generation
5G	Fifth Generation
A	Ampere
mA	milli-Ampere
ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design Systems
AM-AM	Amplitude to amplitude modulation
AM-PM	Amplitude to phase modulation
APD	Analog Pre-Distortion
BTS	Base Transceiver Station
BW	Bandwidth
CW	Continuous Wave
dB	Decibel
dBm	Decibel-milliwatt
DC	Direct Current
DCIV	Direct-current current-voltage
DC-RF	Direct Current-Radio Frequency
DE	Drain Efficiency
DPA	Doherty Power Amplifier
DPD	Digital Pre-Distortion
DUT	Device Under Test
f0	Fundamental frequency
FET	Field Effect Transistor
FR	Frequency Range
G	Power gain of the power amplifier
GaAs	Gallium Arsenide
GaN	Gallium Nitride

GHz	Gigahertz
HEMT	High Electron Mobility Transistor
IDS	Drain-source current
IMD	Intermodulation
IP	Intercept point
LDMOS	Laterally diffused metal oxide semiconductor
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
OPBO	Output Power Back-off
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
Pin	Input power of the power amplifier
PIPO	Input vs Output Power
PM	Power Meter
Pout	Output power of the power amplifier
Psat	Saturated Power of the power amplifier
RF	Radio Frequency
RMDB	Reverse Modulated Dual-Branch
RX	Receiver
SA	Signal Analyzer
SG	Signal Generator
SiC	Silicon Carbide
θ	Conduction Angle
TX	Transmitter
UMS	United Monolithic Semiconductor
V	Volt
VDS	Drain-source voltage
VNA	Vector Network Analyzer
W	Watt

Z	Impedance
ηdrain	Drain Efficiency
Ω	Ohm

Chapter 1. INTRODUCTION

1.1 Background

Power amplifier (PA) is a component in the wireless communication system that amplifies weak signals to the required power levels for effective transmission through the antenna. PAs are the most power-hungry component of the transmit chain in a base transceiver station (BTS). Being an integral part of the transmit chain, the efficiency and power consumption of the PA dictates the overall power budget of the transmitter. Interestingly, more than half of the direct-current (DC) power of the entire system is consumed by the PA itself as shown in Fig. 1.1. This implies that if the PA is not efficient enough, it will create a lot of heat problems in the system. Looking from a commercial angle, the most expensive part of a BTS is not the high frequency components or equipment, in fact it is the electricity bought to run air conditioners and coolers for the base station to get rid of the heat dissipation.

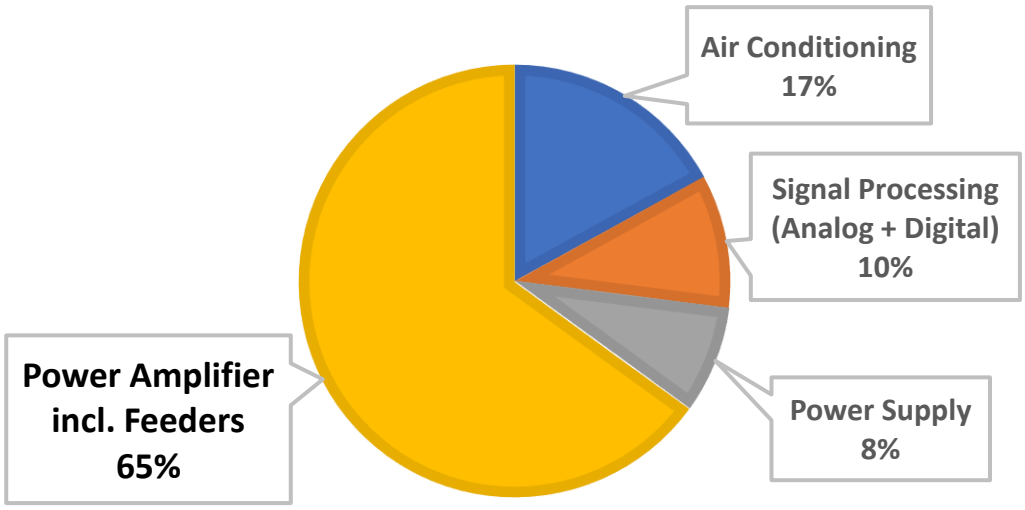


Figure 1.1. Power Consumption in Radio Base Stations [17]

In the modern wireless technology, 5G is implemented in two distinct frequency ranges, sub-6GHz region FR-1 and mm-wave region FR-2. Although the future technology will be driven by fast mm-wave amplification, however, sub-6GHz spectrum will facilitate an easy transition from 4G/LTE to 5G. While there is immense research going on that targets the deployment issues in mm-wave wireless components, there arises a necessity for continued research progress in sub-6GHz domain. The sub-6 GHz 5G deployment extensively employs high peak-to-average power ratio (PAPR) waveforms and poses demanding PA requirements, including linearity, peak efficiency, output power back-off (OPBO) efficiency, and capability of supporting multi-Gb/s modulation, explained below.

In today's wireless communication networks, spectral efficiency is of high importance. Given that the bandwidth is limited, and frequency bands are expensive, full utilization of the available frequency becomes even more critical. This is mainly achieved by varying the modulation techniques to accommodate higher data rates. Consequently, with the modern modulation techniques, there is a generation of high peak-to-average ratio power levels. This poses a challenge for the traditional PAs as they are designed to have high efficiency at peak power such that the efficiency curve peaks at 1-dB compression point and drops drastically at back off.

There are several techniques to enhance the efficiency of a PA at back-off namely RF-pulse modulation [1][34], envelope tracking [2][32-33] and dynamic load modulation [3][5][6][19-27]. Doherty PAs, introduced in mid-1930s, use dynamic load modulation by implementing an impedance inverter to achieve high efficiency at back-off power levels. In this architecture, there is no need of any external circuitry to control efficiency. Numerous DPA designs have been presented in the literature [5][6]. Various new studies that show nuanced load modulation networks can be found in [19-27]. Hence, Doherty PAs are attractive design choices from a research perspective, although there are some performance limitations associated with such architectures discussed further.

In this thesis, an unconventional design architecture for RF power amplifiers is implemented which is based on reverse load modulation technique. The Reverse modulated Dual-Branch (RMDB) PA uses a

current-biased transistor in the main branch to realize optimal load modulation without using the impedance transformer at the output of the PA [4] [7]. Consequently, this topology offers a proper load modulation mechanism over a wider frequency bandwidth since the need for bandwidth limiting transformer is eliminated. Besides, it uses a common output matching network (OMN) which allows lower loss and more compact design which is a highly suitable feature for monolithic microwave integrated circuit (MMIC) designs. The RMDB PA was first proposed by Akbarpour et al. [4] as an application of current-biased transistors. Compared to the conventional architecture, a more optimal/simplistic design approach is used using the proposed technique.

Additionally, MMICs have become more practical to use when it comes to high frequency applications. The two main advantages of using MMIC are, first, the design compactness because of reduced size of the circuit compared to PCB level designs and second, lesser parasitics in the design since there isn't any deice package and its associated parasitic effects which allows better model accuracy. This can result in a broader band design and better load modulation performance across frequencies which will be discussed in detail in later sections. On the other hand, sometimes it is hard to tune the performance of an MMIC post-fabrication which is usually not the case in board-level designs. Nevertheless, the advantages of MMIC makes it a promising design choice.

1.2 Thesis Motivation

The motivation behind this thesis is to design an MMIC PA that can work for the next generation wireless communications. As explained in the section 1.1, for 5G and beyond applications, we need Pas that have high BW as well as can work with high PAPR signals produced by complex modern modulation schemes. Although the conventional Doherty PAs can provide reasonable PAPR, however, the main limitation of such architectures is poor performance across frequencies. This is mainly due to the impedance inverter used at the output of the main branch, which is essential for load modulation, but restricts BW of operation. Therefore, we are looking for a compact wideband PA design solution that can provide good load modulation but without the need of an impedance inverter resulting in a wideband PA with high OPBO.

Also, we want to further reduce the design parasitics associated with the device packaging as much as possible. This thesis targets precisely these requirements through the design of an RMDB MMIC PA.

1.3 Thesis Contribution

As explained above, modern systems require higher back-off power levels of around 8-10dB, to accommodate the complex modulation schemes. In previous works relating RMDB PAs, the initial concept of an RMDB has been introduced, however, proof-of-concept is provided on a PCB level-design which is unsuitable for any compact wireless designs [4]. Extensive theoretical/experimental analysis of an RMDB PA MMIC has also been presented in [7], however, the work uses separate off-chip external circuit to inject RF inputs to each branch of the RMDB in order to control the OPBO and phase to achieve a broader band design. Hence [7] is a partially integrated design as does not include the input power splitter/matching networks in the final MMIC.

This work presents the design, simulation, and measurement of the first fully-integrated RMDB PA MMIC design which provides 10 dB OPBO across 600 MHz BW from 3.4 – 4.0 GHz. This thesis presents, for the first time, a fully integrated PA with input matching network (IMN) and tuned power splitter targeted to minimize the chip size of the RMDB PA that provides load-modulation across 600 MHz frequency bandwidth which is usually not the case with a conventional Doherty PA. This compact design was successfully executed with an overall chip size under 9 mm^2. Continuous wave (CW) measurements are used in this work. The theory and design methodology for an RMDB PA is well explained in the literature [4][7]. However, achieving this goal is not easy due to various trade-offs between size, gain, output power, linearity, efficiency etc, especially when implemented on a compact MMIC.

1.4 Thesis Outline

This thesis focuses on the study and design of high efficiency power amplifiers. This work presents the design, simulation, and measurement of a fully integrated Gallium Nitride (GaN) MMIC RMDB PA for sub-6GHz 5G application. Chapter 1 is an introduction to the work done in this thesis, the motivation behind it and its contribution. Chapter 2 presents the theory and concepts behind power amplifiers, their

operation, and an introduction to the Doherty and RMDB PA architecture. In Chapter 3, the study and design methodology of a high-power single-stage PA MMIC at 2.5 GHz for wireless applications is presented. The work presented in this chapter is done in collaboration with an industrial partner Recon-RF, Inc. *This work was supported by Mitacs through the Mitacs Accelerate progra*m. This chip was designed in Microwave office, AWR design environment software. In chapter 4, the design flow of a wideband MMIC RMDB PA centered at 3.6 GHz is discussed in detail. The circuit was designed using Keysight, Advanced Design System (ADS) software. The design flow entails bias-point selection, stability analysis, s-parameters, load pull and source pull and matching networks. The simulation results and performance predictions are presented in the end. In chapter 5, the layout of the topology sent out for fabrication and the experimental measurement results obtained post-fabrication are presented. Extensive measurements are performed including continuous wave (CW) measurements and are compared with the software simulations predictions. Then a comparison between the previous works and this works is discussed. Finally, the conclusion is given in Chapter 6, and possibilities of future work in continuation of this thesis is presented.

Chapter 2. THEORY OF POWER AMPLIFIERS

2.1 Power Amplifier Introduction

Power amplifier is usually the last active component of a wireless transmitter system that amplifies the RF signal to the required power level at the transmitting antenna. Designing a PA needs consideration of several performance parameters at the same time as shown in Fig. 2.1. The main challenge for a PA designer, however, is getting high efficiency, operational bandwidth and power gain while preserving the linearity. These design parameters have stringent requirements to meet certain wireless standards in most of the modern systems. As a result, there is a need of careful consideration of the trade-off between these parameters since the conditions to optimize these parameters are different and therefore it is not possible to optimize multiple parameters concurrently. These parameters are discussed in the following sections.

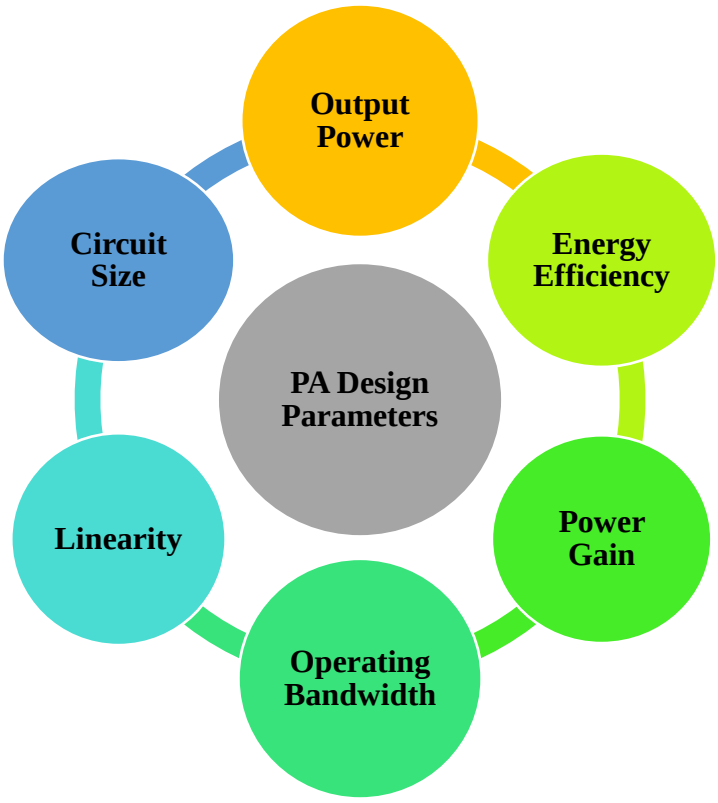


Figure 2.1. Performance trade-off in power amplifier design

A single stage power amplifier schematic is shown in Fig. 2.2. Here, the active device, i.e., transistor, is driven by an external RF power source (Pin) through a matching network at the input and the DC power supply (V_{DD}) is converted into RF output power (Pout) at the fundamental frequency (fo).

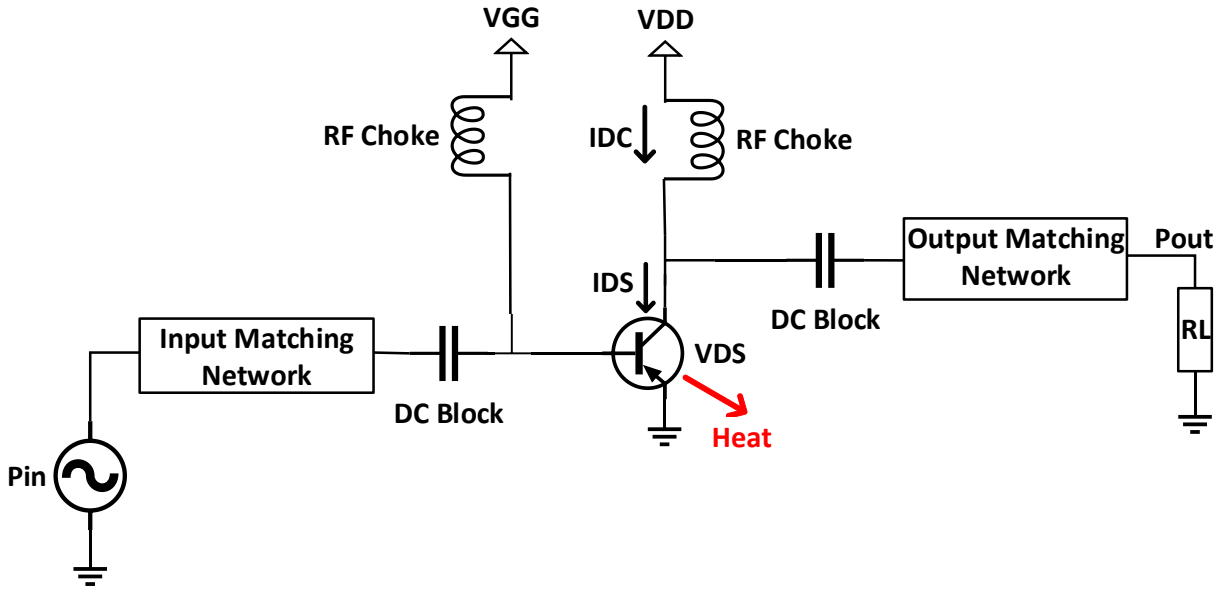


Figure 2.2. Single-stage Power Amplifier Circuit

2.1.1 Efficiency

The most power consuming component of any transmit chain is the PA. Primarily, PA is designed to deliver a specific amount of output power, with high energy efficiency. Simply put, efficiency is the measure of the amount of usable energy extracted relative to the energy supplied. Drain efficiency (ηdrain) at fundamental frequency (f0), is mathematically defined as

$$\eta drain = \frac{Pout(f0)}{Pdc} = \frac{G * Pin}{Pdc} \quad (2.1)$$

Where, ηdrain = Drain efficiency of the PA

Pout = Output power of the PA

Pin = Input power of the PA

G = Power gain of the PA

Pdc = Total DC power injected into the PA

The Pout of the PA can also be evaluated in terms of drain voltage and current waveform Fourier coefficients. The time domain current $I_{DS}(\theta)$ and voltage $V_{DS}(\theta)$ waveforms at the device output (drain) are expressed through their Fourier expansion [8] as

$$V_{DS}(\theta) = V_{DD} - \sum_{n=1}^{n=\infty} (V_{nr} \cos n\theta - V_{ni} \sin n\theta) \tag{2.2}$$

$$I_{DS}(\theta) = I_{DC} - \sum_{n=1}^{n=\infty} (I_{nr} \cos n\theta - I_{ni} \sin n\theta) \tag{2.3}$$

where, V_{DD} and I_{DC} are the DC components of drain voltage and current respectively. V_{nr}, I_{nr} are the real coefficients of drain voltage and current components. V_{ni}, I_{ni} are the imaginary coefficients and θ is the angular frequency. Using (2.2) and (2.3), alternatively the drain efficiency at fundamental frequency (f0) can be computed as

$$\eta drain = \frac{Pout\,(f0)}{Pdc} = \frac{1}{2} \frac{V_{1r}\, I_{1r}}{V_{DD}\, I_{DC}} \tag{2.4}$$

where, $V_{1r}\, I_{1r}$ are the fundamental components of voltage and current respectively

Although ηdrain is a good metric for evaluating the performance of a PA, however, another method for efficiency evaluation is Power Added Efficiency (PAE) given by

$$PAE\ (\%) = \frac{Pout - Pin}{Pdc} \text{ x } 100 \tag{2.5}$$

where, Pout, Pin and Pdc are represented in linear scale**.**

2.1.2 Power Gain

The power gain (G) of a PA is defined as the ratio of Pout to Pin of the PA given by

$$G = \frac{Pout}{Pin} \tag{2.6}$$

where, Pout and Pin are represented in linear scale

Ideally, as the input signal increases, the resulting output signal should increase with a constant gain provided by the amplifier. However, in practical scenario, PA gain is limited in nature. At small signal levels, the gain of a PA is usually constant (linear). However, as the input drive is increased, the device goes into compression due to the nonlinearities of the amplifier and the gain starts decreasing. It is known that non-linearities cause huge signal distortions and hence, ineffective communication. If the transistor is pushed further than a reasonable power level, the device may breakdown and burn. The saturation power (Psat) is the maximum power that a device is able to provide with certain gain compression. Fig 2.3 shows the Pout vs Pin of a single-stage PA. In a transmit chain, more than one amplifier may be used to get the desired gain.

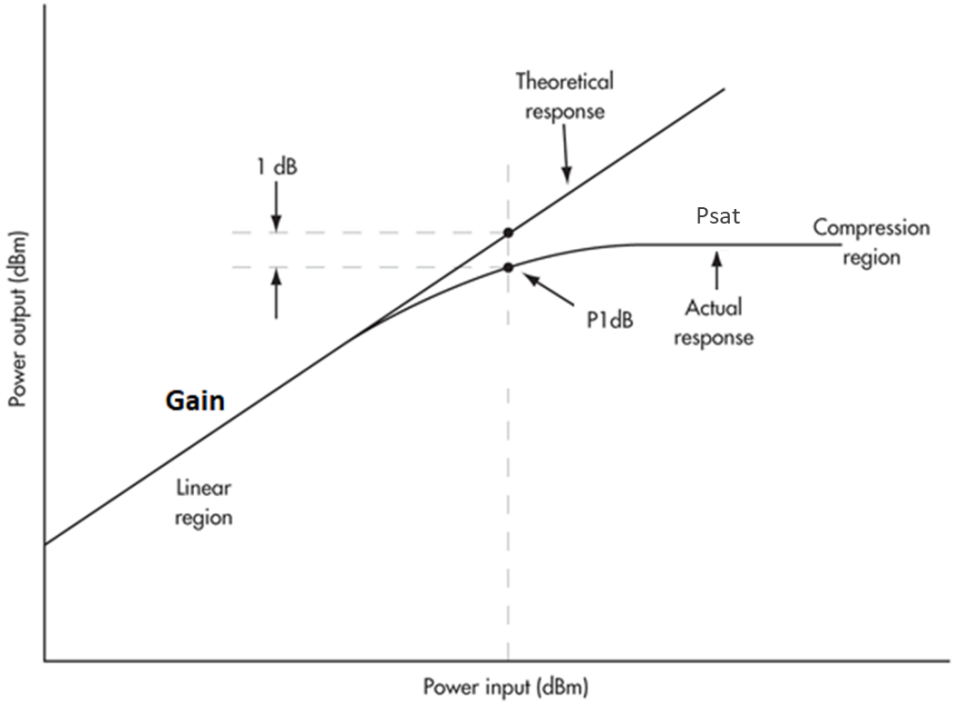


Figure 2.3. Pout vs Pin of a single-stage PA

2.1.3 Linearity

Linearity, in the simplest terms, is the measure of how closely input and output signal resemble. The PA design should be such that it does not distort the signal while amplifying it. Higher the linearity, lesser the distortion. Distortion causes multiple problems:

- Unwanted emissions, primarily harmonic distortions caused by driving the device into compression
- Inability to demodulate at the receiver, amplitude and phase distortion may cause signal to be unrecognizable by the receiver.
- Out-of-band noise, distortion from PA can increase out of band noise floor and create problems with receiver frequencies and/or cause regulatory issues.

Due to this phenomenon, 1-dB compression point (P1dB) value is defined to characterize the linearity of the amplifier as shown in Fig. 2.3. The PA is usually linear at small signal levels. But as the device is driven into compression, non-linearities start to appear. The two most common distortions of importance to a PA designer are AM-AM and AM-PM distortion. However, there is a trade of between linearity and efficiency of a PA. In many cases, the linearity of a PA can be improved using a linearizer such as digital predistortion (DPD) or analog predistortion (APD) to meet the industry standards.

2.2 Classes of operation

Traditional power amplifiers can be divided into two in terms of operation mode: transconductance-mode and switch-mode. The difference between the two types is the drain current and voltage waveforms, the latter having never overlapping current and voltage. In fact, more the overlap between the two waveforms, lesser is the maximum achievable efficiency. The traditional classes: A, B, AB and C are transconductance-mode PAs with different conduction angles. It is important to understand the fundamental operation of each of these classes to be able to design a PA. The various classes are explained next.

2.2.1 Class A

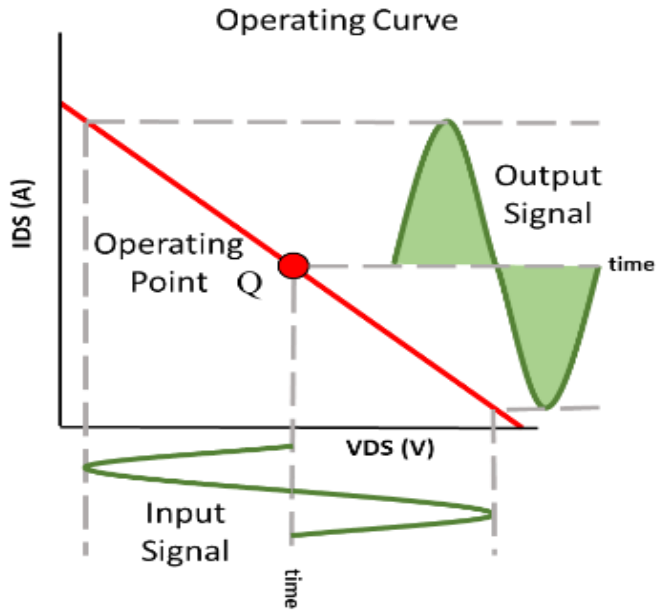


Figure 2.4. Biasing conditions for Class A PAs

The conduction angle for class A amplifier is 2π such that the current flows through the transistor the whole time (Fig 2.4). This is generally known as the linear class of operation as the input power level is low, hence the device operates in the linear region. Since the conduction is 2π, there is a maximum overlap between the current and voltage waveform leading to higher power dissipation. This restricts the maximum theoretical efficiency of the amplifier to 50%. However, the power gain in class A amplifiers is the largest. Additionally, Class A amplifiers are the most linear amplifiers. Such small signal amplifiers are suitable for linear applications like in audio amplifiers etc.

Practically, there always exists harmonics causing distortion such that the output would never perfectly resemble the input. IP2 (Intercept Point 2) and IP3 (Intercept Point 3) is the point at which 2^{nd} and 3^{rd} harmonic power is equal to the fundamental respectively. Higher the IP, better the amplification at large signals. In class A amplifiers, the design space is such that the IP2 and IP3 are very high and thus show better linearity.

2.2.2 Class B

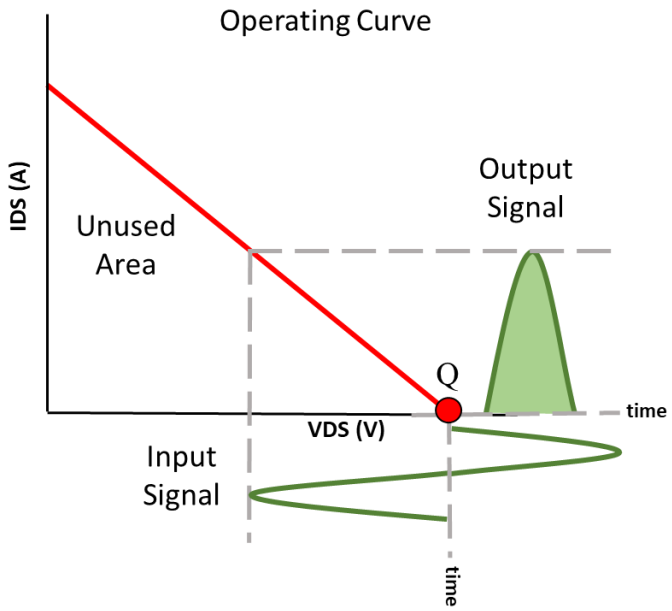


Figure 2.5. Biasing condition for Class B PAs

In class B biasing, the conduction angle is π. The transistor conducts for only half the time i.e., either the positive or the negative cycle of the input (Fig 2.5). This bias condition is also called pinch off. Since there is lesser overlap between current and voltage waveform, the maximum theoretical efficiency of the amplifier can be 78.5%. However, these amplifiers exhibit poor linearity as compared to class A. The harmonic distortions in this class are significantly higher and steps must be taken by the designer to manipulate/remove them using advanced waveform engineering. Class B amplifiers are very popular among power amplifier designs, when used with an additional linearization circuit. This class can be used as the main branch in conventional Doherty architecture.

2.2.3 Class AB

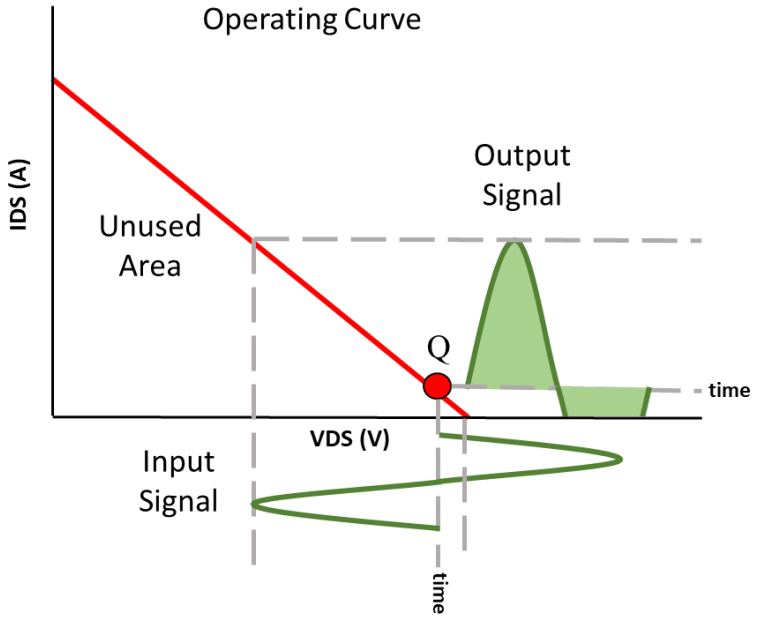


Figure 2.6. Biasing condition for Class AB PAs

The conduction angle is between π and 2π. The transistor conducts for less than full but more than half of the cycle (Fig 2.6). The theoretical maximum achievable efficiency is between 50-78.5%, depending on the position of the bias point which is somewhere between class A and B. Such amplifiers are popular because they provide a good tradeoff between efficiency and linearity. Usually, the Class AB amplifiers find good use in main amplifier branch of the Doherty architecture.

2.2.4 Class C

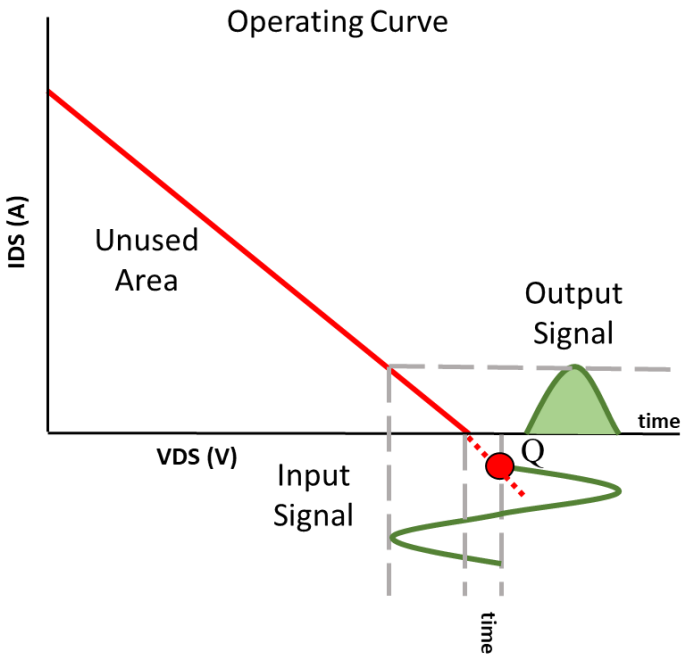


Figure 2.7. Biasing Condition for Class C PAs

The conduction angle is less than π. This class operates in the cut-off region. For the most part, the transistor is in cut-off region such that there is no conduction current in the transistor (Fig 2.7). To be able to have a little current, the device must be driven hard. In other words, at low power level, the device acts as open circuit, but when the input power level is significantly high, the device turns on. The theoretical maximum efficiency however is 100% as the device is mainly in cutoff region. Such amplifiers exhibit very poor linearity. The power gain of class C amplifiers is the lowest. This type of application is ideal to make auxiliary amplifiers in the Doherty architecture which will be discussed in further sections.

2.2.5 Constant-Current Biased Classes

The traditional power amplifiers designs are based on constant voltage power supplies used to bias the output of the transistor, shown by squares in Fig 2.8. In these voltage biased transistors, a constant voltage is applied to the drain of the transistor and the current is controlled by the voltage at the gate. However, in this work, a dual case of voltage biasing is also used in the RMDB power amplifier design.

This new biasing leads to a new set of operational classes called constant-current biased transistor classes namely Class A*, Class AB*, Class B* and Class C* as introduced in [4]. In current biasing scheme, the voltage and current at the output of the transistor are interchanged. The DC source provides a constant-current bias to the drain of the transistor while the voltage at this point can be controlled by the gate voltage at the input terminal.

Referring to [4], for a voltage-biased transistor, in the reduced conduction angle classes of operation (classes AB, B, and C), the bias point is set close to the cut-off region. In this condition, the current is very low and voltage is high such that the transistor is "pinched-off" and will present a quasi-open impedance to the output. However, when the transistor is biased in constant-current, as shown with stars in Fig 2.8, the bias classes (AB*, B*, C*) are biased close to the knee voltage, such that the transistor has a higher current with comparatively very low voltage. In this condition, the transistor presents a quasi-short impedance at the output. The voltage at the output of the transistor is controlled by the voltage at the source.

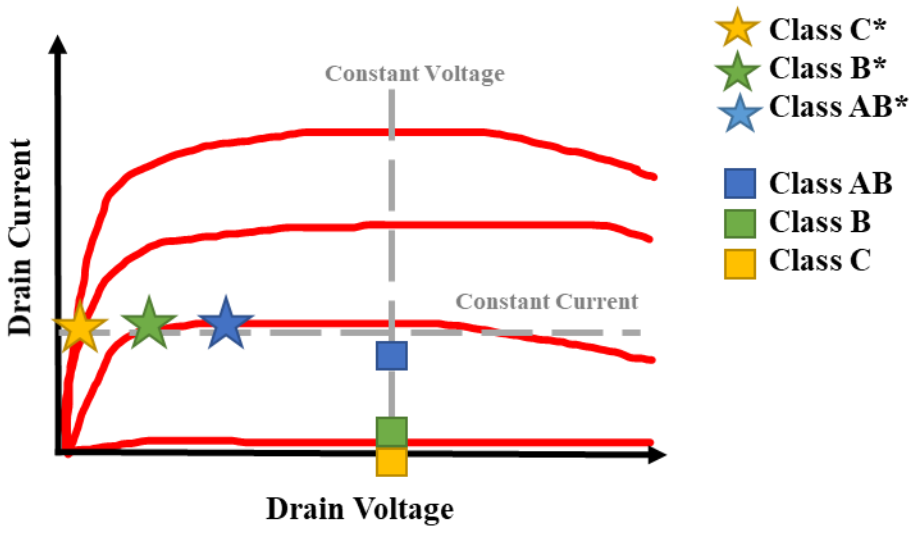


Figure 2.8. Biasing condition for constant current-biased vs voltage-biased transistors

2.3 Load Modulated Power Amplifiers

In modern technology, the modulation schemes such as OFDM, QAM etc. have time varying envelopes with high PAPR typically ranging from 6-10dB. This implies that the transmitter PA should be

able to amplify large but infrequent peak signal power. Moreover, most of the time, it is required to amplify relatively smaller signal powers which makes up the average power. The main challenge with traditional PAs is that the high efficiency is only observed at the peak output power and drastically drops at lower power levels. Thus, the PAs are inefficient for the most part of operation when used with modulated signals in practical scenario. The main idea behind load modulation is to dynamically change the load impedance presented to the transistor in order to improve efficiency at the back off power levels. The Doherty and RMDB PA architectures employ this concept of load modulation to achieve efficiency improvement at back-off.

2.3.1 Classical Doherty

The concept of load modulation was introduced in 1936 by W.H. Doherty [1]. It was originally conceptualized around vacuum tubes. As the years passed, DPAs got lost in the history. Recently in the early 21st century, the concept was resurrected. As shown in Fig 2.9, the efficiency curve at OPBO is much improved in DPA as compared to a conventional PA. Hence, DPA is preferred architecture for modern modulation wireless solutions.

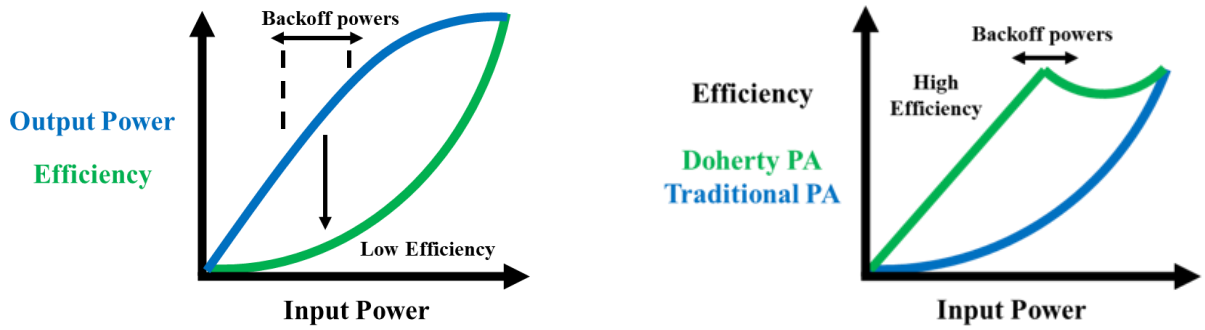


Figure 2.9. Efficiency curve of Conventional Classes vs Doherty Power Amplifier

A basic dual-branched Doherty circuit consists of two amplifiers, the carrier (main), and the peaking (auxiliary). It is important to note that in literature, carrier/main amplifier and peaking/auxiliary amplifier are interchangeable terms. The carrier amplifier is typically biased at class AB while the peaking

is biased in deep-class B or C. This ensures that both amplifiers work at large signal drive but only the carrier works at back-off, maintaining the efficiency throughout the signal. The conventional Doherty designs consists of the carrier and peaking branch biased by DC voltage sources, which provide a constant voltage at the drain while the current is varied/adjusted with the help of gate bias voltage.

The main working principle of a conventional DPA is based on the fact that for a voltage biased transistor, the output power is inversely proportional to the load resistance,

$$Pout \propto 1/RL \tag{2.7}$$

where, RL is the load resistance at the output of the PA, which means, the Psat of a transistor can be increased/decreased by decreasing/increasing the load impedance respectively. In application, if the transistor of the main branch operates with a higher load impedance (say, 2RL), it can saturate earlier and provide the first peak of efficiency at back-off. Beyond this, the main and auxiliary amplifiers can work in conjunction to produce second efficiency peak at Psat.

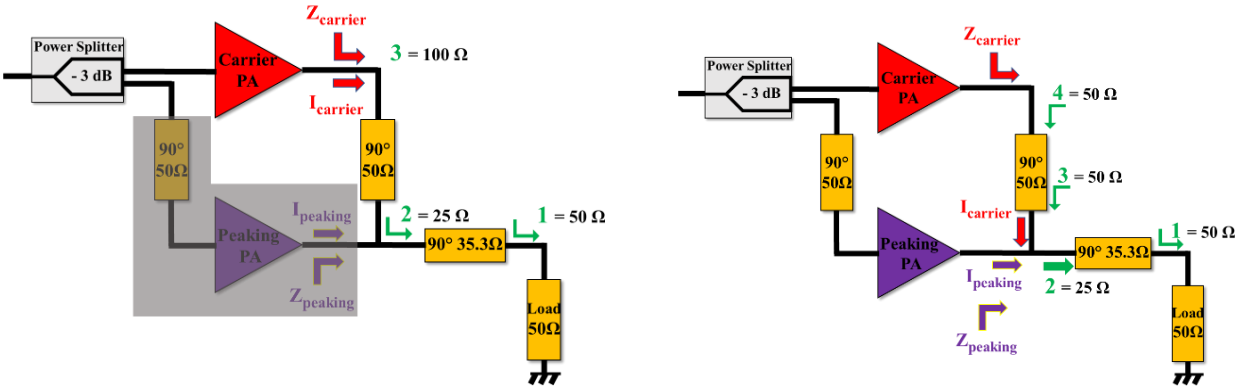


Figure 2.10. Doherty PA at low power (left) vs Doherty PA at high power (right)

The output of the main amplifier is combined with the output of the auxiliary amplifier with an impedance transformer using a 50 Ω quarter-wave transmission line. When main amplifier is under operation at lower power levels i.e., back-off (Fig. 2.10 (left)), the auxiliary amplifier is in non-conducting state and the quarter wave transformer sees the optimum load, RL (50 Ω), at the end. This means that the

optimum load, RL (50 Ω) is transformed to 25 Ω by 35.3 Ω transmission line which is inverted by the 50 Ω quarter wave transformer such that the main amplifier sees twice the optimum impedance, 2RL (100 Ω), at its output as shown by the green arrows in Fig. 2.10 (left).

When the auxiliary amplifier starts to conduct beyond this power level as shown in Fig. 2.10 (right), the current flowing from the output of the auxiliary amplifier increases which results in decreasing load impedance of main and auxiliary amplifiers from 2RL (100 Ω) to RL (50 Ω) and open circuit (very high resistance) to RL (50 Ω), respectively as shown in Fig. 2.11.

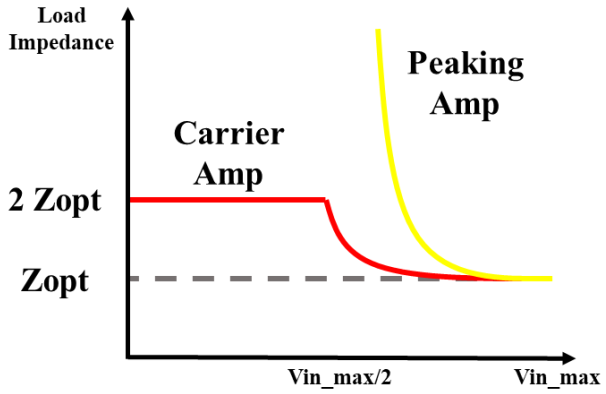


Figure 2.11. Load Modulation in Doherty PA

Output matching networks provide impedance transformation for the two branches. Generally, the load impedances seen by the transistor in the load pull for back-off and Psat conditions are very close in value. Therefore, the matching network for main branch is optimized either for back-off operation or at saturated power as it is hard to design a matching network that can match an impedance to 100 Ω and 50 Ω ohm simultaneously. The main drawback of such architecture is the bandwidth limitation due to circuit elements used in the matching circuits and impedance inverter [15-16]. Thorough analysis has been done in the previous literature which provides enough evidence that with the conventional output combining network implemented using a quarter-wavelength transmission line, the enhancement in output power and efficiency of the Doherty PA significantly reduces when we deviate from the center frequency of operation.

All the design previously implemented cannot avoid using the quarter-wavelength transformer in one way or another which inherently limits the BW of the PA. Also, the designs are complicated and require larger circuit size. These drawbacks essentially are tackled by the RMDB PA which eliminates the need of an impedance inverter all together, hence resulting in a wideband design as explained in following section.

2.3.2 Reverse Load-Modulated Dual-Branch PA (RMDB PA)

In recent years, a new PA architecture was introduced by Akbarpour et. Al [4], which proposed a constant-current drain bias of the carrier amplifier in the conventional Doherty architecture. This is called as the RMDB PA. In this architecture, the carrier PA is connected directly to the load resistance, without any quarter-wavelength transmission line like in the conventional Doherty as shown in Figure 2.12.

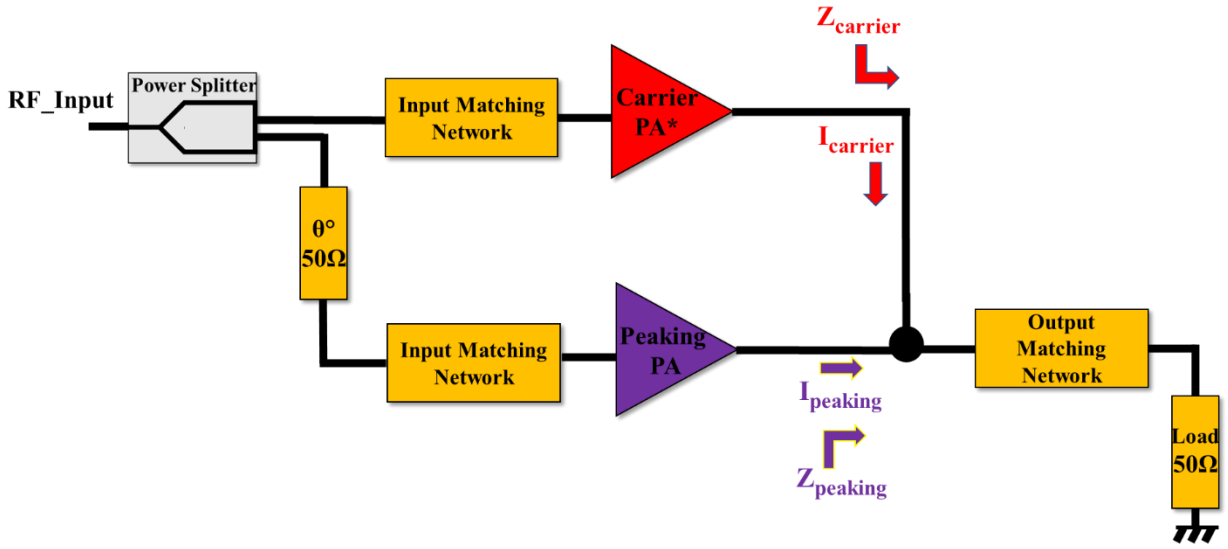


Figure 2.12. Reverse Load-Modulated Dual-Branch PA (RMDB PA) structure

This constant-current biasing led to a new set of properties exhibited by the transistor which opens a door to new designs schemes. One of the major benefits of this new biasing scheme is called Reversed Load Modulation, which means that the maximum output power of the transistor increases by increasing the load impedance (up to a certain optimum impedance), which is the opposite case of conventional

constant-voltage biased transistors as explained in previous section. The output power(Pout) for constant-current drain biased transistor is given by:

$$Pout = RL^* (Idrain^2/2) \quad (2.8)$$

Where, RL is the load impedance and Idrain is drain current [4]. To illustrate the reversed load modulation concept, Fig 2.13 shows the ηdrain vs Pout for various RL for a constant-current biased transistor [4]. The plot clearly shows that efficiency and output power of the transistor increase with increase in the load resistance (from blue to green to red).

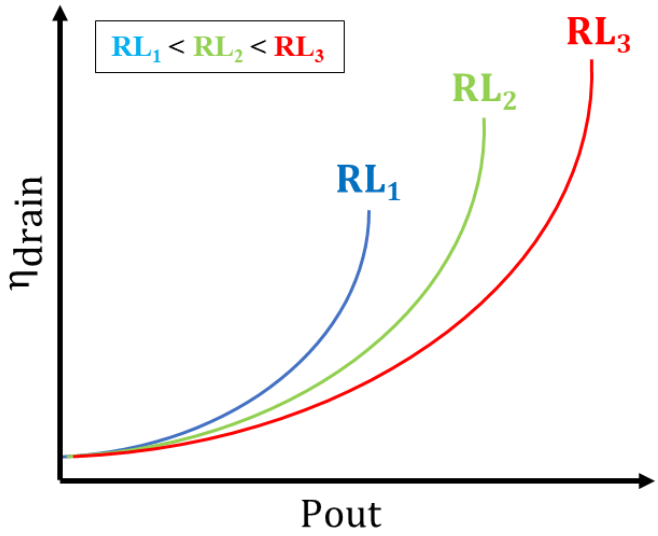


Figure 2.13. ηdrain vs Pout of a constant-current transistor

Reverse load modulation concept can also be explained through load-line plot. Fig 2.14 shows that for a constant-current biased transistor, the increase in RL will result in higher voltage swing, hence higher output power. Hence, at OPBO, we do not require an impedance inverter in the carrier branch. This behavior is opposite to the conventional constant-voltage biased transistors.

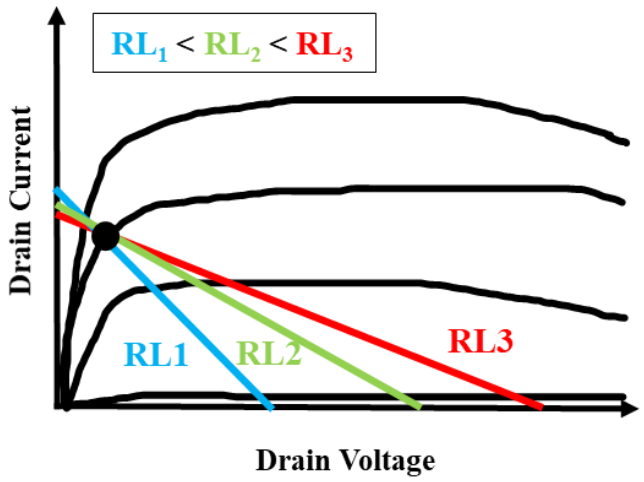


Figure 2.14. Load-line of a constant-current transistor

Utilizing this property of a constant current biased transistor, the need for an impedance inverter in the carrier branch is eliminated as the impedance variation at the junction point is exactly what is desired for this architecture i.e., the carrier amplifier should have a smaller load impedance at the backoff point and the load impedance should increase until the saturation point. This is a critical concept behind the functioning of RMDB PAs. This concept has been very well explained in previous literature for constant-current biased PA [4][7].

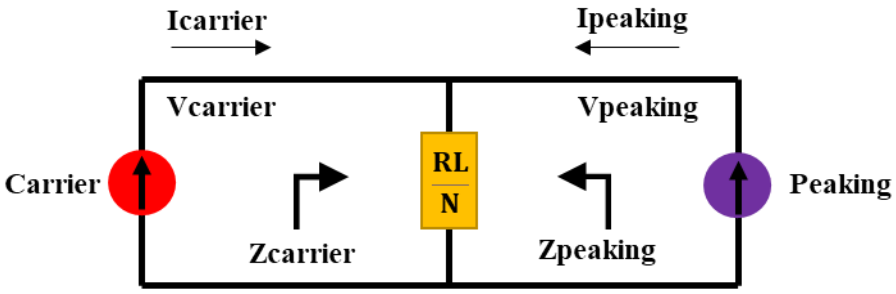


Figure 2.15. Equivalent circuit of RMDB PA

In Figure 2.15, if Icarrier and Ipeaking are the output currents in carrier and peaking branch respectively and Vcarrier and Vpeaking are the output voltage across the device for carrier and peaking

branch respectively, then, the load modulation of load impedance RL for a RMDB PA can be explained using an equivalent circuit, where,

$$\text{OPBO} = 20 \log_{10} \text{N} \tag{2.8}$$

and, $\text{N} = \frac{\text{Psat,PA (saturated power of RMDB PA)}}{\text{Psat,carrier (saturated power of carrier PA)}}$

then the carrier impedance (Zcarrier) and peaking impedance (Zpeaking) are given by:

$$\text{Zcarrier} = \frac{\text{Vcarrier}}{\text{Icarrier}} = \frac{\text{RL}}{\text{N}} \frac{(\text{Icarrier} + \text{Ipeaking})}{\text{Icarrier}} = \frac{\text{RL}}{\text{N}} \left(1 + \frac{\text{Ipeaking}}{\text{Icarrier}}\right) \tag{2.9}$$

$$\text{Zpeaking} = \frac{\text{Vpeaking}}{\text{Ipeaking}} = \frac{\text{RL}}{\text{N}} \frac{(\text{Icarrier} + \text{Ipeaking})}{\text{Ipeaking}} = \frac{\text{RL}}{\text{N}} \left(1 + \frac{\text{Icarrier}}{\text{Ipeaking}}\right) \tag{2.10}$$

To further illustrate and verify the load modulation theory in RMDB PA [7], let's take an example of a symmetric RMDB PA (i.e., N = 2) with RL = 50 Ω as shown in Figure 2.16.

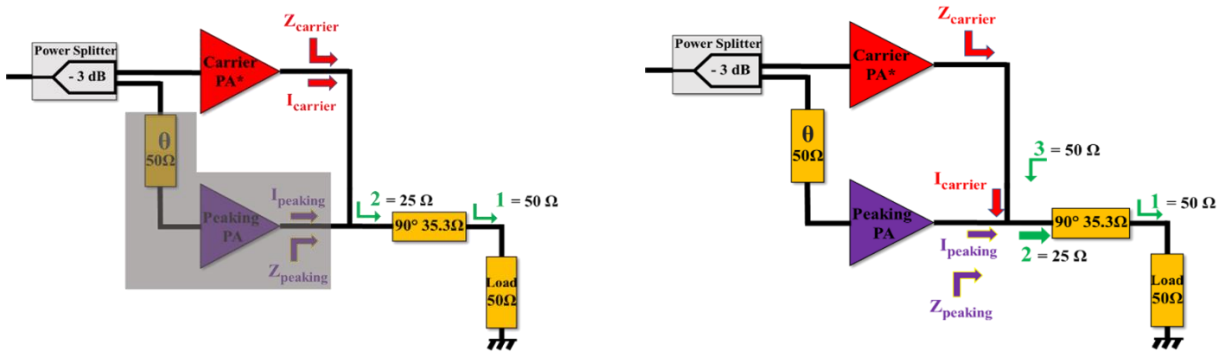


Figure 2.16. RMDB PA at low power (left) vs RMDB PA at high power (right)

In RMDB PA, the output of the carrier amplifier is directly combined with the output of the peaking amplifier. When carrier amplifier is under operation at lower power levels i.e., back-off (Fig. 2.16 (left)), the peaking amplifier is in non-conducting state and current biased transistor sees half of the optimum load, RL/2 (= 25 Ω), verified by equation 2.9. This means that the optimum load, RL (50 Ω) is transformed to 25 Ω by 35.3 Ω transmission line at its output as shown by the green arrows in Fig. 2.16 (left).

When the peaking amplifier starts to conduct beyond this power level, the current flowing from the output of the peaking amplifier increases which results in increasing the load impedance of main and auxiliary amplifiers from RL/2 (25 Ω) to RL (50 Ω) and open circuit to RL (50 Ω), respectively as shown in Fig. 2.17. Also, these values are coherent with the deduced equations 2.9 and 2.10, hence, verifying the theoretical analysis. This effect is termed as reverse load modulation.

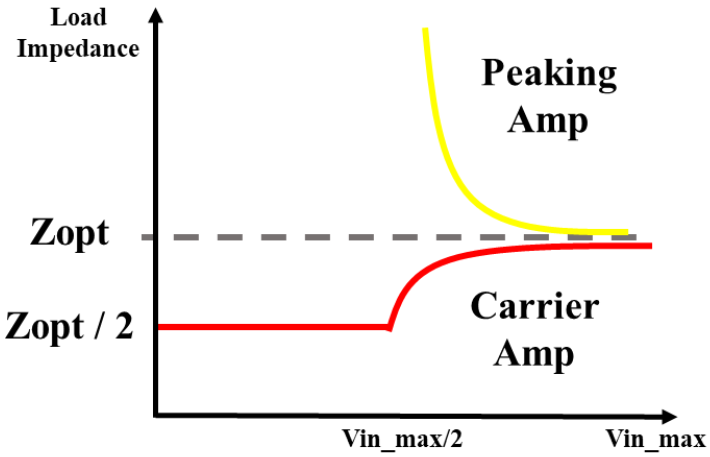


Figure 2.17. Load Modulation in RMDB PA

As mentioned earlier, the impedance inverter is a major contributor towards circuit bandwidth limitation. However, the two branches are connected directly in this architecture, with a common output matching network after the common connection point as shown in Fig. 2.10(a). This reduces the circuit size tremendously which works best for an MMIC design. In this work, an MMIC with constant-current biased RMDB PA architecture is presented. The circuit schematic of the design is shown in Fig 2.18.

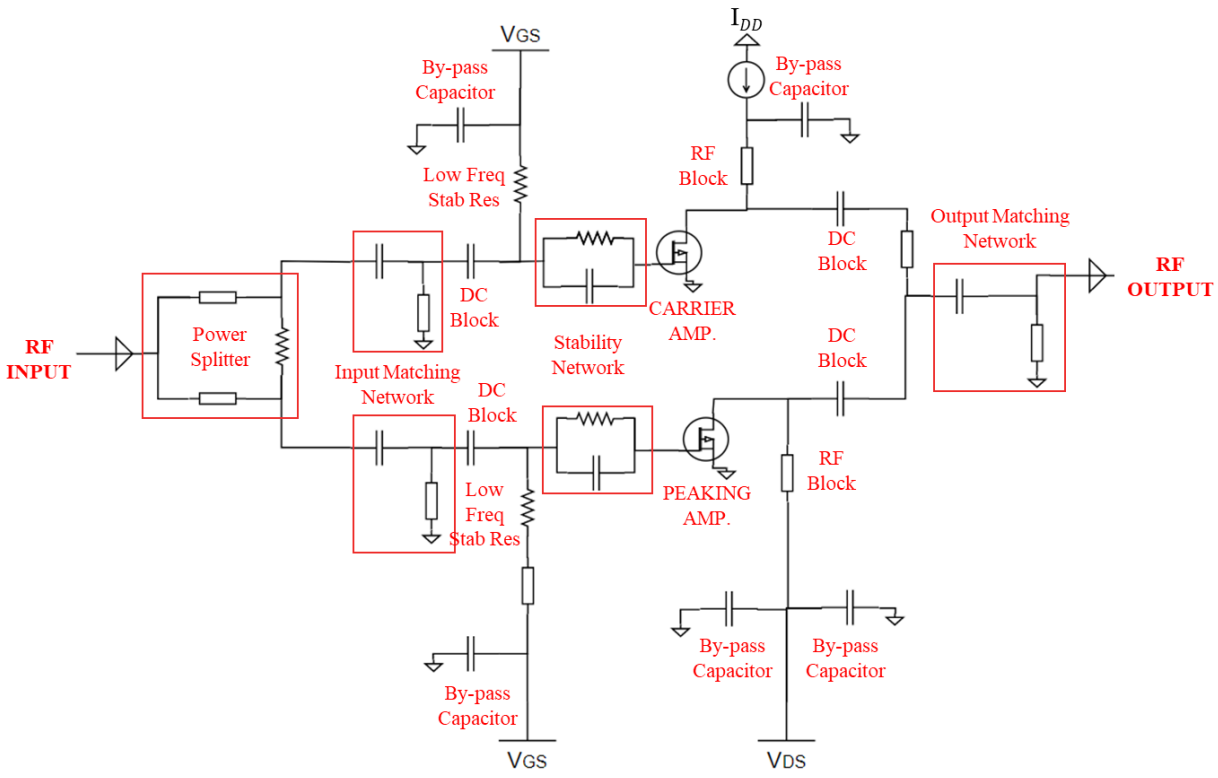


Figure 2.18. RMDB PA Schematic

In this work, an asymmetric PA architecture is implemented which requires a larger size transistor for the peaking PA than for the carrier PA to provide the higher power and wider load modulation range [9-10].

Chapter 3. SINGLE-STAGE POWER AMPLIFIER MMIC AT 2.5 GHZ

3.1 Non-coaxial measurements and TRL calibration

The device under test (DUT) measured by the Vector Network Analyzer (VNA) is usually a network made up of one or more ports each of which can pass, absorb and/or reflect RF signal. The VNA injects RF energy into one port as well as measures the RF emerging from any other ports (Fig 3.1). These measured quantities are usually expressed in the form of S-parameters which are complex, frequency-dependent values. The connections to the DUT can be established either with coaxial connectors when using cables or with non-coaxial media when using test fixtures or making on-wafer measurements with probes. Calibration with coaxial connectors is relatively straight-forward which uses discrete impedance standards easily available in the market. A major problem encountered when making network measurements in microstrip or other non-coaxial media is the need to separate the effects of the transmission medium (on which the device is embedded for testing) from the device characteristics.

When our DUT is connected or "embedded" in a structure or a fixture, we need a method to bring the measurement reference point to the DUT connection points instead of the fixture (red dot shown in Fig 4.6). In other words, calibration is critical for accurate VNA measurements to remove (calibrate out) the effect of the fixture. This is called fixture compensation. The need of fixture compensation is especially true at higher frequencies which are common in modern applications. In the world of electronics, no device is ideal and even simple wire has a small inherent parasitic inductance, capacitance and resistance associated. During an experiment, these normally insignificant frequency dependent properties, manifest themselves at higher frequencies. Thus, as frequency increases, the non-ideal behavior becomes more prominent, especially at GHz level. Therefore, to move the measurement reference plane to the DUT, fixture compensation becomes more important at high frequencies for accurate design and measurement results.

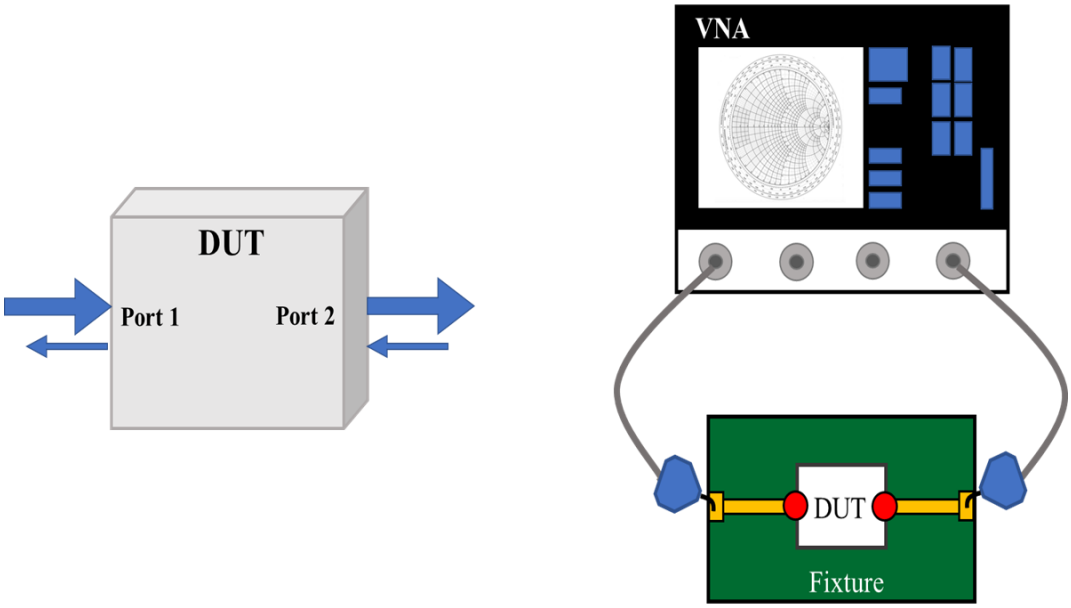


Figure 3.1. Vector Network Analyzer Measurements for Device Under Test

One method of implementing these calibration standards is something called TRL calibration where TRL stands for the calibration standards through, reflect and line.

Transmission lines have traditionally been used as standards and are well understood. There are many advantages of using transmission lines as reference standards. First, transmission lines are among the simplest elements to realize in many non-coaxial media. Second, the impedance of transmission lines can be accurately determined from physical dimensions and materials. These calibration standards are normally implemented in the form of so-called test coupons which are specifically prepared sections of printed circuit boards. Typically, TRL calibration uses four or more coupons of various types. Making measurements with multiple coupons creates a system of equations that can be solved for so called error terms similar to how they are solved for coaxial DUTs and CAL standards. This methodology provides very accurate results if the coupons and DUT have similar characteristic impedances. The accuracy of this measurement also depends on the availability of quality calibration standards.

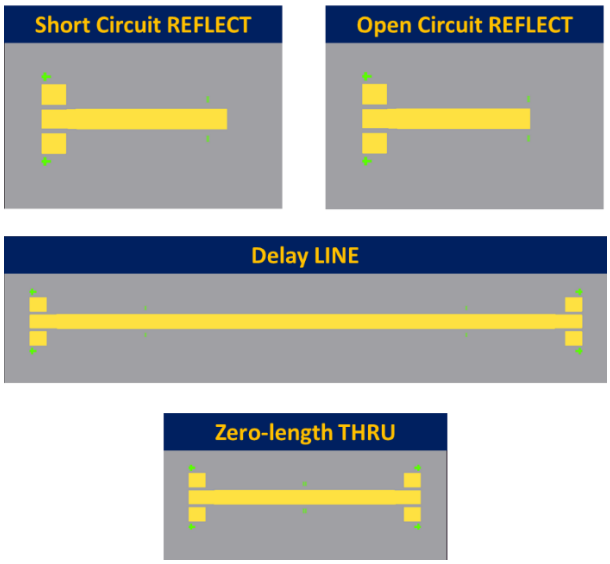


Figure 3.2. TRL calibration kit for up to 10 GHz

Calibration using TRL consists of the three basic standards (Fig 3.2) for measurements:

1. **REFLECT** - connect identical one-port high reflection coefficient devices to each port
2. **THRU** - connection of port 1 and port 2, directly or with a short length of transmission line
3. **LINE** - insert a short length of transmission line between port 1 and 2 (different line lengths are required for the THRU and LINE)

Fixture calibration can produce very accurate measurements however, it does require characterized calibration standards with specific design requirements, and these can be quite challenging to implement.

The work presented in this chapter is done in collaboration with an industrial partner Recon-RF, Inc. *This work was supported by Mitacs through the Mitacs Accelerate progra*m. The calibration standards are designed from 1-10 GHz for customized probes at Recon-RF facility. Fig 3.3 shows that the phase difference between the delay LINE and zero-length THRU lies between 20° to 160° and hence are valid up to 3rd harmonic.

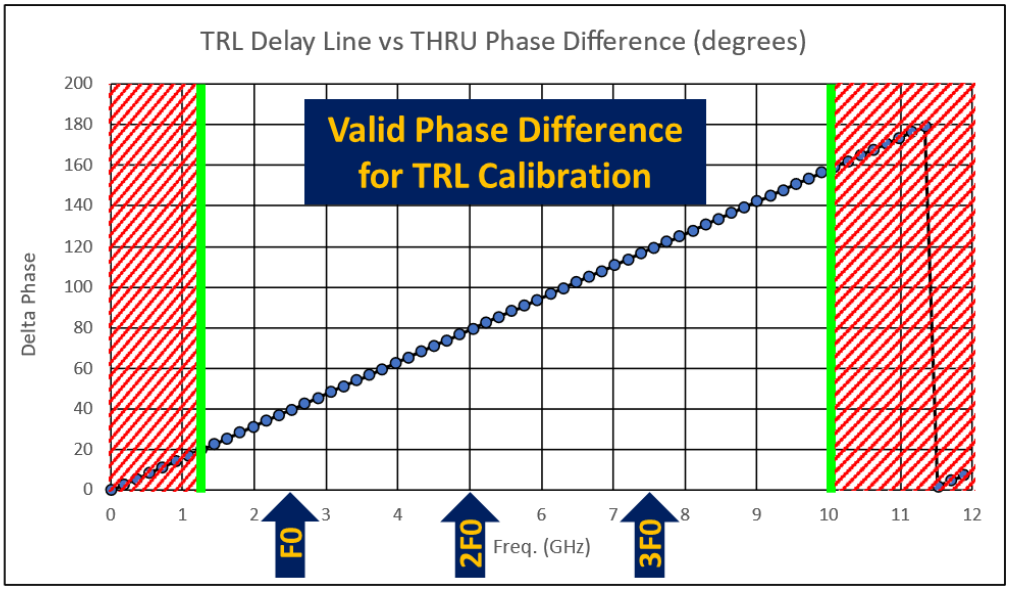


Figure 3.3. The insertion phase difference between the THRU and LINE is between (20 and 160 degrees)

3.2 Single-stage solid state PA MMIC

The design flow of a single-stage PA design begins with selecting a suitable MMIC process and transistor for the application. In this case, the application is wireless communication at 2.5 GHz. The DC bias point of operation is selected through direct-current current-voltage (DCIV) analysis by plotting drain current vs voltage curve for different gate voltages. In this design the CREE GaN field-effect transistor (FET) is biased in class AB as this class of operation provides a good trade-off between linearity and efficiency. Then, stability analysis is done through S-parameter simulations and a series resistor is added at the gate to stabilize the transistor. Fundamental source-pull and load-pull is performed to determine optimum impedances that should presented to the input and output of the transistor, respectively. Since this design is a high-power design, impedance for maximum Pout is selected. Based on this, the matching network is designed for input and output using transmission lines, stubs, and wire bonds. Once the full schematic is obtained, circuit is optimized and fine-tuned for best performance. For this design, the DC biasing networks are off-chip and can be easily added later for circuit measurements. Each step in this design process is discussed in the following sub-sections.

3.2.1 Technology choice – GaN 0.5um HEMT Cree FET

To support modern wireless architecture systems, there is a growing need for architectural research on advanced transmitter/power amplifier technology that can radically push the performance envelope of mm-wave amplification to another level. In terms of frequency and power, GaN outperforms other technologies at all levels. Higher breakdown voltage, higher switching speeds and lower on-resistance offers a lucrative opportunity to deploy GaN RF switches in the actual cellular infrastructure, leading to better performance and a more compact size. Similarly, higher power density cut-off frequency and breakdown voltages also provide room for innovation in deploying GaN-based PAs into such systems for 5G applications.

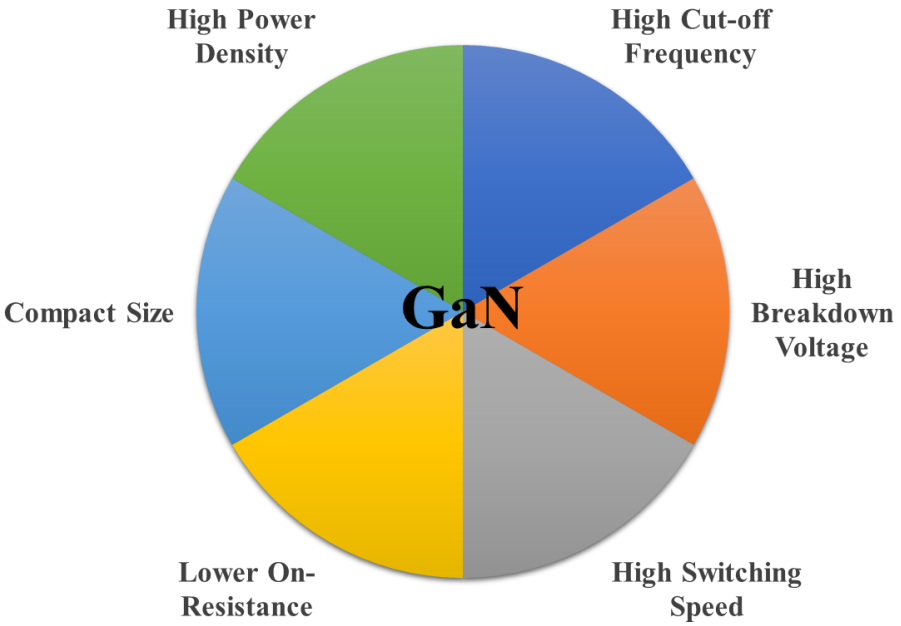


Figure 3.4. GaN Technology Performance Evaluation

The single-stage PA design uses CREE 0.5µm HEMT GaN on Silicon Carbide (SiC) FET biased at 50V Vds, customized by Recon-RF, which can deliver 11W of RF output power per mm of gate width. GaN technology has proven capability for the realization of Solid-State Power Amplifiers (SSPAs). As the

technology matures it is seeing increased adoption for applications requiring high linearity and high-power density.

Careful consideration must be taken while selecting the operating bias voltage and the gate length of the transistor. For example, higher the drain voltage, more the output power capability of the transistor, however, lower the efficiency and power gain. Similarly, shorter gate lengths (e.g., 0.15um, 0.18um etc.) can provide great power densities at higher frequencies (mm waves) and however they come with recoverable and/or non-recoverable performance degradations due to gate length scaling and are also expensive. Since this is a high-power amplifier design, centered at 2.5 GHz operating frequency, the chosen drain bias voltage of 50V and gate length of 0.5um seem reasonable choice.

Process	CREE (High Power GaN on SiC, customized by Recon-RF)
Active Device	HEMT
Power Density	11 W/mm
Gate Length	0.5 um
Cut off frequency	18 GHz
Vpinch	-5 V
Vds DC	50 V
Max frequency	10 GHz

Table 3.1 Transistor Technical Specifications

3.2.2 Detailed Amplifier MMIC Design and Layout

The design of a single-substrate SSPA with a ceramic substrate, wire bonds, and discrete GaN FET is shown in Fig 3.5. Each part of the layout will be discussed in further sections.

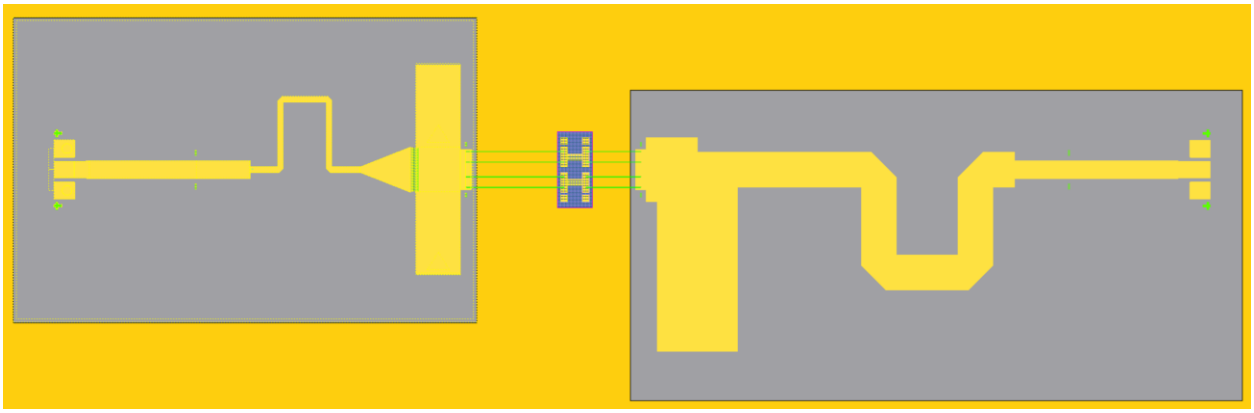


Figure 3.5. Single-stage solid state PA MMIC layout

3.2.2.1 Bias point selection

The design process commenced with selecting the transistor size and bias point of the transistor for meeting design requirements. The 0.5um GaN HEMT CREE FET, (5.5mm x 0.8 mm transistor) can deliver 11 W of RF output power per mm. The transistor is biased in class AB at 50 V and 60mA quiescent current at the drain which will allow a good trade-off between efficiency and linearity. The biasing networks are added off-chip in this design to facilitate proper direct current - radio frequency (DC-RF) isolation post-fabrication.

3.2.2.2 Small signal gain and stability

A graph of the maximum available gain (Gmax) vs frequency is shown in Fig 3.6. At the operating frequency of 2.5 GHz, the maximum available gain Gmax is 23.47 dB. It should be noted that this Gmax is for small signal only. At large signals, the transistor behavior will deviate due non-linearities. A safety margin for gain must be kept in mind allowing for the losses due to bias network, stability circuit, matching networks etc.

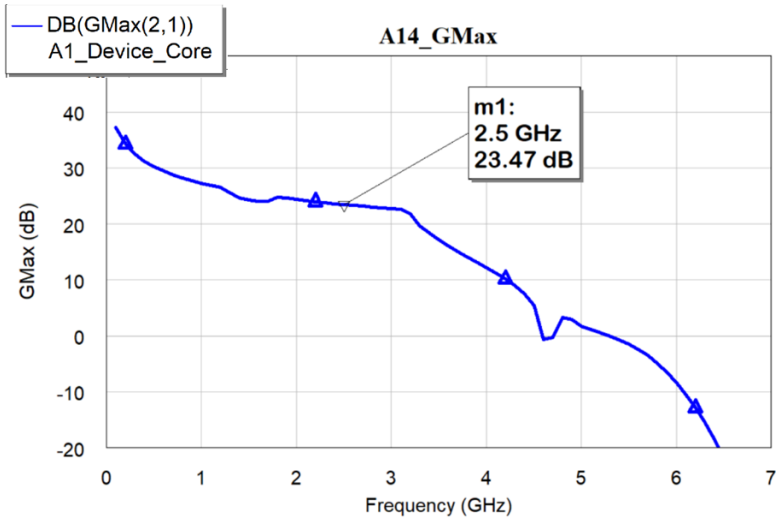


Figure 3.6. Maximum Available Gain vs Frequency

To gauge stability, Mu factor can be used. Mu factor gives a measure for the distance of the nearest instability from the center of the smith chart. Fig 3.7 shows the Mu factor vs frequency indicating the stability condition for the bias points and frequency selected. MU1 (darker) and MU2 (lighter) are the input and output stability Mu factors resp. At 2.5GHz, the FET is potentially unstable and is stabilized using a series resistor at the gate. The Mu for stabilized FET is > 1 at 2.5 GHz. Any low frequency instability can be handled by off-chip biasing circuit.

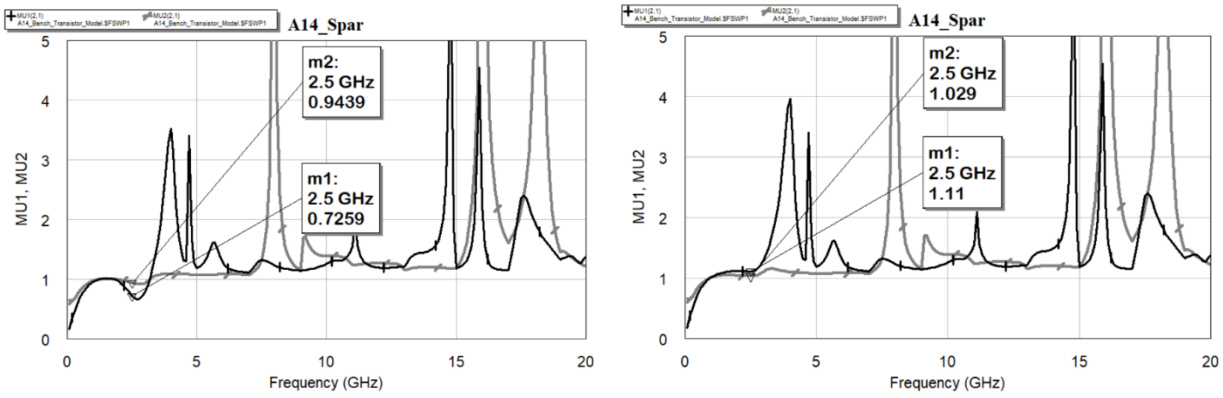


Figure 3.7. Stability Mu factor vs frequency before and after the stability circuit

3.2.2.3 Source pull and Load pull

Optimum design of the output and input matching networks requires large signal characterization of the active device. In fact, scattering parameters (small signal parameters) are no longer effective in terms of device representation under non-linear/large signal conditions. Load-pull technique is then described as a non-linear tool for large signal device characterization.

A load-pull setup consists of the device under test (DUT) with impedance tuners at the output (and input, in case of source-pull). The impedance tuners provide the DUT with the tunable load/source impedance while simultaneously measuring the DUT performance. Note - The source impedance is mainly tuned to enhance the power gain of the active device. The large signal performance can be investigated as a function of input and output terminations, bias point, and input power at a particular frequency. The results can be then presented on the Smith chart in terms of efficiency and Pout contour levels as depicted in Fig.3.8. These contours are the loci of set of impedances over which amplifier exhibit constant output power , PAE etc. The load pull results are discussed next.

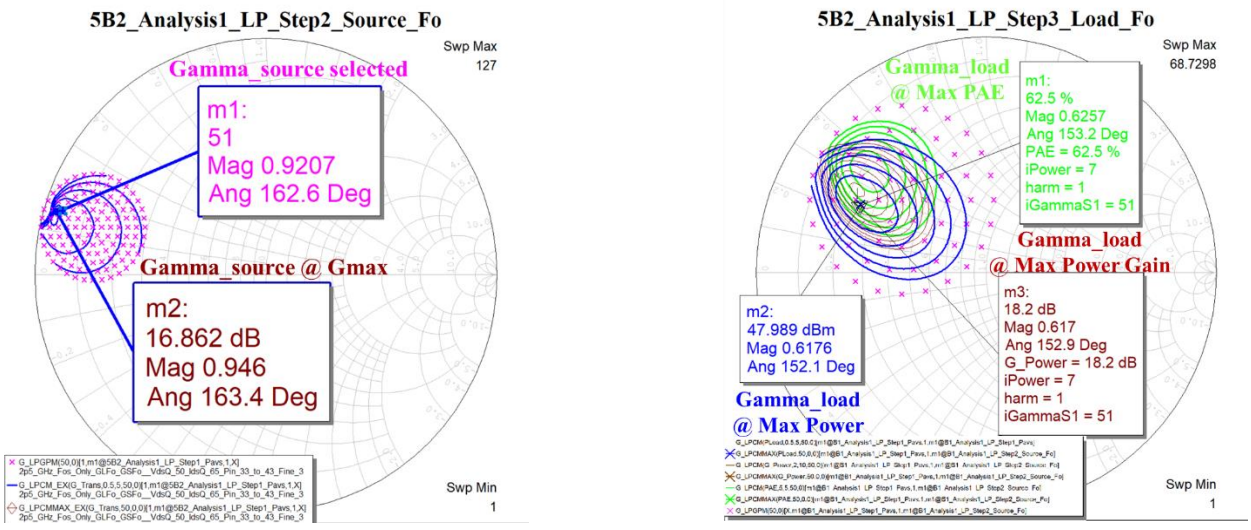


Figure 3.8. Load pull and Source pull Contours for the CREE device

For each frequency and bias point, there is a load and source termination corresponding to maximum achievable output power and efficiency. Consequently, input and output matching networks can be designed in order to present predicted impedance to input and output of the active device to achieve the desired performance. After the loadpull analysis, the transistor is capable of giving max PAE of 65% and max Pout of 48 dBm (63 W). Since this design is for high-power single stage PA, impedance corresponding to max Pout is selected as target for matching network.

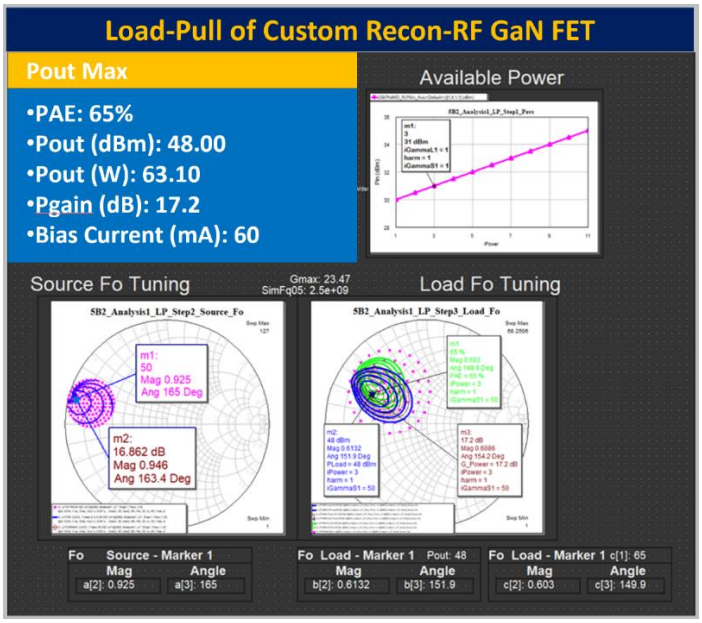


Figure 3.9. Load pull and Source pull Performance summary of the ReconRF FET

Although the CAD simulation load pull results can be trusted in the case of the CREE transistor used, however, in order to verify the simulation and actual performance of the transistor, a modelling cell is designed using single-substrate type 50Ω characterization cell for the discrete GaN FETs and accompanying wire-bonds. This will enable accurate FET characterization measurements and facilitate measurement vs modelling activities for S-parameters, Input vs output power (PIPO), Modeling and Pulsed IV curves. However, the actual load pull measurement is a scope for future work due to time constraints.

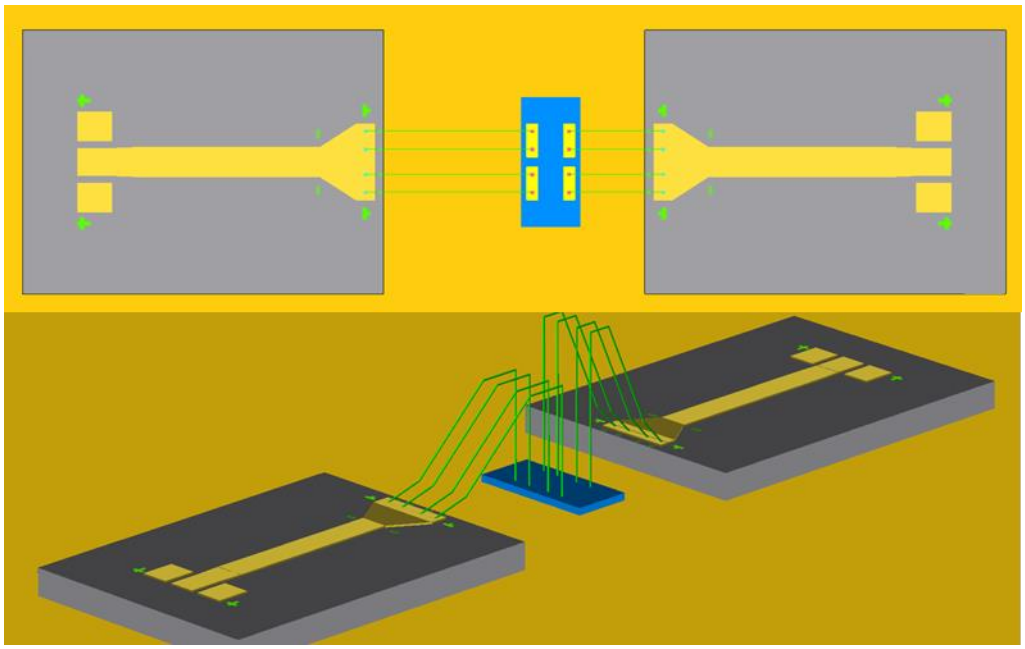


Figure 3.10. A single-substrate (Alumina) type 50 Ω characterization cell for the discrete GaN FETs and accompanying wire-bonds

From virtual load pull, the maximum saturated power delivered to the load is just over 63 W (48 dBm); at this stage no allowance for output matching, combining or biasing networks has been made. Usually, a design performance trade-off must be made while choosing the optimum impedance between efficiency, Pout, gain, linearity etc. Since this PA is designed for high output power, the target impedance chosen is for Max Pout. Fortunately, for this transistor, the two optimum impedances for max PAE and max Pout are not far apart, which works in favor for best achievable performance.

	Source Impedance	**Load Impedance**
Max Pout	**2 + j*6.6 Ω**	**12.7 + j*11.7 Ω**
Max PAE	2 + j*6.6 Ω	13.2 + j*12.6 Ω

Table 3.2 Load and Source Impedances for CREE GaN FET from load pull simulation

3.2.2.4 Matching Network

Before the synthesizing a matching network, the extensive load pull simulations of the nonlinear device model carried out (as mentioned in above section) at various bias points ensured that optimal device size, load impedances and current densities were selected. This process helps in ensuring high success rate of a working design.

After the transistor characterization, matching networks are designed to provide the transistor with the required impedances. The target impedances resulting from virtual load-pull activities were realized through the single Alumina substrate for Input matching network (IMN) and Output matching network (OMN) and transmission line effects producing the correct response at the reference plane of the FET. IMN and OMN is optimized to conjugate match condition to maximize power transfer such that the source and load impedances are a conjugate match of the input and output impedance.

The OMN consists of impedance transformer to transform 50 Ω to 12.7 + j*11.7 Ω for optimum performance. The IMN consists of impedance transformer to transform 50 Ω to 2 + j*6.6 Ω for optimum performance (Fig 3.11).

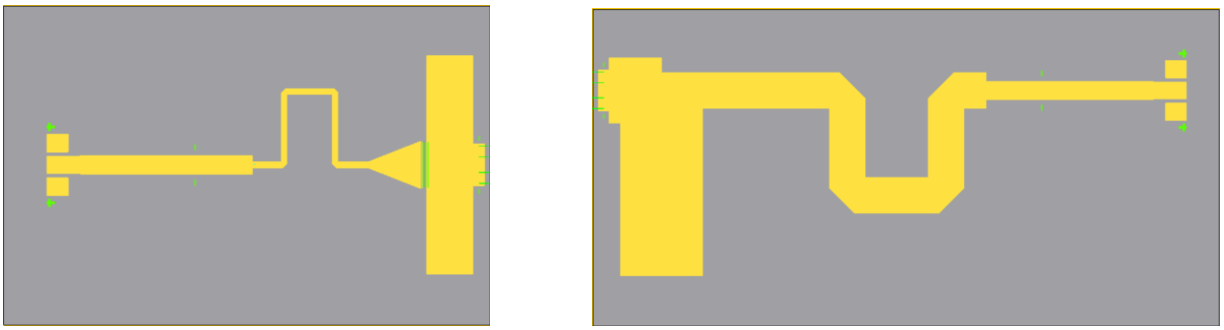


Figure 3.11. Input Matching Network (left) and Output Matching Network (right)

3.2.3 Simulated Performance

The simulations were performed in AWR software in Microwave Office. All the passive structures were EM-simulated in EM Extract and the transistor cell was simulated using CREE's nonlinear device

model. Ground-signal-ground (GSG) pads were included at the RF input and output to allow RF on-wafer probe testing if required.

Fig 3.12 shows power sweep simulation for the EM simulated PA at the center frequency of 2.5 GHz. At 37 dBm Pin, the designed PA can achieve max PAE of 54.3 % at 2.5 dB gain compression with 47.4 dBm Pout (56 W). The output power obtained from this simulation is quite close to the load pull estimation of 48 dBm, which validates the design. As shown in the plot, the efficiency of the PA (green curve) drops after the peak point at 37 dBm. This is because the transistor is in a non-linear region when saturated. Beyond this power level, it goes into deep compression such that there is no increase in Pout with increased Pin, which results in efficiency degradation.

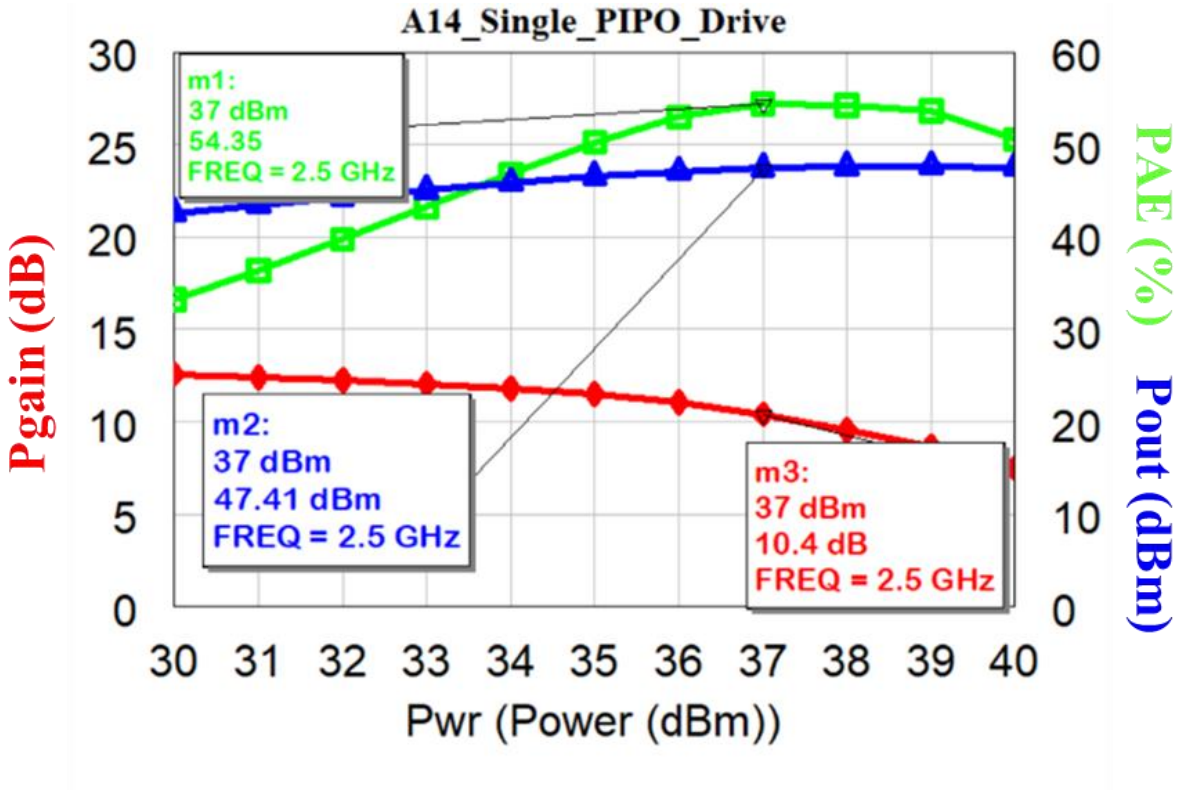


Figure 3.12. Simulated PIPO performance of the single-stage PA

The final layout of the designed single-stage MMIC PA is shown in Fig 3.13 depicting sections including the input and output matching network which transform the 50 Ω terminations to the desired source and load impedances, respectively. An off-chip DC biasing network, consisting of an RF choke and by-pass capacitors with a resistor at the gate for low frequency stability, can be easily added during measurements. This will provide more freedom to stabilize the FET post fabrication and provide appropriate DC-RF isolation in measurements without considerably affecting the RF performance. The overall chip dimensions for the single-stage PA is 20.6 x 9mm^2.

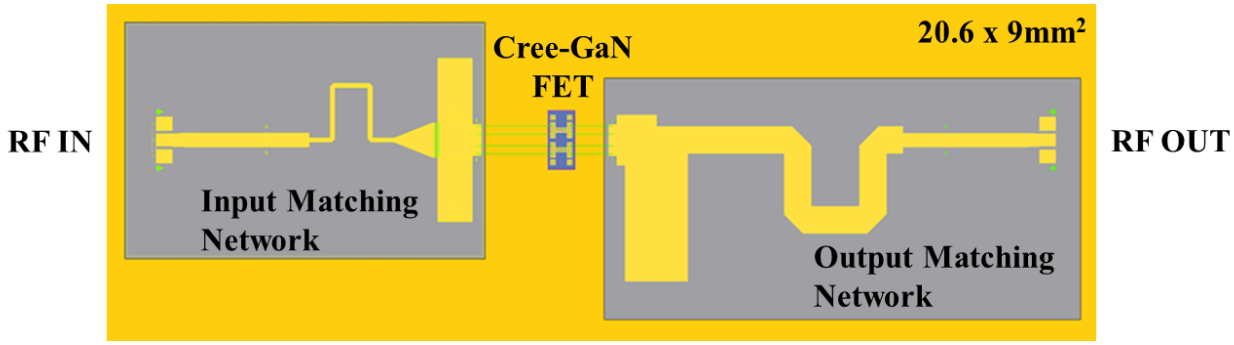


Figure. 3.13. Final layout of the single-stage MMIC PA (chip size 20.6 x 9 mm^2)

As evident from Fig 3.12, the efficiency of a single stage PA drops drastically at back-off power levels. With this low efficiency at OPBO, the single state PA cannot be used as is when driven with modern signals having high PAPR. Therefore, we need a better design architecture with enhanced efficiency at back-off power, such as an RMDB PA, to suit the requirements for modern transmitter systems.

Chapter 4. RMDB POWER AMPLIFIER DESIGN AND SIMULATION

Modern modulation schemes are implemented to increase spectral efficiency of the available, rather expensive, frequency bands. These schemes lead to RF signals with high PAPR and a strong demand is created for PAs to provide high efficiency at both peak and back-off power levels. As explained in detail in section 2.3.2, different from a conventional Doherty PA, RMDB architecture uses a current-biased transistor in the main branch of the PA to achieve proper load modulation without using an impedance inverter at its output. As a result, this architecture presents load modulation across wide bandwidth and facilitates smaller matching network at the output, reducing the overall chip size. This chapter presents and discusses the design methodology and simulated results for an RMDB PA implemented on a MMIC for sub-6 GHz wireless application.

The design flow of an RMDB power amplifier (Fig 4.1) begins with understanding the performance specifications and selecting an appropriate transistor. Since the design in this work is implemented on a MMIC for sub-6 GHz wireless application, a suitable MMIC process is selected. The non-linear FET model available in the design kit is simulated for DC analysis by plotting the drain current and voltage curves over different input gate voltages, and the bias point is selected for each branch. In this RMDB PA, UMS 0.25um GaN HEMTs are used where the main branch FET is biased class B* and auxiliary is biased C, explained in detail in further sections. Following this, we can perform small-signal analysis on the FET for the max available gain and stability analysis of the transistor. If needed, an RC stability network can be added to stabilize the device.

Load-pull analysis is then performed on the transistor to gauge the performance of the device when driven close to saturation. Such analyses are important since power amplifiers work at high powers and small signal behavior analysis will not hold true. Referring to the RMDB PA design flowchart in Fig 4.1, steps 2-4 are performed for both main and auxiliary devices individually. From the load pull, optimum impedance targets are recorded, and matching networks are designed for them. For maximum power

transfer, the source and load impedances are conjugately matched to the input and output impedance of the device through the matching networks. Individual input matching networks for each branch with a power splitter and a common output matching network are designed. RF chokes, DC blocks and by-pass capacitors can be used for RF-DC isolation. Once the basic schematic of the amplifier design is obtained, optimization and fine-tuning can be done to obtain the best performance.

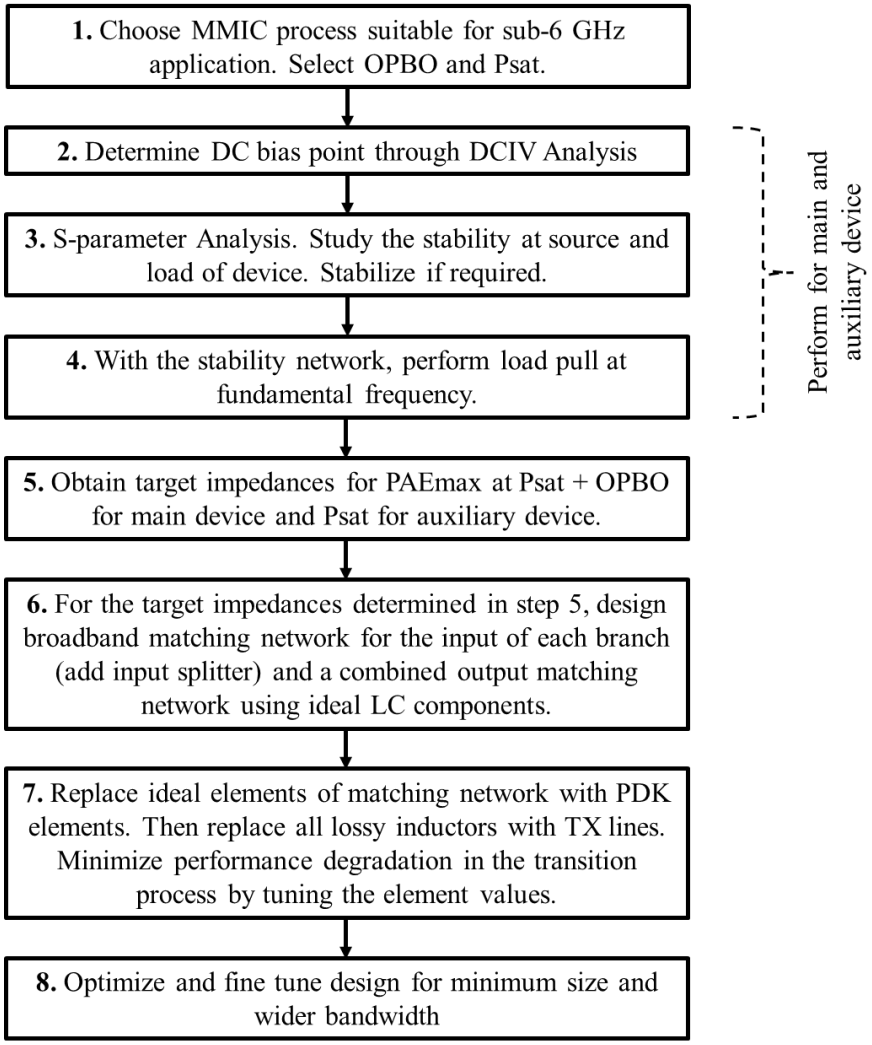


Figure 4.1. RMDB Power Amplifier Design Flow

4.1 Technology choice

With the achievement of large advances in the cellular infrastructure industry, high cutoff frequency devices such as gallium arsenide (GaAs) and gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have accelerated the commercial mainstay market for cellular infrastructure with evolving demands for size, reliability, linearity, power density and energy efficiency [11]. Conventional technologies such as Silicon (Si), laterally diffused metal-oxide semiconductor (LDMOS), or GaAs are limited in performance compared to GaN, which stands as a promising candidate for different applications. GaN-based discrete RF Power transistors are exceeding expectations by providing both flexibility and performance advantage to cater to future demands. In MMIC design, a Process Design Kit (PDK) is often used which, in simple terms, is a library with detailed structural information of all the design components like capacitor, resistors, microstrip lines, vias etc.

In this work, the MMIC RMDB PA is designed and fabricated using UMS GH25 technology. This 0.25 μm gate length GaN high electron-mobility transistor (HEMT) process is suitable for PA designs up to 20 GHz. In this design, an asymmetrical RMDB PA [7] is proposed to provide high OPBO (~ 10-11 dB) while covering the sub-6-GHz 5G frequency from 3.4 to 4.0 GHz.

4.2 Bias point selection

The bias point selected will determine the class of each amplifier branch i.e., main and auxiliary. Selection is based such that both transistors work at large signal drive but only the carrier works at back-off, maintaining the efficiency throughout the signal. For an RMDB PA, the main FET is constant-current biased to provide proper load modulation without the use of an impedance inverter at output. This is because the Pout of a constant current biased transistor decreases with lower load impedance. The reason for selecting a voltage-biased class C amplifier for the peaking branch is the requirement on the power leakage at power back-off before peaking transistor turns ON. As explained in [4], a class C* current-biased transistor has a low small-signal output impedance while a voltage-biased transistor has a high output impedance (with parasitic capacitive reactance). If a current-biased class C* amplifier is used as the peaking

amplifier, then at power back-off, it presents a low output impedance and leads to a high-power leakage into the peaking transistor. To avoid this, we bias the peaking device in class C.

In Fig 4.2, the DCIV curve on the left is of an 8Fx150um transistor for the main branch, biased at class B*, with a constant drain current of 273mA and gate biased at -2.3V. For the auxiliary branch (right), an 8Fx200um transistor, is biased in class C, with a constant drain voltage of 28V and gate biased below pinch-off at -4.9V.

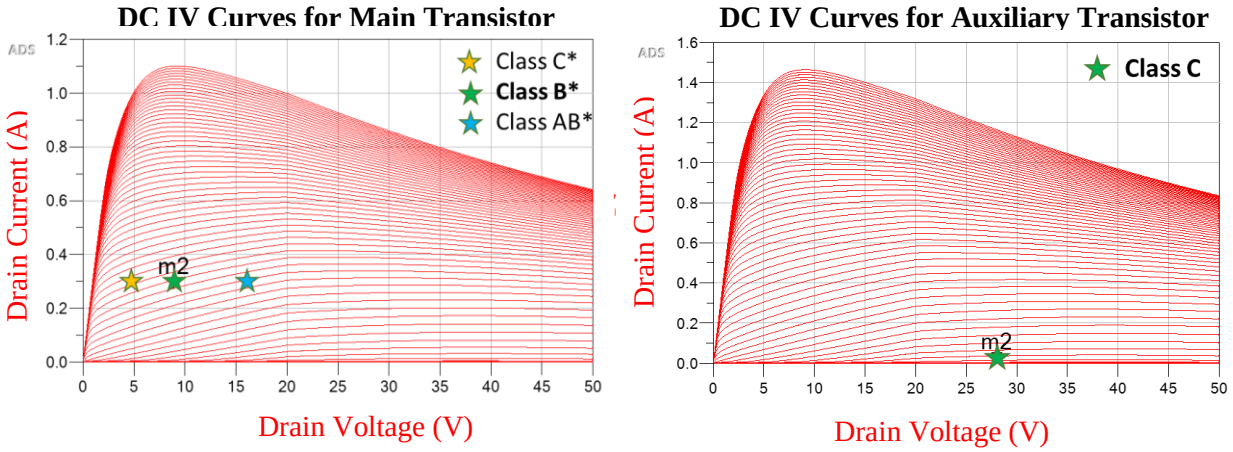


Figure 4.2. DC Bias Point selection for the RMDB PA – Main transistor (left), Auxiliary transistor (right)

4.3 Stability and Small signal gain

The stability network of a transistor must be checked before load pull since it might modify the behavior of the transistor. Both the branches are stabilized separately. Careful consideration taken while stabilizing the transistors is that the stability should not only be in the operating band, but also out of band, especially lower frequencies. Stability of a transistor is crucial to prevent oscillations from occurring upon testing the circuit, which will ruin the performance of the circuit completely. The aim is to push the instability circles out of the smith chart so that the whole chart is available for the design space without the worry of future oscillations (Fig 4.6). The transistors can be stabilized at the gate side by an RC network or a small resistor at the input. Additionally, a resistor is added in the gate bias to attain lower frequency

stabilization. The stability network of each transistor (Fig 4.3) in the RMDB PA differs due to different device size and bias conditions.

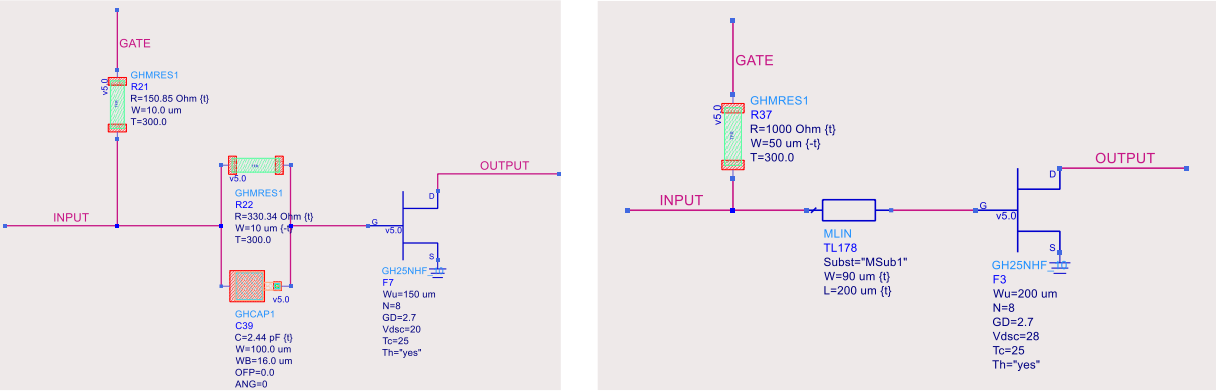


Figure 4.3. Stability Circuit for Main (left) and Auxiliary (right) Branch

It is important to note that stability comes with a trade-off for the gain. Better the stability, lower the gain. Nevertheless, if the transistor is unstable, even the best performing amplifier in simulations will not work in practical scenario. Therefore, both the transistors are stabilized for all frequencies up to 10 GHz (roughly upto 3rd harmonic frequency).

Stability can also be measured using s-parameters through Rollet factor (K) and their matrix determinant (Δ) as mentioned in [18] by,

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} \tag{4.1}$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \tag{4.2}$$

where, S_{11} = Input port voltage reflection coefficient

S_{12} = Reverse voltage gain

S_{21} = Forward voltage gain

S_{22} = Output port voltage reflection coefficient

To achieve unconditional stability, K > 1 and Δ < 1. Stability is an important design consideration in PA design to prevent the device from going into oscillation and damaging itself through sudden high currents. Fig 4.4 and 4.5 show the stability factor (K) and Δ for main and auxiliary device after stabilization and both are unconditionally stable from DC to third harmonic.

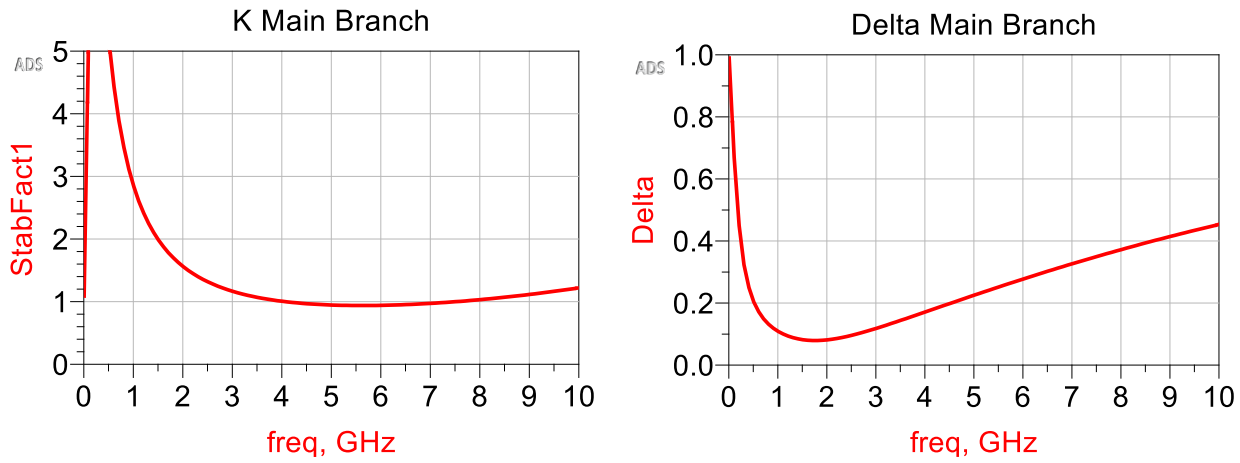


Figure 4.4. Stability Analysis for Main Transistor

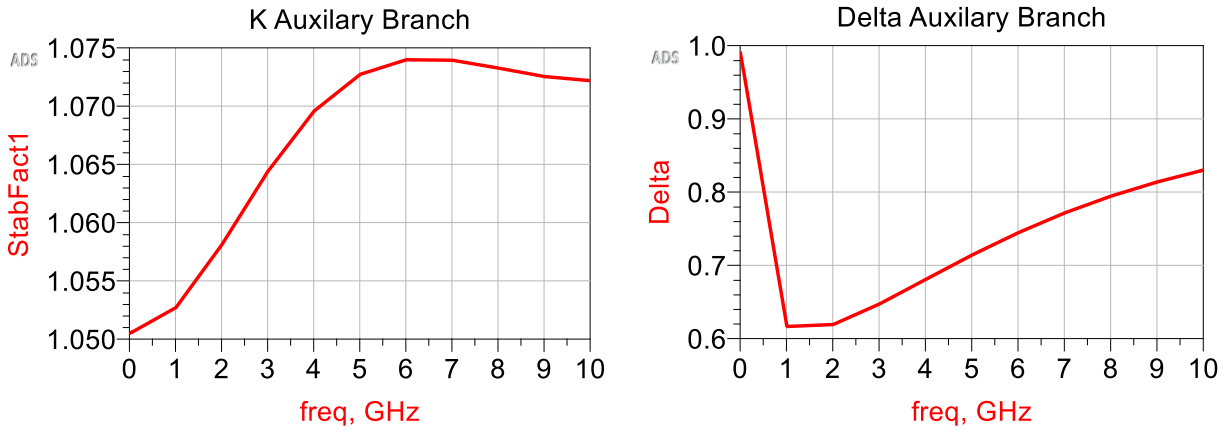


Figure 4.5. Stability Analysis for Auxiliary transistor

Source and load stability circles are also plotted from DC to 10 GHz after stabilization to ensure unstable regions are pushed out of the Smith chart for much greater flexibility in design. Fig 4.6 also

indicates that the transistors are not only stable in design band but also in lower frequencies where the gain is highest.

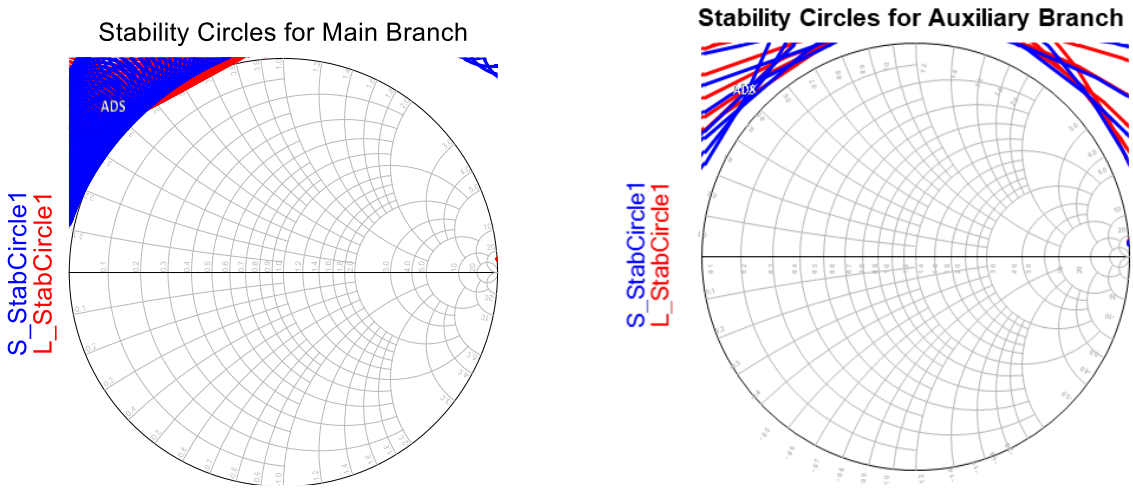


Figure 4.6. Stability Circles for Main Branch (left) and Auxiliary Branch (right)

4.4 Source pull and Load pull

In practical scenario, impedance at the source and load terminations of the amplifier is usually connectors or other cables presenting 50 Ω. The standardization of 50 Ω terminations is chosen as it is a great compromise between power handling and attenuation. However, for optimum performance, in terms of output power, efficiency etc., the transistor must see different impedances at either termination, perhaps with reactive component. To maximize power transfer from the source to the transistor, the source impedance that the transistors see at its input is a complex conjugate of the input impedance. For the output matching, if one wants to maximize the output power, similar conjugate matching approach can be applied, where the transistor is matched with a load equal to the complex conjugate of the transistor output impedance. However, in practice, the load impedance is chosen to optimize the efficiency, the linearity, or the output power. More often, a load impedance that achieves a tradeoff between these metrics is chosen. To know what these impedances are, we perform load pull/source pull. In this work, virtual load pull test bench from ADS is used. This test bench sweeps the input power that excites the device, performs the load pull and plots Pout and efficiency contours as shown in Fig 4.7, with the point of maxima at the common

center of each set of contours. From these plots, the designer can select impedance targets for the design. In this work, the load pull is optimized for maximum PAE condition. For the main branch of the RMDB PA, the load pull is carried out to find the impedances at power back-off (29 dBm) as well as at saturation output power (33 dBm). For the auxiliary branch, the load pull is done only at saturation (38 dBm), since at back-off, the peaking branch is ideally off. The power levels are selected to give the RMDB PA an OPBO of 10 dB at 29 dBm with overall Psat of 39 dBm when both devices saturate.

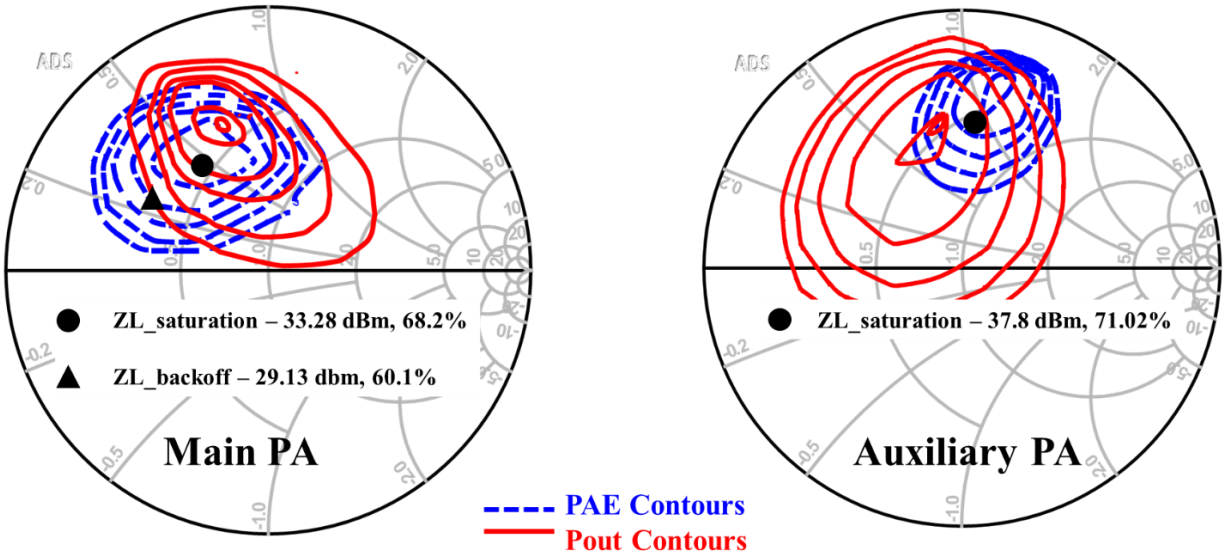


Figure 4.7. Fundamental load-pull simulation results for Main PA (left) and Auxiliary PA (right)

For this design, the three sets of impedances selected for highest PAE, predicts approx. 60 % PAE at OPBO and approx. 70 % PAE at Psat in simulation for the RMDB PA. Based on the load pull, the impedance targets tabulated are as follows:

	Load Impedance	**Source Impedance**
Main_PA_backoff	17.6 + j*11.7	2.7 + j*29.3
Main_PA_sat	22.2 + j*24.1	2.7 + j*29.3
Auxiliary_PA_sat	27.4 + j*48.5	4.3 + j*36.1

Table 4.1. Load and Source Impedances for Main and Auxiliary Devices

For this design, the simulation is done only at fundamental frequency, while keeping the harmonics ideally open. Optimizing harmonic terminations is crucial to achieve accuracy in the final design, however, is a scope of future work. This is rather time consuming and due to time constraints; the performance is studied for just the fundamental frequency. It is worth mentioning that the device along with its stability network is used in the load pull bench as this will result in more accuracy to find the optimum impedances.

Using the load pull bench, analysis and choice is made for the optimum impedance by carefully considering output power, efficiency, and gain compression. This process is iterative and time consuming, however, this is the best way to attain the optimum performance.

4.5 Matching Networks

There are three steps followed in the design of matching networks. Firstly, using lumped components to observe the most ideal possible performance expected through the design. This is achieved by using the Smith Chart Utility tool in ADS. Although simple and straightforward, this technique gives a good starting circuit for the matching network.

Secondly, for a high-pass design, usually LC-network with a series capacitor and shunt inductor are used. Due to the lossy nature and restricted operating bandwidth of the inductors at high frequency, the goal of this step is to replace all inductors obtained in first step, with transmission lines. The matching networks are now realized using capacitors and ideal transmission lines to estimate best performance.

Lastly, after the parameters of ideal transmission lines are found, all passives are replaced by the elements in design kit to simulate close-to-reality performance. The substrate used is shown in Fig 4.8. It should be noted that final tuning will be done once the final design is ready.

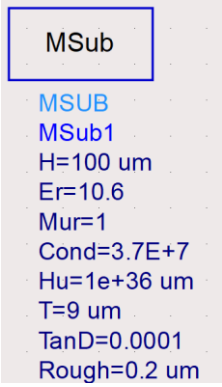


Figure 4.8. Transmission-line Substrate

Following the approach mentioned above, input matching networks for main and auxiliary PA and a common load matching network for the combined branches is designed. The networks are designed to work for wideband operation, 3.4 – 4.0 GHz. The input matching networks (Fig 4.9) of each branch are designed to transform the source impedance in Table 4.1 to 50 Ω at the input using LC networks. To avoid using any lossy inductors at high frequency, the inductors are relaced with transmission lines/stubs.

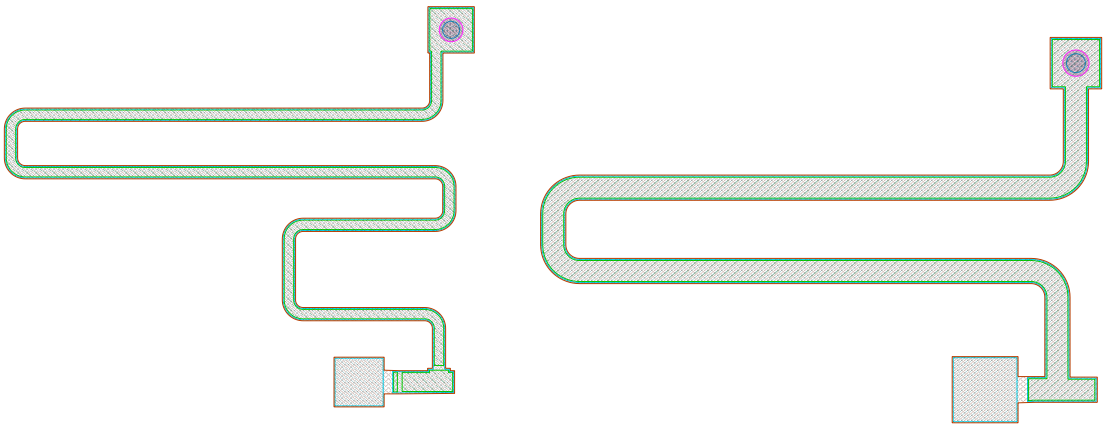


Figure 4.9. Input Matching Network for Main Amplifier (Left) And Peaking Amplifier (Right)

A common output matching network is designed to match the target load impedances in Table 4.1 to 50 Ω at the output. Fig 4.10 shows the resulting output matching network. As explained in section 2.3.2, both the branches in this configuration are directly connected. Hence, a common output matching after the joining point is designed and tuned to modulate the load in both branches. If a separate matching network

is used for the main transistor, this will affect the load modulation at the common joining point. Since we are using a current-biased transistor at the main branch, the FET sees an increased load impedance after the auxiliary PA turns on. If we use any frequency-dependent circuit elements in its output, the load that the main FET sees will vary with frequency and limit the bandwidth. Hence, defeating the purpose of a wideband design. Thus, both the branches should be connected with a common output matching network after the combining point. Although challenging, however if implemented successfully, this will not only make the architecture simpler and wideband but also will reduce the overall chip size.

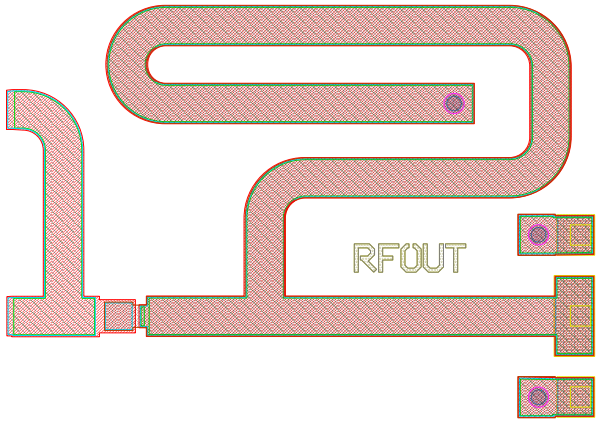


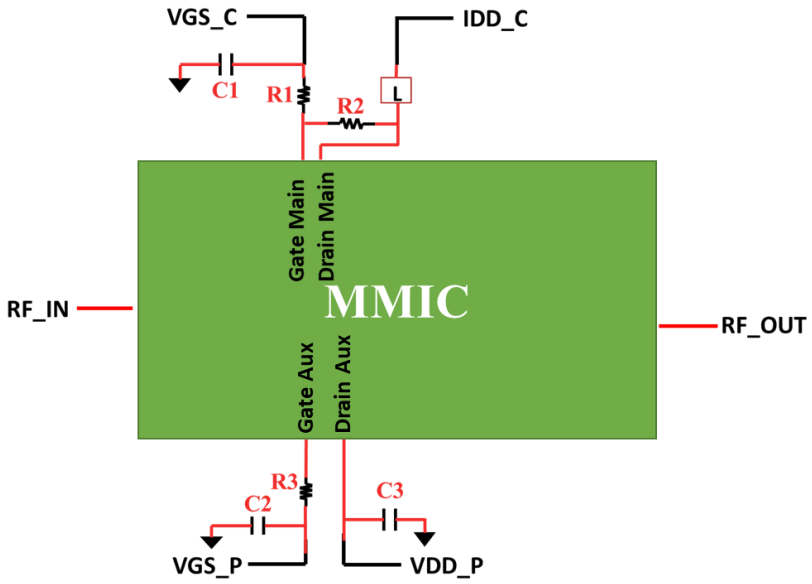
Figure 4.10. Output Matching Network at the Combined Output

4.6 Biasing Network

For the biasing circuit, at the drain of the transistor, a quarter wavelength line is used as an impedance inverter. This provides a good RF choke that prevents the RF signal leaking back into the DC path. Along with this, 20pF by-pass capacitor is used to absorb any stray RF leakage signal on the gate and drain. Along with the on-chip biasing circuit, off-chip circuits shown in Fig 4.11 are used to improve stability and an additional feedback circuit is needed for the current controlled carrier branch, as explained below.

In constant-current transistor, as the transistor dissipates power, it's temperature increases [4]. Due to rise in temperature, the drain bias voltage will increase and can increase to a very high level with the

rising temperature, leading to the breakdown of the transistor itself due to excessive heating. This is called thermal runaway. To avoid this, a voltage feedback circuit (R1 and R2) is added between the gate and drain of the transistor to control the drain voltage. As the drain voltage increases, the voltage adder/feedback circuit increases the gate voltage as well, limiting the voltage at drain and preventing thermal runaway.



Element	Value
C1	4.7 uF, 35 V
R1	600 Ω
R2	10k Ω
R3	400 Ω
C2	3.3 uF, 35 V
C3	10 uF, 100 V
L	560 uH

Figure 4.11. Off-chip feedback circuit on main PA to prevent thermal runaway and additional biasing network on both branches to improve DC RF isolation

4.7 Input Power Splitter and Output Combining network

This design is based on an asymmetrical architecture, i.e, the auxiliary device is larger than the main device. This is done intentionally to increase the back-off level for the DPA. A Wilkinson splitter (Fig 4.12) is used at the input which delivers uneven power to both branches [12]. The capacitors are DC blocks. Additionally, the overall input side of the PA is tuned, including the input splitter and IMNs for the two branches. This is greatly effective in reducing the chip size to less than 9 mm^2 for a compact design. For an MMIC, size of the chip is of great importance as it is directly proportional to the cost of production.

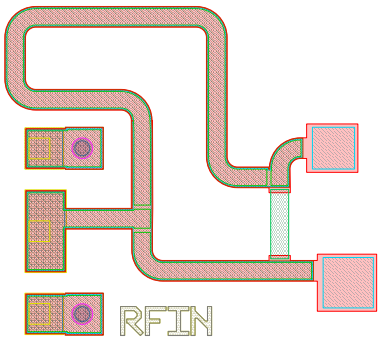


Figure 4.12. Input Power Splitter

At the output, for a RMDB PA, the main branch does not need an impedance transformer. As explained earlier, the maximum output power of a constant-current biased transistor increases by increasing the load impedance (upto a certain optimum impedance), which is exactly what happens organically. Therefore, the two branches are connected directly together using a short transmission line at the output of the main branch. The capacitors are DC blocks which are a part of the output matching network.

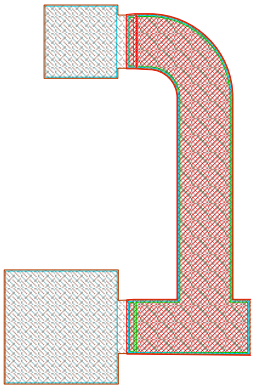


Figure 4.13. Output Power Combiner

Chapter 5. LAYOUT AND MEASUREMENTS OF RMDB PA MMIC

5.1 EM Simulation

After matching networks are designed, the length and width of the transmission lines and stubs were fine-tuned and optimized to provide the best performance results for efficiency, output power and gain. Fig 5.1 shows the schematic of the final amplifier. From left to right, the input signal is split into the two branches by a power splitter. Each branch has an input matching network that is designed to match the source impedance to 50Ω. Then a stability network is added to stabilize the transistor. Then both the branches are connected directly at the output, as explained previously, and a common output matching network is used for load modulation of both branches. DC/RF blocks and by-pass capacitors are used or DC-RF isolation. In this, the carrier FET is biased class B* by a constant-current source at the drain and the peaking FET is biased class C by a constant-voltage source. The overall circuit is later tuned to achieve best performance and reduce size.

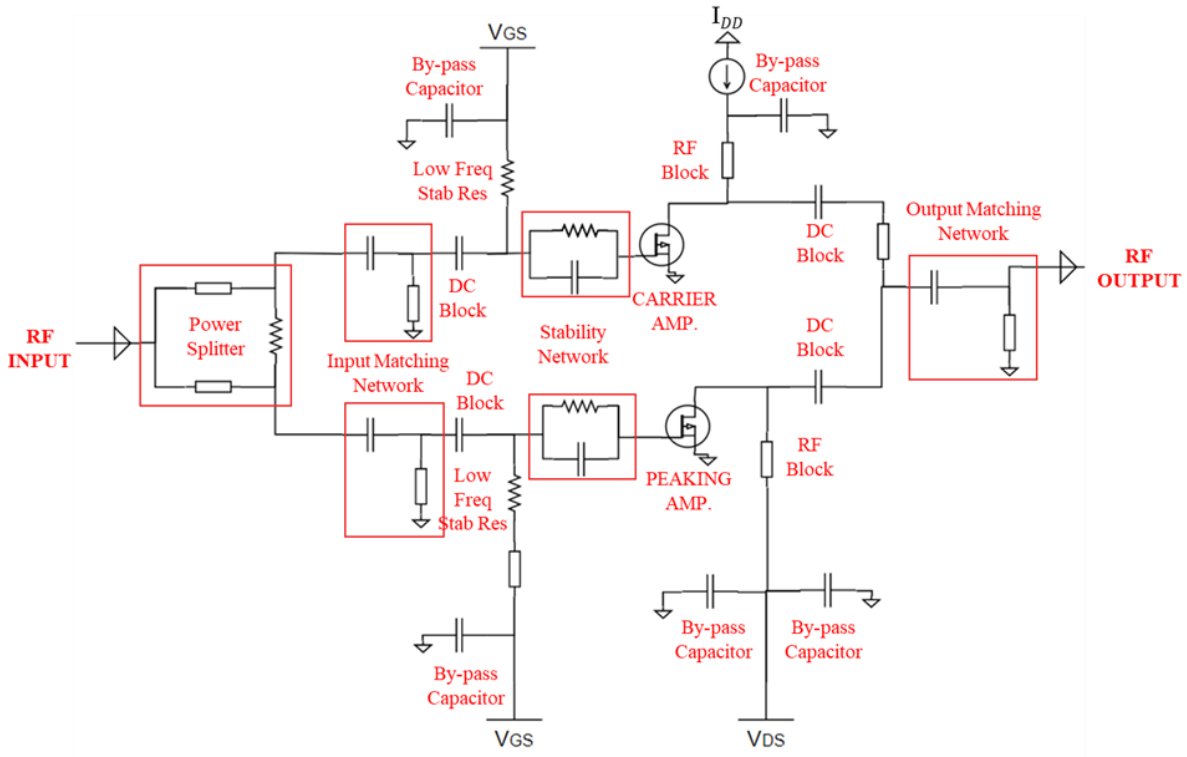


Figure 5.1. Circuit schematic of RMBB PA

All simulations were performed in ADS 2019. All the passive structures were EM-simulated in Keysight Momentum and the transistor cells were simulated using UMS 0.25um GaN HEMT non-linear FET model before sending the layout for fabrication. This is important because the ADS models of the passives do not take into account the coupling effects between the different adjacent elements. Therefore, for more accuracy and accurate design performance predictions, EM simulation is a necessity. The junction temperature of each transistor is calculated to be 50°C for the carrier and 70°C for peaking at room temperature.

One of the advantages of RMDB is the absence of bandwidth limiting quarter-wavelength impedance transformer in the output, making it easier to design broadband load-modulated PAs. With 5G standard having bands of up to 900 MHz in the sub 6 GHz frequency range, having broad band design is a challenge when choosing conventional Doherty PAs. Fig 5.2 shows the frequency response of the EM simulated RMDB PA at 11dB OPBO and at Psat. It is clear from the figure that the operational bandwidth of the simulated PA is 600 MHz from 3.4 – 4.0 GHz where the gain response is considerably flat (i.e., less than 1dB variation across band).

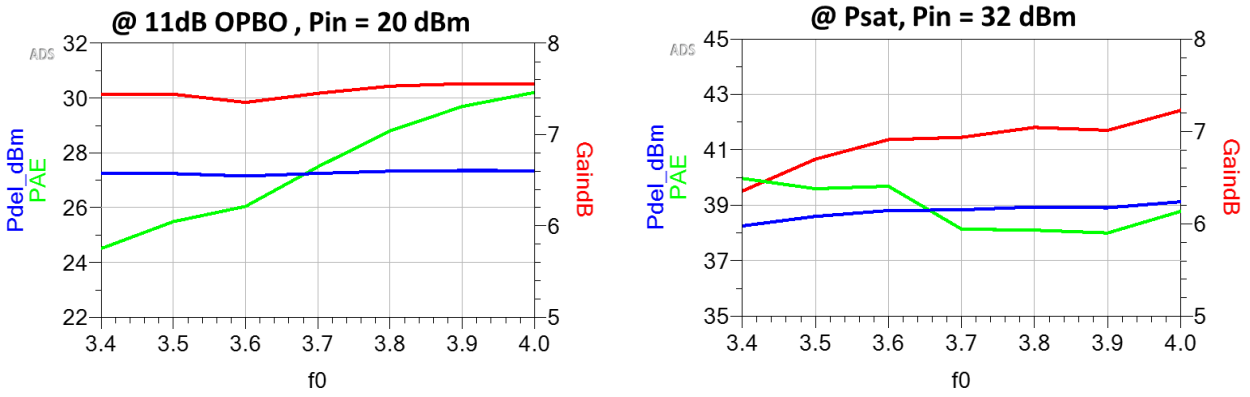


Figure 5.2. EM simulated frequency response of the RMDB PA (3.4-3.8 GHz)

Simulated efficiency and gain vs Pout plotted in Fig 5.3 clearly shows the distinct Doherty peaks, without using an impedance inverter, that the design intended to show with improved performance at back-off power levels. It is clear from the graph that the PA shows the expected load modulation, thereby

enhancing the efficiency significantly at 11 dB output power back-off. The chip size is 8.4mm^2 which is the smallest RMDB MMIC PA design, till date, to the best of author's knowledge.

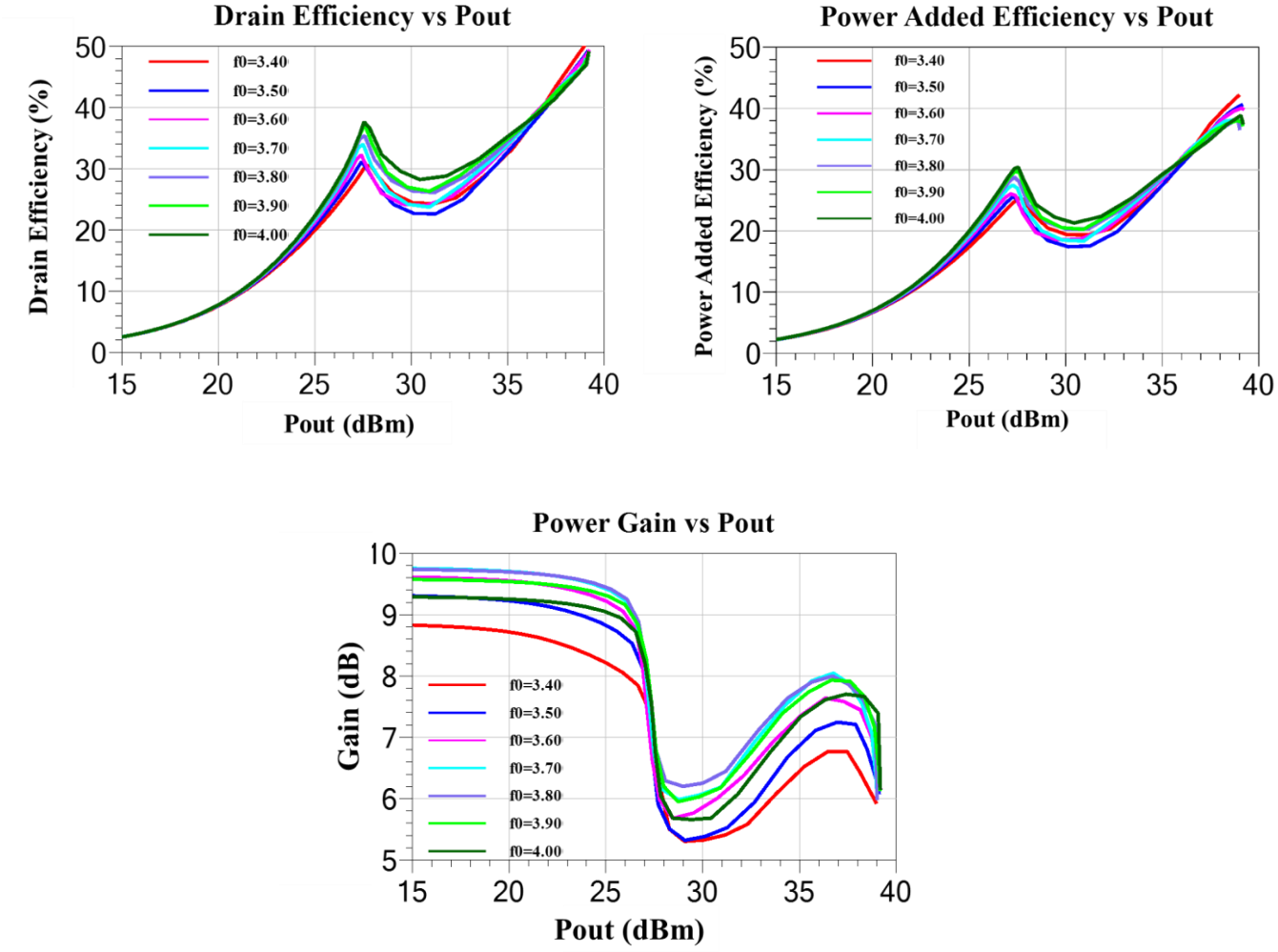


Figure 5.3. RMDB PA EM Simulated Performance with distinct Doherty Peaks (3.4 – 4.0 GHz)

The EM simulated results (Fig 5.3) of RMDB PA predict the frequency of operation of 3.4 – 4.0 GHz giving a wideband design of 600 MHz. This bandwidth shows small-signal gain of variation ±0.5 dB with the average of 9.5 dB. The drain efficiency at Psat (38dBm) is > 48 % and at 10dB OPBO is < 35 % across band. The PAE at Psat is > 38% and > 28% at back-off. The gain compression when the peaking PA starts to turn ON is approx. 4 dB, which is expected from a Doherty-like architecture at first efficiency peak

at BO and then a gain expansion of approx. 2 dB is seen when both PAs saturate. Finally, overall gain compresses after second efficiency peak.

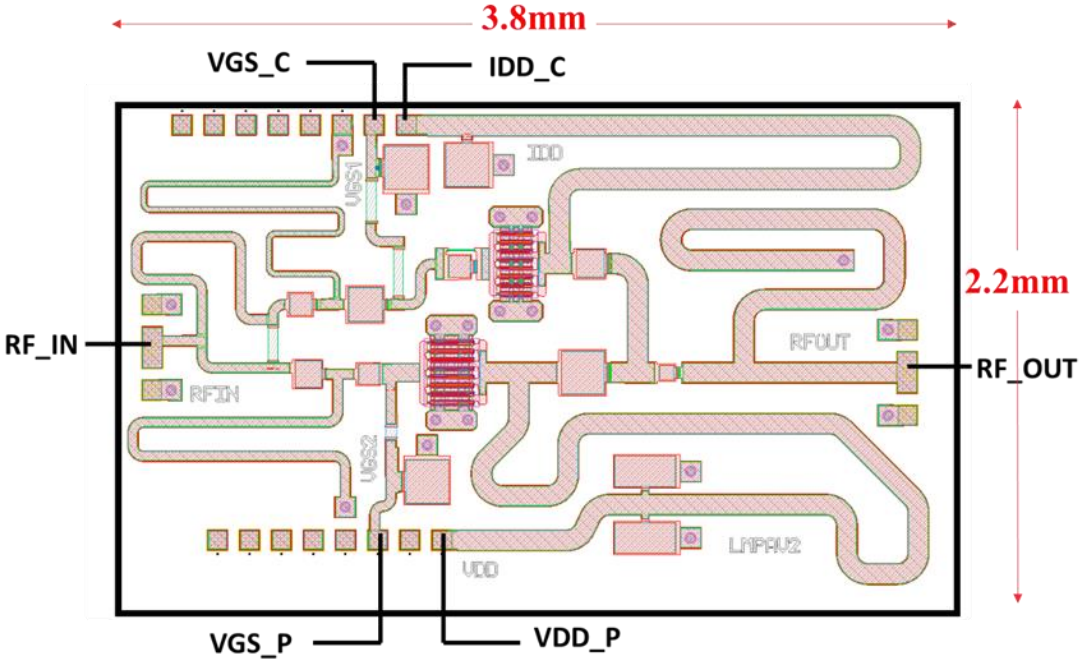


Figure 5.4. Layout of the RMDB PA

5.2 Experimental Analysis and Measurement Results

The fabricated MMIC photograph is shown in Fig 5.5 below with added off-chip biasing circuits. The MMIC dimensions were 3.8 x 2.2 mm. Off-chip DC adapting PCB boards were designed to provide the feedback network to the constant-current biased main transistor input in order to prevent thermal runaway as explained in detail in section 4.6. The additional resistors and capacitors added can be used to handle any low frequency instability and enhance RF-DC isolation using by-pass capacitors and RF choke inductor.

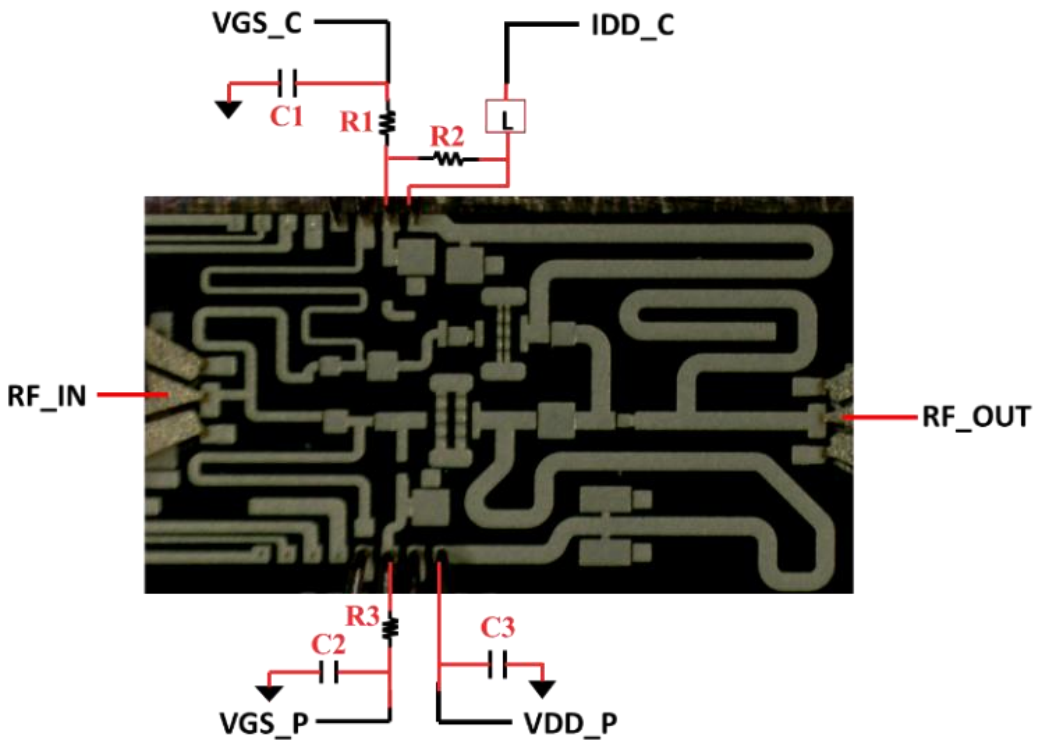


Figure 5.5. Photograph of the fabricated RMDB PA with added biasing networks

5.2.1 Non-coaxial measurements and TRL calibration

As explained in the section 3.1, fixture calibration is a method used to directly characterize the fixture. Rather than attaching a short and/or open at the DUT connection points as shown by the red dots on Fig 3.1, we perform a full calibration with a set of CAL standards. This moves the calibration plane directly to the DUT plane and allows us to calibrate out the fixture. Since we are actually measuring the fixture, fixture calibration is more accurate than any other methodology. A 2-port TRL Cascade Microtech Impedance Standard Substrate Calibration Kit is used for the PA MMIC measurements.

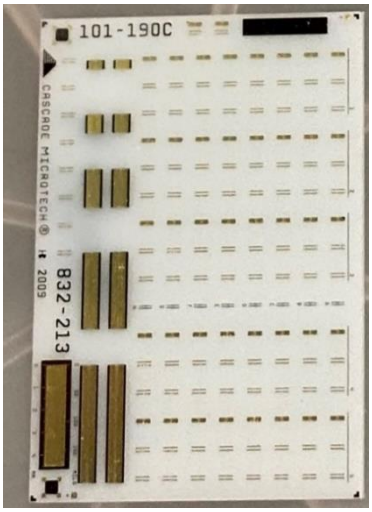


Figure 5.6. Cascade Microtech Impedance Standard Substrate Calibration Kit 101-190 C

These calibration standards are normally implemented in the form of so-called test coupons as shown in Fig. 5.6 which are specifically prepared sections of printed circuit boards. Typically, TRL calibration uses four or more coupons of various types. Making measurements with multiple coupons creates a system of equations that can be solved for so called error terms similar to how they are solved for coaxial DUTs and CAL standards. This methodology provides very accurate results if the coupons and DUT have similar characteristic impedances. The accuracy of this measurement also depends on the availability of quality calibration standards. Cascade Microtech WinCal software was used for calibration. Thru, short, open and load calibrations were performed.

5.2.2 CW Measurements

The purpose of this measurement is to feed a continuous-wave signal to the PA and check the stability and performance of the PA at specific power levels across the band. With these measurements we can see the S-parameters, Intermodulation (IMD) products, harmonics, and gain compression of the PA. The measurement setup is shown in Fig 5.7 in detail. Various path gains and losses are compensated for in all calculations. The CW signal is injected through the signal generator (SG) or vector network analyzer (VNA) into the driver amplifier. The driver is usually a high gain, linear class A/AB amplifier (to minimize

its contributions to distortions) that will drive the input signal to the required power level for the DUT. An isolator is used to prevent any back reflections into the VNA that may potentially damage the equipment. A coupler splits the input into two, one for the power meter that reads the input power and other goes to the RF input probe at the probe station. The DUT is placed at the probe station. DC input power supplies for the gate and drain bias of the transistor are connected to the DUT through the DC probes. The RF output probe receives the output power from the RMDB PA. and this goes to another coupler that splits it into a signal feeding the output power meter and another signal going to the spectrum analyzer (SA). The attenuator prevents a large signal from entering the SA and damaging it. We read the output power from the power meter and analyze the performance with the captured data.

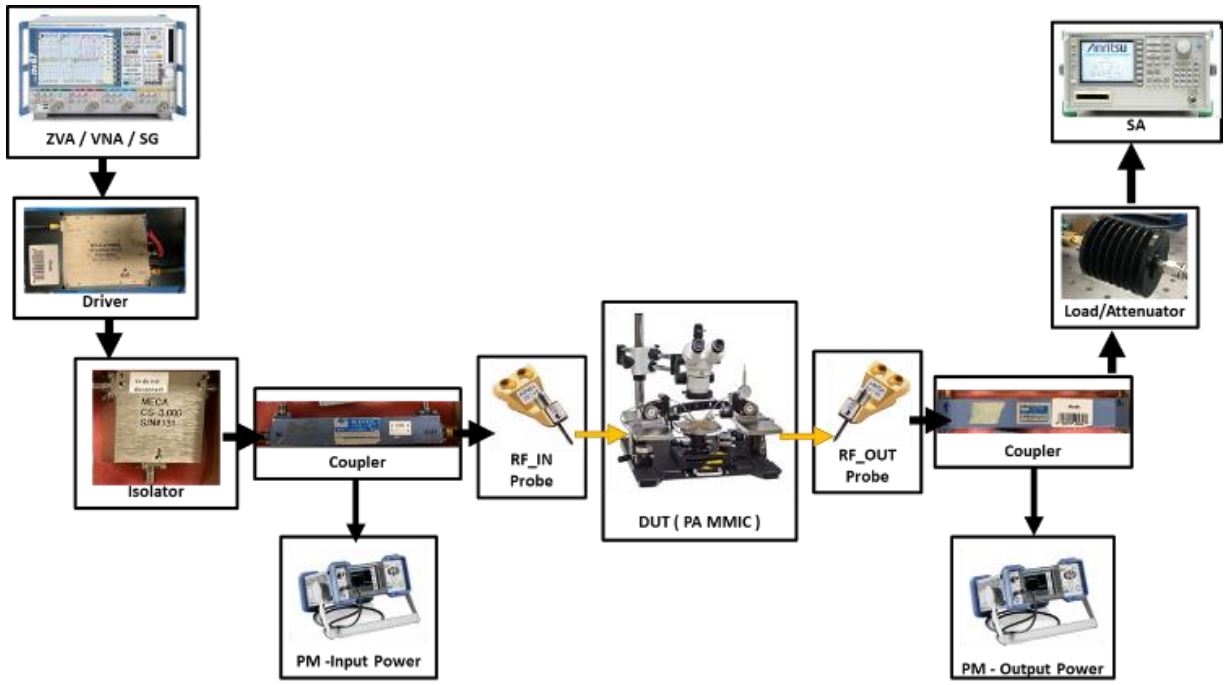


Figure 5.7. Continuous-Wave Measurement Setup

With the CW measurements, we can perform mathematical calculations to compute the efficiency and gain performance of the DUT using equations (2.1), (2.5), (2.6). Various losses and gains in the path were de-embedded in the calculations up to the DUT to obtain accurate results for the PA. The input and

output power read by the power meters and the DC voltage and current values on the power supplies are used in these calculations. The following results were obtained from the measurements:

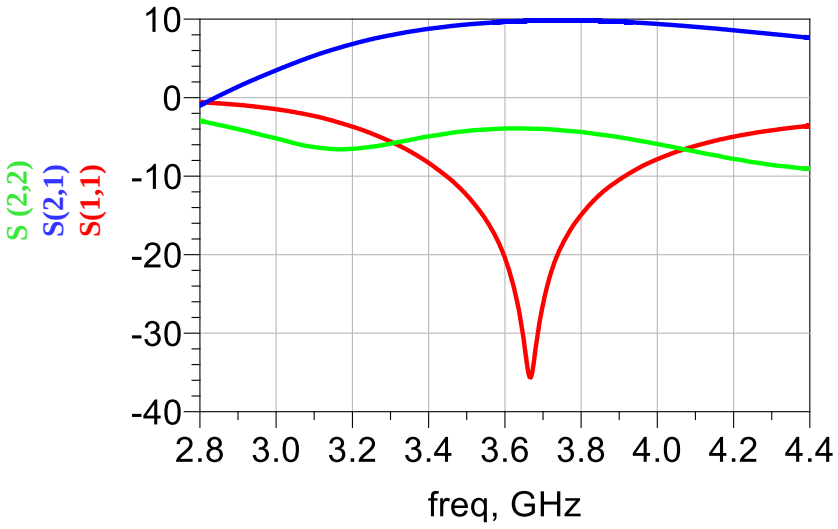
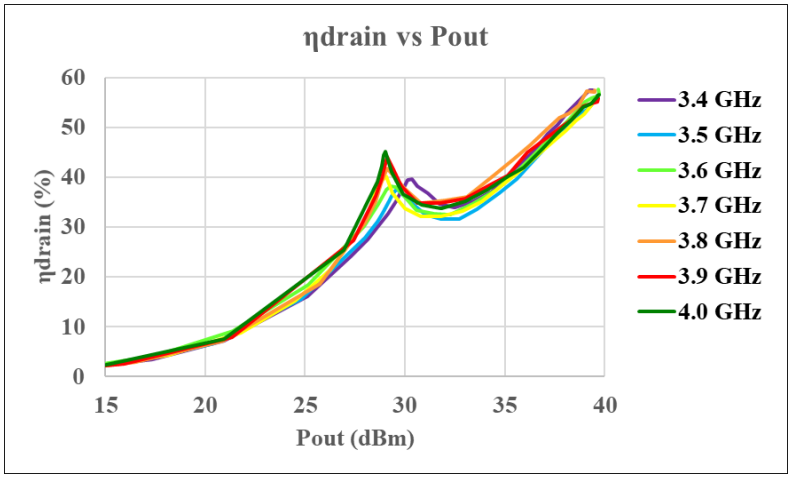
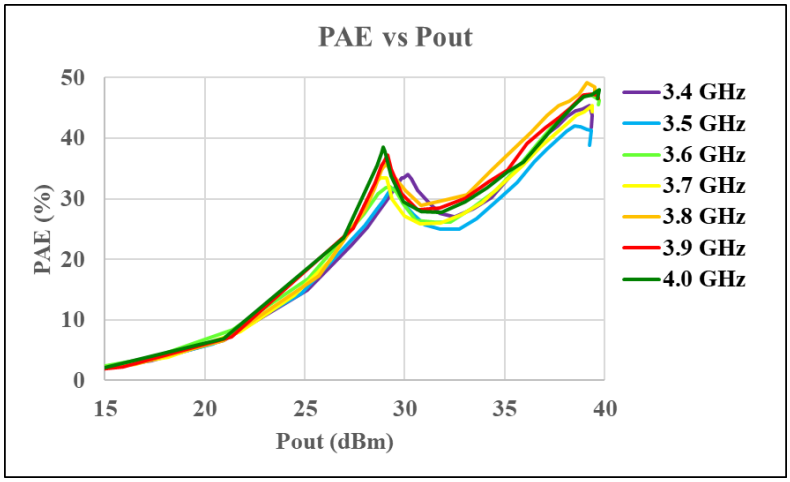


Figure 5.8. Measured S-Parameters Frequency Response

The measured small signal parameters (Fig 5.8) of the RMDB PA show lower than -10 dB input reflection coefficient (S11), a forward gain (S21) of 10 dB and output reflection (S22) better than 5 dB in the band of operation (3.4-4.0 GHz).

The CW measurements of RMDB PA reveal proper load modulation across the band as shown in Fig 5.9. The results are calculated using equations (2.1, 2.5, 2.6). The efficiency vs Pout curve shows a small-signal gain of 10.5 dB with ± 0.5 dB variation across band. The Psat of RMDB PA is greater than 39 dBm (~8W). Drain efficiency at Psat is between 52-57 %, whereas is between 38-46% at 9-10dB OPBO across band. As evident from the efficiency curves, load modulation was successfully implemented.





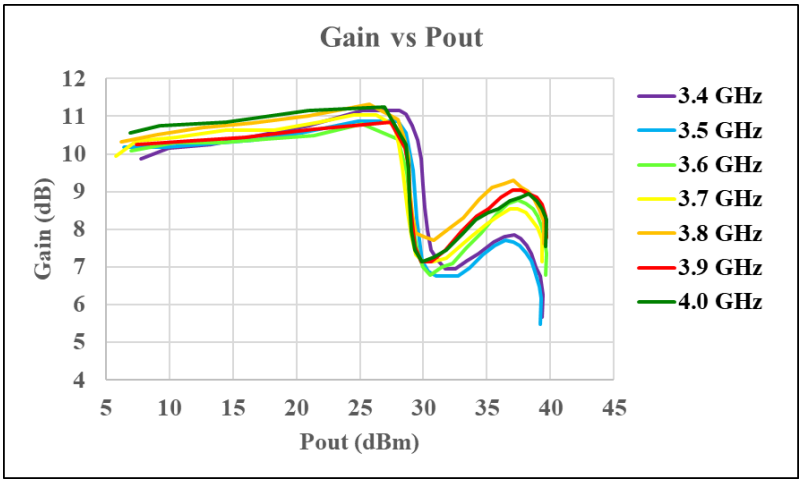


Figure 5.9. Measured Efficiency and Gain vs Pout across 3.4 – 4.0 GHz

This concludes the successful design implementation for this thesis which shows proper load modulation without the use of any quarter-wavelength impedance inverter at the carrier branch output. The CW measurement results discussed above are tabulated in Table 5.1.

Freq (GHz)	Small Signal Gain (dB)	Psat (dBm)	ηdrain @ Psat (%)	ηdrain @ 10dB OPBO (%)	Measurement Condition
3.4 – 4.0	10.5 (±0.5)	> 39	52.5 – 57.5	38 – 46	CW, 9-10 dB OPBO

Table 5.1. CW PA Performance Measurement Results

5.3 Comparison between simulation and experimental results

Table 5.2 gives a summary of comparison between the EM simulated performance and the CW measurement results of the RMDB PA.

	Freq (GHz)	Avg. Small Signal Gain (dB)	Psat (dBm)	Avg. ηdrain @ Psat (%)	Avg. ηdrain @ backoff (%)	Avg. PAE @ Psat (%)	Avg. PAE @ backoff (%)	Measurement Condition
EM	3.4 – 3.9	9.5 (±0.5)	> 38	48	35	38	28	ADS Momentum
CW	3.4 – 4.0	10.5 (±0.5)	> 39	56	44	45	35	CW, 9-10 dB OPBO

Table 5.2. Comparison between Simulation and Measurement Results

As evident in the comparison, measured results for the RMDB PA design are better than EM simulated predictions, by 8-9 % efficiency, however one may expect the opposite. This is due to the inaccuracies in the FET model for constant-current biased case. Usually, the non-linear models are optimized to work for voltage biased drain and due to this, in current biased scheme, the simulations will not be as accurate leading to discrepancy in the simulated and actual measured results. Also, experimental measurements are based on real time systems and are prone to errors effected by external disturbances, instruments interferences,

thermal effects, software used etc. These errors might be positive or negative, nevertheless are out of the designer's control, especially in MMIC designs since the chip cannot be tweaked for compensations once fabricated. However, it is safe to say that measurement results are more reliable to gauge circuit performance since they are based on actual physical hardware.

Finally, Table 5.3 is a comparison to the previous works done on RMDB PA. In [4], the concept of current biased PAs was first introduced, however the proof-of-concept design for a dual branch PA with discrete CREE GaN FETs showed a wideband operation from 0.8-2.2 GHz with gain variation of 4 dB across band but was implemented on PCB-level design. In [7], an RMDB PA MMIC using 0.25um UMS GaN FETs, although wideband design from 2.6-3.8 GHz with a gain variation of 2dB across band but produced a partially integrated circuit with an off-chip external input network to control back-off level.

This thesis presents the first fully integrated RMDB PA MMIC with a gain variation of only 1 dB across 3.4 - 4.0 GHz frequency band. To the best of author's knowledge, this work by far, is the most compact, first fully integrated RMDB PA till date.

	Implementation Process / Transistor	**Freq (GHz)**	**Small Signal Gain (dB)**	**Psat (dBm)**	**ηdrain @ OPBO to Psat (%)**	**Measurement Conditions**	**Chip size**
[4]	PCB Cree GaN	0.8 – 2.2	10.5 - 14.2	39.7 – 40.7	36 - 60	CW, 9dB OPBO	Not comparable
[7]	MMIC UMS 0.25 GaN	2.6 – 3.8	10.2 – 12.5	36.8 – 37.2	37 - 70	CW, 9dB OPBO	9.75 mm^2 Partially integrated
This work	**MMIC UMS 0.25 GaN**	**3.4 – 4.0**	**10 - 11**	**39 – 39.5**	**44 - 56**	**CW, 9-10 dB OPBO**	**8.4 mm^2 Fully integrated**

Table 5.3 Comparison between previous works on RMDB PA

Chapter 6. CONCLUSION

6.1 Summary of the thesis work and contributions

5G is implemented in two distinct frequency ranges, sub-6GHz region FR-1 and mm-wave region FR-2. Although the future technology will be driven by fast mm-wave amplification, however, sub-6GHz spectrum will facilitate easy transition from 4G/LTE to 5G. While there is immense research going on that targets the current deployment issues in mm-wave wireless components, it becomes equally important for continued research in sub-6 GHz domain. The sub-6 GHz 5G deployment extensively employs high peak-to-average power ratio (PAPR) waveforms and poses demanding TXs/PAs requirements, including linearity, peak efficiency, power back-off (PBO) efficiency, and capability of supporting multi-Gb/s modulation. One of the most well research, tried-and-tested design technique to achieve this is Doherty architecture in PAs.

In this thesis, an unconventional architecture, Reverse load-modulated Dual Branch PA (RMDB PA) is discussed, which proposed a constant-current drain bias of the carrier amplifier in the conventional Doherty architecture. This led to a new set of properties exhibited by the transistor which opens a door to new designs schemes. One of the major benefits of this new biasing scheme is called Reserved Load Modulation, which means that the maximum output power of the transistor increases by increasing the load impedance (up to a certain optimum impedance), which is the opposite case of conventional constant-voltage biased transistors.

Utilizing this property of a constant current biased transistor, the need for an impedance inverter in the carrier branch is eliminated as the impedance variation at the junction point is exactly what is desired for this architecture i.e., the carrier amplifier should have a smaller load impedance at the backoff point and the load impedance should increase until the saturation point. The impedance inverter used in conventional Doherty is a major contributor towards circuit bandwidth limitation. Additionally, the two branches are

connected directly in this architecture, with a common output matching network after the common connection point. This reduces the circuit size tremendously which works best for an MMIC design.

A detailed step-by-step methodology of designing the power amplifier MMIC is presented in this thesis, which can also be helpful to fellow researchers stepping foot in the exciting world of PA design. The RMDB PA design uses 0.25um GaN HEMT MMIC process from United Monolithic Semiconductor (UMS). The first fully integrated RMDB PA MMIC provides a small signal gain of 10.5 dB (±0.5dB) across 3.4 to 4.0 GHz band and delivers an output power of greater than 39 dBm at saturation with drain efficiency of greater than 52 % while maintaining greater than 38 % at 9-10dB back-off under CW signal across band. The designed RMDB PA is suited for sub-6 GHz wireless applications.

6.2 Future work

The research activities performed during the thesis has led to multiple topics worth exploring for future. First, an immediate continuation of this work would be to perform advanced waveform engineering and tune the harmonics of the circuit to reveal much higher efficiency. This can be done by doing a harmonic load pull and modifying the matching networks to control the harmonics.

Second, linearity of the PA can be assessed, and an improvement strategy can be carried out. Linearity of any PA is of high importance as well to help prevent distortion in the signals. The PA can be measured with an APD or a DPD to improve linearity as well.

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