THE UNIVERSITY OF CALGARY

DESIGN CONSIDERATIONS FOR BIPOLAR POWER TRANSISTOR SWITCHING CIRCUITS

by

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A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE

DEGREE OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL ENGINEERING

CALGARY, ALBERTA

JUNE, 1990

ISBN 0-315-61945-7

THE UNIVERSITY OF CALGARY

FACULTY OF GRADUATE STUDIES

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled "Design Considerations for Bipolar Power Transistor Switching Circuits" submitted by Dale Tardiff in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

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ABSTRACT

There are a variety of switching power supplies, converters, and power conditioners available today. With improvements in power semiconductor devices, it is possible to improve the efficiency and power handling capability of the various kinds of equipment. Bipolar power transistors offer the advantages of fast and easy switching as well as respectable power ratings. This thesis examines the requirements for the application of bipolar power transistors to switching converters. For a specific application, the base drive and snubber circuits considered in this thesis were intended for use in a three phase, pulse width modulated voltage source inverter. Therefore, the circuits were designed to meet typical parameters for a 20 kW inverter. The thesis presents the design considerations for the base drive and snubber circuits, as well as a review of some of the available circuits. The design of a base drive and snubber circuit is presented to demonstrate the design methodology developed for these circuits. Experimental results are also presented on the circuits that were built.

ACKNOWLEDGEMENTS

Completing this thesis would have been impossible without the assistance of several people. First and foremost, I must thank Dr. T. H. Barton for his support, advice and encouragement throughout the course of my research, as this was essential to me in completing this thesis. Dr. Barton also proofread much of this thesis and made recommendations which helped me to better organize my thoughts and put them in writing. His contributions to the financial support of this project from his research grants was also greatly appreciated.

Several technicians in the department of Electrical Engineering were also helpful. Ed Evanik constructed the base drive cards as well as the controller for the inverter. He also gave me many useful tips on techniques of noise elimination and electronic circuit design. Pat Walsh assisted me with his knowledge of power equipment in general and specifically the various power supplies available in the department. He was also very knowledgeable in regards to electrical measurements in power circuits, especially with respect to the measurement of large voltage and current.

Two colleagues of mine, Corey Mack and Paul Martin, assisted me by proofreading my thesis and making suggestions towards its improvement. Finally, I would like to thank the Department of Electrical Engineering for its financial support during the time spent researching this thesis.

To my Parents

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Nomenclature

α common base transistor gain
β common emitter transistor gain
γ emitter injection efficiency
ω resonant frequency of snubber during reset
ω_s resonant frequency of snubber discharge path
b_t base transport factor
C base drive capacitor
C_o resonant transfer capacitor
C_s snubber capacitor
D_o resonant output diode
D_r resonant transfer diode
D_s snubber diode
h_{fe} DC current gain of a transistor
I, I_{load} load current
I_b base current
I_c collector current
I_e emitter current
I_{bm} maximum base current
I_{cm} maximum collector current
i_{co} current in capacitor C_o
i_{cs} current to capacitor C_s
i_o snubber current fed back to power supply
i_r snubber reset current
I_{rr} diode reverse recovery current
i_s snubber charging current
L base drive inductor
L_r resonant inductor
L_s snubber inductor
M avalance multiplication factor
P_{cond} transistor conduction losses
P_d total power dissipated in transistor
P_{ds} dynamic saturation power loss
P_{off} turn-off power loss
P_{on} turn-on power loss
P_r power dissipation in snubber resistor
P_T transistor power dissipation
Q_{rr} reverse recovery charge in diode
$R_{\theta cs}$ thermal resistance, case to sink
$R_{\theta jc}$ thermal resistance, junction to case
$R_{\theta sa}$ thermal resistance, sink to ambient
R_b base drive turn-on resistor

r_{ds} MOSFET drain-source conduction resistance
R_g base drive turn-off resistor
R_r snubber reset resistor
R_s snubber resistor
t_{cf} turn-off crossover time
t_d turn-on delay time
t_{ds} dynamic saturation interval
t_f transistor fall time
t_{on} transistor turn-on time
t_r rise time
t_{rr} diode reverse recovery time
t_{rs} snubber reset time
t_s transistor storage time
T_a ambient temperature
T_c transistor case temperature
T_j transistor junction temperature
V_{be} transistor base-emitter voltage
$V_{be(sat)}$ base-emitter saturation voltage
$V_{(br)cbo}$ collector-base breakdown voltage, emitter open
$V_{(br)ceo}$ collector-emitter breakdown voltage, base-emitter open
$V_{(br)cer}$ c-e breakdown voltage, resistance from base to emitter
$V_{(br)ces}$ c-e breakdown voltage, $V_{be} = 0$
$V_{(br)cev}$ c-e breakdown voltage, base-emitter reverse biased
V_{cbo} collector-base maximum voltage (punchthrough voltage)
V_{ce} collector-emitter voltage
$V_{ce(sat)}$ collector-emitter saturation voltage
$V_{ceo(sus)}$ collector-emitter sustaining voltage, base-emitter circuit open
V_{cev} maximum V_{ce}, with base-emitter reverse biased
$V_{cev(sus)}$ collector-emitter sustaining voltage
V_{cs} voltage on capacitor C_s
V_{co} voltage on capacitor C_o
V_{dc}, V_s DC supply voltage
V_{ebo} maximum reverse base-emitter voltage
V_p base drive positive supply voltage
W stored energy
Z impedance of snubber during reset
Z_s impedance of snubber during discharge

CHAPTER 1

INTRODUCTION

1.1. Power Semiconductor Devices

There are many applications where power conversion or conditioning is required. This could be in rectifiers, variable speed drives, or power line filters. All of these applications require power semiconductor devices to perform their required functions. In many applications, it is necessary to switch a large amount of power electronically. There are several devices available to do this.

The selection of proper electronic switching devices is important in the design of power electronic equipment. The proper devices are necessary to meet the desired specifications. The devices must be capable of handling the rated power, withstanding the required voltage, and conducting the rated load current. As well, it is important for the devices to be able to switch at the required frequency. They also must be easy to use and be reasonably priced.

For power electronic switching applications, several devices are available. These are silicon controlled rectifiers(SCRs), also known as thyristors, bipolar transistors and power MOSFETs. Thyristors used in inverter applications require a commutation circuit to turn them off. This commutation circuit can increase the switching time by a factor of four, thus reducing the performance of the circuit. Gate turnoff thyristors(GTOs) do not require any special commutation circuits but

are slow. These two devices are used primarily in very high power applications for which other devices are not available. Power MOSFETs have the fastest switching times, and are simple to apply, requiring a smaller amount of additional circuitry. However, these devices tend to be expensive and can handle only lower power levels. Power bipolar transistors can handle more power and are less expensive than MOSFETs[1, 2]. However, the gain is poor for high voltage devices, making base drive design difficult. By using a Darlington configuration, this problem is alleviated at the expense of increased switching time. As well, single bipolar transistors can be quite expensive at high current levels[3]. BIMOS Darlingtons, in which a bipolar transistor is driven by a MOSFET, are becoming quite popular as they combine some of the best features of both devices[4, 5]. Bipolar Darlington configurations usually are the least expensive devices. This thesis explores the design considerations for bipolar power transistors used as switching devices in a typical power conversion circuit.

1.2. Typical Application: Inverter for a Variable Speed Drive

In many industrial applications, a variable speed drive is essential for performing a variety of functions. In the past, most variable speed drives were developed with DC motors. This is because the top speed of an AC motor is determined by the frequency of the supplied power and until recently this frequency was fixed. This problem has now been overcome by improved power semiconductor devices permitting the construction of inverters capable of producing variable frequency three phase ac power at the necessary power levels. This has

made it possible to utilize reliable and inexpensive induction motors in variable speed applications[6].

An inverter is an electronic device that converts DC power to AC power. It achieves this using electronics to switch between the positive and negative DC supply rails. The resulting output is a square wave of the desired frequency. Since the speed of an AC motor is proportional to the frequency of supplied power, the speed is controlled by varying the inverter frequency[6, 7].

Instead of providing a symmetrical square wave output, the square pulse may be switched on and off many times, producing a string of pulses of varying width in place of the continuous voltage of one half cycle of a square wave. When this voltage is applied to a motor the resulting current is close to sinusoidal. This is the Pulse Width Modulation(PWM) technique for motor control. Using PWM reduces harmonics at lower frequencies, which helps reduce torque oscillations and harmonic heating in motors. Without PWM, an inverter is not efficient since the harmonics of a low frequency square wave have a detrimental effect on motor performance[6].

The width of the pulses is determined by a controller which modulates a fixed frequency carrier wave with a sinusoidal reference signal of the desired frequency and amplitude. In this control method, the frequency and voltage supplied to the motor can be varied. When the pulses are longer, the RMS voltage is higher; when the pulses are shorter, the RMS voltage is lower.

This inverter is intended for use in driving a 10 hp induction motor. This will require that the inverter can provide power of 20 kW. This power output insures that the motor can be overdriven, and as well, it also allows for power losses in the motor. For PWM applications, the inverter will be required to run at ten times the desired output frequency, at least. For operation at 120 Hz, this would be 1200 Hz. Also, the pulses should be narrower than this by a factor of ten or greater, so for 1200 Hz PWM operation, a minimum pulse width of 75 μs is desirable. In the next section the transistor ratings will be determined based on the specifications of the inverter.

1.3. Selection of Power Transistors

The switching devices used in the inverter must meet several parameters to operate within specifications. For example, the transistors must be able to withstand the DC input voltage of the inverter. If this voltage is provided by rectifying three phase AC, its value is given by

$$V_{dc} = 3\sqrt{2}\,V_l / \pi \qquad (1.1)$$

where V_l is the line to line voltage of the AC source. If a conventional 120/208V ac source is used, V_{dc} = 281V. To provide a 2:1 margin of safety, transistors rated for 600V are required. The current requirement can also be calculated. For example if the inverter is to provide power up to 20 kW, the full load current is

$$I = 20\,kW / (\sqrt{6}\,V_{dc}) \qquad (1.2)$$

or 29.6A. Therefore transistors rated for 60 A are needed to give a 2:1 margin of safety. Finally, the transistors should have a fast switching speed, so that narrow

pulses in PWM can be produced. Most PWM applications require switching capability in the order of 10 - 20 kHz. The example above mentioned 12 kHz. This requires transistors with a total switching time of 50 μs or less. In this case 25 μs provides the required 2:1 margin of safety.

For this project, Powerex KS224510 Darlington power transistors were used. These devices are two bipolar power transistors connected in a Darlington pair arrangement. The devices are rated to handle a collector current of 100 Amperes and withstand a collector-emitter voltage of 600 Volts when the device is fully off. The Darlington pair provides a current gain of up to 100[8]. This matches the desired specifications from the previous section. The transistors are also capable of switching within 15 μs, which permits the desired minimum pulse width to be obtained. Careful design of the base drive can improve the switching time.

1.4. Major Design Considerations

Two major design problems must be solved in the application of bipolar power transistors. This thesis is concerned with these design considerations. The first consideration is protection of the transistor. The device ratings must not be exceeded and it should operate within its Safe Operating Areas (SOA). [3, 9, 10] This specification is described in chapter 2. This requires the design of a snubber circuit which reduces switching transients in the transistor circuit and keeps it within its Safe Operating Areas. This problem becomes crucial when operating with inductive loads (like motors) because large voltage and current transients

occur. The snubber circuit suppresses these transients so that device ratings are not exceeded. Chapter 4 describes several snubber circuits[11, 12, 13, 14, 15, 16, 17, 18, 19, 20]. This comprehensive literature on snubbers was reviewed, and is summarized in Chapter 4. Experimental results from some of these are presented and the snubber most suitable for these transistors was optimized. As well, the design criteria that was developed as a result of the research for this thesis is also presented in Chapter 4. Chapter 4 also discusses thermal protection of transistors.

The other design consideration is the base drive of the transistor. The correct bias voltage and base current must be provided. In chapter 3, the ideal base drive current pulse is described, and various drive methods to obtain this are compared[3, 5, 21, 22, 23, 24, 25]. Proper design of the base drive provides an optimum transistor switching time and helps keep the device within its Safe Operating Areas. By using the Darlington configuration with its high current gain, it is possible to keep base drive power low, since only moderate base current is required. A base drive suitable for these Darlington transistors was selected. Some design guidelines were developed and are presented in Chapter 3. The results of experimentation and optimization of the drives is also given in Chapter 3.

In order to properly understand the base drive and protection requirements of a power transistor, it is necessary to understand the fundamental physics of the device. Chapter 2 describes the fundamental physics of bipolar power transistors, and contrasts the construction of these devices with conventional low power devices.

As a result of the research for this thesis, several contributions have been made in the areas of base drive and snubber design for bipolar power transistors. First, a set of guidelines for the selection of base drive components is listed in Chapter 3. The various recommended techniques for base drive of power Darlington transistor modules were examined experimentally and are evaluated in Chapter 3. Finally, the base drive circuit that was used has been optimized and this is also summarized in Chapter 3. For the design of a snubber circuit, it was found that there is a large amount of literature available on lossless snubber circuits. This was reviewed and is summarized in Chapter 4. The design criteria for one suitable snubber is presented in Chapter 4. With the experimental results, some guidelines for snubber optimization are also given in Chapter 4. Finally, a single phase inverter was constructed to observe the operation of the base drive and snubber circuits that are described in this thesis. This is a typical application of the devices used. The results of this are given in Chapter 5.

CHAPTER 2

BIPOLAR POWER TRANSISTOR SWITCHING DEVICES

2.1. Introduction

To use a bipolar junction transistor (BJT) as a power switching device, it is necessary to understand the physical operation of the transistor. As well, the static and dynamic operation of the transistor as an electronic switching device is discussed. It is assumed that the reader understands fundamental semiconductor physics.

The construction of a bipolar power transistor has several differences from that of low power devices. These differences are necessary to enable the device to operate at high power levels. Knowing about these differences and their effects is important in properly selecting and utilizing power transistors. This chapter discusses the construction and basic physics of operation of a power BJT, and makes some comparisons with standard low power transistors.

In most cases, the charge control model for semiconductors is sufficient to explain device operation. This model is used because it is simple and straightforward. It uses the distribution of charge in the device as well as its rate of change to explain device behavior. The curves given in this chapter are general curves that do not apply to a particular device.

2.2. Bipolar Power Transistor Structure

All bipolar junction transistors (BJT) have the same basic structure. This consists of a layer of doped semiconductor material sandwiched between two layers of oppositely doped material. If the transistor consists of two layers of n-type material and a layer of p-type in between, it is called an NPN transistor. A PNP transistor consists of two P and one N type layer. Most power transistors are NPN since electron majority carriers are more efficient for conducting large currents. Only NPN devices are discussed in the remainder of this chapter.

In some cases, a layer may be composed of one or more sublayers each with slightly different doping levels. This construction helps to enhance certain properties of the device. In the case of a bipolar power transistor, the collector region often consists of two regions, a lightly doped region near the base, known as the ν region, and the more heavily doped n^+ region, near the collector contact. The ν region greatly increases the ability of the transistor to sustain high voltages, at the expense of a higher forward voltage drop. This additional region is not encountered in a low power transistor.

By changing the thickness of each layer of a transistor, as well as the concentration of charge carriers in the layer, the properties of the transistor can be altered. It is important to understand how this affects the gain of a transistor, its switching time, and its breakdown voltage capability. All these parameters are important for a transistor used as a switching device.

The thickness and doping level of the base and collector regions also affect the switching time of the transistor, most notably the storage time, which is the longest component of switching time. When designing or selecting a transistor, it is important to note that tradeoffs must be made between gain, voltage sustaining capability and switching speed. Improving one often reduces one or more of the other properties. Since a general purpose transistor does not support large voltage or current, these tradeoffs are not necessary for low power devices. In section 2.3 of this chapter, the effects of transistor construction on the various parameters are described.

Even though the transistor is described as having a sandwich like structure, this is seldom the practice in a modern power transistor. Instead, what is known as an interdigitated emitter structure is used. In an interdigitated emitter the emitter is separated into many long, thin strips instead of being a single unit. As well, the base and emitter metallization is alternated on the surface of the transistor. This keeps regions under the base contact in close proximity to the emitter. Regions under the base contact are called near base. Regions between the base and emitter contacts are called peripheral base, and those underneath the emitter are remote base. In an interdigitated emitter structure, the distances from the base contact to the remote base is reduced. In section 2.3 of this chapter the advantages of this structure are described.

2.3. Operation of the Power BJT

2.3.1. Static Characteristics

A BJT operates in one of several states. These are shown in figure 2.01. In the linear region, the collector base junction is reverse biased, and the emitter-base junction is forward biased. In this state I_c is directly proportional to I_b. The transistor is operated as an amplifier. In the cut-off region, both transistor junctions are reverse biased, and as a result almost no collector current flows. In the saturation region, both junctions are forward biased. The current gain and V_{ce} are at a minimum. However, the effective base covers the entire collector region, and as a result turnoff is slow. In the quasi-saturation region, I_b is held to the minimum value needed to turn the transistor fully on, $I_b = I_c / \beta$. This gives an increased value of V_{ce}, but reduces the storage time[10, 9, 1]. In chapter 3 a

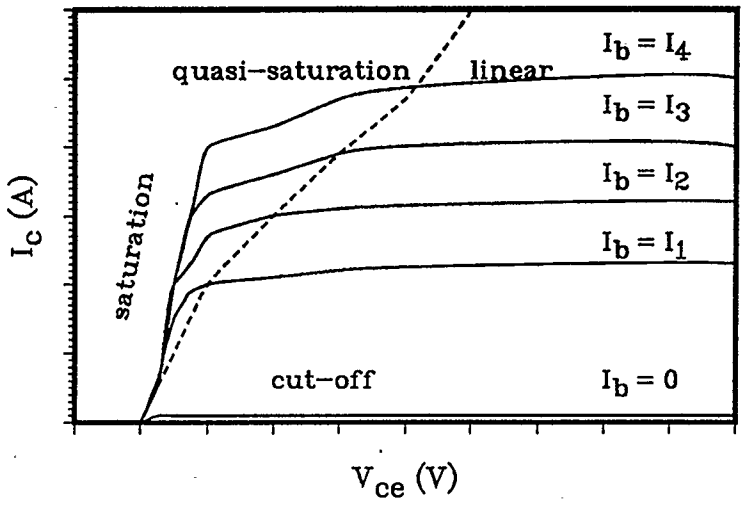


Figure 2.01. Output Characteristics of a Power BJT

circuit called a Baker clamp is discussed which forces the transistor to operate in this region. Power transistors are rarely operated in the linear region. They are either on (saturated or quasi-saturated) or are off.

2.3.2. Transistor Switching Characteristics

Since power transistors are operated as switching devices, their switching characteristics are important. The device must have the appropriate power handling capabilities as well as a fast switching time. By operating in the quasi-saturation region, it is possible to reduce the storage time of the device, but $V_{ce(on)}$ and power loss is increased. These effects are the result of fewer charge carriers in the base of the transistor during quasi-saturation. The designer must determine if the increased power dissipation as a result of this is excessive. If not, then operation in the quasi-saturated mode is recommended.

Several stages of a transistor's switching cycle may be identified[26]. Figure 2.02 shows typical turn on waveforms for a power BJT. The turn-on time, t_{on}, is comprised of two components, t_r and t_d. Turn on delay time, t_d, is the time required to feed enough charge into the base to forward bias the base emitter junction. This time period is usually very small. Collector current rise time, t_r, is the time required for I_c to increase to 90% of its steady state value. The rate of rise of collector current is limited by di_B/dt, the rate at which charge is applied to the base; as well as the effects of the external circuit and current gain. This is the longest portion of the turn on interval. Rectifier recovery current is a surge of

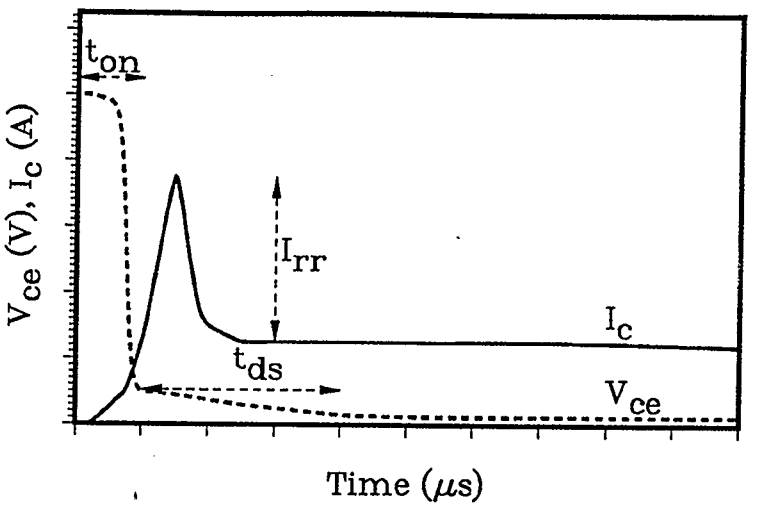


Figure 2.02. Bipolar power transistor turn-on.

current from external components, such as capacitors and fast recovery diodes, that will occur when the transistor is turned on. It should be minimized to prevent excess power loss during turn on. As the base and collector regions of the transistor become charged, the resistance of the base is reduced and the collector voltage begins to fall. By supplying excess base current above that needed for saturation, it is possible to increase the rate of voltage fall. The interdigitated emitter structure becomes important in this situation. By reducing the distance from the base contact to the remote base regions it is possible to get charge into the more remote regions of the base (those below the emitter), and this reduces the turn on time.

Another problem that increases the on-state transistor losses is collector voltage tail-in, or dynamic saturation, which is caused by a phenomenon known as conductivity modulation. The time duration measured from when

V_{ce} = 10 % $V_{ce\ peak}$ until V_{ce} = 110 % $V_{ce(sat)}$ is known as the dynamic saturation interval, t_{ds}. When a transistor is experiencing dynamic saturation it is operating in the quasi-saturation region. In this situation, the base-collector junction is forward biased and charge carriers have entered the collector. Due to the fact that the ν–region of a power transistor is lightly doped, this charge partially overcomes the background doping of the ν-region, effectively making it electrically equivalent to the base region. When the base region extends the entire width of the collector, the transistor has reached hard saturation. As saturation is approached, the rate of voltage decline is reduced, and this produces the tail-in voltage effect. In chapter 3 various base drive techniques are described which help to reduce this effect.

As can be seen in figure 2.03, there are also similar effects at turn-off. The

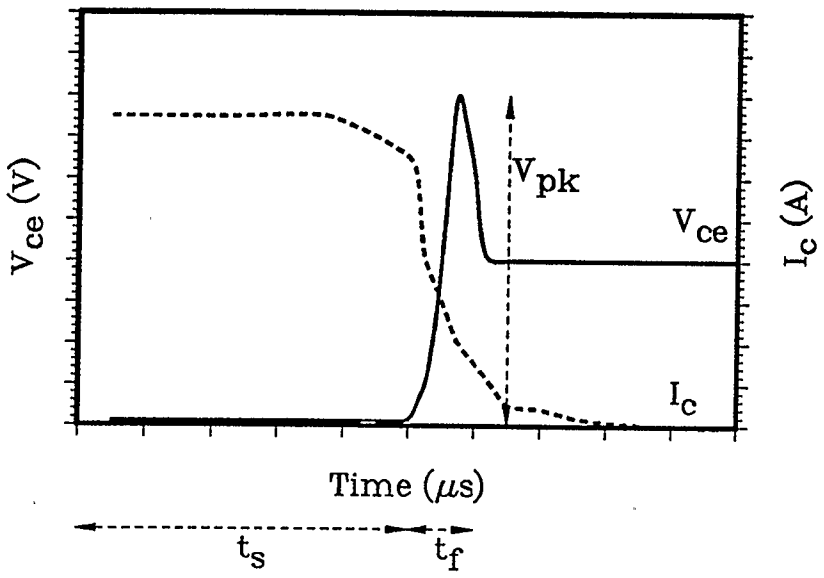


Figure 2.03. Power transistor turn off.

majority of the turn-off interval is the storage time, t_s. This parameter is much longer than any other switching time parameter. For example, in the Powerex KS22451010 Darlington transistors, the switching time specifications are $t_s = 12.0\mu s$, $t_{on} = 2.0\mu s$, $t_f = 3.0\mu s$. Storage time is the delay caused by the need to remove excess charge from the base of the transistor before the transistor begins to cease conduction and can support any significant voltage. This is why operating in quasi-saturation speeds up the transistor. Since there is less charge to remove from the transistor, the storage delay is shorter. Increasing the amount of reverse base current also speeds up this process and reduces the storage time. Since higher voltage transistors have thicker base and collector regions from which to remove charge, it follows that these devices have longer storage times than their low voltage counterparts. A transistor with a thinner base and higher base doping concentration has smaller storage times. Interdigitation also helps to improve storage time, since it provides more area for charge to be removed through, and it shortens the distance to the remote base regions.

Another turn off effect is the collector voltage lift up and rise. As the charge is removed from the transistor its effective resistance increases causing the voltage to increase. However, as charge is being removed from the transistor, the effective transistor cross-section is reduced. This is due to the fact that the charge is not withdrawn as fast from the remote base regions, leaving some areas of the transistor conducting and others not. This causes the voltage to rise quickly, causing large voltage spikes. With an inductive load, current decreases once V_{ce}

reaches a constant value. The effect of an inductive load and dI_c/dt will be to further increase the voltage spike at turn off. An interdigitated emitter will help to reduce this effect.

If a hard reverse drive is used, then the excess charge that remains in the collector will slow down the current fall time, causing a current 'tail' as shown in figure 2.03. This current tailout effect can be reduced if the transistor is operated very close to its breakdown voltage since the increased electric field will aid charge removal. The current tail out effect can also be substantially reduced by keeping reverse base drive to a minimum. In newer transistors a large amount of interdigitation is employed to help reduce the distance of remote base regions from the base contact. Increasing the effective area of the transistor at turn off helps to remove charge and reduce the effects of collector voltage rise and collector current tailout. A high reverse drive also increases the risk of second breakdown[26, 27].

2.3.3. Transistor Gain

It is important for power transistors to have a high current gain. There are several transistor properties that affect the gain. The two most important properties are the base transport factor, b_t, and the emitter injection efficiency, γ [10, 1, 28]. The base transport factor is the portion of electrons from the emitter which succeed in crossing the base and reaching the collector. It is obvious that a thinner base would have a larger base transport factor since the electrons have a smaller distance to travel to reach the collector. Injection efficiency is the fraction of

emitter current which is provided by electrons crossing from the emitter to the base, as opposed to holes crossing from the base to the emitter. In both of these cases, it is necessary for the inefficiencies to be made up by the base current. In ideal conditions, both of these values will be equal to 1. As well, the avalanche multiplication factor, M, also influences the gain. However, in most cases this number is equal to 1, except at high currents or near breakdown conditions. The common base current gain, α, is given by the following equation:

$$\alpha = b_t \gamma M \tag{2.1}$$

The common emitter current gain, β, which is approximately the dc gain, h_{FE}, is given by

$$\beta = \alpha / (1-\alpha) \tag{2.2}$$

By having sufficient gain in the transistor, base drive current may be kept to a minimum. The advantages of this are that the base drive circuit is smaller, easier to construct and more efficient. However, to get a high gain, it is necessary to increase the doping concentration of the base. The result of this is that the voltage blocking capability of the device is greatly reduced. Therefore, transistors with a high sustaining voltage also have a poor gain[10].

One way to avoid this problem is to utilize a Darlington arrangement of 2 or more transistors. A Darlington pair consists of a load transistor that is being driven by another transistor, called a driver transistor. This is shown in figure 2.04. The advantage of the Darlington arrangement is that the gain of the pair is approximately equal to the product of the original transistor gains. A disadvantage

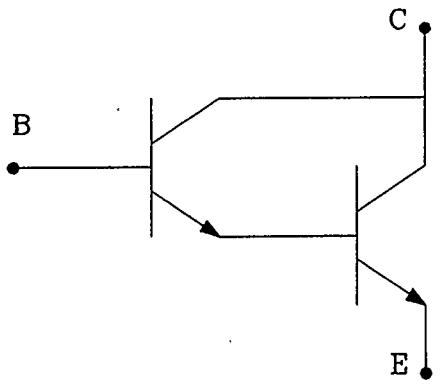


Figure 2.04. Darlington Pair Arrangement

of this is increased switching time. Although the load transistor is in quasi-saturation, the driver transistor does not turn off until the load transistor is fully off. There are several base drive schemes specifically for Darlington transistors that help to speed up the transistor.

2.4. Power Transistor Parameters

There are several limitations on the operation of power transistors. Care must be taken not to exceed device limitations. There are various parameters provided on the manufacturer's data sheets that are described below. An understanding of these parameters will help the user to select the correct transistor for an application and get maximum benefits from its use.

2.4.1. Safe Operating Areas

Figures 2.05 and 2.06 show typical safe operating area curves for a Power BJT. The safe operating areas are a factor in both steady state and transient operation, but are most likely to be exceeded during transient conditions. Going outside these operating regions could lead to transistor failure.

The forward bias safe operating area, shown in figure 2.05, is for conditions where the base-emitter junction is forward biased, mainly transistor turn on. The horizontal line on the safe Operating Area curve, line 1, is the maximum allowable current due to device thermal limitations. Line 2 is the line of maximum power dissipation. This line has a slope of -1 since the value of power dissipation along here is constant. Line 3 is the region where second breakdown occurs. Note that for this region breakdown occurs at lower voltages than would be expected if only

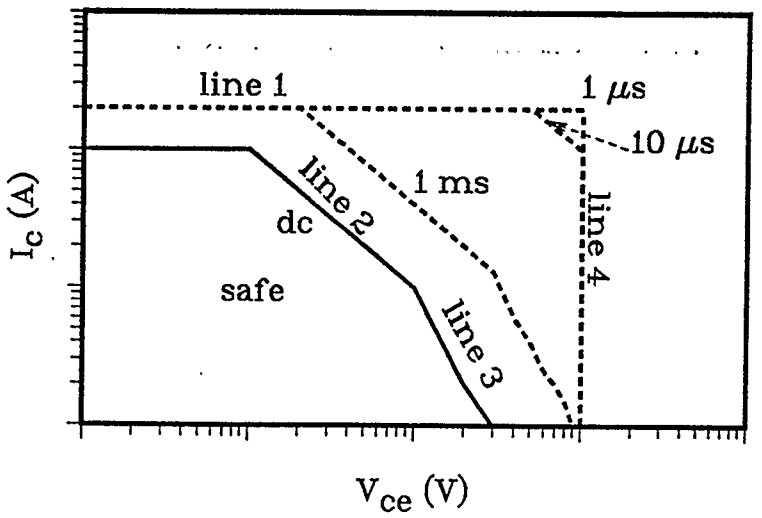


Figure 2.05. Forward Bias Safe Operating Area

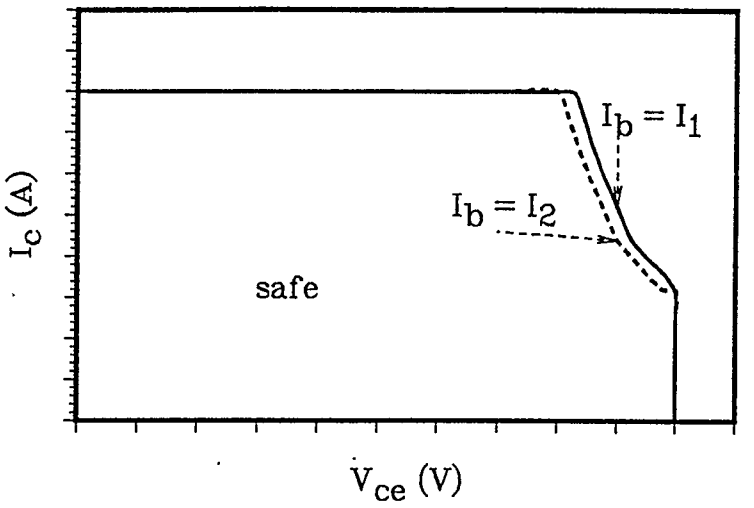


Figure 2.06. Reverse Bias Safe Operating Area

power dissipation is considered. Line 4 shows the maximum collector-emitter voltage. This is the sustaining voltage, described later. Avalanche breakdown will occur if this value is exceeded. There are several curves like this in a set. As the duration of a transistor pulse is shortened, it can withstand higher stresses, hence the outlying curves for the pulse widths shown. A transistor should not be operated outside its safe operating area for even a short period of time. In other words, the values of the transistor parameters at any given time should always be a point that is below the curves. As well, the curves for pulsed operation are non-repetitive, so that continuous application of these pulses at the limits of the safe operating area could lead to device failure. In most applications the device should never be operated outside the DC safe operating area, shown as a solid curve in Figure 2.05. It is important to note that the forward bias safe operating area is thermally sensitive. The device limitations must be derated for a high operating

temperature. It is important to get information from the manufacturer which indicates how to derate the safe operating area.

The reverse bias safe operating area, shown in figure 2.06, is for those conditions where the base-emitter junction is reverse biased, which occurs when the transistor is switched off. Comparing this with figure 2.05, it is seen that a transistor has a more flexible operating range when it is reversed biased. Note also that the breakdown voltage is increased when the junction is reverse biased. The curved line in this diagram is the second breakdown region. The reverse bias safe operating area is not as temperature sensitive as the forward bias region. However, note that this safe operating area is reduced for increased values of reverse base current.

2.4.2. Breakdown Voltages

Breakdown voltage is another important power transistor specification. There are several different breakdown voltages that are specified, each corresponding to different situations.

Avalanche breakdown is the most common form of breakdown in a transistor. Avalanche breakdown is sometimes referred to as 'first' breakdown. It is caused by the multiplication of charge carriers in a depletion region which is subject to a large reverse bias. The avalanche effect is basically a chain reaction. A charge carrier, electron or hole, is accelerated by the electric field and injected into the base of the transistor. This carrier may strike an atom and by impact liberate

another charge carrier, which is also accelerated. If the electric field is high enough, the carrier multiplication caused by this process is sufficient to release huge amounts of carriers, causing a substantial current to flow. This is avalanche breakdown. Note that the process itself is not harmful to the semiconductor and may be reversed. However, usually the increased power dissipation due to the current flow and high voltage drop is excessive, and the device may be thermally damaged.

Punchthrough or reachthrough breakdown is not very common in power transistors. It occurs when the collector-base junction is heavily reverse biased. As the reverse voltage increases, the collector region slowly extends into the base. Punchthrough occurs when the collector region has fully expanded over the base and reaches the emitter. Once again, this form of breakdown is only harmful when there is excessive power dissipation. A power transistor will rarely breakdown at the punchthrough voltage, since the other breakdown modes will likely occur first.

'Second' breakdown is a phenomena usually only encountered in power devices. 'Second' breakdown occurs at lower voltages than avalanche or 'first' breakdown. It is the result of current crowding in the emitter in those emitter areas that are near to the base. This can cause the local current density to exceed the maximum allowable value and cause thermal damage to the silicon. It is usually accompanied by the formation of a mesoplasma, a large region of charged particles, near the ohmic contact. Since the resistance of this region is much lower than the surrounding area, a large portion of the current flows through here,

possibly heating the semiconductor material to the melting point. 'Second' breakdown is described in chapters 1, 2 and 4 of Ref. [10] as well as in Ref. [29].

Various breakdown voltages may be given in the manufacturer's specifications which are dependent on the base emitter circuit:

$V_{(br)ceo}$: Collector-emitter breakdown voltage with $I_b = 0$. This is often referred to as the sustaining voltage.

$V_{(br)ces}$: Collector-emitter breakdown voltage with the base-emitter junction shorted ($V_{be} = 0$).

$V_{(br)cer}$: Collector emitter breakdown voltage with a resistance connected from base to emitter.

$V_{(br)cev}$: Collector-emitter breakdown voltage with the base-emitter junction reverse biased by a voltage. This is the best possible collector-emitter breakdown voltage.

$V_{(br)cbo}$: Collector-base breakdown voltage when $I_e = 0$. This is the punch through voltage.

The maximum current values can be readily seen from the safe operating area curves. When the ratings of a power transistor are specified, it is necessary for the user to determine for which conditions these ratings apply. In many cases $V_{(br)ces}$ and $V_{(br)cer}$ are not specified, but these values are always higher than $V_{(br)ceo}$ and less than $V_{(br)cev}$, and will increase with *decreasing* resistance. Also, many transistors sold in Darlington configurations have some resistance included from

base-emitter, so that many of the values given as sustaining voltage may be higher than $V_{(br)ceo}$. Keeping all these details in mind is important to selecting and properly using the best transistor for the specific application. The next two chapters make use of the information in this chapter in describing how to construct proper transistor base drive and protection.

CHAPTER 3

BASE DRIVE DESIGN

3.1. Introduction

Proper base drive is essential for fast and efficient transistor switching. Keeping the base drive as simple as possible will help keep costs and size down. Most of the essential base drive functions can be provided by a few simple components, and keeping unnecessary components out of the circuit helps to reduce noise and propagation delays. This chapter will describe the requirements for a good base drive circuit and review several commonly used base drive methods. Several optional features that may be incorporated in a base drive will also be discussed. From this information a base drive circuit was selected, designed and constructed. The performance of this base drive circuit is detailed later in this chapter. Some improvements to this base drive were made and are documented later in this chapter.

3.2. Base Drive Requirements

An effective base drive circuit is one that will turn the transistor on and off quickly and efficiently. With a good base drive circuit, not only is it possible to operate the transistors at higher frequencies, but switching losses can also be reduced. A good base drive circuit will keep the transistor's switching time well

within the manufacturer's specifications.

Since a bipolar transistor is a current driven device, proper base drive implies the proper base drive current waveform which is shown in figure 3.01. There are several parts of the waveform that require comment. First, a large overcurrent at turn-on is necessary to insure that the transistor will turn on rapidly. This is also useful in reducing the dynamic saturation interval. Once the transistor has been turned on, it is necessary to provide the required base current to keep the transistor fully on. It is usually a good idea to use a Baker clamp to keep the transistor in quasi-saturation. With a Baker clamp, the transistor's storage time will be reduced, but conduction losses will be increased. It most cases the additional losses can be

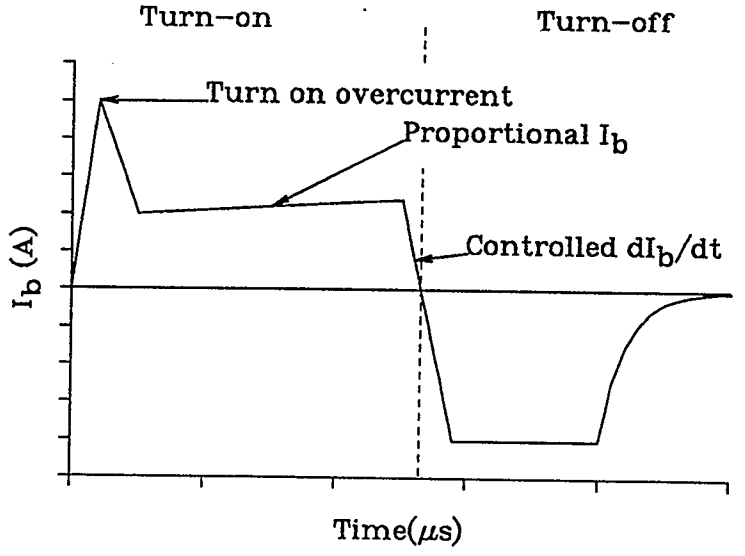


Figure 3.01. Ideal base drive current waveform

tolerated. In this thesis, operation with and without a Baker clamp is compared. Baker clamps are described in Ref. [30].

For turn-off, there are also some requirements to be met. Keeping dI_b / dt at turn-off to a constant level, helps to prevent the current tail out effect. The reason for this is that it will prevent the base-collector junction from becoming forward biased before the base-emitter junction is reverse biased[1]. As well, it is very important to provide a reverse base current to turn off the transistor. This will help to remove charge carriers from the base and collector, and this will in turn greatly speed up turn-off. The ideal base drive waveform is described in several references[21, 3, 5].

Several other important design considerations for base drives are also discussed in some common references[1, 3]. One feature that is essential is dc isolation for the base drive circuit. In many cases, the base drive is applied to a transistor with a floating emitter voltage, as shown in figure 3. 02. In order to provide the correct bias to the transistor, and to insure that it remains on for the desired duration, it is necessary to reference the base drive power supply to the transistor emitter and to provide dc isolation for the base drive circuit from the control logic and from other base drive circuits.

This can be done in one of two ways. One method is to drive the transistor by using a pulse transformer with the secondary connected between the base and emitter[22]. While a continuous on signal is sent to the drive, it is necessary that a chain of narrow pulses is fed into the transformer primary. The pulse transformer

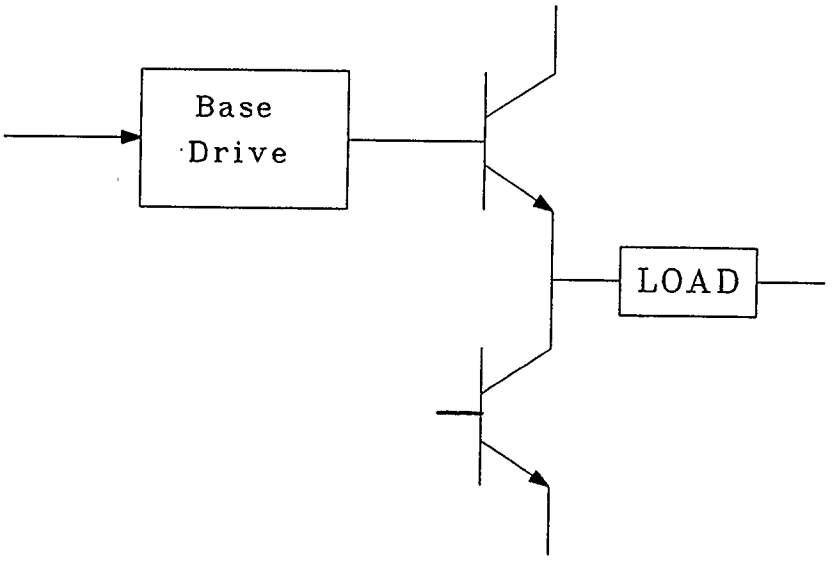


Figure 3.02. Base drive for a floating emitter.

effect will produce a continuous current pulse on the secondary winding which will drive the transistor. Pulse transformers are usually used for transistors that require a large base current. The other method is to provide the base drive circuit with its own isolated power supply, with its ground referenced to the emitter of the transistor being driven. In order to isolate the control logic from the base drive, an optocoupler is used. This type of base drive circuit is described in this chapter.

Various fail-safe features should also be considered for a base drive circuit. If there is no control signal applied to the input of the base drive, the drive should turn off the transistor and hold it off. This will prevent a continuous DC voltage from being applied to the load which may damage the load. As well, keeping transistors off when no control signal is present also prevents a 'feedthrough fault',

in which there is a short circuit across the dc bus due to both transistors in the same phase being on simultaneously. Another situation where a temporary feedthrough fault can occur is when the two transistors on an inverter leg are both switching. If one transistor turns on before the other has turned off fully, there will be a feedthrough. Turn-on of a transistor should be delayed until its complementary transistor has turned off. For situations in which an excessive current flows through a transistor, an overload detection circuit should be used which will shut the transistor off so that it will not be damaged[23]. Some of the base drive methods described in this chapter incorporate these failsafe procedures.

3.3. Review of Various Base Drive Circuits

3.3.1. Base Drive for a single transistor

For a single transistor, the base drive should supply current as described earlier. Since a single power transistor has a low gain, the base current that is required may be large. In many of these applications, it is much more practical to use a pulse transformer to step up the current. This configuration is shown in figure 3.03[22, 24].

Another way to solve this problem is to use a Darlington configuration, as described in chapter 2. In this method, the current is amplified by a driver transistor, which gives the transistor pair a much higher gain than would be possible if only one transistor was used. In high voltage transistors a triple Darlington is sometimes used. This is where one driver transistor drives another

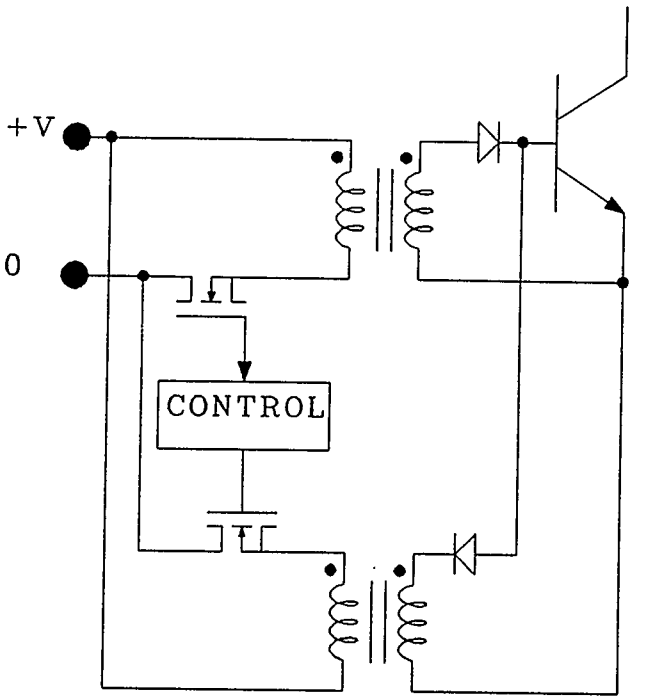


Figure 3.03. Pulse transformer base drive

driver transistor which in turn drives the load transistor. Also, it is possible to use one discrete transistor to drive another, making a Darlington pair from discrete devices. A variation of the Darlington pair that is becoming quite popular is the MOSFET/Bipolar Darlington configuration. In this arrangement a bipolar transistor has a power MOSFET as its driver[4, 5]. This will create a voltage driven device with high gain, a high current capacity and reduced turn-off losses. Many manufacturers are now selling these different devices.

3.3.2. Base Drive Methods for Darlington Transistors

There are several methods available for providing base drive to a power transistor[25,. 5]. In the methods that follow, power MOSFETs are used in the

drive circuits, although it is possible to use a bipolar transistor in the same application. Power MOSFETs were used since they are faster and their gate drive requirements are simple.

The first method is to drive the transistor with a single power supply, as shown in figure 3.04[25, 5]. With this method the transistor is turned on by a current through the resistor, and is turned off by eliminating the base current and allowing the transistor to desaturate. This method is simple to construct but has an extremely poor turn-off time, due mainly to the fact that with no reverse base drive current the charge carriers in the base can only be eliminated by recombination; a

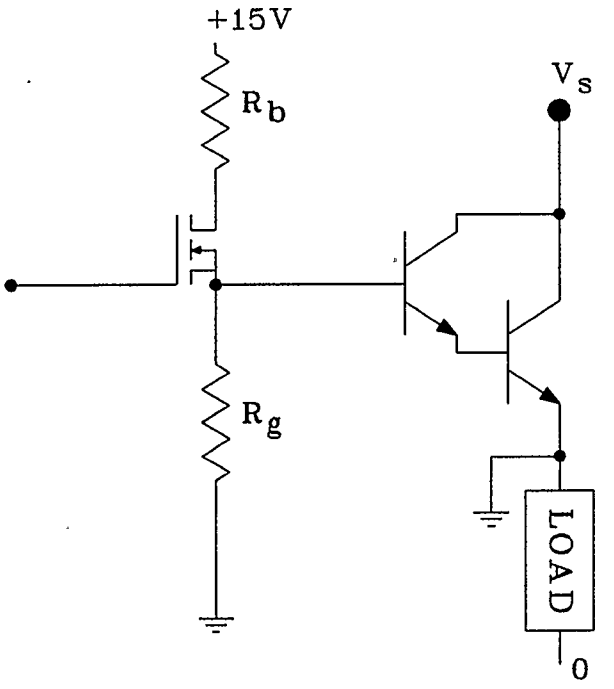


Figure 3.04. Single supply base drive

very slow process. As a result, storage time is very large.

The next method is a dual supply base drive, shown in figure 3.05[25, 5]. This method improves upon the previous method by using a negative power supply to provide reverse base current at turn-off. This reverse base current improves the turn-off time significantly. The main disadvantage of this method is that it consumes more power than other methods and therefore is less efficient. Also, R_g must be large enough to keep V_{be} above the minimum value required for forward

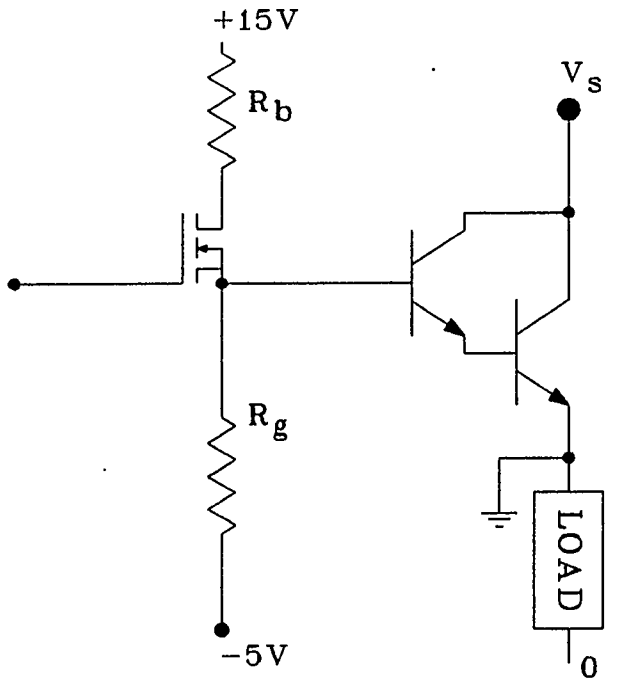


Figure 3.05. Dual supply base drive

bias. This limits the maximum value of reverse base current. This method is practical for a transistor that will be switching at very low frequencies (i.e. up to 10 times power frequency). For high frequencies an improved method should be used.

The improvement is achieved by using two complementary power MOSFETs, as shown in figure 3.06[25, 1, 5]. Bipolar transistors in a push-pull arrangement may also be used in this drive circuit; however, power MOSFETs are recommended because of the improvement in drive speed and the simplification of the base drive circuit. Since the MOSFETs are a complementary pair(one p and one n), only one will be on at a given time. This allows the turn-on and turn-off circuits to be designed independently. The turn-on circuit is designed to provide the required current, $I_{b(sat)}$, to the transistor base. The optional capacitor, C, is used to provide an overcurrent pulse at turn-on. Since this capacitor is fully charged at turn-on, it will discharge rapidly into the transistor base, causing the desired overcurrent effect to occur. The current then falls to the desired level until turn-off.

At turn-off, the forward current is removed and a reverse current is drawn from the base of the transistor. The magnitude of this current is fixed at a level that is determined by R_g. Optionally, no resistance is used and the drive becomes a fixed reverse voltage drive. At turn-off a large current is removed from the base and t_s is short. However, a rapid rate of change of reverse current can cause a tail-out effect. The optional inductor, L, can reduce this. It limits the rate of

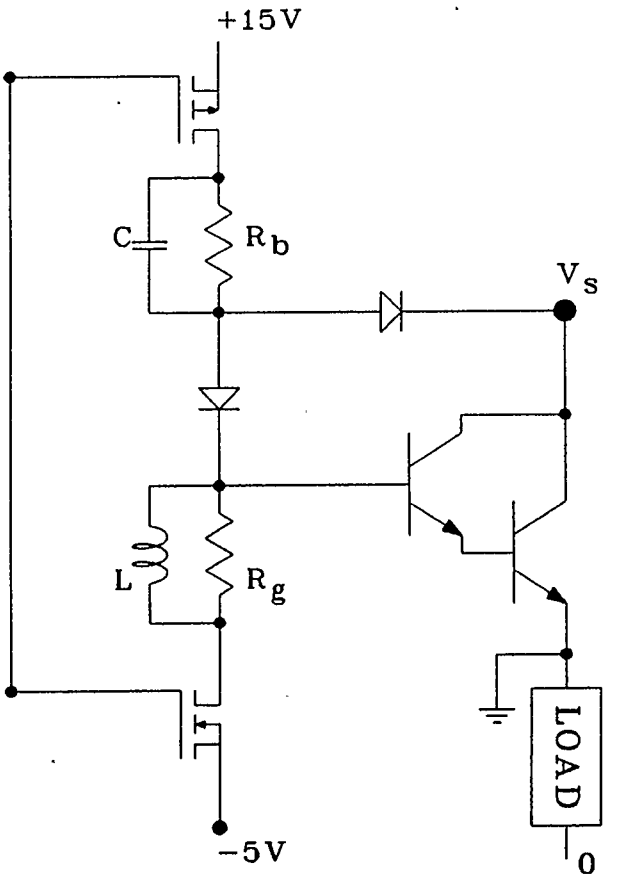


Figure 3.06. Dual MOSFET base drive.

change of the reverse current and as a result the tail out effect is reduced[5]. The resistor is used to provide a current discharge path for the inductor, reducing voltage spikes and noise. With this method the base-emitter junction is reverse biased at turn-off. This insures that the transistor stays off and increases the voltage blocking capability of the transistor to $V_{(br)cev}$.

Baker clamps, shown in figure 3.07, are often used in bipolar power transistor base drives. The base-collector diode provides a detour for the base current, and by reducing the current fed into the base it is possible to force the transistor β to its maximum. As well, V_{ce} is clamped to V_{be}, and this causes the transistor to operate in the quasi-saturation region. This also increases the conduction losses of the transistor. If the additional losses can be tolerated, then operation with a Baker clamp is recommended.

As mentioned earlier, it is important to provide isolation for the base drive. This is accomplished by providing the drive with an independent power supply and using an optocoupler on the input. The final base drive circuit using a Hewlett-Packard HCPL-2200 optocoupler is shown in figure 3.08. This opto-coupler was selected after a thorough search of the available devices. After much

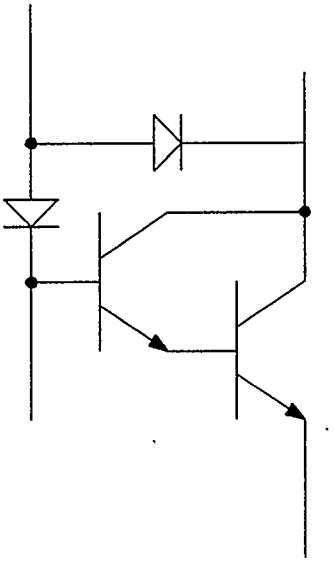


Figure 3.07. Baker clamp

experimentation it was decided that a very fast opto-coupler was required for the base drive to provide peak performance.

All the base drive techniques described in this chapter were tested experimentally. As well, some of the recommended modifications to the base drive were tested to determine how effective they were in practice. From this some recommendations are presented for implementing these features and for choosing the base drive components. The next section will explain how the component values were selected.

3.4. Base Drive Implementation

3.4.1. Selection of Component Values

Careful selection of the components used in the base drive will insure that satisfactory operation is obtained. As a result of the research and experimentation conducted for this thesis, several recommendations can be made. Referring to figure 3.08, the following guidelines can be used to select various components:

(1) Power MOSFETS: Select a device capable of handling twice the required base current, to provide a margin of safety. As well, it should be able to withstand the full power supply voltage of the base drive. The drain to source conduction resistance, r_{ds}, of the MOSFET should be low to limit power loss. Also, it is beneficial to have a device with a low value of gate to source threshold voltage, $V_{gs(th)}$. This will insure proper MOSFET switching. Be sure that the device can handle

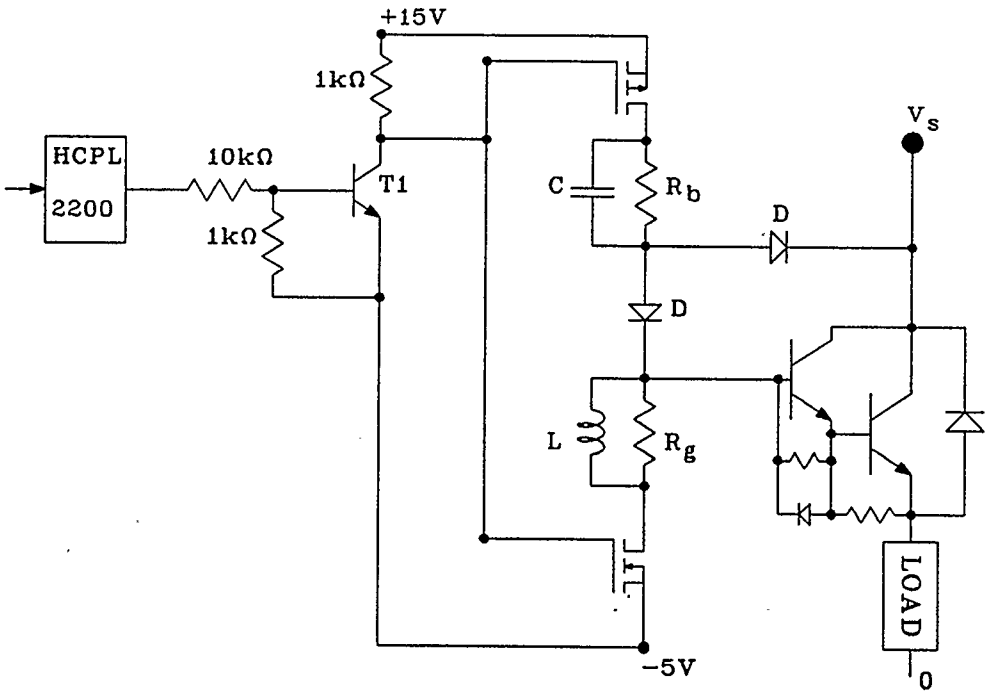


Figure 3.08. Final base drive circuit used

the maximum value of gate to source voltage, V_{gs}, that will be applied. This will guarantee a long device life. In this project an IRF 520 is used for the n-channel MOSFET and an IRF 9520 is used for the p-channel device. Always use a complementary pair of devices to insure that the switching is synchronized.

(2) Optocoupler: A fast optocoupler with very low rise and fall times is greatly desired. This will keep propagation delay to a minimum. A Schmidt trigger device is desirable. This project uses Hewlett-Packard

HCPL-2200 optocouplers. This opto-coupler was selected by the author after a detailed search of the available devices, and significantly improves the response of the base drive. Proper selection of both optocouplers and MOSFETs will insure that switching is a smooth on/off operation without unnecessary delays or leakage currents. A problem with some of the more common opto-couplers is the long rise and fall times which can cause undesirable transition states in the base drive.

(3) The resistance R_b is designed with the following equation, which was developed by a simple analysis of the circuit.

$$R_b = \frac{V_p - I_b(r_{ds}) - V_{be(sat)}}{I_b} \tag{3.1}$$

where

V_p is the positive base drive supply voltage

I_b is the desired base drive current (from specs.)

r_{ds} is the rated value for the power MOSFET

$V_{be(sat)}$ is the rated value for the power transistor

For the devices used in this project, the following values are used:

$V_p = 15V.$

$I_b = 1.3A$

$r_{ds} = 0.4\Omega$

$V_{be(sat)} = 2.5V$

This gives a final value for R_b of 10 Ω.

(4) Diodes: The diodes will conduct the base current when the transistor is on and be faced with the full transistor voltage when the transistor is turned off. All diodes used in the circuit should be rated for maximum base current as well as the maximum voltage rating of the power transistor.

(5) Other components: Transistor T1 is a general purpose switching transistor. Design resistor values to properly bias this transistor so that it turns fully on or completely off in step with the optocoupler output. The inductor L should be in the order of a few micro-henries. This drive uses 5 μH, which was determined experimentally. Select R_g to provide a short L/R time constant, 2 Ω being a good value in this case. This provides a time constant of 2.5 μs, which allows the circuit to recover completely for the next switching cycle. C was selected using trial and error. It was found that 1 μF gave a large overcurrent pulse that lasted for approximately 5 μs. when C is too low, the duration is too short, and when it is too high, the overcurrent pulse is not large enough to be effective.

(6) Power Supplies: Since the transistors that are used in an inverter often do *not* have grounded emitters, it is necessary to use a power supply with a floating ground which is then referenced to the emitter of the transistor being driven. To help reduce the occurence of ground

switching noise, it is recommended that high quality capacitors be used for power supply decoupling. In the base drive described here, the power supply consists of a center-tapped, ± 14V transformer and a full wave rectifier on the output. This is filtered using 4700 μF electrolytic capacitors, and regulated by 7815 and 7905 voltage regulators, which gives the +15/-5 V supply that is desired, as shown in figure 3.09. The regulators are stabilized using 0.1 μF metallized polyester capacitors, which helps reduce ground noise as mentioned earlier. This power supply was designed specifically for this application.

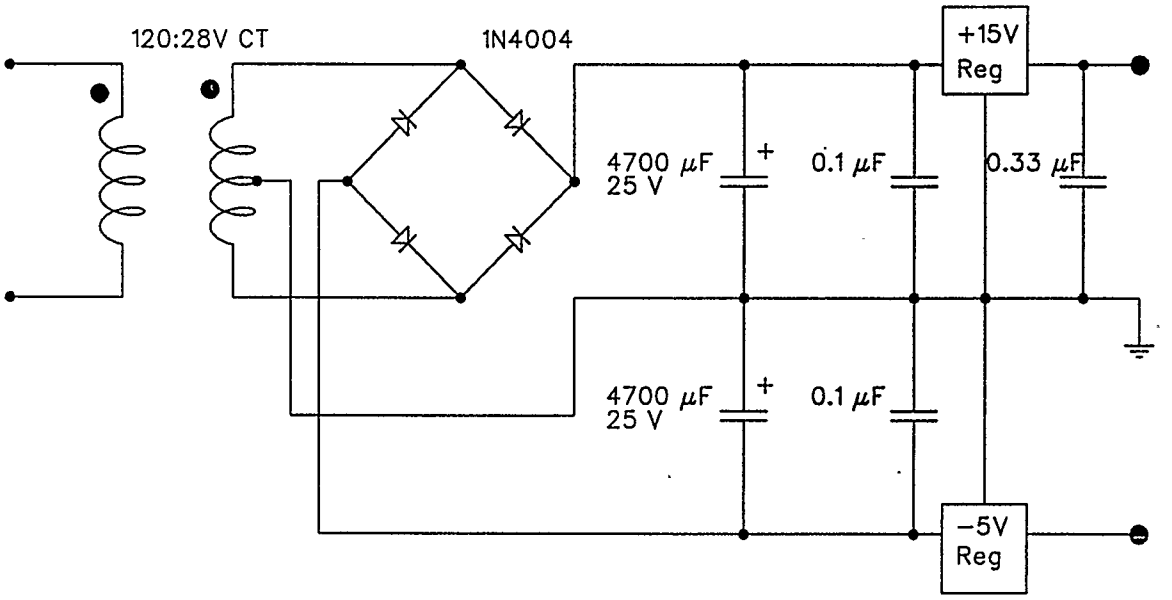


Figure 3.09. Base drive power supply

3.4.2. Measurement Techniques

Taking measurements in a power electronic circuit is not as simple as it is in low voltage/current applications. The most difficult problem is measuring large current, especially if it has a large dc component. As well, noise and interference were also a problem when dealing with high current measurements. Finally, measuring $V_{ce(sat)}$ and t_{ds} also posed a problem since it was necessary to accurately measure a value of 2-3 V in a waveform that varies in a range of over 100 Volts.

Two methods were used to measure current. The preferred method was to use a Tektronics 6302 current probe and amplifier. This probe used a Hall effect device to detect the current in a conductor it was clamped around. The Hall effect device was needed to get the low frequency components of the waveform. The only drawback of the device was that it was limited to a current of 20A. The collector current at full load was 100A.

The second method to measure current was by the use of a current shunt. This is a precision resistance that was placed in the circuit and the voltage drop across it was measured. The shunt used to measure I_c had a resistance of 1 $m\Omega$ and could handle current up to 100A. When used to measure current, it provided a waveform to the oscilloscope of magnitude 1 mV/A. Therefore a 100A pulse appeared as a 100mV pulse.

Noise was a substantial problem with measurements, particularly when using the current shunt. The large currents contributed some of the noise, since these currents create substantial electromagnetic fields. The leads from the current shunt to the oscilloscope were also a problem, as moving the leads could substantially alter the oscilloscope waveform. This problem was solved by enclosing the current shunt in a metal box and connecting it to the oscilloscope using coaxial cables that were twisted together. At low currents, the current shunt waveform was compared to the waveform of the current probe to verify accuracy.

Using a current shunt also requires the use of a differential oscilloscope. With any differential amplifier, common mode noise is a problem. Since some of the noise in the current shunt was not detected by any current probes, it is speculated that this is common mode noise. This can be greatly reduced if one side of the current shunt is grounded by a connection to the oscilloscope ground. In measurements where a grounded current shunt was used the noise was reduced substantially. However, in some cases it is not possible to ground either terminal of a current shunt.

Another source of noise was the oscillations caused by the rapid switching of the power supply ground between two different levels when the transistor was switching off. As a result of stray inductance/capacitance in the power supply ground leads, etc., this set up oscillations that spread throughout the circuit. These voltage fluctuations were often picked up in the current shunt, and since the oscilloscope in this case was sensitive to mV fluctuations the amount of noise

looked quite substantial.

A clamping circuit was required to measure $V_{ce(sat)}$ and t_{ds} since the higher voltage portion will saturate a scope amplifier that is set for low voltages and cause erroneous results[27]. This circuit simply consists of a 10 kΩ resistor and a 5V Zener diode connected from collector to emitter of the transistor under test. The differential scope voltage was measured across the Zener diode. This provided for a waveform that was accurate for the low voltage portion of the transistor switching cycle.

The following equipment was used to take measurements. A differential scope is needed to take accurate measurements of both V_{ce} and the differential voltage across the current shunt. A Tektronics 564B oscilloscope was used since this also provided scale illumination of the oscilloscope grid. A Tektronics P6302 current probe, as mentioned earlier, was also used for current measurement under 20A. Tektronics x10 probes were used to measure voltages. The results of these measurements are described in the next section.

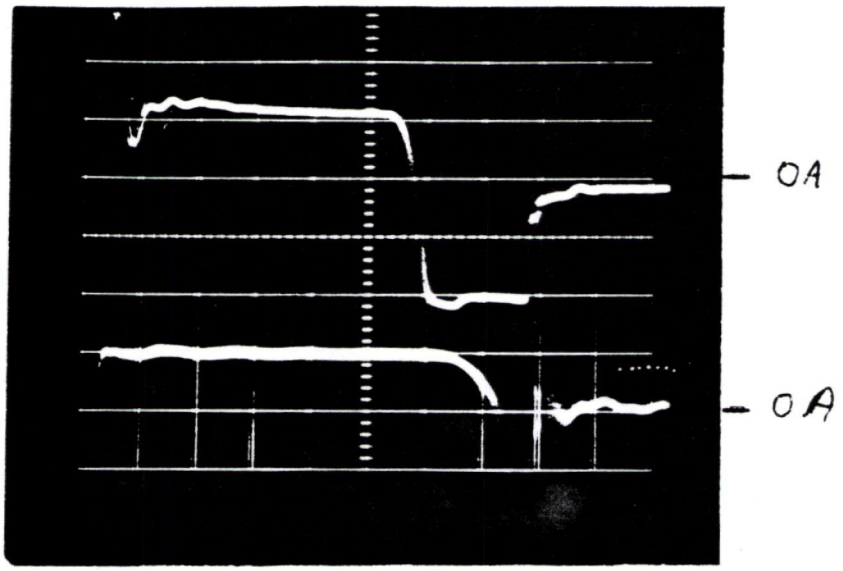
3.4.3. Experimental Results

This base drive was primarily designed to switch in 25 μs or less, and it performed satisfactorily in this respect. All the switching times for the power BJT were found to be within the specifications provided by the manufacturer, and in some cases these values were improved upon. One area where a disappointing performance was observed was with the dynamic saturation interval. This was

found to be quite long. However, even this was found to decrease when the transistor was operated at higher voltages, as will be seen in the next chapter.

Turn on of the power BJT was quite rapid, except for a long dynamic saturation interval. It was found that the transistor could be turned on in under $1\mu s$. As the load inductance was increased, the current rise time also increased, but V_{ce} was found to always drop very rapidly at turn-on. This means that the supplied voltage would be rapidly applied to the load when the transistor is switched on, and turn-on losses would be reduced. Figure 3.10 shows the actual base drive current obtained from this base drive circuit. Note the 1 μs overcurrent pulse at the beginning of the waveform, as well as the reverse current at turn-off. In this and all oscillograms in this chapter, the oscilloscope is triggered by the base drive control signal, so that at the beginning of the waveform turn-on or turn-off is applied. In figure 3.14b the entire dynamic saturation interval can be seen.

Figure 3.11 shows turn-on time as a function of load current. This shows the effect of using the capacitance, C, in the circuit. The choice of optocouplers was found to be significant in turn-on performance. A slow optocoupler resulted in turn-on delays as high as 5 μs. This is why the HCPL-2200 was selected. There are some commercially available base drive modules, and their propagation delay is also about 5 μs. Note that this graph shows two sets of turn-on times. As can be seen, using the input capacitor, C, tends to reduce turn-on time. It was also noticed that during the overcurrent period the transistor voltage was reduced, but this increased again when the pulse ended. After much experimentation, no



V_s = 25V, f_s = 20 kHz I_c = 100A. Top: I_b 1A/div. Bottom: I_c 100A/div. Time: 5 μs/div.

Figure 3.10. Base drive current produced.

capacitor value was found that provided any more improvement of transistor turn-on.

The next graph, figure 3.12, shows the storage time of this transistor with and without a Baker clamp. Notice the significant reduction of storage time with the Baker clamp. However, this is not without some adverse effects. Referring to figure 3.13, oscillograms showing transistor turn-off with and without a Baker clamp can be compared. Most of the noise present in these oscillograms is caused by ground voltage and common mode noise, as described in the previous section. Note that with a Baker clamp more noise is present at turn-off. This could be caused by feedback of noise through the Baker clamp diodes. Since the Baker clamp causes an additional voltage drop of 0.5 V, the additional power loss

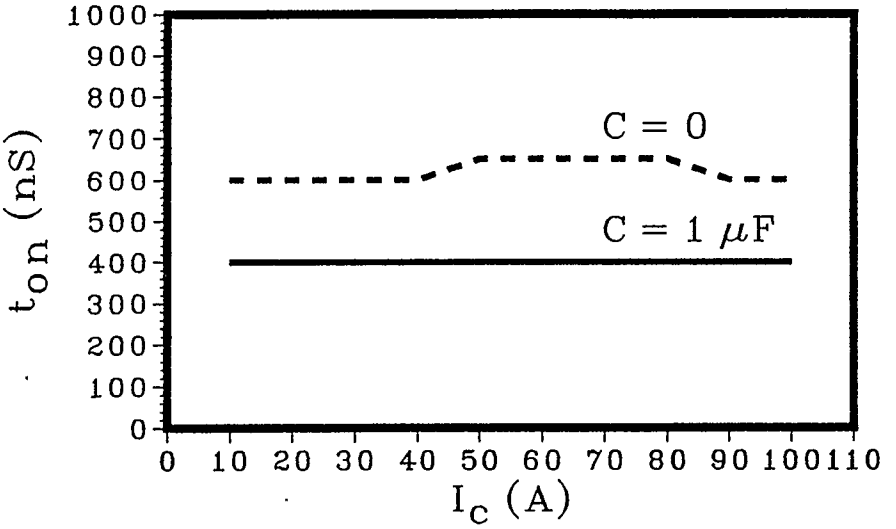


Figure 3.11. Turn-on time of transistor vs. I_c.

associated with the Baker clamp is 100A x 0.5V = 50W. This value is not excessive when it is considered that the load power is 5-10 kW and the transistor can safely dissipate 620W.

In figure 3.14 oscillograms are shown for one entire switching cycle. Figure 3.14a is with f_s = 200 Hz, and figure 3.14b is taken at 2000 Hz. The dynamic saturation interval can be seen in these oscillograms.

Most literature recommends that an inductor be used in the turn-off circuit. Although this did not have any appreciable effect on the speed of turn-off, it was found that a small inductance helped to remove noise in the circuit. It is also reported to help reduce current tail-out at turn-off[5]. This could not be verified

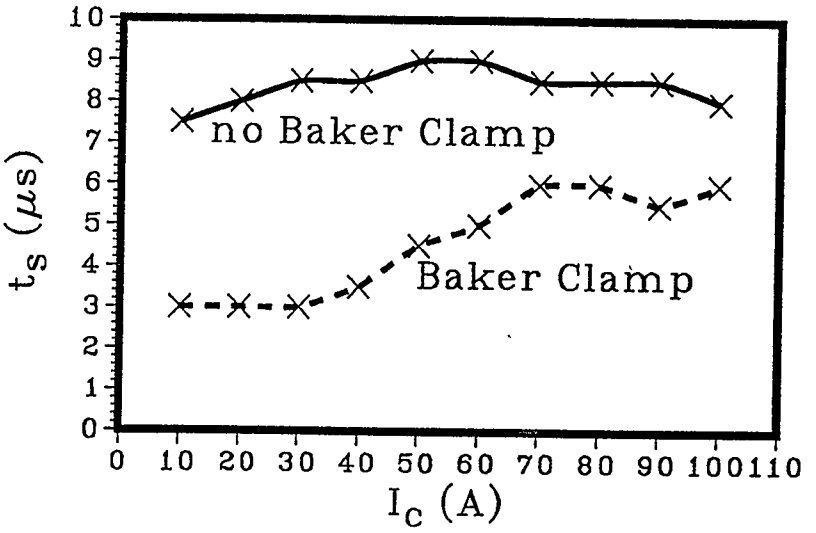


Figure 3.12. Storage time with and without a Baker Clamp experimentally.

3.4.4. Evaluation of Base Drive

Efficiency and high speed switching were the two main objectives that were met with this base drive circuit. Fast switching was necessary since these transistors are to be used for an inverter which would be using Pulse Width Modulation(PWM). By designing for low propagation delay and fast switching, this base drive circuit succeeded in being very fast. The base drive was optimized to provide excellent switching times. Transistor switching times are within the manufacturer's specifications, and this base drive is faster than the commercially available base drive modules.

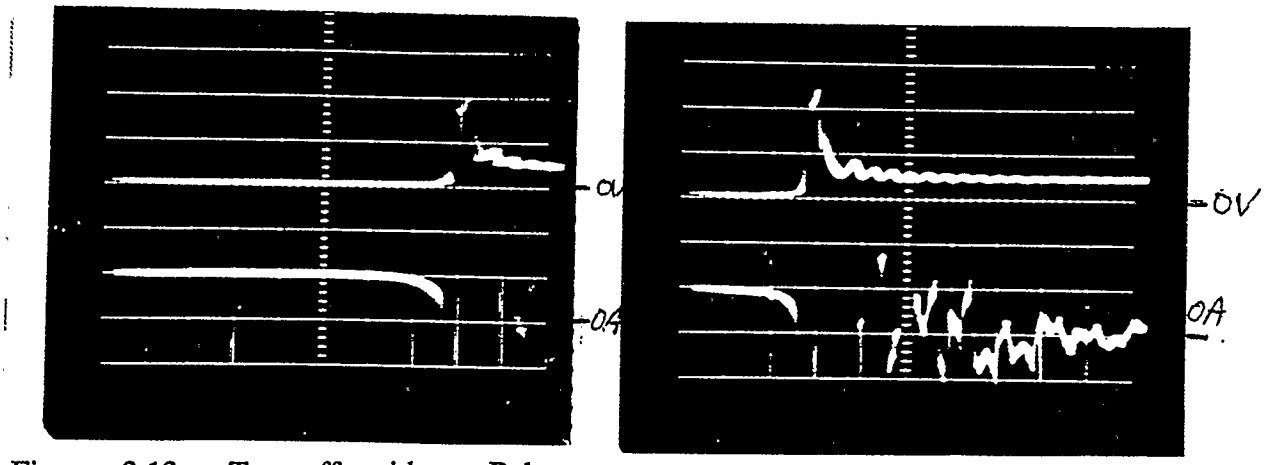


Figure 3.13a: Turn-off without Baker Clamp. I_c=20A, f_s=20kHz. Top: V_{ce} 50V/div. Bottom: I_c 20A/div. Time: 1 μs/div.

Figure 3.13b: Turn-off with Baker Clamp. I_c=20A, f_s=20kHz. Top: V_{ce} 50V/div. Bottom: I_c 20A/div. Time: 1 μs/div.

Figure 3.13. Oscillograms of transistor turn-off

Efficiency is achieved by a base drive that uses as little power as possible and operates the transistor in a way that minimizes losses. Using a dual MOSFET drive helped to accomplish this. Using power Darlington transistors also helped, since the base drive current is lower. The base drive losses are minimized because the current in the power resistors is small and the resistor is not conducting current when it does not have to.

The cost of this base drive was quite high, in fact it was more than the cost of the transistor module itself. However, several expensive components contributed

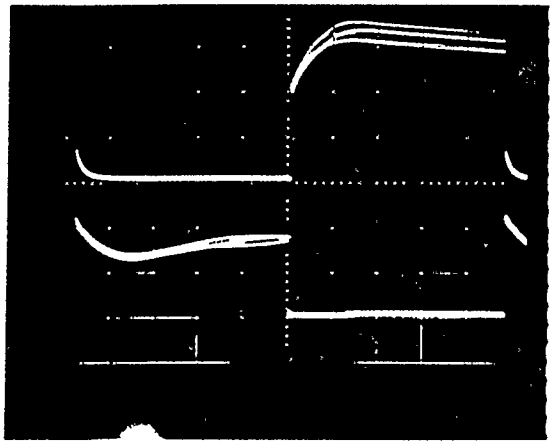


Figure 3.14a: Full cycle at 200Hz. I_c=100A. Top: V_{ce} 10V/div. Bottom: I_c 50A/div. Time: 500 μs/div.

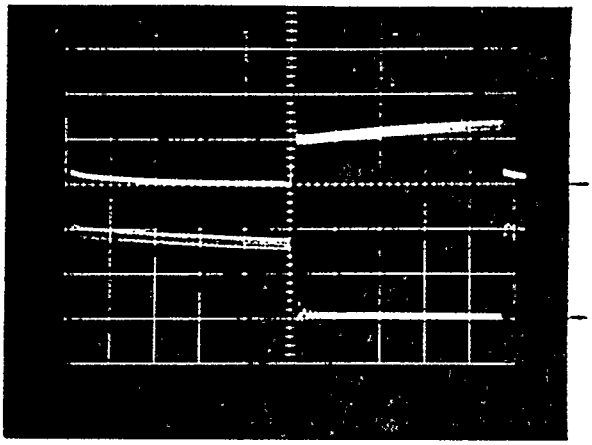


Figure 3.14b: Full cycle at 2000Hz. I_c=100A. Top: V_{ce} 10V/div. Bottom: I_c 50A/div. Time: 50 μs/div.

Figure 3.14. Oscillograms for full switching cycle

largely to this cost. The transformer used in the power supply accounted for almost 1/3 of the cost. As well, the optocoupler was also expensive, since its high speed was desired. If a dual power supply with the positive and negative voltage capability is available, using this could easily reduce the cost. The rest of the circuit is not expensive. Another alternative is integrated base drive modules that have recently become available from the manufacturer. These are smaller and cost less but are much slower than the base drive described in this chapter. A pulse transformer base drive would likely have been even more expensive.

Noise free operation is also desirable in a base drive. Several steps were taken to try to eliminate noise. Placing small capacitors in the circuit tended to slow the circuit down, without eliminating much noise. Sometimes the capacitor would even increase the noise. Some of the noise was the result of the current measuring methods, as described earlier. Since the power supply ground is the emitter of the power transistor, transistor switching quickly changes the ground level. This set up oscillations in the power supply that spread throughout the circuit. None of the noise problems were serious enough to be detrimental to the operation of this circuit. The attempts to reduce noise were entirely experimental, i.e. trial and error, based on typical noise reduction techniques.

3.5. Conclusions

Several possible base drive circuits were reviewed in this chapter. These represent the easiest methods of achieving the desired base drive current. Additions to the circuit can be made if they are needed, but the essential features have been incorporated. This base drive is designed to provide the basic on/off bias current, and improvements were made to operate at 20 kHz. Also, the base drive can be used effectively for a transistor with a floating emitter. Excellent waveforms are obtained at frequencies up to 2000 Hz. This base drive would therefore be adequate for most PWM applications.

As a result of the research and experimentation conducted for this thesis, several recommendations can be made. It is beneficial to use power MOSFETs as

opposed to bipolar transistors in the base drive. Also, the additional components such as capacitors and inductors in the base drive are not very effective in improving performance. Baker clamps provide a significant reduction in storage time of the transistor. Finally, noise was found to be the worst problem in base drives. In section 3.4.1 the design criteria developed for a base drive is summarized.

There are some possible changes that could be made to this base drive in the future. The positive 15V supply could have been reduced to 10V, reducing the value of power dissipated in R_b. A 15V supply was used to make the base drive less sensitive to noise or fluctuations in the supply voltage. With a 10V supply only a minimal improvement in efficiency would be gained. However, less stress would be placed on the semiconductors in the base drive circuit. A circuit could be added to the base drive to provide automatic shut off if there is excessive collector current. It is also possible to develop a base drive circuit which responds to the instantaneous voltage, current or temperature of the transistor. However, such circuits are quite complex and may not be very reliable.

In the next chapter, protection methods will be examined that will help to eliminate the turn-off voltage spikes and other switching transients seen in this chapter. A good base drive circuit coupled with adequate protection is necessary to apply a power BJT in a practical switching circuit.

CHAPTER 4

TRANSISTOR PROTECTION

4.1. Introduction

As can be seen from the oscillograms presented in the preceding chapter, transistor switching creates voltage and current transients which exceed recommended operating conditions. To maintain transistor operation within its forward and reverse bias safe operating areas, it is necessary to use a snubber circuit to reduce these transients. The snubber also reduces power dissipation in the transistor.

In this chapter, several snubber circuits are described. There is a large amount of literature available on lossless snubber circuits. As a result of the research conducted for this thesis, a broad understanding of the state of the art of lossless snubber technology was developed. From this research a paper summarizing these snubber circuits was written[31]. Two passive resonant snubbers were constructed and compared. The results take the form of numerous oscillograms, since the resulting waveforms are the best method of illustrating snubber operation. In addition to the description and review of snubber circuits, some design guidelines have been developed. Guidelines for the selection of snubber components are presented in this chapter. Finally, some of the problems encountered in the implementation of the snubbers are identified, and possible

solutions are offered.

Spikes and switching transients are not the only hazards that a transistor must be protected from. There is also transistor heating due to power dissipation. Some equations are provided which are useful in calculating power dissipation. Since most of this power loss occurs during transistor switching a good snubber and efficient base drive are essential in keeping these losses low. A heat sink is also used to provide thermal protection of the transistor.

4.2. Thermal Protection

It is important to provide adequate thermal protection to a transistor. An estimate of the transistor losses must be made to calculate the thermal protection requirements. Then, using the thermal data provided for the device, the required specifications of the heat sink are determined. From this an appropriate heat sink may be selected. In some cases it may also be necessary to provide a cooling fan in addition to a heat sink. For large devices that dissipate more than 1000W, it may be necessary to use a chill block, a liquid cooled metal block, instead of a heat sink for cooling.

One problem that is evident with this approach is the difficulty of properly estimating the power loss of the device without testing it under operating conditions, but the device cannot be placed under operating conditions without cooling. It is therefore necessary to predict the power loss of the device. The value of maximum power dissipation for the device may also be used for initial

calculations. Using this value insures adequate protection, but if this is much larger than actual losses, then the heat sink is larger and more expensive than necessary.

Equations that may be used to predict the losses of several devices during operation can be found in several papers. These equations are summarized in Ref. [32] and are used to calculate the power loss.

The equations given in this paper for loss calculation in a PWM inverter application are as follows:

$$P_{cond} = V_{ce(sat)} I_c K_3 M + 0.318 I_b V_{be(sat)}$$

$$P_{ds} = K_4(0.1V_s - V_{ce(sat)})I_c$$

$$P_{off} = (0.5)K_5 V_s I_c t_{cf} f_s$$

$$P_{on} = (0.5)K_5 V_s I_c t_r f_s + K_6 V_s I_c t_{rr} f_s + K_7 V_s Q_{rr} f_s$$

where;

P_{cond} is the conduction loss
P_{ds} is the additional loss due to dynamic saturation
P_{off} is the turn-off loss
P_{on} is the turn-on loss
$V_{ce(sat)}$ is the collector-emitter saturation voltage
I_c is collector current
I_b is the base current
V_s is the supply voltage
t_{cf} is the turn-off crossover time
t_r is the turn-on rise time
$V_{be(sat)}$ is the base-emitter saturation voltage
f_s is the switching frequency
t_{rr} is the feedback diode reverse recovery time
Q_{rr} the recovered charge in the feedback diode
K_3, K_4, K_5, K_6, K_7 are various constants
M is the modulation index (< 1)

which are determined from tables included in Ref. [32]. The values of the constants are based on the power factor of the driven load. Since this is unknown, a power factor of 1.0 is used since this will give worst-case conditions. Similarly, M = 1 was also used.

From the specified data, tables, and design criteria, the following values are used to calculate losses for this application:

$V_{ce(sat)} = 2.5V$
$V_c = 500V$
$I_c = 50A$
$I_b = 1.3A$
$t_{cf} = 5\mu s$
$t_r = 2\mu s$
$t_{rr} = 0.6\mu s$
$f_o = 2kHz$
$Q_{rr} = 12\mu C$
$K_3 = 0.25$
$K_4 = 0.15$
$K_5 = 0.25$
$K_6 = 0.33$
$K_7 = 0.5$

Using these values, we get:
$P_{cond} = 32.3W$
$P_{ds} = 356W$
$P_{off} = 31.25W$
$P_{on} = 28.4W$

which gives a total value of power loss of 448 W. The maximum power dissipation for the devices used is 620W. Note that the dynamic saturation accounts for most of the loss. This is not as severe as calculated. The oscillograms for turn-on shown later in this chapter indicate that V_{ce} drops to 10V and then slowly decreases, whereas these equations assume that V_{ce} drops to 0.1 V_s and

then slowly decreases. This value of V_{ce}, 25V, was used in the above calculations.

Using the calculated value for power dissipation and the values of thermal resistance for the device, it is possible to calculate the required thermal resistance of the heat sink. Alternatively, if a particular heat sink is being used, then the maximum allowable power dissipation may be calculated. The maximum allowable junction temperature of the device, T_j = 125°C. Assuming an ambient temperature of 25°C, this gives a temperature difference of 100°C. The maximum value of thermal resistance, R_θ, is given by

$$R_\theta = \frac{T_j - T_a}{P_d} \tag{4.1}$$

The thermal resistance is given by

$$R_\theta = R_{\theta jc} + R_{\theta cs} + R_{\theta sa} \tag{4.2}$$

where;

$R_{\theta jc}$ is the thermal resistance from the transistor junction to its case,
$R_{\theta cs}$ is the thermal resistance from the case to the heat sink, assuming lubrication with a thermal compound,
$R_{\theta sa}$ is the thermal resistance of the heat sink to the ambient air.

For the transistor used, $R_{\theta jc}$ = 0.2 °C/W, and $R_{\theta cs}$ = 0.15 °C/W. A Wakefield 441 heat sink was selected as it is the best one readily available that could be used with these transistors. This heat sink provides a thermal resistance of $R_{\theta sa}$ = 0.2 °C/W with an air flow of 100 fpm or more. This gives a value for R_θ of 0.55 °C/W. From equation 4.2, it is found that the power dissipation, P_d must be less than 182 W. Using a value of 10 V in the equation for P_{ds} gives P_{ds} = 56.25 W

and P_d = 148 W. Note that this is safely within the allowed maximum, whereas maximum P_d would be exceeded if the dynamic saturation effect was at its worst case.

4.3. Protection from Switching Transients

The power transistor is most likely to experience harmful switching stresses when it is switching into an inductive load. The switching trajectory often exceeds the safe operating area, and even if it does not, the high switching losses often increase the thermal dissipation of the device.

4.3.1. Sources of Switching Stresses

When a power transistor switches in the presence of inductance, switching stresses occur. The inductance may be part of the load, or it may be due to inductance in the power supply or the wiring of the circuit. In any case, a power switching device will be turning off a large current, and in a very short time. As a result of circuit inductance, voltage spikes many times larger than the steady state DC supply voltage will occur, which will destroy the transistor if any of the breakdown voltages are exceeded.

These voltage spikes most often occur at turn-off. There are also transients present at turn-on, usually in the form of current surges. These overcurrents are usually caused by recovery currents from other power semiconductor devices that have just switched off, or the discharge of capacitance in the circuit. Although the magnitudes of these currents is not as severe as the voltage spikes at turn-off, they

are still hazardous since the forward bias safe operating area is less rigid than the reverse bias safe operating area.

Protection against these switching stresses is the purpose of a snubber circuit, which consists of devices such as capacitors and inductors which serve to reduce the switching stresses, diodes or other switching devices that will regulate current flow in the snubber, and finally some method of discharging the snubber components prior to the next switching. Snubber circuits vary in complexity, usually as a result of elaborate methods for discharging the snubber components. The following sections describe some of the snubber methods that can be used.

4.3.2. Snubbers

As mentioned previously, there is a variety of methods that are available to provide snubber protection to switching devices. The various snubbers that are available can all be classified into a few general categories[11, 31]. One major distinction between the snubbers is whether they are resonant or non-resonant. With a non-resonant snubber the energy is discharged into a resistor and dissipated, and the maximum operating frequency is limited by the power rating of the resistor. A resonant snubber will store the snubber energy in resonant components (inductors, capacitors, transformers) until it can be discharged into the load or back into the power supply. This will make the system more efficient. More importantly, it makes it possible to operate the switching devices at high frequencies, which is necessary if any form of pulse width modulation (PWM)

control is to be used on the equipment.

The snubber is classified as resonant/non-resonant or active/passive based on how L_s and C_s are discharged. A passive snubber uses only resistors, capacitors, inductors, transformers and diodes to discharge the snubber components. An active snubber circuit uses additional switching devices, power supplies and power converters to discharge the snubber components. Examples of such devices are thyristors, mosfets, switchmode power supplies, etc. Resistive snubbers are described later in this section, and resonant or lossless snubbers are described in section 4.4.

Figure 4.01 shows the basic components of any snubber circuit. The inductor in series with the transistor is used to limit the overcurrent effects at turn-on. It also will drop the entire supply voltage across it at turn-on to keep the transistor operating in the forward bias safe operating area. The capacitor in parallel with the transistor is used to limit the voltage at turn-off. This capacitor absorbs excess current when the transistor is turning off, and will slowly charge to V_s, thus keeping the transistor in its reverse bias safe operating area until it is fully turned off. The diode is used to prevent the capacitor from discharging into the transistor at turn-on. This diode polarizes the snubber. In section 4.5 guidelines are presented to aid in the design of these component values.

A simple RLC snubber is shown in figure 4.02. This snubber is known as a unified snubber since it combines separate turn-on and turn-off snubbers, using only one resistor and one diode to discharge both L_s and C_s [1, 11, 12, 13, 33, 14].

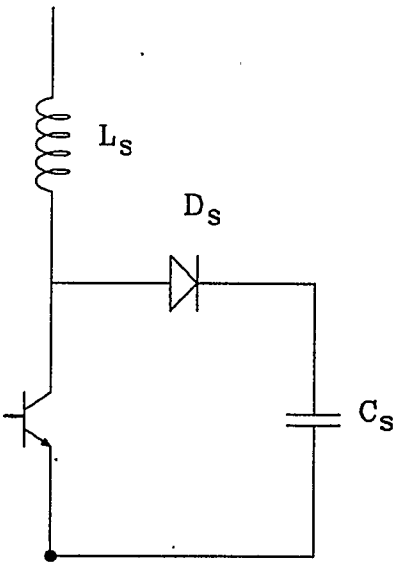


Figure 4.01. Basic snubber components.

L_s limits the turn-on current and C_s will limit the voltage rise at turn-off. When the transistor is turned off fully, and C_s is fully charged, the excess current in L_s will be dissipated in R_s. At turn-on, C_s will discharge into R_s via the transistor. The snubber is polarized by the diode D_s so that the capacitor will not discharge instantly through the transistor and a resonant circuit will not be set up between L_s and C_s.

This snubber circuit is simple, inexpensive, and effective. However, with high power devices switched at PWM frequencies, the power loss in the resistor becomes excessive. Equations that may be used to calculate the resistive power loss are given in section 4.5. This problem is overcome by a resonant snubber, in

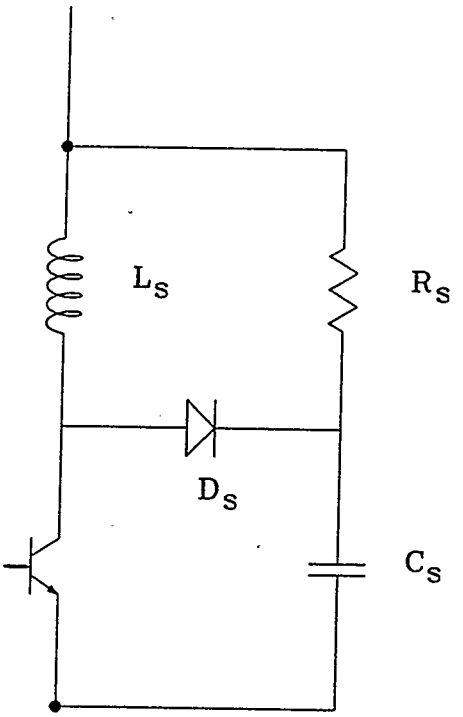


Figure 4.02. RLC snubber circuit.

which the resistor is replaced by a resonant, lossless circuit. Note that a snubber will not eliminate the switching losses, only reduce them to safe levels. To eliminate the losses, it is necessary to switch the devices on or off when either the voltage across or the current in the device is reduced to zero. This is accomplished using a Resonant DC Link Converter, described next.

4.3.3. The Resonant DC Link Converter

The Resonant DC Link Converter, RDCL, uses a resonant circuit in the DC link supplying power to the inverter, as shown in figure 4.03. The RDCL is an alternative to using snubber circuits. It causes the supply voltage to the inverter to be reduced to zero at regular intervals. It is possible to switch the inverter power

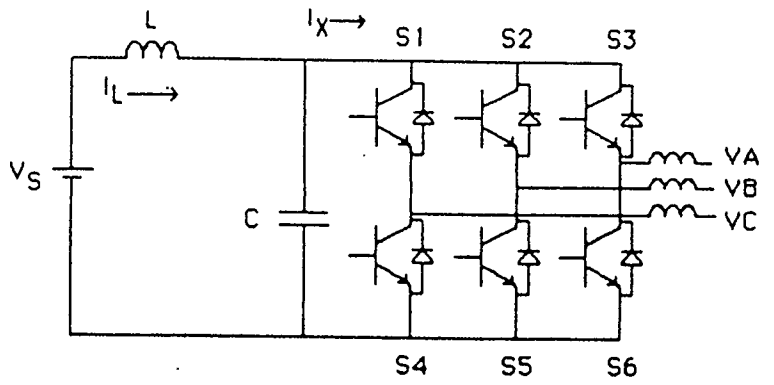


Figure 4.03. Resonant DC Link converter.

devices at these times, avoiding switching losses and SOA considerations. This converter is described in several papers[34, 35, 36].

This converter provides an output similar to that of PWM inverters, except that the voltage pulses are half sine pulses instead of square pulses. If the resonant frequency is high enough, the effect of the resonant link will not be felt by the motor, and it will rotate smoothly, as in a PWM inverter.

One problem with the RDCL converter is the effect of the dead time, which occurs when the DC link is held at zero voltage for switching. For transistors with large t_s and t_f this will mean a long period of deadtime, with distortion effects on the output of the inverter. Due to the complexity of control for this converter, it was not constructed. Only conventional snubber circuits were built and compared for this thesis.

4.4. Summary of Lossless Snubber Circuits

4.4.1. Characteristics of Resonant Snubbers

In a resonant snubber, the energy that is stored in the snubber components is transferred to a resonant circuit and from there it is sent into the load. This improves the efficiency of operation and eliminates the need for a large resistor to dissipate the energy.

There are several different kinds of resonant snubber circuits. Some of the circuits use additional switching devices while others use devices such as switchmode power supplies (SMPS) to transfer the energy back into the load. All of the snubber circuits attempt to fulfill some of the following properties of ideal snubbers, proposed in Ref. [15].

(1) no fundamental losses;
(2) part count as low as possible;
(3) charging and discharging currents for the snubbers should not cause additional current in the power switching devices;
(4) no additional switching devices;
(5) no additional power supplies should be used by the snubbers;
(6) voltage stress on the snubber devices should be limited to the level of the main switching devices;
(7) current in the snubber devices should not exceed the current in the main switching devices;
(8) all voltage stresses should be limited to no more than the dc supply voltage;
(9) high reliability and safety of operation;
(10) circuit functioning should be independent of operating conditions.

Not all of the conditions may be fulfilled, as some of them are mutually exclusive and some will depend on using ideal, lossless devices. Points 3 and 4 are not both obtainable as the stored energy must be discharged through some device. As a result either additional switching devices are used or the energy will pass through the main switching devices. Points 8 and 9 are essential for most applications. Eliminating the overcurrents and overvoltages due to snubber action is also difficult, and often a tradeoff must be made. If the part count is minimized and the snubber does not require any additional power supplies, then cost and size can be minimized.

4.4.2. Examples of Lossless Snubbers

Several different kinds of active snubbers are available. One method is to transfer the energy through a switched-mode power supply (SMPS) or other DC/DC converter back into the DC supply[1, 16]. One possible circuit using this method is shown in figure 4.04. An additional capacitor and/or inductor would be used to transfer the energy from the snubber components to the converter. This additional capacitor is usually much larger than the snubber capacitor, therefore the voltage on it will be small. This method is more complex than other methods, and could be expensive due to the switched-mode power supply. There is also a version of a resistive snubber, described in Ref. [14], in which a self-oscillating push-pull converter (SOI) is used in place of the resistor to return the energy to the load[16].

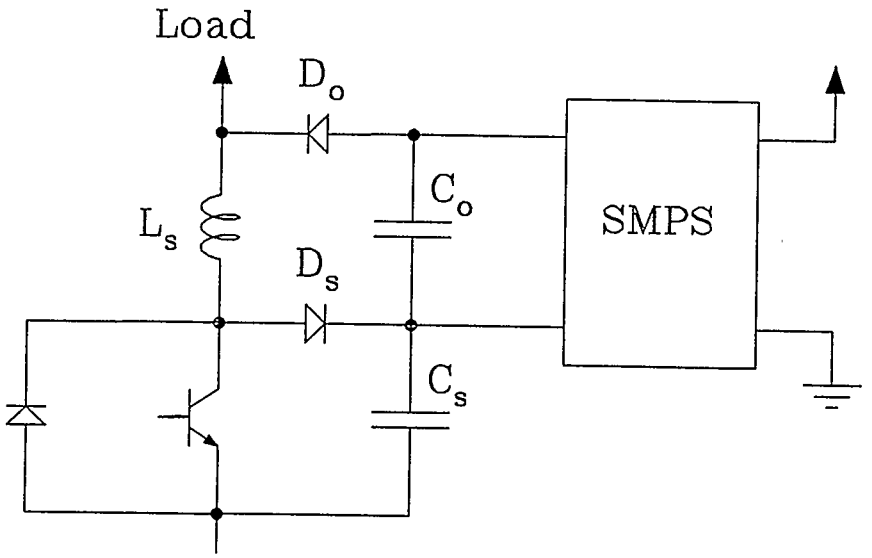


Figure 4.04. Snubber using switched-mode power supply.

Another active technique for recovering the energy in the snubber components uses additional switching devices[15, 17]. In this method, the snubber capacitors are discharged through a thyristor and an inductor via the DC supply, as shown in figure 4.05. Doing this will eliminate the turn-on overcurrent in the main devices

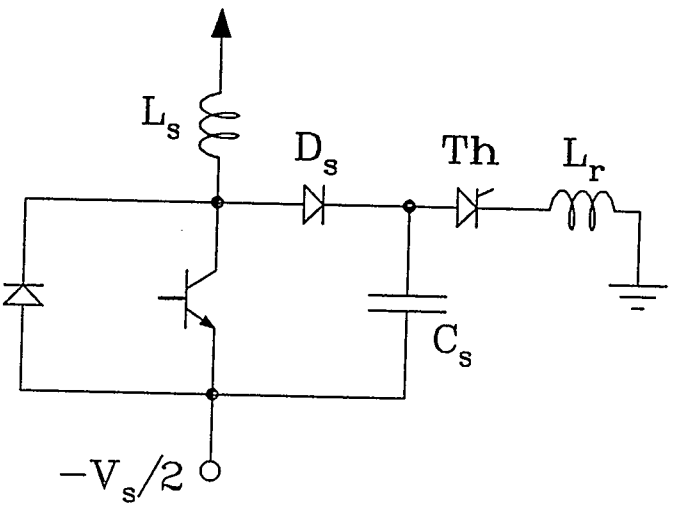


Figure 4.05. Additional switching devices to discharge C_s.

resulting from the discharge of C_s. A voltage clamping circuit can be used to help discharge the inductors, and this will reduce the overvoltage at turn-off[15]. A transformer is used to discharge the turn-on inductor, L_s, in the snubber described in Ref. [17]. Although the method is simple in design, it may be difficult to implement because additional gate drive and control logic is required for the auxiliary thyristors. Additional snubber devices may also be required to protect these thyristors. Implementing this snubber will require that the inverter be fed from a center-tapped DC supply.

A transformer may also be used as a passive element in an energy recovery circuit. In several snubbers, L_s is replaced with a transformer, so that the energy in L_s is recovered in the secondary winding of the transformer[1, 18]. Another approach is to replace the resistor R_s with a transformer, and connect the transformer secondary to the DC supply through a diode, as in a snubber proposed in Ref. [18]. This snubber is shown in figure 4.06. This approach is more practical as it will remove the energy from the capacitors as well as the inductors, and there can be more flexibility in the design of L_s. The transformers for these snubbers may be difficult to construct, and in both snubbers the voltages on the main switching devices may exceed V_s.

Another example of a passive resonant circuit is one described in [1]. This is shown in figure 4.07. In this circuit the energy in L_s and C_s is transferred to the capacitor C_o. When the transistor is switched off and V_{ce} increases, D_o is forward biased and the energy stored in C_o will be sent into the load via the DC supply

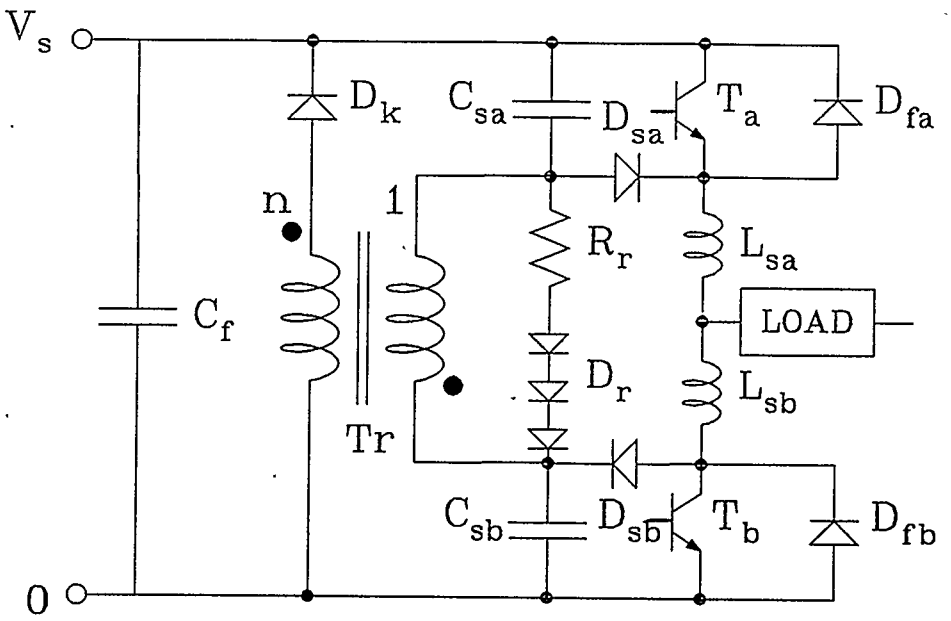


Figure 4.06. W. McMurray snubber circuit.

rail and another leg of the inverter. Another passive resonant snubber is proposed in Ref. [19]. This one is similar to an advanced version of the snubber described in Ref. [20]. The snubber described in Ref. [19] uses more parts. The snubber capacitor does not discharge through the inductor L_s, but through a separate inductor. These two inductors are designed separately for optimum snubber performance. The major disadvantage of this snubber is that it requires five diodes, each requiring a heatsink and possibly a diode snubber.

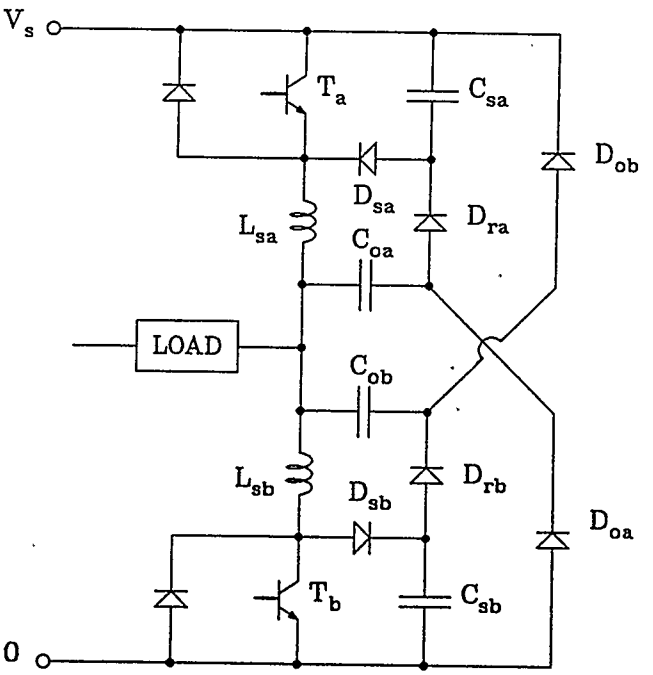


Figure 4.07. Snubber by B. W. Williams.

4.5. Snubber Circuit Design

4.5.1. Resistive Snubbers

This section will provide methods to select snubber components and to calculate the power loss in a resistive snubber. Note that the selection of C_s and L_s is universal for all snubbers. The only difference is that in a lossless snubber the values of these components will affect how energy is transferred in the circuit.

The following equations are used to determine the values of C_s and L_s:

$$C_s = \frac{I\ t_f}{2V_s}\ ;\quad L_s = \frac{V_s\ t_{on}}{I} \tag{4.3}$$

where,

C_s is the snubber capacitance
L_s is the snubber inductance
I is the maximum load current
V_s is the DC supply voltage
t_f is the transistor fall time at turn-off
t_{on} is the transistor turn-on time

These equations are derived in Appendix 1 and are available in several references on snubbers[1, 12, 13].

If C_s and L_s are chosen to be larger than the calculated values, the snubber is oversized. The snubber is undersized if these components are smaller than required. In a lossless snubber it becomes practical to use oversized components.

The energy dissipated in the resistor is the combined energy that is trapped in both the inductor and the capacitor. Using the basic equations for this energy, this will yield

$$W = \frac{1}{2} L_s I^2 + \frac{1}{2} C_s V_s^2. \tag{4.4}$$

This energy is dissipated in each switching cycle. Therefore, the power dissipation in the resistor can be found by multiplying this energy by the frequency at which the transistor will be switched.

$$P_R = \frac{1}{2} f_s (L_s I^2 + C_s V_s^2) \tag{4.5}$$

Note that the power dissipation will be constant regardless of the value of R_s.

The value of R_s is selected to provide a tradeoff between the rapid discharge of C_s and L_s and limiting the value of the overcurrent or overvoltage that the transistor will experience. C_s can be considered to be fully discharged in five time constants, i.e. $5R_sC_s$. Since the initial charge on the capacitor is V_s, the maximum overcurrent in the transistor is V_s/R_s. A similar situation applies to the inductor. The time constant for discharge is L_s/R_s, and the maximum overvoltage on the transistor will be IR_s.

The diode must be able to at least withstand the voltage V_s. However, since the diode is not always conducting, it need not be rated for the full current I. At higher frequencies, the diode current I_{ds} will approach I/2. It is recommended that D_s is a fast recovery diode. This will prevent a large diode recovery current from surging through the transistor at turn-on. Also, in some cases this current can cause the circuit to oscillate. This effect occurs most often in resonant snubbers.

4.5.2. Lossless Snubbers

After much research, an approximate set of criteria was developed for the design of resonant snubbers. Exact equations cannot be given for several reasons. First, the mathematical analysis of the circuit becomes too detailed for simple calculation of the circuit parameters. Second, there are many non-ideal effects in the circuit that defy analysis. Finally, many tradeoffs and adjustments must be made to optimize the final circuit. The Williams snubber is used for this example of snubber design.

The minimum values required for L_s and C_s are calculated as they are for a resistive snubber. To design the value of C_o, as well as adjusting C_s and L_s, the following equations are to be considered:

$$i_r = \frac{V_s}{Z}\sin(\omega t) \tag{4.6}$$

$$t_{rs} = \frac{1}{\omega_s}\left(\frac{\pi}{2} - \alpha\right) + t_{sd} \tag{4.7}$$

$$t_{sd} = \frac{1}{\omega}\cos^{-1}\left(\frac{-1}{n}\right) \tag{4.8}$$

where:

$$Z = \sqrt{\frac{L_s}{C_s}\frac{(n+1)}{n}}$$

$$\omega = \sqrt{\frac{n+1}{nC_sL_s}}$$

$$\omega_s = \frac{1}{\sqrt{L_sC_o}}$$

$$\alpha = \sin^{-1}\left(\frac{1}{\sqrt{n}}\right)$$

$$n = \frac{C_o}{C_s}$$

The maximum current in the transistor will be the sum of the load current and the snubber reset current, $I+i_r$. The snubber impedance, Z, must be high enough to insure that the maximum transistor current is not exceeded. The value of n must be greater than or equal to 1, to insure that C_s discharges fully. It was discovered experimentally that a value of n >>1 is desirable. This is documented in the next

section. The snubber reset time, t_{rs}, is determined by ω. Note that as a result of these equations Z and t_{rs} are inversely proportional. This means that by speeding up the snubber reset, the current stress on the transistor is increased. A tradeoff must be found between sensible values of C_s and C_o, reset time, transistor stress, and a reasonable value of L_s. Large inductors and capacitors are bulky and expensive, but the components are of no value if the snubber cannot meet desired specifications. It will be necessary to change component values so that acceptable values of Z and t_{rs} are obtained.

Selection of diodes is equally important in the design of a snubber. The diodes should always be of the fast recovery type, the faster the better. The diode recovery current will increase the transistor stress and may cause the snubber to oscillate. Select a diode with a maximum breakdown voltage of V_s, since this voltage may appear anywhere in the circuit. The RMS current can be approximated to $I/\sqrt{2}$, since the diode can be expected to work at a 50 % duty cycle. For the diode D_o, its RMS current can be approximated by $I_{do} = V_s C_o f_s$. This equation assumes that the total charge stored on C_o will be discharged into the load via D_o each and every cycle. This equation does not take into account current from L_s which travels through $D_s - D_r - D_o$, so the calculated current may be low.

Using the above equations, and the specifications desired for the inverter, the following snubber components were selected.

C_s = 50A * 3 μs / (2 * 250V) = 0.3 μF.
L_s = 250V * 2 μs / 50 A = 10 μH.
$C_o = C_s$ = 0.3 μF.

The snubber was oversized by making $C_s = 1\,\mu F$. With the value of L_s given, Z = 4.5 Ω. This will result in a peak value of i_r = 56A. It also gives a value of ω = 447 214 rad/s and ω_s = 316 228. This will result in $t_{rs} = 7\ \mu s$. This is quite fast, however, the large current is of concern, since the devices are rated for 100A. To limit the peak value of i_r to 25 A, an impedance of 10 Ω is required. Using the given value of $C_s = 1\ \mu F$, this will result in $L_s = 50\ \mu H$. This results in t_{sd} = 15.7 μs. To allow for possible operation at up to 500V, L_s and Z were increased further. The final value of L_s was 100 μH. Also, the value of C_o was increased to 5 μF to improve the reliability of the circuit. This is discussed in section 4.6.3. As a result of the experimental work on this circuit, it is recommended that C_o be much larger than C_s to insure that C_s can discharge fully. With these component values, the circuit parameters are now as follows. Z = 22 Ω, giving a peak value of current of 22.4 A with V_s = 500 V. The snubber reset time, $t_{rs} = 47\ \mu s$. Although this does not give the desired 2:1 margin of safety, this is still an acceptable value. There is still room to modify and improve the snubber, however, financial and time constraints prevented further work on the circuit. In the next section the experimental results of the various snubber circuits developed will be presented. This will supplement the design information that has been developed, and demonstrates the complexity of lossless snubber networks.

4.6. Performance of Snubber Circuits

Three different snubber circuits were tested and compared. In this section the results of these test will be compared. As previously stated, these results are given as several oscillograms. Not only is the transistor voltage and current during switching observed, but waveforms for other snubber quantities are also observed. This will help to provide an understanding of how the snubber operates and how modifying component values affects overall performance.

One of the major difficulties with getting quality results was the difficulty in measuring current, especially above 20A. Since the transistor current is DC, a current transformer cannot be used. Also, most Hall effect devices do not respond well to the high frequency components of a signal, and therefore it is difficult to detect short duration transients which may be present and detrimental to circuit operation. For many situations, the current was measured using a current shunt. As these devices are sensitive to noise, it is often necessary to shield the device to get an accurate measurement. The output is observed on a differential scope. As with any differential amplifier, common mode noise is significant and should be reduced. This can be reduced if one side of the current shunt can be grounded. However, in many cases the shunt measured current in a portion of the circuit which was live, and neither side could be grounded. Since it was not always possible to ground one side of the current shunt, there was a substantial common mode component of the signal which distorted the output and gave poor results.

On the following pages are several oscillograms of various circuit waveforms which are described below. The first snubber described is the basic resistive snubber proposed by McMurray[12]. Then the Williams snubber [1] for both single transistor and two transistor operation will be examined. This snubber is then compared with the resonant snubber proposed in Refs. [1,. 18]. Finally, the results of using the Williams snubber in a single phase H-bridge inverter will be presented.

4.6.1. Basic Snubbers

The RLC snubber is simple to build and test, and it demonstrates the fundamentals of snubber protection. The oscillograms of figure 4.08 show V_{ce} and I_c for various component values in the snubber. Two things were observed. In figure 4.8a-4.8c, the necessity of L_s is demonstrated. These oscillograms are for transistor turn-on. Figure 4.8a shows what happens with no inductance. Note the very large current surge at turn on. The inductor L_s is needed to reduce this. In figure 4.08b it is seen that a saturable inductance is not practical for transistor protection, since a large current will saturate it quickly and render it useless. Figure 4.08c shows the waveforms with a 75 μH non-saturable (air core) inductor. Figures 4.08d-4.08f show the transistor at turn-off. Note that the voltage will exceed V_s temporarily at turn-off. This is caused by the discharge of inductor L_s as well as the turn on delay of the feedback diode D_f. It was observed that a capacitor value $C_s = 1\ \mu F$ was sufficient to limit the rise of transistor voltage.

Larger values of C_s were only slightly more effective in limiting the amount of voltage overshoot. In figure 4.08d-4.08f the results of using 3 different capacitor values are shown.

In figure 4.09, several oscillograms are presented which demonstrate the operation of the Williams snubber for one transistor. These oscillograms detail the operation of several sections of the snubber, showing both the expected waveforms and several non-ideal effects. In these waveforms, the distortion due to common mode noise in the current shunt is very significant.

The first waveform shows V_{ce} and I_c at turn-on. As the oscillogram shows, V_{ce} does not fully decrease to its saturation value, due to dynamic saturation. Also, I_c surges to a very high value and then returns to normal during a period of 1 μs. These effects are a problem because this current can push the transistor into its second breakdown mode, and the extra power dissipation can overheat the transistor. However, when a full bridge circuit is used, this current spike is absent since there is a path for the snubber energy to be discharged into the load. In Figure 4.14a it is seen that the dynamic saturation problem is not as severe as it appears to be. The dynamic saturation loss calculation assumed that at turn on V_{ce} would decline until $V_{ce} = 0.1V_s = 25$ V. However, the oscillograms show that V_{ce} falls to 5 V at turn-on, and from this value it declines slowly to 2 V. Again, common mode noise distorts these results since it was not always possible to ground one side of the current shunt.

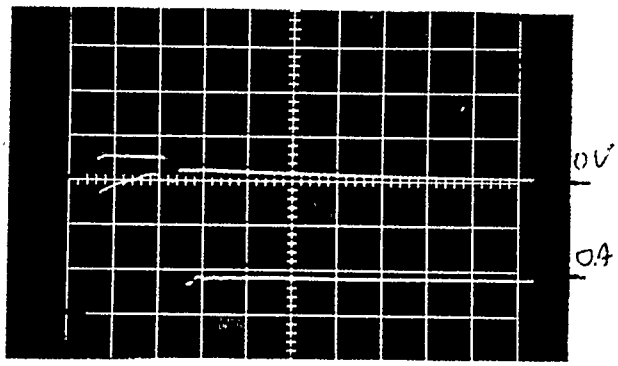


Figure 4.08a: L_s = 0. Top: V_{ce} 20V/div. Bottom: I_c 50A/div. Time: 10 µs/div.

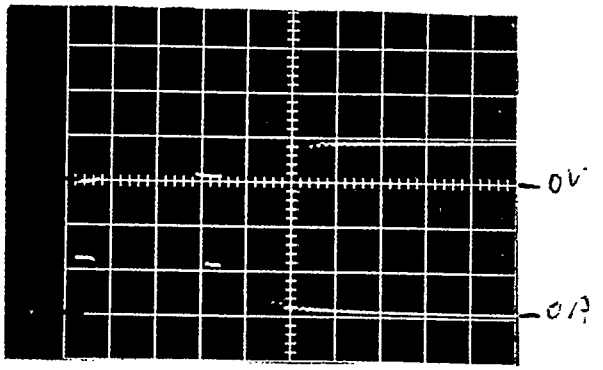


Figure 4.08b: Saturable L_s. Top: V_{ce} 20V/div. Bottom: I_c 50A/div. Time: 10 µs/div.

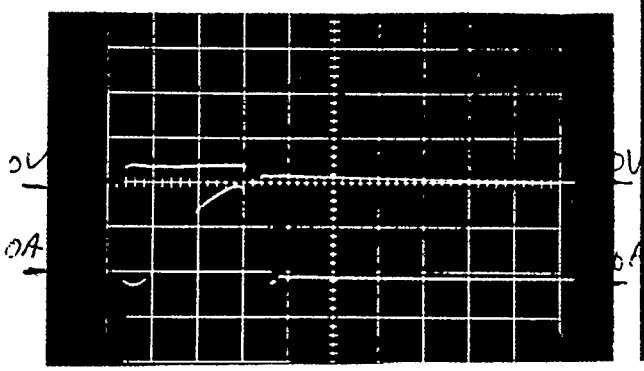


Figure 4.08c: L_s = 75 µH. Top: V_{ce} 20V/div. Bottom: I_c 50A/div. Time: 10 µs/div.

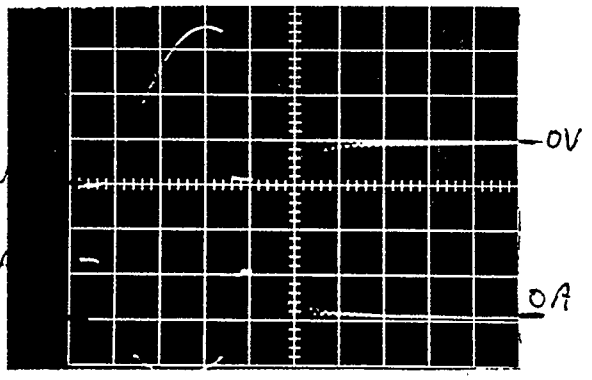


Figure 4.08d: C_s = 1 µ F. Top: V_{ce} 100V/div. Bottom: I_c 50A/div. Time: 10 µs/div.

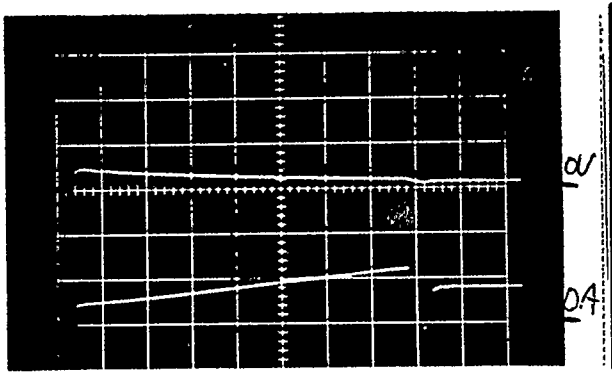


Figure 4.08e: C_s = 2 µ F. Top: V_{ce} 100V/div. Bottom: I_c 50A/div. Time: 10 µs/div.

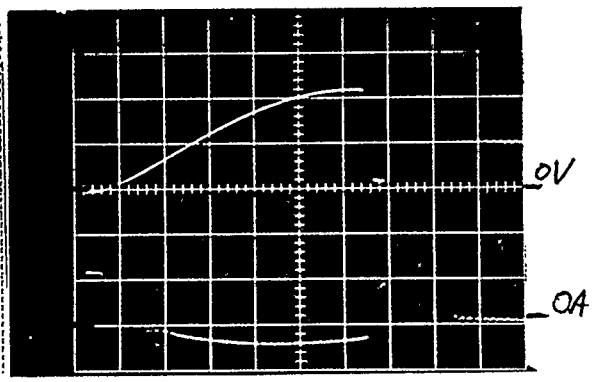


Figure 4.08f: C_s = 5 µ F. Top: V_{ce} 100V/div. Bottom: I_c 50A/div. Time: 10 µs/div.

Figure 4.08. RLC snubber results.

Figure 4.09b shows V_{ce} and I_c at turn-off. It can be seen that the voltage rise

is very slow, except for a voltage spike right at turn-off. This spike is caused by stray inductance in the circuit as well as the turn-on delay of diode D_s. Since this voltage spike remains lower than V_s, it is only a problem if it causes excess power dissipation.

Figure 4.09c shows V_{cs} and V_{co} for one entire switching cycle. Although C_s discharges into C_o, as expected, the voltage begins ringing when the transistor is switched off. This is caused by the lack of a second inverter leg, so the energy cannot be switched into the load, as desired for this snubber. In the next section it will be seen that these voltages do not oscillate as much. Another possible cause of these oscillations is the reverse recovery of the diodes. When they recover, the current pulse in the resonant circuit excites oscillations that do not die down quickly. This indicates the need for fast recovery diodes in snubber applications. These oscillations were not evident with single phase operation. This would indicate that when the stored energy can be released into the load it reduces oscillation in the circuit. Also, when single phase operation was implemented, a current probe became available and this eliminated the problem with common mode noise.

Figure 4.09d shows I_{co} and I_c for an entire switching cycle. These waveforms were greatly affected by common mode noise, since it was necessary that the shunt was floating. In the next section, the results of using this snubber on a full inverter leg are discussed. As well, the results of testing another snubber, proposed by W. McMurray, will also be presented.

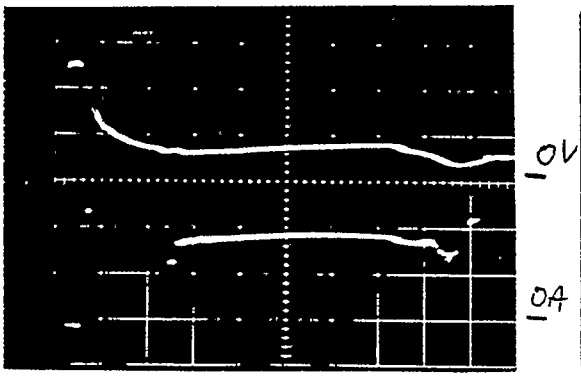


Figure 4.09a: Turn-on.
V_s = 150V, f_s = 5kHz, I_L = 100A.
Top: V_{ce} 100V/div. Bottom: I_c 50A/div.
Time: 1 µs/div.

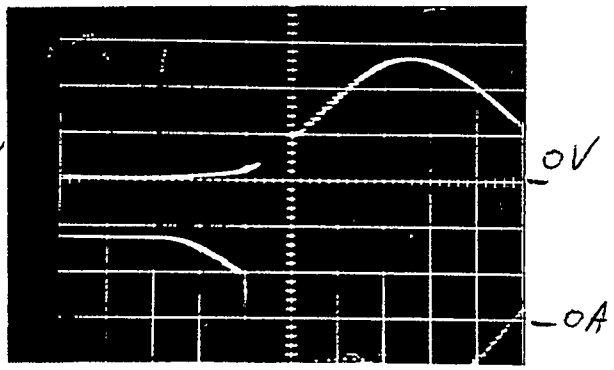


Figure 4.09b: Turn-off.
V_s = 150V, f_s = 5kHz, I_L = 100A.
Top: V_{ce} 100V/div. Bottom: I_c 50A/div.
Time: 10 µs/div.

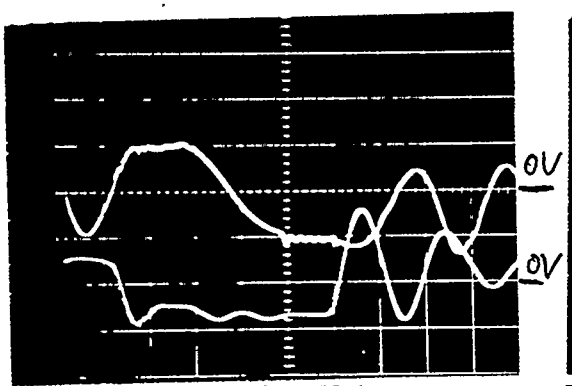


Figure 4.09c: Capacitor Voltages.
V_s = 150V, f_s = 10kHz, I_L = 100A.
Top: V_{co} 50V/div. Bottom: V_{cs} 100V/div. Time: 10 µs/div.

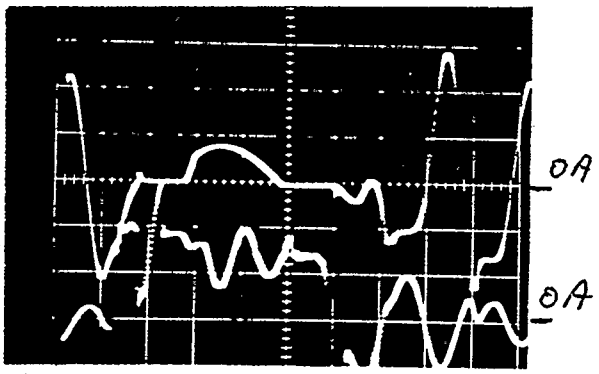


Figure 4.09d: Snubber Currents.
V_s = 150V, f_s = 10kHz, I_L = 100A.
Top: I_r 10A/div. Bottom: I_c 50A/div.
Time: 10 µs/div.

Figure 4.09. Results for Williams snubber with one transistor.

4.6.2. Resonant Snubber with Dual Transistor Operation

A single inverter leg was constructed using two complementary switched transistors. This setup was used to evaluate the performance of two different snubbers, the Williams snubber and the McMurray snubber. The circuits were those shown in figures 4.06 and 4.07. Current was switched on and off into a

40mH inductor to evaluate the snubbers with an inductive load. One transistor carried the current, and at turn off this current was then conducted by the feedback diode of the opposite transistor. The current was essentially DC, but the large inductance caused voltage spikes at turnoff that the snubber had to absorb.

The waveforms for the Williams snubber were essentially the same as those described in the previous section. For this reason, only the waveforms of the McMurray snubber are shown in this section. Using these, a comparison of the two snubbers may be made. From the observations made, the optimum snubber of each type was constructed and a single phase bridge circuit was constructed by placing a load between the two inverter legs. This made it possible to compare both snubbers under identical test conditions.

In figure 4.10a and 4.10b, the oscillograms of the turn-off waveforms are shown. Figure 4.10a is for the transistor on the positive rail, and figure 4.10b is for the transistor on the ground rail of the DC supply. In the waveform for V_{cea} the smooth rise of voltage due to snubber action can be seen. The only exception to this smooth rise is the voltage spike that occurs immediately when turn-off begins. This is caused by the delay in the turn-on of diode D_{sa}. Also, stray inductance in the D_s–C_s loop would also contribute to this voltage spike. A large amount of noise and oscillation can be seen in the transistor current. This noise is due in part to oscillations set up by the sudden switching of a diode or transistor. The problems mentioned earlier with current shunt measurements are also evident in these oscillograms. Note that the transistor voltage, V_{ce}, exceeds the DC supply

voltage, V_s for transistor T_a. In some cases $V_{cea} = 2V_s$. This effect is not seen for transistor T_b. The reasons for the asymmetry of the results is that the two snubber capacitors discharge via different paths, and transistor T_a carries the bulk of the load current, while transistor T_b conducts primarily through its feedback diode.

Figures 4.10c and 4.10d are the waveforms for transistor turn-on. In the voltage waveform, the effect of dynamic saturation can be seen. Figure 4.10c shows the turn-on for transistor T_a. and the turn-on waveforms for transistor T_b are given in figure 4.10d. Notice the dynamic saturation of this transistor. Also note that there are heavy oscillations in these waveforms, especially for I_{cb} at turn-on. Since, for this test, a single inverter leg switched DC current into an inductive load, the feedback diode was turned on rapidly, and this could cause both circuit oscillations as well as common mode noise in the oscilloscope. When this snubber was used in one leg of a single phase inverter, performance improved somewhat. However, the voltage overshoot problem still remained.

In figure 4.11a, a comparison of V_{csa} and V_{csb} is provided. This shows the different voltage overshoot between the two transistors. Figures 4.11b and 4.11c show the effect of putting an airgap in the transformer core. Figure 4.11b is I_p and I_s with no airgap, whereas figure 4.11c shows these quantities with an airgap in the core. The airgap keeps the transformer from saturating and therefore permits a much better transfer of power, at the expense of greater leakage in the transformer. A good indication of the flaws of this snubber circuit is provided by

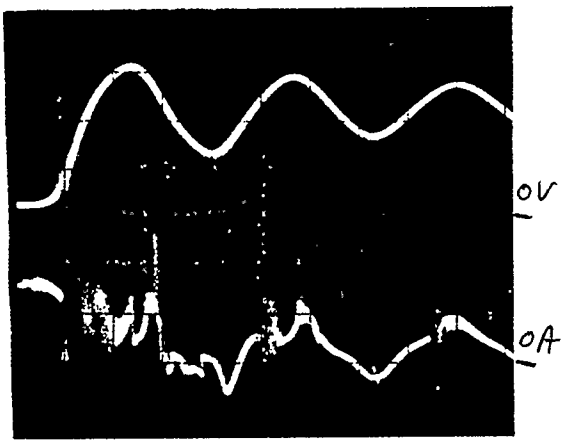


Figure 4.10a: T_a Turn-off.
V_s = 100V, f_s = 5kHz, I_L = 70A. Top: V_{ce} 50V/div. Bottom: I_c 50A/div. Time: 10 μs/div.

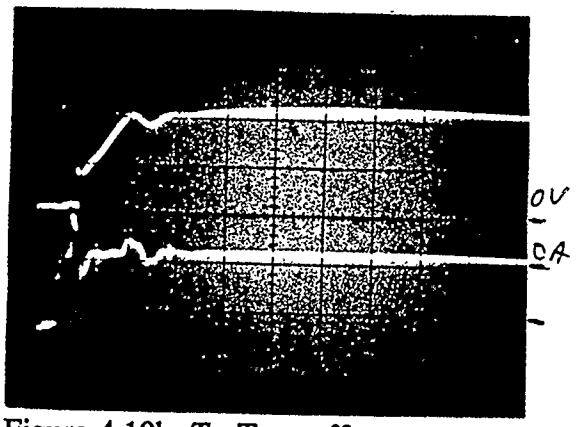


Figure 4.10b: T_b Turn-off.
V_s = 100V, f_s = 1kHz, I_L = 70A. Top: V_{ce} 50V/div. Bottom: I_c 50A/div. Time: 50 μs/div.

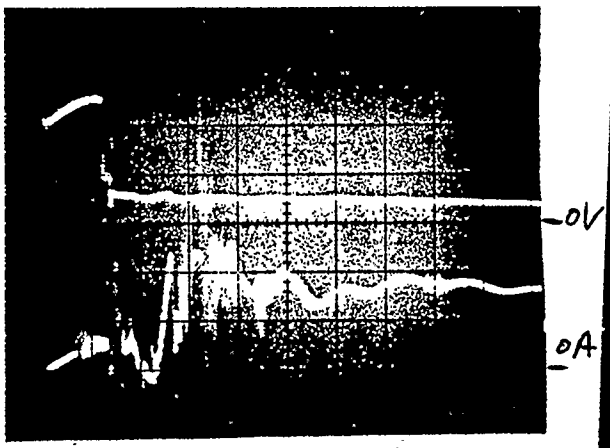


Figure 4.10c: T_a Turn-on.
V_s = 100V, f_s = 5kHz, I_L = 70A. Top: V_{ce} 50V/div. Bottom: I_c 50A/div. Time: 10 μs/div.

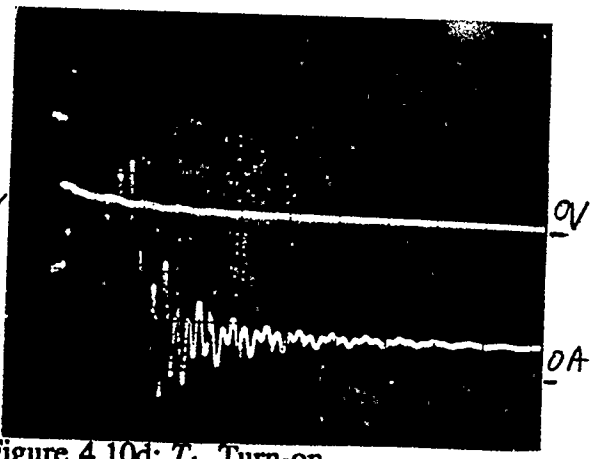


Figure 4.10d: T_b Turn-on.
V_s = 100V, f_s = 1kHz, I_L = 70A. Top: V_{ce} 50V/div. Bottom: I_c 50A/div. Time: 50 μs/div.

Figure 4.10. Transistor waveforms in McMurray snubber.

figure 4.11d, which shows V_{cea} and I_r. In the figure, V_{cea} exceeds V_s, while I_r is quite large. This would cause a lot of power dissipation in the reset resistor, which would defeat the purpose of having a resonant snubber.

As stated earlier, the only problem encounted in the Williams snubber was the the failure of several transistors and diodes. It was speculated that this could be

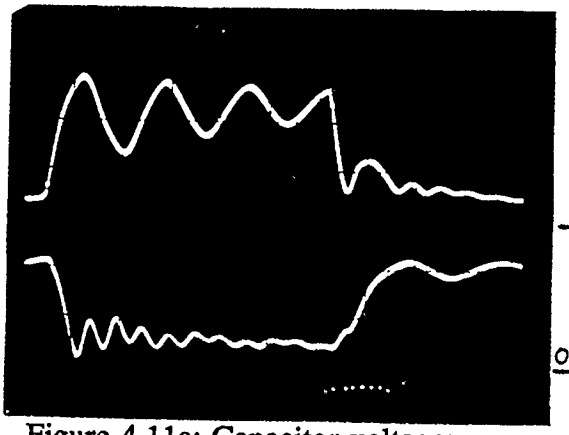


Figure 4.11a: Capacitor voltages. V_s = 100V, f_s = 5kHz, I_L = 70A. Top: V_{csa} 50V/div. Bottom: V_{csb} 50V/div. Time: 20 µs/div.

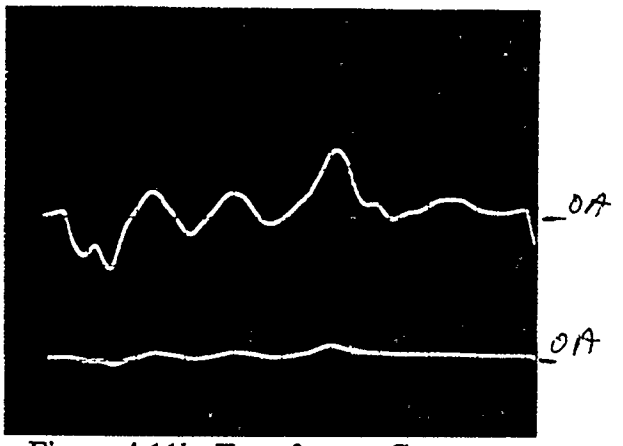


Figure 4.11b: Transformer Currents. V_s = 100V, f_s = 5kHz, I_L = 70A. Top: I_p 5A/div. Bottom: I_s 1A/div. Time: 20 µs/div.

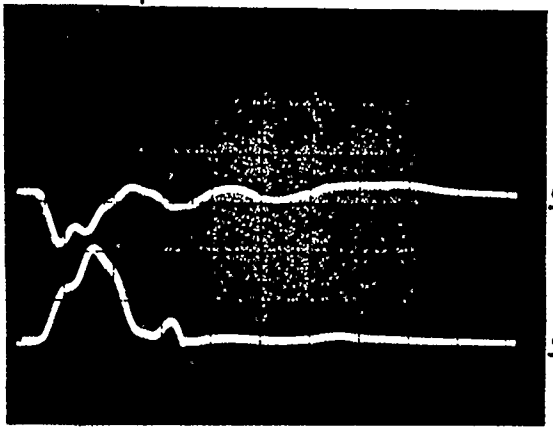


Figure 4.11c: Transformer Currents with airgap in core. V_s = 75V, f_s = 5kHz, I_L = 50A. Top: I_p 10A/div. Bottom: I_s 5A/div. Time: 20 µs/div.

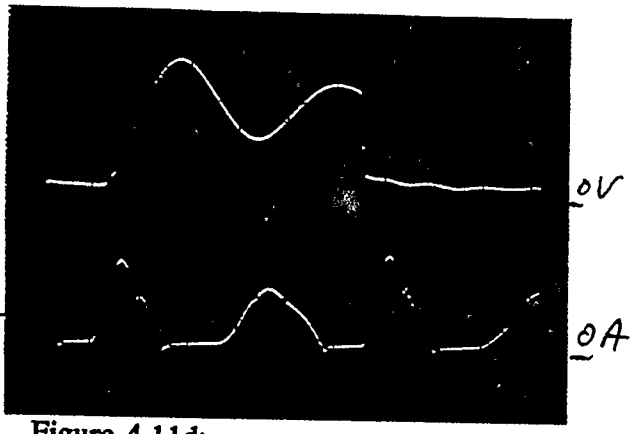


Figure 4.11d: V_s = 100V, f_s = 10kHz, R_L = 12.5Ω. Top: V_{ce} 50V/div. Bottom: I_r 20A/div. Time: 10 µs/div.

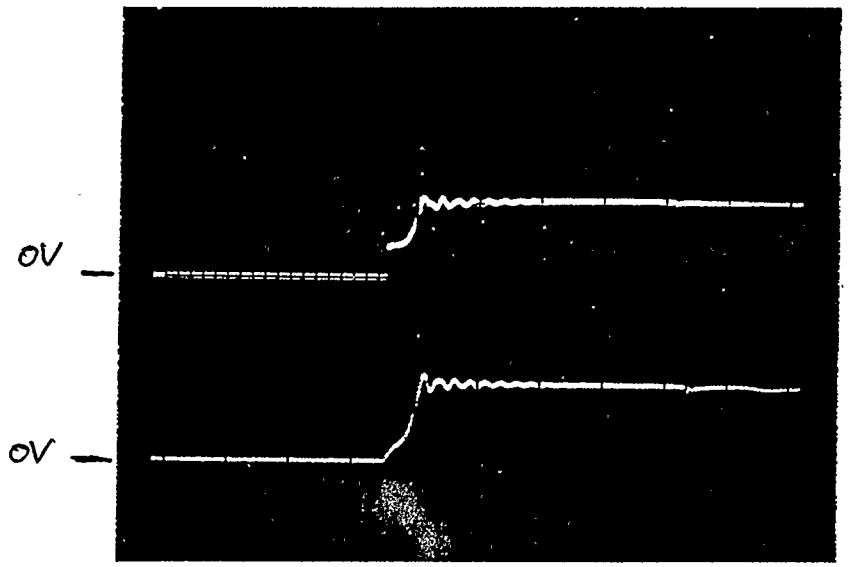
Figure 4.11. McMurray snubber oscillograms.

the result of diode recovery current through D_o–D_r–D_s–T. However, a careful examination of the diode currents, with a Tektronix A6303 current probe which had become available, showed very little diode recovery current. Using additional inductances to limit this current did not prevent transistor failures. However, it was noticed that the capacitor C_s did not fully discharge to zero volts. Since this

caused a sudden rise in V_{ce} at turn off, this was determined to be the cause of the transistor failures. The reason C_s did not discharge fully is that it had to discharge into C_o. It seems that C_o could not absorb the charge on C_s quickly enough. Capacitor C_o, which was 1 μF, was replaced with a 5 μF capacitor. The result of this is shown in figure 4.12. Notice that the voltage rise at turn-off is slower, without a sudden jump in voltage. The next section deals with the results of operating a single phase bridge inverter with this snubber where C_o is 5 μF.

4.6.3. Resonant Snubber with Single Phase AC Operation

When both the McMurray and Williams snubbers were operated



Inductive Load
V_s = 60V, f_s = 200Hz. Top: V_{ce} (C_o = 1 μF) 50V/div. Bottom: V_{ce} (C_o = 1 μF) 50V/div. Time: 50 μs/div.

Figure 4.12. Effect of changing C_o in Williams snubber.

simultaneously in a single phase inverter, it was clear that the Williams snubber provided a more satisfactory performance. The overvoltage on the transistors was minimal, and the current oscillations were reduced from their previous levels. In this section, the final oscillograms demonstrating the operation of this snubber at 250V will be presented.

In figure 4.13a, V_{cea} and I_{ca} are shown for 250V, 50A operation at 2 kHz. As can be seen, there is some voltage overshoot at turn-off, but this is only on the order of about 10%. The rise of V_{ce} is controlled well, since C_s is discharged at turn-off. In figure 4.13b, these quantities for transistor turn-on are shown. As with all turn-on waveforms, dynamic saturation is evident. However, the voltage rapidly falls to 5V, while the current rises smoothly, which results in reasonably low power dissipation at turn on. These results indicate that this snubber provides adequate protection for these transistors during switching.

In figure 4.14a, I_r and V_{ce} are shown for one switching cycle. This is to demonstrate the operation of the snubber as well as give an indication of the overcurrent in the transistor due to snubber action. Figure 4.14b compares the voltages V_{cs} and V_{co} for a switching cycle. It can be seen that C_s discharges fully into C_o.

4.7. Conclusions

The existence of large voltage and current transients in a power electronics circuit makes device protection a necessity. In this chapter, several requirements

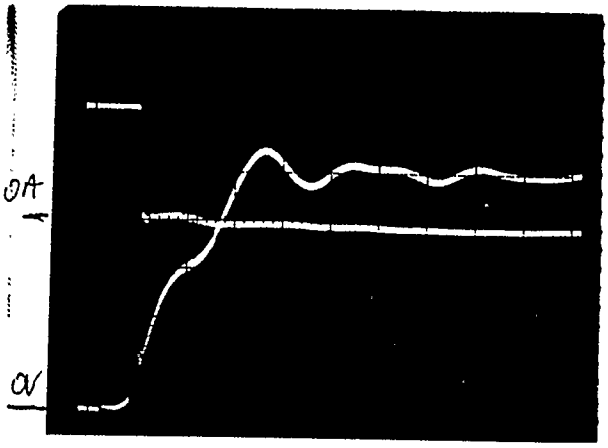


Figure 4.13a: Turn-off waveforms. V_s = 250V, f_s = 2kHz, I_L = 50A. Top: I_c 20V/div. Bottom: V_{ce} 50A/div. Time: 5 µs/div.

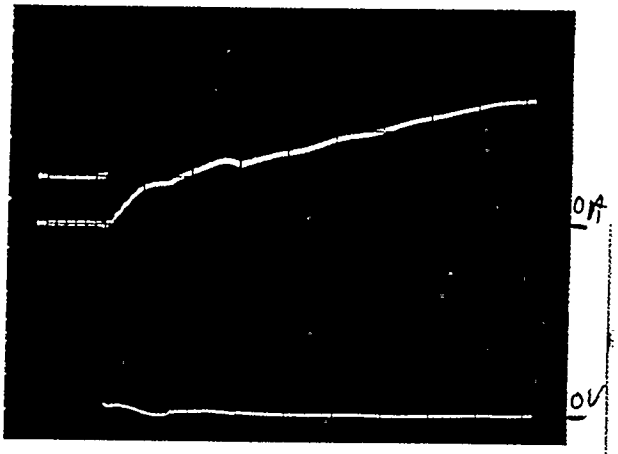


Figure 4.13b: Turn-on waveforms. V_s = 250V, f_s = 2kHz, I_L = 50A. Top: I_c 20V/div. Bottom: V_{ce} 50A/div. Time: 5 µs/div.

Figure 4.13. Williams snubber in single phase inverter.

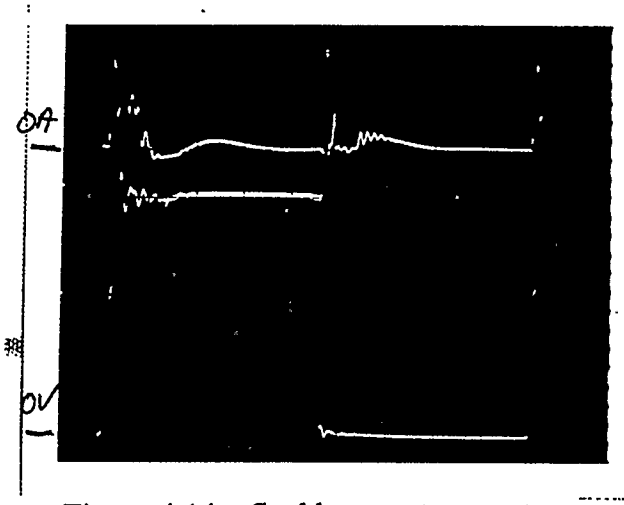


Figure 4.14a: Snubber reset current. V_s = 250V, f_s = 2kHz, I_L = 50A. Top: I_r 20V/div. Bottom: V_{ce} 50A/div. Time: 50 µs/div.

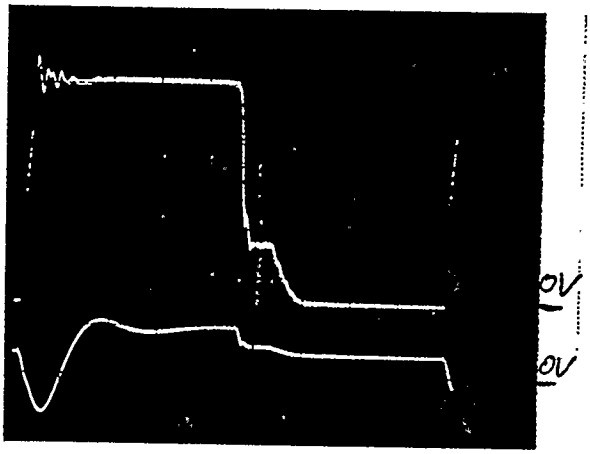


Figure 4.14b: Capacitor Voltages. V_s = 250V, f_s = 2kHz, I_L = 50A. Top: V_{cs} 50V/div. Bottom: V_{co} 50V/div. Time: 50 µs/div.

Figure 4.14. Operation of Williams Snubber.

for transistor protection were reviewed and specific requirements for protection of KS224510 Power Darlington transistors were considered. The large collection of

information on snubbers was reviewed and summarized. Two of these snubbers were designed, built and tested. From this a general set of guidelines for lossless snubber design was developed and is presented in section 4.5. It was found that the snubber described by B. W. Williams was the most appropriate for this application. This snubber was modified to suit the needs of the transistors used. Some problems with this snubber were identified and solved.

As the first section of this chapter indicated, a good snubber alone is not enough for adequate transistor protection. Proper heat sinks and cooling are needed to avoid thermal problems. Also, the DC input should be filtered and perhaps be equipped with surge suppression to eliminate input noise and voltage spikes. The control logic could have numerous failsafe features incorporated to turn the transistor drives off in the event of an output short circuit or other similar fault. It would also be helpful to minimize the effects of a power device failure to prevent damage to the rest of the system. Some new base drive methods are being developed which react to the transistor voltage and current to keep the transistor within its safe operating areas.

The design presented in this chapter incorporated as many of these techniques as time allowed. With the transistor protected in this manner, several switching power circuits can be constructed. One particular application, a three phase voltage source inverter, is presented in Appendix B. In the next chapter the operation of a single phase bridge inverter is described. Since this operation requires both adequate base drive and transistor protection, this inverter is an excellent example

of the end result of the research into these two areas. It is typical of an application of power BJTs or other switching devices.

CHAPTER 5

CONCLUSIONS

5.1. Single Phase Inverter

One possible application of power BJTs is in an inverter. An inverter is used to convert a DC voltage to an AC voltage source. It accomplishes this by switching the DC voltage on and off, creating a square wave. This on-off switching is accomplished by the dual transistor "leg" that is described in Chapter 4. Depending on which transistor is on, the load alternately is exposed to the positive DC supply or to ground. By placing the load between two such legs, and coordinating the switching of all transistors correctly, a single phase inverter is constructed. By switching the transistors, the voltage across the load will either be $+V_s$ or $-V_s$. The result of this is a square wave AC voltage applied to the load of frequency f_s, the frequency at which the transistors are switched, and an RMS voltage of $V_s / \sqrt{2}$.

Figure 5.01 shows the schematic of a single phase bridge inverter. This diagram shows the two legs of the inverter, with the base drive and snubber circuits excluded. When transistors 1 and 4 are turned on, the voltage across the load is positive. When transistors 2 and 3 are turned on, the voltage across the load will be negative. These pairs of transistors are controlled simultaneously. The frequency at which these transistors are switched from one pair to the other

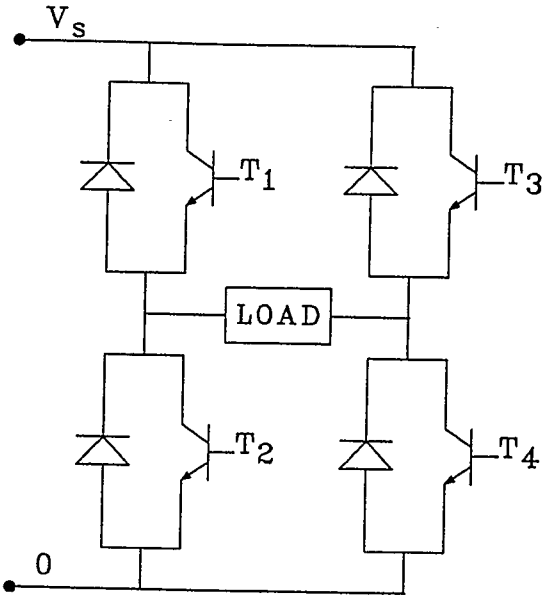
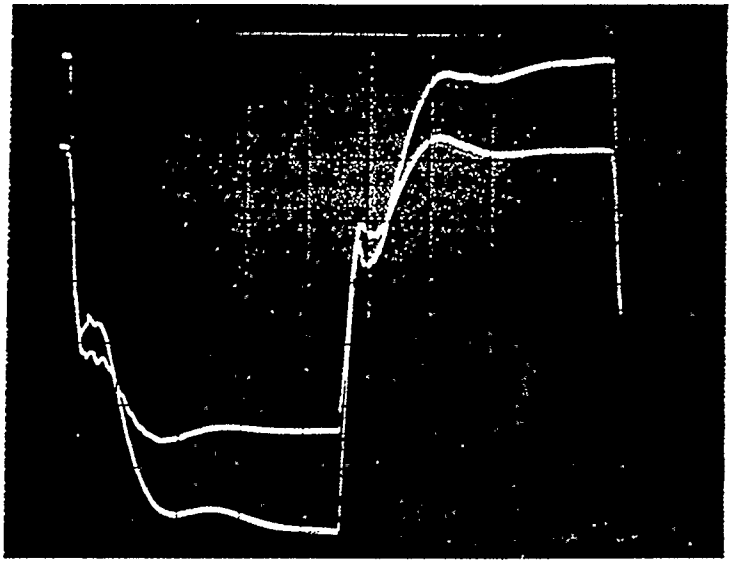


Figure 5.01. Single phase inverter

determines the frequency of the applied voltage to the load. As an additional protection measure, a short delay is incorporated when a transistor turns on. This delay allows the other transistor on the leg ample time to turn off. This will prevent a feedthrough fault from occurring in the circuit.

In figure 5.02 the output waveforms of the inverter are given. These waveforms show the voltage and current in a resistive load that is fed by this single phase inverter. When the load is inductive, the current will be closer to being sinusoidal, since the inductance will help remove harmonics. Various improvements can be made to this circuit to provide an output that is approximately sinusoidal. Note that in order to implement these improvements, as well as other control techniques discussed in this chapter, it is necessary to have adequate base and protection for the transistors. This will make it possible to switch the devices rapidly in a variety of load conditions.



Inverter Output Voltage and Current
I_{load} = 50 A. f_s = 2000 Hz. V_s = 250 V. Upper: V_{out} 50 V/div.
Lower: I_{load} 20 A/div. Time: 50 μs/div.

Figure 5.02. Output of single phase inverter

5.2. Summary

To implement the base drive of the transistors, several methods were considered. In a base drive, parameters such as speed, efficiency, size, cost, and safety features are all considered. Not all these may be implemented, since cost and size may limit how many other features may be incorporated. The base drive for this project was fast and efficient, but very few protection features were added. To keep the base drive from becoming overly complex no automatic shutdown or overload detection features were implemented. The base drive circuit uses a complementary pair of power mosfets to switch the transistor on or off. Additional components are used to shape the base current pulse to make it closer to the ideal

base drive current pulse. Some experimental results were provided to show that this base drive operates within the desired specifications. Base drive isolation was provide by using an isolated power supply and grounding the base drive and supply to the emitter of the power transistor. The base drive was optimized after some experimental work to determine the effect of various components on the base drive effectiveness. The design criteria developed for a base drive circuit is reviewed in section 3.4.1.

For transistor protection, several resonant snubbers were examined. Several active and passive snubbers described in the available literature were considered. This literature was reviewed and summarized in this thesis. Two passive resonant snubbers were designed, built, tested and compared in this thesis. It was found that one snubber, described by B. W. Williams, was far superior for this particular application. Design considerations were examined in detail for this snubber. This snubber was constructed and tested under expected operating conditions. Much time was spent getting this snubber to perform properly. Some flaws in the snubber were identified and corrected. Although the snubber is lossless, it tends to resonate. and device non-idealities made proper operation difficult to obtain. The snubber design criteria presented in this thesis may be applied to other snubbers of this type.

The design of the snubber includes several factors. First, C_s and L_s must be designed to provide adequate protection of the devices. The other components are then selected to discharge C_s and L_s in the required time period. There must be

some tradeoffs made in the values of these components to strike a balance between the speed of snubber reset and the additional loading on the devices due to snubber action. Finally, the maximum voltage and current at various points in the snubber circuit must be calculated to determine the ratings of diodes and other snubber components.

Also related to transistor protection is the problem of heat dissipation in the transistor. The thermal requirements of the transistors are determined, and an adequate heat sink is selected. It is recommended that some form of forced convection, (i.e. cooling fans or chill blocks) be used, since the equipment will very likely be enclosed in a cabinet, making cooling by natural convection difficult.

5.3. Future Considerations in Research

Earlier a single phase inverter was described. If the inverter is expanded to three legs, a three phase inverter may be constructed. This has many useful applications in AC drives. Appendix B describes a three phase voltage source inverter. If the design of the inverter is such that it can be operated at the speeds necessary for pulse width modulation, then a variety of control methods may be implemented. Two that are of interest are a "constant volts/hz" controller and field oriented control.

A constant volts/Hz controller is the simplest. It maintains the ratio of RMS voltage at the output to the frequency at a constant value. This will result in the motor operating smoothly in its constant torque region at speed less than the base

speed. (The base speed is the rated speed of the motor at 60 Hz.) The controller is designed such that at frequencies above that of the base speed, the voltage is overmodulated, and the waveform diverges from true PWM towards a simple square wave. In this region the voltage becomes constant, and the motor operates in the constant power region. With this controller, the armature current of the motor remains relatively constant. This control method can be improved by using feedback of motor speed and armature current. Also, the armature voltage and current can be used to estimate the airgap flux, which can then be used in feedback with a bang bang controller.

An alternate control method is field oriented control. The principle of this control method is to convert the rotating voltage and current of the motor to direct and quadrature axis components. Since these are stationary components, the same control algorithms used for a DC machine may now be used to control the inverter. The D and Q axis components are then converted back to rotating, i.e. three phase sinusoidal components and then converted to PWM signals and sent to the inverter. This control method gives a very good transient response, and would be suitable for applications where the load conditions vary constantly.

With a good control algorithm and an inverter using a PWM controller, many control methods can be used. Many modern controllers implement a suitable control algorithm with a microprocessor based system. An inverter can then be used to convert the output to the high voltage and current needed in a motor. In this arrangement it can be said that the microprocessor is the brains of the system

and the power electronics is the muscle. Power electronic switching devices are equally as effective in other types of equipment as well. DC/DC converters, rectifier/inverter units in HVDC transmission, and power line filtering equipment all use power semiconductor switching devices. Proper use if the switching devices will greatly improve the reliability of the equipment. This implies that both adequate base drive and sufficient protection are implemented.

REFERENCES

1. B.W. Williams, *Power Electronics: Devices, Drivers and Applications.* Hong Kong: MacMillan, 1987.

2. Michael S. Adler, Scott R. Westbrook, "Power Semiconductor Switching Devices - A Comparison Based on Inductive Switching," *IEEE Transactions on Electron Devices* Vol. ED-29, no. 6, pp. 947-951 June 1982.

3. Powerex, Incorporated, *Powerex Power Semiconductor Data Book.* Youngwood, Pennsylvania: Powerex, Incorporated, October, 1987.

4. Fred C. Lee, "Bipolar-FET Combinational Devices," in *MOSPOWER Applications*, Siliconix Incorporated, Santa Clara, CA 1984. pp. 6-130 to 6-134.

5. Hoang Le-Huy, Philippe Viarouge, Yves Jean, "Power Transistor Drive Circuits Using Power Mosfets," *Transactions on Industry Applications*, pp. 774-781 IEEE, 1982.

6. S.B. Dewan, G.R. Slemon, A. Straughen, *Power Semiconductor Drives.* Toronto: Wiley Interscience, 1985.

7. Bimal K. Bose, "Motion Control Technology - Present and Future," *IEEE Transactions on Industry Applications* Vol. IA-21, pp. 1337-1342 Nov/Dec 1985.

8. Westinghouse Electric Corporation, *Westinghouse Isolated Power Modules Data Book.* February 1985.

9. Westinghouse Electric Corporation, *Westinghouse Silicon Power Transistor Handbook.* 1967.

10. Sorab K. Ghandhi, *Semiconductor Power Devices.* New York: John Wiley and Sons, 1977.

11. Angelo Ferraro, "An Overview of Low-loss Snubber Technology for Transistor Converters," *IEEE Power Electronics Specialist Conference,* pp. 466-477 IEEE, 1982.

12. William McMurray, "Selection of Snubbers and Clamps to Optimize the Design of Transistor Switching Converters," *IEEE Transactions on Industry Applications* Vol. IA-16, no. 4, pp. 513-523 July/August 1980.

13. K. S. Rajashekara, Joseph Vithyathil, V. Rajagopalan, "Protection and Switching-Aid Networks for Transistor Bridge Inverters," *IEEE Transactions on Industrial Electronics* Vol. IE-33, no. 2, pp. 185-192 May 1986.

14. Tore Undeland, Frode Jenset, Arne Steinbakk, Terge Rogne, Magnar Hernes, "A Snubber Configuration for both Power Transistors and GTO PWM Inverters," *Power Electronics Specialist Conference,* pp. 42-53 IEEE, 1984.

15. Franz C. Zach, Karl H. Kaiser, Johann W. Kolar, Franz J. Haselsteiner, "New Lossless Turn-on and Turn-off (Snubber) Networks for Inverters, Including Circuits for Blocking Voltage Limitation," *IEEE Transactions on Power Electronics* Vol. PE-1, no. 2, pp. 65-75 April 1986.

16. Johan C. Bendien, Heinz van der Broeck, Gert Fregien, "Recovery Circuit for Snubber Energy in Power Electronic Applications with High Switching Frequencies," *IEEE Transactions on Power Electronics* Vol. PE-3, no. 1, pp. 26-30 January, 1988.

17. Joachim Holtz, Samir Fahim Salama, "High-power Transistor PWM Inverter with Complete Switching Energy Recovery," *International Conference on Electrical Machines* Vol. 3, pp. 995-998 Tech. Univ. Munchen, Sept. 1986.

18. W. McMurray, "Efficient Snubbers for Voltage Source GTO Inverters," *IEEE Transactions on Power Electronics* Vol. PE-2, no. 3, pp. 264-272 July 1987.

19. P.O. Lauritzen, H.A. Smith, "A Nondissipative Snubber Effective Over a Wide Range of Operating Conditions," *IEEE Power Electronics Specialist Conference,* pp. 345-354 June 6-9, 1983.

20. B. W. Williams, "High-voltage High-frequency Power Switching Transistor Module with Switching-aid-circuit Energy Recovery," *IEE*

Proceedings, Pt B Vol. 131, no. 1, pp. 7-12 January 1984.

21. David B. Bell, "Designing Optimal Base Drive for High Voltage Switching Transistors," *Proceedings of Powercon 7* Vol. F1, pp. 1-12 Power Concepts, Inc., 1979.

22. R.B Prest, J.D. Van Wyk, "Base Drive for High Current Low Loss Bipolar Power Transistor Switches," *Power Electronics Specialist Conference*, pp. 442-452 IEEE, 1986.

23. K. Rischmuller, "An Improved Base Drive Method Eliminates Switching Aid Networks in Transistorized High Power Converter Circuits," *Proceedings of Powercon 8* Vol. G1-1, pp. 1-9 Power Concepts, Inc, 1981.

24. P.H. Swanepoel, J.D. van Wyk, J.J. Schoeman, "Transformer Coupled Direct Base Drive Technology for High Power, High Voltage, Bipolar Transistor PWM Converters," *IEEE IAS Conference Record*, pp. 906-913 IEEE, 1987.

25. Warren Schultz, "Speeding Up the Very High Voltage Transistor," *Powerconversion International* Vol. 10, no. 2, Intertec Communications, February 1984.

26. W.R. Skanadore, "Understanding and Using Third-Generation Bipolar Switching Transistors," *POWERCONVERSION INTERNATIONAL* Vol. 10, no. 9, pp. 26-39 Intertec Communications, September 1984.

27. Warren Schultz, "Dynamic Saturation," *POWERCONVERSION INTERNATIONAL* Vol. 9, no. 9, Intertec Communications, October 1983.

28. Edward S. Yang, *Fundamentals of Semiconductor Devices*. New York: McGraw-Hill, 1978.

29. Harry A. Schafft, "Second Breakdown-A Comprehensive Review," *Proceedings of the IEEE* Vol. 55, no. 8, pp. 1272-1288 IEEE, August 1967.

30. Warren Schultz, "Baker Clamps: Traditional concepts Updated for Third Generation Power Transistors," *Powerconversion International* Vol. 10, no. 7, pp. 40-45 Intertec Communications, July/August 1984.

31. Dale Tardiff, T. H. Barton, "A Summary of Resonant Snubber Circuits for Transistors and GTOs," *IEEE IAS Conference Record* Vol. 1, pp. 1176-1180 Oct. 1989.

32. Joseph H. Rockot, "Losses in High-Power Bipolar Transistors," *IEEE Transactions on Power Electronics* Vol. PE-2, no. 1, pp. 72-79 IEEE, January 1987.

33. M. H. Pong, R. D. Jackson, "Computer-aided Design of Power Transistor Inverter Snubber Circuits," *IEE Proceedings, Pt. B* Vol. 134, no. 2, pp. 69-78 March 1987.

34. D. M. Divan, "The Resonant DC Link Converter-A New Concept in Static Power Conversion," *IAS Annual Meeting*, pp. 648-656 IEEE, 1986.

35. G.L. Skibinski, D.M. Divan, "Characterization of Power Transistors Under Zero Voltage Switching," *IEEE IAS Conference Record*, pp. 493-503 IEEE, 1987.

36. M. Kheraluwala, D. M. Divan, "Delta Modulation Strategies for Resonant Link Inverters," *Power Electronics Specialist Conference*, pp. 271-278 IEEE, 1987.

APPENDIX A

Derivation of Snubber Equations

The equations provided by B.W. Williams to describe his snubber are derived in this appendix. The following diagram shows this snubber. First the equations for transistor turn-on are derived. The following initial conditions are assumed:

$$V_{co} = 0;\ V_{cs} = V_s;\ I_{ls} = 0.$$

Assuming linear current rise at turn on,

$$i_t = \frac{I\ t}{t_{on}} = i_{ls},$$

and,

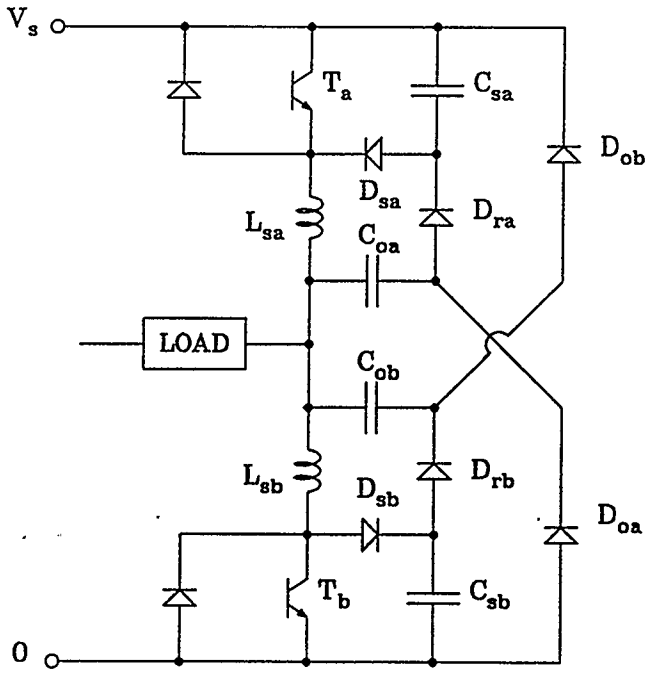


Figure A.01. Williams Snubber.

$$v_{ls} = L_s \frac{di_{ls}}{dt} = \frac{I\,L_s}{t_{on}}$$

To insure that $v_{ce} = 0$, it is necessary that $v_{ls} = V_s$. Therefore,

$$V_s = \frac{I\,L_s}{t_{on}};\ L_s = \frac{V_s\,t_{on}}{I.}$$

For L_s larger than this value,

$$i_{ls} = i_t = \frac{1}{L_s}\int v_{ls}\,dt = V_s\frac{t}{L_s}.$$

This will slow the rise of current and reduce the losses due to dynamic saturation. When i_t = I, $v_{ls} = 0$ volts, $V_{co} = 0$ volts, and $V_{cs} = V_s$. D_r is forward biased and C_s will discharge via D_r–C_o–L_s–T. Using Kirchoff's loop rule:

$$-v_{cs}-v_{dr}-v_{co}-v_{ls}-v_{ce} = 0$$

Assuming $v_{dr} = v_{ce} = 0$ volts,

$$\frac{1}{C_s}\int i_{cs}\,dt + \frac{1}{C_o}\int i_{co}\,dt + L_s\frac{di_{ls}}{dt} = 0.$$

$$i_{cs} = i_{co} = i_{ls} - I = i_r.$$

$$\frac{i_r}{C_s} + \frac{i_r}{C_o} + L_s\frac{di_r^2}{dt^2} = 0.$$

Now, $C_o = n\,C_s$. Therefore,

$$L_s\frac{d^2}{dt^2}i_r + \frac{n+1}{n\,C_s}i_r = 0.$$

$$\frac{d^2}{dt^2}i_r + \omega^2 i_r = 0,$$

and,

$$i_r = I_A\sin(\omega t) + I_B\cos(\omega t).$$

At t = 0, $i_{ls} = i_r + I = I$. Therefore, $i_r = 0$, and $I_B = 0$.

$$i_r = I_A \sin(\omega t).$$

This equation can be integrated to obtain equations for v_{cs} and v_{co}.

$$v_{cs} = \frac{1}{C_s}\int i_r dt = \frac{1}{C_s}\int I_A \sin(\omega t)dt = \frac{-I_A}{\omega c_s}\cos(\omega t) + V_{CSA}$$

$$v_{co} = \frac{-I_A}{n\,\omega C_s}\cos(\omega t) + V_{COA}$$

$$v_{ls} = L_s \frac{di_r}{dt} = L_s \frac{d(I + i_r)}{dt} = I_A\, \omega L_s \cos(\omega t)$$

From the original Kirchoff law equation,

$$v_{cs} + v_{co} + v_{ls} = 0,$$

$$I_A\, \omega L_s \cos(\omega t) - \frac{I_A}{\omega C_s}\cos(\omega t) + V_{CSA} - \frac{I_A}{n\,\omega C_s}\cos(\omega t) + V_{COA} = 0.$$

Since

$$\omega L_s = \frac{n+1}{n\, C_s\, \omega} = Z,$$

the $\cos(\omega t)$ terms in this equation cancel, leaving $V_{CSA} + V_{COA} = 0$. At t = 0, $v_{cs} = V_s$, and $v_{co} = 0$. From the equations for v_{cs} and v_{co},

$$V_{CSA} - \frac{I_A}{\omega C_s} = -V_s$$

$$V_{COA} - \frac{I_A}{n\,\omega C_s} = 0.$$

Adding these two equations yields,

$$V_{CSA} + V_{COA} - \frac{(n+1)I_A}{n\,\omega C_s} = -V_s.$$

$$V_s = \frac{(n+1)I_A}{n\,\omega C_s} I_A = \frac{n\,\omega C_s V_s}{n+1} = \frac{V_s}{Z}$$

$$-V_s = V_{CSA} - \frac{nV_s}{n+1}$$

$$V_{CSA} = -\frac{V_s}{n+1}$$

$$0 = V_{COA} - \frac{V_s}{n+1}\ ;\ V_{COA} = \frac{V_s}{n+1}$$

This yields the following equations for snubber discharge at transistor turn-on.

$$i_r = \frac{V_s}{Z}\sin(\omega t)$$

$$v_{cs} = -\frac{V_s}{n+1} - \frac{nV_s}{n+1}\cos(\omega t) = \frac{-V_s}{n+1}(1+n\cos(\omega t))$$

$$v_{co} = \frac{V_s}{n+1} - \frac{V_s}{n+1}\cos(\omega t) = \frac{V_s}{n+1}(1-\cos(\omega t))$$

Since, as stated in chapter 4, n > 1, these conditions will continue until $v_{cs} = 0$, at which time D_s will conduct, and L_s will release its stored energy into C_o. The time at which this occurs will be referred to as t_{sd}.

$$v_{cs} = \frac{-V_s}{n+1}(1 + n\cos(\omega t_{sd})) = 0$$

$$t_{sd} = \frac{1}{\omega}\cos^{-1}(\frac{-1}{n})$$

At this time,

$$v_{co} = \frac{V_s}{n+1}(\frac{n+1}{n}) = \frac{V_s}{n};$$

and,

$$i_r = \frac{V_s}{Z}(\sin(\cos^{-1}(\frac{-1}{n}))) = \frac{V_s}{Z}\frac{\sqrt{n^2-1}}{n}.$$

Now, i_t = I, since i_r is conducted by D_s. $v_{cs} = i_{cs} = 0$. Using Kirchoff's law,

$$v_{ls} + v_{co} = v_{ds} + v_{dr} = 0.$$

$$L_s \frac{di_r}{dt} + \frac{1}{C_o}\int i_r\, dt = 0.$$

$$\frac{d^2 i_r}{dt^2} + \frac{i_r}{L_s C_o} = 0.$$

$$i_r = I_C \sin(\omega_s (t - t_{sd})) + I_D \cos(\omega_s (t - t_{sd}))$$

At $t = t_{sd}$, $i_r = \frac{V_s}{Z}\frac{\sqrt{n^2-1}}{n}$. Therefore,

$$I_D = \frac{V_s}{Z}\frac{\sqrt{n^2-1}}{n} = \frac{V_s}{Z_s}.$$

$$v_{co} = \frac{1}{C_o}\int i_r\, dt = \frac{1}{C_o}\left[\frac{-I_C}{\omega_s} cos\,(\omega_s (t - t_{sd}) + \frac{V_s}{\omega_s Z_s}\sin(\omega_s (t - t_{sd})\right] + V_{COB}$$

Since $v_{ls} + v_{co} = 0$,

$$\omega_s L_s \left[I_C \cos(\omega_s (t - t_{sd})) - \frac{V_s}{Z_s}\sin(\omega_s (t - t_{sd}))\right]$$

$$+ \frac{1}{\omega_s C_o}\left[-I_C \cos(\omega_s (t - t_{sd})) + \frac{V_s}{Z_s}\sin(\omega_s (t - t_{sd}))\right] + V_{COB} = 0.$$

Now, $\omega_s L_s = \frac{1}{\omega_s C_o}$. From this, it is found that $V_{COB} = 0$.

$$v_{co} = \frac{1}{\omega_s C_o}\left[-I_c \cos(\omega_s (t - t_{sd})) + \frac{V_s}{Z_s}\sin(\omega_s (t - t_{sd}))\right]$$

At t = t_{sd}, $v_{co} = \frac{V_s}{n}$. Therefore,

$$\frac{-I_C}{\omega_s C_o} = \frac{V_s}{n},$$

and,

$$I_C = \frac{-V_s\,\omega_s\,C_o}{n}.$$

This leads to

$$i_r = \frac{-V_s\,\omega_s\,C_o}{n}\sin(\omega_s(t-t_{sd})) + \frac{V_s}{Z_s}\cos(\omega_s(t-t_{sd}))$$

$$v_{co} = \frac{V_s}{n}\cos(\omega_s(t-t_{sd})) + \frac{V_s}{\omega_s\,C_o\,Z_s}\sin(\omega_s(t-t_{sd})).$$

Now: $Z_s = \frac{n}{\sqrt{n-1}\,\omega_s\,C_o}$ Therefore,

$$i_r = \frac{-V_s\,\omega_s\,C_o}{n}\sin(\omega_s(t-t_{sd})) + \frac{\sqrt{n-1}}{n}V_s\,\omega_s\,C_o\cos(\omega_s(t-t_{sd})),$$

and,

$$v_{co} = \frac{V_s}{n}\cos(\omega_s(t-t_{sd})) + \frac{\sqrt{n-1}}{n}V_s\sin(\omega_s(t-t_{sd})).$$

This may be simplified by using

$$\cos(\alpha+\beta) = \cos\alpha\cos\beta = \sin\alpha\sin\beta.$$

Letting

$$\cos\alpha = \frac{\sqrt{n-1}}{\sqrt{n}}, \text{ and } \sin\alpha = \frac{1}{\sqrt{n}},$$

it is found that

$$i_r = \frac{V_s\,\omega_s\,C_o}{\sqrt{n}}\cos(\omega_s(t-t_{sd}) + \alpha)$$

and,

$$v_{co} = \frac{V_s}{\sqrt{n}}\sin(\omega_s(t-t_{sd}) + \alpha).$$

This is further reduced to

$$i_r = \frac{V_s \omega_s C_o}{\sqrt{n}} \cos(\omega_s t + \phi),$$

and,

$$v_{co} = \frac{V_s}{\sqrt{n}} \sin(\omega_s t + \phi).$$

This will continue until $t = t_{rs}$, where $i_r = 0$ and the snubber is fully reset in preparation for transistor turn-off. The following conditions now hold:

$$t_{rs} = \frac{1}{\omega_s}(\frac{\pi}{2} - \alpha) + t_{sd}$$

$$v_{cs} = 0$$

$$v_{co} = \frac{V_s}{\sqrt{n}}$$

$$i_{ls} = i_t = I$$

The action of the snubber at turn-off can be broken down into three stages. The first is conventional snubber action, where i_t declines linearly while C_s charges slowly to limit the change in the voltage V_{ce}. In the second stage, V_{ce} has increased to the point where $V_{ce} + V_{co} = V_s$, and D_o is forward biased, and C_o discharges through D_o into the DC supply. In the final stage, the transistor has turned off completely, C_s will charge to V_s and C_o will discharge completely. This will leave the circuit in the state it was in prior to turn-on. The following equations describe snubber operation during the first stage. Although these stages have been described in the literature for this snubber, the equations have not been derived, and a partial derivation has been developed in this chapter.

$$i_t = I\,(1-\frac{t}{t_f})$$

$$i_{cs} = I - i_t = \frac{I\,t}{t_f}$$

$$v_{ce} = v_{cs} = \frac{1}{C_s}\int i_{cs}\,dt = \frac{I}{C_s\,t_f}[\frac{1}{2}t^2] + V_{CSC}$$

At t = 0, $V_{cs} = 0$, therefore $V_{CSC} = 0$, and

$$v_{ce} = v_{cs} = \frac{I\,t^2}{2\,C_s\,t_f}$$

Assuming that $v_{ce} = V_s$ at $t = t_f$, the equation for the value of C_s can be derived.

$$v_{ce} = V_s = \frac{I\,t_f}{2\,C_s}$$

$$C_s = \frac{I\,t_f}{2\,V_s}$$

During this stage, i_{ls} = I, and $v_{ls} = 0$ volts. D_o becomes forward biased when

$$v_{ce} + v_{co} = V_s.$$

This occurs when

$$v_{ce} = v_{cs} = \sqrt{n} - \frac{1}{\sqrt{n}}\,V_s.$$

Consider this to happen at a time $t = t_x$. Now,

$$i_{co} + I = i_{ls},$$

$$i_{ls} - i_t = i_{cs},$$

$$v_{cs} + v_{ls} + v_{co} = V_s.$$

$$\frac{1}{C_s}\int i_{cs}\,dt + L_s\,\frac{di_{ls}}{dt} + \frac{1}{C_o}\int i_{co}\,dt = V_s$$

$$\frac{i_{cs}}{C_s} + \frac{i_{co}}{C_o} + L_s \frac{d^2 i_{ls}}{dt^2} = 0$$

$$\frac{i_{ls} - I\left[1 - \frac{t}{t_f}\right]}{C_s} + \frac{i_{ls} - I}{C_o} + L_s \frac{d^2 i_{ls}}{dt^2} = 0$$

$$\frac{d^2}{dt^2} i_{ls} + \frac{1}{L_s}\left[\frac{1}{C_s} + \frac{1}{C_o}\right] i_{ls} = \frac{I}{L_s C_s}\left[1 - \frac{t}{t_f}\right] + \frac{I}{L_s C_o}$$

$$i_{ls} = I_E \sin(\omega t) + I_F \cos(\omega t) + I_G\left[1 - \frac{t}{t_f}\right] + \frac{I_H}{L_s C_o}$$

Substituting this into the differential equation gives

$$\omega^2 I_G\left[1 - \frac{t}{t_f}\right] + \omega^2 I_H = \frac{I}{L_s C_s}\left[1 - \frac{t}{t_f}\right] + \frac{I}{L_s C_o}.$$

$$I_G = \frac{I}{\omega^2 L_s C_s}\ ;\ I_H = \frac{I}{\omega^2 L_s C_o}$$

$$\omega^2 = \frac{n+1}{n L_s C_s}$$

Therefore,

$$I_G = \frac{n I}{n+1}\ ;\ I_H = \frac{I}{n+1}.$$

Transposing by t_x gives,

$$i_{ls} = I_E \sin\omega(t - t_x) + I_F \cos\omega(t - t_x) + I - \frac{n I t}{(n+1) t_f}$$

$$i_{co} = i_{ls} - I = I_E \sin\omega(t - t_x) + I_F \cos\omega(t - t_x) - \frac{n I t}{(n+1) t_f}$$

$$i_{cs} = i_{ls} - i_t = I_E \sin\omega(t - t_x) + I_F \cos\omega(t - t_x) + \frac{I t}{(n+1) t_f}$$

At $t = t_x$, i_{ls} = I, therefore,

$$I_F + I - \frac{n\,I\,t_x}{(n+1)\,t_f} = I,$$

and,

$$I_F = \frac{n\,I\,t_x}{(n+1)\,t_f}.$$

The voltage equations may be found from these currents.

$$v_{co} = \frac{1}{C_o}\int i_{co}\,dt$$

$$= \frac{1}{C_o}\left[\frac{-I_E}{\omega}\cos\omega(t-t_x) + \frac{n\,I\,t_x}{(n+1)\,\omega\,t_f}\sin\omega\,(t-t_x) - \frac{n\,I\,t^2}{2\,(n+1)\,t_f}\right] + V_{COD}$$

$$v_{cs} = \frac{1}{C_s}\int i_{cs}\,dt$$

$$= \frac{1}{C_s}\left[\frac{-I_E}{\omega}\cos\omega\,(t-t_x) + \frac{n\,I\,t_x}{(n+1)\,\omega\,t_f}\sin\omega\,(t-t_x) + \frac{I\,t^2}{2\,(n+1)\,t_f}\right] + V_{CSD}$$

$$v_{ls} = L_s\frac{di_{ls}}{dt} = \omega L_s\,I_E\cos\omega\,(t-t_x) - \omega L_s\,\frac{n\,I\,t_x}{(n+1)\,t_f}\sin\omega\,(t-t_x) - \frac{n\,I\,L_s}{(n+1)\,t_f}$$

From $v_{cs} + v_{co} + v_{ls} = V_s$, and noting that $\omega L_s = \frac{1}{\omega}(\frac{1}{C_o} + \frac{1}{C_s}) = Z$, and

$C_o = n\,C_s$,

$$V_{COD} + V_{CSD} - \frac{n\,I\,L_s}{(n+1)\,t_f} = V_s.$$

At $t = t_x$,

$$v_{cs} = \sqrt{n} - \frac{1}{\sqrt{n}}\,V_s\;;\quad v_{co} = \frac{V_s}{\sqrt{n}}.$$

$$\frac{-I_E}{\omega\,C_o} - \frac{n\,I\,t_x^2}{2\,C_o\,(n+1)\,t_f} + V_{COD} = \frac{V_s}{\sqrt{n}}$$

$$-\frac{I_E}{\omega C_s} + \frac{I\, t_x^2}{s\, C_s\, (n+1) t_f} + V_{CSD} = \frac{\sqrt{n}-1}{\sqrt{n}}\, V_s$$

Adding these two equations together,

$$V_{COD} + V_{CSD} - Z\, I_E = V_s$$

$$V_s \frac{n\, I\, L_s}{(n+1)\, t_f} - Z\, I_E = V_s$$

$$I_E = \frac{n\, I\, L_s}{(n+1) Z\, t_f}$$

After this, V_{COD} and V_{CSD} can be calculated. At t = t_f the transistor will turn-off completely. From this point on, the following will happen. First, C_s will charge up to V_s, and be clamped there by D_r and D_o. Second, C_o will fully discharge, and the load current will then be fully conducted by the feedback diode of the complementary transistor. At this stage, the snubber components are in the states prior to transistor turn-on, as already discussed. The equations for these final stages of snubber operation are not derived because the algebra is quite complex and once the transistor has turned off, further snubber action has no affect on the safe operating areas or on transistor losses.

APPENDIX B

Voltage Source Inverter Operation

Using a fully protected transistor with adequate base drive, a variety of power switching circuits may be constructed. This appendix describes the construction of a three phase voltage source inverter. In figure B.01, a three phase voltage source inverter is shown. Note that base drive and snubber circuits are not shown to simplify the diagram. This inverter is operated by the voltage pulses shown in figure B.02. This will be the shape of the line to line voltage output of the inverter. As described in chapters 3 and 4, the base drive and control circuits will

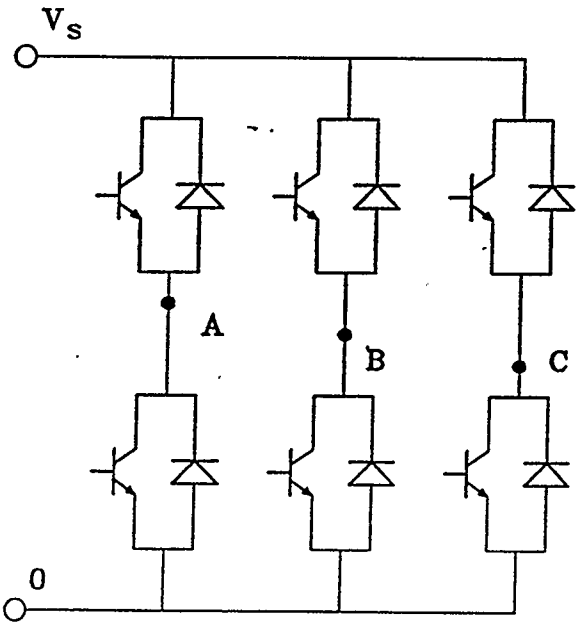


Figure B.01. Three phase voltage source inverter.

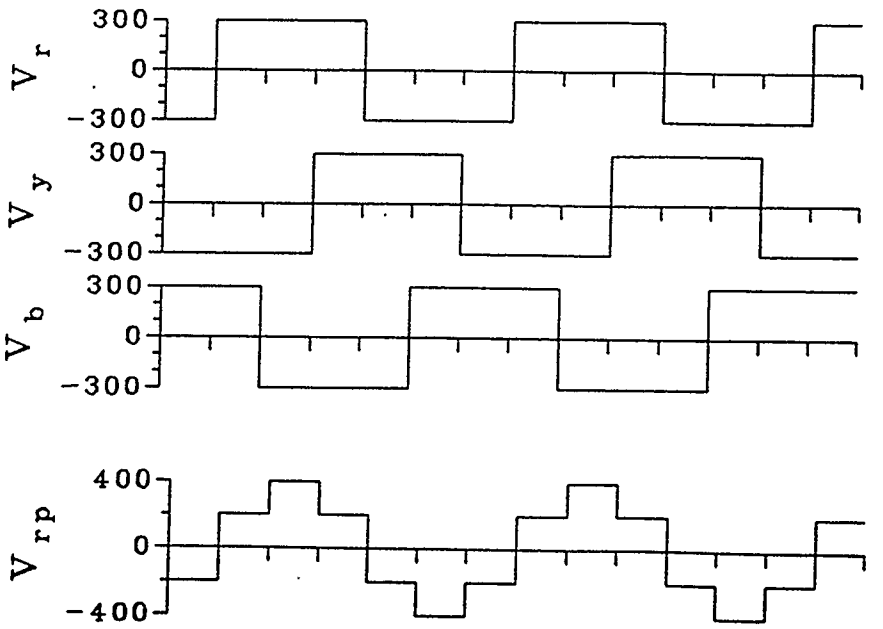


Figure B.02. Base drive control signals for inverter.

be designed so that the two transistors on one leg will be switched in proper sequence with each other, and both will not be turned on simultaneously.

The square wave AC voltage that is output by this inverter has a 120° phase difference between phases, as well as being of the correct sequence(ABC or positive sequence). Note that reversing the phase sequence can be done by changing the sequence of the controller signals. If the line to neutral voltages of the inverter are observed, it would be seen that they appear in a stairstep fashion. This is known as a six step wave.

A major problem with this square wave output is the harmonic content of the voltage and current produced. Since an inverter is most likely used to provide power to an induction motor, this could be significant. If the motor is operated at power frequency and above, i.e. 50-60 Hz and upwards, this will not be a problem. The inductance of the motor as well as its mechanical time constant will filter out the harmonics. However, if the frequency goes substantially below this value, then the harmonics become a problem. For example, with operation at 10 Hz, there will be a harmonic (the 5th) at 50 Hz. Since the motor can respond to this frequency, this harmonic will have noticeable effects. It will cause torque oscillations and harmonic heating in the motor.

To avoid these problems, some other control method must be employed. The most common of these techniques is Pulse Width Modulation (PWM), in which a carrier of sufficiently high frequency (> 1 kHz) is modulated by a sine wave of the desired frequency. This will result in a chain of pulses at the carrier frequency but the width will vary from almost zero to 100 % of the base width of the pulse. Instead of producing a pure square wave output, PWM will cause the square wave pulse to be switched on and off many times in one cycle. When looked at in terms of a frequency spectrum, it is shown that this voltage greatly reduces the low order harmonics of the power frequency portion of the signal. All that remains is the desired fundamental frequency of the voltage driving the motor, as well as the carrier signal and its harmonics. However, the motor will filter out these higher order harmonics leaving only the fundamental frequency of the power supplied to

the motor and marginal residual harmonics. As a result, the motor will operate smoothly at the desired speed.

Several things were done to implement this circuit. The base drive circuit for each transistor was assembled on its own PC board, which contained all the components except for the transformer. Since each base drive was separate, it could be mounted as close as possible to its transistor. It is very desirable to connect the base drive ground to the transistor emitter using as short a lead as possible. This helps to reduce ground problems. A twisted pair of wires may then be used to connect the base drive back to the controller, which may be remote.

The snubber circuit is built around the transistor. This requires a lot of space, since some snubber components are quite large. All the snubber components have been interconnected using AWG 6 stranded, insulated wire, since it is expected that up to 100A may be conducted in the snubber. The individual snubber components have been described in chapter 4. The diodes used in the snubber are also expected to carry large values of current. For this reason they are mounted on a heat sink. D_s and D_r are both mounted to the same sink, whereas D_o is on a separate sink. The diodes may be ordered with either anode or cathode as the stud, making dual mounting of these diodes possible. Since these heat sinks are all live, they must be mounted on insulated spaces and kept from other conducting or grounded surfaces. Figure B.03 shows a photograph of one phase as it has been constructed.

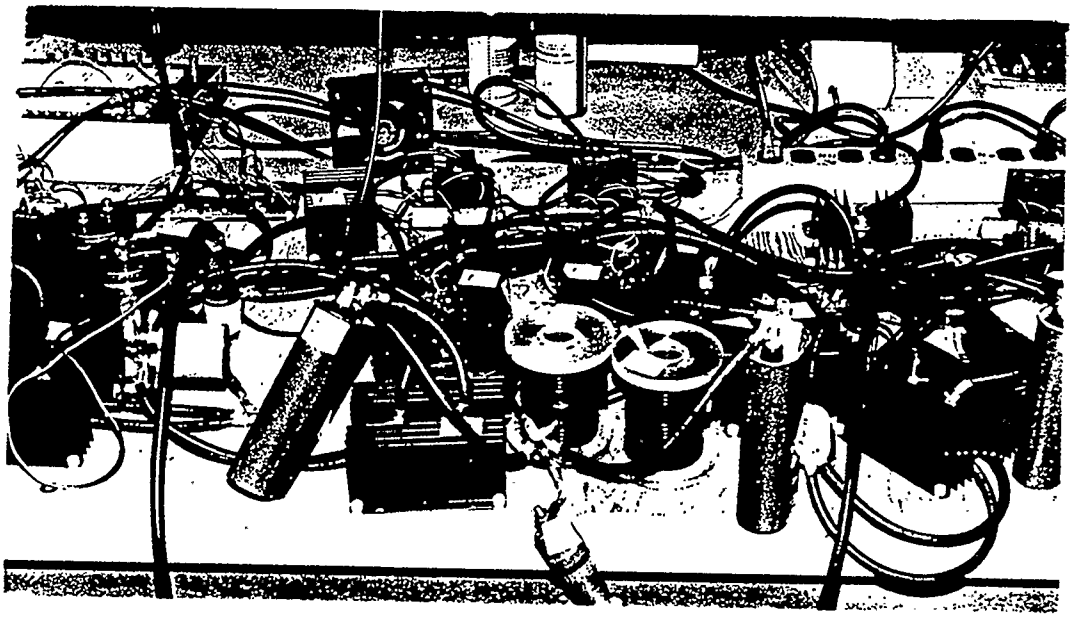


Figure B.03. Photograph of one phase of inverter.

The individual phases are identified by a color code scheme. All ground connections (true and floating grounds) are made with green wires. Phases A, B, and C are color coded red, black and blue respectively. The output of the inverter is obtained from three appropriately colored 100 Amp socket type connectors. The positive and negative DC input rails to the inverter are color coded red and black respectively. For added safety and reliability, a capacitor and varistor have been connected in shunt across the DC input rails. This is to a provide smoother DC input and to eliminate spikes which may be present on the input and which could damage the transistors.

It would likely be desirable to mount the inverter into a cabinet. When doing this, it will be necessary to separate each phase and mount it in its own section of the cabinet. It is very important to keep the base drive and snubbers close to the transistors. Also, a cooling fan should be provided for each phase. The fan should be able to blow air over all the heat sinks as well as the base drive card. Two or more fans should be used if necessary. The controller may be placed in a separate part of the cabinet or mounted elsewhere and connected to the appropriate drives. Isolation of the controller from the actual power electronics is essential. With this information it is hoped that a reliable and practical inverter can be constructed.