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A METHOD OF DESIGNING DIGITAL LDI LADDER FILTERS USING THE BILINEAR TRANSFORMATION

by

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The undersigned certify that they have read, and recommended to the Faculty of Graduate Studies for acceptance, a thesis entitled, "*A Method of Designing Digital LDI Ladder Filters Using the Bilinear Transformation*", submitted by Babu K. Ramesh in partial fulfillment of the requirements for the degree of Master of Science.

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Abstract

This thesis proposes a new method of designing digital LDI [1] ladder filters, which is known as "The Precompensation Design Method". This technique uses the voltage/current signal flow graph (*V/I* SFG) simulation design techniques. The motivation for this work is to design a class of digital LDI ladder filters with elliptic magnitude response using analog ladder filter prototypes so that the low sensitivity property of the analog ladder filters is transferred to the digital domain.

A relationship between the LDI and bilinear transformed impedances is first investigated. This relationship forms the basis of the precompensation design procedure. This design procedure realizes the bilinear transformed transfer function of an analog ladder filter using the LDI integrator as the building block. Network transformation techniques are suggested to construct *V/I* SFG's containing only analog integrators. A *V/I* SFG synthesis procedure is developed to investigate the applicability of this design technique to different types of ladder networks. The proposed design technique is demonstrated with design examples of low-pass, high-pass, band-pass and band-stop filters. The sensitivity of the magnitude-frequency response to multipier coefficient quantization of a digital LDI ladder filter and an equivalent wave digital filter is investigated.

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To all the good forces in the universe
which helped me succeed in this endeavour.

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LIST OF SYMBOLS

AAF	antialiasing filter
A_a	minimum stopband attenuation
A/D	analog to digital
a_k	denominator coefficients of $H(z)$
$(a_k)_M$	quantized denominator coefficients of $H(z)$
A_p	maximum passband ripple
$B_C(z)$	bilinear transformed capacitive impedance
BDI	bilinear discrete integrator
b_k	numerator coefficients of $H(z)$
$(b_k)_M$	quantized numerator coefficients of $H(z)$
$B_L(z)$	bilinear transformed inductive impedance
BW_p	passband width
BW_s	stopband width
C	capacitor
$CCVS$	current controlled voltage source
C_i^n	normalized capacitor values
dB	decibels
$e(n)$	error function
F	farads

f_a	stopband frequency
f_{la}	lower stopband frequency
f_p	passband frequency
f_s	sampling frequency
FSF	frequency scaling factor
f_{ua}	upper stopband frequency
f_{up}	upper passband frequency
f_{lp}	lower passband frequency
G	reactance
H	henries
$H(z)$	z-domain transfer function
I	current
L	inductor
LDD	lossless discrete differentiator
LDI	lossless discrete integrator
$LDI_C(z)$	LDI transformed capactive impedance
$LDI_L(z)$	LDI transformed inductive impedance
L_i^n	normalized inductor values
MT	magnitude truncation
$(n)_M$	binary number n with M bit representation
ODI	optimal discrete integrator
P	power

P_{max}	maximum power delivered from source to output resistor in ladder network
Q	Q-factor of analog filter
R	resistor
RO	rounding
R_1 R_2	termination resistors of doubly terminated ladder networks
rads	radians
rad/sec	radians/second
RMS	root mean square
s	analog complex frequency
T	sampling period
TCT	two's complement truncation
TR	y- or z-type transmittances
V	voltage
VCVS	voltage controlled voltage source
V/I SFG	voltage/current signal flow graph
V_s	voltage source
V'_s	precompensated voltage source
x_i	component value in ladder network
$x(t)$	continuous time signal
$x'(t)$	sampled signal
z	digital complex frequency

Z–Y–Z	a ladder block with z-type transmittances in its parallel branches and a y-type transmittance in its series branch.
Z–Z–Z	a ladder block with z-type transmittances in its parallel and series branches
ω	analog frequency variable in radians/sec
Ω	digital frequency variable
$\delta(t - nT)$	impulse function
Δ	step size
α	loss in the ladder network
θ	phase
ε	smallest number
ω_a	analog filter stopband frequency in radians/sec
ω_p	analog filter passband frequency in radians/sec
ω_o	geometric center frequency

CHAPTER 1

INTRODUCTION

1.1. Introduction and Purpose of the Thesis

A considerable amount of interest has been shown in the design of digital filters which exhibit low sensitivity in their frequency response characteristics to multiplier coefficient variations. This property allows the use of smaller wordlengths in the implementation of multipliers. Different digital filter structures can be realized directly from the same filter transfer function [2]. Among these directly derived structures the cascade realization is found to exhibit the least sensitivity to coefficient quantization [3]. Other structures which are realized by the discrete simulation of an analog ladder filter prototype offer better sensitivity properties [1,4]. Orchard [5,6] has investigated the sensitivity properties of the reactance ladder filter designed to operate between a resistive source and a resistive load. He has shown that these doubly terminated analog networks exhibit points of zero sensitivity in the passband of the filter characteristics with respect to component variations [6]. In this thesis the low sensitivity digital LDI ladder filters are designed using the *V/I* SFG simulation design method.

Wave digital filters were originally proposed by Fettweis [4]. These filters were derived by modeling the analog ladder filters using the principles of transmission line operation, so that the low sensitivity property is preserved in the

corresponding wave digital filters. Wave digital filter structures have been obtained with unit element filters and resonant transfer filters [7,8]. Subsequent work by Chu and Crochiere [9,10] has verified that wave digital filters exhibit exceptional low sensitivity to digital multipler coefficients. The sensitivity behavior of wave digital filters is also discussed in [8,11,12,13]. An alternative approach is the direct simulation of elements such as inductors, capacitors and resistors in the prototype analog ladder filter [1]. In this method, discrete approximations to integration are used for the simulation of the analog integrators and differentiators in the *V/I* SFG of the analog ladder filter. In this thesis the low sensitivity digital LDI ladder filters are designed using the *V/I* SFG simulation design method.

The direct application of the conventional bilinear transformation to the *V/I* SFG of an analog leapfrog ladder filter results in unrealizable structures which have delay free loops [1,4]. Bruton proposed the LDI transformation [1] as an alternative to the conventional bilinear transformation for the discrete simulation of analog ladder filters. Although the problem of delay free loops was solved, unfortunately the direct application of this transformation resulted in unstable transfer functions [1].

An approximate design method of digital LDI ladder filters is given in [1]. An LDI digital filter that approximates the *V/I* SFG of the prototype analog ladder filter is known to exhibit low transfer function sensitivity to the multiplier coefficients [1]. The exact design of digital all-pole transfer functions for the LDI digital ladder filter is developed in [14,15,16]. The LDI integrator $[T / (z^{1/2} - z^{-1/2})]$

has been used as the building block in the design of low sensitivity digital low-pass ladder filters [1,15,16]. Similarly, low sensitivity digital high-pass filters can be constructed by using lossless discrete differentiators (LDD) [T / ($z^{½} + z^{-½}$)] as the building block [1,15]. The LDI concept has also been successfully applied to switched capacitor networks [17,18,19-23]. Many monolithic switched capacitor filters have been fabricated [19,23].

When applied to analog elliptic ladder filters, the approximate design method in [1], ladder filters, results in unstable transfer functions. The *V/I* SFG of elliptic analog ladder filters consist of both analog integrators and differentiators. When these analog integrators and differentiators are realized using the LDI and the LDD transformations, the poles lie outside the unit circle. As one solution to this problem, an exact method of designing digital LDI ladder filters is investigated in this thesis. This method realizes a bilinear transformed elliptic transfer function using LDI integrators as the building blocks.

The classical bilinear transformation maps the entire imaginary axis of the s-plane onto the unit circle in the z-plane. The LDI transformation maps only the portion ($-2/T < \omega < 2/T$) of the imaginary axis onto the unit circle [1]. The LDI transformation is not strictly a stable transformation. Filters designed using the LDI transformation can be made stable by introducing small errors in the passband characteristics [1]. Bilinear integrators have a direct path from the input to the output. Unrealizable delay free loops occur when these integrators are used in implementing digital ladder filters. Since the LDI integrator does not have a delay free

path from the input to the output, it can be used in realizing digital ladder structures. This design method combines the advantages of the bilinear frequency mapping with that of the practical realizability of the LDI integrators.

Lee and Chang [17,18] devised a precompensation scheme for transforming an analog elliptic ladder filter to a switched capacitor elliptic ladder filter using the bilinear transformation. This scheme requires the use of bilinear terminations which results in unrealizable discrete structures, rendering the method unsuitable for digital filter implementation. In this thesis, a precompensation scheme is devised so that the frequency warping characteristics of the bilinear transformation are preserved and a stable elliptic digital ladder filter is realized.

First a relationship between the impedances obtained by using bilinear and LDI transformations is investigated. It is found that the LDI transformed impedance of an inductor L (original element) and the bilinear transformed impedance of *a parallel combination of an inductor L and a capacitor* $-T^2/4L$ *(prototype element)* are the same when these transformed impedances are scaled with a suitable scaling factor. It is also found that the LDI and the bilinear transformed impedances of a capacitor are the same when the same scaling factor is used. The terminating resistor is not strictly derived using the LDI transformation. The $R\,z^{-1/2}$ is chosen as a terminating element so as to retain the bilinear mapping. It is found that the LDI transformed impedance of $R\,z^{-1/2}$ (original element) and the bilinear transformed impedance of *the parallel combination of a resistor and a capacitor of value* $-T/2R$ *(prototype element)* are the same when the

same scaling factor is used.

This relationship between the LDI and bilinear transformed elements leads to the proposed precompensation design technique. In this method an original analog ladder filter is first modified to include the prototype elements. The effect of negative capacitors appearing as a result of this modification are compensated for with suitable element substitutions. Care must be taken to ensure that the resulting network contains only prototype elements. The impedance of every prototype element is transformed using the bilinear transformation and then replaced with the equivalent LDI transformed impedances. This is done by substituting prototype elements with their equivalent original elements. It is important to mention that the LDI transformed transfer function of the precompensated network obtained in this manner is the same as the bilinear transformed transfer function of the original analog ladder filter structure. In order to obtain realizable digital filter structures it is necessary that the *V/I* SFG of the structure contains only analog integrators.

When the *V/I* SFG construction techniques suggested in [24] are applied to elliptic ladder filter structures, undesirable differentiators occur in the *V/I* SFG. Allstot et.al. [23] suggested a technique of implementing transmission zeros for switched capacitor LDI ladder filters. When applied to digital filters, this method gives rise to feed forward and feedback paths, which cause unrealizable delay free loops. This method is further developed to eliminate the delay free loops, thus rendering the method suitable for digital filter implementations.

The method suggested in this thesis transforms the precompensated networks into an equivalent form consisting of voltage controlled voltage sources (VCVS) and current controlled voltage sources (CCVS). The *V/I* SFG of such a network consists of only analog integrators and does not contain delay free loops when used for digital filter implementations. A synthesis procedure for precompensated ladder networks is proposed.

The suggested precompensation design procedure is illustrated with design examples of elliptic low-pass, high-pass, band-pass and band-stop filters. These digital filters were simulated on a VAX 11/780 computer and the sensitivity of their frequency magnitude response characteristics with respect to multiplier coefficient quantizations are investigated. A digital elliptic LDI ladder filter designed using this design method is compared with an equivalent wave digital filter for the sensitivity of their responses with respect to multiplier coefficient quantizations. These digital structures are found to exhibit comparable multiplier quantization effects in the passband. The LDI ladder filter uses fewer adders than the comparable wave digital filter. This reduction in the LDI hardware decreases the number of computations per output sample (thus decreasing the filter response time), the size and the cost of the filter hardware.

The organization of the thesis is as follows. In Chapter 2, some aspects of digital filter design are presented. Chapter 3 focuses on the characteristics of the bilinear and LDI frequency transformations and on the bilinear and LDI integrators. Spectral transformations required in the design of normalized low-pass filter from

different filter type specifications are also given, in Chapter 3. The proposed precompensation design procedure is presented in Chapter 4. The relationship between the LDI and bilinear transformed impedances, and the design steps of the precompensation design procedure are also presented in Chapter 4. The suggested network transformation procedure to obtain realizable *V/I* SFG's, and the *V/I* SFG synthesis to investigate the applicability of this network transformation to different structures are presented in Chapter 5. The design method is illustrated with design examples in Chapter 6. The results of the simulations are presented in Chapter 6. Chapter 7 summarizes the main conclusions of the thesis and also includes the recommendations for further research.

CHAPTER 2

DIGITAL FILTER DESIGN CONCEPTS

2.1. Introduction

Digital filtering is the process of spectrum shaping using digital components as basic elements. Digital filters are used to approximate linear shift-invariant discrete time filters [25,26,27] which are desired in many digital signal processing applications. These filters are implemented using special purpose digital hardware or on a microcomputer using finite precision arithmetic. Finite precision arithmetic is non-linear in nature [25,26,27]. Hence digital filters are in fact non-linear discrete systems. Digital filter design methods have for the most part used z-transform techniques and frequency domain criteria borrowed from continuous time filter theory [27].

This chapter provides some concepts of filters which are essential in designing digital filters. Ideal sampling, aliasing, antialiasing filters and non-ideal arithmetic effects on digital filter characteristics are discussed.

2.2. Ideal sampling

The first step in the processing of analog signals is to sample the analog signal periodically. Let $x(t)$ and $x'(t)$ represent the input continuous signal and the sampled output signal, respectively. A convenient model for the ideal sampling

process is an impulse sampler which performs the following operation on $x(t)$ [28] to generate $x'(t)$ given by

$$x'(t) = x(t) \sum_{n=-\infty}^{+\infty} \delta(t - nT)$$
$$= \sum_{n=-\infty}^{n=+\infty} x(nT)\ \delta(t - nT) \quad . \tag{2.1}$$

Note from (2.1) that the sampled output signal $x'(t)$ is obtained by multiplying the continuous input signal with an impulse train $\delta(t - nT)$. The practical sampling systems can be considered as an ideal impulse sampler in cascade with a linear continuous element called zero-order-hold. This sampler is termed as sample and hold unit and is as shown in Fig. 2.1. Let $g(t)$ represent the impulse train. The frequency spectrum $G(\omega)$ of $g(t)$ is given by

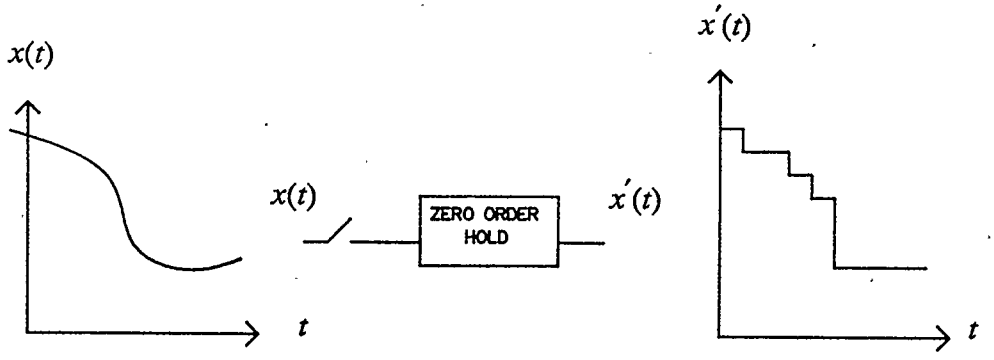


Figure 2.1 Sample and Hold

$$G(\omega) = \frac{2\pi}{T} \sum_{n=-\infty}^{n=+\infty} \delta(\omega - \frac{2\pi n}{T})$$

$$= \frac{1}{T} \sum_{n=-\infty}^{n=+\infty} \delta(f - \frac{n}{T}) \quad .$$

The impulse sampler multiplies $x(t)$ with the impulse train $g(t)$. In the frequency domain the output of the sampler can be obtained by the convolution of $G(\omega)$ and $X(\omega)$ to give

$$X'(\omega) = \frac{1}{T} \sum_{n=-\infty}^{n=+\infty} X(\omega - \frac{2\pi n}{T}) \tag{2.2}$$

where T is the sampling period [28].

Note that equation (2.2) indicates that the spectrum of the sampled signal $X'(\omega)$ contains the spectrum of the unsampled signal $x(t)$ attenuated by a factor $\frac{1}{T}$. Also note that there are infinite repetitions of $\frac{1}{T} X(\omega)$ at integer multiples of the sampling frequency $\omega_s = 2\pi/T$. Thus the output of the sampler has a periodic spectrum

$$X'(\omega) = X'(\omega - 2\pi\frac{n}{T}) \tag{2.3}$$

where n ranges over all the integers.

As T increases, the frequency spectra associated with the terms in the summation in (2.2) move closer to each other causing an overlap of spectra. This overlapping of spectra is termed as aliasing. Obviously if the input signal is bandlimited so that

$$X(\omega) = 0 \quad \text{for} \quad |\omega| > \frac{\pi}{T} \tag{2.4}$$

the spectrum overlap does not occur. The minimum sampling frequency for which (2.3) holds is called Nyquist sampling frequency. In order for a given signal to be recoverable without loss of information, it must be sampled at a frequency at least as large as the Nyquist sampling frequency, which is twice the highest frequency component contained in the signal [25,26].

2.3. Antialiasing Filters (AAF)

The problem of aliasing in digital filters is overcome by the use of antialiasing filters, whose function is to bandlimit the input signal to satisfy the condition in (2.4). These filters should bandlimit the input spectral energy, without introducing distortion and without generating excessive noise ; they are generally continuous time analog low-pass filters.

Consider the responses shown in Fig. 2.2. As shown in this figure, the stopband frequency of the antialiasing filter is chosen to be $(f_s - f_a)$, where f_a is the stopband frequency of the digital filter. The spectral energy of the input signal in the range $(\frac{f_s}{2} \le f \le f_s - f_a)$ will alias back into the frequency range $(f_a \le f \le \frac{f_s}{2})$. However, since the frequency range $(f_a \le f \le \frac{f_s}{2})$ falls in the stopband of the digital filter, no additional frequency components will appear at the output. The Sallen-Key type of continuous time filters [24] can be used to realize the desired antialiasing filter characteristics. Oversampling and decimation techniques can be

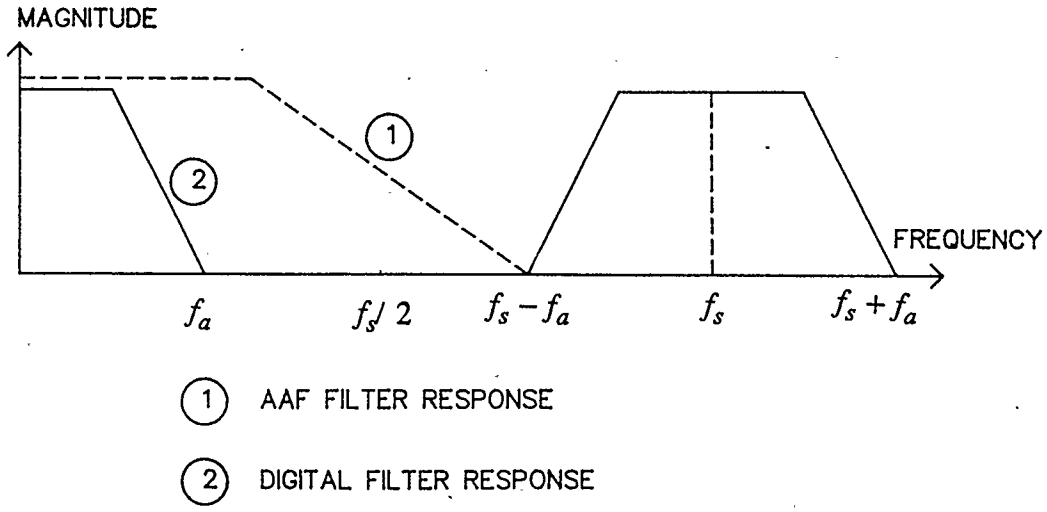


Figure 2.2 Response of digital filter and antialiasing filter.

used to reduce the requirements of the AAF [29].

2.4. Effects of Finite Wordlength in Digital Filters

In the implementation of digital filters, multiplier coefficients are realized with only finite number of bits as the wordlength of any hardware register or computer memory is limited. The four common sources of error due to finite wordlength are [30,31].

(1) the quantization of the input signal into a set of discrete levels

(2) error in the filter characteristics due to the representation of the filter coefficients by a finite number of bits, known as quantization error .

(3) the accumulation of roundoff errors due to nonlinear arithmetic operation

(4) Overflow errors due to limited number range.

In addition to the limited wordlength, the accuracy of a digital filter depends on the form of filter realization and the type of arithmetic used. The two important problems associated with fixed point arithmetic are

(1) due to rounding of arithmetic operations, especially in multiplications, a noise of random character is introduced which determines the signal to noise ratio of the system.

(2) the limitation of the coefficient wordlength leads to the change in the filter characteristics, e.g. magnitude frequency response, stability, etc.

If quantization is not very coarse, a linear model for a system behavior and a statistical model for the errors can be obtained [30].

2.5. Error Due to Input Signal Quantization

If the input signal is inherently discrete no errors exist. Since most input signals are continuous, analog to digital (A/D) conversion is necessary before digital processing can be done and hence there is a basic source of error in this conversion.

The input signal quantization operation can be considered as the substitution of the input signal samples with a finite number of bits in the binary representation. Hence any input sample can be represented in the form

$$x'(n) = x(n) + e(n)$$

where $x'(n)$ is the value taken for the sample and $e\ (n)$ is the quantization error. The usual approach for treating the effects of input quantization is to regard $e(n)$ as white noise [32,33,34]. Suppose the quantizer has equal step size Δ , then $e(n)$ is bounded by $-\Delta/2 \leq e(n) \leq \Delta/2$. Also $e\ (n)$ has zero mean and variance $\frac{\Delta^2}{12}$. Depending on the type of quantization used different distributions are obtained for the quantization noise.

The steady state output component due to $e(n)$ is a zero mean wide_sense_stationary sequence with power spectral density given by

$$H(z)\ H(\frac{1}{z})\ \frac{\Delta^2}{12}$$

where $H(z)$ is the transfer function of the filter [35]. The mean squared value of the error at the output due to input quantization can be obtained by integrating power spectral density and is given by [34]

$$\frac{1}{2\pi j} \oint H(z)\ H(\frac{1}{z})\ \frac{\Delta^2}{12}\ \frac{dz}{z} \quad ,$$

which can be evaluated numerically or algebraically.

2.6. Error Due to Finite Wordlength of Multiplier Coefficients

This type of error depends on the number of binary digits used to represent the multiplier coefficients, and on the type of number representation used.

2.6.1. Number Representation and Associated Errors

A real number can be represented using a finite number of bits either in the fixed point form or in the floating point form [25,26]. A floating point number offers greater dynamic range at the cost of extra bits. However, the implementation is complex and the computations are slower than the fixed point case. Unlike the fixed point addition, both addition and multiplication of floating point numbers can introduce roundoff errors [36]. Only fixed point form is considered in this thesis.

Let n be a normalized number, so that $|n| \leq 1$. Then n has the 2's complement representation

$$n = -n_o + \sum_{k=1}^{k=\infty} n_k 2^{-k} \quad ; \quad n_k = 1 \quad or \quad 0 \quad . \tag{2.5}$$

Rounding or quantization can be used to represent the number n with a word length of M bits $(n)_M$. Rounding of a number to M bits, having an initial representation with more than M bits, is accomplished by choosing the rounded result $(n)_M$ as a M bit number closest to the initial unrounded quantity. Quantization is accomplished by discarding all bits which are less significant than the least significant bit which is retained. Since rounding introduces less errors than magnitude quantization, consider rounding for discussion purposes. The error due to rounding lies within the bounds given by

$$-2^{-M} < n - (n)_M \leq 2^{-M} \quad .$$

The approximation error ε may be defined as

$$(n)_M = n + \varepsilon \tag{2.6}$$

with $-2^{-M} \leq \varepsilon \leq 2^{-M}$. This error is referred to as quantization noise [37]. The errors due to the inaccuracy in number representation are modeled as small random quantities statistically independent of one another with a uniform probability distribution in the range $(-2^{-M}, 2^{-M})$ [37,33].

Overflow is said to occur when the digital filter computes a number which cannot be represented in the arithmetic used in the digital filter. Under no overflow conditions fixed point numbers introduce no errors. However fixed point number multiplication can cause overflow errors [25,26]. Overflow appears in the form of transient errors or in the form of oscillations at the digital filter output. Another point to consider is the representation of negative numbers. Two's complement number representation is widely used in digital filter hardware realizations [25,26,27]. Three main features of two's complement number system are [25,26,38]:

(1) two's complement number set has only one representation of zero as against two in other number representations

(2) the magnitude of the final result of a sequence of two's complement arithmetic operations is not increased with the overflow occuring anywhere in the sequence of operations

(3) no extra bit is required to represent negative numbers.

2.6.2. Effect Due to Multiplier Coefficient Inaccuracy

The digital filter transfer function $H(z)$ can be defined as the ratio of the z-transform of the output sequence to the z-transform of the input sequence [28]. As a result of fixed wordlength used in a digital filter, each coefficient of the filter transfer function $H(z)$

$$H(z) = \frac{\sum_{k=0}^{k=n} b_k z^{-k}}{1 + \sum_{k=0}^{k=n} a_k z^{-k}} \tag{2.7}$$

is replaced with its M bit representation according to (2.6). Hence the coefficient a_k is replaced with a_{k_M} which equals $a_k + \alpha_k$, where the absolute value of α_k is bounded by 2^{-M}. Similarly, each b_k is replaced by $(b_k)_M$ which equals $b_k + \beta_k$. These perturbations in a_k and b_k cause the filter characteristics to change. The actual filter transfer function now becomes

$$[H(z)] = \frac{\sum_{k=0}^{k=n} b_{k_M} z^{-k}}{1 + \sum_{k=0}^{k=n} a_{k_M} z^{-k}} \cdot \tag{2.8}$$

One method of measuring the effect of coefficient wordlength inaccuracy is by computing the frequency response of the actual filters with quantized coefficients, i.e by using the actual transfer function in (2.8) and then comparing it with the ideal response associated with the transfer function in (2.7). This method is used in this thesis to find the minimum number of bits required to represent

multiplier coefficients so that the actual filter response meets the required specifications of the filter.

The other significant effect due coefficient inaccuracy is the possible movement of poles from inside to outside of the unit circle in the z-plane. One can also calculate the movement of the poles and zeroes of the transfer function due to coefficient quantization and then apply network sensitivity theory to study the changes in the filter response [30,2].

2.7. Error Due to Non-Ideal Arithmetic Operations

The multiplication of two numbers of n bits each results in a product with $2n$ bits. However, since the register lengths are finite, the product has to be quantized so as to accommodate in the available registers. The second non-linear filter operation is the adder overflow, in which case the most significant bit must be altered to produce a word that can again be stored in the register. The errors due to arithmetic roundoff could be very serious.

The effects of non-ideal arithmetic operations are [32,39,40,41]

1) Quantization noise

2) Quantization limit cycle and

3) Overflow oscillations .

The popular quantization schemes, namely rounding (RO), magnitude truncation (MT) and two's complement truncation (TCT) are well described in [26,27]. Both MT and TCT introduce a larger error than RO; however, they are easy to

implement in hardware form. Under adder overflow conditions saturation arithmetic [42] and zeroing arithmetic [41] technique can be used.

With constant or zero input to a feedback section of the filter, the quantization errors can lead to a small periodic oscillations called limit cycles at the output of the filter. Many methods proposed to control limit cycle oscillations are described in [43,44,45].

2.8. Summary

The discussion presented in this chapter is mainly focussed on the concepts of aliasing, antialiasing filters, and non-ideal arithmetic effects of digital filters. The two undesirable effects due to finite wordlength in multiplier coefficients are the degradation of the signal to noise ratio and the deterioration of the frequency-magnitude response of the filter. Limit cycles and overflow oscillations arising from non-ideal arithmetic pose problems in digital filter implementations.

CHAPTER 3

SPECTRAL TRANSFORMATIONS

3.1. Introduction

The traditional method of designing digital filters involves the transformation of an analog filter into a digital filter meeting prescribed specifications [25,26,27]. This is a reasonable approach because the field of analog filter design is highly advanced [27], and because many useful analog filter design tables are available [46,47]. This approach is used in this thesis. The design method developed maps the excellent low sensitivity properties of the doubly terminated analog ladder filters into digital ladder filters. The low sensitivity properties of the lossless doubly terminated analog ladder filters and the spectral transformations used to transform these analog ladder filters into digital ladder filters are investigated. Discrete transfer functions required for the realization of discrete integrators are also discussed.

3.2. Loss Sensitivities in Doubly Terminated Ladder Filters

Doubly resistively terminated lossless two port ladder networks exhibit exceptional low sensitivity of their loss_frequency response to their component variations including variations in the terminating resistors [5,6]. It has been shown in [6] that the passband attenuation of a conventional doubly terminated analog ladder

filter is less sensitive to errors in component values than the attenuation of the corresponding singly terminated filters. This property has motivated many new high quality RC-active, switched capacitor and digital filter design techniques [1,4,20,23]. Consider a reactance ladder filter to operate between a resistive source and a resistive load as shown in Fig. 3.1. For this network the transducer function is defined as [24]

$$\alpha + j\beta = \ln H(j\omega) = \ln \frac{V}{2V_2} \sqrt{\frac{R_2}{R_1}} \tag{3.1}$$

where the loss α is in *nepers* and the phase β is in *radians*. Note that

$$\begin{aligned} 2\alpha &= \ln |H(j\omega)|^2 \\ &= \ln \frac{|V|^2/4R_1}{|V_2|^2/R_2} = \ln \frac{P_{\max}}{P_2} \end{aligned} \tag{3.2}$$

where $P_{\max}$ is the maximum power available from the source R_1 and P_2 is the

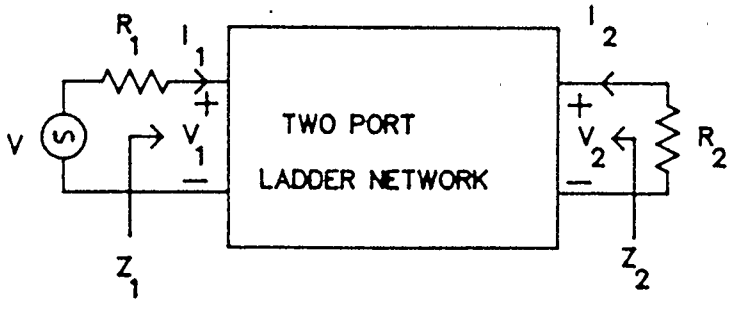


Figure 3.1 Doubly terminated two port ladder network

power dissipated in R_2. Since the two-port is assumed to be passive, the loss α is always nonnegative and is equal to zero when $P_2 = P_{max}$.

If the ladder filter is designed such that at the frequencies of minimum loss over the passband the source delivers its maximum available power into the load, one finds to a first order approximation that at some frequencies in the passband and for every component the sensitivity of the loss to component tolerances is zero. This can be easily checked by referring to Fig. 3.2 noting that when one has zero loss in a reactance network, a component change, whether an increase or decrease, can only cause the loss to increase; in the neighborhood of the nominal value, the curve relating the loss to any component value must therefore be quadratic and consequently $\frac{\partial \alpha}{\partial x_i} = 0$, where x_i is any component value [6]. If α is small, $\frac{\partial \alpha}{\partial x_i}$ will also remain small [6].

Hence as Orchard states [5] "If one designs a conventional equal ripple-passband filter with the usual magnitude of ripple (say $\leq$ 0.2 *dB*), and arranges to

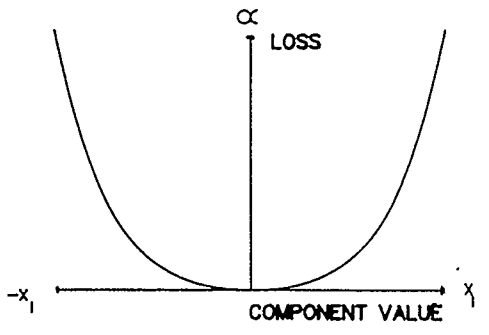


Figure 3.2 Loss vs component value of doubly resistively terminated analog ladder network

get maximum transfer of power at the frequencies of minimum loss, then both α and $\frac{\partial \alpha}{\partial x_i}$ are exactly zero at these frequencies and, because of the small passband ripple, $\frac{\partial \alpha}{\partial x_i}$ also remains small everywhere else in the passband. This is the basis of the low sensitivity of conventional ladder filters and of those RC-active and digital filters which are modeled on the ladder."

From partial differentiation of (3.2) it is possible to show that

$$\frac{x_i}{|V_2|}\,\frac{\delta|V_2|}{\delta x_i} = -\,x_i\frac{\delta\alpha}{\delta x_i} \tag{3.3}$$

and

$$\frac{x_r}{|V_2|}\,\frac{\delta|V_2|}{\delta x_r} = -\,x_r\frac{\delta\alpha}{\delta x_r} \pm \frac{1}{2} \tag{3.4}$$

where x_i represents any reactive element in the filter and x_r represents the terminating resistors. From (3.3) it is clear that the output voltage V_2 will share the zero sensitivity of the loss function with respect to the variations in values of the reactive elements. Also, it is observed in (3.4) that changes in the terminating resistor values will introduce a frequency independent shift to V_2, due to the terms $\pm$ 1/2, in addition to the small changes due to $\frac{\delta\alpha}{\delta x_r}$. Similar expressions can be obtained for output power P_2 [6].

3.3. Bilinear and LDI Transformations

After identifying the low sensitivity property of the analog ladder filter structures, consider the frequency transformations required to transform these analog ladder filters into digital ladder filters. The two frequency transformations which are of interest are the bilinear and LDI transformations. The frequency mapping properties of these two transformations and the realization of discrete integrators using these two transformations are discussed.

3.3.1. Bilinear Transformation

The bilinear transformation is an algebraic expression that provides a simple mapping between continuous and discrete domains. This transformation transforms the entire $j\omega$ axis of the s-plane onto the unit circle, in the z-plane. The bilinear transformation is given by

$$s = \frac{2}{T}\,\frac{z-1}{z+1} \quad . \tag{3.5}$$

The significant properties of this transformation are

a) it maps the entire $j\omega$ axis onto the unit circle, including the points at $\pm j\infty$,

b) it maps the open left-half plane of the s-domain to the interior of the unit circle in z-domain,

c) it maps the open right-half plane of the s-domain to the exterior of the unit circle in the z-domain.

d) The inverse transformation

$$z = \frac{1 + \frac{sT}{2}}{1 - \frac{sT}{2}}$$

has analogous reciprocal properties.

Clearly rational functions transform to rational functions and poles in the left-half plane transform to the poles inside the unit circle. In other words, a stable analog filter transforms to a stable digital filter, and zeros on the imaginary axis and at infinity transform to zeros on the unit circle. This mapping characteristic is shown in Fig. 3.3

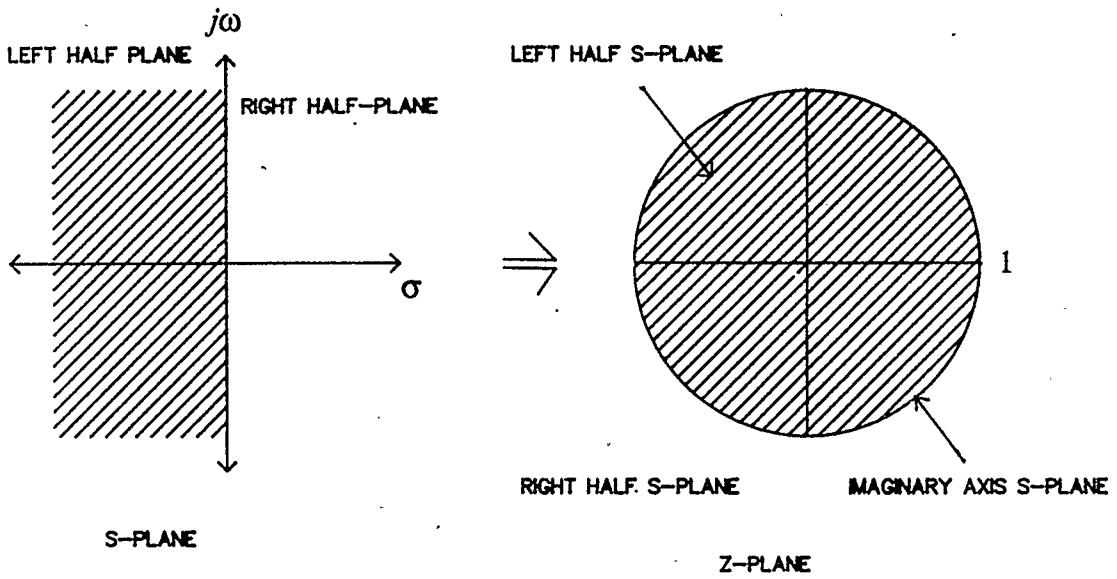


Figure 3.3 Mapping property of the bilinear transformation

To demonstrate the mapping property substitute $z = e^{j\Omega T}$ in (3.5) to arrive at

$$s = \frac{2}{T} \frac{e^{j\Omega T} - 1}{e^{j\Omega T} + 1} \tag{3.6}$$

where $\Omega = 2\pi f / fs$ is the normalized frequency variable in the digital domain. The equation (3.6) can be written as

$$\begin{aligned} s &= \frac{2}{T} \left[\frac{e^{j\Omega T/2} - e^{-j\Omega T/2}}{e^{j\Omega T/2} + e^{-j\Omega T/2}} \right] \\ &= \frac{2}{T} j\tan(\Omega T/2) \end{aligned} \tag{3.7}$$

Substitute $s = j\omega$ in (3.7) to arrive at

$$\omega = \frac{2}{T} \tan(\Omega T/2) \tag{3.8}$$

The frequency warping characteristics of the bilinear mapping is shown in Fig. 3.4 for the case $T = 2$. For small values of Ω the mapping is approximately linear; otherwise, the mapping is non-linear. This non-linearity introduces distortion in the frequency axis. The bilinear transformation always yields a stable digital filter transfer function $H(z)$ from a stable analog filter transfer function $H(s)$. Since the bilinear transformation warps the frequency axis, the analog filter must be prewarped using the relation in (3.8).

3.3.2. Bilinear Discrete Integrator (BDI)

The usefulness of this transformation in the realization of discrete integrators is discussed. One of the important features of discrete integrators is to simulate an

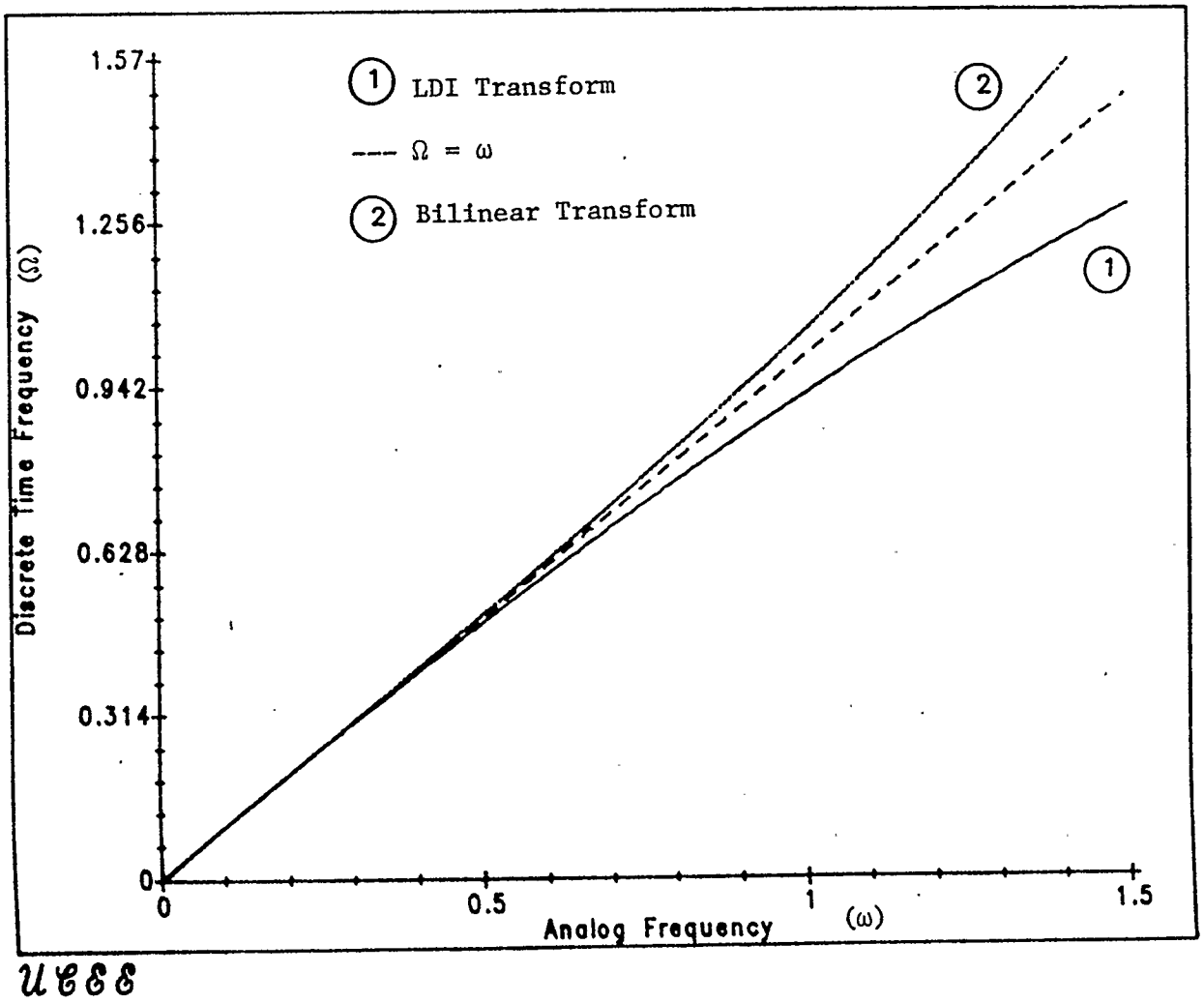


Figure 3.4 Warping characteristics of the bilinear and LDI Transformations

analog integrator so that the fractional magnitude error and the analogous phase error are practically zero or tolerably low-valued [1,48]. Different s- to z- transformations proposed for this purpose are based on different numerical integration techniques [1,48].

The transfer function for the discrete integrator is [48]

$$I_{D_i}(e^{j\omega T}) = \frac{G_i}{j\omega}\,(1+\varepsilon)\,e^{j\theta} \tag{3.9}$$

where G_i the i'th intergrator gain and is given by

$G_i = \frac{1}{RC_i}$ for capacitive reactance and

$= \frac{R}{L_i}$ for inductive admittance.

Different discrete intergrators are compared by comparing the phase error θ and fractional magnitude error ε using (3.9)

In the bilinear discrete integrator the numerical integration is approximated by the area of the trapezoidal whose two bases are $f\,[(N-1)T]$ and $f\,[NT]$ and with height is T as shown in Fig. 3.5(a). The phase θ and fractional magnitude errors ε are given by [1]

$$\theta = 0 \quad \text{and} \quad \varepsilon = \frac{\omega T}{2}\,cot(\frac{\omega T}{2}) - 1 \quad . \tag{3.10}$$

The BDI does however correspond to lossless elements ($\theta = 0$) so that the errors in the attenuation function, due to dissipation in the LC elements, is clearly zero for

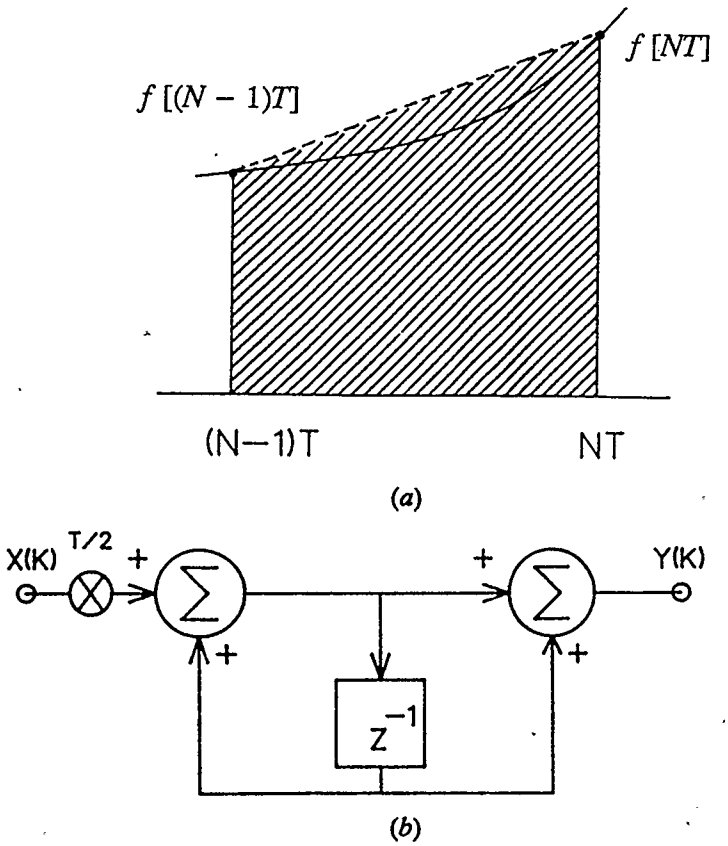


Figure 3.5 Bilinear discrete integrator
(a) Trapezoidal numerical integration
(b) Bilinear discrete integrator

all T. Discrete integrators should not give rise to undesirable delay free loops when used to realize digital ladder filters from the *V/I* SFG of the leapfrog analog ladder filters. The disadvantage of BDI is that, since the degree of the numerator and denominator of (3.5) is the same, any discrete realization of this transfer function will result in delay free forward path [1,4] as shown in Fig. 3.5(b). Consequently combining BDI's in the leapfrog manner will inevitably result in unrealizable delay free loops. Thus BDI's cannot be used in digital ladder filter design by *V/I* SFG simulation techniques, in spite of its useful frequency mapping properties.

3.3.3. LDI Transformation

The LDI transformation is an another important transformation which maps continuous transfer functions into discrete transfer functions so that the essential properties of the continuous time system is transformed to the discrete domain. This transformation is given by [1]

$$s = \frac{1}{T} \frac{z-1}{z^{1/2}} \quad . \tag{3.11}$$

The significant properties of this transformation are

a) it maps only that strip of width $-2/T$ to $+2/T$ of the open left-half plane to the interior of the unit circle as shown in Fig. 3.6.

b) the portion $|\omega| > 2/T$ is not mapped on to the z-plane

c) this transformation is not a stable transformation.

To demonstrate the mapping property substitute $z = e^{j\Omega T}$ in (3.11) to arrive at

$$s = \frac{1}{T} \left[e^{j\Omega T/2} - e^{-j\Omega T/2} \right] \quad . \tag{3.12}$$

Substitute $s = j\omega$ in (3.12) to obtain

$$\omega = \frac{2}{T} \sin(\Omega T/2) \quad . \tag{3.13}$$

Note that Ω in (3.13) is the normalized digital frequency variable. The frequency warping characteristics of the LDI transformation is shown in Fig. 3.4. Also note that as the continuous time frequency ranges from

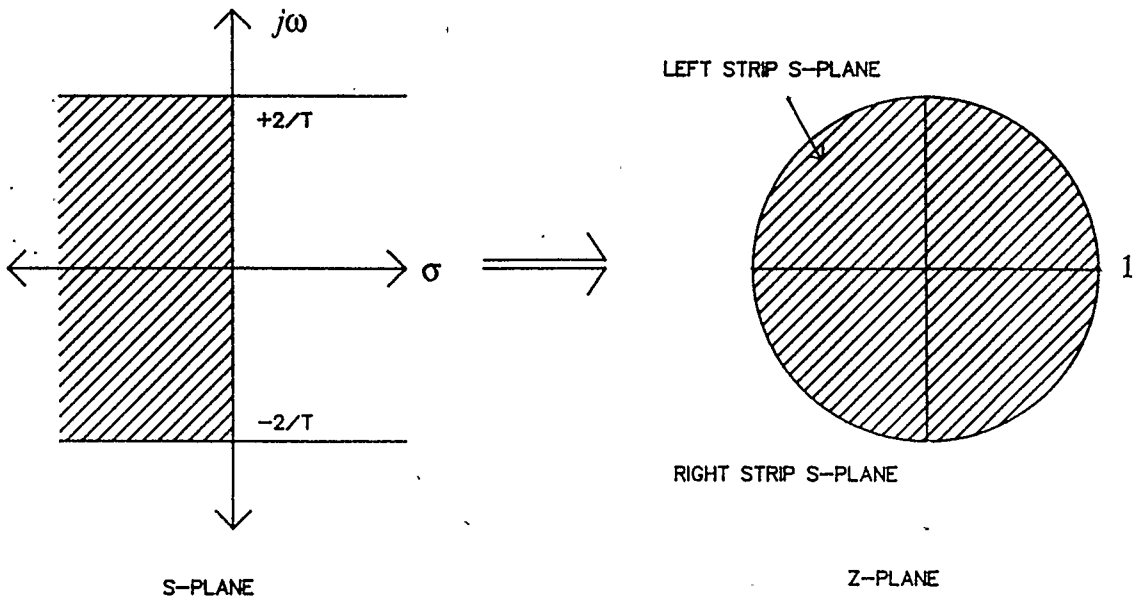


Figure 3.6 Mapping property of the LDI transformation

$$\frac{-f_s}{\pi} < \frac{\omega}{2\pi} < \frac{f_s}{\pi}$$

the discrete-time filter frequency ranges over its entire principle range of

$$\frac{-f_s}{2} < \frac{\Omega}{2\pi} < \frac{f_s}{2} \quad .$$

From equations (3.8) and (3.13) the distortion introduced due to the nonlinearity by the LDI transformation (sinusoid) is less than that due to the bilinear transformation (tangent). The nonlinearities introduced by these two transformations in frequency warping characteristics is compared in Fig. 3.4. One important point to

mention is that the true LDI transformation is not strictly a stable transformation. The expression for the LDI transformation in (3.11) remains unaltered when z is replaced by $-z^{-1}$, so that for every pole z_j of the transformed LDI network there must exist another pole at $-z_j^{-1}$. Clearly one of the poles z_j or $-z_j^{-1}$ must lie outside the unit circle or both should lie on the unit circle ; as a result the exact LDI transformation is strictly unstable. However, stability can be introduced into the LDI transformed structures at the cost of some distortion in the frequency mapping characteristics of the transformation [1]. The usefulness of the LDI transformation in realizing discrete integrators is considered in the next section.

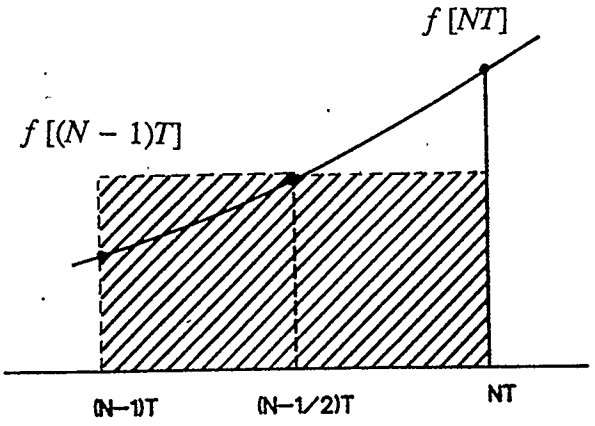
3.3.4. Lossless Discrete Integrator (LDI)

The numerical integration technique used in this integrator is shown in Fig. 3.7(a). Here the integration of $f(t)$ is approximated by the area of the rectangular whose height is $f\,[(N-\frac{1}{2})T]$ and its width is T as shown in Fig. 3.7(a).

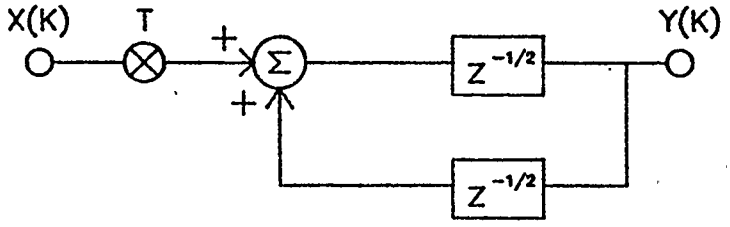
The phase error and fractional magnitude error for the LDI transformation are [1]

$$\theta = 0 \quad \text{and} \quad \varepsilon_2 = \frac{\omega T}{2}\left[cosec\left[\frac{\omega T}{2}\right] - 1\right] \quad . \tag{3.14}$$

The realization of this integrator is shown in Fig. 3.7(b). Note that this integrator does not have a delay free path from the input to the output. Also note that this integrator contains half unit delays in its realization. The disadvantage of this integrator is that any discrete structure realized using the LDI integrator is strictly



(a)



(b)

Figure 3.7 LDI integrator
(a) Numerical integration of LDI integrator
(b) LDI integrator

unstable. However, it is possible to propagate the half unit delays from the integrators to the terminations in leapfrog digital ladder filters. Then by eliminating these half unit delays, the network can be made stable with small errors in the frequency response provided that $\omega T \ll 1$ [1].

The bilinear transformation maps the entire imaginary axis while the LDI transformation maps only the portion $-2/T$ *rad/sec* to $+2/T$ *rad/sec* onto the unit circle. In other words, the bilinear transformation compresses the frequency scale whereas the LDI transformation expands it [18]. The bilinear transformation

therefore narrows the transition band and thus improves the filtering function. Unfortunately the BDI has a delay free path from its input to its output, and hence cannot be used to construct leapfrog digital ladder filters.

In order to utilize the merits of these two transformation, in the *V/I* SFG simulation design technique, a new design method which is called "the precompensation design method" is proposed in this thesis. In this design method the bilinear transformation is used to map frequencies from the s- domain to the z-domain to obtain a z-domain transfer function, and then the LDI integrator is used to realize this transfer function. This design method is explained in detail in Chapter 4.

Different discrete transfer functions used for the realization of discrete integrators are discussed in [1,48]. El Masry [48] has proposed a different discrete integrator called optimal discrete integrator (ODI), which has zero phase error and fractional magnitude error less than that due to LDI. The hardware realization of ODI is complex and thus the ODI has limited application.

3.4. Spectral transformations

This section summarizes the spectral transformations, which are used in this thesis to design equivalent analog filters from the digital filter specifications using the bilinear transformation. This procedure involves the design of an analog low-pass filter whose passband edge is normalized to 1 *rad/sec*, and then denormalizing to the desired analog filter. After designing the equivalent normalized low-pass filter from the digital filter specifications there are two distinct approaches available

available to transform the normalized analog low-pass filter into digital filters [25,27]. These two approaches are pictorially represented in Fig. 3.8. In this thesis, the first approach shown in Fig. 3.8(a) is used, in which the normalized analog low-pass filter is first transformed into the desired denormalized analog filter, and is then transformed to obtain the desired digital filter.

In the *V/I* SFG simulation method used in this thesis the element value transformation discussed in [46,47] are used to transform the normalized low-pass filter element values to the corresponding element values for high-pass, band-pass

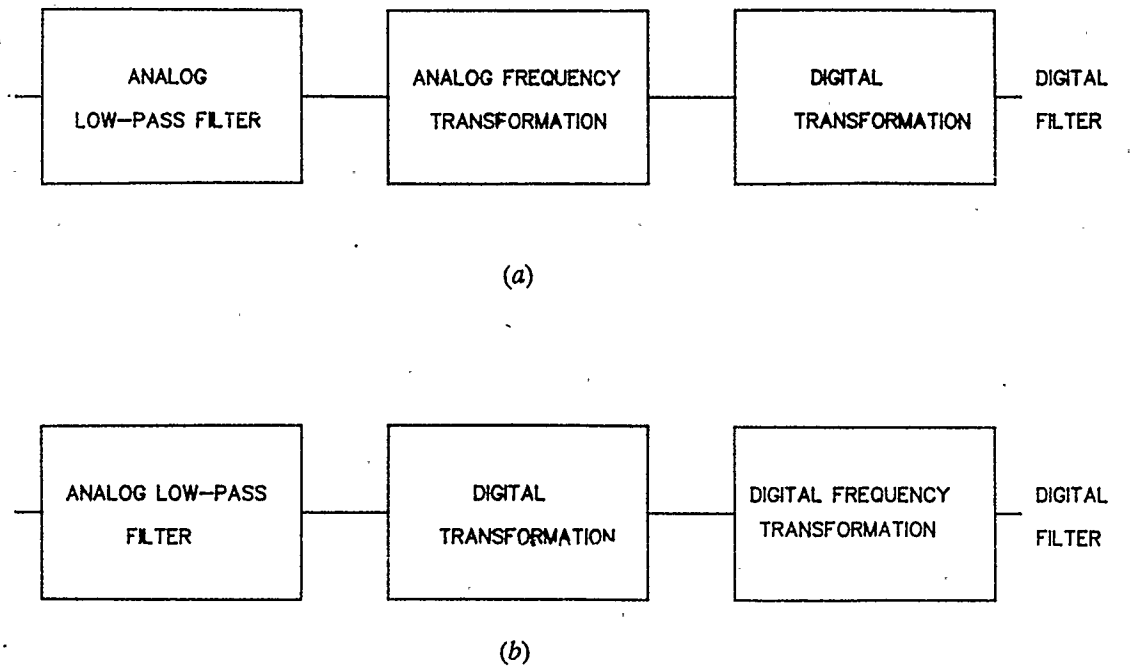


Figure 3.8 Transformations to design digital filters from normalized analog low-pass filter

or band-stop analog filters. The digital transformation of these filters is performed using the discrete integrator transfer functions in the *V/I* SFG of the analog filters to realize the corresponding digital structures.

First consider the transformations required to design a low-pass filter whose passband edge is normalized to 1 *rad/sec* from the digital filter specifications. Let ω and Ω represent the analog and discrete frequency variables, respectively. The subscripts p and a refer to passband and stopband frequencies, respectively. The subscripts l and u refer to lower and upper passband or stopband frequencies in the case of band-pass or band-stop filters, respectively.

Low-pass: Consider the expression (3.8), which relates the analog and digital frequency variables. Since the passband edge of the analog low-pass filter is desired to be at 1 *rad/sec*, choose

$$\frac{2}{T} = \frac{1}{\tan(\Omega_p T/2)}. \tag{3.15}$$

Substitute (3.15) in (3.8) to obtain

$$\omega = \frac{1}{\tan(\Omega_p T/2)} \tan(\Omega T/2) . \tag{3.16}$$

Substitute (3.15) in (3.5) to obtain

$$s = \frac{1}{\tan(\frac{\Omega_p T}{2})} \frac{z-1}{z+1} . \tag{3.17}$$

The expression in (3.16) can be used to obtain the specifications of the normalized

analog low-pass filter. The equation in (3.17) can be used to obtain discrete transfer function $H(z)$ from $H(s)$.

High-pass: Consider the transformation

$$s = \frac{T}{2}\,\frac{z+1}{z-1}\,. \tag{3.18}$$

Substitute $s=j\omega$ and $z = e^{j\Omega T}$ in (3.18), to get

$$\omega = k\frac{1}{\tan(\Omega T/2)} \tag{3.19}$$

where $k = \frac{T}{2}$.

By choosing $k = tan(\Omega_p T/2)$, the passband edge of the analog low-pass filter is normalized to 1 *rad/sec*. Use the value of k in (3.18) and (3.19) to get

$$s = \tan\,(\Omega_p T/2)\;\cdot\;\frac{z+1}{z-1} \tag{3.20}$$

and

$$\omega = \tan\,(\Omega_p T/2\,)\;\cdot\;\frac{1}{\tan(\Omega T/2)} \tag{3.21}$$

The transformation in (3.21) maps $0 \le \omega < \infty$ to $0 < \Omega < \pi$ and $0 < \omega < 1$ to $\Omega_p < \Omega < \pi$ [49].

Band-pass: The transformation to transform a digital band-pass filter specification to a normalized analog low-pass filter specification is given by [25,49].

$$\omega = \frac{\alpha(\beta - \cos \Omega T)}{\sin \Omega T} \tag{3.22}$$

where

$$\alpha = \frac{1}{\tan\left[\frac{\Omega_{Pu}T - \Omega_{Pl}T}{2}\right]}$$

and

$$\beta = \frac{\sin(\Omega_{Pu}T + \Omega_{Pl}T)}{\sin(\Omega_{Pu}T) + \sin(\Omega_{Pl}T)}$$

Also the discrete and analog frequency variables are related by the following equation

$$s = \alpha\left[\frac{z^2 - 2\beta z + 1}{z^2 - 1}\right] \tag{3.23}$$

This transformation maps ±1 *rad/sec* continuous passband frequencies to the lower and upper passband cut off frequencies $\Omega_{Pl}T$ and $\Omega_{Pu}T$ respectively.

Band-stop: The transformation to transform a digital band-stop filter specification to a normalized analog low-pass filter specification is given by [25,49].

$$\omega = \frac{\alpha \sin(\Omega T)}{(\beta - \cos \Omega T)} \tag{3.24}$$

where

$$\alpha = \frac{\cos(\Omega_{Pl}T) - \cos(\Omega_{pu}T)}{\sin(\Omega_{Pl}T) - \sin(\Omega_{pu}T)} \tag{3.25}$$

and

$$\beta = \frac{\sin(\Omega_{pl}T + \Omega_{pu}T)}{\sin(\Omega_{pl}T) + \sin(\Omega_{pu}T)} \quad . \tag{3.26}$$

The s and z domain frequency variables are related by the expression

$$s = \frac{\alpha(z^2 - 1)}{z^2 - 2\beta\, z + 1} \quad . \tag{3.27}$$

This design method is used in this thesis to design analog ladder filter prototype which will be transformed to digital LDI ladder filters using the proposed design technique.

3.5. Summary

From the review of the discussion by Orchard [5,6] it is found that the doubly resistively terminated lossless ladder networks possess the least sensitivity of pass-band attenuation to component variations. It is also found that bilinear transformation possesses the desired frequency mapping properties. The LDI integrator does not have a delay free path from the input to the output. Spectral transformations required in the design of analog ladder filters from digital filter specifications are also discussed.

CHAPTER 4

PRECOMPENSATION DESIGN METHOD

4.1. Introduction

The doubly resistively terminated LC ladder filters are known to exhibit exceptional low sensitivity in passband characteristics to variations in component values. The basic philosophy in the design method adopted by Bruton [1] and Fettweis [4] is to transform the low sensitivity properties of the doubly terminated analog filter prototype to the discrete domain. Fettweis adopted a design method in which a doubly terminated analog ladder filter is modeled by using the wave equations in the transmission line theory to design wave digital filters [4]. The synthesis technique proposed by Bruton allows the digital filter to be realized by direct analogy with the voltage-current relations of doubly resistively terminated LC ladder filters. In this design method, the *V/I* SFG of the analog ladder filter is transformed into the corresponding discrete structure using discrete integrator or differentiator transfer functions [1].

In this chapter the digital all-pole LDI ladder filter design proposed by Bruton is reviewed. The drawbacks of the direct application of this design method to the design of digital elliptic LDI filters from analog elliptic ladder prototypes are discussed. A relationship between the LDI and bilinear transformed impedances is investigated. Based on this relationship a precompensation design method is

proposed. This design technique is used to transform arbitrary analog ladder filters into digital LDI ladder filters. This design method implements a bilinear transformed transfer function using LDI integrators as building blocks.

4.2. Digital all-pole LDI Ladder Filter Design

Bruton adopted an approach based on an analogy with the continuous leapfrog [1,59,51] ladder structure in the voltage/current domain to design all pole LDI ladder filters. It is shown in [1,50,51,] that continuous integrators may be interconnected in the form of leapfrog structure to realize low-pass and band-pass analogs of terminated LC filters. Also it is shown in [1,15] that differentiators may be used in the leapfrog structure to realize high-pass analogs of LC filters. The gains of integrators and differentiators correspond exactly to the L and C element values of the corresponding LC filter. The class of leapfrog structures that are directly analogous to the LCR prototype filter do not strictly allow s-plane zeros [50,51]. Similarly, the discrete transfer functions that are synthesized approximate all-pole LCR prototypes.

Bruton [1] developed a method of discrete simulation of analog integrators in the leapfrog structure. He has shown that the bilinear transformation is not suitable for the realization of discrete integrators since these integrators have a delay free path from the input to the output. Undesirable delay free loops result when these bilinear integrators are connected in the leapfrog manner. As Bruton stated [1], "The prime motivation for the invention and successful implementation of wave

filters is the problem of apparent unrealizability of the direct discrete analog of continuous LC ladder networks".

The bilinear transformation can be modified, so as to introduce a delay from the input node to the output node, and the resulting transformation is called the modified bilinear transformation [1]. The modified bilinear transformation yields realizable low-sensitivity leapfrog digital ladder filters for the case where $\omega T \ll 1$, over the passband. The disadvantage of this method is that the consequence of providing delay free loops is that the passband droop can only be reduced by reducing the delay time T. This introduces limitations in the filter hardware. To overcome this disadvantage Bruton introduced a new frequency transformation called the LDI transformation, which does not provide a delay free path and the transformation maps ideally onto the unit circle for $z = e^{j\omega T}$. This transformation can be used for the discrete simulation of integrator and, in turn, can be used to construct realizable digital filters.

A method of designing all pole low-pass filters using the *V/I* SFG simulation and the LDI transformation is described in [1]. The *V/I* SFG of the original analog low-pass prototype filter is constructed. The analog integrators in the *V/I* SFG are replaced with LDI integrators. Note that the gains of LDI integrators [$\frac{T}{C_n}$, $\frac{T}{L_n}$] are inversely proportional to the values of the L's and C's of the LCR prototype. In this way there is a one to one correspondence between the L and C elements of the analog filter and the multiplier coefficients of the digital filter. Consequently,

the first order sensitivity of the attenuation function to perturbations of gains is zero at frequencies at which the passive LC prototype exhibits zero insertion loss [1].

The discrete structure realized in this method using LDI's as building elements is found to contain half delay elements. Bruton has suggested a method to eliminate these half unit delays in the discrete structure. If each branch impedance of the continuous LC prototype is multiplied by $e^{-sT/2}$, then the realization of each inductive branch has impedance $z_i(s) = sL_i\, e^{-sT/2}$, each capacitive branch has admittance $y_i(s) = sC_i\, e^{-sT/2}$ and the terminating impedances are $R_1\, e^{-sT/2}$ and $R_N\, e^{-sT/2}$.

The $e^{-sT/2}$ or $z^{-1/2}$ impedance transformation does not alter the transfer function or the sensitivity properties of the realization [2], but it does not provide a reduction in the number of delay elements by a factor of two thus simplifying the hardware realization of the LDI filters. It is observed that after the discrete network is scaled by $z^{-1/2}$ elements, the half unit delays will remain at the terminations. The network thus obtained is not strictly stable, for the reason discussed in Section 3.3.3. However, it is proposed in [1] that removal of these half unit delays from the terminating branches makes the network stable. It can easily be shown that if the LC all-pole prototype filter is of the order n and $\omega T \ll 1$, then the exact LDI transformed network will contain n poles that are inside the unit circle and in the right-half y-plane, where $y = z^{1/2}$, and an additional n poles outside the unit circle in the left-half y-plane. Removal of these terminating $z^{1/2}$ elements results in an LDI network that does not contain any half delay elements, so that the input/output

transfer function $H(z)$ may be expressed as $H(y^2)$. In other words $H(z)$ is an even rational function of y so that if the n right-half y-plane poles are inside the unit circle then the n-left half y-plane poles are also inside the unit circle [because of the mirror image symmetry of the singularities of $H(y^2)$ about the imaginary axis] [1,52]. The removal of the terminating $z^{1/2}$ elements therefore will result in a stable structure.

However, the removal of these terminating half delay elements introduces an error in the transfer function [1]. The attenuation error due to fractional errors of the terminating resistances and due to parasitic termination impedances is given in [1]. Choi [21] has analyzed termination errors as a function of sampling frequency for a fifth order Chebychev low-pass filter for complex conjugate terminations in the case of switched capacitor filters. The error introduced increases as the sampling frequency is decreased. Hence, this design method requires higher sampling frequencies in order to reduce errors in the transfer function. Thus the design method adopted in [1] to design digital LDI ladder filters is not exact.

The design method suggested by Bruton when applied directly to analog elliptic ladder filters results in *V/I* SFG's consisting of undesirable analog differentiators. When these differentiators are realized using the LDI transformation, unrealizable non-causal structures result [1]. Also since the degree of the numerator of the differentiator transfer function is less than that of the denominator, any discrete realization of this transfer function results in delay free loops. As a solution to these problems, a design method is proposed in this thesis in which

the bilinear transformed transfer function of the elliptic analog ladder filter is realized using LDI building blocks. No termination approximations are used in this design method thus eliminating attenuation errors in pass-band and stop-band due to termination approximations.

To summarize, the features of the proposed design method are

1 The bilinear transformation is used to map the entire analog frequency range ($-\infty < f < +\infty$) to the discrete domain.

2 LDI blocks are used to realize the bilinear transformed transfer function without delay free loops.

3 Since no termination approximations are used attenuation errors in the pass-band and stop-band due to termination approximations are eliminated.

4 Low-pass, high-pass, band-pass and band-stop digital LDI filters with transmission zeroes can be implemented using this design method.

Thus this proposed design method is intended to combine the advantages of the frequency mapping properties of the bilinear transformation with the practical advantages of the LDI structure to yield low sensitivity digital elliptic LDI ladder filter structures.

4.3. Relationship Between Bilinear and LDI Transformed Impedances

Since the bilinear transformation possesses desired properties in the filter design a relationship between bilinear and LDI transformed impedances is investigated. This relationship leads to a method of realizing a bilinear transformed

transfer function using the LDI as building block.

Lee and Chang [18] devised a precompensation scheme for transforming an analog elliptic ladder filter to a switched capacitor elliptic ladder filter using the bilinear transformation. This scheme requires the use of bilinear terminations which results in unrealizable discrete structures, rendering the method unsuitable for digital filter implementations. In this thesis a precompensation scheme is proposed so that the frequency characteristics of the bilinear transformation are preserved and a stable elliptic digital ladder filter is realized.

First the bilinear and LDI transformed impedances are defined as follows. Let

$$C(s) = \frac{1}{sC} \quad \text{and} \quad L(s) = sL \tag{4.1}$$

represent the capacitive and inductive impedances, respectively. Substituting the expression (3.5) in (4.1), the bilinear transformed capacitive and inductive impedances can be written as

$$B_C(z) = \frac{T}{2C}\,\frac{z+1}{z-1} \tag{4.2}$$

and

$$B_L(z) = \frac{2L}{T}\,\frac{z-1}{z+1} \quad . \tag{4.3}$$

Substituting the expression (3.11) in (4.1) the LDI transformed capacitive and inductive impedances can be written as

$$LDI_C(z) = \frac{T}{C}\,\frac{z^{1/2}}{z-1} = \frac{T}{C}\,\frac{1}{z^{1/2} - z^{-1/2}} \tag{4.4}$$

and

$$LDI_L(z) = \frac{L}{T}\,\frac{z-1}{z^{1/2}} = \frac{L}{T}\,(z^{1/2} - z^{-1/2}) \tag{4.5}$$

respectively. It is known from analog filter theory that scaling the impedances of the analog filter does not alter the filter transfer function. The equivalent to impedance scaling in the analog domain can be carried out in the digital domain also without altering the transfer function. Scaling the z-domain impedances involves in signal flow graph manipulation consisting of shifting the half unit delay elements in the filter network. If each element of the LDI digital filter is scaled by the value $\frac{1}{2}(z^{1/2} + z^{-1/2})$, then the z-transform of the inductor branch is given by

$$L(z) = \frac{L}{2T}\,(z^{1/2} - z^{-1/2})\quad(z^{1/2} + z^{-1/2}) \tag{4.6}$$

$$= \frac{2L}{T}\left[\frac{z^{1/2} + z^{-1/2}}{z^{1/2} - z^{-1/2}} - \frac{z^{1/2} - z^{-1/2}}{z^{1/2} + z^{-1/2}}\right]^{-1} . \tag{4.7}$$

Multiplying both numerator and denominator by $z^{1/2}$ the expression for $L(z)$ simplifies to

$$L(z) = \frac{2L}{T}\left[\frac{z+1}{z-1} - \frac{z-1}{z+1}\right]^{-1} . \tag{4.8}$$

Applying the inverse bilinear transformation to (4.8) we get the s-domain impedance

$$\left[\frac{1}{sL} - \frac{T^2 s}{4L}\right]^{-1} . \tag{4.9}$$

Observe that (4.9) is the Laplace transform of an inductor L connected in parallel with a capacitor having a value of $-T^2/4L$ (a negative capacitor). In other words, *the bilinear transformed and then impedance scaled by inductor L in parallel with a negative capacitor $-T^2/4L$ is equivalent to an LDI transformed inductor L.*

The LDI transformed impedance of a capacitor has the z transform $\frac{T}{C\,(z^{1/2} - z^{-1/2})}$. If this impedance is scaled by the value $\frac{1}{2}\,(z^{1/2} + z^{-1/2})$ the capacitor element z transform is given by

$$C(z) = \frac{T}{2C}\left[\frac{z^{1/2} + z^{-1/2}}{z^{1/2} - z^{-1/2}}\right] .$$

Multiplying both numerator and denominator by $z^{1/2}$ the expression for $C(z)$ simplifies to

$$C(z) = \frac{T}{2C}\left[\frac{z+1}{z-1}\right] . \qquad (4.10)$$

Applying the inverse bilinear transformation to (4.10) we get the Laplace transform $1/sC$. Hence *the bilinear transformed and then impedance scaled capacitor C is equivalent to an LDI transformed capacitor C.*

Note that the termination resistor approximation is not obtained using the LDI transformation. However, the use of the termination $Rz^{1/2}$ allows the implementation of a stable digital filter and retains the bilinear mapping. If this transformed terminator $Rz^{1/2}$ is scaled by the value $\frac{1}{2}(z^{1/2} + z^{-1/2})$ the z transform of the ter-

minating resistor is given by

$$R(z) = \frac{R}{2} \left(z^{1/2} \right) \left(z^{1/2} + z^{-1/2} \right)$$

$$= R \left[\frac{z^{1/2} + z^{-1/2}}{z^{1/2} + z^{-1/2}} - \frac{z^{1/2} - z^{-1/2}}{z^{1/2} + z^{-1/2}} \right]^{-1} .$$

Multiplying both numerator and denominator by $z^{1/2}$ the expression for $R(z)$ simplifies to

$$R(z) = R \left[1 - \frac{z-1}{z+1} \right]^{-1} . \tag{4.11}$$

Applying the inverse bilinear transformation to (4.11) we get the Laplace transform

$$R(s) = \left[\frac{1}{R} - \frac{Ts}{2R} \right]^{-1} . \tag{4.12}$$

Therefore *the bilinear transformed and impedance scaled resistor R in parallel with a negative capacitor –T/2R is equivalent to the transformed value* $Rz^{1/2}$.

The relationships between the LDI and bilinear transformed inductor, capacitor and resistor impedances are tabulated in Table 4.1. *Note that throughout this thesis "Prototype Elements" refer to the group of elements shown in the rightmost column of Table 4.1 and "Original Elements" refer to the group of elements shown in the leftmost column of Table 4.1.*

The results obtained in the above discussion lead to the following important conclusions. Let the elements of the original analog ladder filter be modified so that to every inductor L_n is attached a negative capacitor $-T^2/4L_n$ in parallel and to

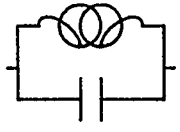
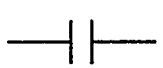
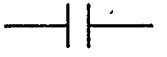
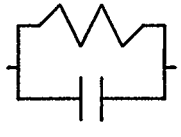
ORIGINAL COMPONENT	LDI TRANSFORM	IMPEDANCE SCALED $(z^{\frac{1}{2}} + z^{\frac{-1}{2}})/2$	INVERSE BILINEAR	PROTOTYPE ELEMENT
 L	$\frac{L}{T}(z^{\frac{1}{2}} - z^{\frac{-1}{2}})$	$\frac{2L}{T}\left(\frac{z+1}{z-1} - \frac{z-1}{z+1}\right)^{-1}$	$\left(\frac{1}{sL} - \frac{Ts}{4L}\right)^{-1}$	 L $-T^2/4L$
 C	$\frac{T}{C}\left(\frac{1}{z^{\frac{1}{2}} - z^{\frac{-1}{2}}}\right)$	$\frac{T}{2C}\left(\frac{z+1}{z-1}\right)$	$\frac{1}{sC}$	 C
 R	$R z^{\frac{1}{2}}$	$R\left(1 - \frac{z-1}{z+1}\right)^{-1}$	$\left(\frac{1}{R} - \frac{Ts}{2R}\right)^{-1}$	 R $-T/2R$

Table 4.1 Relationship between Prototype and Original Elements

every resistor R_n is attached with a negative capacitor $-T/2R_n$ in parallel. These additional negative capacitors alter the transfer function of the analog network. In order to retain the original transfer function attach positive capacitors of the same value to compensate for the effects of the negative capacitors. In other words, the modified network consists of only the prototype elements shown in Table 4.1 and still has the original filter transfer function.

Let the bilinear transformation be used to transform the impedance of every prototype element of the modified network. From the results obtained in Table 4.1, it is obvious that every bilinear transformed impedance has an equivalent LDI transformed impedance. Hence, if the prototype elements in the modified network are replaced with their equivalent original elements from the Table 4.1, a network is obtained whose LDI transformed transfer function is the same as the bilinear transformed transfer function of the original network.

In other words, by using the terminations $Rz^{1/2}$, the LDI transformed digital filter realizes the same transfer function that would be obtained by adding a negative capacitor $-T^2/4L_n$ in parallel with each inductor L_n and a negative capacitor $-T/2R$ with each resistor in the reference analog filter and then transforming to the discrete domain using the bilinear transformation. Hence, if inductors and resistors in the reference analog ladder filter are precompensated by adding positive capacitors of appropriate values in parallel, the resulting LDI digital filter realizes the exact bilinear transformed transfer function of the original reference ladder filter.

This conclusion leads to a new method of designing digital LDI ladder filters which realize the bilinear transformed transfer function. The proposed design method suggests that all the inductors and the termination resistors in the original analog filter should be precompensated with appropriate positive capacitors in parallel. The precompensation of the termination resistors results in a source transformation, which is described in Chapter 6. The proposed method of designing digital LDI ladder filters is described in detail in the following section.

4.4. Precompensation Design Procedure

The design procedure discussed in this section applies to all resistively terminated analog LC ladder filters. Examples of designing different types of ladder filters using this design method are illustrated in Chapter 6.

The approximation methods of analog filter design are highly advanced, yielding results in the form of classical filter tables [46,47] or numerical design data [53]. Hence, it is advantageous to use the design techniques already developed for doubly terminated analog ladder filters. This approach simplifies the design method, thus eliminating the involved approximation procedure of the analog filter design. Based on the relationship between the LDI transformed and bilinear transformed impedances developed in the previous section, a precompensation design procedure is formulated. The analog filter prototype is first precompensated according to this precompensation procedure. The *V/I* SFG of the precompensated analog filter is developed such that it contains only analog integrators, i.e no

differentiators. The LDI shown in Fig. 3.7(b) is used to discretize the analog *V/I* SFG. Finally, the discrete structure is scaled by $z^{-1/2}$ elements to obtain a realizable discrete structure. The design steps of the proposed design procedure are as follows:

Step-1 Start with the specifications of the digital filter. Let Ω and ω represent the frequency variables in the digital filter and the corresponding analog filter, respectively. Suppose f_s is the sampling frequency, and $T = \frac{1}{f_s}$ is the sampling period. The normalized digital filter specifications can be obtained using the relationship

$$\Omega \cdot T = \frac{2\pi f}{f_s} \quad rads. \tag{4.13}$$

where f is the frequency in *Hz*. Use the bilinear transformation to obtain the specifications of the equivalent analog filter. The analog frequency can be calculated using the relation

$$\omega = \frac{2}{T} \tan\left[\frac{\Omega T}{2}\right] \quad rads/sec \ . \tag{4.14}$$

The passband and stopband cutoff frequencies of the equivalent analog filter are obtained using the relationship in (4.14). Since the bilinear transformation is a frequency transformation between the analog and digital domains, the specifications of the passband and

stopband attenuations remain the same in both these domains [25].

Step-2 After obtaining the equivalent frequency specifications in the analog domain, the analog filter meeting these specifications is designed. Three types of approximations which are commonly used in analog filter design are butterworth, chebychev and elliptic approximations. Even though the design procedure suggested in this section applies to all these three types of analog filters, only the elliptic function ladder filters are considered.

The design tables, which contain the LCR values of the analog ladder filters, after solving the elliptic approximation, are available [46,47]. Computer programs have been developed to design elliptic analog ladder filters [53]. When digital LDI band-pass or band-stop filters have to be designed, the first step is to design a normalized analog low-pass filter whose passband edge is at 1 *rad/sec*, and then use frequency transformations to obtain analog band-pass or band-stop filters [46]. Thus, in this step the LCR values of the equivalent analog ladder filter are obtained using either design tables or design programs.

Step-3 It is mentioned in the previous section that the inductors and resistors in the original filter are to be precompensated by adding a

positive capacitor of appropriate value in parallel, to realize the exact bilinear transformed transfer function in LDI digital ladder filters.

Hence, modify the elements in the original filter structure to represent the prototype elements in the Table 4.1. In other words, every inductor L is replaced by an inductor in parallel with a negative capacitor $\frac{-T^2}{4L}$, every resistor R is replaced with a resistor in parallel with a negative capacitor $\frac{-T}{2R}$ and the capacitors remain unchanged. Modify only the required element values of the analog filter, so as to compensate for the effect of each additional negative capacitor which was introduced with the element substitutions. The resulting network should consists of only prototype elements after element substitutions. This step will involve the transformation of the input voltage source, which is discussed in detail in Chapter 6. The network thus obtained consists of only prototype elements and still has the original filter transfer function. This network is referred to as the precompensated network.

Step-4 Recall that if the bilinear transformed impedances of the prototype elements in Table 4.1 are scaled with the scaling factor $(z^{1/2} + z^{-1/2})/2$ the resulting impedances are same as the LDI

transformed impedances of the original elements in the Table 4.1. Transform every prototype element in the precompensated network using the bilinear transformation and replace it with its equivalent LDI transformed impedance. This is done by simply substituting every prototype element in the precompensated network with its equivalent original element from Table 4.1.

The network thus obtained, referred to as the LDI equivalent of the precompensated network, contains only LDI transformed impedances. Note that the LDI transformed transfer function of this network is the same as the bilinear transformed transfer function of the original filter. Hence, this network can be discretized by realizing LDI transformed impedances of every branch in the network using LDI integrators.

Step-5 Construct a *V/I* SFG of the precompensated network to contain only analog integrators $\frac{1}{s}$ and no differentiators s. Consider the LDI transformation in (3.11). This expression represents the transfer function of a differentiator. Since the degree of the numerator is greater than that of the denominator, any realization of this transfer function results in delay free paths [1]. Also the realization of discrete differentiators using LDI transformation results in non-causal structures. Hence the LDI transformation cannot be

used for discrete differentiator realization. For this reason the *V/I* SFG's of the precompensated filters should consist of only analog integrators, which can be realized by LDI elements. This condition restricts the types of analog filters to which this precompensation method can be applied. The types of analog filters which can be designed using this design method are investigated in Chapter 5.

A network transformation is proposed in Chapter 5 to transform many precompensated networks to equivalent forms, consisting of current and voltage controlled voltage sources which can be realized using LDI integrators.

Step-6 Replace every analog integrator in the *V/I* SFG with an LDI element. The terminating resistor R_i should be replaced with $R_i\, z^{1/2}$ terminator as discussed in Section 4.3. The summing nodes in the *V/I* SFG can be realized with adders. The network thus obtained can be implemented with half unit delay elements by doubling the sampling frequency. However, it is not economical to realize this network, since the number of half unit delay elements is large.

Step-7 Recall that scaling the LDI ladder network by $z^{-1/2}$ elements does not alter the filter transfer function. By applying this technique to the discrete structure obtained in Step 6, all half unit delays can be

eliminated from the network, and the resulting network is found to consist of only unit delay elements. Scaling the discrete network by $z^{-1/2}$ delay elements can be done by moving the delay elements throughout the network. *V/I* SFG manipulation can also be performed on the discrete network to obtain realizable networks without delay free loops. The suggested *V/I* SFG identities shown in Fig 4.1 can be applied at different nodes of the network to realize a network with only unit delay elements. It is found that the structures obtained after scaling the network by $z^{-1/2}$ delay elements consist of integrators implemented by Forward Euler and Backward Euler structures [48]. It is also found that there are no half unit delay elements left at the terminations after scaling the network by $z^{-1/2}$ elements.

The design procedure suggested above is simple and straightforward. Recall that in the digital LDI ladder filters which realize the Chebychev transfer function, the expressions for the coefficients of multipliers have one to one correspondence with the element values of the original filter. Note that in this design method, some of the coefficients of the multipliers in the digital filter do not have a one_to_one correspondence with the elements of the analog prototype. The expressions for the coefficients of the multipliers are found to consist of more than one element value of the original filters. The one_to_one correspondence between the multiplier coefficients and the analog element values is lost because of the network

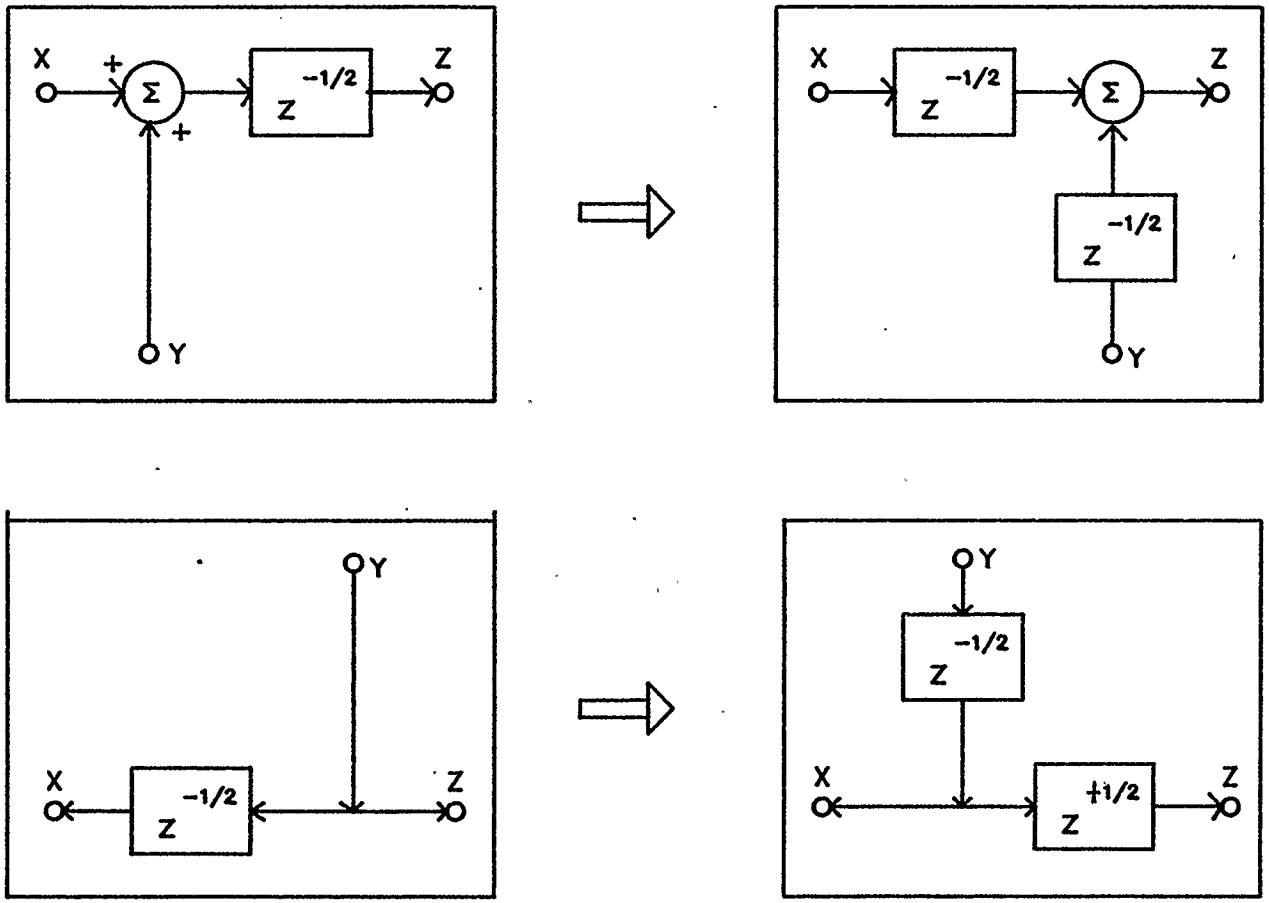


Figure 4.1 *V/I* SFG Identities

transformation which is performed on the precompensated filters to realize *V/I* SFG's with only analog intergators in them.

Theoretically, this design procedure can be applied to any analog circuit consisting of LCR elements. Practically, on the other hand this design procedure can be applied only to those analog structures whose precompensated networks, consist of only analog integrators in their *V/I* SFG's. A variety of practically important digital LDI ladder filters can be designed using this design method. In order to identify the class of analog filters which cannot be designed in this design method, a signal flow graph synthesis procedure of precompensated analog ladder filters is discussed in the next chapter.

4.5. Summary

The design procedure of digital all-pole ladder filters suggested by Bruton is reviewed and its limitations are discussed when applied to the design of elliptic digital ladder filters. A relationship between the bilinear and LDI transformed impedances is investigated. Based on this result, a precompensation design procedure is developed for the design of elliptic digital ladder filters.

CHAPTER 5

V/I SFG SYNTHESIS OF PRECOMPENSATED NETWORKS

5.1. Introduction

In the precompensation design the *V/I* SFG of the precompensated ladder network should consists of only analog integrators. When the *V/I* SFG of the precompensated low-pass, high-pass, band-pass or band-stop filters with transmission zeroes are constructed, undesirable differentiators occur. In order to eliminate these differentiators in the *V/I* SFG's, a network transformation is suggested in this chapter. This network transformation transforms the precompensated ladder network into an equivalent form containing VCVS's and CCVS's. A *V/I* SFG synthesis is presented to examine the applicability of this network transformation to different networks; some examples are also given.

5.2. Ladder Topology and its V/I SFG

A transmittance in a *V/I* SFG and the *V/I* SFG itself can be of two types, namely impedance type (z-type) and admittance type (y-type). A z-type transmittance or *V/I* SFG has current as its input variable and voltage as its output variable. A y-type transmittance or *V/I* SFG has voltage as its input variable and current as its output variable [24]. The rules for the *V/I* SFG simulation of series and parallel connections of y- and z-type transmittances [24] are summarized below.

Rule-1 The *V/I* SFG simulation of a parallel connection of y-type transmittances always results in a y-type *V/I* SFG.

Rule-2 The *V/I* SFG simulation of a parallel connection of a y-type and a z-type transmittance always results in a z-type *V/I* SFG.

Rule-3 A parallel connection of branches can possess no more than one z-type transmittance in its z-type *V/I* SFG.

Rule-4 The simulation of a series connection of an arbitrary number of z-type transmittances always results in a z-type *V/I* SFG.

Rule-5 The simulation of a series connection of a z-type and a y-type transmittance always results in a y-type *V/I* SFG.

Rule-6 A series connection of branches can possess no more than one y-type transmittance in its y-type *V/I* SFG.

A general leapfrog ladder filter consisting of transmittances in series and parallel branches is shown in Fig. 5.1. Using the rules stated above two types of *V/I* SFG's can be constructed for the general ladder network in Fig. 5.1. By choosing all parallel branches as z-type and all series branches as y-type transmittances (Z-Y-Z ladder), a z-type *V/I* SFG can be constructed. On the other hand, by choosing all the parallel branches as y-type and series branches as z-type transmittances (Y-Z-Y ladder), a y-type *V/I* SFG can be constructed.

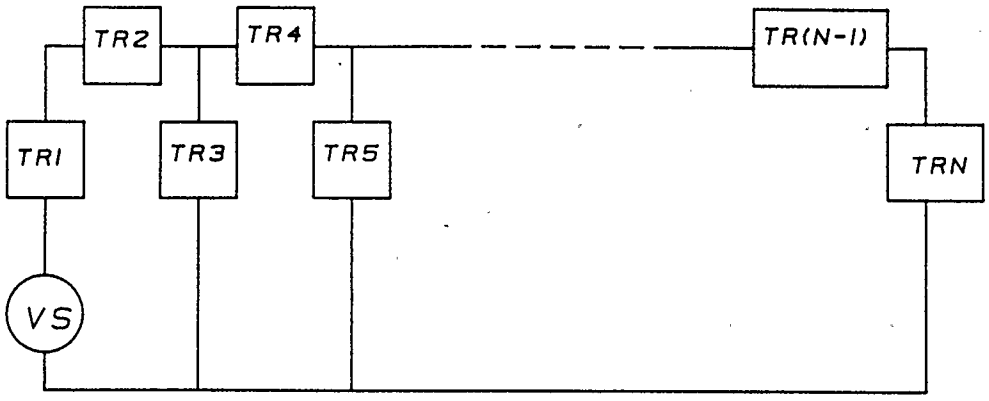


Figure 5.1 General analog ladder network

5.2.1. Z-type V/I SFG of the General Ladder Network

The construction of z-type *V/I* SFG of the general ladder network shown in Fig. 5.1 is discussed. First, choose the transmittance TR1 to be of y-type. According to Rule-5 of *V/I* SFG construction, since TR1 is of y-type, the *V/I* SFG of the series combination of TR1 and TR2 is always of y-type irrespective of the transmittance type of TR2. Hence, TR2 can be of either z- or y-type transmittance. Choose TR2 to be of z-type transmittance. Note that TR3 appears in parallel with the series combination of TR1 and TR2. Since it is required to construct a z-type *V/I* SFG of the general ladder network, choose transmittance TR3 to be of z-type. The type designation of transmittances to realize z-type *V/I* SFG of the general ladder is shown in Fig. 5.2. According to Rule-2, since the z-type TR3 appears in parallel with the y-type *V/I* SFG, the resulting *V/I* SFG is of z-type. The transmittance TR4 appears in series with the z-type *V/I* SFG developed so far. Hence it has to be of y-type. This procedure is repeated to arrive at the *V/I* SFG of the

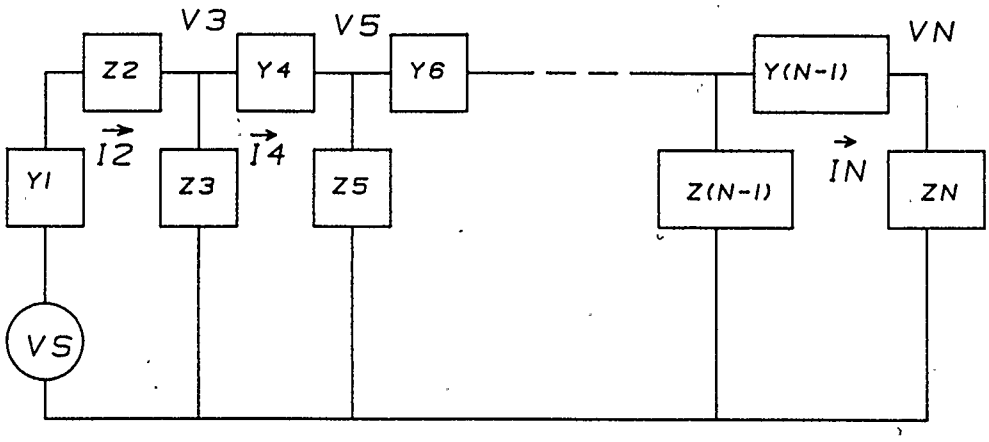


Figure 5.2 General z-type ladder network

overall network as shown in Fig. 5.3. Note that the selection of TR3 as z-type requires that all subsequent shunt branches be of z-type and all series branches be of y-type.

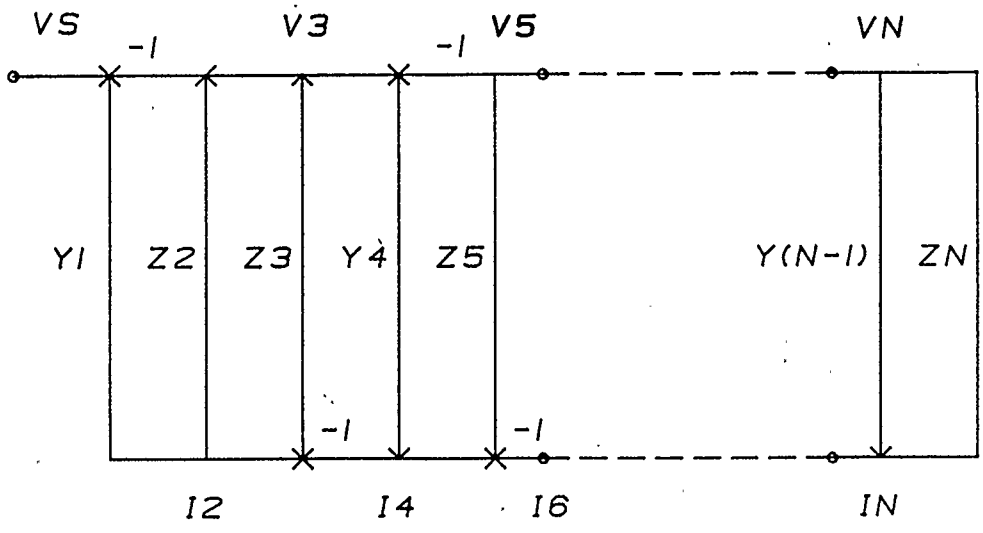


Figure 5.3 Z-type *V/I* SFG of the general ladder network

5.2.2. Y-type V/I SFG of the General Ladder Network

The construction of the y-type *V/I* SFG for the ladder network in Fig. 5.1 is described. As discussed in the previous section, the transmittances TR1 and TR2 are chosen to be of y- and z-type, respectively, to represent the series connection with a y-type *V/I* SFG. In order to construct a y-type *V/I* SFG for the ladder network, choose TR3 as a y-type transmittance as shown in Fig. 5.4. Since the transmittance TR3 appears in parallel with the y-type *V/I* SFG of TR1 and TR2, the resulting *V/I* SFG is of y-type. The transmittance TR4 appears in series with the y-type *V/I* SFG constructed so far. Hence it has to be of z-type. The transmittance type designations of the ladder network in Fig. 5.1 to realize a y-type *V/I* SFG are shown in Fig. 5.4. The resulting *V/I* SFG is shown in Fig. 5.5.

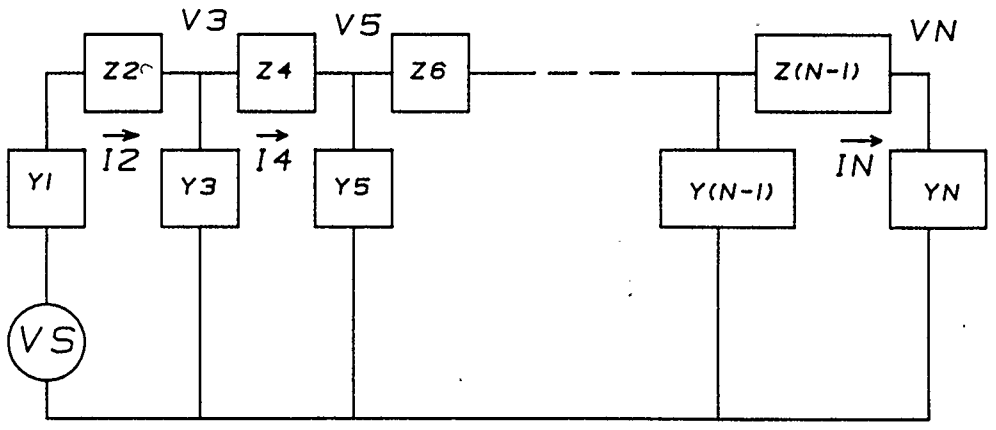


Figure 5.4 General y-type ladder network

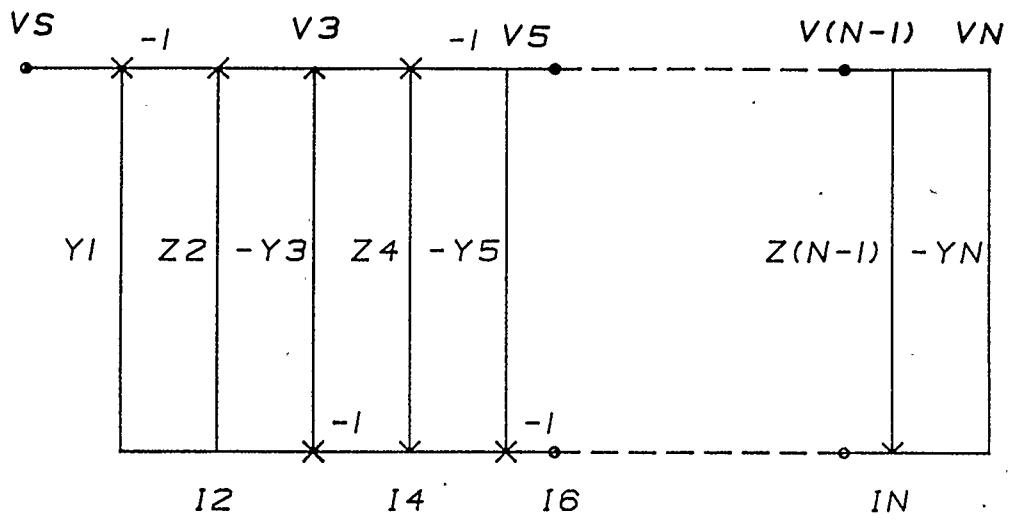


Figure 5.5 Y-type *V/I* SFG of the general ladder network

Note that the selection of TR3 as y-type requires all subsequent shunt branches be of y-type and all series branches be of z-type. It is important to mention that the *V/I* SFG of any leapfrog ladder structure falls into one of the two types of *V/I* SFG's mentioned above.

5.3. V/I SFG Simulation of Foster Circuits

The branch elements of ladder filters have driving point immitances that are realizable with inductors, capacitors or either one of the two Foster LC type one port networks shown in Fig. 5.6. Since the final *V/I* SFG of the ladder network should consist of only analog integrators, the capacitors are chosen as z-type transmittances resulting in integrating transmittances $(1 / s C_i)$, and the inductors are chosen as y-type transmittances resulting in integrating transmittances $(1 / s L_i)$.

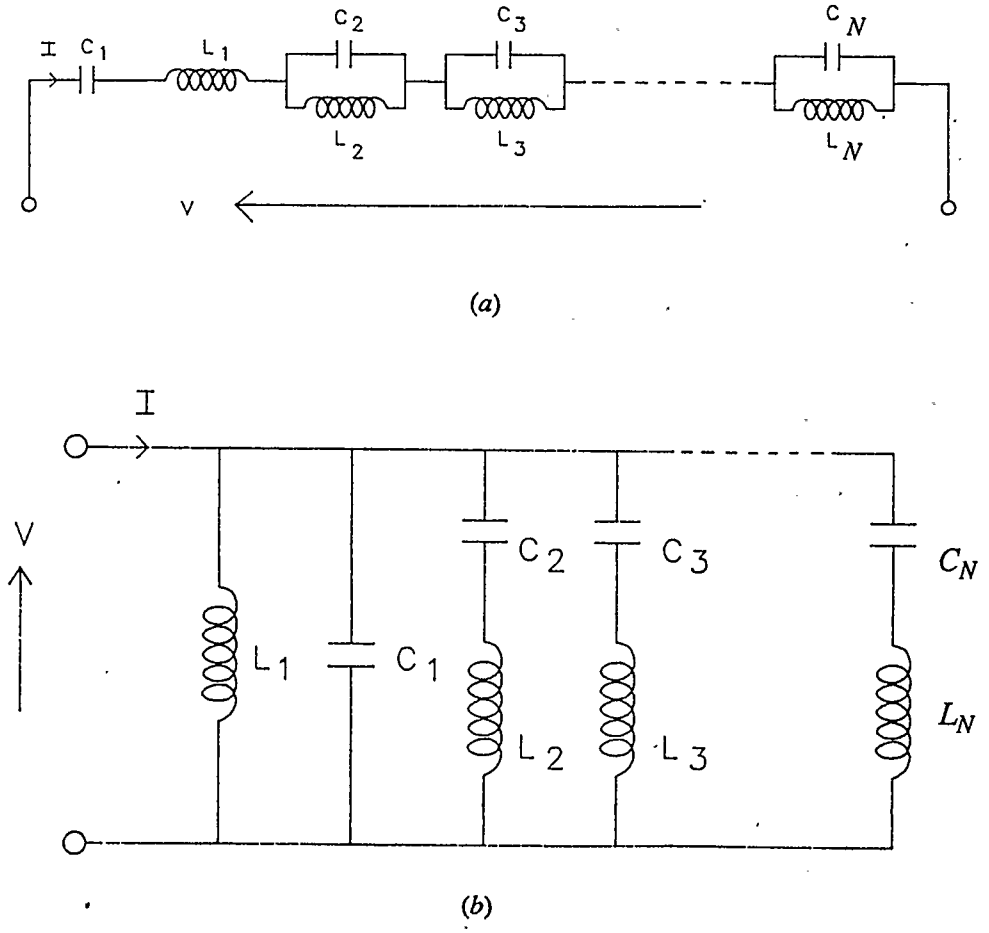


Figure 5.6 Foster networks
(a) Foster-I Network
(b) Foster-II Network

5.3.1. V/I SFG of Foster-I circuit

In the Foster-I circuit shown in Fig. 5.6(a), the inductors L_2, L_3 ,....., L_N are chosen to be of y-type and capacitors C_1, C_2, C_3 ,....., C_N to be of z-type transmittances. According to Rule-2, the parallel combination of a capacitor and an inductor is simulated by a z-type *V/I* SFG consisting of only analog integrators. Hence each parallel combination of an inductor and a capacitor in Foster-I circuit

can be simulated by z-type *V/I* SFG's. If inductor L_1 is chosen to be of y-type transmittance, according to the Rules-2 and -5, a y-type *V/I* SFG consisting of only integrators can be constructed to represent the Foster-I circuit as shown in Fig. 5.7(a). Note that the *V/I* SFG in Fig. 5.7(a) consists of only integrators as desired. If we choose the inductor L_1 to be of z-type, according to Rules-2 and -4, the resulting z-type *V/I* SFG consists of an undesirable differentiator. *Hence only the y-type V/I SFG of a Foster-I circuit can be constructed using only analog integrators.*

5.3.2. V/I SFG of Foster-II circuit

In the Foster-II circuit shown in Fig. 5.6(b), all the inductors $L_1, L_2, L_3, \ldots\ldots\ldots, L_N$ are chosen to be y-type and all the capacitors $C_2, C_3, C_4, \ldots\ldots\ldots, C_N$ are chosen to be z-type transmittances. From Rule-5, the series connection of an inductor L_i and a capacitor C_i is simulated by a y-type *V/I* SFG. If C_1 is chosen to be of z-type transmittance, it is clear from Rule-2 that a z-type *V/I* SFG consisting of only integrators can be constructed and is shown in Fig. 5.7(b). Observe that the *V/I* SFG in Fig. 5.7(b) consists of only integrators as desired. If C_1 is chosen to be of y-type transmittance, the *V/I* SFG which simulates the Foster-II circuit is found to consist of an undesirable differentiator. *Hence only the z-type V/I SFG of the Foster-II circuit can be constructed using only analog integrators.*

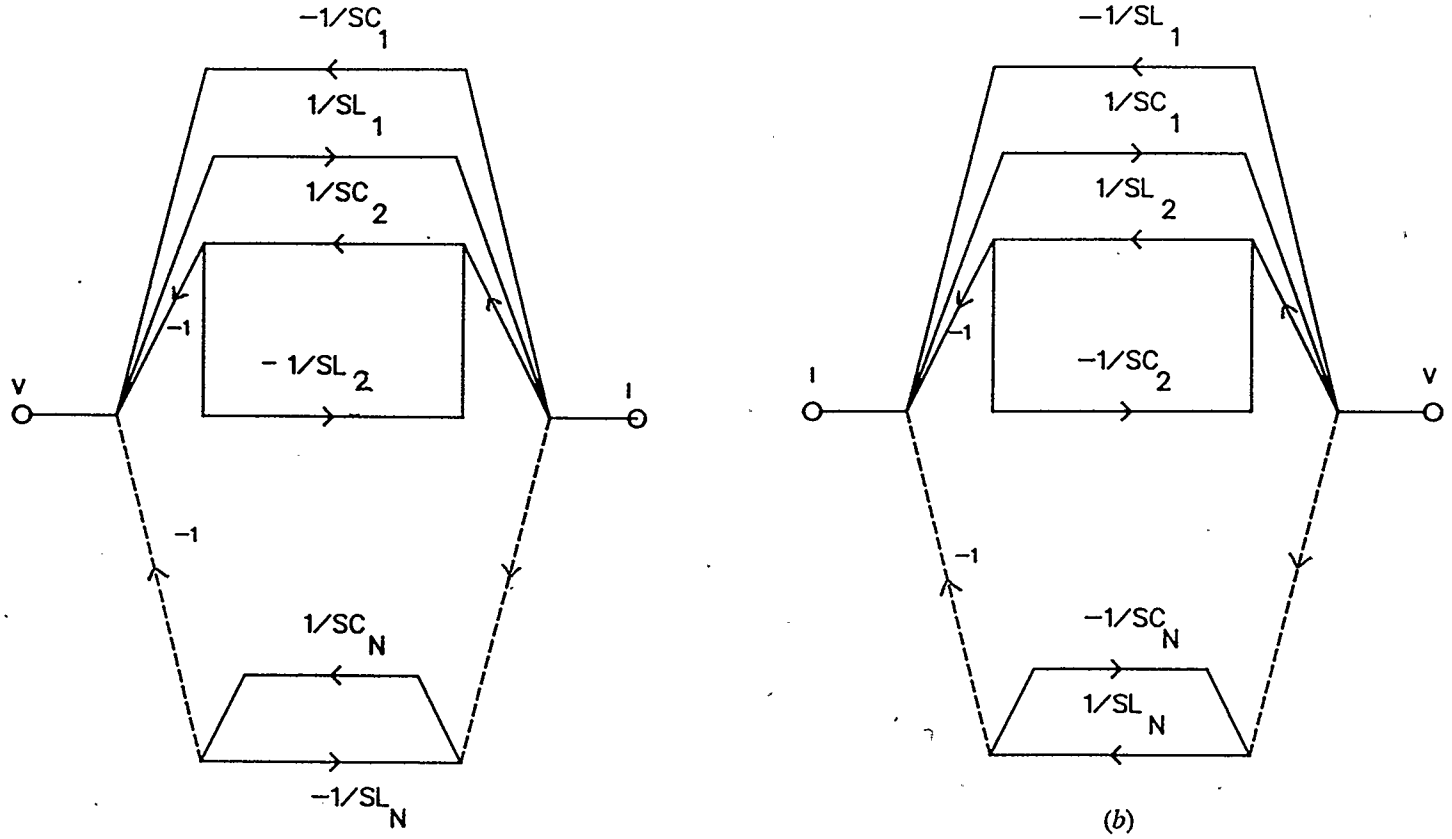


Figure 5.7 *V/I* SFG of Foster circuits
(a) Y-type *V/I* SFG of Foster-I circuit
(b) Z-type *V/I* SFG of Foster-II circuit

Therefore only the y-type V/I SFG of a Foster-I circuit and only the z-type V/I SFG of a Foster-II circuit can be constructed using only analog integrators.

5.4. V/I SFG Simulation of Precompensated Foster networks

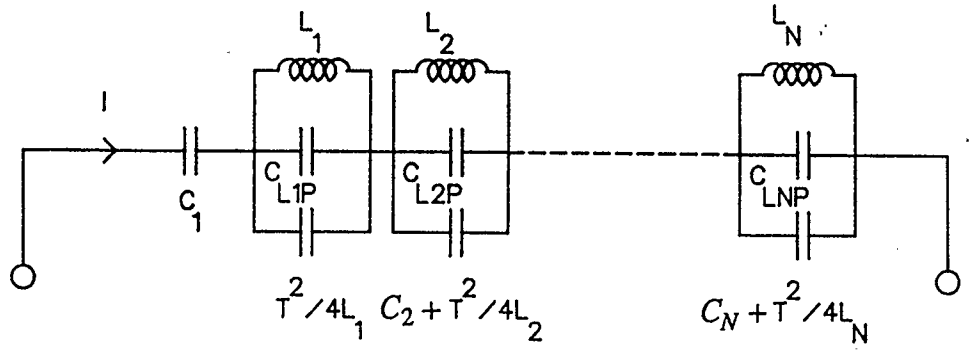
Inductors, capacitors and Foster circuits constitute the series and parallel branches of the analog ladder filters. It is required by the precompensation design method that the *V/I* SFG of the precompensated analog ladder filter network consist of only integrators i.e, no differentiators. The LDI integrators are used to replace these analog integrators in the *V/I* SFG for the discrete simulation of analog filters. Since the elements of the original analog ladder filter are precompensated as proposed in the precompensation design procedure, the *V/I* SFG construction of the precompensated Foster circuits is considered next.

5.4.1. V/I SFG of the Precompensated Foster-I circuit

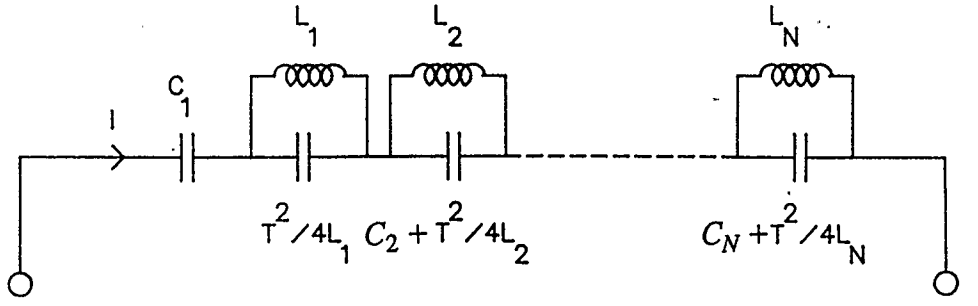
From Section 5.3.1, only the y-type *V/I* SFG consisting of integrators can be constructed for the Foster-I circuit. According to the precompensation procedure discussed in Section 4.4, every inductor in the original analog filter is to be replaced with an inductor in parallel with a negative capacitor while the capacitors of the original filter remain unchanged in the precompensated network. Also it is stated in step-3 of the precompensation design procedure that the element substitutions should be done such that the resulting network consists of only prototype elements shown in Table 4.1. Applying this precompensation procedure to the Foster-I circuit in Fig. 5.6(a), the precompensated Foster-I network shown in Fig.

5.8(a) is obtained. According to Step-4 of the design procedure, the prototype elements are replaced with their equivalent original elements from Table 4.1 to obtain

$$C_{L1P} = -T^2/4L_1$$
$$C_{L2P} = -T^2/4L_2$$
$$C_{LNP} = -T^2/4L_N$$



(a)



(b)

Figure 5.8 Precompensated and LDI equivalent of Foster-I circuit
(a) Precompensated Foster-I circuit
(b) LDI equivalent of the Precompensated Foster-I circuit

the LDI equivalent of the precompensated Foster-I network as shown in Fig. 5.8(b). It is required to construct the *V/I* SFG of the network in Fig. 5.8(b).

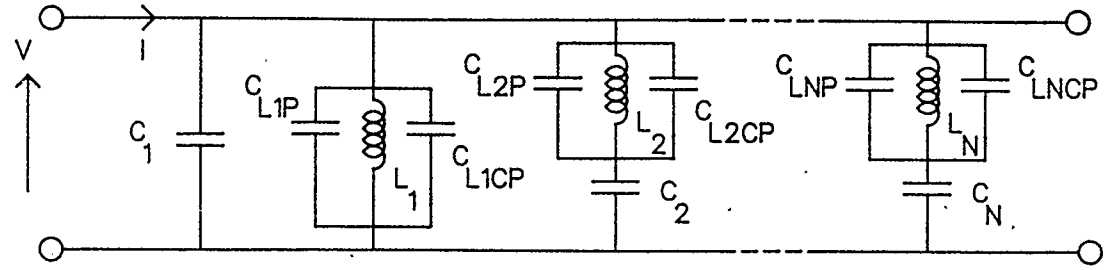
It is stated in Section 5.3 that all the inductors in the precompensated circuit are chosen to be of y-type ($1 / sL_i$) and all the capacitors to be of z-type ($1 / sC_i$) transmittances, so that the final *V/I* SFG consists of only integrators. Observe that due to the element substitution according to the precompensation design procedure, only the y-type transmittance $1 / sL_1$ (due to the inductor L_1 in the series connection) changes to a z-type transmittance due to the addition of a negative capacitor in parallel with the inductor L_1. Since all the element groups in the precompensated Foster-I circuit constitute z-type transmittances, from Rule-4 it is clear that *only a z-type V/I SFG for the precompensated Foster-I circuit can be constructed using only analog integrators.*

5.4.2. V/I SFG of the Precompensated Foster-II circuit

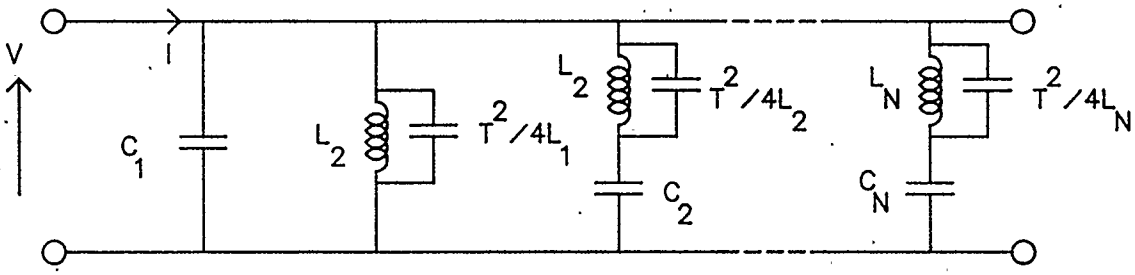
The precompensated Foster-II circuit is shown in Fig. 5.9(a). Note that the network in Fig. 5.9(a) consists of only prototype elements shown in the Table 4.1. The LDI equivalent network of the precompensated Foster-II circuit is shown in Fig. 5.9(b). Using the network equivalents shown in Fig. 5.10 [46] the precompensated Foster-II circuit in Fig. 5.9(b) can be simplified to a network having the network topology of the original Foster-II circuit shown in Fig. 5.6(b). The element values of the resulting network can be calculated using the equations

$$C_{L1P} = -T^2/4L_1 \qquad C_{L1CP} = +T^2/4L_1$$
$$C_{L2P} = -T^2/4L_2 \qquad C_{L2CP} = +T^2/4L_2$$

$$C_{LNP} = -T^2/4L_N \qquad C_{LNCP} = +T^2/4L_N$$



(*a*)



(*b*)

Figure 5.9 Precompensated and LDI equivalent of Foster-II circuit
(a) Precompensated Foster-II circuit
(b) LDI Equivalent of the Precompensated Foster-II circuit

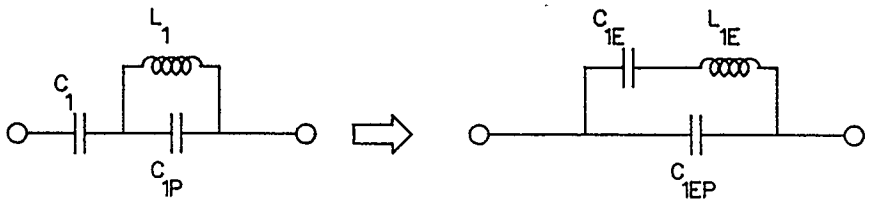


Figure 5.10 Network equivalents-I

$$L_{1E} = L_1 \left[\frac{C_{1P} + C_1}{C_{1P}} \right]^2$$

$$C_{1E} = \frac{C_1}{1 + \left[\frac{C_{1P}}{C_1} \right]}$$

$$C_{1EP} = \frac{C_1}{1 + \left[\frac{C_1}{C_{1P}} \right]}$$

From the rules in Section 5.2, it is evident that *only a z-type V/I SFG can be constructed for the precompensated Foster-II circuit using only integrators.*

Therefore only a z-type V/I SFG can be constructed for both the precompensated Foster-I and Foster-II type of circuits using only analog integrators.

5.5. V/I SFG Simulation of Precompensated General Ladder Network

An analog ladder filter consisting of z-type transmittances in the parallel branches and y-type transmittances in the series branches is said to made up of Z-Y-Z ladder blocks. Similarly an analog ladder filter consisting of y-type transmittances in the parallel branches and z-type transmittances in the series branches is said to made up of Y-Z-Y ladder blocks. In other words any ladder filter is made up of either Z-Y-Z or Y-Z-Y ladder blocks. Note that after the precompensation, all y-type transmittances are converted to z-type transmittances (due to the addition of negative capacitors in parallel with y-type transmittances). Hence due to precompensation a ladder network consisting of Z-Y-Z or Y-Z-Y ladder blocks will transform into a network consisting of only Z-Z-Z ladder blocks. Unfortunately, the Z-Z-Z ladder blocks do not conform to the standard ladder topology. In order to avoid these undesirable Z-Z-Z ladder blocks a network transformation is suggested to transform Z-Z-Z ladder blocks into realizable Z-Y-Z ladder blocks. Since only z-type *V/I* SFG can be constructed for both the precompensated Foster type circuits, they can represent the z-type parallel branches of a general ladder block. Since a y-type series branch is required to construct a Z-Y-Z ladder block, it is necessary to transform two Z-Z-Z ladder blocks with precompensated Foster-I and Foster-II circuits in their series branches so that the transformed ladder blocks are of Z-Y-Z type.

5.5.1. Z-Z-Z Ladder Block with Foster-I Circuit in the Series Branch

To develop the transformation method consider the Z-Z-Z ladder block shown in Fig. 5.11, having a precompensated Foster-I circuit in the series branch and capacitive z-type transmittances in the parallel branches. The method proposed is to transform the z-type series branch into a set of y-type series branches and z-type parallel branches. Since the capacitors in parallel with the inductors make the series branch z-type (Rule-2), the suggested method will transform the network to an equivalent form where these capacitors do not exist. This network transformation will introduce CCVS's between nodes 2-0 3-0, 4-0, ... , N-0 as shown in Fig. 5.12. These CCVS's are formed by passing current through the capacitive transmittances and hence represent z-type transmittances in the parallel branches. Note that the capacitor C_1 between nodes 1 and 2 in the network in Fig. 5.12 represents a series z-type transmittance, thus forming a Z-Z-Z ladder block in the

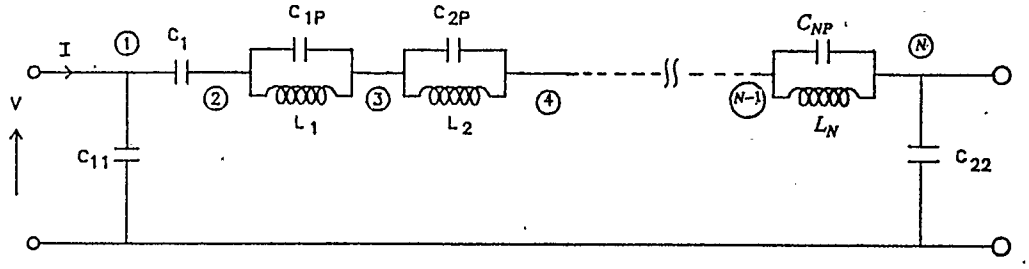


Figure 5.11 Z-Z-Z ladder block with Precompensated Foster-I circuit in the series branch

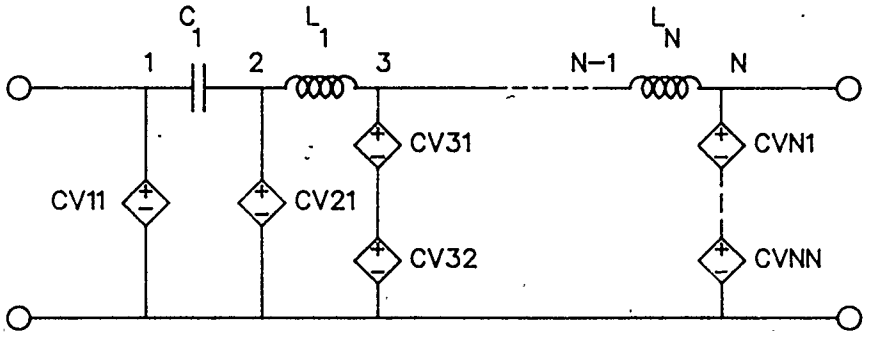


Figure 5.12 A transformed equivalent network of Fig. 5.11

Z-Y-Z ladder network. The simple transformation shown in Fig. 5.10 may be used to overcome this problem. By making use of this transformation the equivalent network of the Z-Z-Z ladder can be represented as shown in Fig. 5.13. The node equation for node 1 is

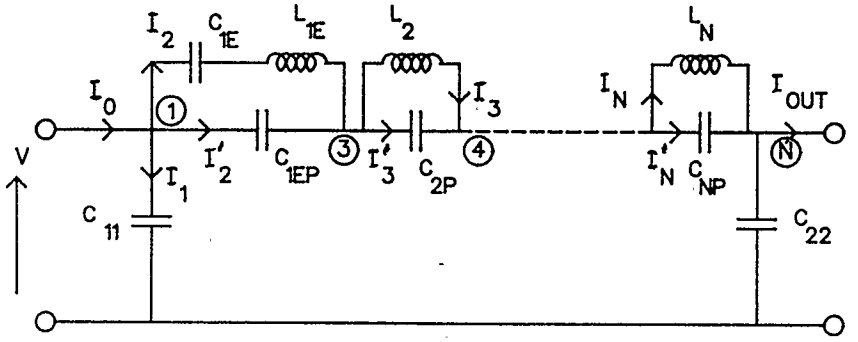


Figure 5.13 An equivalent network of Fig. 5.11

$$I_0 = I_1 + I_2 + I_2'$$

$$= V_1 (sC_{11}) + I_2 + (V_1 - V_3)\, sC_{1EP} \quad .$$

Similarly, using the node equations for nodes 3, 4, ... N in Fig. 5.13 and solving for the node voltages it is possible to show that

$$V_1 = \frac{1}{s(C_{11} + C_{1EP})}(I_0 - I_2) + \frac{C_{1EP}}{(C_{11} + C_{1EP})} V_3 \qquad (5.1)$$

$$V_3 = \frac{1}{s(C_{2P} + C_{1EP})}(I_2 - I_3) + \frac{C_{1EP}}{(C_{2P} + C_{1EP})} V_1 + \frac{C_{2P} V_4}{(C_{2P} + C_{1EP})} \qquad (5.2)$$

$$V_4 = \frac{1}{s(C_{2P} + C_{3P})}(I_3 - I_4) + \frac{C_{2P}}{(C_{2P} + C_{3P})} V_3 + \frac{C_{3P} V_5}{(C_{2P} + C_{3P})} \qquad (5.3)$$

$$V_N = \frac{1}{s(C_{NP} + C_{22})}(I_0 - I_{out}) + \frac{C_{NP}}{(C_{NP} + C_{22})} V_{N-1} \quad . \qquad (5.4)$$

Note that in equations (5.1)-(5.4) the terms containing $1 / s$ represent CCVS's. Also observe that a CCVS is formed by passing current through the z-type transmittance. In addition to the terms containing CCVS's there are also terms which represent VCVS's.

By careful observation of equations (5.1)-(5.4) it is evident that the voltage at each node is formed by a fraction of the voltages from the nodes on either side. For example notice that the voltage V_1 gets a fraction $\frac{C_{1EP}}{C_{11} + C_{1EP}}$ of the voltage V_3 and the voltage V_3 gets a fraction $\frac{C_{1EP}}{C_{2P} + C_{1EP}}$ of the voltage V_1. The discrete

V/I SFG constructed using equations (5.1)-(5.4) will consist of feed-forward and feedback paths between two adjacent nodes resulting in delay free loops which are not desirable in digital filter implementations. To eliminate the occurrence of delay free loops the node voltages which feed-forward and feedback are broken in the signal flow and are instead replaced by feed-forward or feedback paths from current nodes in the *V/I* SFG. Substitute (5.1) in (5.2) to arrive at

$$V_3 = \frac{1}{s\,Y\,(\,C_{2P} + C_{1EP}\,)}\,(\,I_2 - I_3\,) + \frac{X}{sY}\,(\,I_0 - I_2\,) + \frac{C_{2P}\,V_4}{Y\,(\,C_{2P} + C_{1EP}\,)} \tag{5.5}$$

where

$$X = \frac{C_{1EP}}{(\,C_{2P} + C_{1EP}\,)\,(\,C_{11} + C_{1EP}\,)}$$

and

$$Y = (\,1 - X\,C_{1EP}\,)\,.$$

Similarly substitute (5.5) in (5.3) to obtain

$$V_4 = \frac{1}{sA\,(\,C_{2P} + C_{3P}\,)}\,(\,I_3 - I_4\,) + \frac{X}{sYA}\,(\,I_2 - I_3\,) + \frac{X\,C_{2P}}{sYA\,(\,C_{2P} + C_{3P}\,)}\,(\,I_0 - I_2\,) + \frac{C_{3P}}{A(\,C_{2P} + C_{3P}\,)}\,V_5 \tag{5.6}$$

where

$$A = 1 - C_{2P}\,B$$

and

$$B = \frac{C_{2p}}{Y\,(\,C_{2P} + C_{1EP}\,)\,(\,C_{2P} + C_{3P}\,)}$$

In general

$$V_N = \frac{1}{s\,X1}\,(\,I_0 - I_2\,) + \frac{1}{s\,X2}\,(\,I_2 - I_3\,) + \ldots\ldots + \frac{1}{s\,XN}\,(\,I_0 - I_{out}\,) \qquad (5.7)$$

where $X1, X2, \ldots\ldots XN$ are algebraic expressions with capacitor values as variables. Observe that equation (5.7) consists of 'N' CCVS's. The equations (5.5)-(5.7) yield the network shown in Fig. 5.14 which is functionally equivalent to the network in Fig. 5.11. The expressions for CCVS's and VCCS's shown in Fig. 5.14 can be obtained from equations (5.1), (5.5)-(5.7).

It is important to mention that all the parallel branches of network in Fig. 5.14 are z-type transmittances and hence can be realized by z-type *V/I* SFG's. Furthermore, all the series branches in the equivalent network are y-type transmittances. In other words, the network in Fig. 5.14 is the Z-Y-Z equivalent of the Z-Z-Z ladder block in Fig. 5.11. Hence it is possible to construct a *V/I* SFG of the two port network consisting of only integrator branches. Note that the method used to eliminate the delay free loops may be applied to other structures. However, there can be slight variations to this transformation which implement feed-forward and feedback paths in the *V/I* SFG without forming delay free loops. This point is made clear in the next chapter, in which the design method is illustrated with

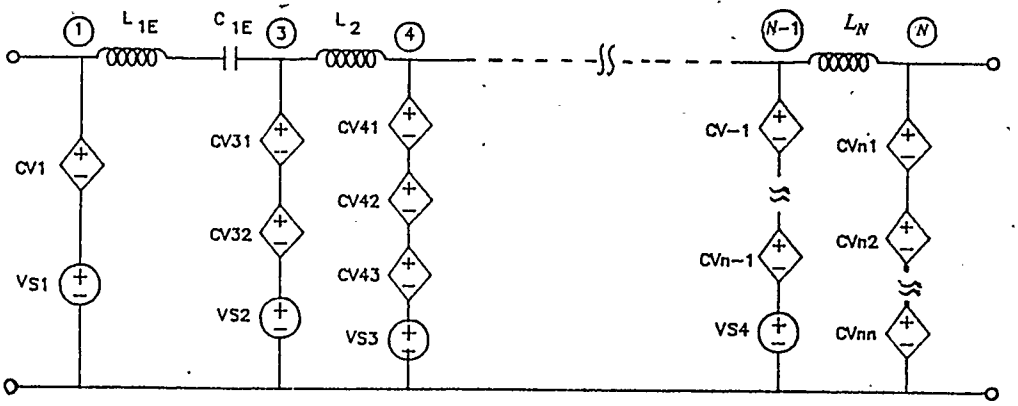


Figure 5.14 Z-Y-Z equivalent network of Z-Z-Z ladder block in Fig. 5.11

examples.

5.5.2. Z-Z-Z Ladder Block with Foster-II Circuit in the Series Branch

An LC network similar to the network in Fig. 5.11 in which the series branch is replaced with a precompensated Foster-II circuit is considered. As can be seen from Fig. 5.9(b), the presence of a single capacitor in the parallel connection of elements in the precompensated Foster-II circuit makes the branch to be of z-type. To convert the series branch to y-type the transformation procedure developed for the network in Fig. 5.11 can be used. Thus the suggested network transformation converts a two port network with z-type precompensated Foster-I or Foster-II circuits in the series branch and capacitive transmittances in the parallel branch to an

equivalent two port network with y-type transmittance in the series branch and z-type transmittances in the parallel branches.

The argument developed so far can be extended to the two port network, shown in Fig. 5.15, in which the parallel branches are precompensated Foster-II circuits, and the series branch is a precompensated Foster-I circuit. Since only z-type *V/I* SFG can be constructed for both Foster circuits, the two port network in Fig. 5.15 constitutes an undesirable Z-Z-Z ladder block. By applying the network transformation developed above, the two port network can now be represented as shown in Fig. 5.16. This network is a functional equivalent of the two port network shown in Fig. 5.16. Observe that the new branches in the Foster-II circuits which appeared due to the network transformation are made up of current and voltage controlled voltage sources representing z-type transmittances. Hence the the network in Fig. 5.16 can still be constructed by a z-type *V/I* SFG. The transformation has thus introduced y-type transmittances in the series branches, converting the Z-Z-Z type ladder block to an equivalent Z-Y-Z type ladder block. Similar arguments can be applied to a Z-Z-Z ladder block which has precompensated Foster-I circuits in the parallel branches and precompensated Foster-II circuit in the series branch. The *V/I* SFG of the complete precompensated ladder network can be obtained by further extending the argument developed above. A set of network equivalents given in [46,47] is useful for the application of the network transformation procedure developed above for different types of analog ladder networks.

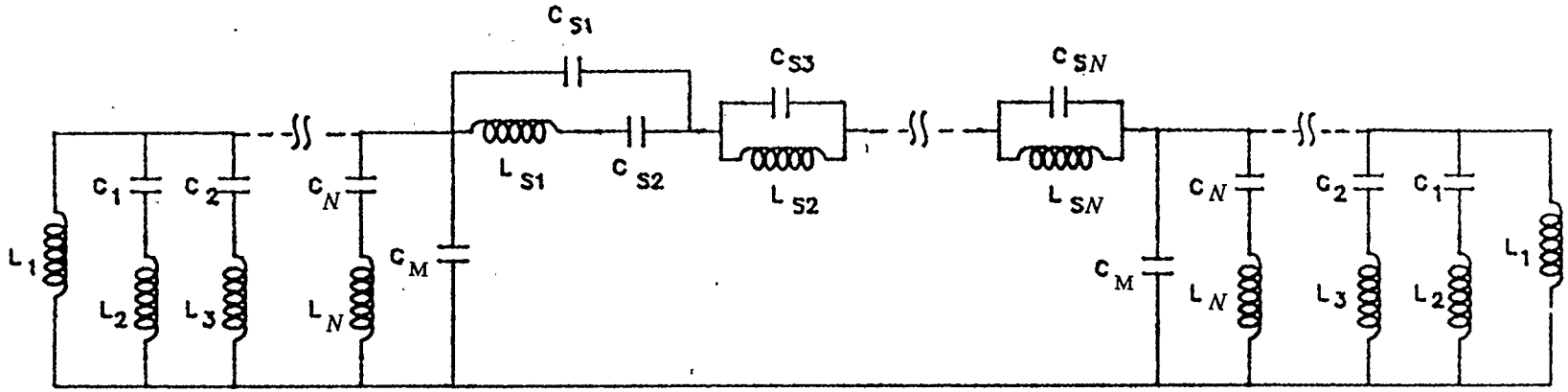


Figure 5.15 Ladder block with precompensated Foster-II circuit in the parallel branches and Foster-I Circuit in the Series Branch

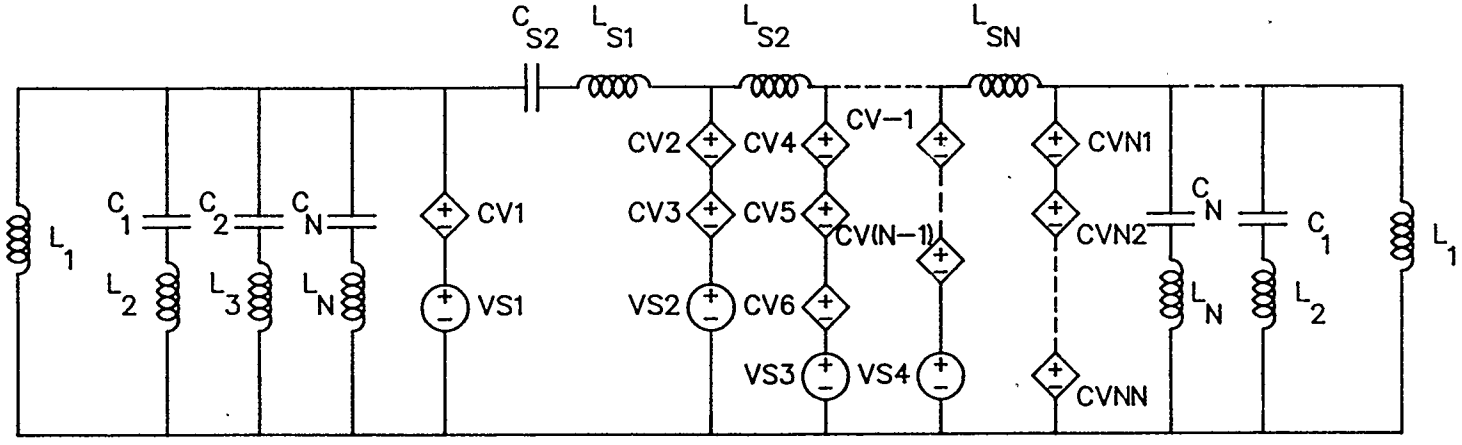


Figure 5.16 Transformed functional equivalent network of Fig. 5.15

In some ladder networks, a single capacitor appears as a series branch of the ladder. In this case, it is not possible to convert a Z-Z-Z ladder to a Z-Y-Z ladder. This method cannot be applied to ladder structures which have a single capacitor in their series branches. Some practical filter structures are examined for the applicability of the network transformation procedure developed above.

5.6. V/I SFG Realizability of Practical Filters

Three analog filter structures are examined for the realizability of their *V/I* SFG. A low-pass ladder without stopband zeroes, a band-pass filter with no finite zeroes and a high-pass filter with finite zeroes are presented as Examples 1 to 3. *Note that the subscript p in element values in Figures 5.18, 5.20 and 5.22 represent the precompensated elements.*

5.6.1. Example-1. Low-pass filter without stopband zeroes

Consider the analog low-pass filter shown in Fig. 5.17. According to the

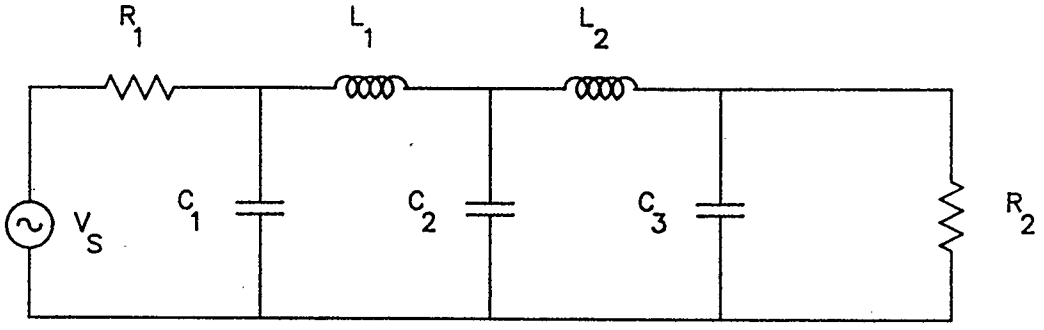


Figure 5.17 Low-pass filter without stopband zeroes

precompensation procedure, negative capacitors appear across each inductor in the network. These negative capacitors are compensated for with positive capacitors of the same value across the inductors. When these prototype elements are replaced with their equivalent elements from the Table 4.1, the resulting LDI equivalent of the precompensated network is as shown in Fig. 5.18. Note that the parallel branches of the ladder block in Fig. 5.18 are of z-type transmittances and the series branches are also of z-type transmittances. Hence this ladder section is of Z-Z-Z type. Since the series branch in the ladder block is not completely capacitive the network transformation discussed in Section 5.5 can be applied to convert the Z-Z-Z ladder block to a Z-Y-Z ladder block. Thus the filter can be realized using this design method.

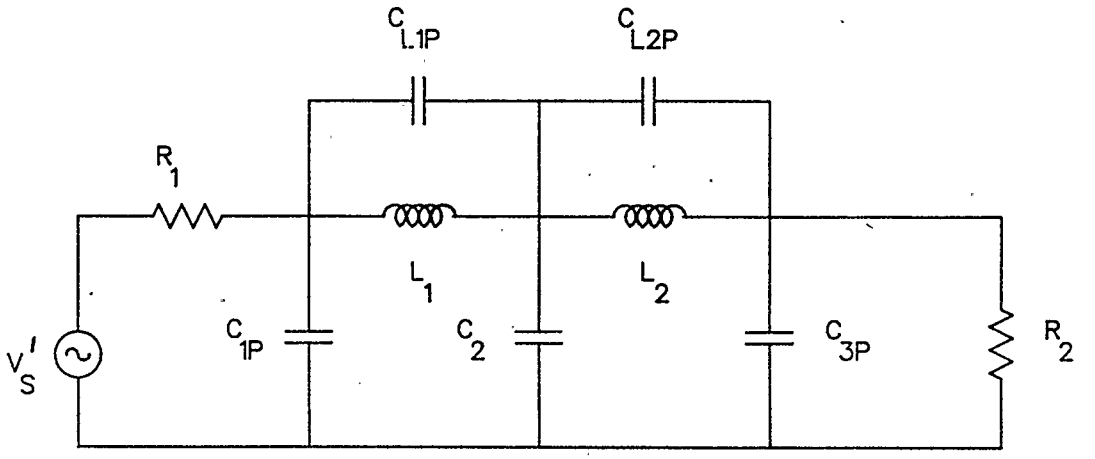


Figure 5.18 LDI equivalent of the precompensated network of the low-pass filter in Fig. 5.17

5.6.2. Example-2. Band-pass Filter With no Finite Zeroes

Consider the band-pass filter in Fig. 5.19. After precompensation and source transformation the LDI equivalent of the precompensated band-pass filter takes the form shown in Fig. 5.20. Observe that the parallel branches of the ladder block in the network in Fig. 5.20 are of z-type transmittances and the series branches of this ladder block are of Foster-I type. Hence this ladder block is also of Z-Z-Z type. Since this ladder block does not conform to the ladder topology, it is transformed to a Z-Y-Z ladder block as described in the Section 5.5. The series branch of this network is first replaced with its equivalent network shown in Fig. 5.10 to avoid the occurrence of a single capacitor in the series branches of the resulting equivalent network. The network transformation discussed in Section 5.5 can now be applied to transform the Z-Z-Z ladder block to Z-Y-Z ladder block. Thus the band-pass filter can be realized using this design method. The *V/I* SFG of the

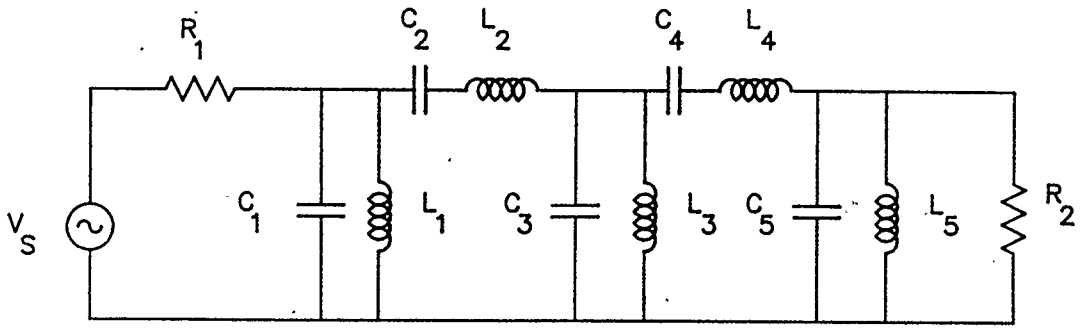


Figure 5.19 Band-pass filter with no stopband zeroes

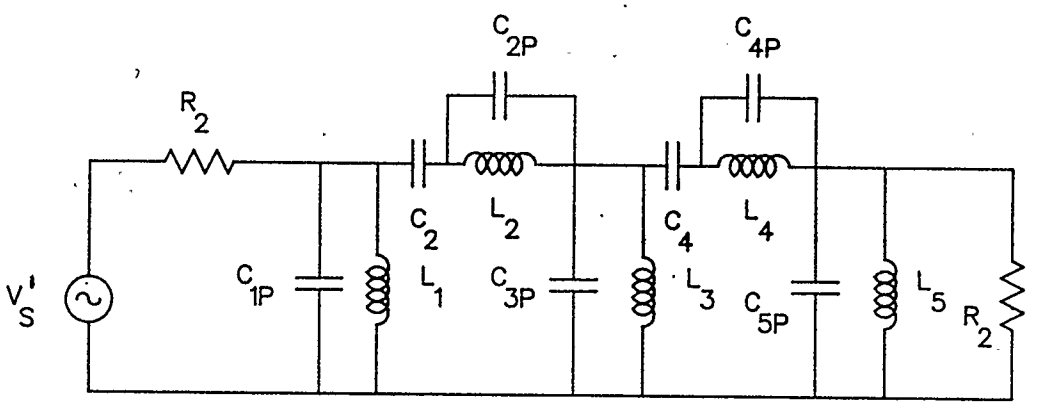


Figure 5.20 LDI Equivalent of the Precompensated Network of the Band-pass Filter in Fig. 5.19

transformed network can easily be constructed.

5.6.3. Example-3. High-pass Filter With Finite Zeroes

Consider the high-pass filter in Fig. 5.21. After precompensation, the LDI equivalent network of the precompensated network is obtained by element substitutions from Table. 4.1, and the resulting network is shown in Fig. 5.22. Since the series branch in the ladder block consists of a capacitor, the network transformation described in the previous section cannot be applied to this network. Hence this high-pass filter cannot be realized by this design method. The high-pass filters can be obtained by first designing an equivalent digital LDI low-pass filter and then transforming to a digital LDI high-pass filter as explained in Chapter 6.

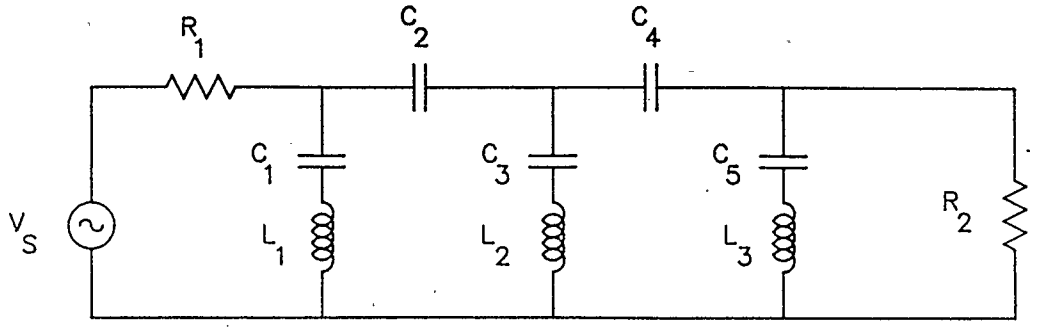


Figure 5.21 High-pass filter with finite zeroes

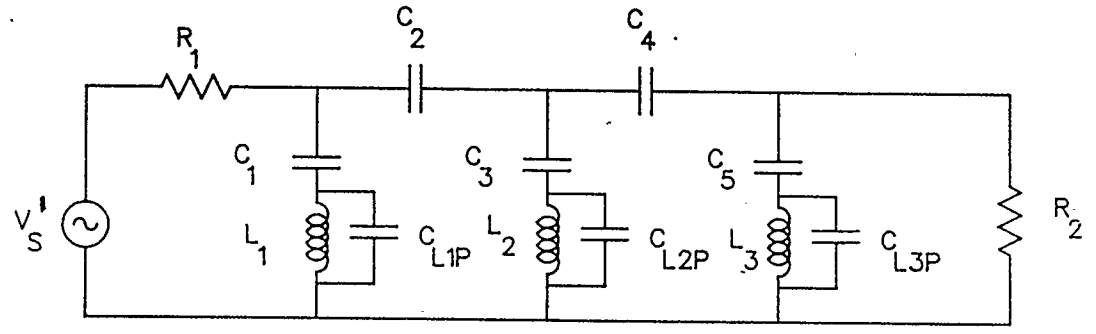


Figure 5.22 LDI equivalent network of the high-pass filter in Fig. 5.21

The three examples discussed above demonstrate the *V/I* SFG synthesis of precompensated ladder filter structures. Similar procedures can be developed for other useful filter structures to investigate the applicability of the precompensation design method.

5.7. Summary

The *V/I* SFG simulation of series and parallel transmittances is reviewed. It is found that only z-type *V/I* SFG's can be constructed for the precompensated Foster-I and Foster-II circuits. Hence the precompensated ladder network always consists of Z-Z-Z ladder blocks. A network transformation is developed so as to transform the network to consists of Z-Y-Z ladder blocks. This transformation introduces CCVS's and VCVS's in the equivalent network. A technique of eliminating delay free loops is also discussed. Three analog ladder filter networks are considered to examine the applicability of the proposed network transformation.

CHAPTER 6

DESIGN EXAMPLES OF DIGITAL LDI LADDER FILTERS

6.1. Introduction

In this chapter the precompensation method of designing digital LDI ladder filters is demonstrated with design examples of low-pass, high-pass, band-pass and band-stop filters which have elliptic magnitude response. The design steps follow the same lines as that of the design procedure described in Chapter 4. The LDI digital filters designed in this section are simulated on a VAX 11/780 computer to examine their magnitude-frequency response characteristics. The multiplier coefficient quantization effects on the magnitude frequency response characteristics of these filters are investigated. The sensitivity of the magnitude frequency response characteristics of a digital LDI ladder to coefficient quantization is compared with that of an equivalent wave digital filter. It is found that both types of filters exhibit almost identical behavior in the variations of their magnitude-frequency response with respect to the multiplier quantization effects.

6.2. Digital LDI Lowpass Filter Design

A fifth order elliptic digital ladder filter having the following specifications is chosen as an example

Low-pass Filter Specification

Passband Edge (f_p)	3.235 kHz
Stopband Edge (f_a)	6.47 kHz
Sampling Frequency (f_s)	32 kHz
Maximum Passband Ripple (A_p)	0.01087 dB
Minimum Stopband Attenuation (A_a)	54 dB .

Steps 1-2 (Chapter 4, Section 4.4)

These steps involve the design of an equivalent analog low-pass filter using the bilinear transformation. The normalized digital filter specifications are

$$\Omega_p T = 2\pi f_p / f_s = \frac{2\pi \times 3.235 \times 10^3}{32 \times 10^3} = 0.6352 \ \ rads.$$

$$\Omega_a T = 2\pi f_a / f_s = \frac{2\pi \times 6.47 \times 10^3}{32 \times 10^3} = 1.2704 \ \ rads.$$

The next step is to design an equivalent analog filter, whose passband edge is normalized to 1 *rad/sec*. The passband and stopband edges of the normalized analog low-pass filter are

$$\omega_p = 1 \ rad/\text{sec}$$

and

$$\omega_a = \frac{1}{\tan\left[\frac{\Omega_p T}{2}\right]} \cdot \tan\left[\frac{\Omega_a T}{2}\right] = 2.242 \quad rad/sec \quad .$$

Since the bilinear transformation only warps the frequency axis, the specifications of the passband and stopband attenuations are the same in both frequency domains. The approximation problem can be solved in the analog domain to obtain the analog LC values of an elliptic low-pass filter meeting the above specifications. Standard design tables and computer programs are available to design the analog low-pass filters with elliptic magnitude response [46,47,53]. The design procedure used in this thesis to design an analog elliptic low-pass filters is based on the method outlined in [46].

This example is based on a fifth order low-pass filter. The steepness factor is $\frac{\omega_a}{\omega_p} = 2.242$. A normalized low-pass filter for which the magnitude response transition from less than 0.01087 dB to more than 54 dB occurs within a frequency ratio of 2.242 is selected from the design tables [46, page no. 12-78]. The normalized filter component values are

$$C_1^n = 0.7187 \ F \qquad C_2^n = 0.0617 \ F$$

$$C_3^n = 1.4627 \ F \qquad C_4^n = 0.1729 \ F$$

$$C_5^n = 0.6229 \ F$$

$$L_2^n = 1.2421 \ H \qquad L_4^n = 1.0893 \ H \quad .$$

Note that the terminating resistor values are chosen to be unity. In order to obtain the actual component values of the filter meeting the specification, the element values are to be denormalized as explained below.

The basis for the use of normalized filter design is the fact that a given normalized filter response can be scaled (shifted) to a frequency range by dividing the reactive elements by a frequency scaling factor (FSF) [46], given by

$$FSF = \frac{desired\ \ frequency}{reference\ \ frequency} \quad .$$

In this example, the reference frequency is 1 *rad/sec.*, and the desired frequency is 21038.26 *rad/sec.* The denormalized filter element values are therefore

$$C_1 = \frac{C_1{}^n}{FSF \times R} = 34.162\ \mu F \qquad C_2 = \frac{C_2^n}{FSF \times R} = 2.933\ \mu F$$

$$C_3 = \frac{C_3{}^n}{FSF \times R} = 69.526\ \mu F \qquad C_4 = \frac{C_4^n}{FSF \times R} = 8.218\ \mu F$$

$$C_5 = \frac{C_5{}^n}{FSF \times R} = 29.698\ \mu F$$

$$L_2 = \frac{L_2^n \times R}{FSF} = 59.04\ \mu H \qquad L_4 = \frac{L_4^n \times R}{FSF} = 51.72\ \mu H$$

where R is terminating resistance (1 Ohm in this example). The capacitance and inductor values given above are with reference to the low-pass filter in Fig. 6.1.

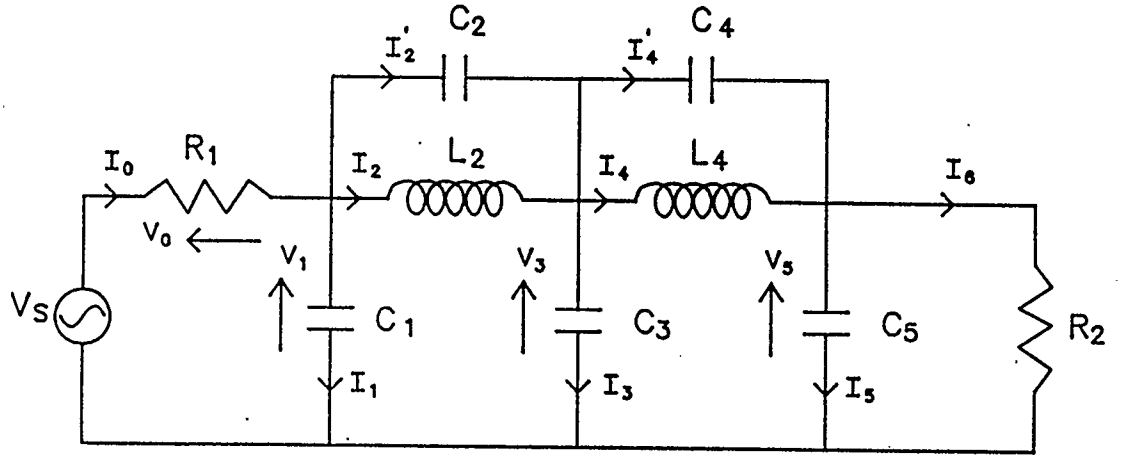


Figure 6.1 Fifth order elliptic analog low-pass ladder filter

Step-3

As mentioned in Step-3 of the general design procedure in Chapter 4, the elements of the original filter are replaced with their prototype equivalent components from Table 4.1 to arrive at the network in Fig. 6.2. Before applying the impedance transformation the effects of the negative capacitors which occur due to the prototype equivalent substitutions are compensated for. The effects of the negative capacitors in parallel with L_2, L_4 and R_2 are compensated by padding with additional capacitors of value $\frac{T^2}{4L_2}$, $\frac{T^2}{4L_4}$ and $\frac{T}{2R_2}$, respectively. The procedure to compensate the effect of the negative capacitor $-\frac{T}{2R_1}$ in parallel with the source resistor is not straightforward. This precompensation procedure involves the source

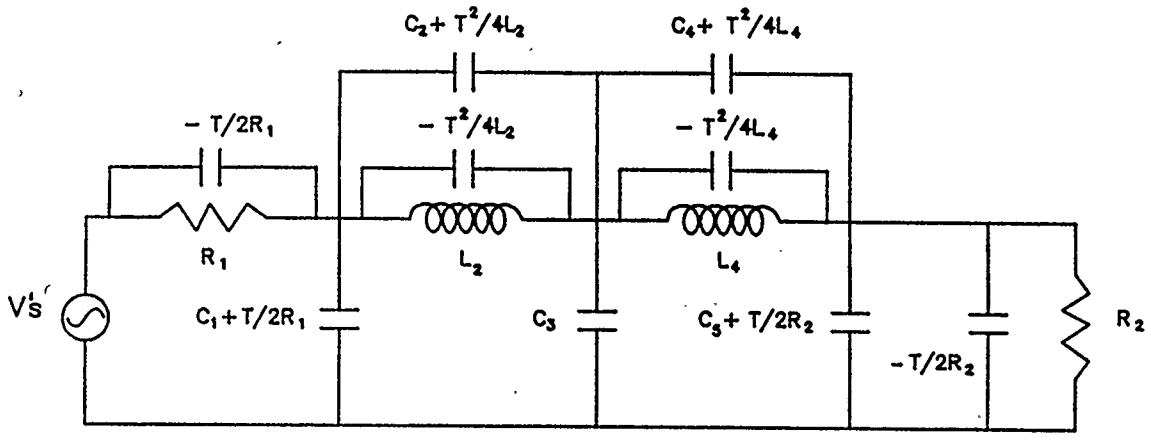


Figure 6.2 Precompensated analog low-pass ladder filter

transformation of the input voltage source described in the following section.

Source Precompensation Procedure

This subsection highlights the transformation of the input voltage source of the analog filter due to the precompensation of the original analog network. The source precompensation discussed in this section applies to any kind of doubly-terminated analog LCR network. This procedure is used in the design examples of digital LDI high-pass, band-pass and band-stop filters. To illustrate the source precompensation procedure, a first order analog low-pass filter as given in Fig. 6.3(a) is considered.

As discussed in Chapter 4, in Step-3 of the general design procedure the resistor R in Fig. 6.3(a) is replaced with its prototype equivalent from Table 4.1 (a

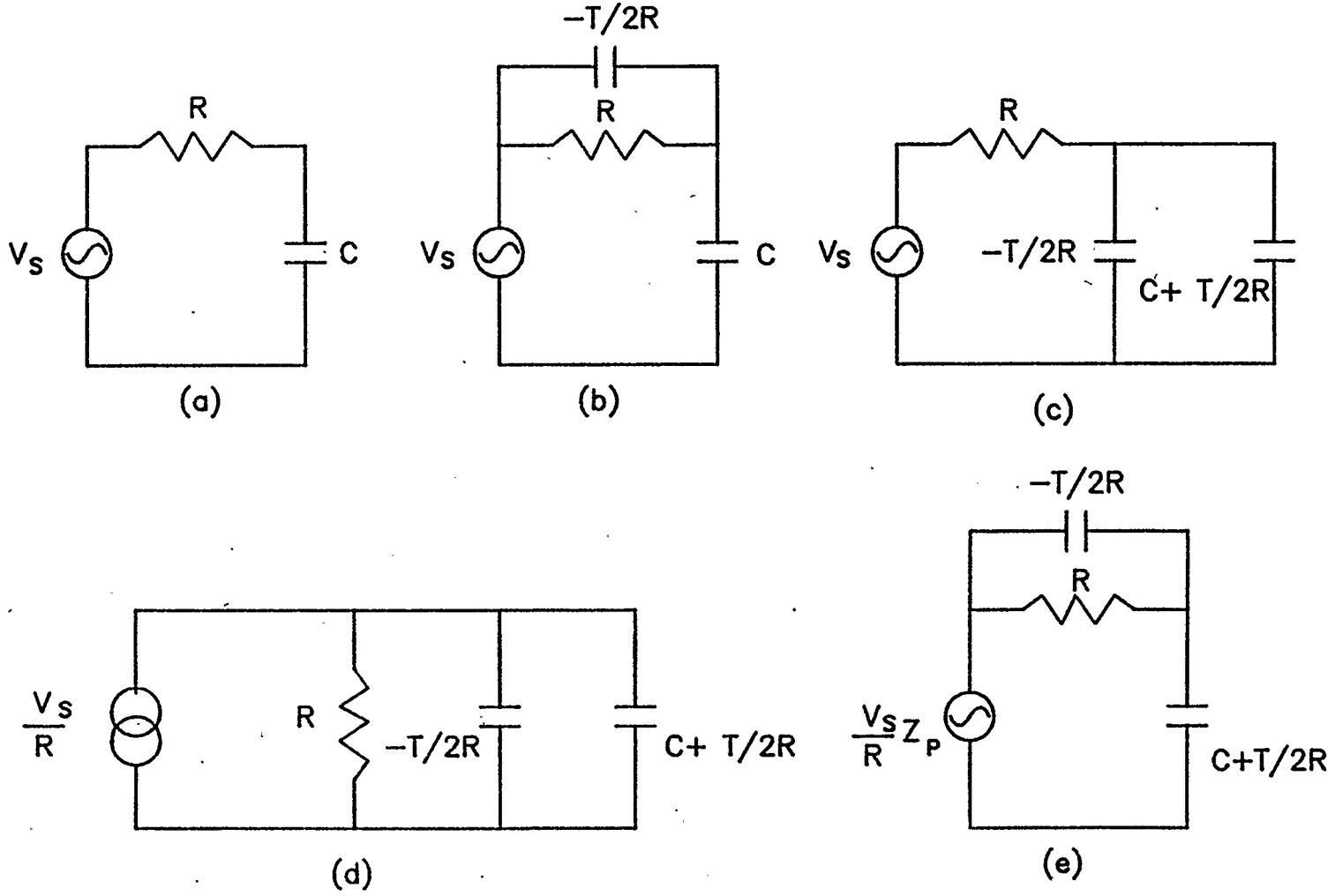


Figure 6.3 Source precompensation design procedure

negative capacitor $-\frac{T}{2R}$ in parallel with R) to arrive at the network in Fig. 6.3(b). The capacitor $-\frac{T}{2R}$ across the source resistor R will be compensated for by changing the capacitor C to C' where

$$C' = C + \frac{T}{2R} \tag{6.1}$$

and by modifying the source voltage V_s to V_s' where

$$V_s' = \frac{V_s}{R}\left[\frac{1}{R} - \frac{T\,s}{2R}\right]^{-1} \tag{6.2}$$

To demonstrate equations (6.1) and (6.2), first precompensate only the capacitor C by $(C + \frac{T}{2R})$ as shown in Fig. 6.3(c). Apply Thevenin's theorem to the circuit in Fig. 6.3(c) to arrive at Fig. 6.3(d). By using the Norton's theorem the equivalent network of Fig. 6.3(d) is obtained and is shown in Fig. 6.3(e) where

$$Z_p = \left[\frac{1}{R} - \frac{T\,s}{2R}\right]^{-1} \tag{6.3}$$

The precompensated and source transformed circuit in Fig. 6.3(e) is now the same as the circuit in Fig. 6.3(a). Note that the source voltage is modified to the new value V_s' given in Eqn. (6.2). Using the bilinear transformation, the equation (6.3) maps to the z-domain value

$$Z_p \rightarrow R\left[1 - \frac{z-1}{z+1}\right]^{-1} \tag{6.4}$$

Hence, the transformed value of the source V_s' is

$$V_s' = V_s\left[1 - \frac{z-1}{z+1}\right]^{-1} \tag{6.5}$$

which simplifies to

$$V_s' = V_s\frac{z+1}{2} \tag{6.6}$$

This source transformation maps a zero at infinity in the analog domain to a zero at $z = -1$ in the discrete domain as required by the bilinear transformation. It is interesting to note that this input network is the same as used in [52] to force frequencies of zero magnitude sensitivity in LDI filters. A z-domain realization of the transformed input voltage source is shown in Fig. 6.4. To summarize, in order to compensate for the effects of the negative capacitor $-\frac{T}{2R}$ across the source terminating resistor, the input voltage source is modified from V_s to V_s' and the capacitor C is padded with a positive capacitor of value $\frac{T}{2R}$.

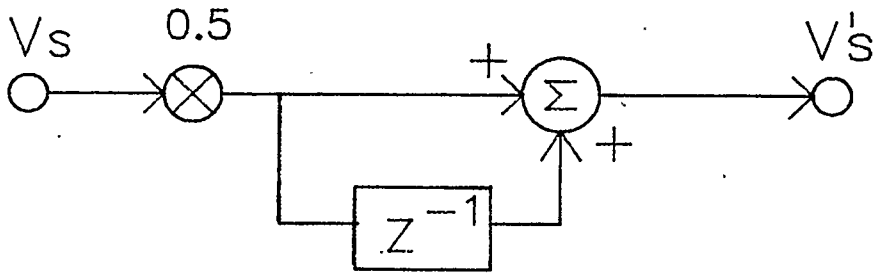


Figure 6.4 Precompensated voltage source

This source precompensation is used in the network in Fig. 6.2. Observe that the source V_s is transformed to V_s', and the capacitor C_1 is modified to $C_1 + \frac{T}{2R_1}$ in order to compensate for the negative capacitor $-\frac{T}{2R_1}$ across R_1. A list of original and precompensated element values is given in Table 6.1. Note that the networks in Fig. 6.1. and Fig. 6.2. are functionally the same. Also observe that the network in Fig. 6.2. consists of only prototype elements.

Step-4

In this step the impedance transformation is applied such that the transfer function of the original filter is unaltered. It is demonstrated in Chapter 4 that the bilinear transformed and impedance scaled impedance of a prototype element in Table 4.1 is equal to the LDI transformed impedance of the equivalent original element in the same Table 4.1. Using this relationship, the impedance transformation can be carried out as follows. Every prototype element in the network in Fig. 6.2 is replaced with its equivalent original element in Table 4.1 to result in the network shown in Fig. 6.5, which is referred to as the *LDI equivalent of the precompensated filter*. The element values modified due to precompensation are referred to as C_1', C_2', C_4' and C_5' in Fig. 6.5 and are listed in Table 6.1. Note that the bilinear transformed transfer function of the network in Fig. 6.2 is the same as the LDI transformed transfer function of the network in Fig. 6.5. Thus, the impedance transformation technique is applied to obtain a precompensated network with LDI

Original Element	Precompensated Element
C_1	$C_1' = \left[C_1 + \frac{T}{2R_1} \right]$
C_2	$C_2' = \left[C_2 + \frac{T^2}{4L_2} \right]$
C_4	$C_4' = \left[C_4 + \frac{T^2}{4L_4} \right]$
C_5	$C_5' = \left[C_5 + \frac{T}{2R_2} \right]$
V_s	$V_s' = V_s \left[\frac{z+1}{2} \right]$

Table 6.1 List of original and precompensated elements of fifth order low-pass ladder filter

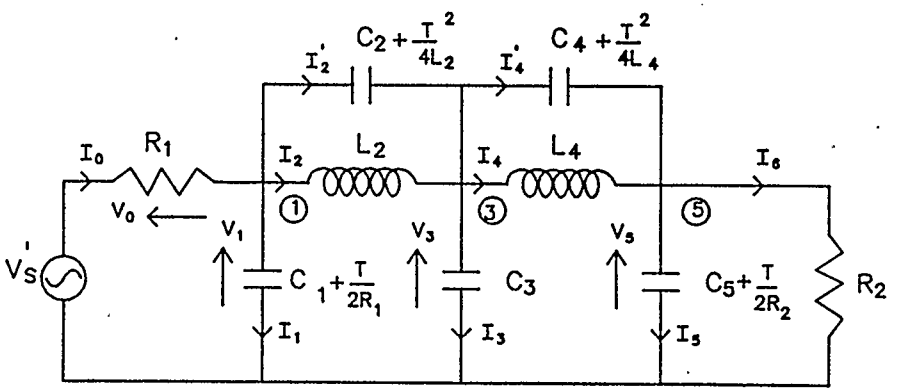


Figure 6.5 LDI equivalent of the precompensated filter in Fig. 6.2

transformed impedances. Each LDI transformed impedance can be implemented using the LDI integrators shown in Fig. 3.7(b).

Step-5

The *V/I* SFG of the precompensated network in Fig. 6.5 is constructed next. As mentioned in the general design procedure, the *V/I* SFG must contain only analog integrators and no differentiators. To construct a *V/I* SFG with analog integrators only the *V/I* SFG construction techniques developed in Chapter 5 are used. Note that the precompensated network in Fig. 6.5 is made up of *Z–Z–Z* type ladder blocks. The network transformation method, suggested in Chapter 5 is applied to transform these *Z–Z–Z* ladder blocks into *Z–Y–Z* ladder blocks.

The transmission zeroes may be implemented in analog LC ladder filters by adding shunt elements to the series branches of the filter. The transmission zeroes

decrease the transition bandwidth of the filter, by introducing sharp roll off characteristics, and thus improve the filter stopband characteristics. The *V/I* SFG without these shunt elements are found to consist of only analog integrators. The direct addition of the shunt capacitors to implement transmission zeros give rise to analog differentiators in the *V/I* SFG which result in unrealizable structures when using the LDI transformation. In order to overcome this problem, the *Z–Z–Z* type ladder blocks are transformed to *Z–Y–Z* type ladder blocks as explained below.

The node equation for node-1 of the network in Fig. 6.5 is

$$I_0 = I_1 + I_2 + I'_2 \quad .$$

Substitute expressions for the currents I_1 and I'_2 to get

$$I_0 = V_1 \, s \, C'_1 + I_2 + (V_1 - V_3) \, s \, C'_2 \quad .$$

Solve for V_1 to get

$$V_1 = \frac{1}{s(C_1' + C_2')} (I_0 - I_2) + \frac{C'_2}{(C_1' + C_2')} V_3 \quad . \tag{6.7}$$

The node equation for node-3 in Fig. 6.5 can be written as

$$I_2 + I'_2 = I_3 + I_4 + I'_4 \quad .$$

Substitute the current expressions for I'_2, I'_4 and I_3 to get

$$I_2 + (V_1 - V_3) \, s \, C'_2 = V_3 \, (sC_3) + I_4 + (V_3 - V_5) \, s \, C'_4 \quad .$$

Solve for V_3 to get

$$V_3 = \frac{1}{s(C_2' + C_3 + C_4')}\,(I_2 - I_4) + \frac{C_2'}{(C_2' + C_3 + C_4')}\,V_1 + \frac{C_4'}{(C_2' + C_3 + C_4')}\,V_5 \quad (6.8)$$

Similarly the expression for V_5 can be obtained as

$$V_5 = \frac{1}{s(C_4' + C_5')}\,(I_4 - I_6) + \frac{C_4'}{(C_4' + C_5')}\,V_3 \quad (6.9)$$

Observe from (6.7) and (6.8) that voltage variable V_1 is formed from a fraction of voltage variable V_3 and vice-versa. Similarly from (6.8) and (6.9) it is clear that voltage variables V_3 and V_5 are formed out of mutual fractional voltage contributions. A *V/I* SFG constructed based on equations (6.7) (6.8) and (6.9) is found to consist of feed forward and feedback paths which constitute undesirable delay free loops. To eliminate the dependency of the voltage variables substitute (6.7) and (6.9) in (6.8), and solve for V_3 to obtain

$$V_3 = \frac{C_2'}{sXY(C_1' + C_2')}\,(I_0 - I_2) + \frac{1}{sXY}\,(I_2 - I_4) + \frac{C_4'}{sXY(C_4' + C_5')}\,(I_4 - I_6) \quad (6.10)$$

where

$$X = C_3 + C_2' + C_4' - \frac{C_2'^2}{(C_1' + C_2')} \quad (6.11)$$

and

$$Y = 1 - \frac{C_4'^2}{X(C_4' + C_5')} \tag{6.12}$$

Using the network equations (6.7, 6.9, 6.10) the functional equivalent of the precompensated network in Fig. 6.5 is obtained and is shown in Fig. 6.6. The current controlled voltage sources in Fig. 6.6 can be computed from the equations

$$V_{51A} = \frac{1}{s(C_1' + C_2')}(I_0 - I_2) \tag{6.13}$$

$$V_{51B} = \frac{C_2'}{(C_1' + C_2')} V_3 \tag{6.14}$$

$$V_{53A} = \frac{C_2'}{sXY(C_1' + C_2')}(I_0 - I_2) \tag{6.15}$$

$$V_{53B} = \frac{1}{sXY}(I_2 - I_4) \tag{6.16}$$

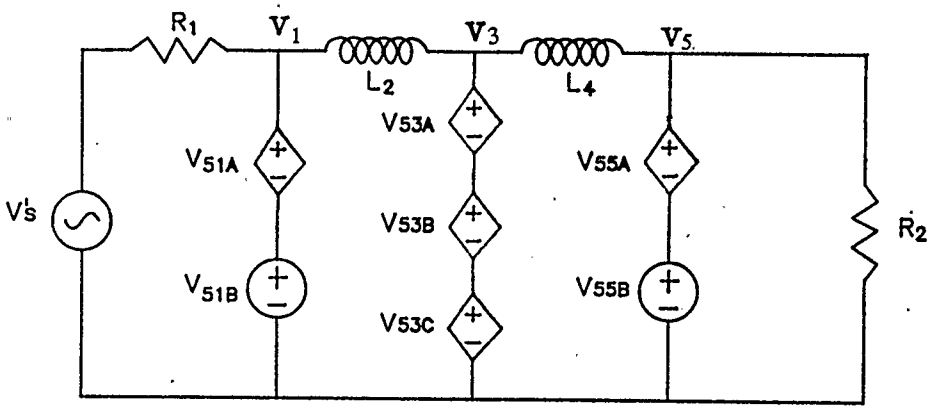


Figure 6.6 Functional equivalent form of the low-pass filter in Fig. 6.5

$$V_{53C} = \frac{C_4'}{sXY(C_4' + C_5')}(I_4 - I_6) \tag{6.17}$$

$$V_{55A} = \frac{1}{s(C_4' + C_5')}(I_4 - I_6) \tag{6.18}$$

$$V_{55B} = \frac{C_4'}{(C_4' + C_5')} V_3 \tag{6.19}$$

The *V/I* SFG of the network in Fig. 6.6 is constructed using equations (6.13)-(6.19) and is shown in Fig. 6.7. Note that the resulting *V/I* SFG consists only of analog integrator blocks $1/s$ which, when realized by LDI elements, result in realizable digital filter structures without delay free loops. The expressions for the branch multipliers in the *V/I* SFG in Fig. 6.7 are

$$m11 = \frac{1}{(C_1' + C_2')}, \qquad m12 = \frac{C_2'}{(C_1' + C_2')}, \tag{6.20}$$

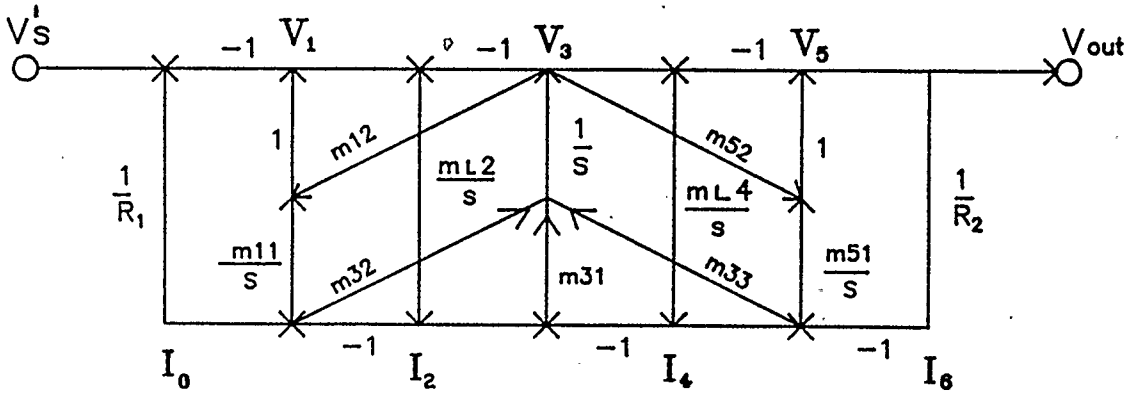


Figure 6.7 *V/I* SFG of the low-pass filter in Fig. 6.6

$$m32 = \frac{C_2'}{XY\,(C_1' + C_2')}\ , \qquad m31 = \frac{1}{XY}\ , \tag{6.21}$$

$$m33 = \frac{C_4'}{XY(C_4' + C_5')}\ , \qquad m51 = \frac{1}{(C_4' + C_5')}\ , \tag{6.22}$$

$$m52 = \frac{C_4'}{(C_4' + C_5')}\ , \tag{6.23}$$

$$ml_2 = \frac{1}{L_2}\ , \qquad ml_4 = \frac{1}{L_4}\ . \tag{6.24}$$

Different expressions for V_3 and V_5 can be derived by solving the voltage/current equations of the precompensated filter. If (6.7) is substituted in (6.8) we get

$$V_3 = \frac{1}{sX}\,(I_2 - I_4) + \frac{C_2'}{sX(C_1' + C_2')}\,(I_0 - I_2) + \frac{C_4'}{X}\,V_5\ . \tag{6.25}$$

And if (6.25) is substituted in (6.9) we get

$$\begin{aligned} V_5 = {} & \frac{1}{sY(C_4' + C_5')}\,(I_4 - I_6) + \frac{C_4'}{sXY(C_4' + C_5')}\,(I_2 - I_4) \\ & + \frac{C_2'\,C_4'}{sXY(C_4' + C_5')(C_1' + C_2')}\,(I_0 - I_2)\ . \end{aligned} \tag{6.26}$$

A different *V/I* SFG can be formed using this new set of equations (6.7), (6.25) and (6.26). This *V/I* SFG also yields a discrete structure without delay free loops when approximated by LDI elements and after scaling by $z^{-1/2}$. However, the structure obtained by the realization of the *V/I* SFG in Fig. 6.7 requires fewer

coefficient bits to implement the same transfer function.

Step-6

In this step the s- to z- transformation is performed on the *V/I* SFG shown in Fig. 6.7. Replace the analog integrator blocks in Fig. 6.7 by digital LDI blocks shown in Fig. 4.1. The unity terminating resistors are approximated by $z^{-½}$ delay elements and the summing nodes by adders to obtain the network shown in Fig. 6.8. The discrete network thus obtained represents the LDI digital low-pass filter.

Step-7

Although the network in Fig. 6.8 may be implemented strictly as designed, it is not economical in terms of the number of delay elements required. To eliminate the half delay elements in the network in Fig. 6.8, the filter is scaled by $z^{-½}$ delay elements. The resulting filter structure is shown in Fig. 6.9 and contains only unit delays. The $z^{-½}$ delay element which appears at the input due to scaling of the network can be neglected since it does not introduce any errors in the magnitude frequency response of the filter.

The coefficients of the multipiers in Fig. 6.9 are evaluated using equations

$$mp0 = 1.0 \tag{6.27}$$

$$mp1 = T.m11 = \frac{T}{C_1' + C_2'} = 0.549642146 \tag{6.28}$$

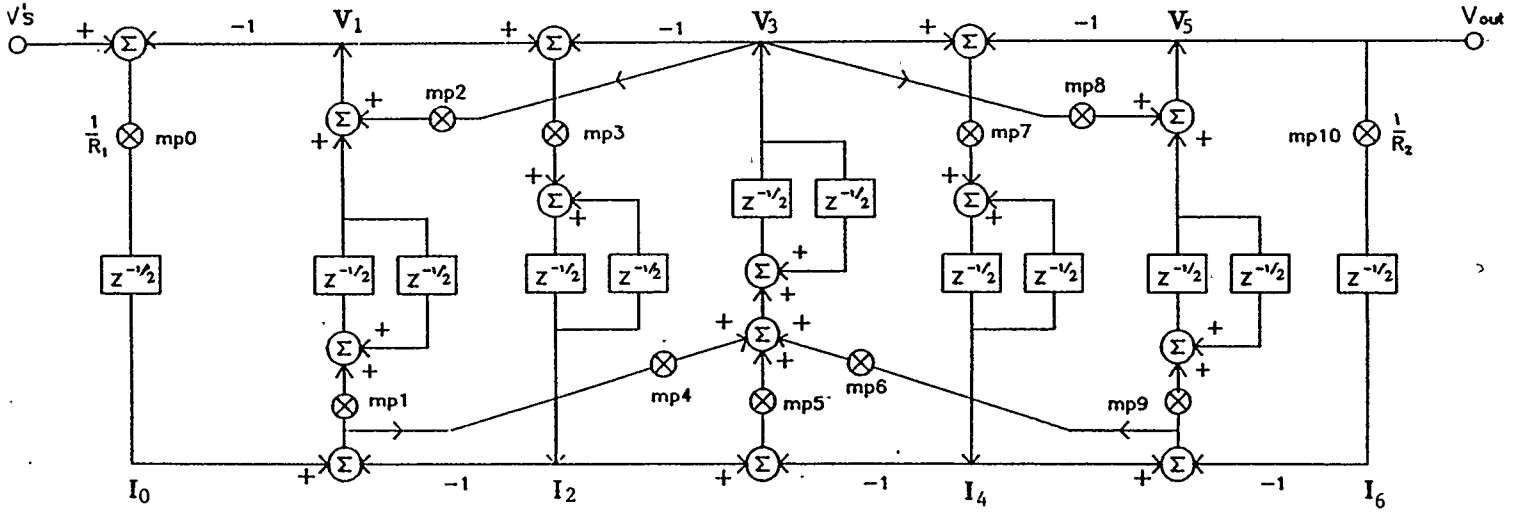


Figure 6.8 LDI transformed network of the *V/I* SFG in Fig. 6.7

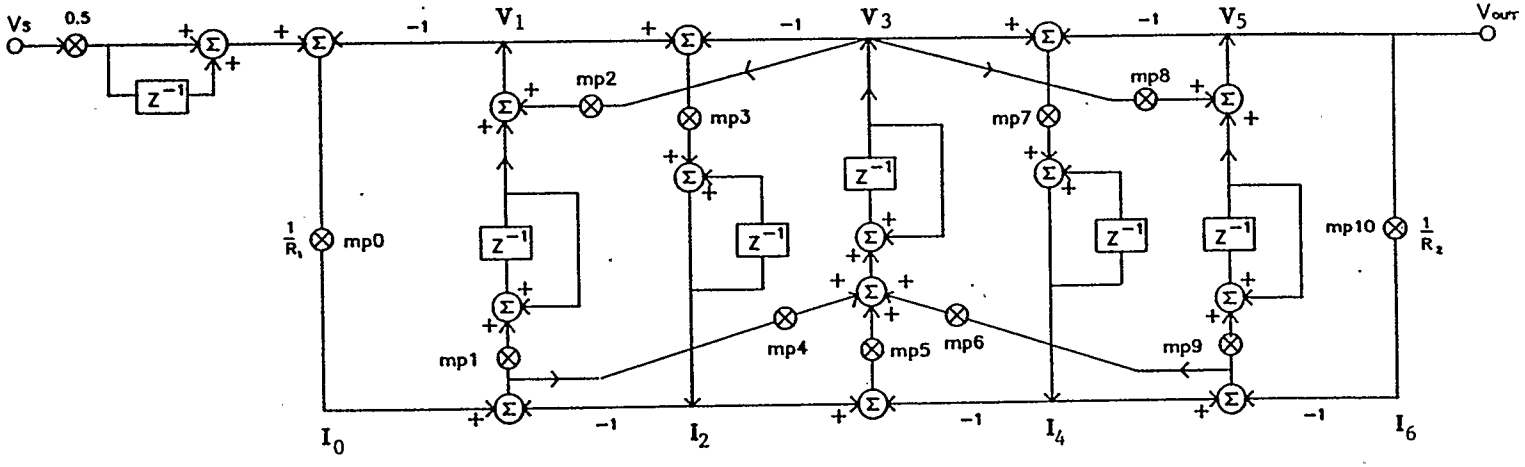


Figure 6.9 Fifth order digital, elliptic, LDI low-pass filter without delay free loops

$$mp2 = m12 = \frac{C_2'}{C_1' + C_2'} = 0.124318905 \tag{6.29}$$

$$mp3 = T \,.\, ml2 = \frac{T}{L_2} = 0.529302180 \tag{6.30}$$

$$mp4 = T \,.\, m32 = \frac{T \,.\, C_2'}{XY(C_1' + C_2')} = 0.0452935807 \tag{6.31}$$

$$mp5 = T \,.\, m31 = \frac{T}{XY} = 0.364333779 \tag{6.32}$$

$$mp6 = T \,.\, m33 = \frac{T \,.\, C_4'}{XY(C_4' + C_5')} = 0.0810094401 \tag{6.33}$$

$$mp7 = T \,.\, ml4 = \frac{T}{L_4} = 0.603549898 \tag{6.34}$$

$$mp8 = m52 = \frac{C_4'}{(C_4' + C_5')} = 0.222349510 \tag{6.35}$$

$$mp9 = T \,.\, m51 = \frac{T}{(C_4' + C_5')} = 0.537253320 \tag{6.36}$$

$$mp10 = 1.0 \tag{6.37}$$

The variables X and Y in equations (6.31)-(6.33) are obtained using equations (6.11)-(6.12). The transfer function of the structure in Fig. 6.9 is of the form

$$H(z) = \frac{a_5z^5+a_4z^4+a_3z^3+a_2z^2+a_1z+a_0}{b_6z^6+b_5z^5+b_4z^4+b_3z^3+b_2z^2+b_1z+b_0} \tag{6.38}$$

The unquantized transfer function coefficients of (6.38) are computed and are listed in Table 6.2.

$a_0 = 0.005035502890$	$b_0 = 0.0$
$a_1 = 0.004020829256$	$b_1 = -0.1976839015$
$a_2 = 0.008128506133$	$b_2 = 1.182857612$
$a_3 = 0.008128506133$	$b_3 = -3.00$
$a_4 = 0.004020829256$	$b_4 = 4.077185474$
$a_5 = 0.005035502890$	$b_5 = -2.993421644$
	$b_6 = 1.0$

Table 6.2 Unquantized transfer function coefficients.

The ideal magnitude frequency response of the LDI low-pass filter is given in Fig. 6.10. The passband attenuation characteristics obtained after quantizing the multiplier coefficients to 8, 11 and 12 bits are given in Fig. 6.11. For coefficient quantization of 12 bits the attenuation characteristic in the passband closely matches the ideal characteristic. For multiplier coefficient quantization of 11 bits or less the passband response is degraded although the stopband response meets the original specification. It is found that the magnitude frequency response in the passband of Chebychev LDI digital filter [15] with a multiplier quantization of 10 bits approximates that of an elliptic LDI digital filter using 12 bits. Thus an increase in the filter hardware of 5 adders, 4 multipliers and 1 delay unit and two additional coefficient bits provides an improved elliptic response characteristic.

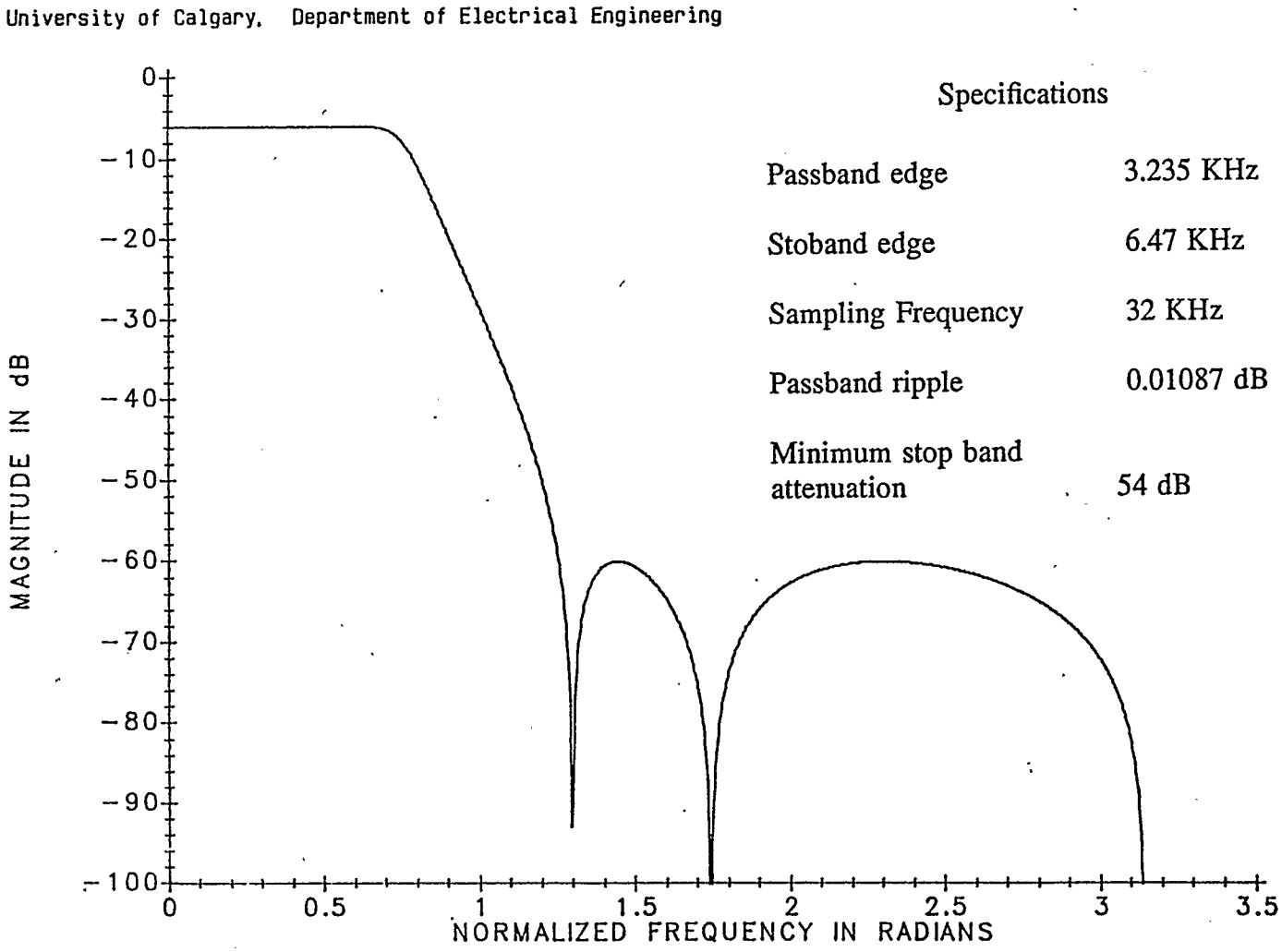


Figure 6.10 Magnitude frequency response of fifth order digital LDI low-pass ladder filter

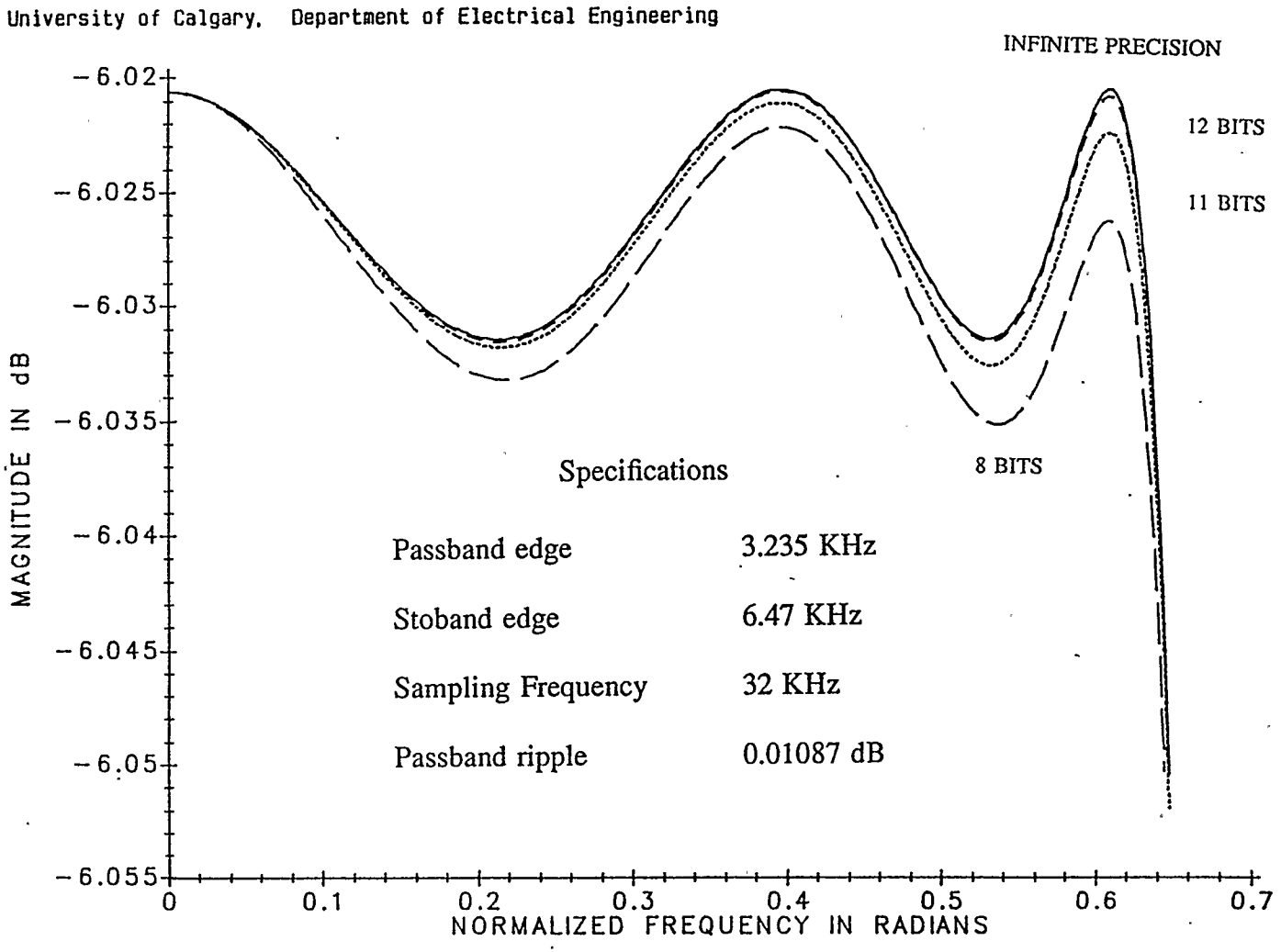


Figure 6.11 Passband response of fifth order digital LDI low-pass filter

6.2.1. Even Order Digital LDI Low-pass Filter Design

A precompensated elliptic analog low-pass filter of order 4 is shown in Fig. 6.12. Due to the precompensation procedure, a negative capacitor of value $\frac{-T^2}{4L_4}$ appears in parallel with the inductor L_4. To compensate the effect of this negative capacitor a positive capacitor of the same value is padded across it. Also, a negative capacitor of value $\frac{-T}{2R_2}$ appears in parallel with R_2, whose effect is canceled by a positive capacitor of the same value across it. This network is the same as the precompensated fifth order low-pass network in Fig. 6.1. Thus, due to precompensation an even order structure transforms to a structure of order one greater than the even order. Hence an even order structure is realized by using the next odd order structure. Thus the design of even order structures requires the same hardware as that of the next higher order structure. In addition, as the

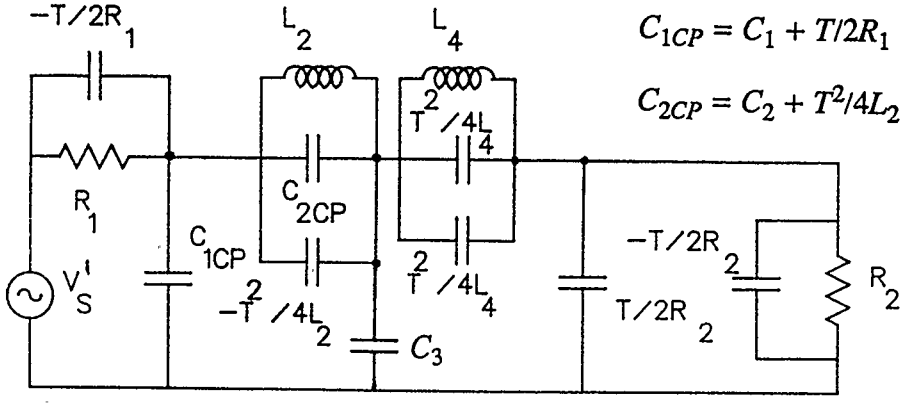


Figure 6.12 Precompensated fourth order elliptic low-pass ladder filter

compensating capacitor must cancel exactly the negative capacitor, the sensitivity of even order structure is expected to be higher.

6.3. Digital LDI Highpass ladder filter design

Consider the analog elliptic high-pass filter shown in Fig. 6.13. Note that the series branches of this network consist of only capacitive transmittances. It is mentioned in Chapter 5 that the network transformation developed to transform *Z–Z–Z* ladder block to *Z–Y–Z* ladder block cannot be applied to a network which consists of only capacitive transmittances in their series branches. Most of the analog ladder high-pass filter networks have only capacitive transmittances in their series branches. Hence, the precompensation method cannot be applied directly to this class of high-pass filters. However, a digital LDI ladder low-pass filter can be transformed to a digital LDI high-pass filter as explained below.

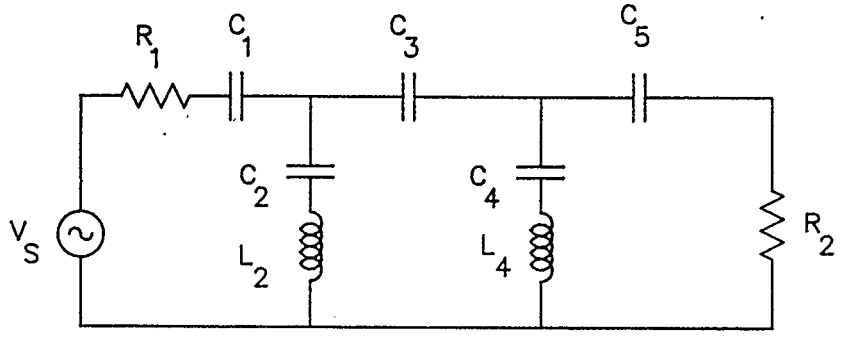


Figure 6.13 Fifth order elliptic high-pass ladder filter

The z-domain transfer function of a high-pass filter can be obtained by replacing z by $-z$ in the transfer function of a low-pass filter. Also this transformation maps the passband edge of the digital low-pass filter Ω_{LP} to the passband edge of the high-pass filter at $(\pi - \Omega_{LP}T)$ radians. Apply this transformation to the LDI transfer function, to arrive at

$$\left[\frac{T}{z^{1/2} - z^{-1/2}}\right] \longrightarrow \left[\frac{-j\,T}{z^{1/2} + z^{-1/2}}\right] .$$

This transformation can be realized by the digital network shown in Fig. 6.14. Observe that the network in Fig. 6.14 is the LDD differentiator block, which is the building block in digital LDI high-pass ladder filters. The suggested steps in designing a digital LDI high-pass ladder filter are as follows.

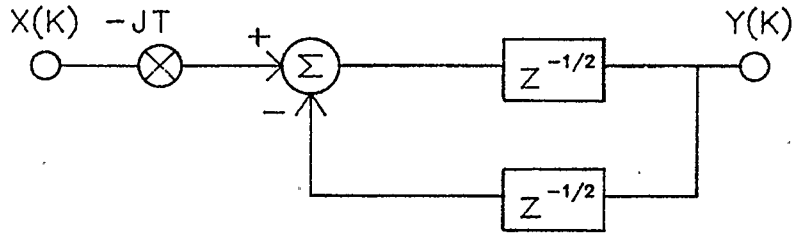


Figure 6.14 Building block for LDI high-pass filters

Step-1

Let Ω_{HP} represent the normalized passband frequency of the LDI digital high-pass filter. Design a LDI digital low-pass filter having its normalized passband frequency at $(\pi - \Omega_{LP}T)$ radians using the method outlined in Steps 1-2 of Section 6.2.

Step-2

Repeat Step-3 to Step-5 of Section 6.2 to obtain the *V/I* SFG of the low-pass filter consisting of analog integrators.

Step-3

Replace every analog intergrator in the *V/I* SFG in Fig. 6.7 low-pass filter with the high-pass filter building block shown in Fig. 6.14.

Step-4

Replace z by $-z$ in the z-domain transfer function of the precompensated voltage source to arrive at the transfer function of the precompensated voltage source for the high-pass filter

$$\left[V_s' = \frac{z+1}{2} V_s\right] \longrightarrow \left[\frac{1-z}{2} V_s\right] .$$

This transformed transfer function can be realized as shown in Fig. 6.15. Replace the precompensated voltage source in the digital LDI low-pass filter with the voltage source shown in Fig. 6.15. Scale the network with $z^{-1/2}$ delay elements. The

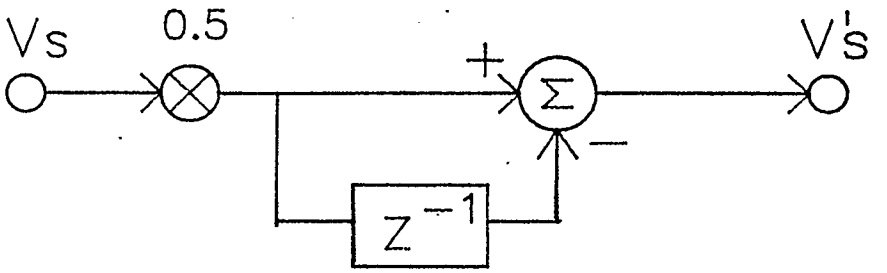


Figure 6.15 Precompensated voltage source for digital LDI high-pass filters

network thus obtained represents the digital elliptic LDI high-pass filter and is shown in Fig. 6.16. Notice that the structure in Fig. 6.16 has the same network topology as that of LDI low-pass filter in Fig. 6.9, except that some of the branches have negative inputs.

A fifth order digital LDI high-pass elliptic ladder filter having the following specifications is chosen as an example.

High-pass filter specifications.

Passband Edge	6006 Hz
Stopband Edge	3991 Hz
Maximum Passband ripple	0.01087 dB
Minimum Stopband attenuation	39.53 dB

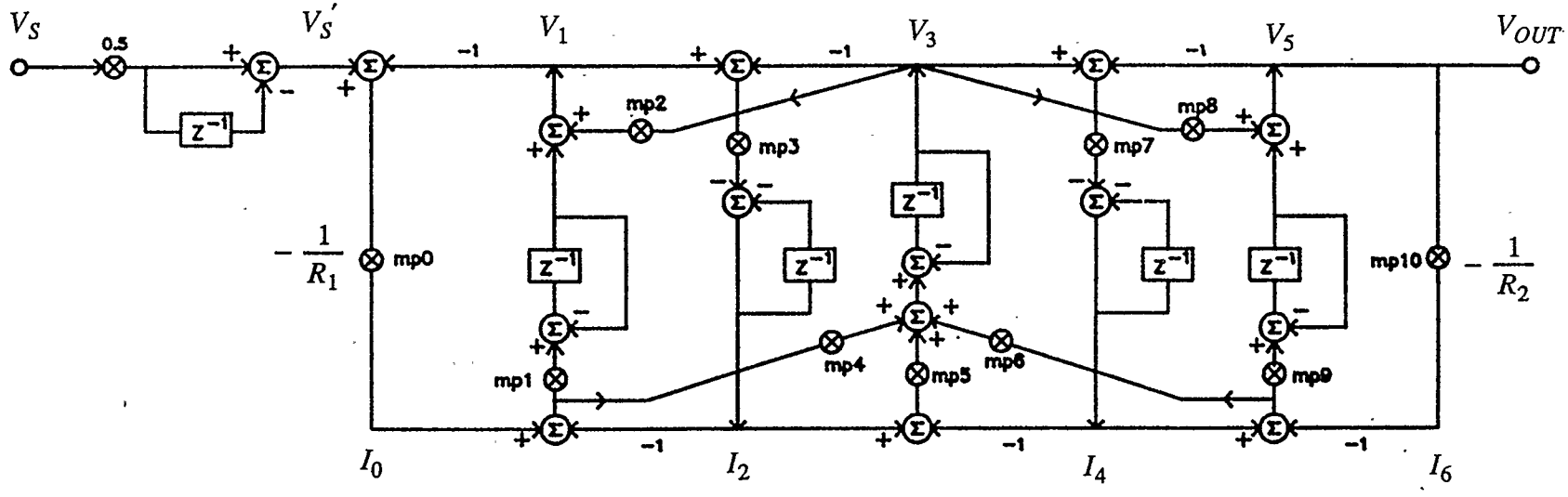


Figure 6.16 Fifth order digital elliptic LDI high-pass ladder filter

Sampling frequency 32 KHz

The normalized passband frequency of the high-pass filter is Ω_{HP}=1.17936 *rads*. The normalized passband frequency Ω_{LP} of the low-pass filter to be designed is $(\pi - \Omega_{HP}) = 1.96349$ *rads*.

A digital LDI low-pass ladder filter is first designed as described in section 6.1 to meet this specification. The analog integrators in the *V/I* SFG of the low-pass filter in Fig. 6.7 are replaced with the high-pass filter building blocks shown in Fig. 6.14, and the input voltage source is replaced with the transformed source in Fig. 6.15. The network thus obtained is scaled with $z^{-1/2}$ delay elements to result in the LDI high-pass filter in Fig. 6.16. The multiplier coefficients of this network are

mp0 = 1.0	mp1 = 0.708908021
mp2 = 0.48836118	mp3 = 2.57201672
mp4 = 0.4076823	mp5 = 0.834796667
mp6 = 0.508258939	mp7 = 3.49709058
mp8 = 0.608841538	mp9 = 0.598555565
mp10 = 1.0.	

This filter has been simulated using a digital filter simulation program on a VAX 11/780 and the magnitude-frequency response obtained is shown in Fig. 6.17. The coefficients of the multipliers are quantized to wordlengths of 13, 12 and 11 bits

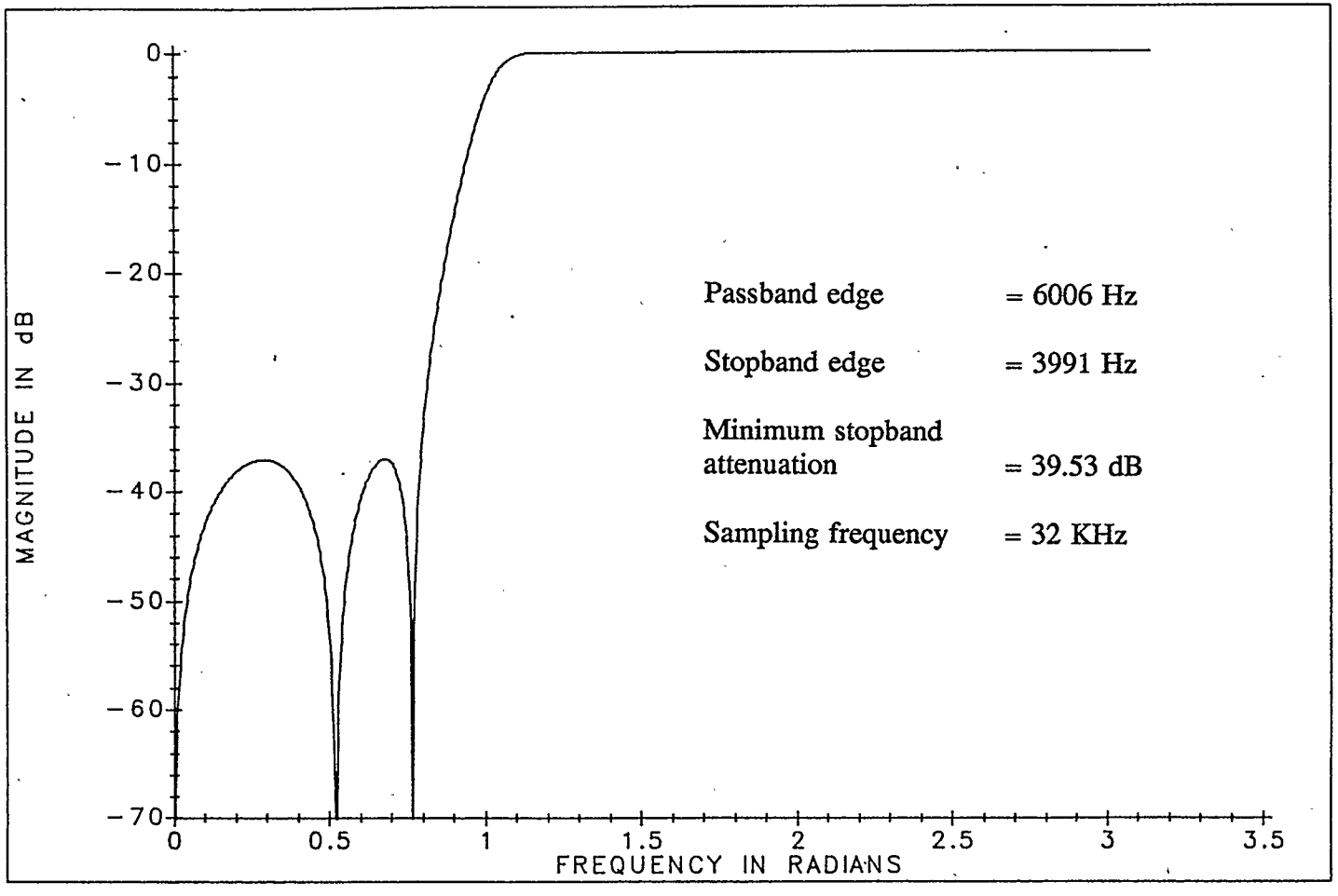


Figure 6.17 Magnitude frequency response of digital LDI high-pass filter

and the passband responses obtained are shown in Fig. 6.18. Note that the response obtained for 13 bit coefficient quantization closely matches the ideal response.

To summarize, the precompensation design method cannot be applied directly to analog elliptic high-pass ladder filters. A digital LDI low-pass ladder filter is first designed, and is then transformed to a digital LDI ladder high-pass ladder filter.

6.4. Digital Elliptic LDI Bandpass Filter Design

A sixth order digital elliptic LDI band-pass filter having the following specifications is chosen as an example.

Band-pass Filter Specifications

Lower passband cutoff frequency (f_{lp})	5000 Hz
Upper passband cutoff frequency (f_{up})	9000 Hz
Lower stopband cutoff frequency (f_{la})	4000 Hz
Upper stopband cutoff frequency (f_{ua})	10,000 Hz
Sampling frequency (f_s)	32 kHz
Maximum passband attenuation	0.1773 dB
Minimum Stopband attenuation	17.86 dB
Filter order	6

Step-1

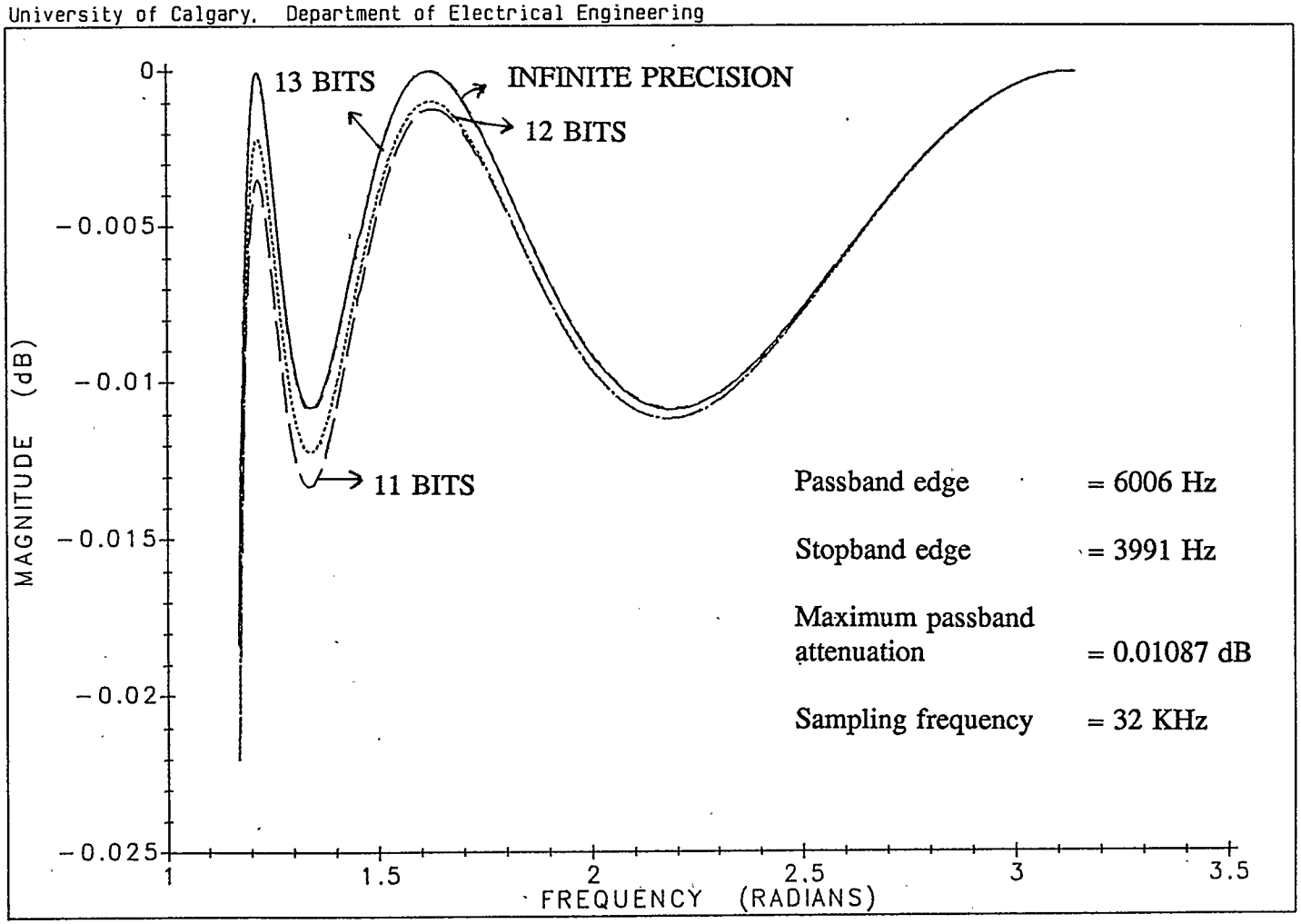


Figure 6.18 Passband response of digital LDI high-pass filter

The normalized digital band-pass filter specifications are

$$\Omega_{lp} \cdot T = 2\,\pi\, f_{lp} / f_s = 0.981748 \;\; rad.$$

$$\Omega_{up} \cdot T = 2\,\pi\, f_{up} / f_s = 1.767146 \;\; rad.$$

$$\Omega_{la} \cdot T = 2\,\pi\, f_{la} / f_s = 0.785398 \;\; rad.$$

$$\Omega_{ua} \cdot T = 2\,\pi\, f_{ua} / f_s = 1.963495 \;\; rad.$$

The frequency specifications of the equivalent analog band-pass filter obtained using the bilinear transformation are

$$\omega_{lp} = \frac{2}{T}\tan\left[\frac{\Omega_{lp}T}{2}\right] = 34192.47 \; rad/sec$$

$$\omega_{up} = \frac{2}{T}\tan\left[\frac{\Omega_{up}T}{2}\right] = 77970.35 \; rad/sec$$

$$\omega_{la} = \frac{2}{T}\tan\left[\frac{\Omega_{la}T}{2}\right] = 26496.8 \; rad/sec$$

$$\omega_{ua} = \frac{2}{T}\tan\left[\frac{\Omega_{ua}T}{2}\right] = 95710.42 \; rad/sec$$

Step-2

In this step an elliptic analog band-pass filter meeting the specifications mentioned above is designed. The method of designing an elliptic analog band-pass filter used in this example follows the steps outlined in [46]. Bandpass filters obtained by the transformation from a low-pass filter exhibit geometric symmetry. The geometric center frequency of such a filter is given by

$$\omega_o = \sqrt{\omega_{lp}\ \omega_{up}} = 51650.17\ rad/sec$$

To normalize the band-pass filter specifications, the geometric symmetry must be considered. For each stopband frequency specified, the corresponding geometric frequency is calculated and a steepness factor is computed based on the more severe requirement [46]. For $\omega_{la} = 26496.8\ rad/sec$ the corresponding geometric upper stopband cutoff frequency is calculated using equation $\omega_{ua} = \omega_o^2 / \omega_{la}$, and for $\omega_{ua} = 95710.42\ rad/sec$ the corresponding lower stopband cutoff geometric frequency is calculated using $\omega_{la} = \omega_o^2 / \omega_{ua}$. These results are tabulated below

ω_{la} *rad/sec*	ω_{ua} *rad/sec*	$\lvert\omega_{ua} - \omega_{la}\rvert$ *rad/sec*
26496.8	100681	74184
27873	95710	67837

The second pair of frequencies has the lesser separation and therefore represents the more severe requirements of the band-pass filter and hence is considered as the critical specification for the low-pass filter design. The geometrical symmetry requirements can be summarized as

Geometric center frequency (ω_o) = 51650 *rad/sec*

Passband width (BW_p) = 43777.88 *rad/sec*

Stopband width (BW_s) = 67837 *rad/sec*

$$The\ \ band\text{–}pass\ \ steepness\ \ factor = \frac{Stopband\ width}{Passband\ width} = 1.55 \cdot$$

A normalized low-pass filter which makes a transition from less than 0.1773 dB to more than 17.86 dB within a frequency ratio, of 1.55 is chosen from the design tables [46]. Since a low-pass filter of order n transforms to a band-pass filter of order $2n$, a 3rd order low-pass filter is chosen from the design tables [46] in order to realize a sixth order band-pass filter. The normalized element values of the third order low-pass filter are

$$C_1 = 0.9334\ F \qquad L_2 = 0.7973\ H$$

$$C_3 = 0.9334\ F \qquad C_2 = 0.4318\ H$$

The band-pass filter transfer function can be obtained from a low-pass transfer function by replacing the frequency variable with the new variable [46].

$$f_{bp} = f_o\left(\frac{f}{f_o} - \frac{f_o}{f}\right) \cdot \tag{6.39}$$

Note that when $f = f_o$, i.e, at the geometric center frequency, the response of the band-pass filter corresponds to the zero frequency response of the low-pass filter. The band-pass frequency variable in (6.39) can be used to transform the impedance of the low-pass filter elements.

Substitute (6.39) in the reactance expression of a capacitor, i.e. $\frac{1}{j\omega C}$, to obtain

$$\frac{1}{j\omega C + \dfrac{1}{j\omega \,/\, \omega_o^2 C}} \cdot \tag{6.40}$$

Observe that the expression (6.40) represents the impedance of a parallel resonant LC circuit. Similarly, by performing the above substitution in the expression for the reactance of an inductor, $j\omega L$, the impedance equation becomes

$$j\omega L + \frac{1}{j(\dfrac{\omega}{\omega_o^2 L})} \cdot \tag{6.41}$$

The expression (6.41) corresponds to a series resonant LC circuit. Thus an LC low-pass filter can be transformed into a band-pass filter having the equivalent bandwidth by resonating each capacitor with a parallel inductor and each inductor with a series capacitor. This transformation transforms every pole and zero of the low-pass filter into a pair of poles and zeros in the band-pass filter. The analog filter is first converted to a normalized band-pass filter having a center frequency of $\omega_o = 1 rad/sec$. The Q factor of the band-pass filter is defined by

$$Q_{BP} = \frac{f_o}{BW_p} = 1.179887 \cdot$$

where BW_p is the passband width. To obtain the normalized band-pass filter having a center frequency of $\omega_o = 1$ *rad/sec*, multiply all inductance and capacitance values of the normalized low-pass filter by Q_{BP}, and resonate each inductor with a series capacitor and each capacitor with a parallel inductor. The resonating elements have simply the reciprocal values given by

$$C_{1n} = (0.9334 * Q_{BP}) = 1.10129\ F \qquad L_{1n} = \frac{1}{C_1 n} = 0.90803\ H$$

$$L_{2n} = (0.7973 * Q_{BP}) = 0.940718\ H \qquad C_{2n} = \frac{1}{L_2 n} = 1.0630\ F$$

$$C_{3n} = (0.4318 * Q_{BP}) = 0.50947\ F \qquad L_{3n} = \frac{1}{C_{3n}} = 1.96282\ H$$

$$C_{4n} = (0.9334 * Q_{BP}) = 1.10129\ F \qquad L_{4n} = \frac{1}{C_{4n}} = 0.90803\ H$$

To complete the design, the filter has to be denormalized to a center frequency of ω_o. Multiply all inductors and capacitors by $\frac{1}{\omega_o}$ to obtain the actual values of the elements of the band-pass filter in Fig. 6.19, given by

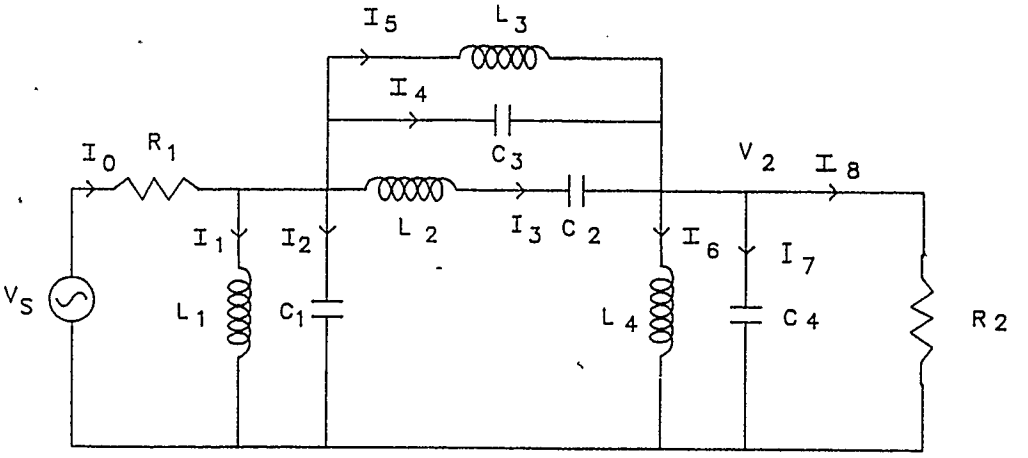


Figure 6.19 Sixth order analog elliptic band-pass ladder filter

$C_1 = 21.322\ \mu F$ $C_2 = 20.58\ \mu F$ $C_3 = 98.639\ \mu F$ $C_4 = 21.32\ \mu F$

$L_1 = 17.58\ \mu F$ $L_2 = 18.213\ \mu F$ $L_3 = 38\ \mu F$ $L_4 = 17.58.\ \mu F.$

Step-3

In this step the elements of the band-pass filter in Fig. 6.19 are modified to represent the prototype elements in the Table 4.1. In order to simplify the precompensation procedure, the network transformation shown in Fig. 6.20 is used to transform the band-pass filter into an equivalent form as shown in Fig. 6.21. The following equations are used to compute the normalized element values in the equivalent networks in Fig. 6.20. [Note: The expressions in (6.43-6.44) use normalized element values].

$$\beta = 1 + \frac{1}{2\,L_{2n}\,C_{3n}} + \sqrt{\frac{1}{4\,L_{2n}^2\,C_{3n}^2} + \frac{1}{L_{2n}\,C_{3n}}} \qquad (6.43)$$

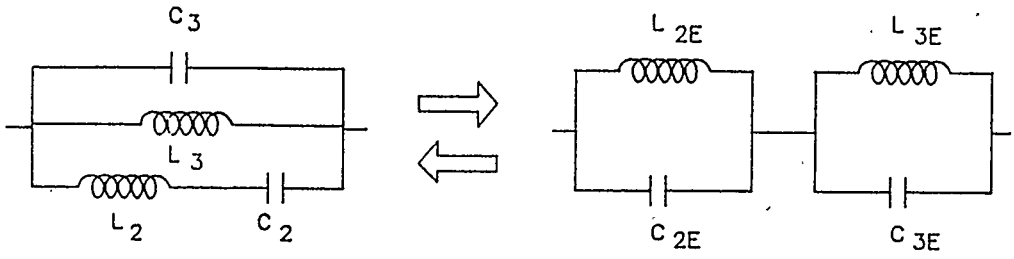


Figure 6.20 Network equivalents-II

$$C_{L1P} = -T^2/4_{L1P} \qquad C'_{2E} = +T^2/4_{L2E} \qquad C_{1P} = C_1 + T/2_{R1} + T^2/4_{L1}$$
$$C_{L4P} = -T^2/4L_{4P} \qquad C'_{3E} = C_{3E} + T^2/4L_{3E} \qquad C_{4P} = C_4 + T/2_{R2} + T^2/4L_4$$

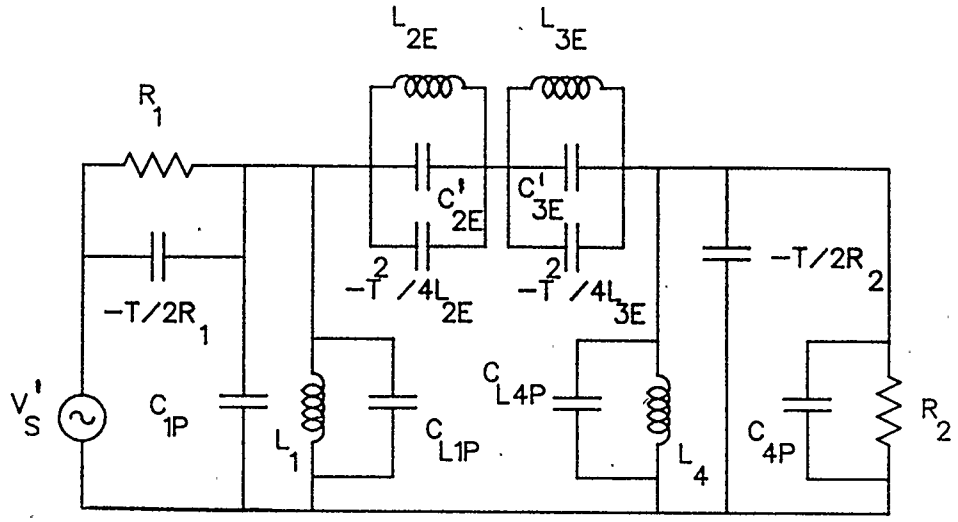


Figure 6.21 Precompensated sixth order elliptic band-pass filter

$$L_{2E} = \frac{1}{C_{3n}(\beta + 1)} = 0.4068\ H \tag{6.44}$$

$$L_{3E} = \beta\, L_{2E} = 0.1556\ H \tag{6.45}$$

$$C_{2E} = \frac{1}{L_{3E}} = 0.64266\ F \tag{6.46}$$

$$C_{3E} = \frac{1}{L_{2E}} = 2.4582301\ F \tag{6.47}$$

Denormalizing the element values to a center frequency of ω_o, the actual component values of the transformed series branch are

$$L_{2E} = 7.8759\ \mu H \qquad C_{2E} = 12.4427\ \mu H$$

$$L_{3E} = 3.01259\ \mu H \qquad C_{3E} = 47.59\ \mu F.$$

When the elements in the band-pass filter are modified to represent the prototype elements in the Table 4.1, negative capacitors of value $-T^2 / 4\ L_{2E}$ and $-T^2 / 4\ L_{3E}$ appear in parallel with L_{2E} and L_{3E}, respectively. To compensate for the effects of these capacitors, positive capacitors of the same value are added to C_{2E} and C_{3E}, respectively. The input source is modified to V_s' and the capacitor C_1 is modified to $C_1 + T / 2R_1$ in order to compensate for the effect of the negative capacitor $-T / 2R_1$ across R_1 as explained in section 6.1.

Step-4

As discussed in Step-4 of the general design procedure in Section 4.4 of Chapter 4, substitute every prototype element in the network in Fig. 6.21 with its equivalent elements from Table 4.1 to arrive at the network shown in Fig. 6.22. Note that the LDI transformed transfer function of the precompensated network in Fig. 6.22 and the bilinear transformed transfer function of the network in Fig. 6.19 are the same.

The series branch of the network in Fig. 6.22 is transformed back into its equivalent branch, as shown in Fig. 6.20, using the following equations.

$$L'_2 = \frac{L_{2E} \cdot L_{3E}\,(L_{2E} + L_{3E})\,(C'_{2E} + C'_{3E})^2}{(L_{2E}\,C'_{2E} - L_{3E}\,C'_{3E})^2} \tag{6.48}$$

$$L'_3 = L_{2E} + L_{3E} \tag{6.49}$$

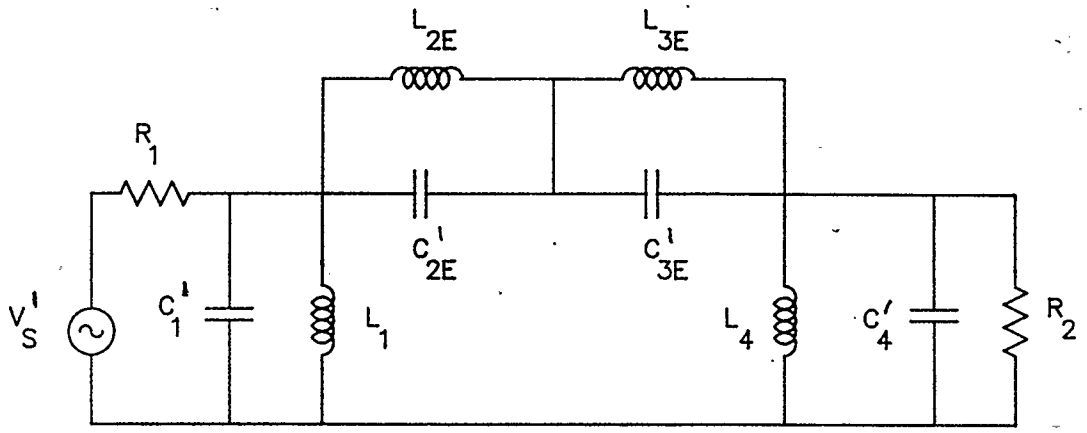


Figure 6.22 LDI equivalent of the precomensated band-pass filter

$$C'_2 = \frac{(L_{2E}\, C'_{2E} - L_{3E}\, C'_{3E})^2}{(C'_{2E} + C'_{3E})\,(L_{2E} + L_{3E})^2} \tag{6.50}$$

$$C'_3 = \frac{C'_{2E} \cdot C'_{3E}}{C'_{2E} + C'_{3E}} \tag{6.51}$$

The LDI equivalent of the precompensated network is shown in Fig. 6.23, and its precompensated element values are

$C'_1 = 50.8348\ \mu F$ $\quad L_1 = 17.580\ \mu H$

$C'_2 = 12.46346\ \mu F$ $\quad L'_2 = 49.664\ \mu H$

$C'_3 = 24.406\ \mu F$ $\quad L'_3 = 38.00\ \mu H$

$C'_4 = 50.834\ \mu F$ $\quad L_4 = 17.58\ \mu H.$

Step-5

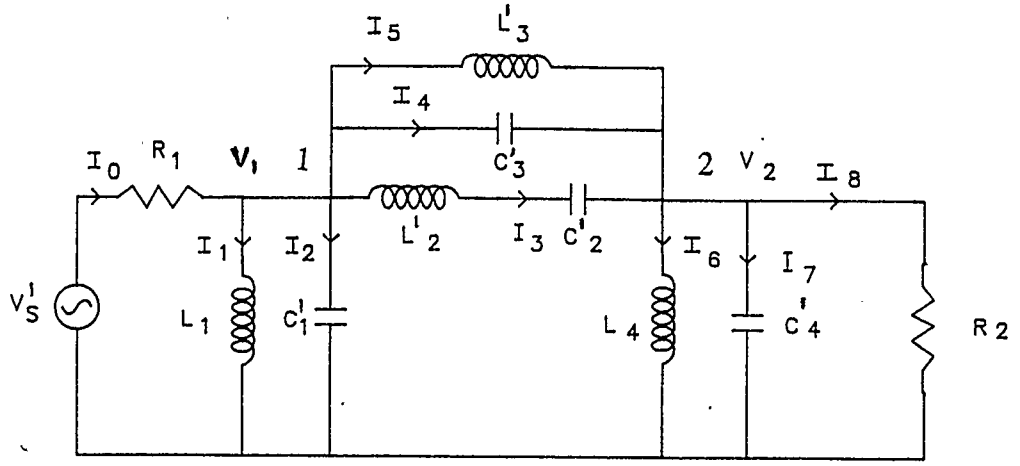


Figure 6.23 Equivalent form of the band-pass filter in Fig. 6.22

In this step it is required to construct a *V/I* SFG of the analog network in Fig. 6.23 consisting of only analog integrators. Notice that the series and the parallel branches of the network in Fig. 6.23 are z-type transmittances. The capacitor C_3' in the series branch can be transformed into a current controlled voltage source as discussed in Chapter 5, thus converting the z-type series branch to a y-type series branch. Also, the same network transformation can be used to transform the inductor L_3' into current controlled voltage sources in order to reduce the number of integrators in the *V/I* SFG. The suggested network transformation is performed as follows. Using the current equation for node-1

$$I_o = I_1 + I_2 + I_3 + I_4 + I_5$$

$$= I_1 + V_1\, sC_1' + I_3 + (V_1 - V_2)\, sC_3' + I_5 \quad ,$$

solve for V_1 to arrive at

$$V_1 = \frac{1}{s(C_1' + C_3')}(I_o - I_1 - I_3 - I_5) + \frac{C_3'}{C_1' + C_3'} V_2 \quad . \tag{6.52}$$

Similarly the node equation of node-2 is

$$I_3 + I_4 + I_5 = I_6 + I_7 + I_8 \quad ,$$

and thus

$$I_3 + (V_1 - V_2)\, sC_3' + I_5 = I_6 + V_2\, sC_4' + I_8 \quad .$$

Solve for V_2 to obtain

$$V_2 = \frac{1}{s(C_4' + C_3')}(I_3 + I_5 - I_6 - I_8) + \frac{C_3'}{C_3' + C_4'} V_1 \quad . \tag{6.53}$$

It is clear from (6.52) and (6.53) that voltage V_1 at node-1 contributes to the voltage V_2 at node-2 and vice versa. Thus an attempt to construct a *V/I* SFG using these equations will result in a delay free loop between node-1 and node-2. To eliminate this delay free loop substitute (6.52) in (6.53) to arrive at

$$V_2 = \frac{1}{s(C_3' + C_4')}(I_3 + I_5 - I_6 - I_8) + \frac{C_3'}{s(C_1' + C_3')(C_3' + C_4')} I_0 - I_1 - I_3 - I_{5)} + \frac{C_3'^2}{(C_1' + C_3')(C_3' + C_4')} V_2 \quad . \tag{6.54}$$

and substitute (6.53) in (6.52) to arrive at

$$V_1 = \frac{1}{s(C_1' + C_3')}(I_0 - I_1 - I_3 - I_5)$$

$$+ \frac{C_3'}{s(C_1' + C_3')(C_3' + C_4')}(I_3 + I_5 - I_6 - I_8) \qquad (6.55)$$

$$+ \frac{C_3'}{C_1' + C_3')(C_3' + C_4')} V_1 \quad .$$

Let

$$N = \frac{C_3'}{(C_1' + C_3')(C_3' + C_4')} \quad \text{and} \quad M = (1 - C'_3 \cdot N)$$

Simplify (6.54) and (6.55) to obtain

$$V_1 = \frac{1}{sM(C_1' + C_3')}(I_o - I_1 - I_3 - I_5) + \frac{N}{sM}(I_3 + I_5 - I_6 - I_8) \qquad (6.56)$$

$$V_2 = \frac{1}{sM(C_3' + C_4')}(I_3 + I_5 - I_6 - I_8) + \frac{N}{sM}(I_0 - I_1 - I_3 - I_5) \qquad (6.57)$$

The inductor L_3' in the series branch can be transformed as follows. The node equation for node-1 can be written as

$$I_0 = \frac{V_1}{sL_1} + I_2 + I_3 + I_4 + \frac{V_1 - V_2}{sL'_3} \quad .$$

The above equation simplifies to

$$(I_0 - I_2 - I_3 - I_4) = \frac{L_1 + L'_3}{sL_1L'_3} V_1 - \frac{V_2}{sL'_3} \quad . \qquad (6.58)$$

Similarly, the node equation for node-2 can be written as

$$I_3 + I_4 + \frac{V_1 - V_2}{sL'_3} = \frac{V_2}{sL_4} + I_7 + I_8 \cdot$$

The above equation simplifies to

$$(I_3 + I_4 - I_7 - I_8) = \frac{L'_3 + L_4}{sL'_3 L_4} V_2 - \frac{1}{sL'_3} V_1 \cdot \qquad (6.59)$$

Using equations (6.56)-(6.59) the network shown in Fig. 6.24 can be constructed, to represent the functional equivalent model of the filter in Fig. 6.23. In this model the subscripts CV and VC represent current controlled voltage sources and voltage controlled current sources, respectively. The expressions for these voltage and current sources are

$$CV1 = \frac{1}{sM(C_1' + C_3')}(I_0 - I_1 - I_3 - I_5) \qquad CV2 = \frac{N}{sM}(I_3 + I_5 - I_6 - I_8),$$

$$VC1 = \frac{L_1 + L'_3}{sL_1 L'_3} V_1 \qquad VC2 = -\frac{V_1}{sL'_3},$$

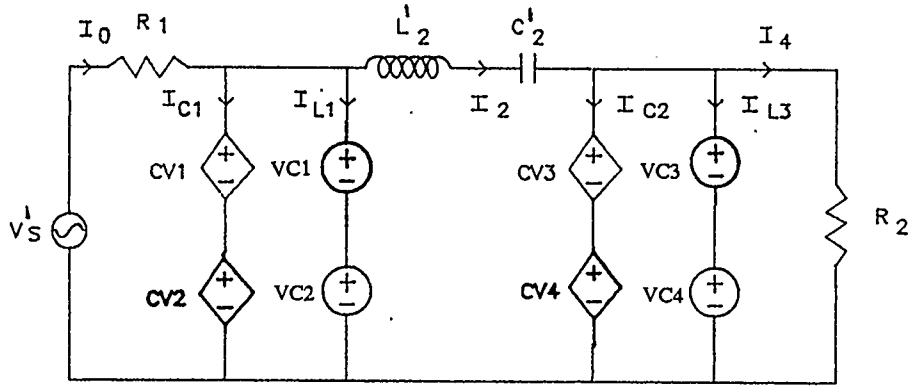


Figure 6.24 Functional equivalent of the band-pass filter in Fig. 6.23

$$CV3 = \frac{1}{sM(C_3' + C_4')}\,(I_3 + I_5 - I_6 - I_8) \qquad CV4 = \frac{N}{sM}\,(I_0 - I_1 - I_3 - I_5),$$

$$VC3 = \frac{L'_3 + L_4}{sL'_3L_4} \qquad \text{and} \qquad VC4 = -\frac{1}{sL'_3}\,V_1.$$

The *V/I* SFG constructed using the equations (6.56) - (6.59) is shown in Fig. 6.25. Observe that this *V/I* SFG contains only analog integrators as desired. The expressions for the multiplier coefficients in the *V/I* SFG in Fig. 6.25 are

$$SMP1 = \frac{1}{M(C_1' + C_3')} \qquad SMP2 = \frac{L_1 + L_3'}{L_1L_3'}$$

$$SMP3 = -\frac{1}{L_3'} \qquad SMP4 = \frac{1}{L_2'}$$

$$SMP5 = -\frac{1}{C_2'} \qquad SMP6 = -\frac{1}{L_3}$$

$$SMP7 = \frac{L_3' + L_4}{L_3'L_4} \qquad SMP8 = \frac{1}{M(C_3' + C_4')}.$$

$$SMP9 = \frac{N}{M} \qquad SMP10 = \frac{N}{M}$$

Step-6

A discrete structure can be obtained by replacing every analog integrator in the *V/I* SFG with LDI integrator blocks. Note that the unity terminating resistors must be approximated with $z^{1/2}$ delay elements as was done in the low-pass and high-pass filter designs.

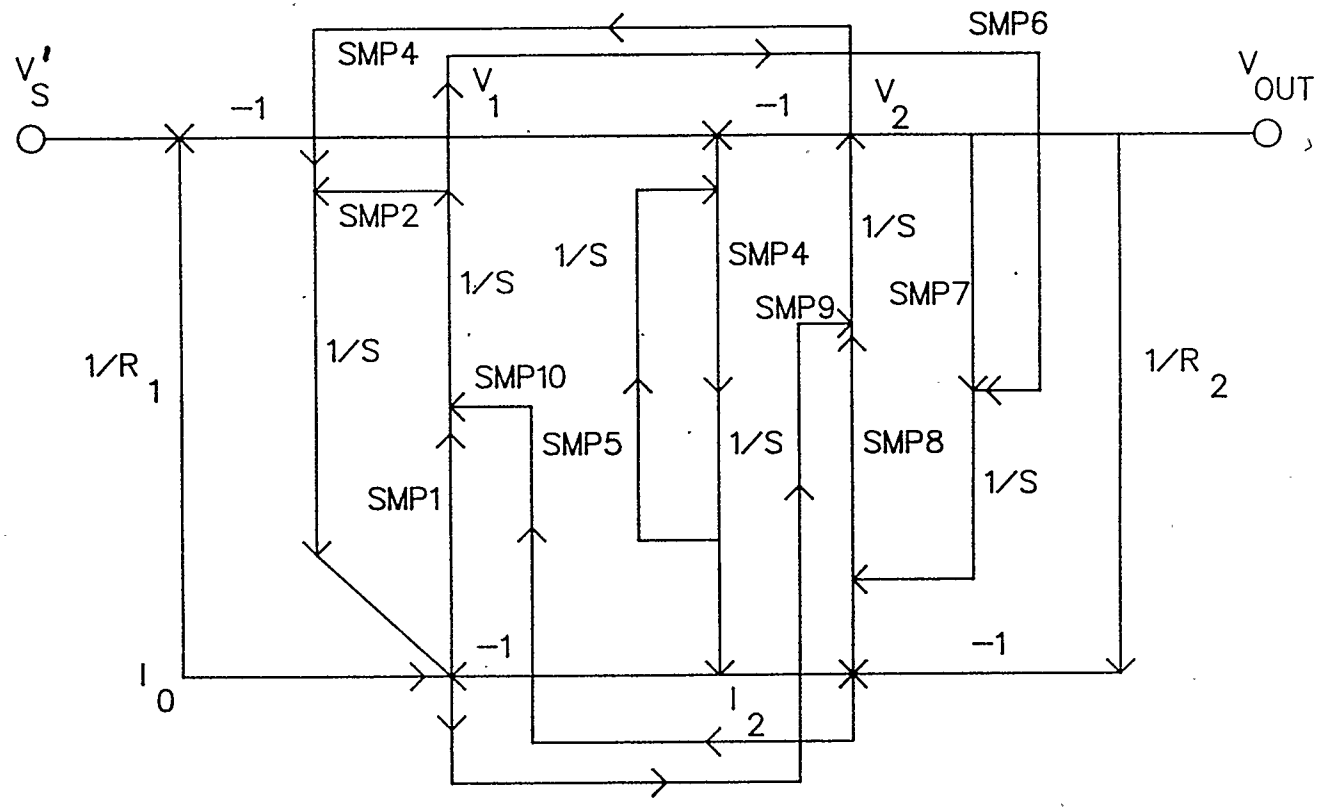


Figure 6.25 *V/I* SFG of the band-pass filter in Fig. 6.24

Step-7

This discrete network can strictly be implemented with half unit delays. Since it is not economical to do so, the network is scaled with $z^{-½}$ delay elements to obtain only unit delays. The final realizable digital LDI band-pass filter is shown in Fig. 6.26. The $z^{-½}$ delay element which appears at the input due to the scaling of the network has been neglected since it does not introduce any errors in the magnitude response of the filter. The multiplier coefficients in the digital LDI band-pass filter can be evaluated using the expressions

$$mp0 = 1.0$$

$$mp1 = \frac{T}{M(C_1' + C_3')} = 0.46417233$$

$$mp2 = \frac{TN}{M} = 0.150564045$$

$$mp3 = \frac{L_1 + L_3'}{L_1 L_3'} \cdot T = 2.59991193$$

$$mp4 = \frac{T}{L_3'} = 0.822327852$$

$$mp5 = \frac{T}{C_2'} = 2.50732756$$

$$mp6 = \frac{T}{L_2'} = 0.629224479$$

$$mp7 = \frac{TN}{M} = 0.150564045$$

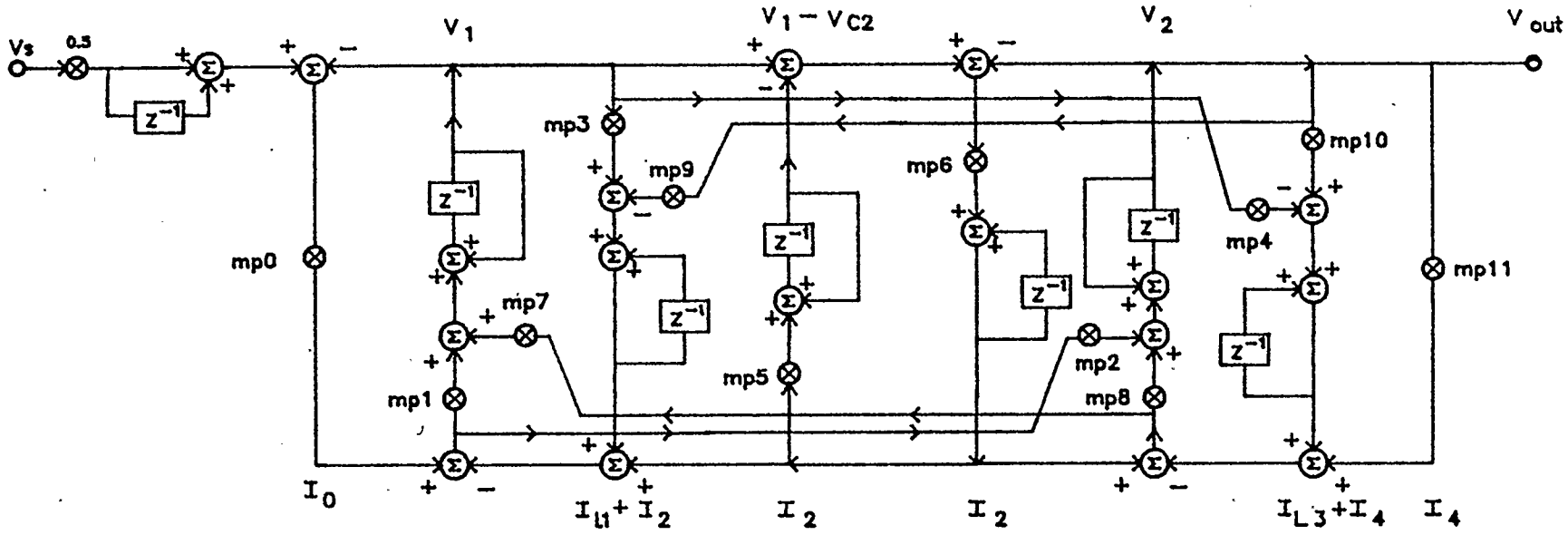


Figure 6.26 Sixth order digital LDI band-pass filter with unit delay elements

$$mp8 = \frac{T}{M(C_3' + C_4')} = 0.464172333$$

$$mp9 = \frac{T}{L_3'} = 0.822327852$$

$$mp10 = T\frac{L_3' + L_4}{L_3'L_4} = 2.59991193$$

$$mp11 = 1.0$$

This digital LDI band-pass filter has been simulated using a digital filter simulation program on a VAX 11/780. The magnitude-frequency response of this filter is shown in Fig. 6.27. Observe the response obtained in Fig. 6.27 meets the stopband specifications. The passband attenuation characteristics obtained after quantizing the multiplier coefficients to 8 and 12 bits are shown in Fig. 6.28. Note that the response due to 12 bits of quantization closely matches the ideal response characteristics. For multiplier coefficient quantization of 11 bits or less the passband response is degraded although the stopband meets the specification.

6.5. Digital Elliptic LDI Bandstop Filter Design

A digital elliptic LDI band-stop filter having the following specifications is chosen as a design example

Band-stop Filter Specifications

Lower passband cutoff frequency (f_{lp})	3000 Hz
Upper passband cutoff frequency (f_{up})	6000 Hz
Lower stopband cutoff frequency (f_{la})	3500 Hz

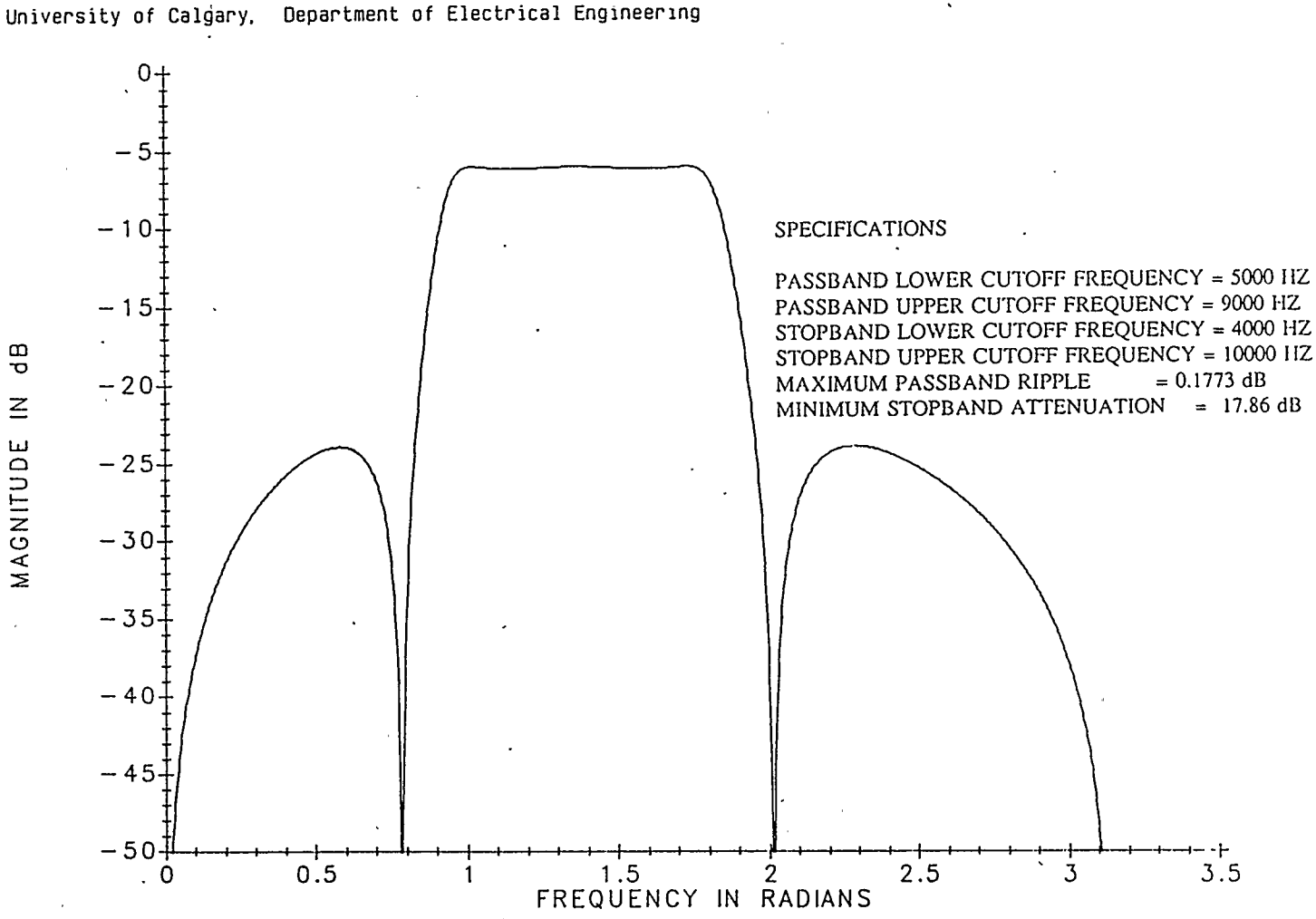


Figure 6.27 Magnitude-frequency response of the band-pass filter

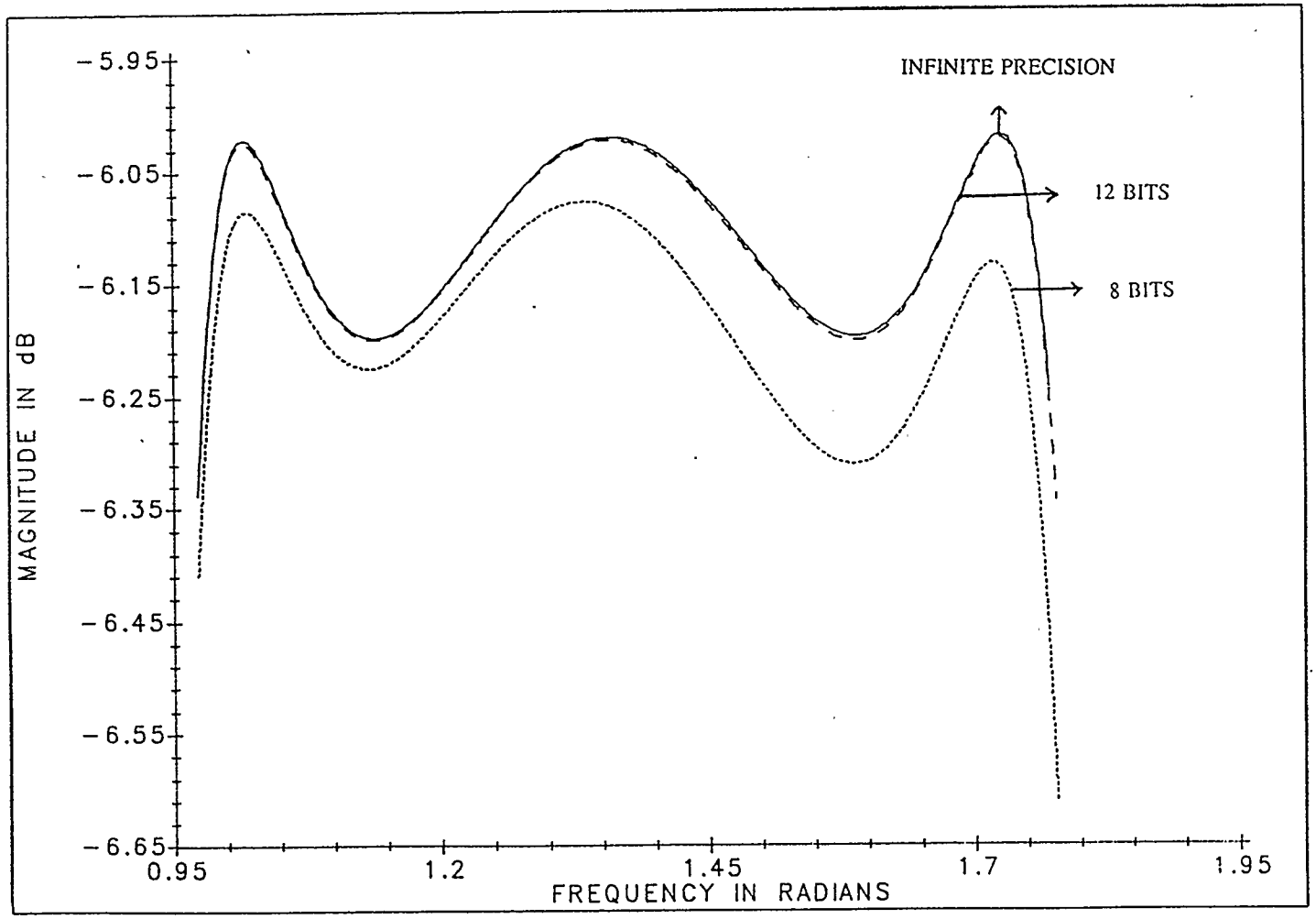


Figure 6.28 Passband response of the digital LDI band-pass filter

Upper stopband cutoff frequency (f_{ua})	5500 Hz
Sampling frequency (f_s)	32 KHz
Maximum passband attenuation	0.1773 dB
Minimum Stopband attenuation	14.60 dB
Filter order	6.

Step-1

The normalized digital band-pass filter specifications are

$\Omega_{lp}T = 2\,\pi\, f_{lp} / f_s = 0.589049\ rad.$ $\Omega_{up}T = 2\,\pi\, f_{up} / f_s = 1.17810\ Rad.$

$\Omega_{la}T = 2\,\pi\, f_{la} / f_s = 0.687223\ rad.$ $\Omega_{ua}T = 2\,\pi f_{ua} / f_s = 1.07992\ Rad.$

The frequency specifications of the equivalent analog band-stop filter obtained by using the bilinear transformation are

$$\omega_{lp} = \frac{2}{T}\tan\left[\frac{\Omega_{lp}T}{2}\right] = 19405.65\ rad/sec$$

$$\omega_{up} = \frac{2}{T}\tan\left[\frac{\Omega_{up}T}{2}\right] = 42741.62\ rad/sec$$

$$\omega_{la} = \frac{2}{T}\tan\left[\frac{\Omega_{la}T}{2}\right] = 22889.56\ rad/sec$$

$$\omega_{ua} = \frac{2}{T}\tan\left[\frac{\Omega_{ua}T}{2}\right] = 38341.11713\ rad/sec$$

Step-2

The method used to design an elliptic analog band-stop filter in this example is outlined in [46]. Band-stop filters obtained by the transformation from a low-pass filter also exhibit a geometric symmetry. The geometric center frequency of such a filter is given by

$$\omega_o = \sqrt{\omega_{lp}\ \omega_{up}} = 28813.5\ rad/sec\ .$$

To normalize the band-stop filter specifications, the geometrical symmetry must be considered. For each stopband frequency specified, the corresponding geometric frequency is calculated and a steepness factor is computed based on the more severe requirement. For ω_{la} the corresponding geometric frequency is given by $\omega_{ua} = \frac{\omega_o^2}{\omega_{la}}$ and for ω_{ua} the corresponding geometric frequency is given by $\omega_{la} = \frac{\omega_o^2}{\omega_{ua}}$. These results are tabulated as

ω_{la} *rad/sec*	ω_{ua} *rad/sec*	$\lvert\omega_{ua} - \omega_{la}\rvert$ *rad/sec*
22889.6	36270.6	13381
21653	38341	16681

Notice that the second pair of frequencies has the larger separation and therefore represents the more severe requirement and will be used in the low-pass filter specifications. The geometrical symmetry requirements of the band-stop filter can

be summarized as

$$\text{Geometric center frequency } (\omega_o) = 28813.5 \text{ } rad/sec$$

$$\text{Passband width } (BW_p) = 23335.97 \text{ } rad/sec$$

$$\text{Stopband width } (BW_s) = 16688 \text{ } rad/sec$$

$$\textit{The bandreject steepness factor} = \frac{\textit{Passband width}}{\textit{Stopband width}} = 1.39670$$

A low-pass filter whose passband edge is normalized to 1 *rad/sec* and which makes the transition from less than 0.1773 dB to more than 14.60 dB within a frequency ratio of 1.39670 is chosen from the design tables [46], and the element values of the normalized filter are

$$C_1 = 0.8689\ F \qquad L_2 = 0.7082\ F$$

$$C_3 = 0.8689\ F \qquad C_2 = 0.5942\ F \quad .$$

Note that unity terminating resistors are chosen in this design. Since a normalized low-pass filter of order n transforms to a band-stop filter of order $2n$, a third order low-pass filter is chosen from the design table [46].

Band-stop filters are designed initially by transforming the normalized low-pass into a high-pass network having a cutoff frequency equal to the required bandwidth and at the desired impedance level. The normalized low-pass filter is transformed into a normalized high-pass filter by replacing all inductors by capacitors and all

capacitors by inductors with reciprocal values. The resulting filter is shown in Fig. 6.29 and the element values are

$$L_{1H} = \frac{1}{C_1} = 1.15088\ H \qquad L_{2H} = \frac{1}{C_{2H}} = 1.6829\ H$$

$$L_{3H} = \frac{1}{C_3} = 1.15088\ H \qquad C_{2H} = \frac{1}{L_2} = 1.41203\ F \quad .$$

Observe that when $f = f_0$, i.e at the geometric center frequecy, the response of the band-stop filter corresponds to the zero frequency response of the high-pass filter. Thus an LC high-pass filter can be transformed into a band-stop filter having an equivalent bandwidth by resonating each capacitor with a parallel inductor and each inductor with a series capacitor [46]. To obtain the normalized band-stop filter having a center frequency of $\omega_0 = 1 rad/sec$, multiply all inductors and capacitors by the Q-factor of the band-stop filter Q_{bs}, which is given by

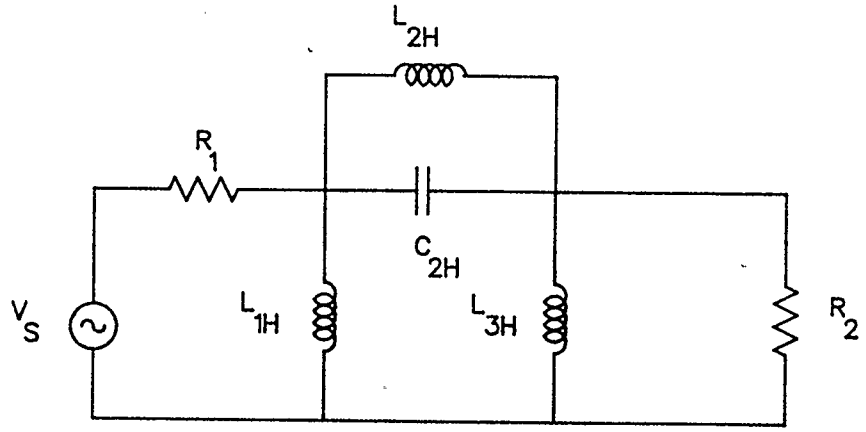


Figure 6.29 Third order high-pass ladder filter

$$Q_{bs} = \frac{f_0}{passband\ \ width} = 1.23402$$

Since the center frequency is 1 *rad/sec*, the resonant elements are simply the reciprocal of the elements themselves. To complete the design the filter has to be denormalized to a center frequency ω_0, which is performed by dividing all reactive element values by ω_0. The element values of the band-stop filter, shown in Fig. 6.30 are

$$L_1 = L_4 = 49.289\ \mu H \qquad C_1 = C_4 = 24.4372\ \mu F$$

$$C_3 = 60.474\ \mu F \qquad L_3 = 30.33\ \mu H$$

$$L_2 = 72.07497\ \mu H \qquad C_2 = 25.449\ \mu F \quad .$$

Step-3

As suggested in the general design procedure in Section 4.4 of Chapter 4, the elements of the band-stop filter in Fig. 6.30 are to be modified to represent the prototype elements in Table 4.1. In order to simplify the precompensation design procedure, the series branch of the band-stop filter in Fig. 6.30 is transformed to an equivalent form shown in Fig. 6.20. The normalized transformed element values can be calculated using equations (6.43)-(6.47) in which L_{2H} and C_{3H} are used instead of L_{2D} and C_{3D}. The normalized transformed element values of the equivalent series branch are

$$L_{2E} = 0.214004\ H \qquad C_{2E} = 2.77861\ F$$

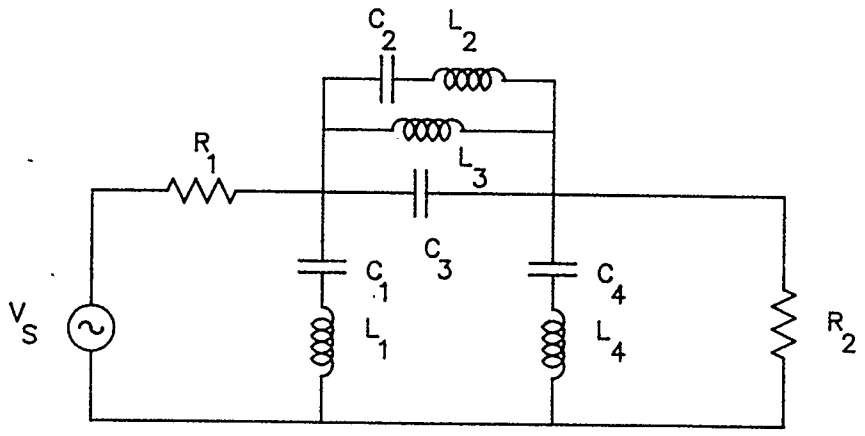


Figure 6.30 Sixth order elliptic band-stop ladder filter

$$L_{3E} = 0.359892\ H \qquad C_{3E} = 4.67281\ F$$

The denormalized element values of the transformed branch, obtained by dividing the elements by ω_0, are

$$L_{2E} = 7.42722\ \mu F \qquad C_{2E} = 96.4345\ \mu F$$

$$L_{3E} = 12.4904\ \mu F \qquad C_{3E} = 162.174\ \mu F.$$

When the elements in the band-stop filter are modified to represent prototype elements in Table 4.1, negative capacitors of value $-T^2/4\ L_{2E}$ and $-T^2/4\ L_{3E}$ appear in parallel with L_{2E} and L_{3E}, respectively, as shown in Fig. 6.31; positive capacitors of the same value can be added to C_{2E} and C_{3E} in order to compensate for the effects of the negative capacitors as shown in Fig. 6.31. Also, due to the precompensation of the negative capacitor across the source terminating resistance the

$$C_{L1P} = -T^2/4L_1 \qquad C_{L1CP} = +T^2/4L_1$$
$$C_{L4P} = -T^2/4L_4 \qquad C_{L4CP} = +T^2/4L_4$$
$$C_{2EP} = C_{2E} + T^2/4L_{2E} \qquad C_{L2EP} = -T^2/4L_{2E}$$
$$C_{3EP} = C_{3E} + T^2/4L_{3E} \qquad C_{L3EP} = -T^2/4L_{3E}$$

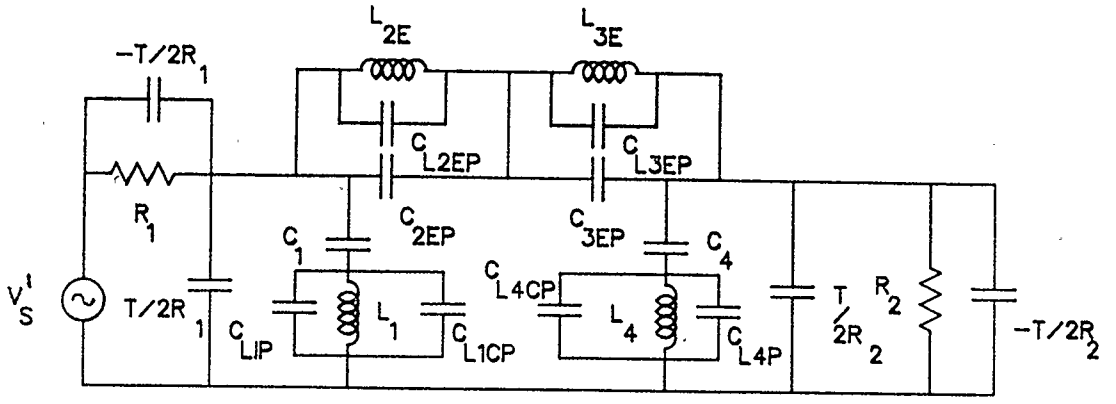


Figure 6.31 Precompensated band-stop ladder filter

input voltage source V_s transforms to V_s' given in (6.6) and the capacitor C_1 transforms to $C_1 + T/2\ R_1$, as discussed in section 6.1. Notice that the network in Fig. 6.31 consists of only prototype elements.

Step-4

In this step every prototype element in the network in Fig. 6.31 is substituted for by its equivalent element from Table 4.1, to arrive at the LDI equivalent of the precompensated network as shown in Fig. 6.32. The series branch of the network in Fig. 6.32 is transformed back into its equivalent branch as shown in Fig. 6.20 using the equations (6.48)-(6.51). Also the parallel branches are transformed into

$$C_{2EP} = T^2/4L_{2E} \qquad C_{3EP} = T^2/4L_{3E}$$

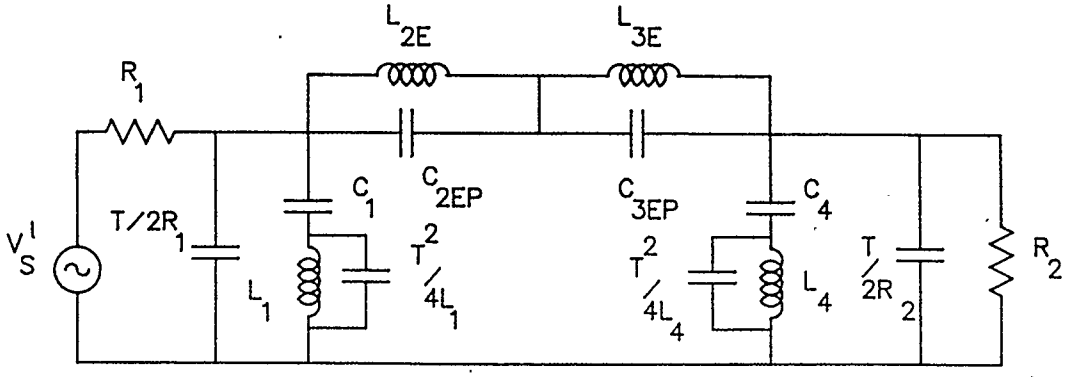


Figure 6.32 LDI equivalent network of the band-stop filter in Fig. 6.31

their equivalent forms as shown in Fig. 5.10, to arrive at the final LDI equivalent of the precompensated network as shown in Fig. 6.33. The computed element values in this network are

$$C_1 = 19.74346\ \mu F$$

$$L_2 = 71.29503\ \mu H \qquad C_2 = 20.31878\ \mu F$$

$$L_3 = 19.9176\ \mu H \qquad C_3 = 75.5483\ \mu F$$

$$L_4 = L_2 \qquad C_4 = C_2$$

$$L_6 = 104.256\ \mu H \qquad C_6 = 13.8951\ \mu F$$

$$C_5 = 19.74346\ \mu F.$$

Step-5

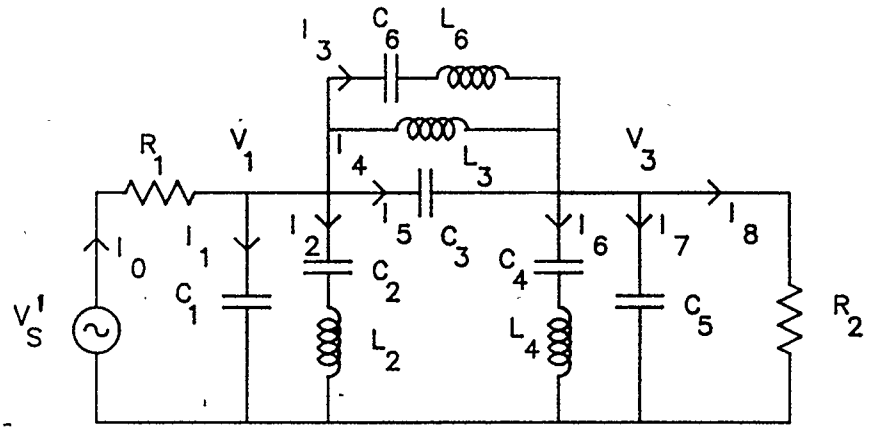


Figure 6.33 Equivalent network of the band-stop filter in Fig. 6.32

Observe that the series and parallel branches of the networks in Fig. 6.33 represent z-type branches. In other words, the parallel branches and the series branch of the network in Fig. 6.33 are of precompensated Foster-II type circuits. Hence, the network in Fig. 6.33 represents a *Z–Z–Z* ladder block. For the reason given in section 5.4 of Chapter 5, it is not possible to construct a *V/I* SFG of this network consisting of only analog integrators.

Since the series branch in Fig. 6.33 contains a z-type transmittance due to the capacitor C_3, the network transformation procedure outlined in Chapter 5 is used to eliminate this capacitance (z-type transmittance) so that the transformed series branch represents a y-type branch and the whole network will transform to a *Z–Y–Z* ladder. The current equation of node-1 is

$$I_o = I_1 + I_2 + I_3 + I_4 + I_5$$

$$= V_1\, sC_1 + I_2 + I_3 + I_4 + (V_1 - V_2)\, s_3 \cdot$$

Solve for V_1 to arrive at

$$V_1 = \frac{1}{s(C_1 + C_3)} (I_o - I_2 - I_3 - I_4) + \frac{C_3}{C_1 + C_3} V_3 \cdot \qquad (6.60)$$

Similarly, the node equation for node-2 is

$$I_3 + I_4 + I_5 = I_6 + I_7 + I_8 \cdot$$

Substitute for I_5 and I_7 to arrive at

$$I_3 + I_4 + (V_1 - V_2)\, sC_3 = I_6 + I_8 + V_3\, sC_5 \cdot$$

Solve for V_3 to obtain

$$V_3 = \frac{1}{s(C_3 + C_5)} (I_3 + I_4 - I_6 - I_8) + \frac{C_3}{C_3 + C_5} V_1 \qquad (6.61)$$

Observe from equations (6.60) and (6.61) that nodal voltage at node-1, V_1, is fed with a fractional part of the nodal voltage at node-2, V_2, and vice versa. Hence the *V/I* SFG constructed using these equations will consists of a feed-forward and feedback path forming an undesirable delay free loop. To eliminate the delay free loop the procedure developed in Chapter 5 is followed. Substitute (6.61) in (6.60) to arrive at

$$V_1 = \frac{1}{s\,P\,(C_1 + C_3)} (I_0 - I_2 - I_3) + \frac{Q}{s\,P} (I_3 - I_6 - I_8) \qquad (6.62)$$

where

$$Q = \frac{C_3}{(C_1 + C_3)(C_3 + C_5)} \quad \text{and} \quad P = (1 - C_3 \cdot Q) \cdot$$

Substitute (6.59) in (6.60) to arrive at

$$V_3 = \frac{1}{s\,P\,(C_3 + C_5)}\,(I_3 - I_6 - I_8) + \frac{M}{s\,P}\,(I_0 - I_2 - I_3) \cdot \qquad (6.63)$$

Using (6.62) and (6.63) the network representing the functional equivalent of the band-stop filter is shown in Fig. 6.34. The current controlled voltage sources in Fig. 6.34 are given by the expressions.

$$CV1 = \frac{1}{s\,P\,(C_1 + C_3)}\,(I_0 - I_2 - I_3) \qquad CV2 = \frac{Q}{s\,P}\,(I_3 - I_6 - I_8)$$

$$CV3 = \frac{1}{s\,P\,(C_3 + C_5)}\,(I_3 - I_6 - I_8) \qquad CV4 = \frac{M}{s\,P}\,(I_0 - I_2 - I_3)$$

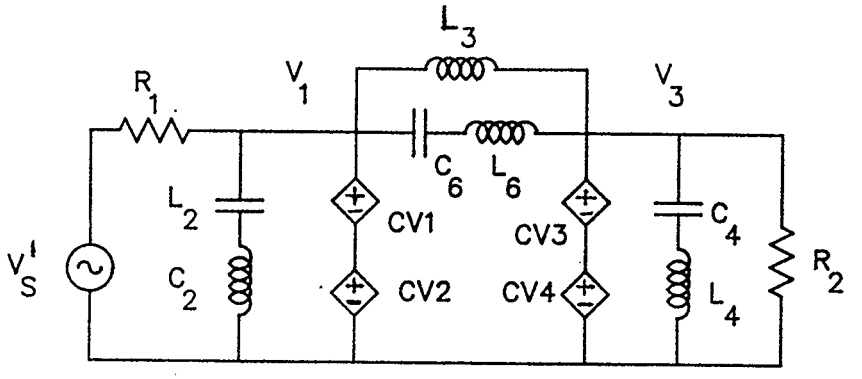


Figure 6.34 Functional equivalent of band-stop filter

Using equations (6.62) and (6.63), the *V/I* SFG of the functional equivalent circuit in Fig. 6.34 can be obtained as shown in Fig. 6.35.

Step-6

In this step the analog signal flow graph is transformed by replacing the analog integrators with LDI blocks and replacing the resistors with $z^{-1/2}$ delay elements. The resulting network consists of only $z^{-1/2}$ elements.

Step-7

To eliminate the half unit delay elements, the discrete network is scaled with $z^{-1/2}$ delay elements. The final realizable digital LDI band-stop ladder filter is shown in Fig. 6.36. The multiplier coefficients of the digital LDI band-stop filter can be evaluated using the expressions,

$$mp0 = 1.0$$

$$mp1 = \frac{T}{P(C_1 + C_3)} = 0.882863$$

$$mp2 = \frac{T\,Q}{P} = 0.699944$$

$$mp3 = \frac{T}{L_2} = 0.438314$$

$$mp4 = \frac{-T}{C_2} = -1.53779$$

$$mp5 = \frac{T}{L_3} = 1.56896$$

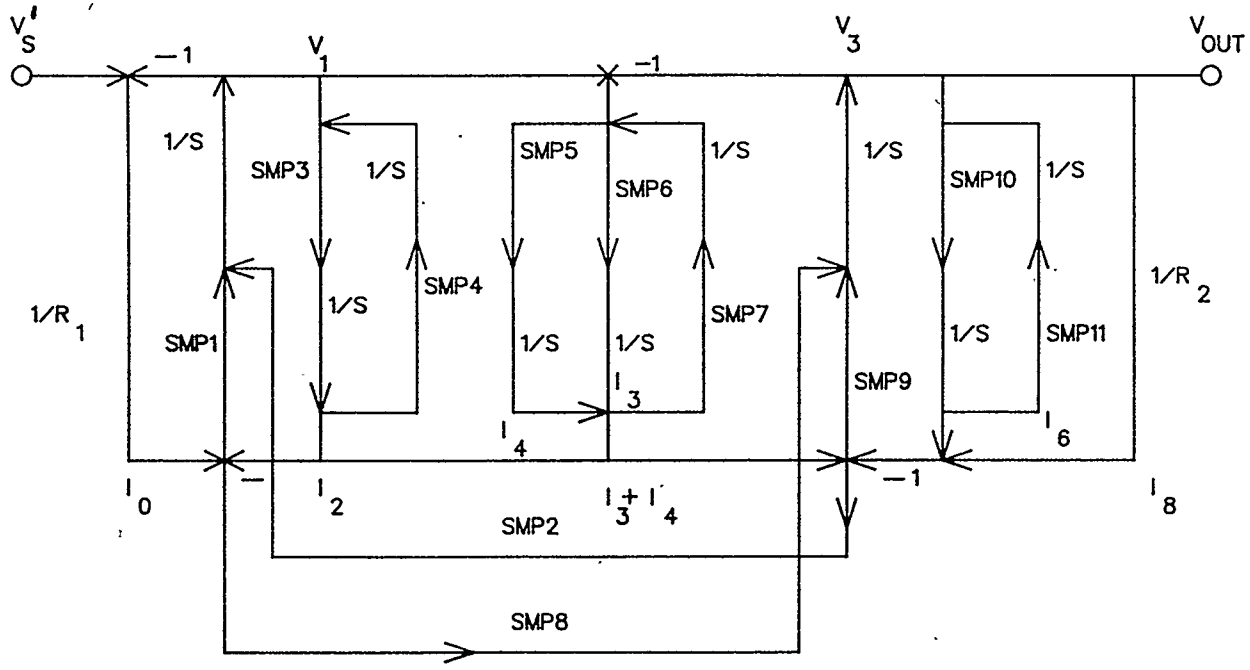


Figure 6.35 *V/I* SFG of the band-stop filter in Fig. 6.34

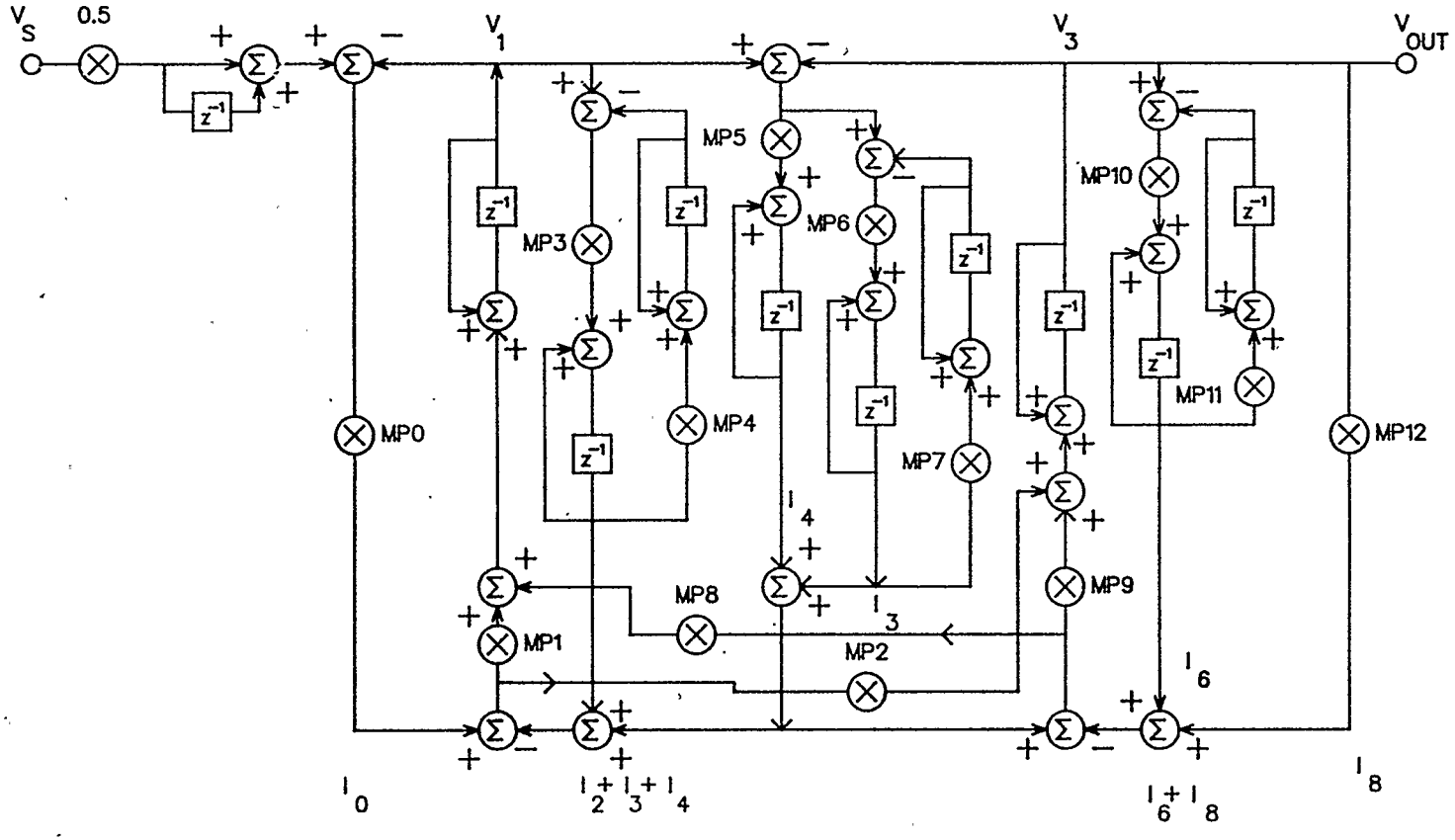


Figure 6.36 Sixth order digital LDI band-stop filter, without delay free loops

$$mp6 = \frac{T}{L_6} = 0.299743$$

$$mp7 = \frac{-T}{C_6} = -2.24900$$

$$mp8 = \frac{TQ}{P} = 0.699944$$

$$mp9 = \frac{T}{P(C_3 + C_5)} = 0.882863$$

$$mp10 = \frac{T}{L_4} = 0.438314$$

$$mp11 = \frac{-T}{C_4} = -1.53799$$

$$mp12 = 1.0$$

The magnitude-frequency response of the digital LDI band-stop filter obtained by simulation is shown in Fig. 6.37. The upper and lower pass-band responses due to multiplier coefficient quantizations are shown in Fig. 6.38 and Fig. 6.39, respectively. It can be seen from these results that the upper pass-band characteristics is more sensitive than the lower pass-band characteristics of the band-stop filter to multiplier coefficient quantizations. From Fig. 6.38 it is clear that the magnitude frequency response of the lower pass-band closely matches the ideal response characteristics for multiplier coefficient quantization of 8 bits, while 17 bits are required to achieve the same result for the upper pass-band. For a 15 bit coefficient quantization the response starts drooping at half the sampling frequency. This behaviour is probably due to the shift in the pole-zero locations of the band-

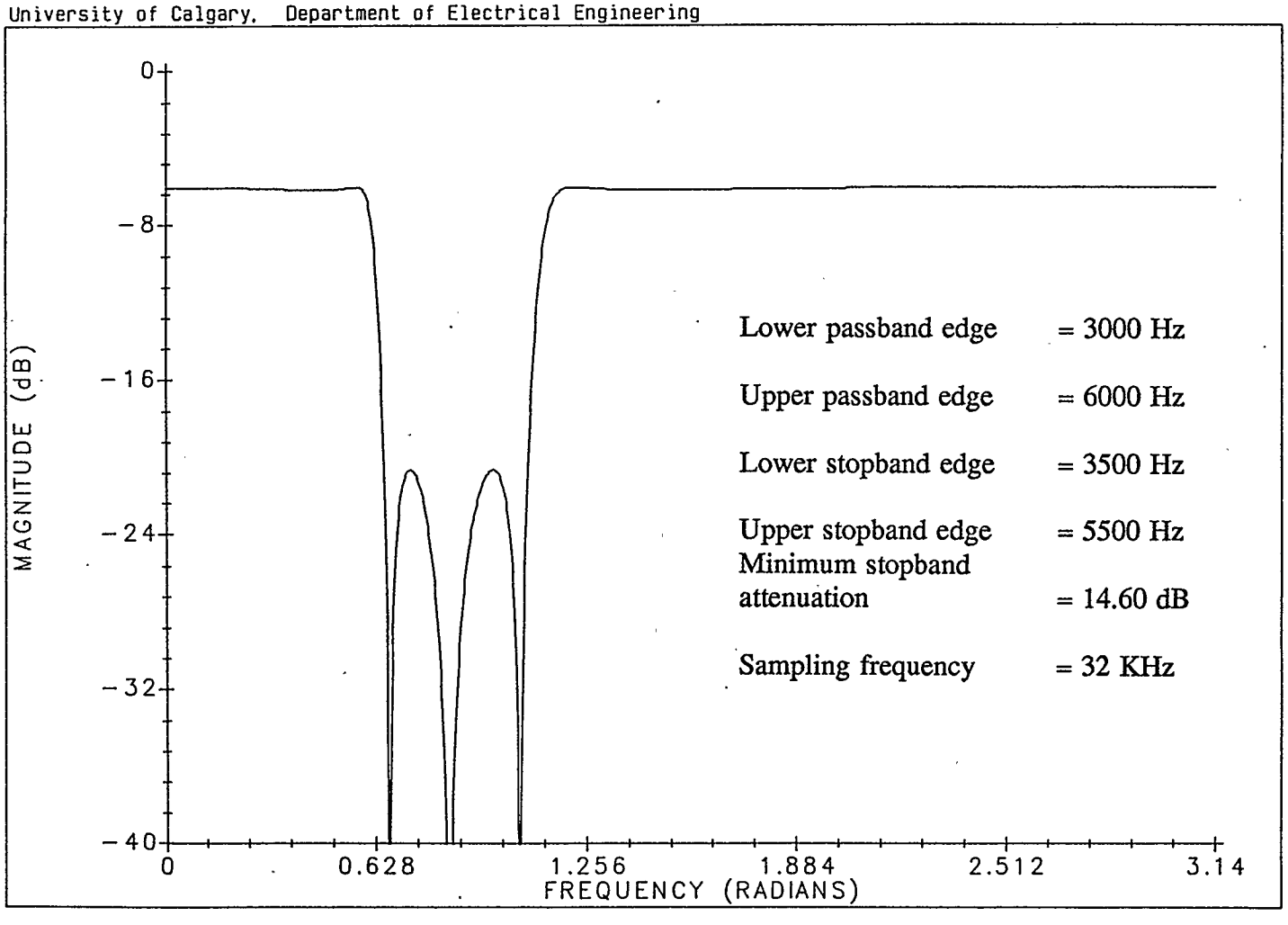


Figure 6.37 Magnitude-frequency response of LDI band-stop filter

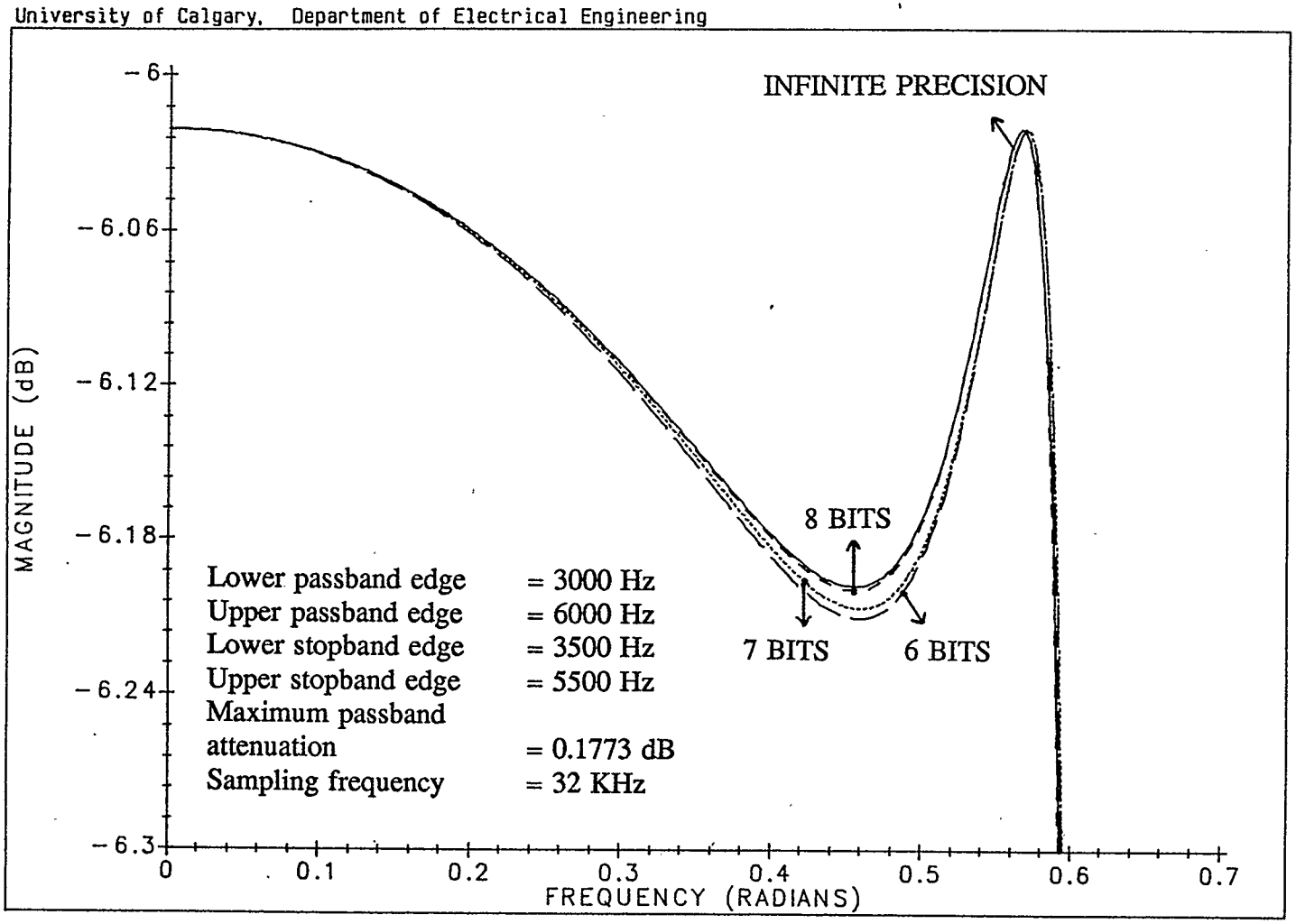


Figure 6.38 Lower pass-band response of digital LDI band-stop filter

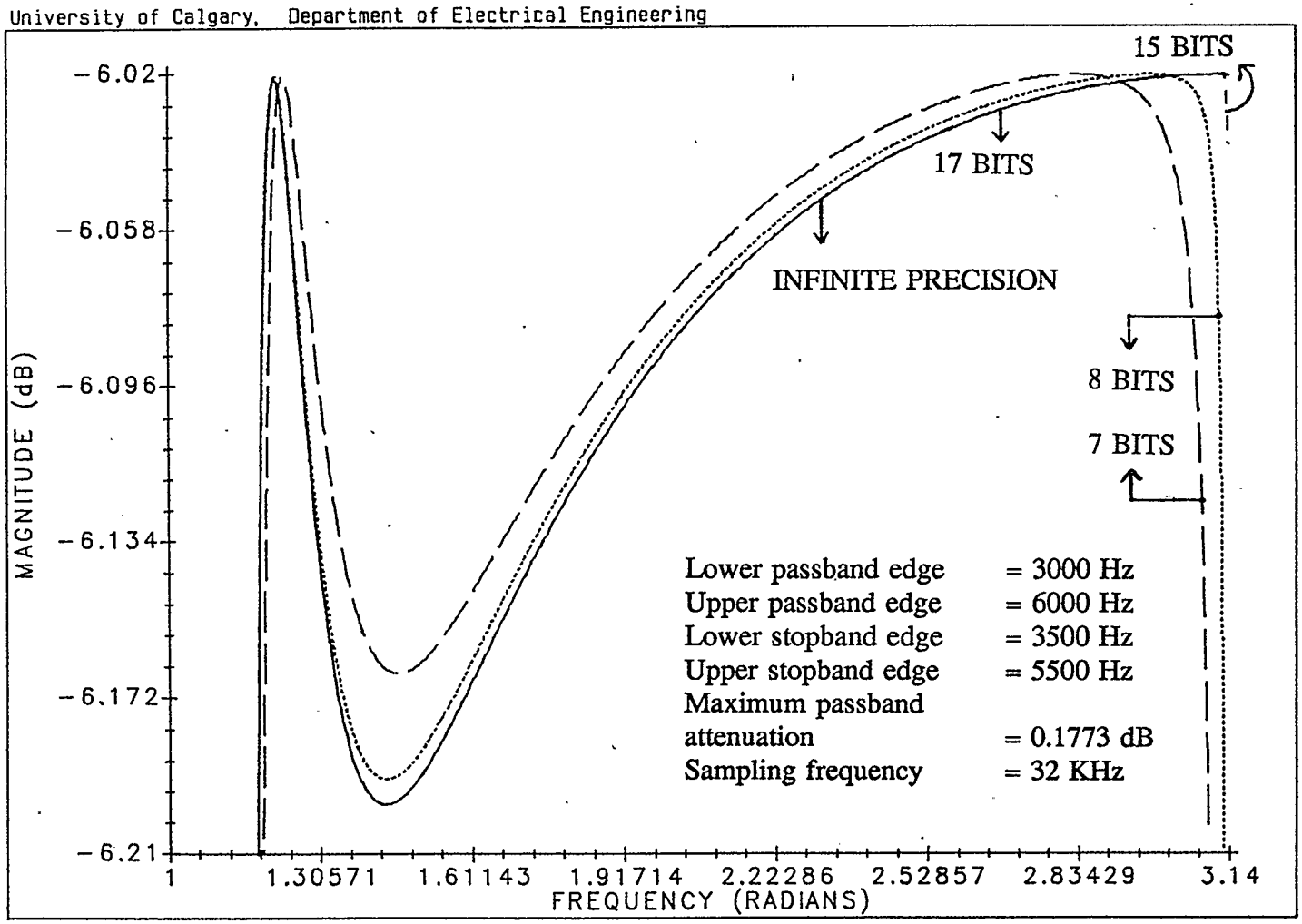


Figure 6.39 Upper pass-band response of digital LDI band-stop filter

stop filter transfer function. This does not deteriorate the filter behaviour, since it is desired in digital filter design that the attenuation at frequencies $(f_s - f_p)$ should be about 30 dB for avoiding aliasing phenomenon.

6.6. LDI and Wave Digital Ladder Filters

A conjecture made by Fettweis [4] that if digital filter structures are modelled after analog ladder structures, which are known to have desirable coefficient sensitivity properties, then the resulting digital ladder structures will also have these properties and can be implemented with low coefficient wordlengths. This conjecture was first investigated by Crochiere [9] by comparing the digital ladder structure coefficient sensitivity of a seventh order Chebychev low-pass filter with that of the equivalent cascade structures of direct and coupled form sections. The conclusion drawn by Crochiere is that the digital ladder structures in many cases can be implemented with lower coefficient wordlengths than the conventional structures [9].

It is demonstrated in Section 3.1 that doubly terminated ladder filters exhibit low sensitivity of their passband frequency response to element value variations. The digital ladder and wave digital filters can be designed directly from the analog ladder prototypes. Fettweis [4] adopted a transmission line model in which every analog element is characterized by a wave port with incident and reflected waves to arrive at wave digital filter structures. Bruton[1] designed an LDI ladder filter based on the analogy with the continuous leapfrog filter in the voltage/current

domain to arrive at digital LDI ladder structures. Chrochiere and Chu have verified in [9,10] that wave digital filters exhibit exceptional lowsensitivity behaviour to quantization of digital multiplier coefficients.

The sensitivity behaviour of the frequency responses of the wave digital and digital LDI ladder filters where both filters are designed from the same analog LC ladder filter prototype are compared in [1]. The analog LC ladder filter chosen for this purpose is a seventh order Chebychev low-pass filter. When the relative passband error criterion proposed by Crochiere [9] is adopted for comparison purposes it is observed that both types of filters exhibit almost identical sensitivity behaviour in the passband [1].

In both design methods adopted by Fettweis and Bruton every multiplier coefficient in the digital structure is directly related to a component value in the analog ladder filter prototype. Note that in the precompensation design method this direct relationship between the multiplier coefficients and the prototype filter element values does not exist. Observing expressions (6.31), (6.33), etc., it is evident that a multiplier coefficient value is an algebraic combination of different element values of the analog ladder filter. Hence, it is useful to compare the sensitivity behaviour of the passband of the digital LDI ladder filter designed using the precompensation method with that of an equivalent wave digital filter.

A wave digital filter is designed from the same analog prototype, shown in Fig. 6.1, so as to meet the same specifications of the digital LDI ladder filter in Fig. 6.9. The Crochiere [9] and root mean square (RMS) error criterions are

chosen to measure the degradation of the filter response. The Crochiere error criterion is given by

$$Relative\ error = \begin{cases} \dfrac{H_{\max} - H_{\min} - A_M}{A_M} & H_{\max} - H_{\min} \geq A_M \\ 0 & H_{\max} - H_{\min} \leq A_M \end{cases}$$

$H_{\max} = \max \left| H\left(e^{j\omega T} \right) \right|$ in the passband (decibels)

$H_{\min} = \min \left| H\left(e^{j\omega T} \right) \right|$ in the passband (decibels)

A_M = Specified passband ripple in (dB).

The *RMS* error criterion is given by

$$RMS\ error = \frac{\sum_{n=1}^{n=M} (x_n^{ID} - x_n^{Q})^2}{M}$$

where

x_n^{ID} - is the nth data point in the passband frequency range of the ideal magnitude-frequency response,

x_n^{Q} - is the nth data point in the passband frequency range of the quantized magnitude-frequency response,

and

M - is the total number of points taken in the passband frequency range.

Quantization of the filter coefficients is performed by rounding of the numbers using fixed point arithmetic. The sign bit is not counted when reference is made to the coefficient wordlength.

The filters are designed for a maximum passband ripple specification of 0.0187 dB. The relative error in the passband for both filters is calculated for the range of 4 to 12 bits. The Crochiere and RMS errors obtained are shown in Fig. 6.40 and Fig. 6.41, respectively. From these figures it is evident that wave digital ladder and elliptic LDI ladder filters exibit comparable relative errors. The RMS error for LDI is less than that of wave digital filter.

Another set of wave and digital LDI ladder filters are designed to meet the same frequency specifications, maximum passband ripple of 1.49 dB and a minimum stopband attenuation of 77 dB. The relative error and RMS error obtained for coefficient quantizations of 4 to 12 bits are shown in Fig. 6.42 and Fig. 6.43, respectively. From these figures it is clear that both the filters exhibit comparable relative errors. The RMS error for LDI is less than that of the wave digital filter.

When the filter hardware of both LDI and wave filters are compared it is found that the bit multiplier product of both filters are equal. The bit multiplier product of any digital filter is defined as the product of the number of multipliers in the digital filter and the number of bits used to represent the multiplier coefficients. The number of adders, multipliers and delay units found in both types

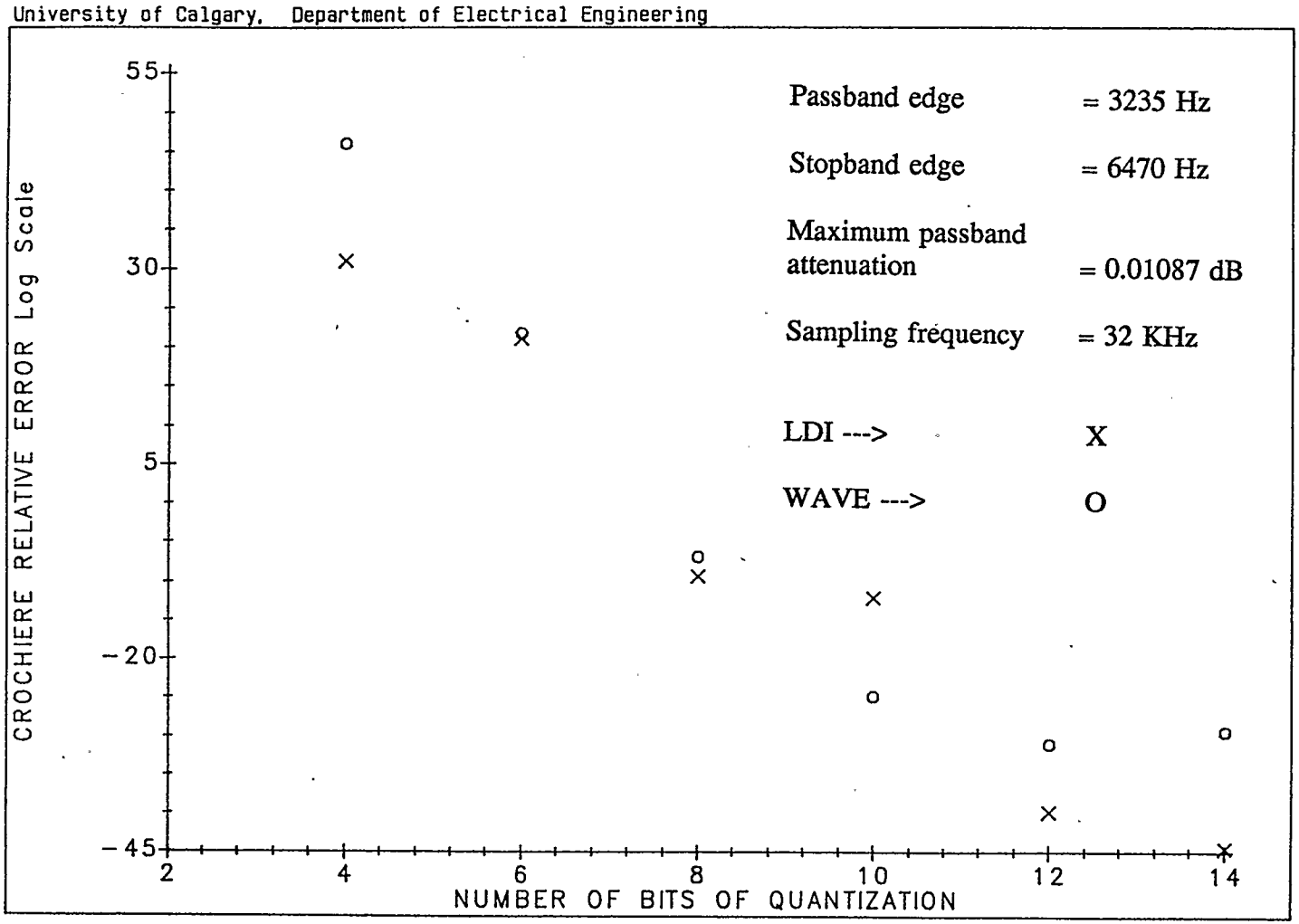


Figure 6.40 Crochiere relative error comparison of LDI and wave digital filters (pass-band ripple = 0.01087 dB)

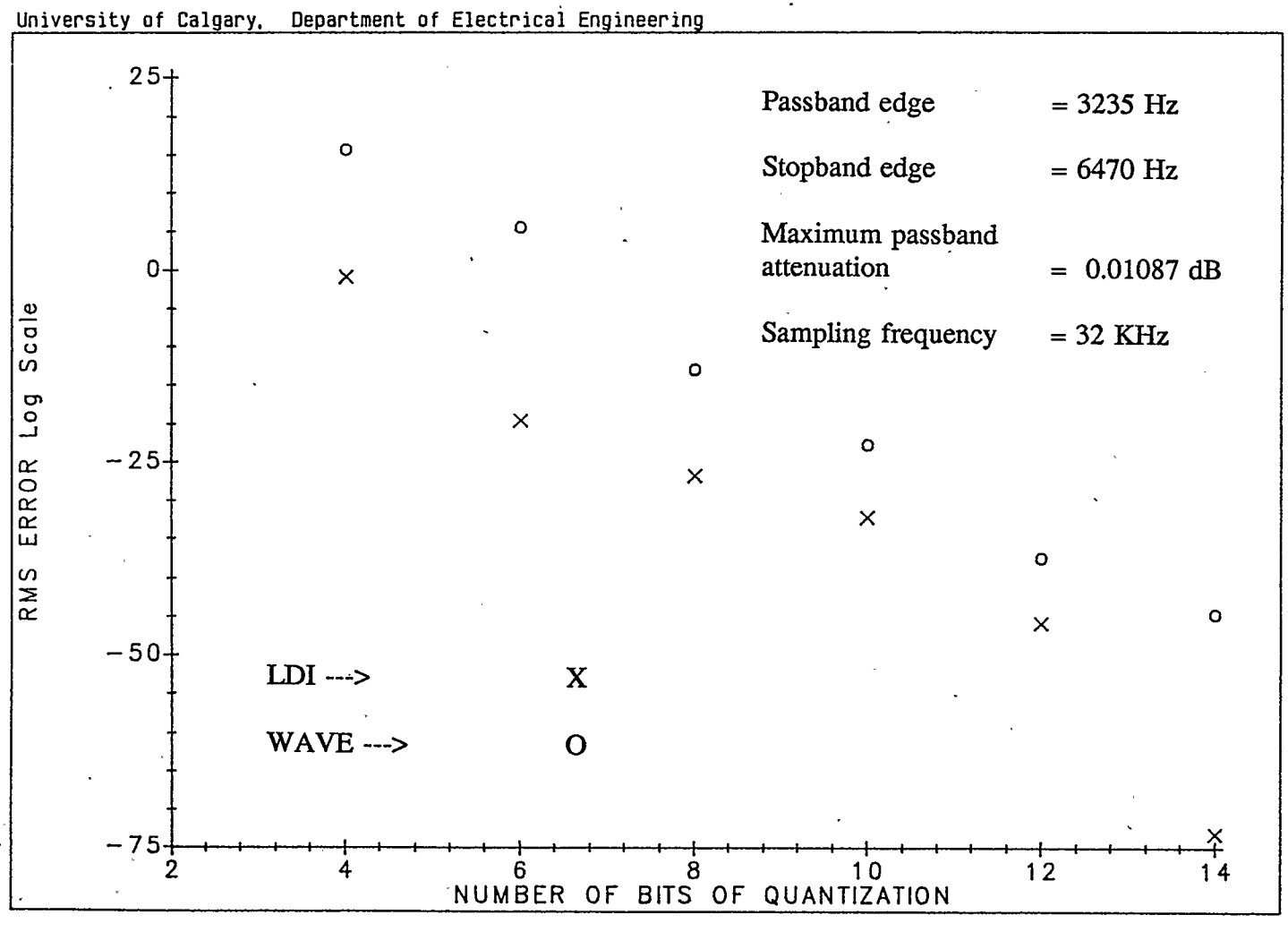


Figure 6.41 RMS error comparison of LDI and wave digital filters (passband ripple = 0.01087 db)

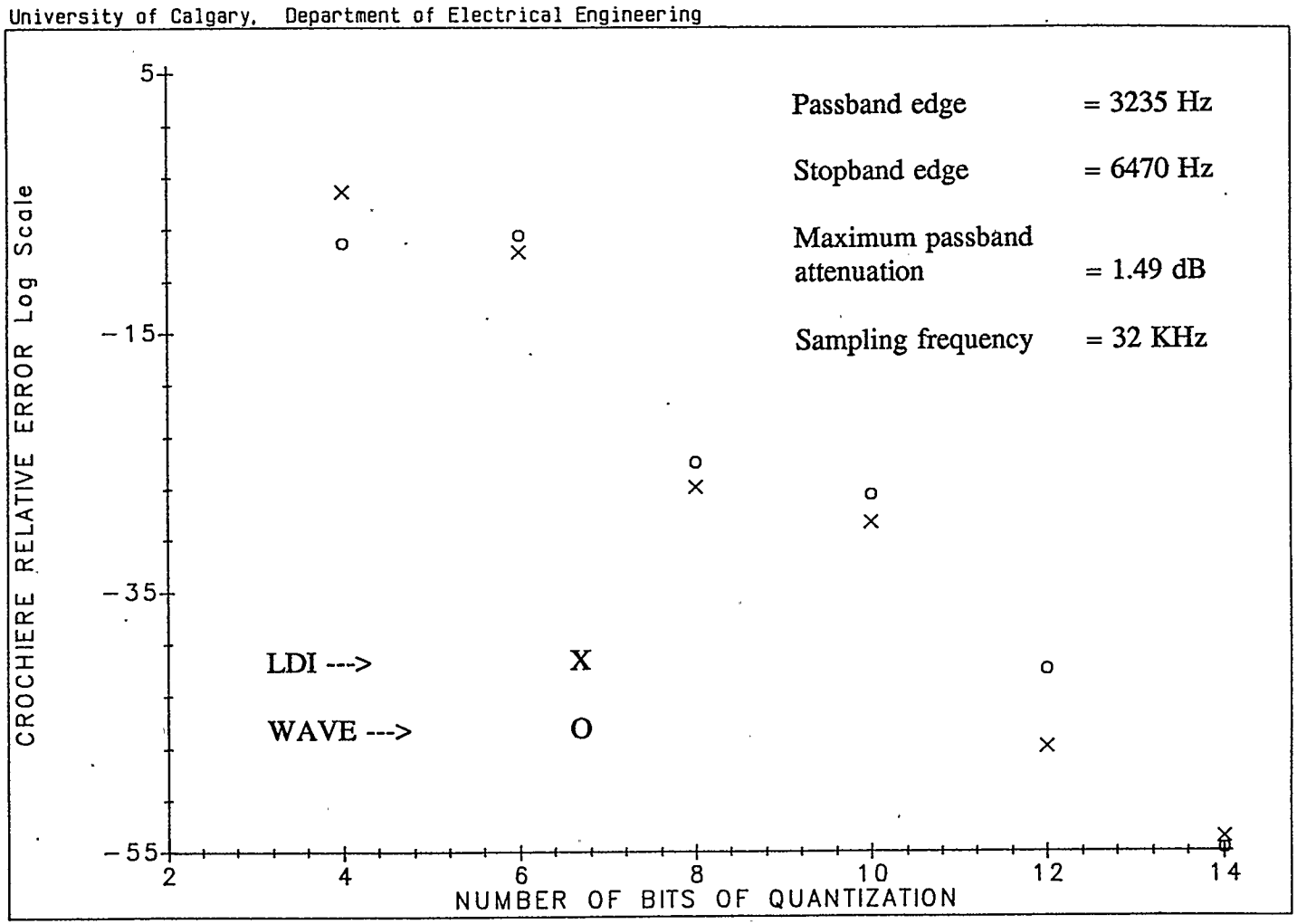


Figure 6.42 Crochiere relative error comparison of LDI and wave digital filters (pass-band ripple = 1.49 dB)

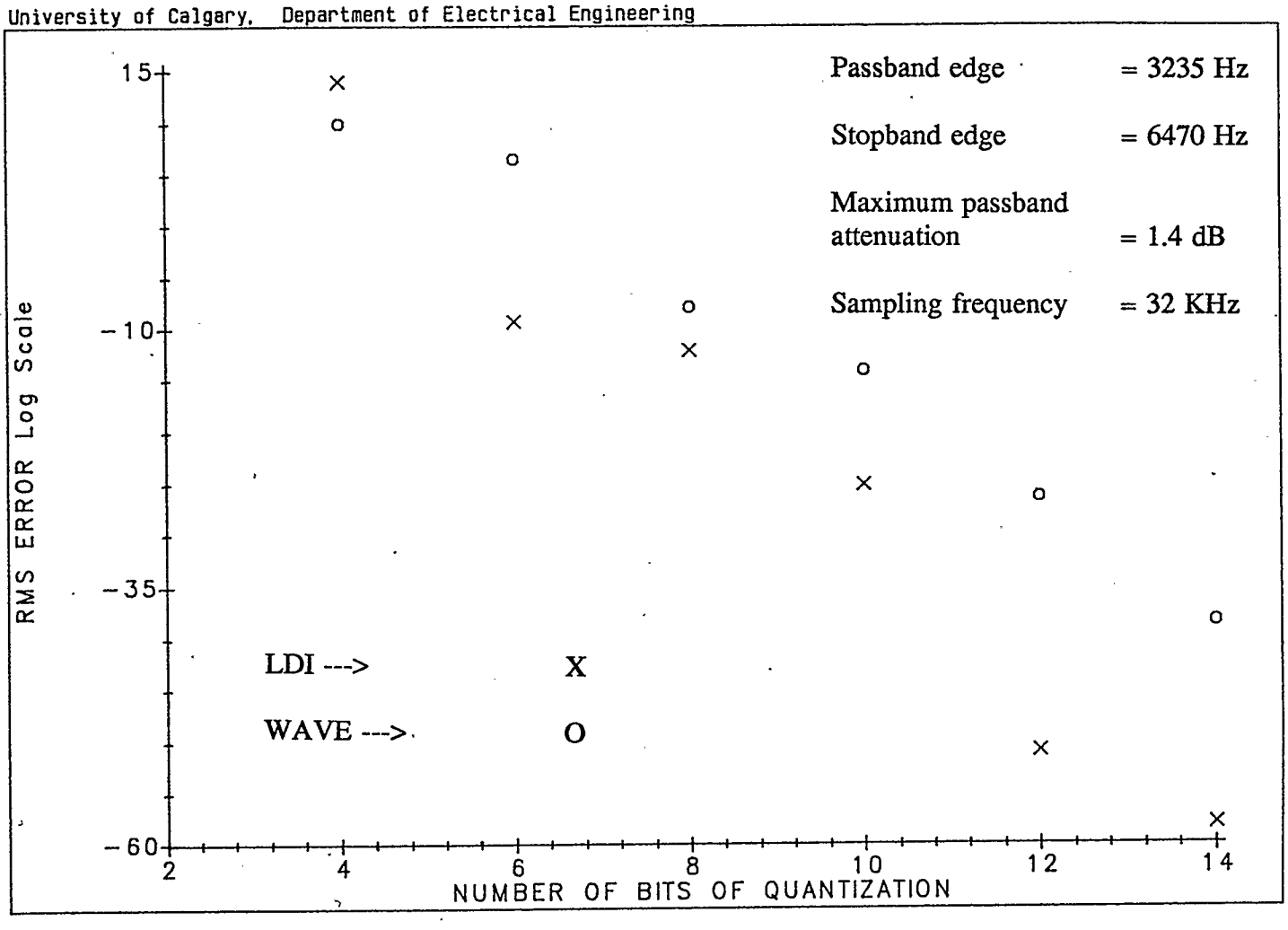


Figure 6.43 RMS error comparison of LDI and wave digital filters (pass-band ripple = 1.49 dB)

of filter hardware are tabulated in the Table 6.3.

	ADDERS	MULTIPLIERS	DELAY-UNITS
LDI Ladder	15	9	5
Wave Digital Ladder	30	8	5

Table 6.3 Hardware comparison of LDI and wave digital filters

Note that the number of unit delays and multipliers in both filter structures are comparable, and the elliptic LDI ladder is found to use one half the number of adders used by the corresponding wave digital ladder filter. The reduced hardware requirements of a digital LDI ladder filter decreases the hardware cost and computational speed of the filter, which is a desirable feature for digital filters.

6.7. Digital Elliptic LDI Ladder Filter Design Program

A computer program has been written in the *C* programming language to design digital LDI ladder filters with elliptic magnitude response using the precompensation design procedure. This program is capable of designing digital LDI low-pass, high-pass, band-pass and band-stop filters. The program uses the specifications of the digital LDI ladder filter as the input and generates the digital filter multiplier coefficients as the output. The corresponding digital filter structures are provided in [54].

The design methods used in this program development are discussed in Sections 6.2, 6.3, 6.4 and 6.5. A structured design method is followed in the development of the program. Each function has one entry point and one exit point. The top-down programming method is adopted. This program structure enables us to add additional modules to the existing software with minimal changes. Programs to design higher order filters can be easily added to the filter design program as and when they are developed.

The design details of this program can be seen in [54]. From the specifications of the digital LDI ladder filter the specifications of the equivalent analog low-pass filter whose passband is normalized to 1 *rad/sec* is first obtained. To obtain the element values of the normalized low-pass filter an analog elliptic ladder filter design program by P. Amstutz [53] is used. Small changes are made in this program to meet our input-output requirements. The main features of the program in [53] are that it can be used to design elliptic analog low-pass filters of up to a maximum order of 31. Only odd order filters can be designed using this program [53]. The same program can be used to design analog elliptic high-pass filters. This program can be conveniently used to design elliptic analog filters provided that no attenuation pole of multiplicity higher than 2 is required.

Functional modules are developed to precompensate different analog ladder filters. The types of digital LDI ladder filters which can be designed using the existing program are

Lowpass	3-9 (Odd-order only)
Highpass	3-9 (Odd-order only)
Bandpass	6,10
Band-stop	6,10

Expressions to obtain higher order filter multiplier coefficients can be derived and functions can be subsequently added as and when the modules are developed. Every module is individually tested and the whole program is developed by adding these tested modules together in steps. The program details are provided in [53].

6.8. Summary

In this chapter the proposed precompensation design procedure is demonstrated with design examples. A fifth order filter digital LDI low-pass filter is designed. It is found that the magnitude-frequency response of this filter for a multiplier coefficient quantization of 12 bits meets the ideal response. The proposed precompensation design method cannot directly be applied to the design of digital LDI high-pass ladder filter. Instead, a digital LDI low-pass filter is transformed to a digital LDI high-pass ladder filter. Examples of designing digital LDI band-pass and band-stop filters are also given. Finally, the sensitivity of the magnitude-frequency responses due to multiplier coefficient quantization of a digi-

tal LDI ladder and wave digital ladder filters are compared. It is found that the filters exhibit comparable sensitivity behaviour. Also digital LDI filters require less hardware than the equivalent wave digital filters. A filter design program is written, which enables to design low-pass, high-pass, band-pass and band-stop filters.

CHAPTER 7

CONCLUSIONS

7.1. Results and Discussion

In this thesis a method of designing digital LDI ladder filters from doubly resistively terminated lossless ladder networks using the bilinear transformation has been proposed. In this method the principles of *V/I* SFG simulation design are used. Filters designed using the *V/I* SFG simulation design principle are known to exhibit low sensitivity of their magnitude frequency characteristics to multiplier coefficient quantizations.

Since the LDI transformation is strictly an unstable transformation, the bilinear transformation is used for frequency warping. However bilinear integrators give rise to delay free loops when used to implement analog integrators directly in the V/I SFG of leapfrog ladder structures. Therefore LDI integrators are used in this design method. Thus this design method combines the advantages of the bilinear frequency mapping with the practical realizability of LDI integrators. In other words, LDI integrators are used to realize the bilinear transformed transfer function of the analog ladder filter networks. In order to accomplish this, a relationship between the LDI and bilinear transformed impedances is first investigated.

The proposed design procedure is simple and straightforward. In the V/I SFG simulation design method proposed by Bruton [1], approximations are made to the

terminating resistors to make the resulting LDI filter stable. In this design method no such approximations are used. No detailed mathematical analysis is involved in the design procedure. The use of standard analog ladder filter design tables or filter design programs simplify the design procedure.

In order for this design method to be used for different types of analog ladder networks, it is required that the V/I SFG of the precompensated networks consist of only analog integrators. A network transformation method is suggested to obtain the V/I SFG of the precompensated ladder networks consisting of only analog integrators. This transformation can also be used to reduce the number of integrators in the *V/I* SFG. A *V/I* SFG synthesis procedure is presented to demonstrate the applicability of this transformation to different networks. This transformation can be used for switched capacitor ladder filter designs also.

Design examples of low-pass, high-pass, band-pass and band-stop filters are presented to demonstrate the design procedure. Even order low-pass filters should be realized by the next higher order filter structure. High-pass filters cannot be designed by the direct application of this design method to analog high-pass ladder filter prototypes. However, a digital LDI ladder low-pass filter is first designed and then transformed into digital LDI high-pass ladder filter.

Filters designed using this precompensation method exhibit low sensitivity of their magnitude-frequency response to multiplier coefficient wordlengths. It is also found that the RMS error in the deviation of the coefficient quantized response from the ideal response of a digital LDI low-pass ladder filter is less than that of

an equivalent wave digital filter. The filters designed using this design method require less hardware than their equivalent wave digital filters. Reduced hardware reduces the computing time, cost and size of the filter. Reduced computing time increases the sampling frequency, which in turn, increases the usable bandwidth of the digital LDI ladder filter.

Another feature of this design method is that the resulting structures have some regularity in their hardware. Higher order filter structures can be easily built because of the modular nature of the filter structure. This design method can be applied to any analog network whose precompensated network consists of only analog integrators in its *V/I* SFG. In short, this design technique combines the advantages of the frequency mapping of the bilinear transformation with the practical advantages of the LDI integrators to yield low sensitivity digital elliptic LDI ladder filter structures.

7.2. Recommendations for further research

One of the limitations of this design method is that it cannot be directly applied to the design of digital LDI high-pass filters. As a possible solution to this problem, a relationship between the LDD and bilinear transformed impedances can be investigated. In this case a network transformation has to be investigated so that the resulting V/I SFG's consists of only analog differentiators. It will be useful to investigate the sensitivity of the magnitude frequency responses due to multiplier coefficient quantization of this class of filters.

Another useful research topic which is recommended is the investigation of the practical realizability of this class of filters in digital filter hardware especially from the VLSI implementation view point. Bit serial architecture is a state of the art design technique popularly used in digital filter implementations [55]. Implementations of these filters using bit serial architectures is worth considering.

Systolic architectures [56] are becoming popular in digital filter implementations. These architectures are successfully applied for the implementation of finite impulse response filters[57]. Some infinite impulse response filters have also been implemented. These architectures allow the implementation of digital filter banks for signal processing, image processing and speech processing applications. Since these filters may be implemented using the dual phase clocking techniques, it is useful to investigate the application of these filters in the design of filter banks using the concepts of systolic cell architectures.

In this thesis the magnitude frequency response due to multiplier coefficient quantizations of a digital LDI filter is compared with that of an equivalent wave digital filter. Fettweis has used the concepts of pseudoenergy to prove that the wave digital filters retain the low sensitivity of their analog ladder prototypes[58]. Similar mathematical analysis may be worked out to prove the low-sensitivity property in these digital LDI ladder structures.

These filters should be examined for the existence of limit cycle oscillations. If there exist any limit cycle oscillations, different methods of eliminating limit cycles can be investigated. The noise behavior of this class of digital filters can

also be investigated and compared with other standard digital filter architectures.

REFERENCES

[1] Bruton L.T., "Low sensitivity digital ladder filters," *IEEE Trans. On Circuits & Syst.,* Vol. CAS-22, pp. 168-176, Mar. 1975.

[2] Gold, B. and C. Rader, *Digital processing of signals* New York: McGraw-Hill, 1969.

[3] Avenhaus, E., "On the design of digital filters with coefficients of limited word length", *IEEE Trans. Audio Electroacoust.,* vol. AU-20, pp. 206-211, Aug. 1972.

[4] Fettweis, A., "Digital filter structures related to classical filter networks," *Arch. Elektr. Ubertr. 25, 79-89 (1971).*

[5] Orchard, H.J., "Inductorless Filters", *Electron Lett.* vol.2, No.6, pp. 224-225, June 1966.

[6] Orchard, H.J., "Loss sensitivities in singly and doubly terminated filters", *IEEE Trans. On Circuits & Syst.,* May 1979, pp. 293-297

[7] Bingham, J.A., "A new type of digital filter with a reciprocal ladder configuration" *IEEE Int. Symp. Circuit Theory,* Dig. Tech. papers, pp. 129-130

[8] Fettweis, A., "Some principles of designing digital filters imitating classical filter structures", *IEEE Trans. On Circuit Theory (Corresp.)* vol. CT-18, pp. 314-316, March 1971.

[9] Crochiere, R.E., "Digital ladder structures and coefficient sensitivity", *IEEE Trans. Audio Electroacoust.* vol. AU-20, pp. 240-246, Oct. 1972.

[10] Chu, A. and R. E. Crochiere, "Comments and experimental results on optimal digital ladder structures", *IEEE Trans. Audio Electroacoust (Corresp.)* vol. AU-20, pp. 317-318 Oct. 1972.

[11] Sedlmeyer, A. and A. Fettweis, "Digital filters with true ladder configuration", *Int. Journal Circuit Theory Appl.,* vol. 1, pp. 5-10 1973

[12] Sedlmeyer, A. and A. Fettweis, "Realization of digital filters with true ladder configuration" in *Proc. 1973 Int. Symp. Circuit Theory,* Toronto, Ont. Canada, pp. 149-152

[13] Renner, K. and S.C. Gupta, "On the design of wave digital filters with low sensitivity properties", *IEEE Trans. On Circuit Theory,* Vol. CT-20, pp. 555-567, Sept. 1973.

[14] Vaughan-Pope, D.A., and L. T. Bruton, "Transfer function synthesis using generalized doubly terminated two pair networks," *IEEE Trans. On Circuits & Syst.,* vol. CAS-24, pp. 79-88, Feb. 1977.

[15] Liu, E.S.K., L.E. Turner and L.T. Bruton, "Exact synthesis of LDI and LDD ladder filters," *IEEE Trans. On Circuits & Syst.,* vol. CAS-31, No 4 pp. 369-381, Apr. 1984.

[16] Bruton, L.T. and D.A. Vaughan-Pope, "Synthesis of digital ladder filters from LC filters," *IEEE Trans. On Circuits & Syst.,* Vol. CAS-23, pp. 395-402, June. 1976.

[17] Lee, M.S. and C. Chang, "Low sensitivity switched capacitor ladder filters", *IEEE Trans. On Circuits & Syst.,* Vol. CAS-27, pp. 475-480, June 1980.

[18] Lee, M.S. and C. Chang, "Switched capacitor filters using the LDI and Bilinear transformations," *IEEE Trans. On Circuits & Syst.,* Vol. CAS-28, pp. 265-270, Apr. 1981.

[19] Davis, R.D. and T.N. Trick, "Optimum design of lowpass switched capacitor ladder filters", *IEEE Trans. On Circuits & Syst.,* Vol. CAS-28, pp. 522-527, June. 1980.

[20] Jacobs, G.M., D.J. Allstot, R.W. Broderson and P.R. Gray, "Design techniques for MOS switched capacitor ladder filters," *IEEE Trans. On Circuits & Syst.,* Vol. CAS-25, pp. 1014-1021, Dec. 1978.

[21] Choi, T.C. and R.W. Brodersen, "Considerations for high frequency switched capacitor ladder filters," *IEEE Trans. On Circuits & Syst.,* Vol. CAS-27,No 6 pp. 545-552, June. 1980.

[22] Martin, K., "Improved circuits for the realization of switched capacitor ladder filters," *IEEE Trans. On Circuits & Syst.,* Vol. CAS-27, No 4 pp. 237-244, Apr. 1980.

[23] Allstot, D.J., R.W. Brodersen and P.R. Gray, "MOS Switched capacitor ladder filters," *IEEE Journal of Solid State Ckts.,* Vol. SC -13 No-6, pp. 806-814, Dec. 1978.

[24] Bruton L.T., "RC Active circuits", *Prentice-Hall Inc., Englewood Cliffs,* New Jersey, 1980.

[25] Antonio, A., "Digital Filters, Analysis and Design", *McGraw-Hill Book Company,* 1979.

[26] Rabiner, L.R. and B. Gold, "Theory and Application of Digital Signal Processing", *Prentice-Hall, Englewood Cliffs,* N.J., 1975.

[27] Oppenheim, A.V. and R.W. Schafer, "Digital Signal Processing", *Prentice-Hall, Englewood Cliffs,* N.J., 1975.

[28] Childers D. and A. Durling, "Digital filters and signal processing", *Welt Publishing Company,* New York, 1975.

[29] Schafer R.W, and Rabiner L.R, "A digital signal processings approach to interpolation", *Proceeding of the IEEE,* Vol.61, No.6, June 1973.

[30] Kaiser, J.F., "Some practical considerations in the realization of linear digital filters", *Proc. annual 3rd Allerton Conf. Circuit and System Theory,* Monti Cello, IL. Oct. 1969, pp. 69-78

[31] Liu, B., "Effect of finite wordlength on the accuracy of digital filters - A review", *IEEE Tran. On Circuit Theory,* Nov. 1971

[32] Gold, B. and C.M. Rader, "Effects of quantization noise in digital filters", *AFIPS Proc., 28,* pp. 213-219 (1966)

[33] Katzenelson, J., "On errors introduced by combined sampling and quantization", *IRE Trans. Automat. Control.,* Vol. AC-7, Apr. 1962, pp. 58-68.

[34] Knowles, J.B. and R. Edwards, "Effects of finite wordlength computer in a sampled data feedback system" *Proc., Inst., Elec., Eng., Vol., 112, June 1965, pp. 1197-1207*

[35] Kaiser, J.F., "Digital Filters in System Analysis by Digital Computers", F.F. Kuo and J.F. Kaiser, Eds. New York, *John Wiley & Sons, 1966, pp. 218-285.*

[36] Wilkinson, J.K., "Rounding Errors in Algebraic Process", *Prentice-Hall, Englewood Cliffs,* N.J., 1963.

[37] Bennett, W.R., "Spectra of Quantized Signals", *Bell Syst., Tech. J.,* Vol. 27, July 1948, pp. 446-472.

[38] Meerkotter, K. and Wegner, W, "A new second order digital filter without parasitic oscillations", *Arch, Elck., Ubertragung,* Vol 29, No 7/8 pp. 312-314, 1975.

[39] Kaiser, J.F., "The Digital Filter and Speech Communication", *IEEE Trans. Audio Electroacoust.* Vol. AU-16, pp. 180-183, June 1968.

[40] Jackson, L.B., "An Analysis of Limit Cycles due to Multiplication Rounding in Recursive Digital Filters", in *Proc. 7th Anul. Allerton Conf. Circuit and System Theory,* Monti Cello, IL. Oct. 1969.

[41] Ebert, P.M., J.E. Mazo and M.G. Taylor, "Overflow Oscillations in Digital Filters", *Bell. Syst. Tech. Jou.,* Vol. 48, pp. 2999-3020, Nov. 1969.

[42] Rabiner, L.R. et.al., "Terminology in Digital Signal Processing", *IEEE Trans. Audio Electroacoult.,* Vol. AU-20, pp. 322-337, Dec. 1972.

[43] Butterweck, H.J., "Suppression of Parasitic Oscillations in Second-Order Digital Filters by means of Controlled Rounding Arithmetic", *Arch. Elek. Ubertraqung.,* Vol. 29, pp. 371-374, Sept. 1975.

[44] Lawrence, V.B., "Control of Limit Cycles Oscillations in Second-Order Recursive Digital Filters using Constrained random Quantization", *IEEE Trans. on ASSP,* Vol. ASSP-26, No. 2, April 1978.

[45] Barnes, C.W. and A.T. Fam, "Minimum Norm Recursive Digital Filters that are Free of Overflow Limit Cycles", *ibid.,* 1977 CAS-24, pp. 569-574.

[46] Williams, A.B., "Electronic filter design handbook," *McGraw-Hill Book Company.,* 1981.

[47] Zverev, A.I., "Handbook of Filter Synthesis", *John Wiley & Sons,* New York, 1967.

[48] Masry, E.I. and A.A. Sakla, "Low sensitivity digital ladder filters" *Proc. 13th* Asilomar Conf. on Circuits, Systems and Computers, (Pacific Grove, CA) Nov. 1979, pp. 273-278.

[49] Peled, A. and B. Liu, "Digital Signal Processing", *John Wiley and Sons,* 1976.

[50] Bruton, L.T., "Topological equivalent of inductorless ladder structures using integrators", *IEEE Trans. Audio Electroacoust.,* Vol. AV-20, pp. 317-318, Oct. 1972.

[51] Girling F.E.J. and E.F Good, "Active filters -12, The leapfrog or active ladder synthesis", *Wireless world,* Vol. 76, pp. 341-345, July 1970.

[52] Vaughan-Pope, D.A., " Low sensitivity digital ladder filters", *Phd thesis, Dept. Of Elec. Eng.*, Univ. Of Calgary, Calgary, Canada, May, 1976.

[53] Amstutz, P., "Elliptic approximation and elliptic filter design on small computers", *IEEE Trans. On Circuits & Systs.*, vol. CAS-25, No-12i, pp 1001-1011

[54] Ramesh, B.K and Turner L.E, "Digital LDI ladder filter design program", *Dept. Of Electrical Engineering, Univ. of Calgary* (Under preparation)

[55] Denyer, P. and Renshaw, D, "VLSI signal processing : A bit serial approach", *Addison-Wesley Publishing Company,* 1985.

[56] Kung, H.T, Whitehouse, H.J and Kailath, J, "VLSI and modern signal processing", *Prentice-Hall Inc.*, Englewood Cliffs, New Jersey 07632

[58] Fettweis, "Pseudopassivity, sensitivity and stability of wave digital filters", *IEEE Trans. On Circuit Theory,* Vol. CT-19, No-6, pp. 668-673, Nov 1972