

THE UNIVERSITY OF CALGARY

A High Efficiency Linearized Radio Frequency

Power Amplifier

by

Garry Funk

A THESIS

**SUBMITTED TO THE FACULTY OF GRADUATE STUDIES
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE
DEGREE OF MASTER OF SCIENCE**

**DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING**

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled "**A High Efficiency Linearized Radio Frequency Power Amplifier**", submitted by Garry Funk in partial fulfillment of the requirements for the degree of Master of Science.

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Abstract

Personal Communication Services have placed new demands on telecommunications technology. New, spectrally efficient, modulation schemes require better linear performance from the power amplifier. A truly portable terminal requires energy efficiency to ensure long talk time without bulky batteries.

Traditional Class A, B, AB and C amplifiers are quite linear but have low efficiency when converting dc power into radio frequency power. High efficiency Class D, E, F and S amplifiers, on the other hand, are unfortunately highly non-linear. A linearization technique that reduces signal distortion while using high efficiency amplifiers is required.

This thesis discusses the design, analysis and implementation of a distortion reduction system for a 1 GHz, 1/2 Watt Class E amplifier. Envelope elimination and restoration is the linearization method chosen to achieve reduction of signal distortion. The measured performance of the system is presented along with a review of high efficiency amplifiers and linearization techniques.

Acknowledgements

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Dedication

I dedicate this thesis to my sons Nicholas and Dylan, and my wife Deb.

For forming the solid foundation upon which my confidence rests.

For proving that the strength of love conquers any problem.

Table of Contents

Approval Page	ii
Abstract	iii
Acknowledgements	iv
Dedication	v
Table of Contents	vi
List of Figures	ix
List of Symbols and Abbreviations	xiii
Chapter One - Introduction	1
1.1. Personal Communications Services	1
1.2. High Efficiency Amplifiers and Linearization Techniques.....	2
1.3. Thesis Outline	3
Chapter Two - High Efficiency Amplifiers	5
2.1. Classes of High Efficiency Amplifiers.....	5
2.1.1. Class D.....	5
2.1.2. Class E.....	8
2.1.3. Class F	12
2.1.4. Class S.....	14
2.2. Amplifier Distortion.....	17
2.2.1. Amplitude Distortion	17
2.2.2. Phase Distortion	20
2.2.3. Pulse Width Modulation Distortion	20
Chapter Three - Highly Non-Linear Amplifier Linearization Techniques	22
3.1. Linear Amplification using Non-Linear Components.....	25
3.1.1. Simple System	26
3.1.2. Chireix System	28

3.2.	Envelope Elimination and Restoration	33
3.2.1.	Basic System	33
3.2.2.	Enhanced System	36
Chapter Four - System Analysis.....		38
4.1.	System Distortion	38
4.1.1.	System Components	40
4.1.1.1.	Envelope Detector	40
4.1.1.2.	Modulator.....	43
4.1.1.3.	Limiter.....	46
4.1.1.4.	Main RF PA	52
4.1.2.	Intermodulation Distortion Products	54
4.1.2.1.	Intermodulation Distortion due to Imperfect Limiter Performance	55
4.1.2.2.	Intermodulation Distortion due to Time Delay	57
4.1.2.3.	Intermodulation Distortion due to the Modulator Frequency Response	60
4.1.2.3.	Intermodulation Distortion due to Feedthrough	62
4.2.	System Efficiency.....	64
Chapter Five - Experimental Circuit, Measurements and Results.....		67
5.1.	System Implementation.....	67
5.1.1.	Circuit Module Specifications	68
5.1.2.	Modulator Construction	69
5.1.3.	Phase Extractor Construction	70
5.1.4.	Main Amplifier Construction	71
5.2.	Experimental Procedure and Results.....	73

5.2.1.	Main Power Amplifier	73
5.2.1.1.	Frequency Response	73
5.2.1.2.	Linearity and Feedthrough	75
5.2.2.	Envelope Detector	78
5.2.3.	Modulator	81
5.2.3.1.	Linearity	81
5.2.3.2.	Frequency Response	82
5.2.3.3.	Efficiency	83
5.2.4.	Phase Extractor and Delay Measurement.....	85
5.2.5.	Reduction of Intermodulation Distortion Products	87
Chapter Six - Conclusions and Future Work.....		92
References		94
Appendices		98
A.1.	Limiter Analysis (limiting angle $e = 57.9$ deg)	99
A.2.	Delay Analysis (delay = 6.0 deg, $e = 0.9$ deg)	105
A.3.	Frequency Analysis (cutoff freq = 6.25 fundamental)	111

List of Figures

Figure 2.1	Complementary Voltage-Switching Class D PA (a) Schematic Circuit and (b) Equivalent Circuit	6
Figure 2.2	Complementary Voltage-Switching Class D PA waveforms	6
Figure 2.3	Class E PA (a) Schematic Circuit and (b) Equivalent Circuit	8
Figure 2.4	Class E Amplifier Waveforms (a) Switch timing (b) Voltage across the switch (c) Current through the switch (d) Output voltage at the load	10
Figure 2.5	Third Harmonic Peaking Class F PA Schematic Circuit	12
Figure 2.6	Third Harmonic Peaking Class F PA wave forms	13
Figure 2.7	Class S Modulator Schematic	15
Figure 2.8	Class S Switching Wave forms	16
Figure 2.9	Definition of 1 dB Compression Point	18
Figure 2.10	Output Spectrum of a device with two input sinusoids and third order distortion	19
Figure 2.11	Spectral Response of a PWM Signal	20
Figure 2.12	Envelope Signal and Corresponding Frequency Spectrum	21
Figure 3.1	Simplified FeedForward System	23
Figure 3.2	Simplified Feedback System	23
Figure 3.3	Simplified Predistortion System	25
Figure 3.4	Simple Linc System	26
Figure 3.5	Chireix LINC System	28
Figure 3.6	Admittance at Output of Power Amplifiers with $B_s = 0$, Normalization; $R_0 = 1$, $R_L = 2$	30
Figure 3.7	Efficiency of Chireix LINC System with B_s ' at Various Values, Normalization; $R_0 = 1$, $R_L = 1$	32

Figure 3.8	Basic Envelope Elimination and Restoration System	33
Figure 3.9	Phasor Diagram of Two Tone Input Signal	34
Figure 3.10	Envelope Elimination and Restoration System with Envelope Feedback	36
Figure 4.1	Simplified Block Diagram of Method for Determining Distortion	39
Figure 4.2	Time Domain and Truncated Frequency Domain Representation of an Ideal Envelope Signal	40
Figure 4.3	Non-Ideal Envelope Characteristic	41
Figure 4.4	Modulator Block Diagram	43
Figure 4.5	Ideal Limiter Waveforms (a) Input Signal (b) Envelope Limiter Gain Function (c) Phase Information at Limiter Output	46
Figure 4.6	Non-ideal Envelope Limiter Gain Function	47
Figure 4.7	Relationship of Envelope Signal and ELGF for Determination of Fourier Series Variables	49
Figure 4.8	Calculation of Phase Modulation Component Spectra (a) Modulation of first tone with ELGF (b) Modulation of second tone with ELGF (c) Frequency Spectra at output of Limiter (d) Time domain output of Limiter	50
Figure 4.9	Main Power Amplifier Block Diagram	52
Figure 4.10	Typical Amplitude Modulation Transfer Function for a Class E Amplifier	53
Figure 4.11	Feedthrough Network	53
Figure 4.12	Effect of Limiting Angle on Intermodulation Distortion Products.....	56

Figure 4.13	Delay Angle	58
Figure 4.14	Effect of Delay Angle on Intermodulation Distortion Products	59
Figure 4.15	Effect of Modulator Cutoff Frequency on Intermodulation Distortion Products	61
Figure 4.16	Class E Efficiency versus Phase Signal Input Power	63
Figure 4.17	Closed System Used for Efficiency Analysis	64
Figure 4.18	Comparison of Total Efficiency versus Individual Modulator and Main Amplifier Efficiency (Main Amplifier Power Gain = 20).....	66
Figure 5.1	System Implementation	67
Figure 5.2	Modulator Schematic	69
Figure 5.3	Phase Extractor Schematic	71
Figure 5.4	Lumped Component Schematic of Class E Amplifier	72
Figure 5.5	Test Setup for Determination of Class E Amplifier's Operating Characteristics	73
Figure 5.6	Class E Amplifier Total Efficiency vs. Frequency	74
Figure 5.7	Class E Amplifier Total Efficiency vs. Input Power	75
Figure 5.8	Class E Amplifier Amplitude Modulation Characteristic.....	76
Figure 5.9	Class E Amplifier Total Efficiency vs. Supply Voltage	77
Figure 5.10	Envelope Detector Test Setup.....	78
Figure 5.11	Envelope Detector Response with Input Signals at 1040.00 MHz and 1040.03 MHz	79
Figure 5.12	Envelope Detector Response with Input Signals at 1040 MHz and 1041 MHz	80
Figure 5.13	Modulator Linearity	81
Figure 5.14	Modulator Frequency Response	82

Figure 5.15	Modulator Collector Efficiency	84
Figure 5.16	Test Setup to Measure Limiting Angle and Signal Delay	85
Figure 5.17	Measurement of Limiting Angle and Signal Delay	86
Figure 5.18	Theoretical Limiter Frequency Spectrum (Limiting Angle = 5.3°).....	88
Figure 5.19	Measured Effect of Modulator Cutoff Frequency and Class E Feedthrough Effects on Intermodulation Distortion Products	89
Figure 5.20	Performance measurement with and without Distortion Reduction System Enabled	91

List of Symbols and Abbreviations

α	input coupling factor
β	output coupling factor
ϕ	phase angle
$\phi(t)$	maximum phase deviation
γ	modulator sensitivity
η	efficiency
η_T	total efficiency
λ	wavelength
π	numerical value of pi
Σ	summation
θ	product of angular frequency and time
ω	angular frequency (radians / second)
Ω_0	normalization frequency
∞	infinity
AM	Amplitude Modulation
b	filter coefficients
B	susceptance
C	capacitor
d	delay angle
dB	logarithmic ratio of powers, i.e. $10 \log_{10}(\text{power}_1 / \text{power}_2)$
dBc	logarithmic ratio referenced to the main signal
dBm	logarithmic ratio referenced to 1 mW
dc	direct current
DFFT	Discrete Fast Fourier Transform
DQPSK	Differential Quadrature Phase Shift Keying
DSP	Digital Signal Processing
e	limiting angle
EER	Envelope Elimination and Restoration
ELGF	Envelope Limiter Gain Function
Em	maximum value of the envelope signal
Env	general envelope signal
f	frequency (Hz)
f_c	cutoff frequency

FET	Field Effect Transistor
f_m	frequency of the message signal
f_o	fundamental frequency
FR4	fiberglass printed circuit board
G	open loop gain
GaAsFET	Gallium Arsenide Field Effect Transistor
GHz	gigaHertz
H	feedback loop transfer function
HF	High Frequency
Hz	Hertz (cycles / second)
I	large signal current
i	instantaneous small signal current
i_c	instantaneous small signal collector current
I_{cm}	maximum collector current
I_{dc}	large signal current provided from power supply
IDFFT	Inverse Discrete Fast Fourier Transform
Im	imaginary axis
IMD	intermodulation distortion product
IMD3	third order intermodulation distortion products
IMD5	fifth order intermodulation distortion products
IMD7	seventh order intermodulation distortion products
I_o	output current
IP	intersection point
i_s	instantaneous small signal switch current
J_n	Bessel function of the first kind of order n
k_1	first order power series coefficient
k_2	second order power series coefficient
k_3	third order power series coefficient
kHz	kiloHertz
L	inductor
LINC	Linear Amplification using Non-linear Components
M	power series coefficient
MHz	megaHertz
N	minimum value or envelope floor

PA	power amplifier
PCS	Personal Communication Services
P_{dc}	dc power
P_i	input power
PLL	Phase Locked Loop
PM	Phase Modulation
P_o	output power
PWM	Pulse Width Modulation
Q	Transistor
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
R	resistor
Re	real axis
RF	Radio Frequency
RFC	Radio Frequency Choke
rms	root mean square
S	scattering parameter
SC	Splitter / Combiner
SMA	standard radio frequency connector
SWR	Standing Wave Ratio
t	time
T	time period
v	instantaneous small signal voltage
V	large signal voltage
V_{bias}	large signal bias voltage
v_c	instantaneous small signal transistor collector voltage, referenced to ground
V_{cc}	large signal collector power supply voltage
v_{ce}	instantaneous small signal transistor voltage measured at the collector, referenced to the emitter
v_{cm3}	maximum instantaneous collector voltage measured at the third harmonic frequency
v_D	instantaneous small signal diode voltage, referenced to ground
V_{DD}	large signal drain power supply voltage

V_{ds}	instantaneous small signal FET drain voltage referenced to the source
V_{gs}	instantaneous small signal gate voltage referenced to the source
v_o	instantaneous small signal output voltage, referenced to ground
V_{om}	maximum output voltage
V_p	peak envelope voltage
V_t	threshold voltage
W	Watt
X	reactance
Y	admittance
y	switch off time (radians)
Z	impedance

Chapter One - Introduction

The development of an amplifier that possesses the characteristics of linearity and high efficiency may seem to be unattainable. However, the use of highly efficient amplifiers combined with a linearization technique can achieve these goals. Amplifiers which provide these advantages will find use in a variety of communications products of today and those of the future.

1.1. Personal Communications Services

PCS is the acronym that has been given to a new concept in telecommunications services. It is intended that these services provide the user with freedom of movement while initiating and receiving calls. The user will be assigned a unique and personal number with which they may be reached anywhere in the world on either public or private networks. The person's terminal may be fixed, movable or mobile and will enable the user to define a set of services which suits his or her needs [1].

To achieve this vision, PCS will require an unprecedented integration of telecommunications systems and services, all of which must be achieved while minimizing the bandwidth used and the power consumed. The bandwidth restriction has led to the use of spectrally efficient digital modulation schemes such as quadrature amplitude modulation (QAM) or quadrature phase shift keying (QPSK). These modulation techniques in turn place restrictions on the performance of the supporting hardware. In particular, the linear output range of the power amplifier stage must be increased to transmit the signals with reduced distortion.

Increasing the linearity of the power amplifier has traditionally been achieved at the expense of wasted power. For instance, a mildly non-linear Class A amplifier operated well below the 1 dB compression point will not generate significant distortion, but at the same time waste over half of the battery input power. Wasted power means less talk time for the user with a battery powered device. What is needed is an amplifier that provides the required linearity while maintaining an acceptably high power efficiency.

1.2. High Efficiency Amplifiers and Linearization Techniques

Amplifiers which possess theoretical power efficiencies of 100% do exist. Unfortunately this highly desirable characteristic comes bound with the undesirable characteristic of a highly non-linear transfer function. The amplifiers which fall under this category are denoted as Class D, E, F and S. These amplifiers are used in a "switched" mode to perform the operation of single pole and double pole switches. The currents and voltages through the devices are controlled by the drive signals and tuned output filters to ensure that a finite current and a finite voltage on the device output cannot occur simultaneously. Thus no power is dissipated in the active device.

Using these classes of amplifiers requires a linearization technique to reduce the distortion of the output signal to an acceptable level. Feed forward, feedback and predistortion are techniques that can be used to reduce the distortion of mildly non-linear amplifiers.

Feed forward techniques traditionally require two power amplifiers and high power combining devices. Feedback techniques offer a reduction of the distortion proportional to the loop gain but at the cost of reduced output gain.

Predistortion techniques require complex modulation circuitry and or Digital Signal Processing (DSP) to achieve a reduction in the distortion level.

For the strongly non-linear amplifiers only signal separation and recombination linearization techniques can be used to produce low distortion systems. These techniques offer reduced distortion with a simple open loop architecture.

The linearization technique chosen for implementation in this work is called Envelope Elimination and Restoration . This method makes use of input signals which possess both amplitude (envelope) and phase information. The envelope component of the input signal is amplified in a high efficiency modulator. The phase component is recombined with the envelope component in a second high efficiency amplifier. The result is an amplified replica of the input signal with very low distortion level. Not only is this technique suitable for use with cellular modulation schemes like $\pi/4$ DQPSK, it can also be used to efficiently amplify combined signals, such as exist in a cellular base station, with reduced power consumption and space requirements.

1.3. Thesis Outline

This thesis discusses the analysis, design and testing of an Envelope Elimination and Restoration amplifier system. Chapter Two provides an introduction of the types of high efficiency non-linear amplifiers which can be used to implement the EER system. Chapter Three reviews the linearization techniques used to date on non-linear amplifiers. Chapter Four details the analysis of the EER system, providing insight into the critical areas in the system which affect signal distortion reduction. Chapter Five presents the testing methods used to determine the performance of the EER system. Chapter Six

summarizes the experimental results and provides conclusions and recommended future work.

Chapter Two - High Efficiency Amplifiers

This chapter provides an overview of the types of high efficiency amplifiers available, as well as the types of distortion that they are susceptible to. It is intended that the introduction presented here will provide the reader with a basic understanding of the theoretical operation of these special amplifiers.

2.1. Classes of High Efficiency Amplifiers

There are numerous texts which provide in-depth information on the operation of linear and approximately linear power amplifiers. These systems are denoted by the classification of A, B, AB and C. These amplifiers possess the desirable trait of linear amplification of a signal, but at the cost of efficiency.

The less well known classes of amplifiers are denoted as D, E, F and S. These amplifiers possess the desirable trait of high efficiency at the cost of non-linear amplification. High efficiency is achieved by operating the active devices in a switching mode and reducing power dissipation. Tuned output filters are used to ensure that the output signal possesses only the fundamental frequencies present in the input signal.

2.1.1. Class D

The "Class D" amplifier was first discussed by P.J. Baxandall in 1959. Since that time they have been used successfully in high power AM transmitters and low power HF transmitters [2]. The amplifier system consists of a pair of transistors connected to a tuned output circuit. The switching action of the two transistors is complementary to one another, resulting in the two pole switch equivalent circuit shown in Figure 2.1.

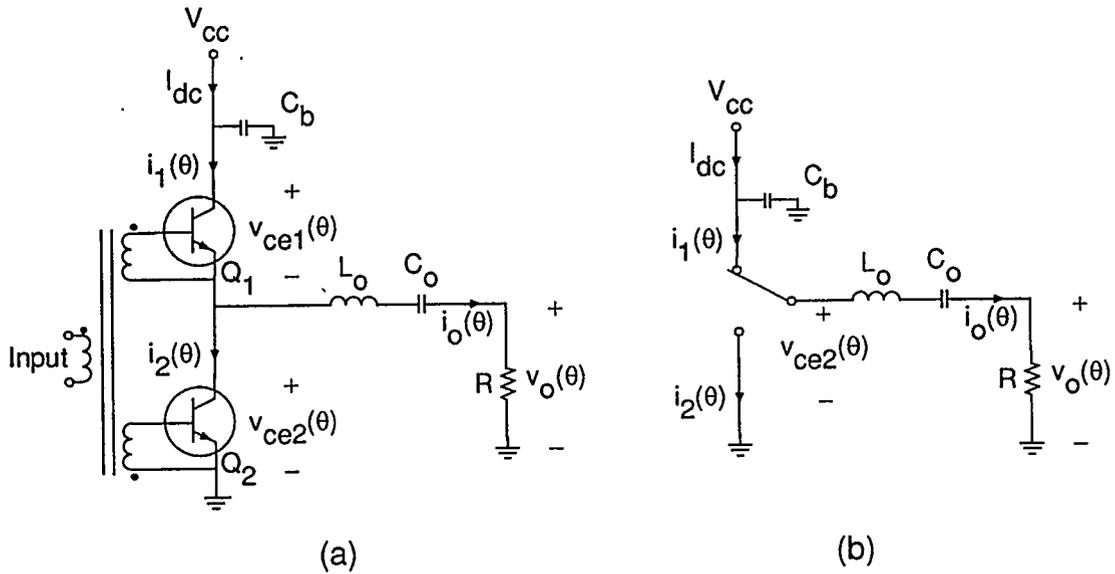


Figure 2.1 Complementary Voltage-Switching Class D PA (a) Schematic Circuit and (b) Equivalent Circuit

The purpose of the tuned output circuit is to provide a direct path to the load for the fundamental frequencies and to present a high impedance for all switching harmonics. The output of an ideal circuit is an amplified sinusoidal version of the input signal.

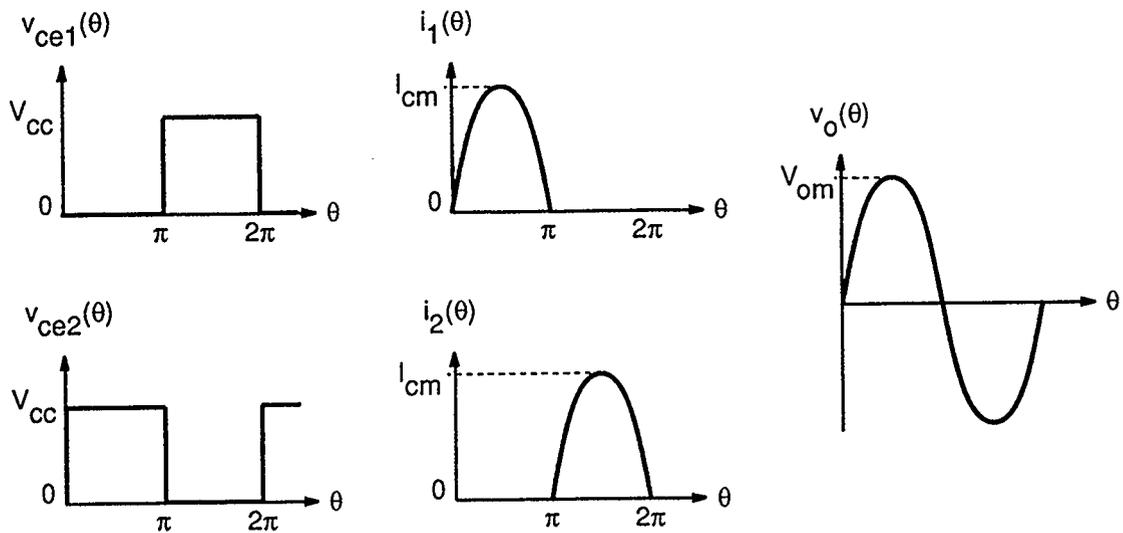


Figure 2.2 Complementary Voltage-Switching Class D PA waveforms

The ability of this amplifier to achieve an efficiency of 100% lies in the fact that when maximum current is being drawn through a transistor the voltage across the transistor is zero, as can be seen in Figure 2.2. Thus all of the dc power is delivered to the load and no power is dissipated in the transistors. Assuming that the input has a 50% duty cycle the voltage across Q_2 is:

$$v_{c2}(\theta) = V_{cc} \left[\frac{1}{2} + \frac{1}{2} s(\theta) \right] \quad (2.1)$$

Where the square wave form is defined by the Fourier series:

$$s(\theta) = \frac{4}{\pi} \left(\sin\theta + \frac{1}{3} \sin 3\theta + \frac{1}{5} \sin 5\theta \dots \right) \quad (2.2)$$

Due to the removal of the dc and harmonic components by the tuned output filter the current presented to the load resistor is:

$$i_o(\theta) = \frac{2V_{cc}}{\pi R} \sin\theta \quad (2.3)$$

This output current flows alternately through Q_1 and Q_2 , whichever is on. Therefore the output currents through the transistors are half sinusoids with a maximum current (I_{cm}) equal to $2V_{cc}/\pi R$. The dc input current is the average value of $i_1(\theta)$:

$$I_{dc} = \frac{I_{cm}}{\pi} = \frac{2}{\pi^2} \frac{V_{cc}}{R} \quad (2.4)$$

This current is used to determine the collector input power:

$$P_i = V_{cc} I_{dc} = \frac{2}{\pi^2} \frac{V_{cc}^2}{R} \quad (2.5)$$

The rms output power delivered to the load is derived from the maximum voltage at the output:

$$P_0 = \frac{V_{om}^2}{2R} = \frac{2}{\pi^2} \frac{V_{cc}^2}{R} \quad (2.6)$$

If it is assumed that the amplifiers have very large current gain values, the input power required to execute the switching action is negligible. The collector efficiency of the circuit is therefore defined from equations (2.5) and (2.6) to be 100%. In reality the Class D amplifiers do not achieve 100% efficiency. This reduction in the efficiency is caused by factors such as finite on resistance of the transistors, charge storage in the transistors which requires discharging at the beginning of the following half cycle, and finite switching times. Even with these practical limitations Class D amplifiers have been built that deliver efficiencies in excess of 90% [3].

2.1.2. Class E

The “Class E” amplifier was first introduced by Nathan and Alan Sokal in 1975 [4]. The main components of the system are: 1) switching transistor 2) RF choke 3) voltage invariant shunt capacitor and 4) tuned output filter.

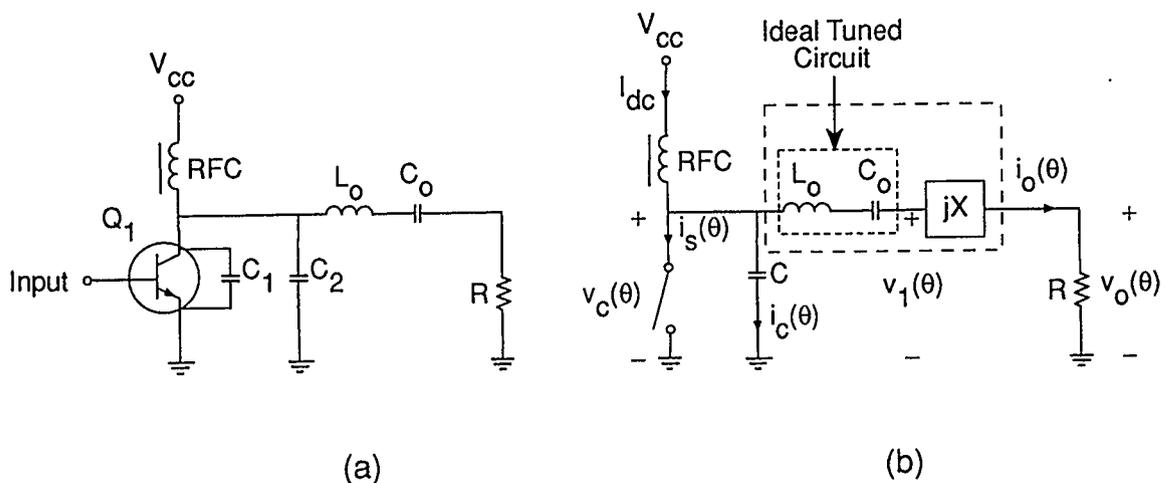


Figure 2.3 Class E PA (a) Schematic Circuit and (b) Equivalent Circuit

The shunt capacitance C is composed of the inherent transistor capacitance and an externally added capacitance C_2 , chosen to achieve amplifier performance. The simplest tuned output filter consists of a series inductor and capacitor combination. If the tuned filter is ideal it will serve as a block to all frequency components not at the fundamental frequency. The ideal filter is detuned by the reactance component X to achieve optimum performance.

The operation of the circuit may be analyzed if the following four assumptions are made:

- 1) The reactance of the RFC choke is sufficiently large as to ensure a constant dc current to the circuit.
- 2) The quality factor of the tuned output filter is sufficiently high as to ensure a sinusoidal output signal at the fundamental frequency.
- 3) The shunt capacitance does not vary with the applied voltage across it.
- 4) The transistor is acting like an ideal switch.

With these assumptions in mind the operation of the circuit proceeds as follows:

- 1) The input signal to the amplifier is a sinusoid or square wave at a fundamental frequency f_0 .
- 2) When the switch first opens, a charging current, $i_c(\theta) = I_{dc} - i_o(\theta)$, flows into the shunt capacitor. Since the switch is open no current is flowing through it (refer to Figure 2.4c). The collector voltage waveform is a result of this charging current into the shunt capacitor C . The peak collector voltage of approximately $3.6 V_{cc}$ is due to the presence of the tuned circuit and will vary slightly depending on the quality factor of the tuned circuit (refer to Figure 2.4b). If the switch were to remain open at this time the collector voltage would continue as an under-damped sinusoid with a final value of V_{cc} .

- 3) When the under damped collector voltage reaches the first minimum value (i.e. the point where $v_c = 0$ and $\delta v_c / \delta t = 0$) the switch is turned on (refer to Figure 2.4b at $\theta = \pi$). At this time any remaining charge in C is instantaneously removed and the current in the switch is the difference between the constant dc. current and the output current. Note that since the voltage across the switch is zero there is no power dissipation by the device.
- 4) The tuned circuit also acts to allow only the fundamental frequency sinusoid to reach the load while all other frequencies not at the fundamental are blocked. The resultant output is an amplified version of the incoming signal as shown in Figure 2.4 (d).

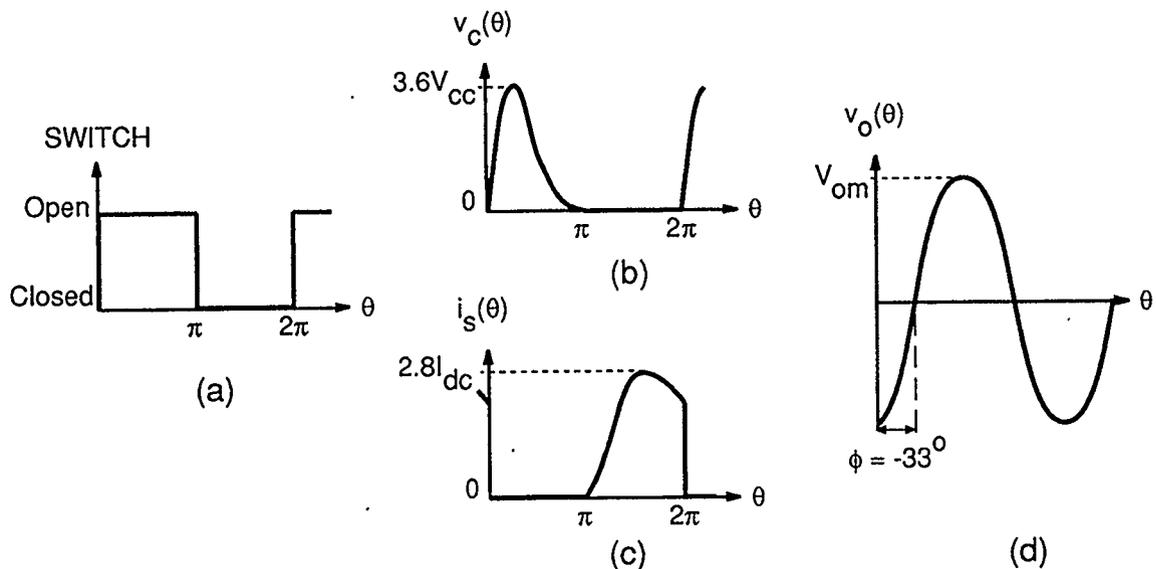


Figure 2.4 Class E Amplifier Waveforms (a) Switch timing (b) Voltage across the switch (c) Current through the switch (d) Output voltage at the load

Determination of the voltages and currents for the Class E amplifier is somewhat more difficult than those specified in the Class D design. However,

Krauss, Bostian and Raab [2] have shown that the collector voltage can be defined as:

$$v_c(\theta) = \left[\frac{I_{dc}}{B} \left(y - \frac{\pi}{2} \right) + \frac{V_{om}}{BR} \sin(\phi - y) + \frac{I_{dc}}{B} \theta + \frac{V_{om}}{BR} \cos(\theta + \phi) \right] \quad (2.7)$$

Where B is the susceptance of the shunt capacitance C at the frequency of operation, y is the switch off time (converted to radians) and ϕ is the phase angle between the output and input sinusoids.

In order to achieve an optimum design, specific values for B and X must be chosen. To determine these values it is necessary to set (2.7) and its derivative with respect to θ equal to zero at $\theta = \pi/2 + y$. This yields $\phi = -32.5^\circ$, $B = 0.1836/R$ and $X = 1.152R$. The output voltage and power can then be defined as:

$$V_{om} = \frac{2}{\sqrt{1 + \frac{\pi^2}{4}}} V_{cc} \approx 1.074 V_{cc} \quad (2.8)$$

$$P_o = \frac{2}{1 + \frac{\pi^2}{4}} \frac{V_{cc}^2}{R} \approx 0.577 \frac{V_{cc}^2}{R} \quad (2.9)$$

And the dc current is $I_{dc} = V_{cc} / 1.734R$. From the dc current and the output power defined in equation (2.9) it is possible to confirm that the theoretical collector efficiency is 100%. Practical Class E amplifiers suffer from finite saturation voltage and on resistance which reduce the efficiency from 100%. However, efficiencies of 96 % at frequencies of 3.9 MHz were reported by the Sokals in 1975. Since that time the frequency of operation has been pushed to 1 GHz with efficiencies approaching 72 % by Everard and Wilkinson [5].

Although the analysis performed by Krauss, Bostian and Raab assumed a constant dc current and a very high quality factor for the tuned output filter, recent papers have provided analysis and design details which do not make these assumptions. Avratoglou and Voulgaris [6] provide an analysis which compensates for finite quality factor in the tuned output filter. Smith and Zulinski [7] provide an analysis which accounts for finite RFC inductance and, Everard and King [8] provide details that allow design of a broad band output filter. These references provide complete information for Class E designs.

2.1.3. Class F

The “Class F” amplifier is probably the oldest high efficiency amplifier [9]. This amplifier is also known by the names “biharmonic”, “polyharmonic” and “multiresonator”. This design is characterized by load networks that have resonance at one or more harmonic frequencies. The design shown in Figure 2.5 is classified as a third-harmonic peaking amplifier.

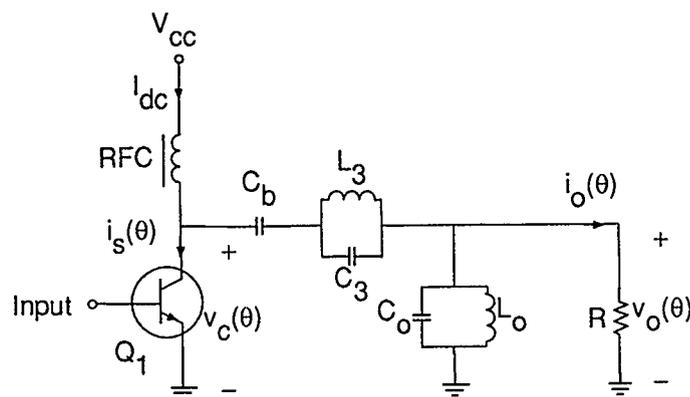


Figure 2.5 Third Harmonic Peaking Class F PA Schematic Circuit

The active device is driven by the input signal to act like a saturating current source during half of the wave form cycle. The 3rd order harmonic resonator is composed of L_3 and C_3 . The purpose is to achieve a match at the

fundamental frequency and resonate at the third harmonic of the fundamental frequency. The resonator action causes the dc, fundamental and 3rd order voltage components to be present at the collector of the transistor. By designing the resonator to apply the proper phase and magnitude of the third order component a voltage wave form similar to that shown in Figure 2.6 is achieved.

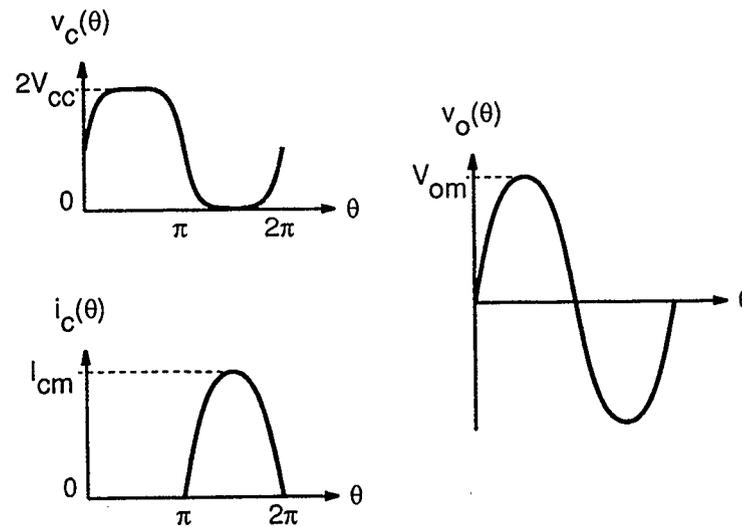


Figure 2.6 Third Harmonic Peaking Class F PA wave forms

The second tuned circuit composed of L_o and C_o provides a path to ground for all frequencies not at the fundamental frequency. This filter acts to shape the collector current through the application of the even order current components. The filter also ensures that the output wave form is a sinusoid at the fundamental frequency.

The analysis of this amplifier requires two assumptions: 1) the amplitude and phase of the third harmonic voltage can be set to appropriate values and 2) the half sine wave collector current and the second tuned circuit produces a sinusoidal output voltage at the fundamental frequency. Using assumption one, the collector voltage can be written as:

$$v_c(\theta) = V_{cc} + V_{om} \sin\theta + V_{cm3} \sin 3\theta \quad (2.10)$$

Krauss, Bostian and Raab chose a value for V_{cm3} of $V_{om}/9$ to achieve maximum flatness of the collector voltage. The value of V_{om} can be easily evaluated by noting that the collector voltage wave form is zero at $\theta = 3\pi/2$.

$$V_{om} = \frac{9}{8} V_{cc} \quad (2.11)$$

The output power can be written as:

$$P_o = \frac{V_{om}^2}{2R} = \left(\frac{9}{8}\right)^2 \frac{V_{cc}^2}{2R} \quad (2.12)$$

The dc current is the average of the half sinusoidal collector current, $I_{dc} = I_{cm}/\pi$. Where the maximum collector current is defined as:

$$I_{cm} = \frac{2V_{om}}{R} \quad (2.13)$$

The dc input power can be evaluated as:

$$P_i = I_{dc} V_{cc} = \left(\frac{9}{8}\right) \frac{2V_{cc}^2}{\pi R} \quad (2.14)$$

Using equations 2.12 and 2.14 to calculate the collector efficiency yields a maximum theoretical efficiency of 88.4 %. Nojima, Nishiki and Chiba [10] have reported a power added efficiency of 75% for a 1.7 GHz, 3W design.

2.1.4. Class S

The Class S technique was invented in 1932 by B.D. Bedford [11]. The modern design incorporates a switching transistor and tuned output filter as in the Class D and E systems. Unlike these other systems, the input signal is modulated using pulse width modulation techniques. The Class S design has

only recently received popular review. The change in attitude towards this technique is due to the increase of inexpensive integrated circuits required for the implementation.

The technique is suitable for both amplification and modulation. For this reason the Class S modulator was chosen as a promising design to provide modulated power to a second high efficiency amplifier (refer to section 3.2 "Envelope Elimination and Restoration"). Since a modulator is only required to provide positive voltage to the load, a single transistor and diode are sufficient.

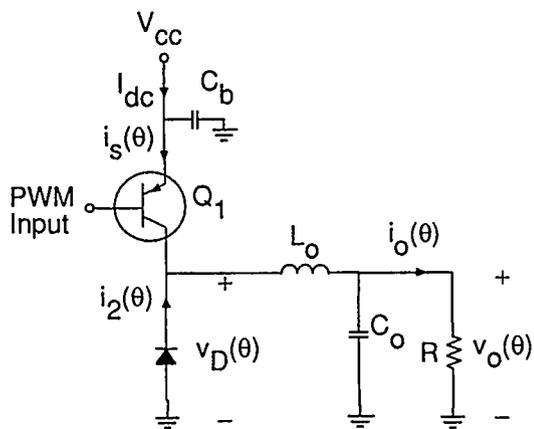


Figure 2.7 Class S Modulator Schematic

The transistor acts as a single pole switch. The switch replicates the incoming PWM pulses, alternately connecting and disconnecting the lowpass output filter, formed by L_o and C_o , to the power supply.

The lowpass filter acts as an averaging stage, smoothing out the transitions and provides a slowly varying current to the load. Different pulse widths produce different average output values. During the times when the switch is "off", the inductor of the low pass filter will continue to draw current up through the diode (refer to Figure 2.8). To minimize current drooping during the off periods a multiple stage filter can be used, however, it is necessary to make

the first component an inductor to ensure that a high impedance is presented to the switch.

The result is an efficiently amplified replica of the input envelope.

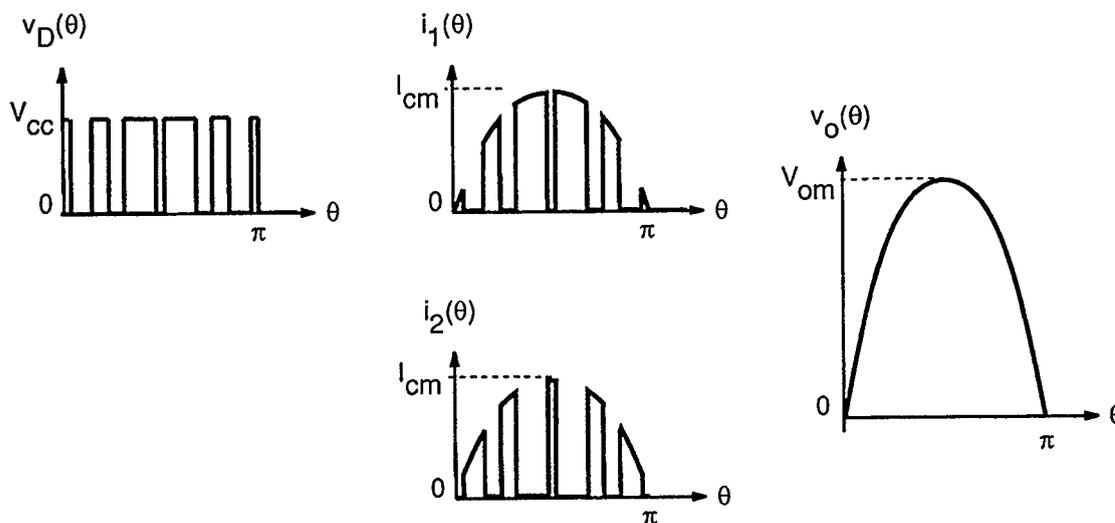


Figure 2.8 Class S Switching Wave forms

The output voltage of the modulator can have any value between 0 and V_{cc} . Consequently the output power is:

$$P_o \leq \frac{V_{cc}^2}{R} \quad (2.15)$$

The active device never experiences non-zero voltage and non-zero current at the same time. As a result, the Class S modulator has a theoretical efficiency of 100 %. Practical Class S modulators providing 100 W of power at frequencies above 57 kHz while still maintaining efficiencies in excess of 90 % have been built [12].

2.2. Amplifier Distortion

A linear amplifier derives its name from the mathematical concept of linearity. Thus a linear amplifier's output will be a scaled and time delayed version of the input. A non-linear amplifier may cause distortion in the output signal by modification of the amplitude and or time delay information. These modifications result in output power compression, phase distortion and excess frequency terms known as intermodulation and harmonic distortion products. The Class S amplifier also suffers from distortion due to the sampling of the input waveform known as PWM distortion.

2.2.1. Amplitude Distortion

The most common non-linearity characterization of a system is amplitude distortion. Assuming that the output voltage is an instantaneous function of the input voltage and the non-linearity is weak, then the output voltage $v_o(t)$ can be related to the input voltage $v_i(t)$ by a simple power series:

$$v_o(t) = k_1 v_i(t) + k_2 v_i(t)^2 + k_3 v_i(t)^3 \quad (2.16)$$

If a single tone, $v_i(t) = A \cos \omega_1 t$ is applied to a device whose output voltage is described by equation 2.16 then the output voltage becomes:

$$v_o(t) = \frac{1}{2} k_2 A^2 + \left(k_1 A + \frac{3}{4} k_3 A^3 \right) \cos \omega_1 t + \frac{1}{2} k_2 A^2 \cos 2\omega_1 t + \frac{1}{4} k_3 A^3 \cos 3\omega_1 t \quad (2.17)$$

The first term in equation 2.17 is the dc component of the output voltage. The second term represents the component of the output voltage at the fundamental frequency ω_1 . The third and fourth terms represent the components of the output voltage at the second and third harmonic frequencies respectively. The gain of the fundamental component can be written in the form:

$$k_1 A \left(1 + \frac{3}{4} \frac{k_3}{k_1} A^2 \right) \quad (2.18)$$

Thus the fundamental component gain will be greater than $k_1 A$ if $k_3 > 0$ and less than $k_1 A$ if $k_3 < 0$. This property is called the gain expansion or gain compression of the device. Most practical devices are gain compressive. An industry standard for the characterization of a device is the statement of the 1 dB compression point. This is the point on the power transfer characteristic where the output power has deviated from the linear transfer characteristic by 1 dB (refer to Figure 2.9).

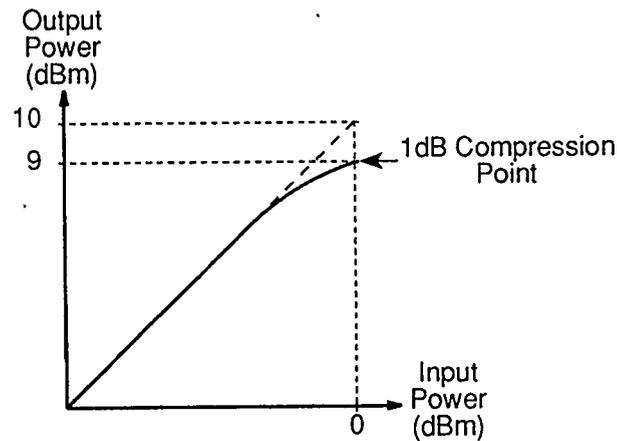


Figure 2.9 Definition of 1 dB Compression Point

A standard method for measuring the amount of AM distortion generated in a device is to apply an input signal that consists of two equal amplitude sinusoids separated in frequency. This test is called the “Two Tone” test. Applying the input signal $v_i(t) = A \cos \omega_1 t + A \cos \omega_2 t$ to the device transfer function defined by equation 2.16 will yield an output voltage as follows:

$$v_o(t) = k_2 A^2 + k_2 A^2 \cos(\omega_1 - \omega_2)t + \left(k_1 A + \frac{9}{4} k_3 A^3 \right) \cos \omega_1 t \\ + \left(k_1 A + \frac{9}{4} k_3 A^3 \right) \cos \omega_2 t + \frac{3}{4} k_3 A^2 \cos(2\omega_1 - \omega_2)t$$

$$\begin{aligned}
& + \frac{3}{4}k_3A^3 \cos(2\omega_2 - \omega_1)t + k_2A^2 \cos(\omega_1 + \omega_2)t + \frac{1}{2}k_2A^2 \cos 2\omega_1t \\
& + \frac{1}{2}k_2A^2 \cos 2\omega_2t + \frac{3}{4}k_3A^3 \cos(2\omega_1 + \omega_2)t + \frac{3}{4}k_3A^3 \cos(2\omega_2 + \omega_1)t \\
& + \frac{1}{4}k_3A^3 \cos 3\omega_1t + \frac{1}{4}k_3A^3 \cos 3\omega_2t
\end{aligned} \tag{2.19}$$

Figure 2.10 shows a graphical representation of equation 2.19.

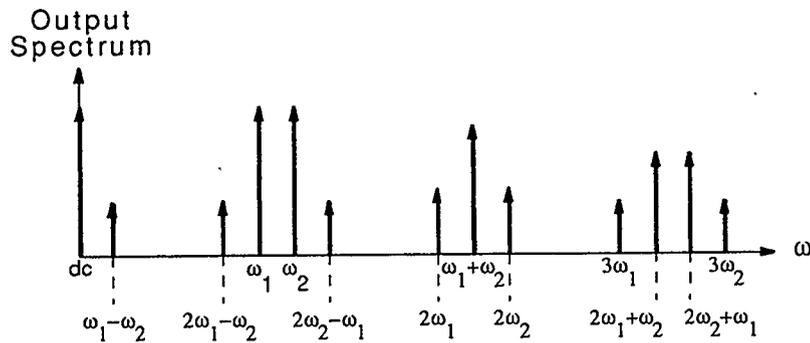


Figure 2.10 Output Spectrum of a device with two input sinusoids and third order distortion

The output signal consists of six different types of components. The first component occurs at dc followed by the fundamental frequency components ω_1 and ω_2 . The second and third harmonic components are located at frequencies $2\omega_1$, $2\omega_2$ and $3\omega_1$, $3\omega_2$. The second order intermodulation product components occur at frequencies of $\omega_1 \pm \omega_2$ (i.e. the sum of the coefficients of ω_1 and ω_2 is two). And finally the third order intermodulation product components occur at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$.

Practical systems are not concerned with the second and third harmonic components, and the second order intermodulation components. These components can be removed through appropriate filtering. However, the third order components fall within the pass band of the system and cannot be removed by filtering. This means that the system 3rd order intermodulation products

(IMD3s) must be reduced to as much as possible to reduce distortion in the output signal.

2.2.2. Phase Distortion

A phase distortion called AM to PM conversion occurs when the magnitude of the input signal can affect changes in the phase of the output signal. The AM to PM conversion is defined as the change in output phase for a 1 dB increment of output power. Phase distortion also generates IMD products that are similar in nature to amplitude distortion. Thus the reduction of these products will also ensure reduction of phase distortion.

2.2.3. Pulse Width Modulation Distortion

The PWM technique used to create the input signal for a Class S amplifier contributes a different type of distortion than the previously discussed Amplitude and Phase distortion. The PWM is in effect sampling the input wave form. The result of this sampling is additional spurious components as shown in Figure 2.11.

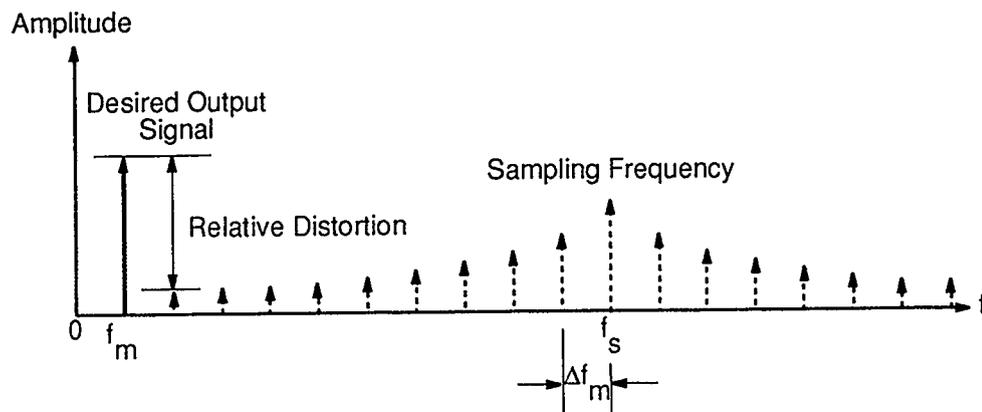


Figure 2.11 Spectral Response of a PWM Signal

Raab has shown that if the input is a single sinusoid with amplitude $V_{om} \leq V_{cc}$, then the magnitude of the n th spurious product associated with the k th harmonic of the switching frequency is given by:

$$|V_{k,n}| = \frac{2V_{cc}}{k\pi} J_n \left(k\pi \frac{V_{om}}{V_{cc}} \right) \quad (2.20)$$

where: J_n is a Bessel function of the first kind of order n

Those spurious products which fall within the pass band of the amplified signal will cause distortion. It is therefore necessary to choose a sampling frequency that is suitably high as to reduce the distortion to an acceptable level. For an amplifier with a distortion level due to PWM of -40 dBc it is necessary to choose a sampling frequency at least 5 times the highest frequency in the input signal.

The most demanding input signal, in terms of frequency bandwidth, that the Class S modulator must amplify is the envelope signal shown in Figure 2.12.

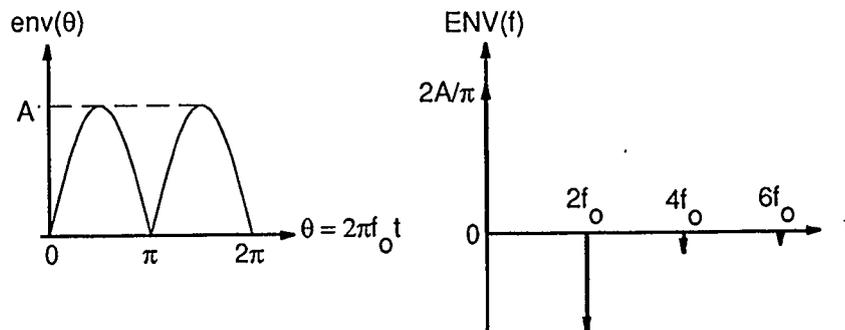


Figure 2.12 Envelope Signal and Corresponding Frequency Spectrum

Raab and Rupp have determined that if the envelope spectrum is sampled at 10 times the fundamental frequency then the distortion level is below -40 dBc.

Chapter Three - Highly Non-Linear Amplifier Linearization Techniques

This chapter provides an overview of the types of linearization techniques available. It is intended that the brief introduction presented here will provide the reader with a general understanding of the number of different types of linearization techniques available. For an in-depth handling of these techniques the reader should study the references quoted. The main portion of this chapter will deal with two linearization techniques tailored to highly non-linear amplifiers.

There have been many methods proposed for the purpose of amplifier linearization. These techniques can be grouped according to the following characteristics: 1) feedforward, 2) feedback, 3) predistortion and 4) signal separation and recombination.

The earliest methods include the use of feedforward structures, first proposed in the 1920's by Harold S. Black. A feedforward structure uses a cancellation signal at the output of the system. The cancellation signal, which contains only the distortion products, is subtracted from the amplifier output signal. A simplified block diagram of a feed forward system is shown in Figure 3.1.

Generation of the cancellation signal can be achieved through the use of a network of delay lines, couplers, attenuators and auxiliary amplifiers. Due to the complex circuitry involved, feed forward techniques were generally restricted to larger systems.

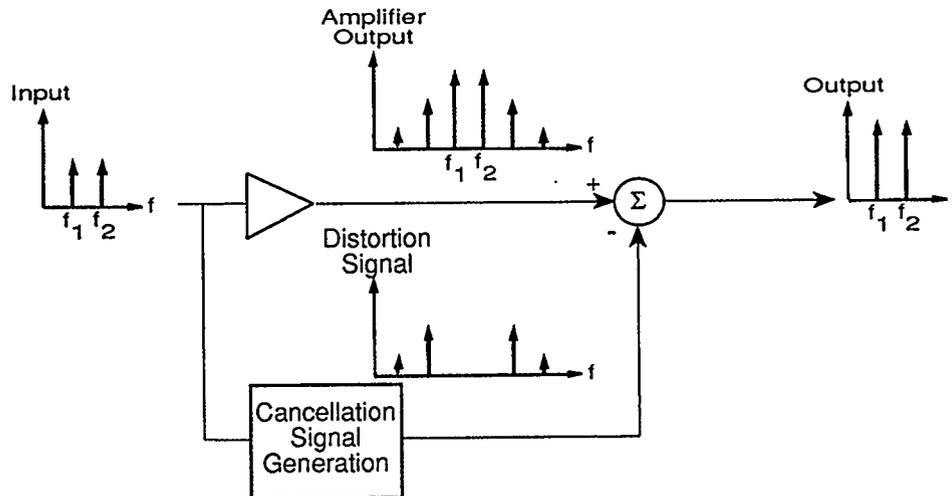


Figure 3.1 Simplified FeedForward System

Feedback techniques, on the other hand, are characterized by the fact that they use the sampled output of the amplifier, subtracted from the original input signal to achieve reduction of the intermodulation distortion products. A simplified feedback system is shown in Figure 3.2.

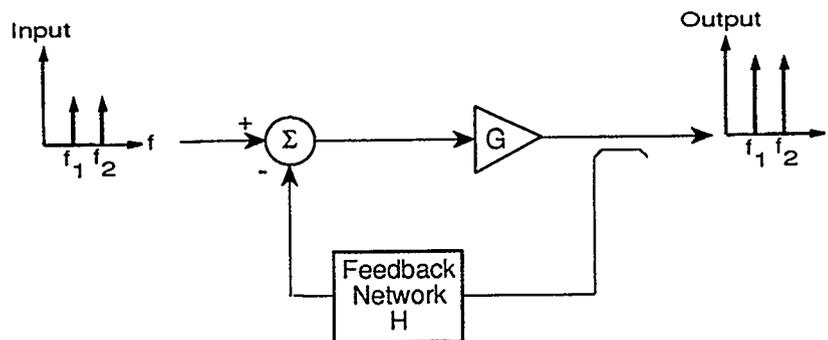


Figure 3.2 Simplified Feedback System

The system shown in Figure 3.2 is best known as the passive RF Negative Feedback technique [13]. For this technique the intermodulation products are reduced by the loop gain $1/(1+GH)$.

A modification of this system using an active element in the feedback path is known as Active Feedback Linearization [14]. The active feedback system has the advantage of providing a larger dynamic range.

Reduction of the amplifier's intermodulation products can also be achieved through the negative feedback of the intermodulation products only [15]. This system has the advantage of distortion reduction without loss of active gain.

The last feedback system, to be mentioned here, compares the input and output envelope components to produce an error signal [16]. This feedback system will be described in detail as part of the system enhancements later in this chapter.

A common design difficulty of all feedback systems is the delay encountered in the feedback path. This delay places restrictions on the maximum frequency at which the system will remain stable. The design of the feedback system requires that the gain must be less than one at frequencies where oscillation may occur. As the frequency of operation and the bandwidth is increased the design for stable operation becomes more and more difficult.

Another method of reducing distortion uses the technique of modifying the input signal and is appropriately called "predistortion" linearization [17]. These techniques are similar in nature to the feedforward technique in that they use signal cancellation to reduce the unwanted distortion in the output signal.

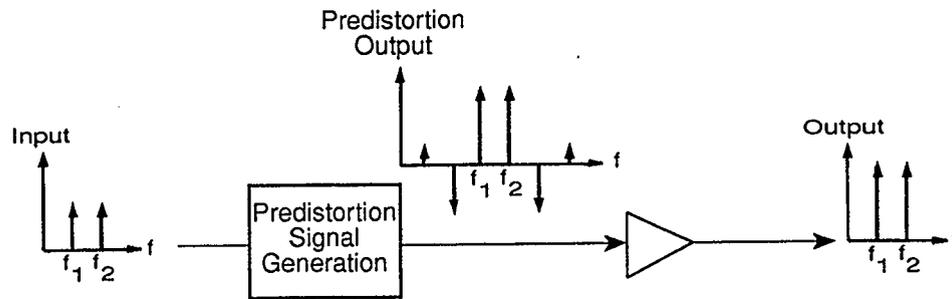


Figure 3.3 Simplified Predistortion System

Generation of the predistortion signal requires an understanding of the non-linearities in the amplifier. The rf cuber predistortion system [18] adjusts the phase and amplitude of the input signal to the amplifier to achieve the reduction in the intermodulation products. The adaptive complex gain predistortion system [19] uses information sampled at the output of the amplifier to continuously modify the predistortion signal.

Although all of the previously mentioned methods have the ability to reduce the distortion generated by mildly non-linear amplifiers, there are two methods which are specifically designed to reduce the distortion generated by highly non-linear amplifiers. The remainder of this chapter will focus on these two techniques.

3.1. Linear Amplification using Non-Linear Components

The LINC system (Linear Amplification using Non-Linear Components) is fundamentally different from the previously mentioned linearization methods in that there is no feedback used and the amplifier itself can be highly non-linear. The LINC technique was originally called "Outphasing". These systems were first developed during the 1930's by H. Chireix [20] to improve the efficiency and linearity of AM-broadcast transmitters.

3.1.1. Simple System

The basic principle for the LINC system is to separate the baseband input signal, which contains either or both amplitude and phase information, into two constant amplitude signals. These two constant amplitude signals can be separately amplified by a pair of highly non-linear amplifiers. The amplified component signals are passively re-combined to produce an amplified replica of the input signal. A block diagram of a simple LINC system is shown in Figure 3.4.

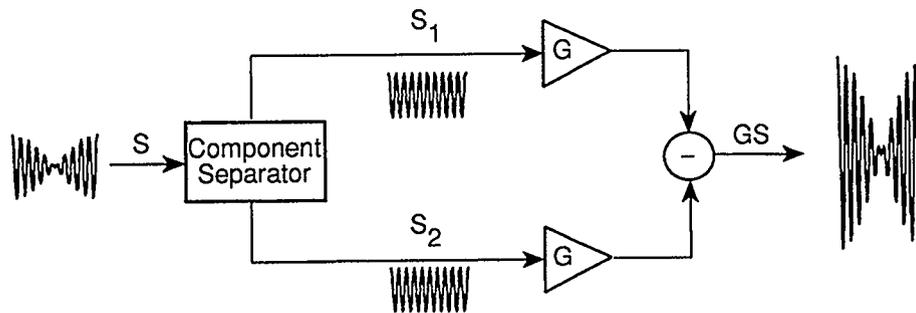


Figure 3.4 Simple Linc System

To gain a basic understanding of the system operation, consider first the input signal.

$$S(t) = E(t) \cos \omega_0 t \quad (3.1)$$

where: $E(t) = E_m \sin \phi t$ and is defined as the envelope

E_m is the maximum value of the envelope

The component separator produces the two constant amplitude signals S_1 and S_2 which are related to the input signal as follows:

$$S(t) = S_1(t) - S_2(t)$$

$$S(t) = \frac{E_m}{2} \{ \sin[\omega_0 t + \phi(t)] - \sin[\omega_0 t - \phi(t)] \} \quad (3.2)$$

where: $S_1(t) = \frac{E_m}{2} \sin[\omega_0 t + \phi(t)] \quad (3.3)$

$$S_2(t) = \frac{E_m}{2} \sin[\omega_0 t - \phi(t)] \quad (3.4)$$

The output is generated after amplification of the two constant amplitude signals and recombination.

$$GS_1(t) - GS_2(t) = GE_m \sin\phi(t) \cos\omega_0 t = GS(t) \quad (3.5)$$

The ideal operation of the system, although straight forward theoretically, is difficult to achieve in a practical system. To ensure stable operation the maximum phase deviation, $\phi(t)$, must remain $\leq \frac{\pi}{2}$. This requirement restricts the implementation of the system to modulation schemes such as full carrier amplitude modulation and amplitude shift keying.

The performance of the system is also affected by the degree of match between the two amplifiers. Suppression of broad band phase modulation components at the combiner relies on a very tight tolerance on the gain and phase match in the two amplifier paths (0.01 dB gain error and 0.1° phase error will give a component suppression of only 54 dB) [21]. An early implementation of the simple LINC system demonstrated an IMD level 22 dB below the fundamentals.

The efficiency of the simple LINC system also suffers due to combining the output signals. Since the two amplifier output signals are time varying, the action at the combiner will result in an output signal which undergoes periods of maximum signal and minimum signal. These variations in the output signal

correspond to a time-varying load impedance. The effects of an impedance variation on the system efficiency differ for varying types of power amplifiers. Therefore the efficiency characteristics of a LINC system also depend on the type of power amplifier used. Raab [22] has shown that the instantaneous efficiency of a simple LINC system using class B amplifiers varies linearly with the ratio of the maximum output voltage to the supply voltage.

$$\eta = \frac{P_0}{P_{dc}} = \frac{\pi}{4} \frac{V_{om}}{V_{DD}} \quad (3.6)$$

A simple LINC system is quite satisfactory for a class D power amplifier whose efficiency remains high regardless of the load impedance. For systems which utilize a load sensitive power amplifier, the Chireix system described below is recommended.

3.1.2. Chireix System

The Chireix system adds transmission-line couplers and shunt reactances (refer to Figure 3.5) to reduce the effects that varying load impedances have on the system efficiency .

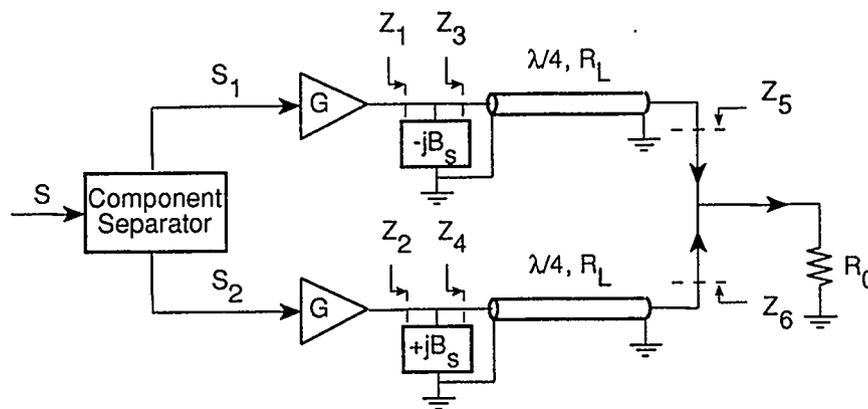


Figure 3.5 Chireix LINC System

Raab [22] has shown that the impedance looking into the load are described by the following equations:

$$Z_5 = 2R_o \frac{V_o}{V_{om}} (\sin \phi + j \cos \phi) \quad (3.7)$$

$$Z_6 = 2R_o \frac{V_o}{V_{om}} (\sin \phi - j \cos \phi) \quad (3.8)$$

The quarter wavelength transmission lines transform the impedance towards the amplifiers according to the formula,

$$Z_3 Z_5 = R_L^2. \quad (3.9)$$

The admittance at the input to the transmission lines can be identified as

$$Y_3 = \frac{Z_5}{R_L^2} = \frac{2R_o}{R_L^2} \frac{V_o}{V_{om}} (\sin \phi + j \cos \phi) \quad (3.10)$$

$$Y_4 = \frac{Z_6}{R_L^2} = \frac{2R_o}{R_L^2} \frac{V_o}{V_{om}} (\sin \phi - j \cos \phi) \quad (3.11)$$

where: V_o is the output voltage at the load resistor and

V_{om} is the maximum value of the output voltage.

Figure 3.6 shows the magnitude, and the real and imaginary parts of the admittance at the drain of the amplifiers when no shunt admittance is present (i.e. $B_s = 0$). From this information it is clearly evident that the amplifier load impedance increases towards infinity as the system output decreases to zero.

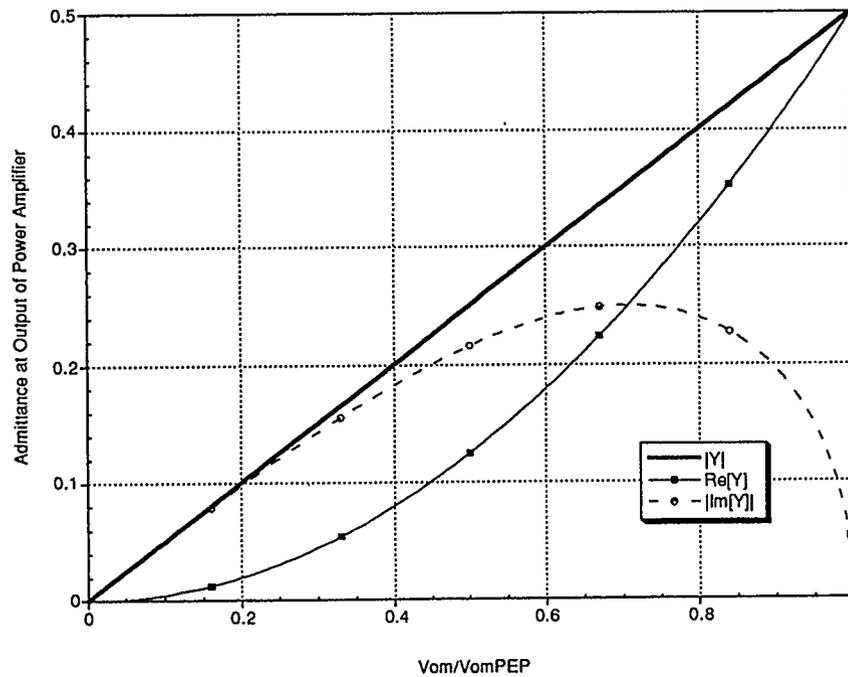


Figure 3.6 Admittance at Output of Power Amplifiers with $B_s = 0$,
Normalization: $R_0 = 1$, $R_L = 2$.

It is also evident from Figure 3.6 that the amplifiers are driving highly reactive loads over the majority of the output signal swing. The influence of the reactive loads upon the system can be partially controlled by the introduction of the shunt reactances $-B_s$ and $+B_s$. The admittance at the output of the amplifiers is now defined as:

$$Y_1 = Y_3 - jB_s = G_1 + jB_1 \quad (3.12)$$

$$Y_2 = Y_4 - jB_s = G_1 - jB_1 \quad (3.13)$$

The conductance and susceptance terms in equations 3.12 and 3.13 are defined as:

$$G_1 = \frac{2R_0}{R_L^2} \frac{V_o}{V_{om}} \sin \phi = \frac{2R_0}{R_L^2} \left(\frac{V_o}{V_{om}} \right)^2 \quad (3.14)$$

$$B_1 = \frac{2R_0}{R_L^2} \left(\frac{V_o}{V_{om}} \sqrt{1 - \left(\frac{V_o}{V_{om}} \right)^2} - B_s' \right) \quad (3.15)$$

where: B_s' is the normalized shunt admittance

$$B_s' = \frac{R_L}{2R_0} B_s \quad (3.16)$$

Examining equation 3.15 reveals that the susceptance loading the power amplifier can be reduced to zero for one particular output amplitude by setting the value of B_s' .

$$B_s' = \frac{V_o}{V_{om}} \sqrt{1 - \left(\frac{V_o}{V_{om}} \right)^2} \quad (3.17)$$

The effect the shunt admittance has upon the efficiency of the system is demonstrated in Figure 3.7. This graph clearly indicates that it is possible to tune the system efficiency to a maximum at one specific amplitude output. Figure 3.7 also indicates that for a value of $B_s' = 0$ the system efficiency is the same as the efficiency of the power amplifier, which in this case is Class B.

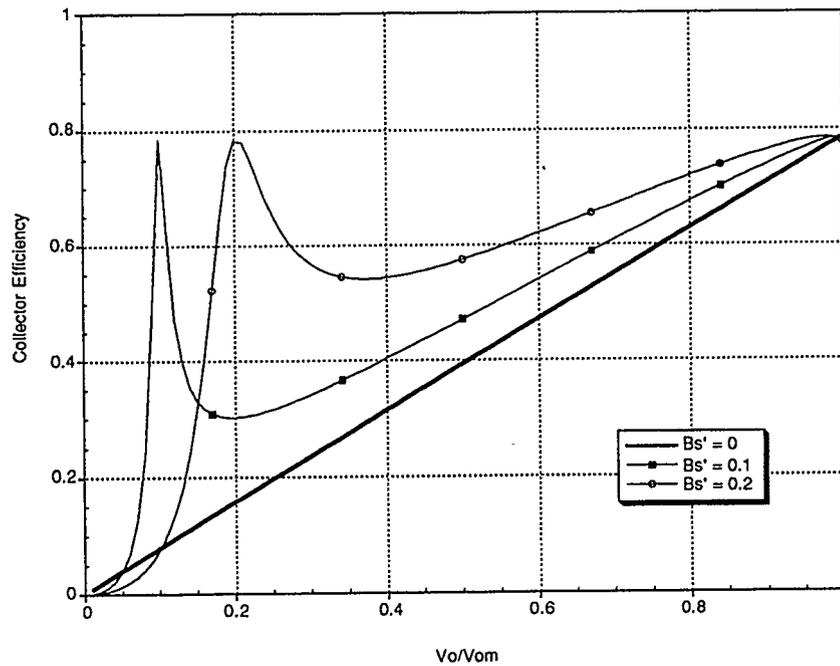


Figure 3.7 Efficiency of Chireix LINC System with Bs' at Various Values, Normalization: $R_o = 1, R_L = 1$

A recent implementation, by Bateman, of a 160 MHz LINC system demonstrated intermodulation suppression in excess of 55 dB. A disadvantage of the LINC system lies in the construction of the “component separator”. Bateman’s system [21] required the construction of a DSP which contained dual Phase Locked Loops (PLL) and a switching matrix to ensure stable operation.

The next section will deal with a linearization system which, until very recently, has not received much attention.

3.2. Envelope Elimination and Restoration

The envelope elimination and restoration (EER) system shares a common bond with the LINC system in that it relies on the separation and recombination of signals. The technique lends itself well to the use of highly non-linear amplifiers. The EER technique was originally designed by L. R. Kahn during the 1950's [23]. The first practical system using EER was a 100 kW AM transmitter which, at the time, was the most powerful single-sideband transmitter in operation.

3.2.1. Basic System

The basic principle for the EER system is to separate the baseband input signal, which contains both amplitude and phase information, into a phase only component and envelope only component. The phase signal is used to initiate the switching action of the highly non-linear main power amplifier. The amplified envelope component is used to control the power output from the main power amplifier. The active recombination of the phase and envelope signals in the main power amplifier generates an amplified replica of the input signal. A block diagram of a simple EER system is shown in Figure 3.8.

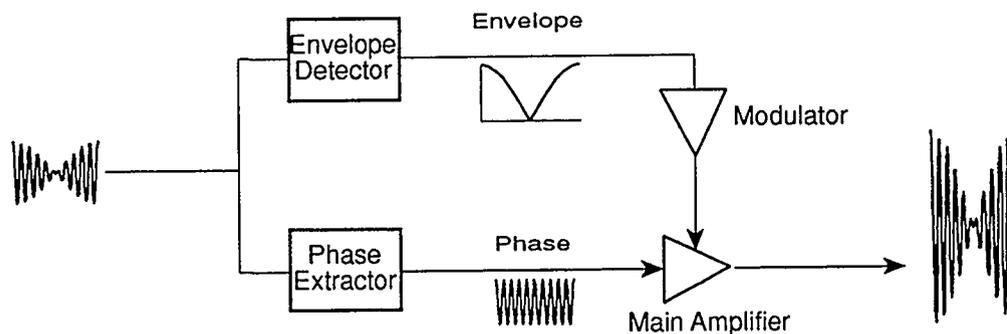


Figure 3.8 Basic Envelope Elimination and Restoration System

A detailed analysis of the EER system is reserved for Chapter Four. However, a simple discussion of the operation can be carried out here. Consider an input signal composed of the summation of two equal amplitude tones with frequencies ω_1 and ω_2 . The phasor diagram for the input signal is shown in Figure 3.9.

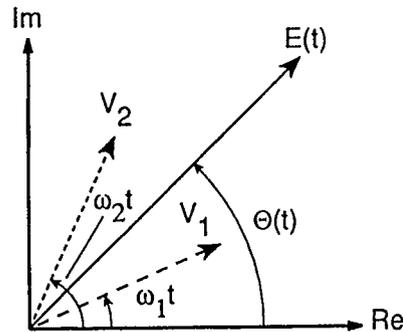


Figure 3.9 Phasor Diagram of Two Tone Input Signal

The envelope or magnitude component can be determined with the help of a few well known trigonometric identities to be.

$$E(t) = \sqrt{V_1^2 + V_2^2 + 2V_1V_2 \cos(\omega_2 - \omega_1)t} \quad (3.18)$$

For the case when both signals are of equal amplitude equation 3.19 reduces to:

$$E(t) = 2V \cos\left(\frac{\omega_2 - \omega_1}{2}t\right) = 2V \cos \omega_m t \quad (3.19)$$

where: $\omega_m = \frac{\omega_2 - \omega_1}{2} \equiv$ modulation frequency

Likewise, the phase component is written as:

$$\text{Phase}(t) = \sin\left[\omega_1 t + \tan^{-1}\left\{\frac{V_2 \sin(\omega_2 - \omega_1)t}{V_1 + V_2 \cos(\omega_2 - \omega_1)t}\right\}\right] \quad (3.20)$$

Equation 3.20 also reduces when the signals are of equal amplitude.

$$\text{Phase}(t) = \sin\left(\frac{\omega_1 + \omega_2}{2}\right)t = \sin\omega_o t \quad (3.21)$$

where: $\omega_o = \frac{\omega_2 + \omega_1}{2} \equiv$ phase frequency

The modulator and main amplifier apply a combined gain (G) only to the envelope component resulting in the overall output described below:

$$GE(t)\text{Phase}(t) = G(2V \cos\omega_m t)\sin\omega_o t = G(V_1 \sin\omega_1 t + V_2 \sin\omega_2 t) \quad (3.22)$$

The advantages of the EER system are listed below:

- 1) Implementation of the Phase Extractor is much simpler than the Component Separator required by the LINC system. In fact, the Phase Extractor is basically a hard limiter. The only criteria for the limiter is the minimization of amplitude modulation to phase modulation conversion.
- 2) The EER system is unconditionally stable.
- 3) The loads seen by the main power amplifier and by the modulator are not time variant, this allows the simple design of power matching circuits to be performed.
- 4) There is no requirement that the modulator and main power amplifier be matched as in the LINC system. The main criteria for the main amplifier and modulator is that together they linearly amplify the envelope component of the input signals. The main amplifier response to power supply variation is known as the "Amplitude Modulation Characteristic" of the device. Note that this requirement does not mean that a linear amplifier is required for the main power amplifier, Chapter Four will explain how a Class E amplifier is ideally suited for amplitude modulation.

- 5) Use of a Class S Modulator with a Class D, E or F main amplifier results in a system efficiency that remains high over a large range of input signal levels.

3.2.2. Enhanced System

The EER system lends itself to a modification which can improve the distortion reduction performance even if the main amplifier has a non-linear amplitude modulation characteristic. The modification used is “Envelope Feedback”. The implementation of envelope feedback requires a modest increase in circuit complexity as shown in Figure 3.10.

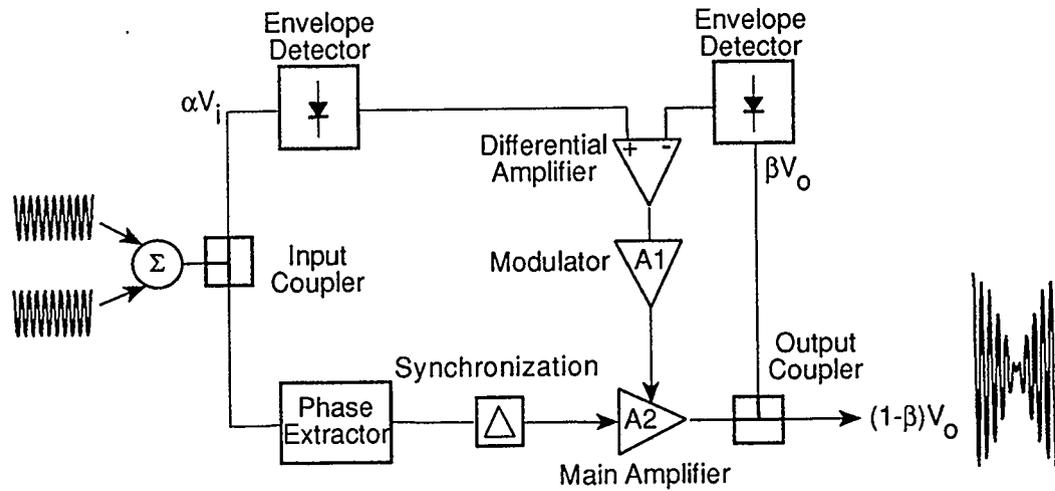


Figure 3.10 Envelope Elimination and Restoration System with Envelope Feedback

Arthanayake and Wood [16] have shown that the circuit gain (i.e. envelope gain) with envelope feedback can be defined as:

$$G = \frac{(1-\beta)A_2(A_1 + \alpha\eta\gamma V_i)}{(1 + A_2\beta\eta\gamma V_i)} \quad (3.23)$$

where: A_1 = gain of the modulator
 A_2 = amplitude modulation gain of the main amplifier

V_c = modulator control voltage from difference amplifier

V_i = input signal level

V_o = output signal level from main amplifier

γ = modulator sensitivity = dA_1/dV_c

α = input coupling factor

β = output coupling factor

η = rectification efficiency of detectors

If the modulator sensitivity is increased towards infinity equation 3.23 takes on a somewhat simpler appearance.

$$\lim_{\gamma \rightarrow \infty} G = (1 - \beta) \left(\frac{\alpha}{\beta} \right) \quad (3.24)$$

Equation 3.24 indicates that as sensitivity is increased the overall envelope gain becomes independent of the individual gains A_1 and A_2 . Thus the distortion products resulting from non-linear gains can be reduced. A reduction of the order of 30 dB was simulated for an EER system using envelope feedback and others have reported up to 35 dB reduction in intermodulation distortion using this technique.

Chapter Four - System Analysis

4.1. System Distortion

The distortion that input signals undergo as a result of passing through the Envelope Elimination and Restoration system is analyzed using a combination of the following techniques:

- 1) determination of the Fourier series of a periodic signal
- 2) modulation (multiplication) of two or more signals
- 3) transformation to and from the time domain and the frequency domain using a Discrete Fast Fourier Transform (DFFT) and the Inverse Discrete Fast Fourier Transform (IDFFT)
- 4) determination of the frequency response using filter theory.

The use of modulation theory and Fourier series techniques to predict the intermodulation distortion was first proposed by Kahn [23]. The analysis begins by describing the input signal in terms of its frequency spectrum. The effect upon the input spectra of the envelope detector and modulator that make up the envelope signal path and of the phase extractor in the phase signal path, is calculated. The total distortion effects are determined in the frequency domain when the distorted envelope and phase signals re-combine at the main amplifier (refer to Figure 4.1)

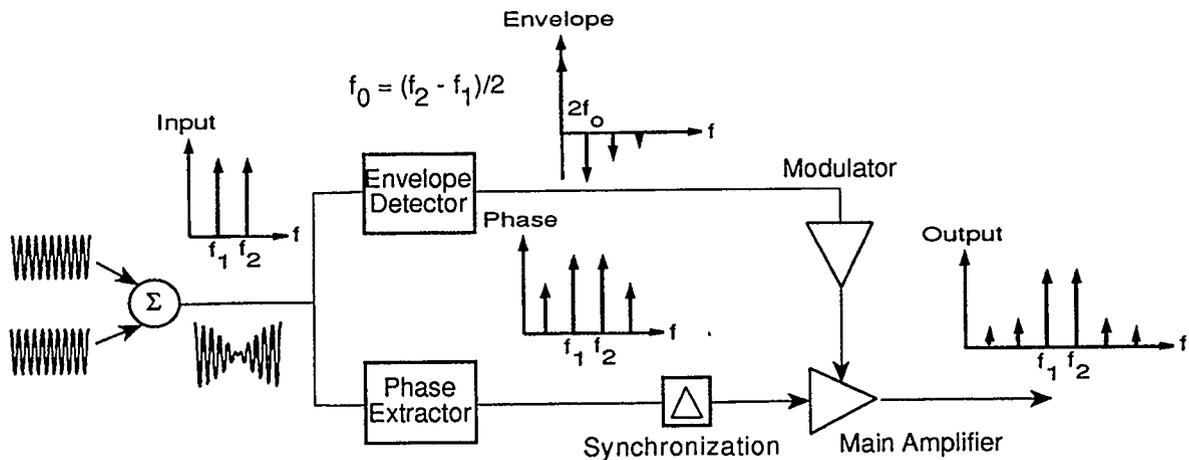


Figure 4.1 Simplified Block Diagram of Method for Determining Distortion

With the simplified block diagram in mind, an overview of the analysis follows:

- 1) the frequency spectrum for the input signals is defined, maintaining frequency, magnitude and relative phase information
- 2) the output frequency spectrum of the envelope detector is calculated from the Fourier series
- 3) the envelope signal is amplified by the "Modulator" block, where it undergoes distortion due to non-linearity and frequency response limitations
- 4) the Fourier series of the "Envelope Limiter Gain Function" (ELGF) for the Phase Extractor is calculated. Note, the concept of the ELGF will be described in detail later in this chapter
- 5) the ELGF spectrum modulates the input signal spectrum producing the phase signal

- 6) the amplified envelope signal is recombined with the phase signal in the main amplifier. The effects of varying the main amplifier's power, via the modulator, and the feedthrough of the phase signal by the main amplifier are evaluated. This step produces the output signal
- 7) the intermodulation distortion of the output signal relative to the fundamental input signal is compared in the frequency domain.

4.1.1. System Components

Before an overall system analysis can be achieved the behavior of each component is identified, defined and modeled.

4.1.1.1. Envelope Detector

The purpose of the envelope detector is to extract the amplitude information embedded in the combined input signals. The time domain response and truncated frequency spectrum of an ideal envelope detector is shown in Figure 4.2.

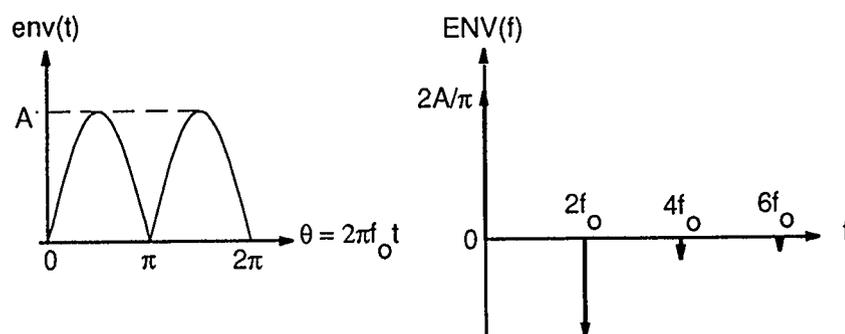


Figure 4.2 Time Domain and Truncated Frequency Domain Representation of an Ideal Envelope Signal

During the analysis the envelope signal is represented by the Fourier series. If one chooses the minimum amplitude of the envelope to occur at zero,

the waveform then has an even symmetry which requires only cosine terms in the description of the series. The Fourier series for the ideal envelope can be described as:

$$\text{env}_{\text{ideal}}(t) = a_0 + \sum_n a_n \cos(n\omega_0 t) \quad (4.1)$$

where: $n = 2, 4, 6, \dots$

a_0, a_2, a_4, \dots are the Fourier coefficients of the series

$\omega_0 = 1/T$ and is denoted as the fundamental frequency of the series in radians

Actual implementation of the envelope detector reveals that the ideal response cannot be achieved exactly. Instead the output exhibits non-ideal characteristics as shown in Figure 4.3.

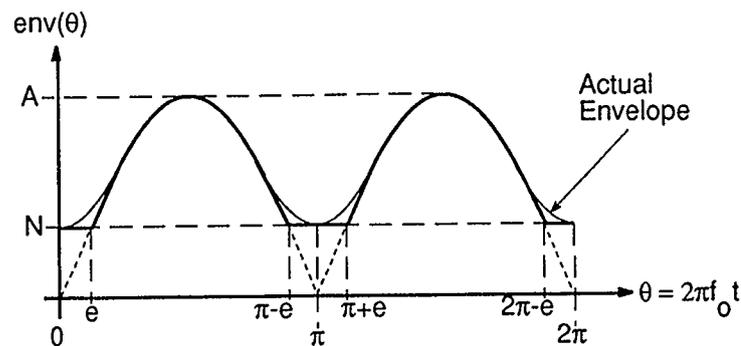


Figure 4.3 Non-Ideal Envelope Characteristic

In Figure 4.3 the envelope detector output develops a "floor" designated by the value N . This floor is a result of noise and the inability of the detector to pass an infinite number of harmonics. The value of N will approach zero with the use of an envelope detector designed for use at high frequencies or by the reduction of the envelope frequency. It is acceptable to approximate the floor as a flat section.

The non-ideal envelope function is defined as:

$$\text{env}(t) = [N]_0^e + [A \sin \theta]_e^{\pi-e} + [N]_{\pi-e}^{\pi+e} - [A \sin \theta]_{\pi+e}^{2\pi-e} + [N]_{2\pi-e}^{2\pi} \quad (4.2)$$

where: $e = \sin^{-1} \frac{N}{A}$

N is the minimum value or "floor"

A is the maximum value of the envelope

The dc coefficient for the Fourier series of the non-ideal envelope is evaluated in the following manner:

$$a_0 = \frac{1}{T} \int_0^T f(\theta) d\theta = \frac{1}{\pi} \left[\int_0^e N d\theta + A \int_e^{\pi-e} \sin \theta d\theta + \int_{\pi-e}^{\pi} N d\theta \right] \quad (4.3)$$

$$a_0 = \frac{1}{\pi} [2Ne + A \cos(e) - A \cos(\pi - e)]$$

Due to even symmetry there are no sine terms in the series. The remaining coefficients are evaluated using Equation 4.4:

$$a_n = \frac{2}{\pi} \left[\int_0^e N \cos n\theta d\theta + A \int_e^{\pi-e} \sin \theta \cos n\theta d\theta + \int_{\pi-e}^{\pi} N \cos n\theta d\theta \right] \quad (4.4)$$

$$a_n = \frac{1}{\pi} \left[\frac{N}{n} \{ \sin(ne) - \sin(n(\pi - e)) \} + A \left\{ \frac{\cos(e(n+1)) - \cos((\pi - e)(n+1))}{n+1} + \frac{\cos((\pi - e)(n-1)) - \cos(e(n-1))}{n-1} \right\} \right]$$

The fundamental frequency is equal to one half of the separation between the input signal frequencies. It can be shown that the odd order cosine coefficients (i.e. a_1, a_3 , etc.) are zero.

The frequency spectrum is now easily constructed from the preceding information. For a frequency spectrum which does not display negative frequencies (i.e. a single sided spectrum) the coefficients of the Fourier series are equivalent to the magnitude of the spectral components. The phase angle

of the spectral components is determined by the sign of the Fourier coefficients, either 0° or 180° . The frequencies at which the spectral components are located corresponds to the frequency of the cosine term in the Fourier series shown in Equation 4.1 (i.e. $2\omega_0$, $4\omega_0$, etc.).

4.1.1.2. Modulator

The purpose of the modulator is to provide sufficient gain to the relatively weak incoming envelope signal so that it may be used to drive the high efficiency main amplifier. Ideally the modulator has a linear transfer characteristic and a flat frequency response. An ideal modulator produces an exact amplified replica of the input signal envelope. Implementation of the modulator reveals that some non-linear effects will be imparted to the envelope signal as it undergoes amplification. The model used for the modulator is shown in Figure 4.4.

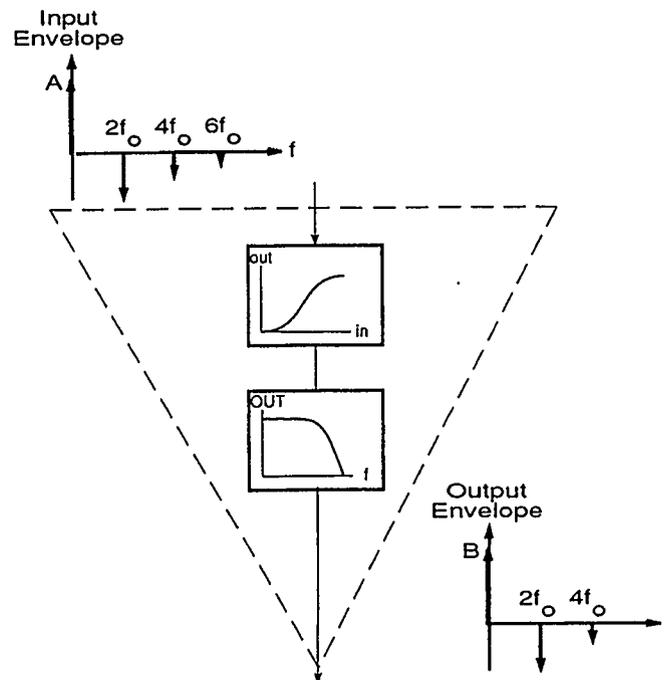


Figure 4.4 Modulator Block Diagram

In the first stage of the modulator model the effect of a non-linear voltage transfer characteristic is represented. The expression used to model the non-linearity of the modulator is:

$$v_{out} = M_0 + M_1 \times v_{in} + M_2 \times v_{in}^2 + \dots + M_n \times v_{in}^n \quad (4.5)$$

The order of the polynomial in Equation 4.5 is chosen to ensure that the approximation accurately represents the actual transfer characteristic of the modulator. It was determined that a ninth order polynomial is sufficient to ensure that 99.99% of the errors in the curve fit are accounted for by the variance of the measured data. The result of passing the envelope detector signal through the non-linear transfer characteristic is the appearance of frequency terms at $12f_0$, $14f_0$, etc. and new components at dc, $2f_0$, $4f_0$ etc. These new spectral components will add and subtract from existing spectral components. The additions to and modifications of the original envelope spectrum cause distortion by altering the shape of the envelope signal.

Before modulating the approximated envelope signal with the non-linear transfer characteristic, the envelope signal data was normalized to ensure that no data point exceeded the upper limit of the non-linear transfer characteristic approximation. The normalized envelope signal data is modulated with the non-linear transfer characteristic by multiplication in the time domain via a mathematical analysis program [26].

In the second stage of the modulator model, the effect of a finite frequency response is represented. The finite frequency bandwidth is used to determine the number of spectral components that will exist in the output envelope spectrum. The modulator frequency response is modeled by a 2nd

order Butterworth low pass filter. The equation describing the Butterworth frequency response is:

$$H(s) = \frac{b_0}{b_2 \left(\frac{s}{\Omega_0} \right)^2 + b_1 \left(\frac{s}{\Omega_0} \right) + b_0} \quad (4.6)$$

where: $s = j\omega$

b_0, b_1, b_2 are the filter coefficients

Ω_0 is the normalization frequency

The Butterworth filter coefficients and normalization frequency are evaluated from measured data using the curve fitting capabilities of the data analysis program [27]. The curve fit routine uses the method of least squares when curve fitting and can be used to fit a general function, entered by the user, to a set of measured data.

The process of filtering is most easily performed in the frequency domain. A DFFT is performed on the envelope data set which contains the high order spectral components. The resulting frequency spectrum of the envelope signal is multiplied by the 2nd order Butterworth low pass filter approximation. This step has the effect of reducing the magnitude of the higher frequency components. In preparation for modulation in the main amplifier, an IDFFT is performed on the envelope signal at this point.

The construction of the envelope signal entering the main amplifier has now been completed. The next step in the analysis is the generation of an approximation to the phase signal entering the main amplifier. The construction of the phase signal approximation begins with the input signals entering the limiter.

4.1.1.3. Limiter

The purpose of the limiter is to remove the amplitude variation effects embedded in the input signal. In order to produce an output signal of constant amplitude, the limiter must apply a varying gain to the input signal; large gain when a low level signal is present and small gain when a high level signal is present. An ideal limiter can therefore be thought of as a variable gain device. The variable gain of the limiter is denoted the "Envelope Limiter Gain Function", ELGF, and is equal to the inverse of the envelope of the input signal [24].

$$\text{elgf}(t) = \frac{1}{\text{env}(t)} \quad (4.7)$$

Modulation of the input signal with the envelope limiter gain function removes the amplitude modulation and produces the phase only information shown in Figure 4.5(c).

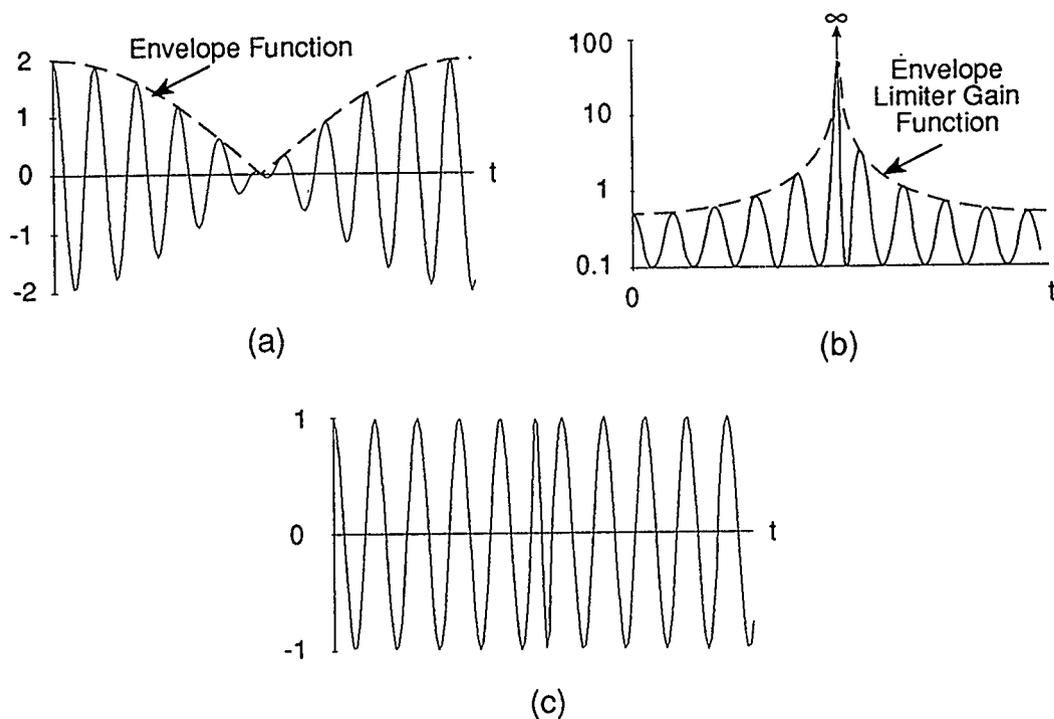


Figure 4.5 Ideal Limiter Waveforms (a) Input Signal (b) Envelope Limiter Gain Function (c) Phase Information at Limiter Output

The method of determining the Fourier series for the ELGF begins by inverting the envelope function as shown in Figure 4.6.

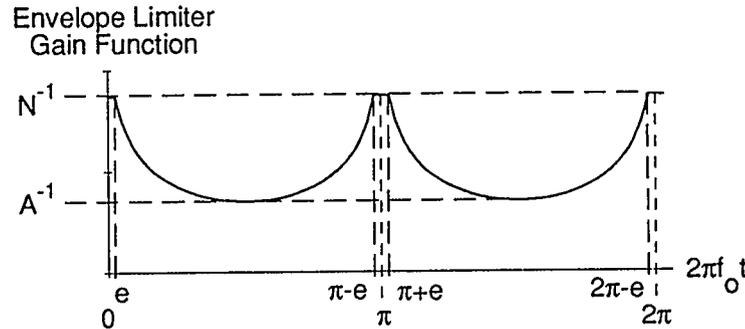


Figure 4.6 Non-ideal Envelope Limiter Gain Function

In Figure 4.6 the limiter has a finite maximum gain represented by the value N^{-1} . The minimum gain is represented by the value A^{-1} . The expression for the ELGF is derived with the aid of Figure 4.3 and Figure 4.6.

$$\text{elgf}(t) = \frac{1}{\text{env}(t)} \approx \left[\frac{1}{N} \right]_0^e + \left[\frac{1}{A} \times \frac{1}{\sin \theta} \right]_e^{\pi-e} + \left[\frac{1}{N} \right]_{\pi-e}^{\pi+e} \quad (4.8)$$

Next, the Fourier coefficients describing this wave form are determined. The fundamental frequency of the Fourier series is taken to be equal to half of the difference between the two input signal frequencies. The dc coefficient is evaluated using equation 4.9:

$$a_0 = \frac{1}{T} \int_0^T \text{elgf}(\theta) d\theta = \frac{1}{\pi} \left[\int_0^e \frac{d\theta}{N} + \int_e^{\pi-e} \frac{d\theta}{A \sin \theta} + \int_{\pi-e}^{\pi} \frac{d\theta}{N} \right] \quad (4.9)$$

$$a_0 = \frac{1}{\pi} \left[\frac{2e}{N} + \frac{1}{A} \ln \left\{ \frac{1 + \cos(e)}{1 - \cos(e)} \right\} \right]$$

The even symmetry of the wave form indicates that all odd coefficients are equal to zero. Equation 4.10 defines the second coefficient in the Fourier series.

$$\begin{aligned}
 a_2 &= \frac{2}{\pi} \left[\int_0^e \frac{\cos(2\theta)d\theta}{N} + \int_e^{\pi-e} \frac{\cos(2\theta)d\theta}{A \sin(\theta)} + \int_{\pi-e}^{\pi} \frac{\cos(2\theta)d\theta}{N} \right] \\
 a_2 &= \frac{2}{\pi} \left[\frac{\sin(2e)}{N} + \frac{1}{A} \ln \left\{ \frac{\cos\left(\frac{e}{2}\right) \sin\left(\frac{\pi-e}{2}\right)}{\cos\left(\frac{\pi-e}{2}\right) \sin\left(\frac{e}{2}\right)} \right\} - \frac{4}{A} \cos(e) \right] \quad (4.10)
 \end{aligned}$$

In like manner the remaining even order coefficients can be calculated using the following series.

$$a_n = \frac{2}{\pi} \left[\frac{2 \sin(ne)}{nN} + \frac{1}{A} \ln \left\{ \frac{\cos\left(\frac{e}{2}\right) \sin\left(\frac{\pi-e}{2}\right)}{\cos\left(\frac{\pi-e}{2}\right) \sin\left(\frac{e}{2}\right)} \right\} - \frac{4}{A} \left\{ \sum_{j=2}^n \frac{\cos((j-1)e)}{j-1} \right\} \right] \quad (4.11)$$

where: $j = 2, 4, 6, \dots$ $n = 2, 4, 6, \dots$

Before solution of Equations 4.9 through 4.11 is possible, the values of A and N must be known. Determination of these variables is performed using the relationships of the envelope and the ELGF as shown in Figure 4.7.

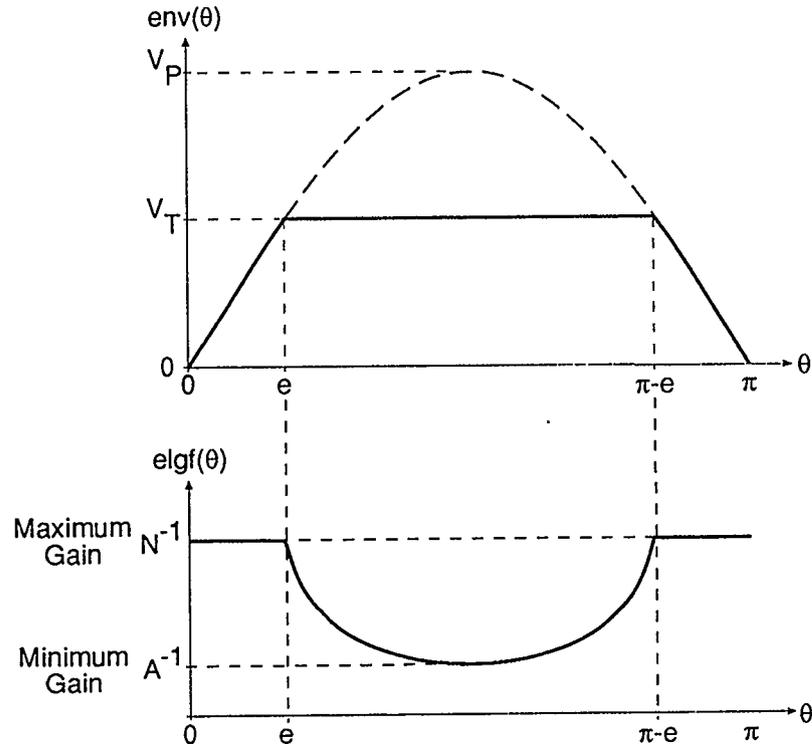


Figure 4.7 Relationship of Envelope Signal and ELGF for Determination of Fourier Series Variables

Below the threshold voltage, V_T , the envelope signal remains unmodified and therefore the maximum gain value is unity. The variable N is therefore also unity since it is the inverse of the maximum gain.

The minimum gain value is determined at the point where the input signal reaches the maximum value, V_P . At this point the limiter must maintain the output at the threshold voltage. Therefore the minimum gain is:

$$\min \text{ gain} = \frac{V_T}{V_P} = A^{-1} = \sin(e) \quad (4.12)$$

where: V_T is the threshold voltage at which limiting occurs

V_P is the peak voltage the envelope would reach without limiting

It is now possible to construct the Fourier series describing the ELGF. Once this is accomplished, the phase signal at the output of the limiter is calculated.

The phase signal is produced by modulating the input signals with the ELGF. The effect of modulating each input signal by the ELGF can be observed in the frequency domain.

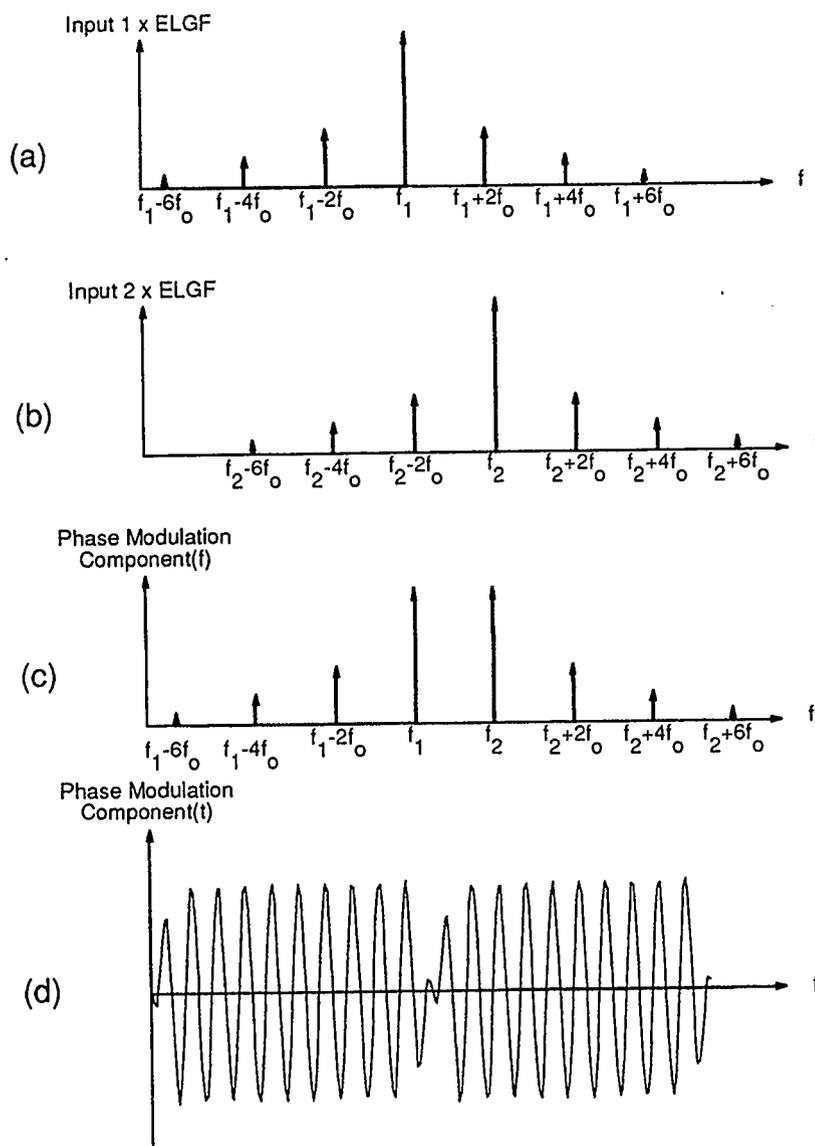


Figure 4.8 Calculation of Phase Modulation Component Spectra (a) Modulation of first tone with ELGF (b) Modulation of second tone with ELGF (c) Frequency Spectra at output of Limiter (d) Time domain output of Limiter

In Figure 4.8(a) the first input tone located at frequency f_1 is modulated by the ELGF spectrum. Similarly, in Figure 4.8(b) the result of modulating the second input tone located at frequency f_2 with the ELGF is shown. The separate spectra are summed together to produce the phase modulation component spectrum of a two-tone equal input signal as shown in Figure 4.8(c). The time domain representation of the phase signal at the output of the limiter is shown in Figure 4.8(d).

The construction of the phase signal entering the main amplifier has been completed at this point. All that remains to complete the analysis is to combine the envelope signal and phase signal in the main amplifier.

4.1.1.4. Main RF PA

The purpose of the main power amplifier is to produce an amplified replica of the input signals while keeping the distortion to a minimum. The model used for the main power amplifier is shown in Figure 4.9.

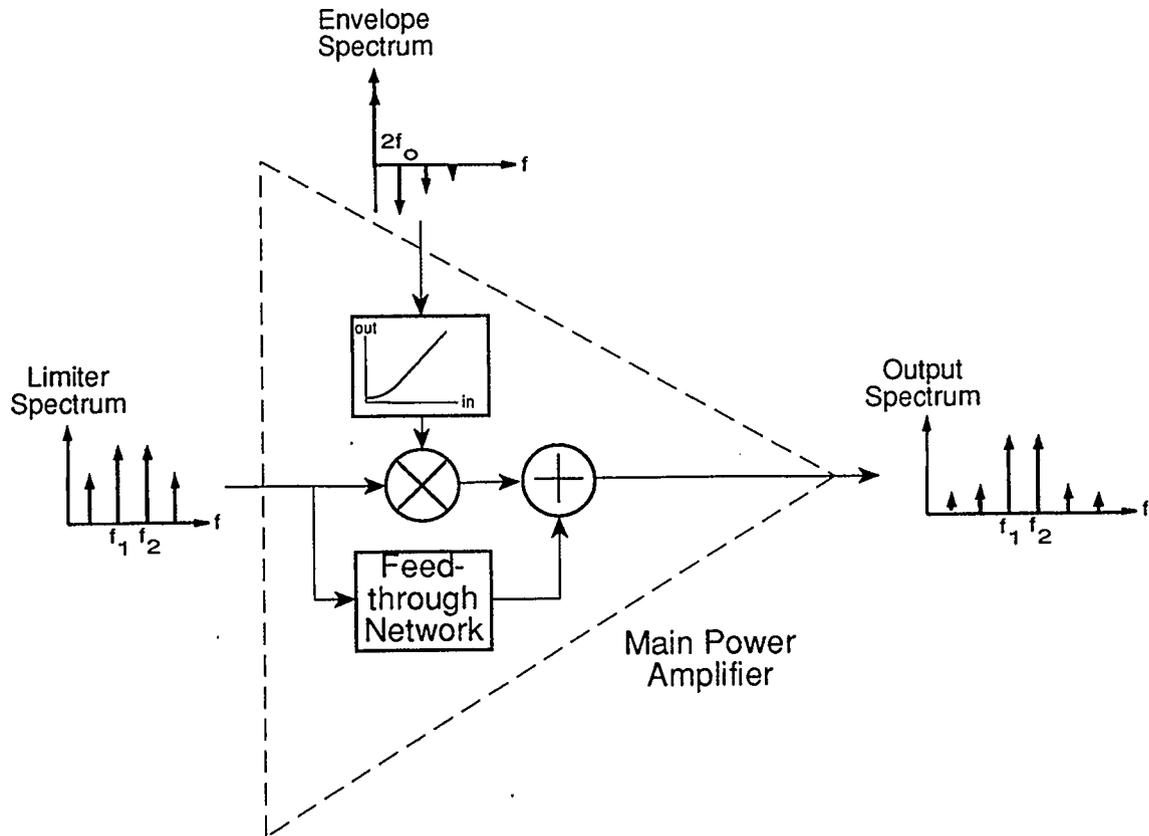


Figure 4.9 Main Power Amplifier Block Diagram

The model presented in Figure 4.9 accounts for two behavior characteristics of the main power amplifier. The first characteristic is the response to a varying power supply voltage. The non-linear modulation transfer function is modeled in the same manner presented in the Modulator section. The envelope signal is first passed through a non-linear transfer function block before being multiplied by the phase signal.

Kazimierczuk [25] and others have shown that the output signal from a class E amplifier is almost completely proportional to the supply voltage of the amplifier. This linear behavior allows for the use of a multiplier block in the first stage of the amplifier model. The only deviation from this linear behavior occurs at very small supply voltages when feedthrough of the input (phase) signal occurs (refer to Figure 4.10(b)).

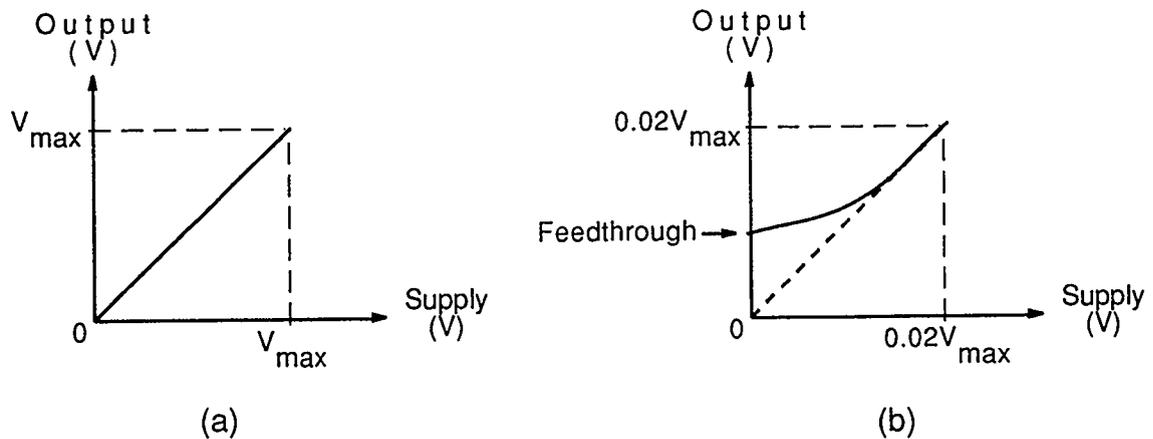


Figure 4.10 Typical Amplitude Modulation Transfer Function for a Class E Amplifier

Due to the complex behavior (i.e. possessing both magnitude and phase characteristics) of feedthrough, it was chosen as the second characteristic of the main power amplifier to be modeled. The feedthrough network used to predict the distortion at the output is a simplified model of a FET.

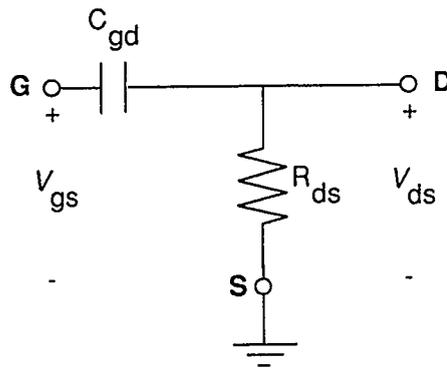


Figure 4.11 Feedthrough Network

The expression for the feedthrough network is the well known voltage divider equation.

$$\frac{V_{ds}}{V_{gs}} = \frac{R_{ds}}{R_{ds} + \frac{1}{j\omega C_{gd}}} \quad (4.13)$$

The component values for C_{gd} and R_{ds} are taken from the specification sheet of the transistor or may be approximated from the S-parameters for the device.

The final output signal results from a multiplication of the phase signal by the envelope signal and a final addition of the feedthrough distortion. The magnitude of the intermodulation distortion products can be identified by transforming the time domain output to the frequency domain using a DFFT.

4.1.2. Intermodulation Distortion Products

The process of analyzing the intermodulation distortion effects upon a system is rather complicated. By its very nature a system is composed of a number of components, each of which possess unique non-linearities that contribute to the overall distortion at the output. In order to simplify the analysis, it was decided to concentrate on the major components and their characteristics which most affect system performance. In each of the following sections one component is isolated, and the major performance characteristic is varied to determine the dependence of the 3rd, 5th and 7th order intermodulation distortion products on this characteristic. During this process the remaining components in the system are treated as having ideal behavior.

4.1.2.1. Intermodulation Distortion due to Imperfect Limiter Performance

A good measure of the performance of a limiter is the amount of time the signal is maintained at the limiting threshold relative to the total period of the waveform. The amount of time the output signal resides at the limiting threshold is defined by the limiting angle (ϵ) as shown in Equation 4.12 and in Figure 4.7.

The analysis begins by generating two equal amplitude sinusoid signals and combining them together by simple addition. This results in a two tone signal. The maximum amplitude that the two tone signal achieves is denoted the peak voltage, V_P . The minimum amplitude of the two tone signal is zero. The fundamental frequency of the envelope waveform is equal to one half the separation between the input signal frequencies.

An ideal envelope wave form is generated using Equations 4.3 and 4.4 with a value of N equal to zero. The number of coefficients required to form the ideal envelope waveform is evaluated by comparing the size of the n th coefficient to the 2nd coefficient in the series. When the size of the n th coefficient is less than 1% of the 2nd coefficient the series is deemed to be complete enough that it will not introduce significant distortion effects. As a result of this criteria a series of 18th order for the ideal envelope waveform is used.

To achieve a variation of the limiting angle, the threshold voltage V_T is adjusted from the value of zero to the peak voltage V_P (refer Figure 4.7). This results in a variation of the limiting angle from 0° to 90° .

The coefficients of the ELGF are calculated using equations 4.9 and 4.11. The number of coefficients required to form the ELGF is evaluated by comparing

the size of the n th coefficient to the 2nd coefficient in the series. When the size of the n th coefficient is less than 1% of the 2nd coefficient, the series is deemed complete enough that it will not introduce significant distortion effects. As a result of this criteria, the series varies from an order of 26, for a limiting angle of 30° , to the 188th order for a limiting angle of 85° .

The ELGF modulates the two tone input signal producing the phase signal that enters the main power amplifier. By multiplying the ideal envelope signal with the phase signal the output of the main power amplifier is produced. The IMD products are observed in the frequency domain.

Figure 4.12 shows the relationship of the theoretical intermodulation distortion products to the limiting angle.

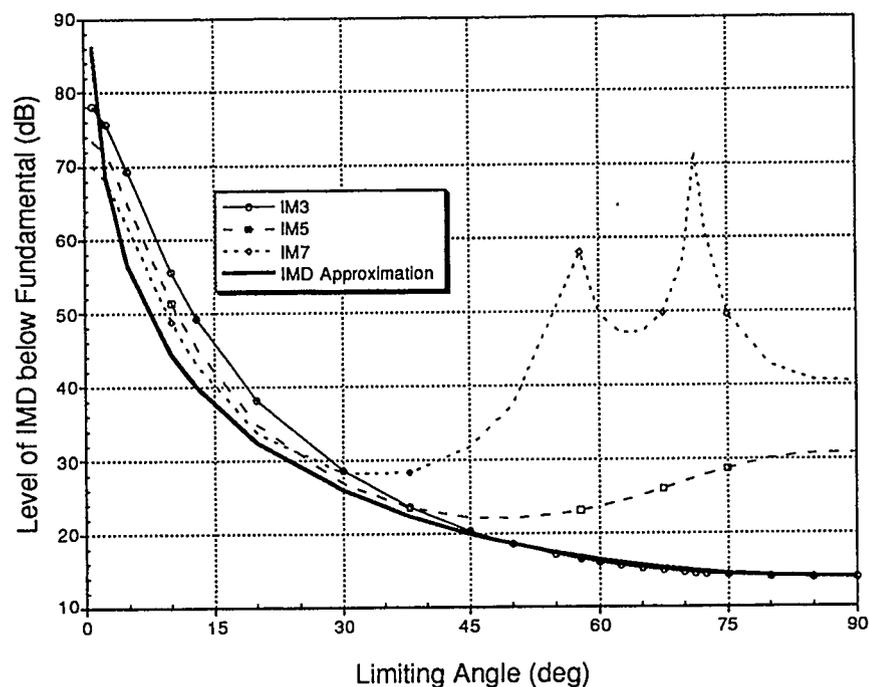


Figure 4.12 Effect of Limiting Angle on Intermodulation Distortion Products

From Figure 4.12 it is observed that the best limiter performance is achieved when the limiting angle is small. A curve fit is performed to generate an expression relating the level of intermodulation distortion products to the limiting angle (ϵ) to yield:

$$\text{IMD} \leq \frac{1}{5\pi} \sin^2(\epsilon) \quad (4.14)$$

Therefore to ensure that the IMD's are 30 dB below the fundamental of a two-tone signal, a limiting angle of less than 23° is required. If it is desired to have intermodulation distortion products 40 dB below the fundamental, then a limiting angle less than 12.9° is required.

A copy of the MathCAD file detailing the limiter analysis is shown in Appendix A.1.

4.1.2.2. Intermodulation Distortion due to Time Delay

Recombination of the envelope signal and phase signal at the main power amplifier allows for the possibility that a timing error may occur. Misalignment is quantified by comparing the time at which the 180° discontinuity of the phase signal occurs with reference to the zero point of the envelope signal as shown in Figure 4.13.

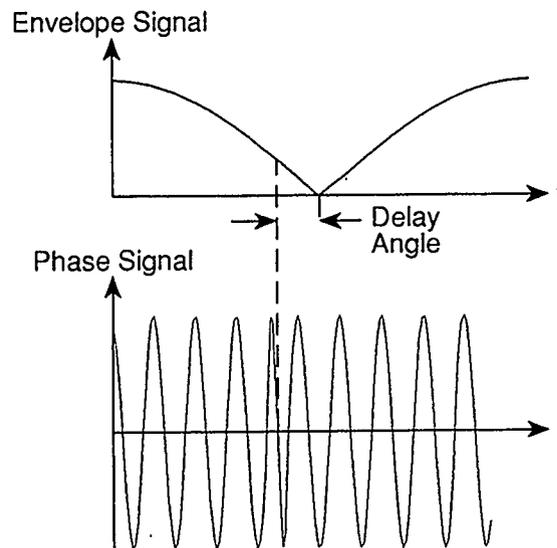


Figure 4.13 Delay Angle

The delay angle ranges from 0° , for perfect alignment, to 90° when the phase discontinuity occurs at the peak value of the envelope signal. Due to the symmetry of the waveforms a positive delay angle has the same effect as a negative delay angle.

The analysis begins in the same manner as described for the limiter, i.e., by generating a two tone signal and calculating an ideal envelope series. The performance of an ideal limiter was approximated by setting the limiting angle to within 1% or 0.9° of a perfect limiter. This compromise is necessary to keep the order of the ELGF series to a manageable level.

Misalignment is simulated by placing a delay in the envelope signal. The near ideal phase signal and delayed envelope signal recombine in the main power amplifier resulting in the theoretical intermodulation distortion products shown below.

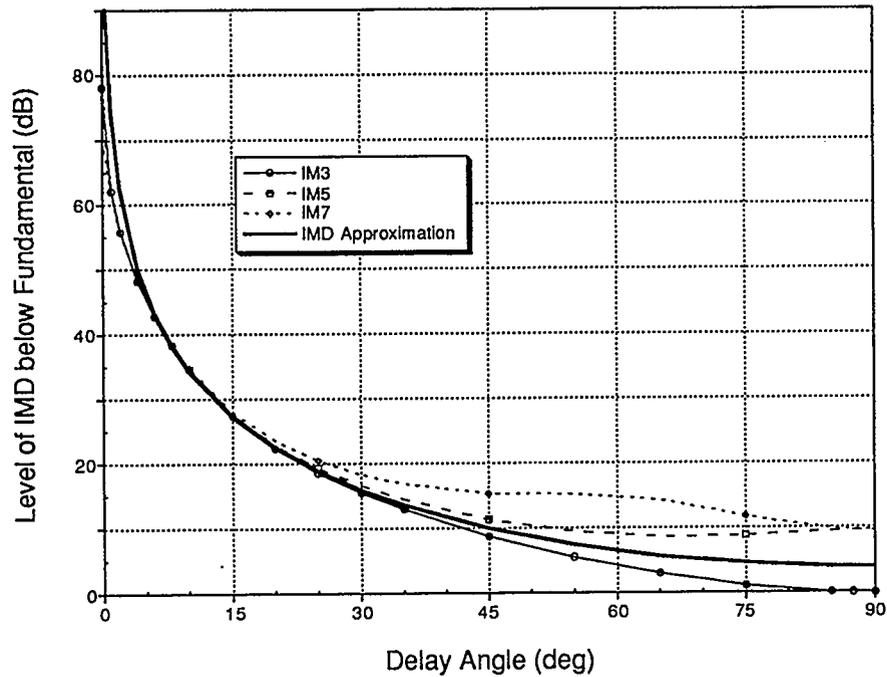


Figure 4.14 Effect of Delay Angle on Intermodulation Distortion Products

From Figure 4.14 it is observed that the best performance is achieved when the delay angle is small. A curve fit of the data points where the IMD's are 30 dB to 40 dB is performed to generate an expression relating the level of intermodulation distortion products to the delay angle to yield:

$$\text{IMD} \leq \frac{2}{\pi} \sin^2(d) \quad (4.15)$$

where: d is the delay angle

Therefore to ensure that the IMDs are 30 dB below the fundamental of a two-tone signal, a delay angle of less than 12.9° is required. If it is desired to have intermodulation distortion products 40 dB below the fundamental, then a

delay angle less than 7.2° is required. These predictions agree with a similar analysis performed by Raab [12].

A copy of the MathCAD file detailing the delay analysis is shown in Appendix A.2.

4.1.2.3. Intermodulation Distortion due to the Modulator Frequency Response

Another major characteristic of the system is the frequency bandwidth of the modulator. The frequency performance is quantified by normalizing the cutoff frequency, f_c , with the envelope signal fundamental frequency, f_o .

The analysis proceeds, as described previously, by generating a two tone signal, calculating an ideal envelope series and calculating a near ideal ELGF series.

The frequency response of the modulator is simulated using a 2nd order Butterworth Low Pass Filter approximation. The effects of filtering the magnitude components of the ideal envelope spectrum, as well as the effect caused by group delay through the filter, are considered. The results of the simulation are shown below.

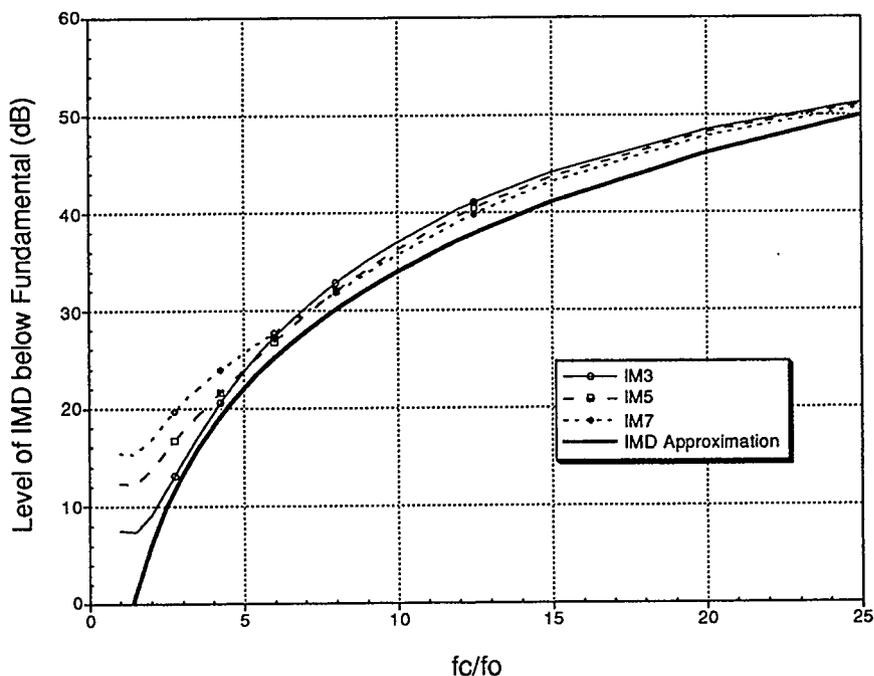


Figure 4.15 Effect of Modulator Cutoff Frequency on Intermodulation Distortion Products

From Figure 4.15 it is observed that the best performance is achieved when the normalized cutoff frequency is large. A conservative curve fit is performed to generate an expression relating the level of intermodulation distortion products to the normalized cutoff frequency to yield:

$$\text{IMD} \leq 2 \left(\frac{f_o}{f_c} \right)^2 \quad (4.16)$$

Therefore to ensure that the intermodulation distortion products are 30 dB below the fundamental of a two-tone signal, a normalized cutoff frequency of approximately 8 is required. If it is desired to have intermodulation distortion

products 40 dB below the fundamental, then a normalized cutoff frequency of approximately 14 is required.

A copy of the MathCAD file detailing the frequency analysis is shown in Appendix A.3.

4.1.2.3. Intermodulation Distortion due to Feedthrough

The amount of feedthrough signal which reaches the output is dependent on the frequency of operation and the component values in the feedthrough network. As the frequency of operation is increased, the reactance of C_{gd} will decrease causing more of the input signal to appear at the output.

An obvious approach to reducing the effect of feedthrough would be to reduce the amplitude of the incoming signal. Unfortunately the reduction of the phase signal contributes to the reduction of the efficiency of the Class E amplifier as shown in the Figure 4.16.

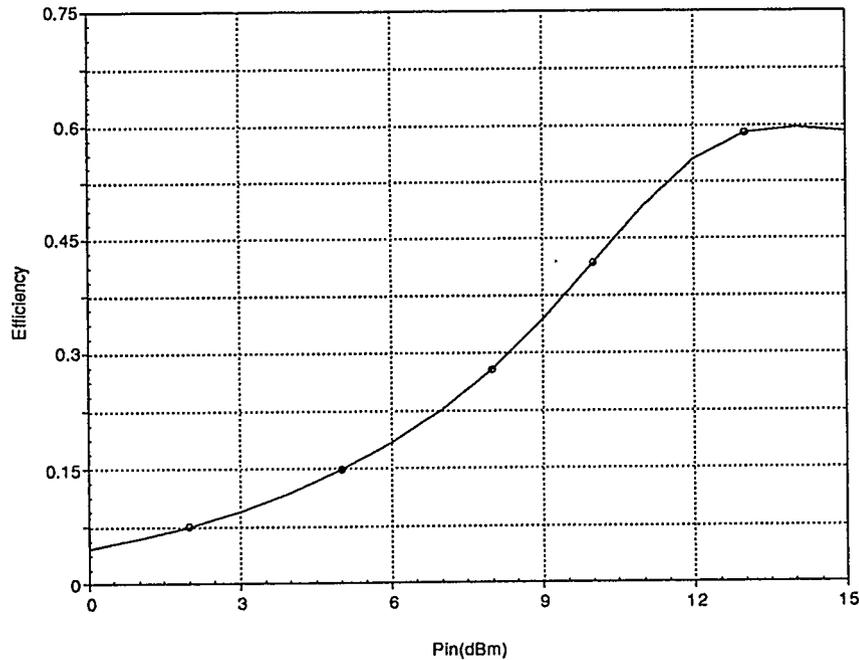


Figure 4.16 Class E Efficiency versus Phase Signal Input Power

Therefore the best performance is achieved when the level of input power is chosen to achieve good efficiency while reducing the feedthrough distortion. An input power of 14 dBm, a frequency of 1 GHz, and the transistor manufacturer's values for $C_{gs} = 0.3$ pF and $R_{ds} = 15$ ohms [28] would result in feedthrough distortion products approaching -27 dBc. This implies that even if the amplifier has no other non-linearities, the distortion cannot be reduced below the level set by feedthrough. A secondary effect of feedthrough makes itself evident in the general appearance of the main amplifier output spectrum. Prior to including the effects of feedthrough the main amplifier spectrum is always symmetrical about the fundamental two tones regardless of the amplifier non-linearities. Adding feedthrough to the system, which causes a varying

phase shift, causes the main amplifier output spectrum to become asymmetrical. These factors are used to verify that feedthrough occurs.

4.2. System Efficiency

By definition, the efficiency of a closed system relates the total output power to the total input power as shown below:

$$\eta = \frac{\text{Total Output Power}}{\text{Total Input Power}} \quad (4.17)$$

The closed system under analysis is shown in Figure 4.17.

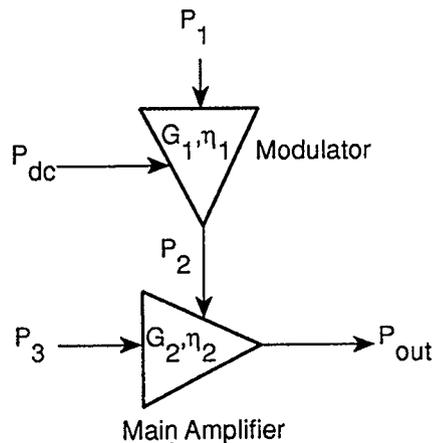


Figure 4.17 Closed System Used for Efficiency Analysis

The modulator and main amplifier possess individual power gains (G_1 & G_2) as well as individual efficiencies (η_1 & η_2). The total efficiency of the system is expressed as:

$$\eta_T = \frac{P_{out}}{P_{dc} + P_1 + P_3} \quad (4.18)$$

An expression defining the output power of the modulator (P_2) as a function of the dc power (P_{dc}), modulator power gain (G_1) and modulator efficiency (η_1) is derived first. The efficiency of the modulator is defined as:

$$\eta_1 = \frac{P_2}{P_{dc} + P_1} \quad (4.19)$$

The output power and input power are related by the power gain as follows:

$$G_1 = \frac{P_2}{P_1} \quad (4.20)$$

Combining and rearranging equations 4.19 and 4.20 yields:

$$P_2 = P_{dc} \times \frac{G_1 \eta_1}{G_1 - \eta_1} \quad (4.21)$$

The power gain expression for the main amplifier is derived in a similar manner and results in:

$$P_{out} = P_2 \times \frac{G_2 \eta_2}{G_2 - \eta_2} \quad (4.22)$$

Combining equations 4.21 and 4.22 produces an expression of the output power in terms of the dc power.

$$P_{out} = P_{dc} \times \frac{G_1 \eta_1}{G_1 - \eta_1} \times \frac{G_2 \eta_2}{G_2 - \eta_2} \quad (4.23)$$

Substituting these findings into Equation 4.18 yields an expression for the total efficiency of the system.

$$\eta_T = \frac{G_2 \eta_1 \eta_2}{G_2 + \eta_2 (\eta_1 - 1)} \quad (4.24)$$

This equation leads to the conclusion that the total system efficiency is independent of the power gain of the modulator. Equation 4.24 also indicates that as the individual amplifier efficiencies approach unity the total system efficiency increases as the main amplifier power gain increases. The best

combination is both high power gain and high efficiency, which is no surprise. Figure 4.18 graphically displays the relationship of total efficiency to the individual amplifier efficiencies.

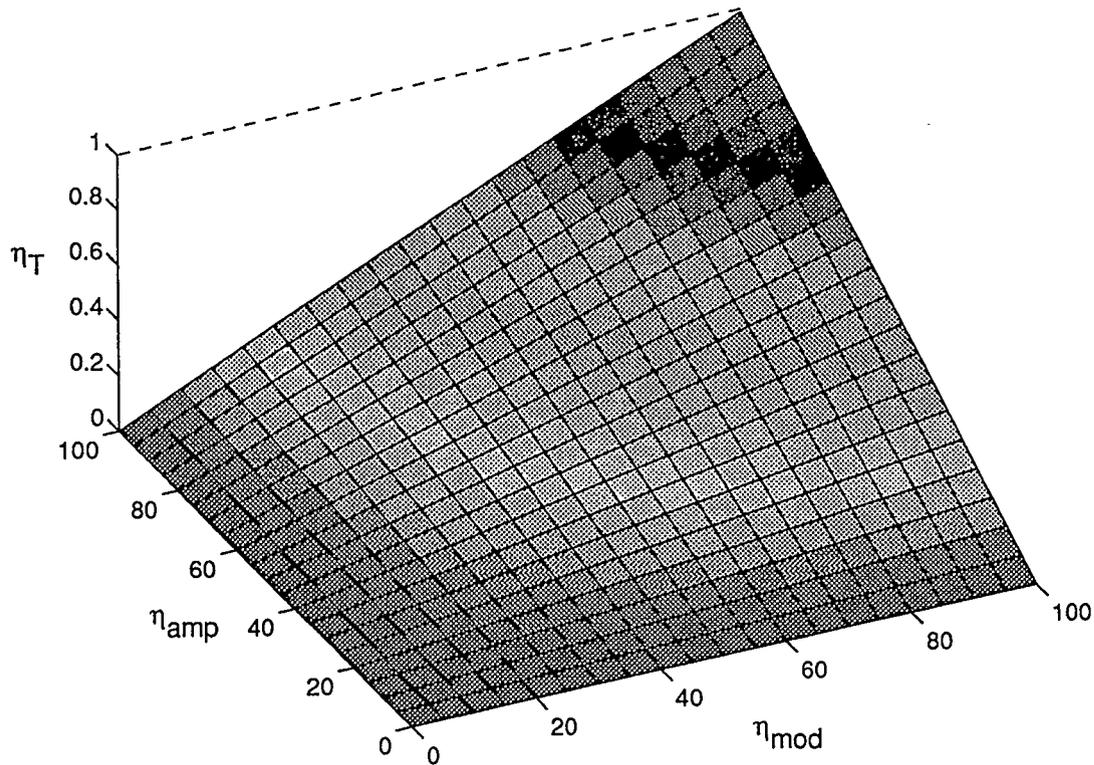


Figure 4.18 Comparison of Total Efficiency versus Individual Modulator and Main Amplifier Efficiency (Main Amplifier Power Gain = 20)

Figure 4.18 demonstrates that the change in total system efficiency varies linearly with change in either the efficiency of the modulator or the main amplifier. This results in the conclusion that total system efficiency is influenced equally by a change in either modulator or main amplifier efficiency.

Chapter Five - Experimental Circuit, Measurements and Results

This chapter discusses the construction of the test system, the experimental procedures used, and the test results obtained. The experiments were designed to check the performance of the envelope detector, modulator, phase extractor and main power amplifier discussed in chapter four. The simulated and measured performances are compared.

5.1. System Implementation

A modular approach was taken in the construction of the distortion reduction system. Commercially available modules were used whenever possible. The final implementation of the system is shown in Figure 5.1.

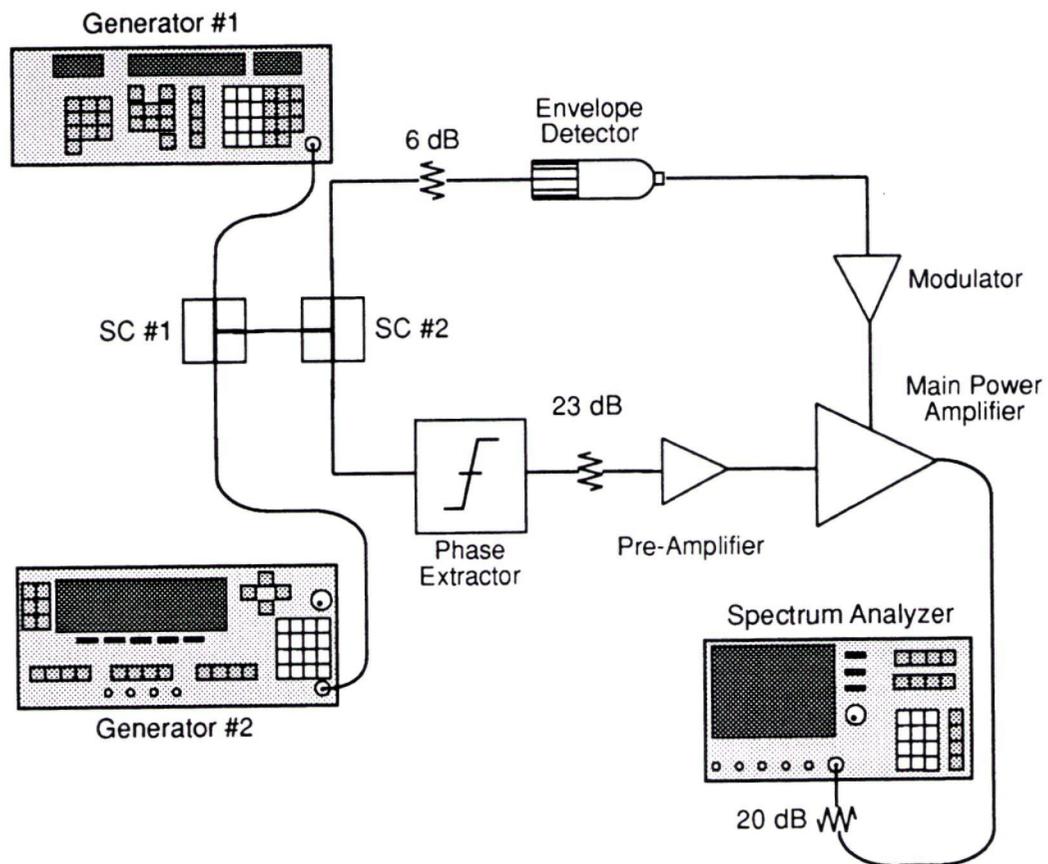


Figure 5.1 System Implementation

The test equipment used to generate and analyze the signals consisted of two signal generators and a spectrum analyzer. Generator #1 is a Hewlett Packard 8657B signal generator with a frequency range of 0.1 to 2060 MHz and a maximum power output of 17 dBm. Generator #2 is a Hewlett Packard 83650A sweep generator with a frequency range of 10 MHz - 50 GHz and a maximum power output of 18 dBm. The spectrum analyzer is a Hewlett Packard 8563A with a frequency range from 9 kHz to 26.5 GHz.

5.1.1. Circuit Module Specifications

Envelope Detector	Hewlett Packard HP 8470B Crystal Detector
	Frequency Range: 10 MHz to 18 GHz
	Maximum Operating Input Power: 200 mW
	Input Impedance: 50 ohms
	Output Impedance: 1 to 2K ohms
	SWR (10 MHz to 4 GHz): 1.15
Sensitivity (High level): 0.3 mW produces 100 mV	
Pre-Amplifier	RF Minicircuits ZHL-42 Amplifier
	Frequency Range: 700 to 4200 MHz
	Minimum Gain: 30 dB
	Output (1 dB Compression): +28 dBm
	3rd Order IP: +38 dBm
SC# 1	RF Minicircuits ZFSC 2-5 Splitter / Combiner
	Frequency Range: 10 to 1500 MHz
	Isolation: 25 dB
	Insertion Loss: 1.5 dB
SC# 2	RF Minicircuits ZFSC 2-2500 Splitter / Combiner
	Frequency Range: 10 to 2500 MHz
	Isolation: 17 dB
	Insertion Loss: 1.4 dB

Components that were not commercially available in an in-line coaxial connector package were developed as part of the research work and manufactured at the TR Labs and UofC facilities. These components consisted of the modulator, phase extractor and the main power amplifier.

5.1.2. Modulator Construction

The modulator is essentially a variable power supply capable of varying the output voltage at frequencies approaching 1 MHz. Since the efficiency of the modulator directly affects the system performance it is desirable to keep the power losses to a minimum. The schematic of the modulator used in the system is shown in Figure 5.2

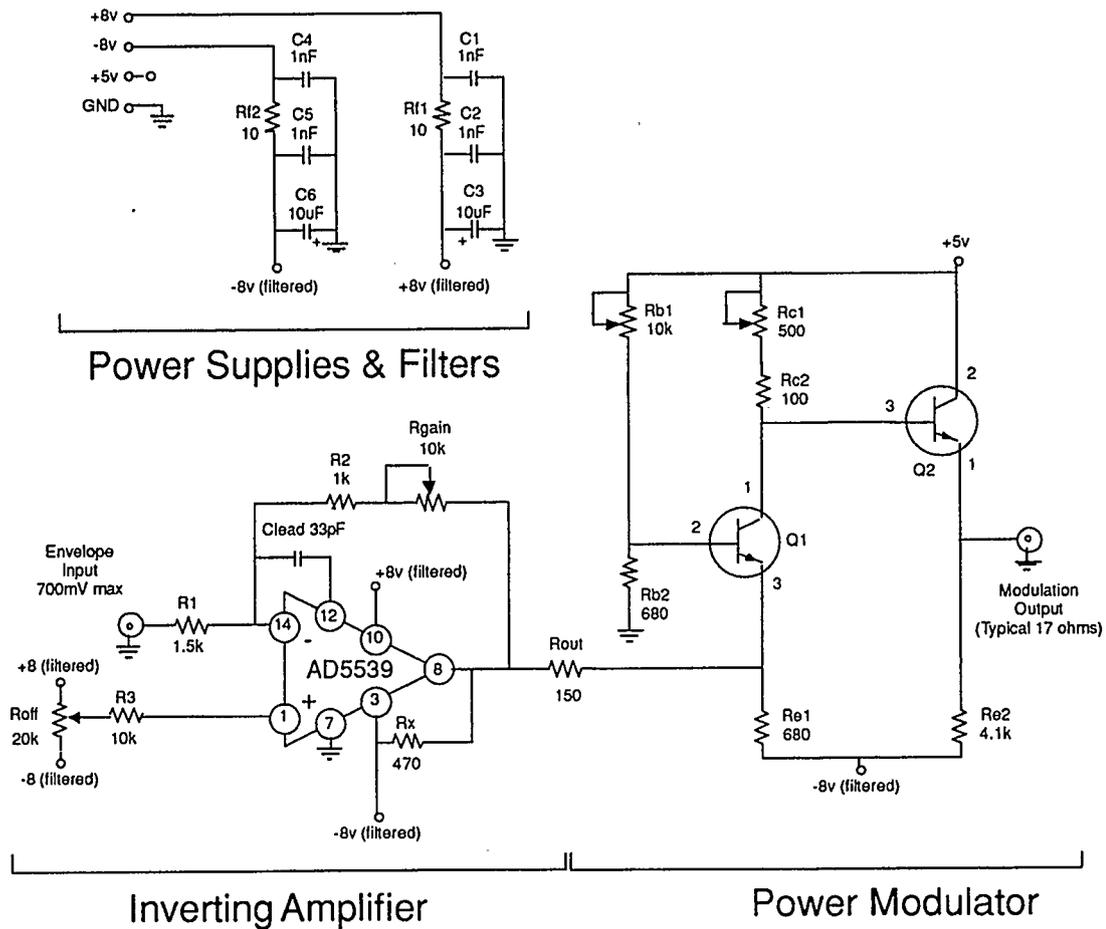


Figure 5.2 Modulator Schematic

The first circuit element is an Analog Devices AD5539 Ultrahigh Frequency Operational Amplifier in an inverting configuration whose purpose is to provide adjustable gain, offset and signal inversion. Transistor Q1 is a Motorola MRF525 NPN high frequency transistor and acts as a buffer stage between the Op-Amp and the final stage. Transistor Q2 is a Motorola MJE182 NPN power transistor and provides the necessary current drive into the load presented by the main power amplifier.

Potentiometers R_{b1} and R_{c1} are used to set the quiescent bias currents in transistors Q1 and Q2 respectively. These adjustments directly affect the linearity of the modulator. Higher bias currents cause the transistors to operate in the linear region of the I_c vs. V_{be} curve. However, in the interest of efficiency, it is expedient to maintain as low a bias current as possible without sacrificing linear operation.

The modulator was built on FR4 fiberglass printed circuit board using surface mount components where possible. SMA connectors were used at the input and output ports. The result was a modulator that possessed good linearity, frequency response and reasonable efficiency characteristics.

5.1.3. Phase Extractor Construction

The heart of the phase extractor circuit is the Avantek UTL-1002 Voltage Controlled Signal Limiter. This device features AM to PM conversion of less than 0.2 degrees per dB and has a voltage controllable limiting threshold. The schematic of the phase extractor used in the system is shown in Figure 5.3.

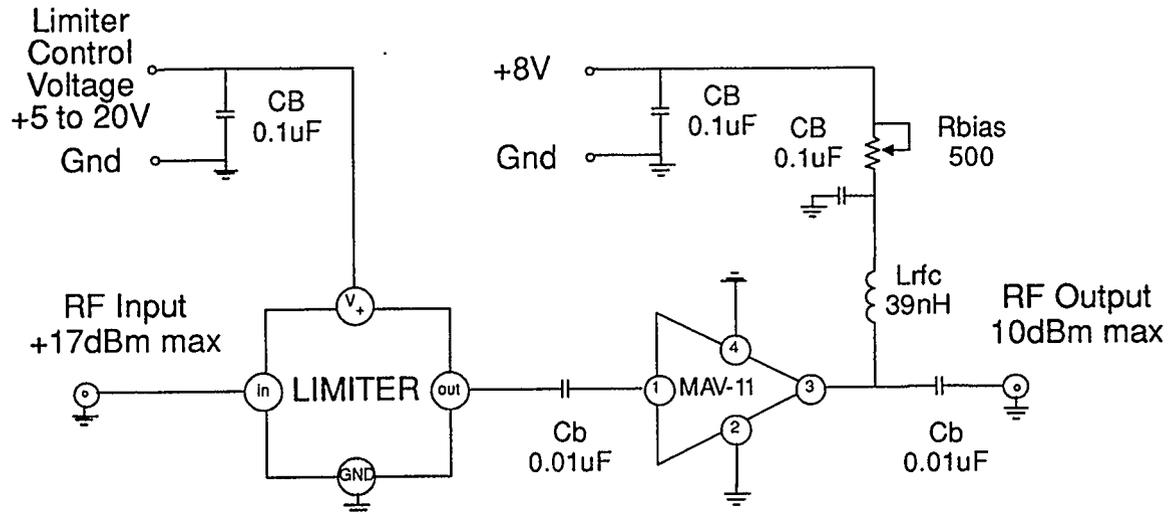


Figure 5.3 Phase Extractor Schematic

The second stage of the phase extractor is a RF Minicircuits MAV-11 monolithic amplifier which provides variable gain through adjustment of the potentiometer R_{bias} .

The phase extractor was built on Ultralam printed circuit board using surface mount components and SMA connectors.

5.1.4. Main Amplifier Construction

The main amplifier chosen for the system was a Class E amplifier and was constructed as a separate project within TRILabs. Design of Class E amplifiers has received increased attention within the last few years [5], [6], and [8] providing clear guidelines for the implementation of a 1 GHz device. The lumped component schematic of the Class E amplifier is shown in Figure 5.4.

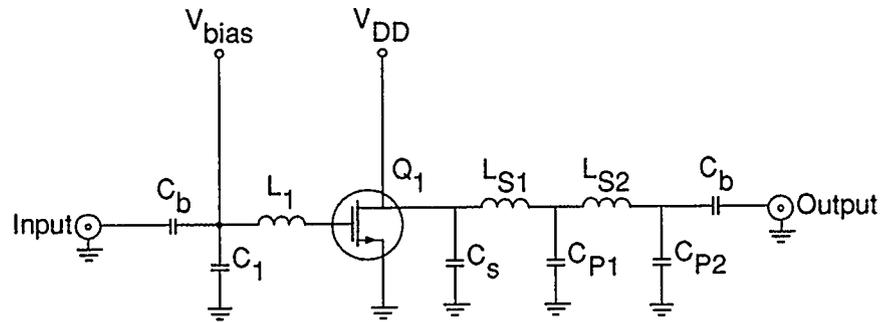


Figure 5.4 Lumped Component Schematic of Class E Amplifier

The switching transistor chosen was the Avantek ATF-44101 2-8 GHz Medium Power Gallium Arsenide FET. This GaAsFET provided a drain to source breakdown voltage of 14 V and a C_{DS} of 1.35 pF making it suitable for low voltage implementation of the 1 GHz Class E design.

The main amplifier was built on Ultralam printed circuit board using a combination of surface mount and microstrip component construction. The input stage of the circuit consists of a bias line and an impedance matching circuit. Negative bias is required to ensure that the depletion type GaAsFET remains off when no RF input signal is present. Failure to bias the device "off" would result in the V_{DD} voltage being shorted to ground and destruction of the GaAsFET.

The multistage output network serves two purposes. As described in chapter two the output stage is designed to ensure that the voltage and current signals are never present at the same time, resulting in high efficiency. The second purpose of the output stage is to match the 50 ohm load to the complex output impedance presented by the GaAsFET. The two shunt capacitors shown in Figure 5.4 were realized using two pairs of open circuit microstrip transmission line stubs. These stubs are a short circuit at the 2nd, 3rd, 4th and 5th harmonics. The two series inductors were also realized by using microstrip transmission lines.

The entire assembly was bolted to a 3/8" thick aluminum heat sink assembly. Use of the Class E amplifier for eight hour periods during experimentation revealed that no heating effects were present.

5.2. Experimental Procedure and Results

Prior to determining overall performance of the system, each component was tested individually to ascertain its operating characteristics.

5.2.1. Main Power Amplifier

The main power amplifier is the most significant component in the system. As such it is necessary to tune the other system components to the main amplifier's operating requirements. The primary operating requirements are frequency and power level of the input signal.

5.2.1.1. Frequency Response

The original design of the Class E amplifier specified an optimized operating frequency of 1 GHz. To confirm the actual optimized operating frequency, the test setup shown in Figure 5.5 was used.

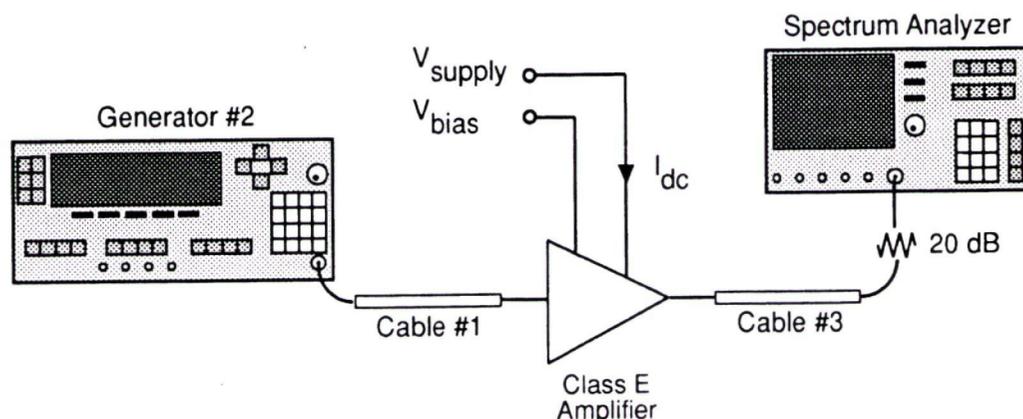


Figure 5.5 Test Setup for Determination of Class E Amplifier's Operating Characteristics

The frequency range chosen for testing was from 950 MHz to 1100 MHz. Attenuation data for Cable #1 and #3 were gathered prior to testing of the Class E amplifier. Supply and bias voltages were provided by the HP6626A System DC Power Supply. The input signal power level was arbitrarily set to +12.65 dBm, which after cable losses resulted in 11.9 dBm entering the amplifier, and Generator #2 was swept through the frequency range producing the efficiency characteristic shown in Figure 5.6.

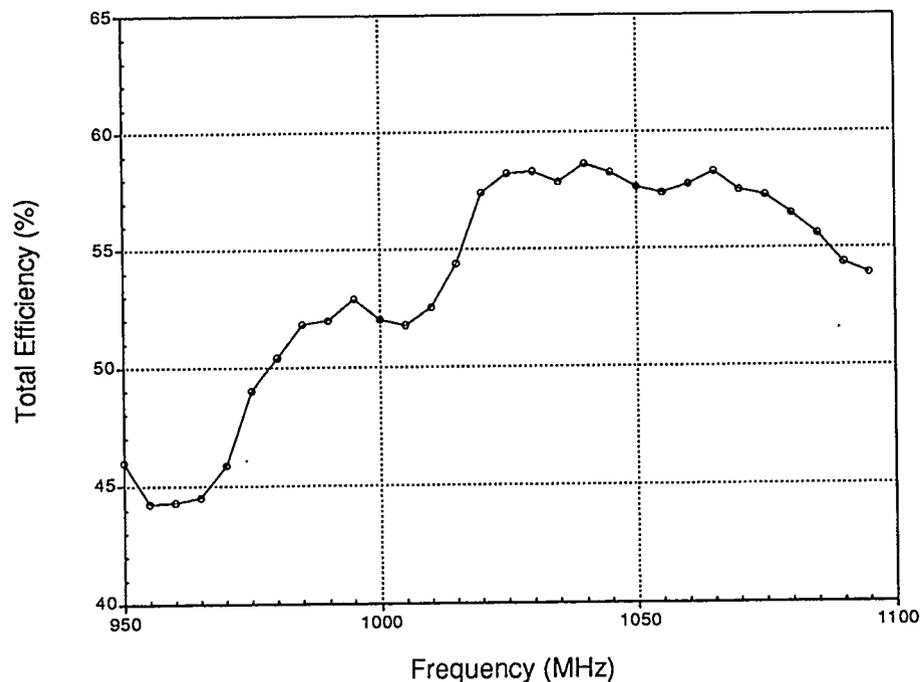


Figure 5.6 Class E Amplifier Total Efficiency vs. Frequency

From the information provided in Figure 5.6 it was observed that the optimum frequency of operation occurs at 1040 MHz.

The next measurement performed on the Class E amplifier was designed to determine the efficiency vs. input power. The same test setup was used. The power provided by Generator #2 was varied from 17.0 dBm downwards and a plot of efficiency versus input power was produced.

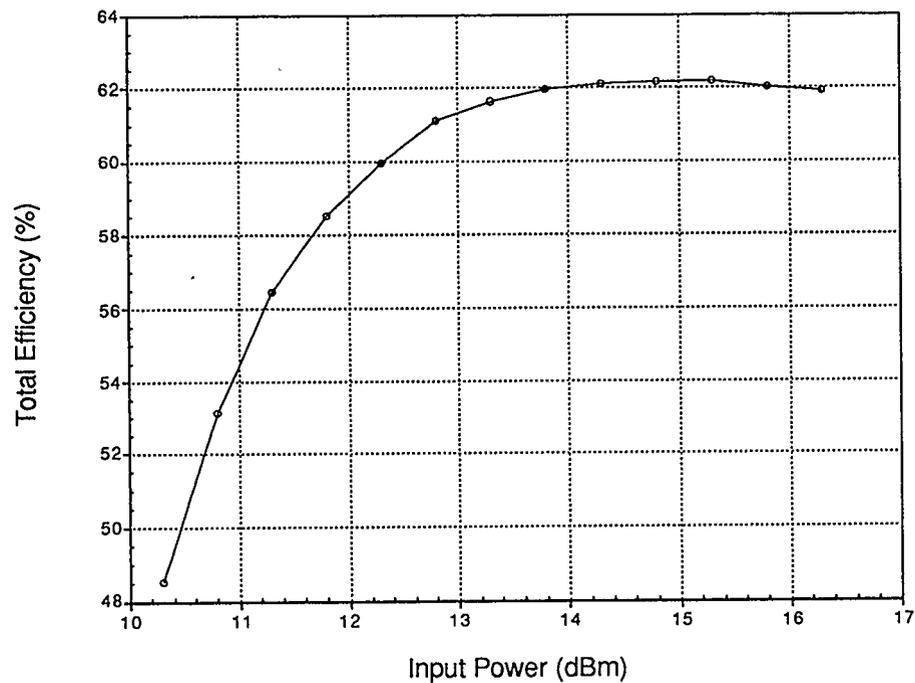


Figure 5.7 Class E Amplifier Total Efficiency vs. Input Power

From the information provided in Figure 5.7 it was determined that a maximum total efficiency of 62.2% is achieved when the input signal level is 15.0 dBm.

5.2.1.2. Linearity and Feedthrough

The next measurement performed on the amplifier determined the linearity of the output to variations in the main power supply, known as the Amplitude

Modulation characteristic. The test setup shown in Figure 5.5 was used. The output power from Generator #2 was adjusted until 16.0 dBm was entering the Class E Amplifier. Variation of the main power supply voltage to the Class E Amplifier produced the result shown in Figure 5.8.

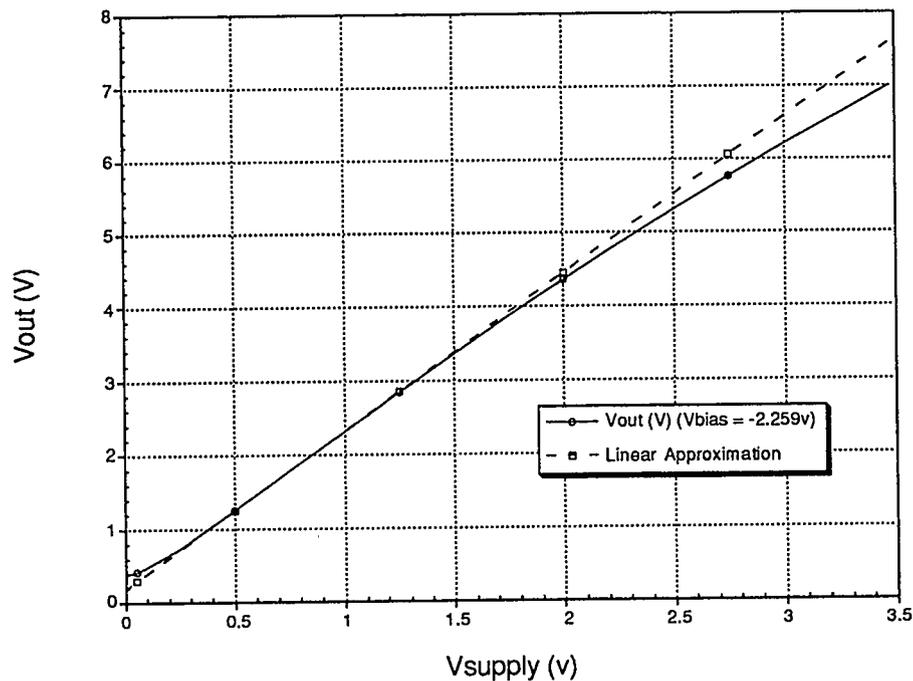


Figure 5.8 Class E Amplifier Amplitude Modulation Characteristic

The results indicate that two areas of concern exist. The first concern is the non-linear behavior of the Class E amplifier. This behavior becomes noticeable at supply voltages above 2.0 V. This non-linearity will result in increased intermodulation distortion products. One method for reducing this effect is through the use of a classical feedback network as described in Chapter 3.

The second concern is the amount of feedthrough signal that occurs at low supply voltages. The amount of feedthrough for this level of input signal is 1.39 dBm. The consequence of this feedthrough is that the minimum distortion for the system will be limited to the minimum value of feedthrough. Variation of the bias voltage provided marginal control over the amount of feedthrough present. However, adjustments of the bias voltage had to remain conservative in order to prevent damage to the amplifier input stage. Bias voltages near zero would result in maximum input signal swings that exceed the gate breakdown voltage and cause device destruction.

The Class E amplifier efficiency versus supply voltage variation is shown in Figure 5.9.

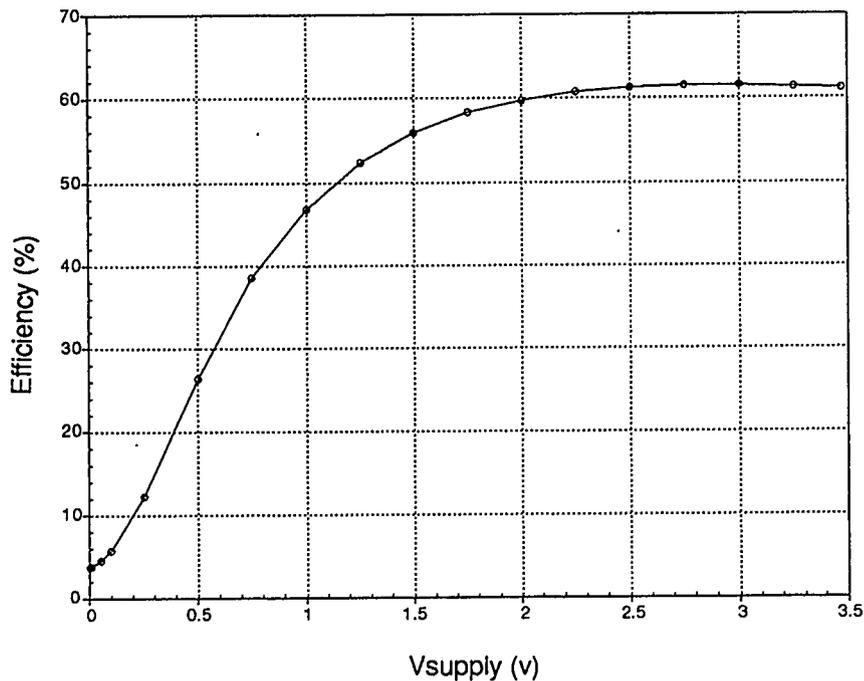


Figure 5.9 Class E Amplifier Total Efficiency vs. Supply Voltage

The efficiency characteristic is good and remains at 60% or better for outputs of 57 % of peak supply voltage (32.5% of peak output power).

Now that the optimum frequency of operation and input power levels have been determined for the Class E amplifier the remainder of the system's components characteristics can be evaluated.

5.2.2. Envelope Detector

The test setup used to determine the response of the envelope detector is shown in Figure 5.10.

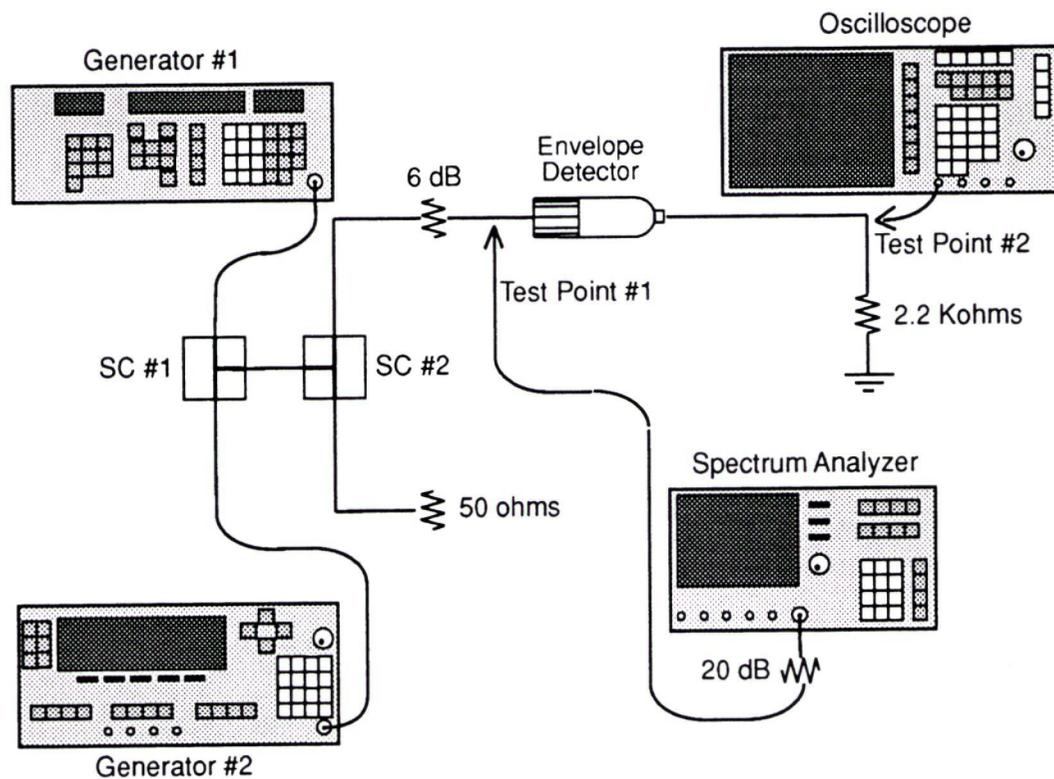


Figure 5.10 Envelope Detector Test Setup

The input signals were first located at 1040.00 MHz and 1040.03 MHz. The output powers of Generator #1 and Generator #2 were adjusted until equal level signals were measured at Test Point #1 (0.17 dBm). The envelope detector

response was captured using the Hewlett Packard HP 54512B Digitizing Oscilloscope and is displayed in Figure 5.11.

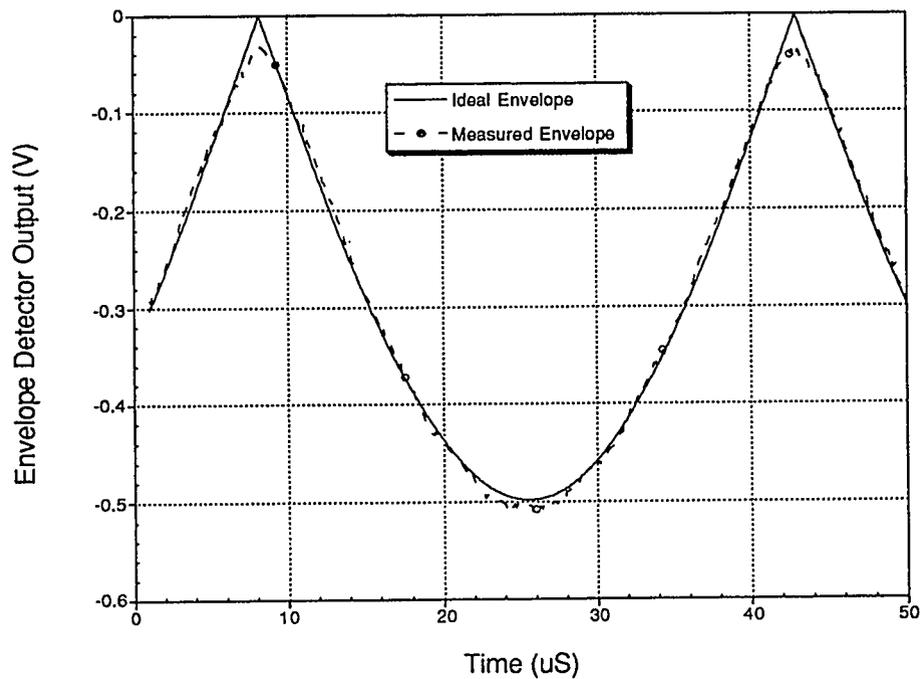


Figure 5.11 Envelope Detector Response with Input Signals at 1040.00 MHz and 1040.03 MHz

The data indicates that the envelope detector is performing very well at these input frequencies when compared to an ideal envelope signal. The floor was measured at -0.03V and the minimum output value was -0.498V.

The separation frequency was then increased to 100 kHz. The envelope detector response varied the floor to -0.036V but otherwise was unchanged from the 30 kHz separation case.

At a separation frequency of 1 MHz the envelope detector response was distorted from the ideal envelope as shown in Figure 5.12.

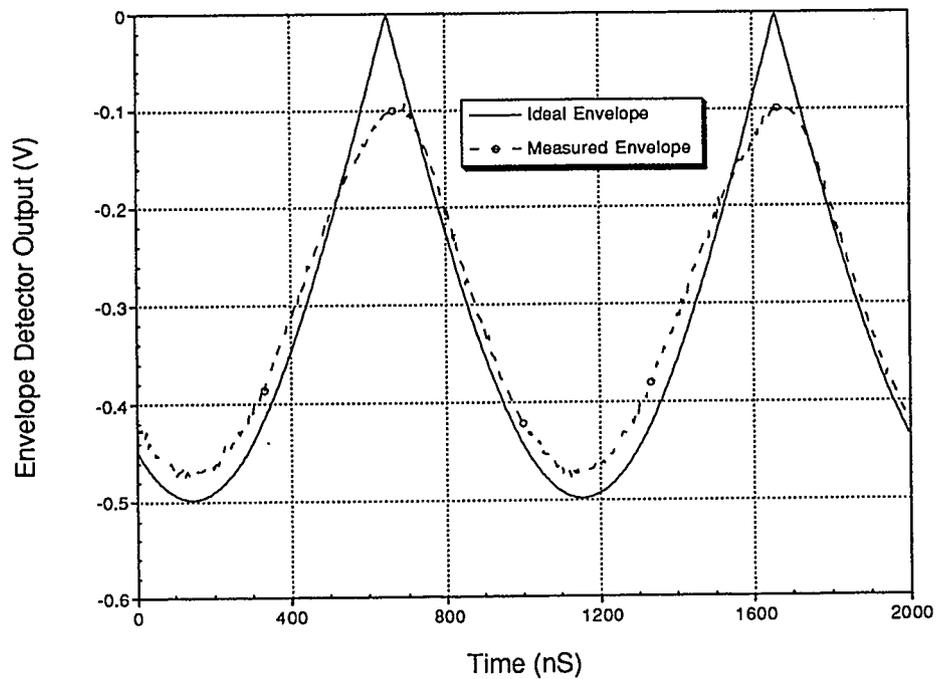


Figure 5.12 Envelope Detector Response with Input Signals at 1040 MHz and 1041 MHz

The results of the performance measurements of the envelope detector indicate that it will introduce negligible distortion when separation frequencies are 30 kHz to 100 kHz. With separation frequencies approaching 1 MHz the distortion produced by the envelope detector is noticeable. Fortunately, the system is intended to operate with signal separation frequencies of 30 kHz and thus this distortion may be avoided.

5.2.3. Modulator

The modulator is one of the most important components of the system, second only to the main power amplifier itself. As such, it must possess the three characteristics of good linearity, wide frequency response and high efficiency. The first characteristic that was examined was the linearity of the modulator.

5.2.3.1. Linearity

The test setup used to measure the linearity of the modulator consisted of a variable voltage supply, dummy load and a voltmeter. The variable voltage supply was used to provide an input signal varying from 0.00V to -0.626V. The dummy load was a resistive 17.8 ohms. The value of the dummy load was derived from the large signal supply voltage and dc current determined earlier during the experiments with the Class E amplifier. The measured linearity of the modulator compared to an ideal linear response is shown in Figure 5.13.

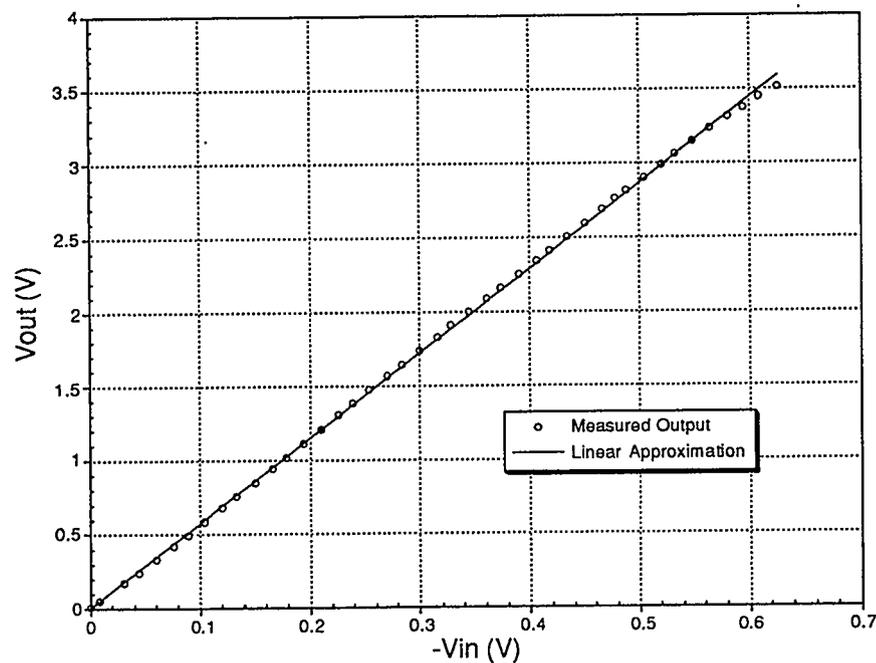


Figure 5.13 Modulator Linearity

A good figure of merit for the modulator is the “Linear Correlation Coefficient” sometimes referred to as the Pearson’s “r”. In this case the modulator demonstrates very good linearity with an r value of 0.9998.. Statistically speaking, this value implies that 99.96% of the errors in the measured data are accounted for by the variance of the measured data. It is therefore safe to imply that the linear response of the modulator will not introduce significant distortion into the system.

5.2.3.2. Frequency Response

The test setup used to determine the bandwidth of the modulator consisted of a Hewlett Packard HP 3314A Function Generator, 17.8 ohm dummy load and the HP54512B Digitizing Oscilloscope. The oscilloscope was used to compare the magnitude and phase of the input and output signals. The measured frequency response of the modulator is compared with a 2nd Order Butterworth low pass filter approximation in Figure 5.14.

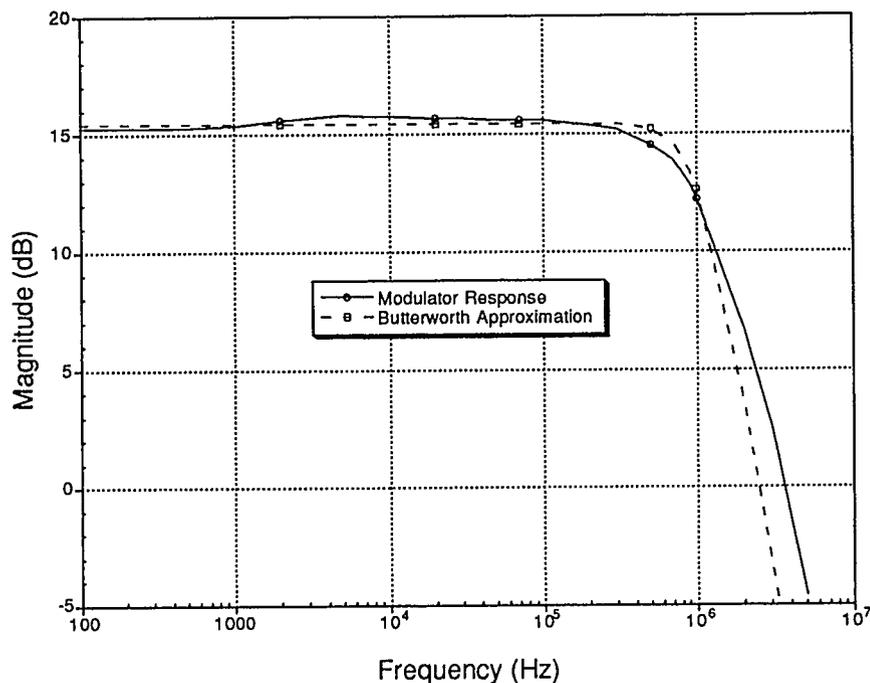


Figure 5.14 Modulator Frequency Response

The measured 3 dB cutoff frequency was 905 kHz. The best fit approximation yielded a cutoff frequency of 1.023 MHz. The measured rolloff approaches 40 dB/decade. In general the modulator does have similar behavior to the 2nd order Butterworth approximation.

Using the measured cutoff frequency of the modulator and the prediction of intermodulation distortion in Figure 4.15 yields the conclusion that in order to maintain the distortion below 30 dB a maximum separation frequency of 226 kHz must not be exceeded.

5.2.3.3. Efficiency

The test setup used to measure the efficiency of the modulator consisted of a variable power supply, dummy load, Hewlett Packard HP 34401A current meter and Fluke 87 voltmeter. The current meter was placed in series with the main dc power to the modulator. During measurements it was discovered that some reduction in output voltage occurred due to the insertion of the current meter. Several different meters were tried, but the HP 34401A caused the minimum change in modulator performance. It was also necessary to disengage the auto ranging feature of the current meter so that current and voltage measurements would not shift to a new level when the meter changed to a different range.

When this modulator was first designed as a system component the primary function was to provide a linear amplification of the envelope signal, little emphasis was placed on the efficiency of the device. The design incorporates an inverting op-amp which requires in excess of 1/4 watts to operate. The reason for choosing the op-amp was simple, the manufacturer provided them free of charge. Since similar devices are available which require only 1/10 of a watt it

was decided to measure the modulator efficiency using the more traditional “collector” efficiency method. Collector efficiency ignores the amount of input power required to drive the amplifier circuit. However, if high gain devices are used the amount of drive power becomes negligible when compared to the total dc power drawn by the device. Since the transistors used in the modulator possess current gains in excess of 100 it is reasonable to assume that the collector efficiency will closely approach the total efficiency under large voltage output conditions. Figure 5.15 displays the collector efficiency of the modulator under varying input signal conditions.

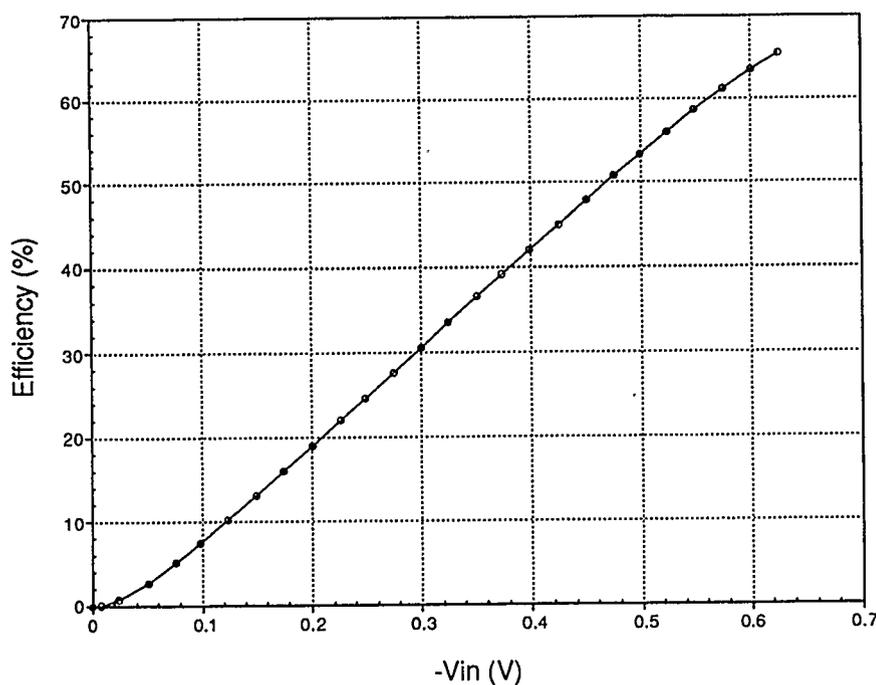


Figure 5.15 Modulator Collector Efficiency

Although the maximum efficiency of the modulator was 65% under full load conditions the near linear reduction of efficiency with output voltage is not

completely desirable. If time had permitted, the construction of a Class S modulator with a flatter efficiency characteristic, i.e., one that maintained a high efficiency value over a wide input signal swing, would have been possible.

5.2.4. Phase Extractor and Delay Measurement

Measurement of the limiting angle of the phase extractor, as well as measurement of the delay between the envelope signal and the phase signal posed a small technical problem. At frequencies of 1 GHz, direct measurement using an oscilloscope is not easily done. However, by mixing the phase signal down to a frequency that was observable on the oscilloscope it was possible to observe both the limiting angle and the delay between the two signals. The test setup shown in Figure 5.16 was used.

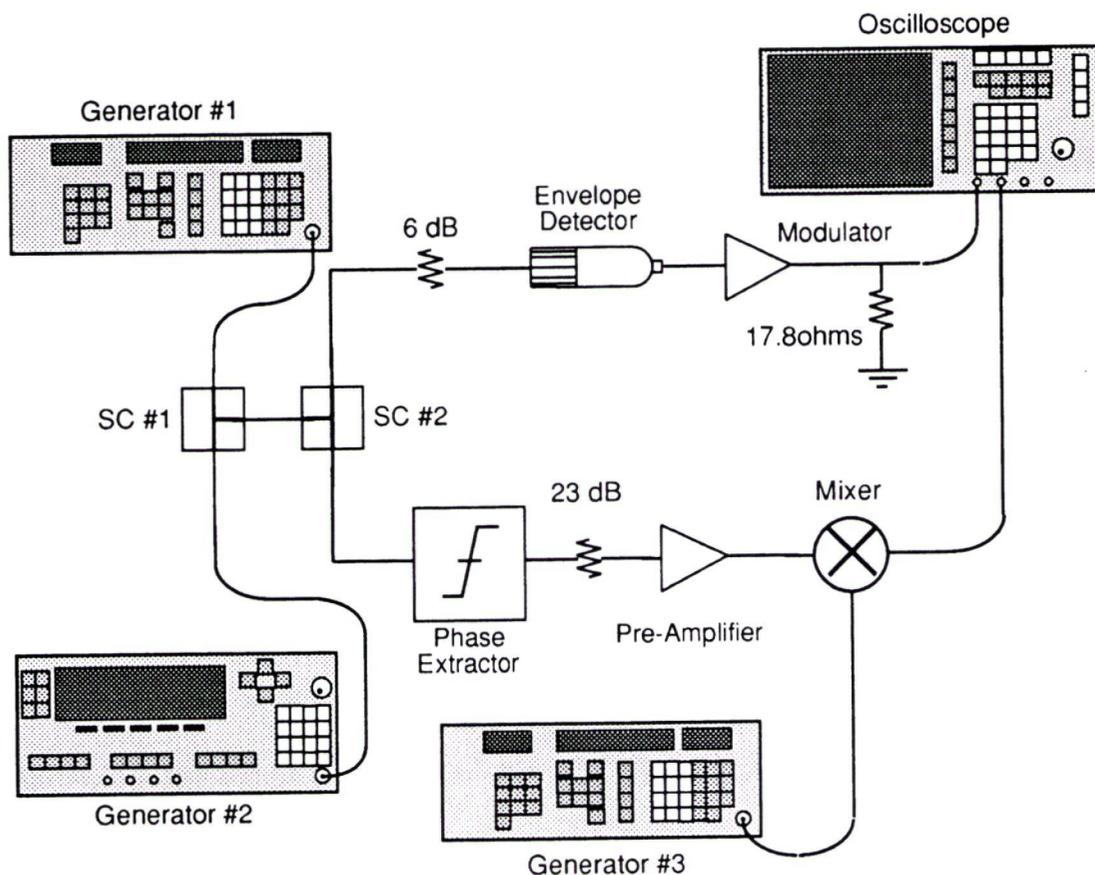


Figure 5.16 Test Setup to Measure Limiting Angle and Signal Delay

Generator #3 was a Hewlett Packard HP 8656B Signal Generator set to 965 MHz. The mixer was a Hewlett Packard HP 8981A-K10 Microwave Downconverter. The output of the mixer was a frequency shifted version of the phase signal centered at 75.015 MHz.

By triggering on the envelope signal it was possible to obtain a stable display that captured both the envelope minimum and the phase signal limiting action. The limiting angle was extracted from the display by measuring the time at which the intersection of the signal maximum / minimum intersected the initial slope of the phase signal (refer to Figure 5.17).

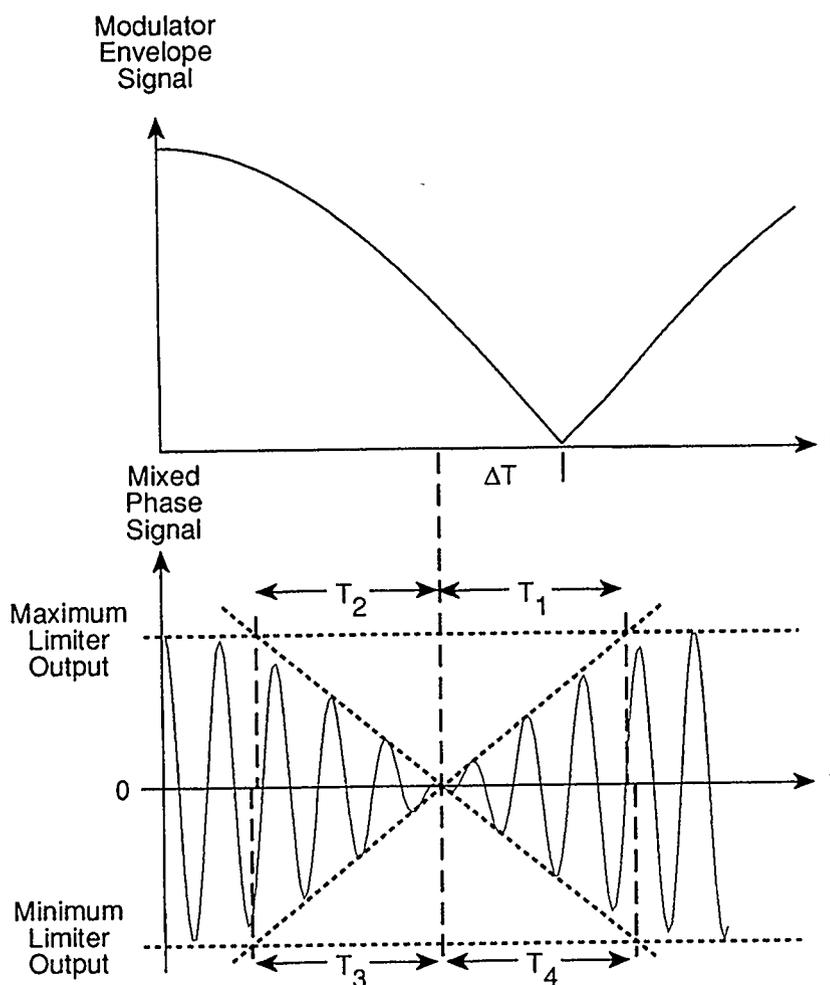


Figure 5.17 Measurement of Limiting Angle and Signal Delay

The four limit times (T_1 through T_4) were averaged resulting in a measured limiting time of 976 μS which converts to a limiting angle of 5.3° . Referencing the simulation data in chapter four (refer to Figure 4.12) a limiting angle of 5.3° should result in intermodulation products at least 55 dB below the fundamental. It is therefore concluded that the limiter performance is very satisfactory and should not introduce significant distortion effects.

The measured delay between the envelope signal and the phase signal was 337 nS which corresponds to a delay angle of 1.8° . Again, referring to the simulation data (refer to Figure 4.14) it is predicted that the actual system delay should produce distortion effects which are at least 60 dB below the fundamental signals.

5.2.5. Reduction of Intermodulation Distortion Products

At this point in the experiment, enough data about the system components has been gathered to make a prediction as to how much the level the intermodulation distortion products will be below the fundamental signals. Assuming a 30 kHz signal separation, 5.3° limiting angle and allowing the natural delay of the Butterworth approximation to determine the signal delay, the level of IMD3 should be approximately 49 dB below the fundamental signals. Unfortunately the actual measured level was 27.5 dB. This discrepancy between the simulation and the actual system is traceable to the feedthrough characteristic of the Class E amplifier. To explain this undesirable characteristic it is useful to investigate the frequency spectrum of the limiter signal entering the Class E amplifier. The frequency spectrum of the limiter output is similar to that shown in Figure 5.18.

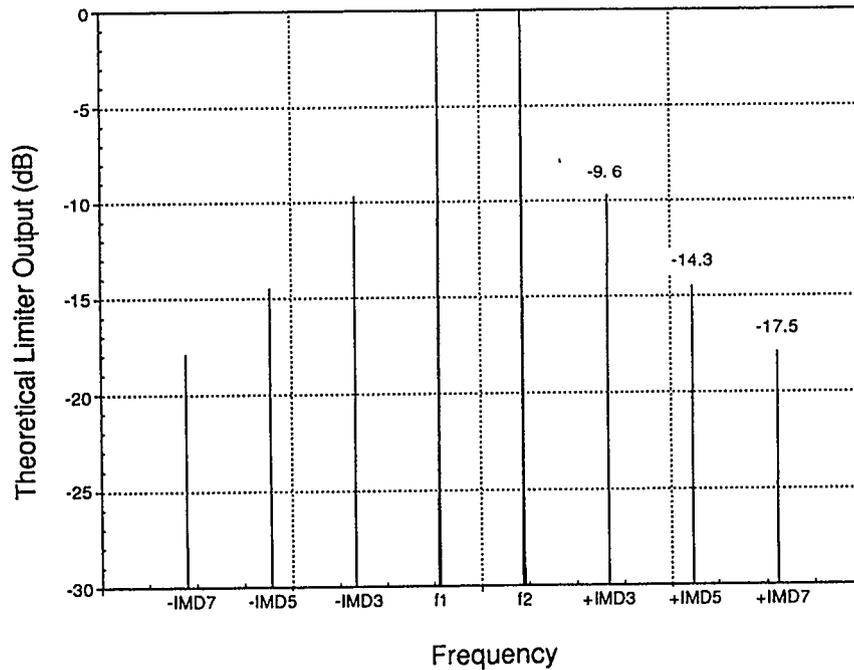


Figure 5.18 Theoretical Limiter Frequency Spectrum (Limiting Angle = 5.3°)

Examination of Figure 5.18 reveals that the signal driving the Class E amplifier also possesses spectral components at the same frequencies that the IMD3, IMD5 and IMD7 components exist. Because of the feedthrough action these spectral components in the limiter signal appear at the output of the Class E amplifier. Due to the voltage divider action, the feedthrough signal has undergone a reduction in magnitude and change in phase. Unfortunately the size of the feedthrough signal may still be significant when compared to the predicted intermodulation distortion products.

Using the linearity measurements for the Class E amplifier (refer Figure 5.8), the size of the spectral components of the limiter signal can be estimated.

This exercise indicates that the IMD3 component will exist at the output of the Class E amplifier at a level of -8.2 dBm. Since the fundamental signal output power is 20.6 dBm the feedthrough distortion will be 28.8 dB below the fundamental signals. Therefore, including the feedthrough effect should result in the intermodulation distortion products approaching a maximum distortion ceiling of 28.8 dB below the fundamental signals.

Of all the system characteristics considered in Chapter Four, the only one which lends itself to manipulation in the actual system is the variation of cutoff frequency to fundamental envelope frequency (i.e. f_c/f_0). This variation was performed by varying the frequency of Generator #2 from 1040.03 MHz to 1041 MHz. The experimental data was used to construct the plot shown in Figure 5.19.

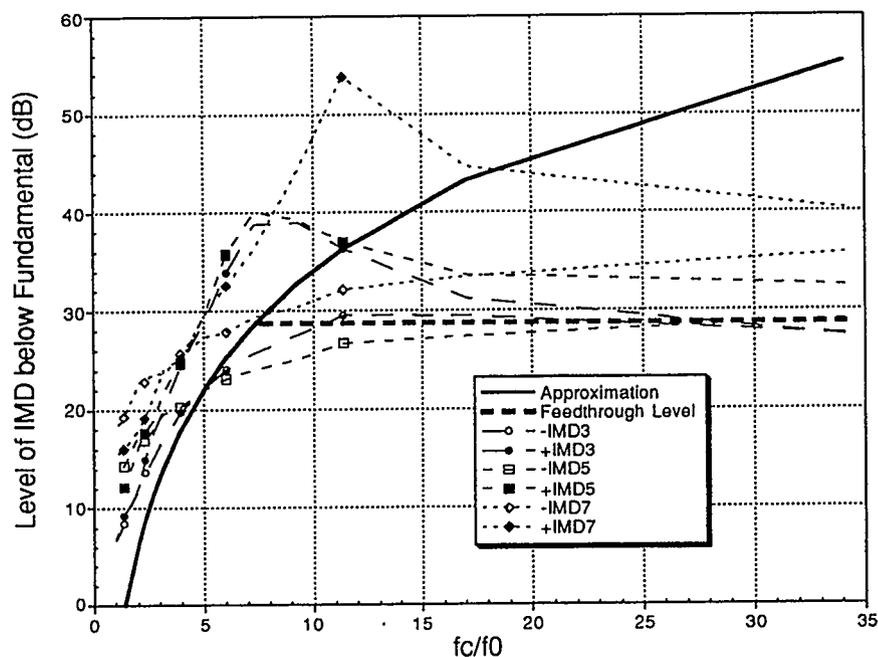


Figure 5.19 Measured Effect of Modulator Cutoff Frequency and Class E Feedthrough Effects on Intermodulation Distortion Products

From Figure 5.19 it is observed that for a f_c/f_0 ratio of five or less the measured data follows the simulation prediction. However, for f_c/f_0 ratios in excess of five the measured data begins to converge with the estimated feedthrough level, thus supporting the hypothesis that feedthrough effects are becoming dominant.

The final performance characteristic of the system is the amount of reduction of intermodulation distortion products with and without the modulator and phase extractor active.

The Class E amplifier's performance is first measured with the phase extractor and modulator removed from the system. The Class E amplifier's main power is provided from a fixed dc power supply. The combined input signals are used to drive the Class E amplifier directly.

In the second case the Class E amplifier performance is measured with the phase extractor and modulator active in the system. Figure 5.20 shows the system performance improvement when the phase extractor and modulator are active in the system.

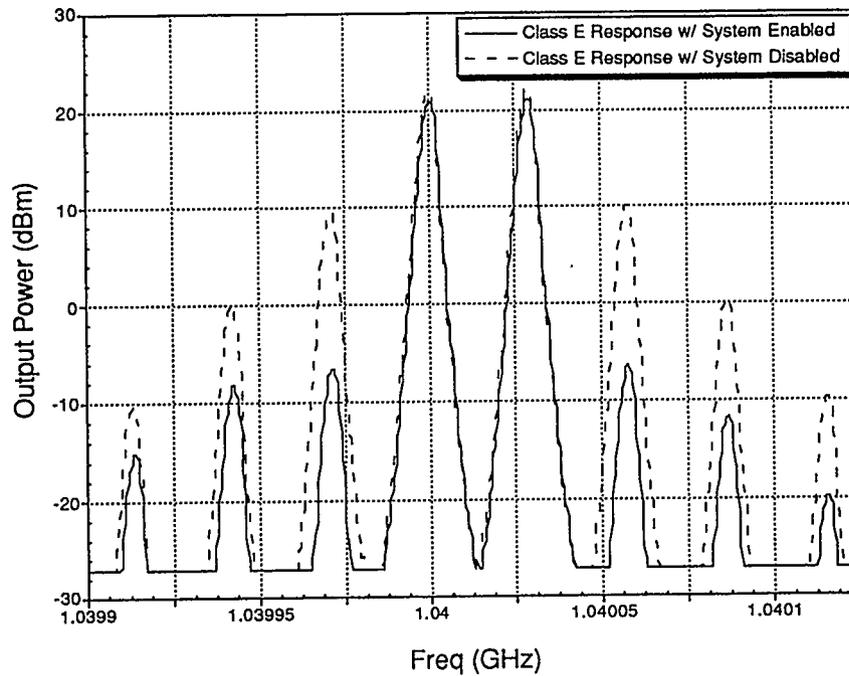


Figure 5.20 Performance measurement with and without Distortion Reduction System Enabled

The results of this final experiment indicate that the distortion reduction system provides an additional 15.1 dB reduction in intermodulation distortion products, achieving a minimum distortion level of 27.5 dB below the fundamental signals.

Chapter Six - Conclusions and Future Work

The experimental results have indicated that the intermodulation distortion products of a highly non-linear amplifier can be reduced through the use of the signal separation and recombination technique known as envelope elimination and restoration.

It has been demonstrated that the analytical method, which uses well known Fourier series techniques, provides useful information that allows prediction of system intermodulation distortion reduction performance. The graphical representation of the analytical results allows easy design of the system by choosing the limiting angle, time delay between envelope and phase signals and cutoff frequency of the modulator.

The prototype circuit successfully demonstrated the ability of envelope elimination and restoration linearization technique to reduce intermodulation distortion products. A 15 dB reduction was achieved which corresponded to a -27.5 dBc distortion level. It was also shown that experimental results asymptotically approach a distortion reduction "ceiling". This inability of the circuit to achieve higher levels of distortion reduction was caused by feedthrough of the phase signal to the output of the main power amplifier. Thus, feedthrough, which is an intrinsic characteristic of the transistor's physical design, begins to play a dominant role in systems operating at 1 GHz or above.

Although the EER system utilizes a simple implementation architecture, the distortion reduction performance should be improved for use in cellular radio systems.

The relatively narrow bandwidth, caused by tuned output filters, of high efficiency amplifiers make them unsuitable for broad band applications, but could be used in narrow band applications such as digital cellular or future PCS modulation schemes.

The total efficiency of the Class E main amplifier exceeded 60 %, over 57 % of the input signal range, and reached a maximum of 62 %. The prototype Class AB modulator used provided a maximum efficiency of 65 %. Thus the total efficiency of the prototype distortion reduction system reaches a maximum of 40.4 %. Use of a practical high efficiency Class S modulator would result in an improved total system efficiency in excess of 54 %. This performance would compare very favorably to existing Class A systems which can only achieve efficiencies approaching 50 %, and then only at maximum output.

Future work would investigate the possibility of introducing a feedthrough neutralization signal at the output of the Class E amplifier, thus reducing the system's sensitivity to transistor feedthrough and allowing continued reduction of the intermodulation distortion products. Introduction of an envelope feedback loop, such as that proposed in Chapter 3 would relax the requirement for a highly linear amplitude modulation characteristic in the main amplifier. Development of a high efficiency Class S modulator with large cutoff frequency would allow a system implementation in situations where multiple channels require efficient amplification, such as in a cellular base station.

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Appendices

The following three subsections are the MathCAD programs used during the analysis of the intermodulation distortion products. The three system parameters investigated were: distortion due to the limiting angle of the phase extractor, distortion due to delay caused by improper synchronization of the envelope and phase information, and distortion due to the cutoff frequency of the modulator.

A.1. Limiter Analysis (limiting angle $e = 57.9$ deg)

Generate the Phase Signal for Input:

Enter Power Level of one signal : $P_{in} := 7$ dBm <=====

$$V_{1dBm} := 0.31622776$$

$$V_{in} := V_{1dBm} \cdot \sqrt{\frac{P_{in}}{20}} = 0.708$$

$$V_P := 2 \cdot V_{in} = 1.416$$

Enter limiter threshold: $V_T := 0.316122$ V <=====

$$A := \frac{V_P}{V_T} = 4.479 \quad N := 1$$

$$e := \text{asin} \left[\frac{N}{A} \right] \cdot \frac{180}{\pi} = 12.901$$

Calculate the Ideal Envelope Fourier Coefficients:

Enter order of series and peak value of envelope:

$$\text{env_order} := 18 \quad B := 3.5 \quad m := 2, 4 \dots \text{env_order}$$

$$b_0 := 2 \cdot \frac{B}{\pi} \quad b_m := 2 \cdot \frac{B}{\pi} \left[\frac{1}{m+1} - \frac{1}{m-1} \right]$$

Calculate the ELGF Fourier Coefficients for the Phase Extractor:

$$\text{elgf_order} := 34 \quad n := 2, 4 \dots \text{elgf_order} \quad j := 2, 4 \dots \text{elgf_order}$$

$$a_0 := \frac{1}{\pi} \left[\frac{2 \cdot e}{N} + \frac{1}{A} \ln \left[\frac{1 + \cos(e)}{1 - \cos(e)} \right] \right] \quad a_0 = 0.453$$

$$a_n := \frac{2}{\pi} \left[\frac{\sin(n \cdot e)}{n \cdot N} + \frac{1}{A} \ln \left[\frac{\cos\left[\frac{e}{2}\right] \cdot \sin\left[\frac{\pi - e}{2}\right]}{\cos\left[\frac{\pi - e}{2}\right] \cdot \sin\left[\frac{e}{2}\right]} \right] + \frac{-4}{A} \sum_j \left[\frac{\cos((j-1) \cdot e)}{j-1} \right] \cdot (j \leq n) \right]$$

Confirm that last coefficient is contributing less than 1% to series:

```
ser1 := env_order, env_order - 2 .. env_order - 8
```

```
ser2 := elgf_order, elgf_order - 2 .. elgf_order - 20
```

$$\text{chk1}_{\text{ser1}} := 100 \cdot \frac{|b_{\text{ser1}}|}{|b_2|}$$

$$\text{chk2}_{\text{ser2}} := 100 \cdot \frac{|a_{\text{ser2}}|}{|a_2|}$$

ser1	chk1
18	0.929
16	1.176
14	1.538
12	2.098
10	3.03

ser2	chk2
34	0.564
32	1.17
30	1.65
28	1.854
26	1.644
24	0.929
22	0.303
20	1.95
18	3.765
16	5.333
14	6.041

Generate Input Signals:

Enter the number of points to represent waveform, freq 1

& freq 2, and number of envelope cycles to generate:

```
num_pts := 4096 f_1 := 1.0000 * 10^9 f_2 := 1.01 * 10^9
num_cycles := 8
```

$$T_{\text{diff}} := \frac{\text{num_cycles}}{f_2 - f_1} \quad T_s := \frac{T_{\text{diff}}}{\text{num_pts}} \quad \omega_0 := 2 \cdot \pi \cdot \begin{bmatrix} f_2 & -f_1 \\ 2 & 1 \end{bmatrix}$$

$$k := 0 \dots \text{num_pts} - 1$$

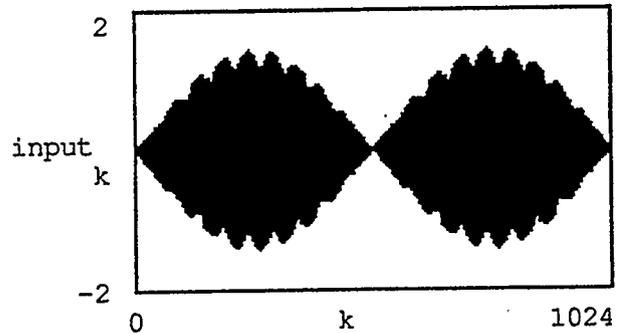
$$\text{env}_k := b_0 + \sum_m b_m \cdot \cos\left[\omega_0 \cdot m \cdot k \cdot T_s\right]$$

$$\text{elgf}_k := a_0 + \sum_n a_n \cdot \cos\left[\omega_0 \cdot n \cdot k \cdot T_s\right]$$

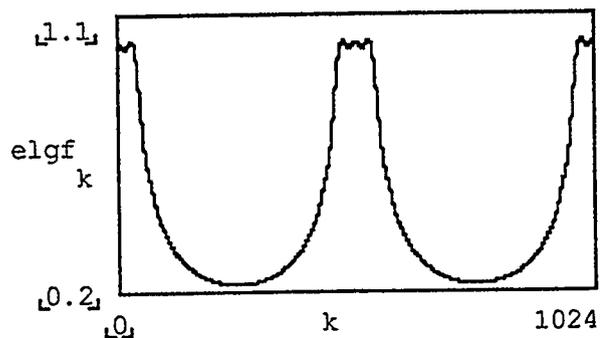
$$\text{in1}_k := V_{\text{in}1} \cdot \sin\left[2 \cdot \pi \cdot f_1 \cdot k \cdot T_s\right] \quad \text{in2}_k := V_{\text{in}2} \cdot \sin\left[2 \cdot \pi \cdot f_2 \cdot k \cdot T_s\right]$$

$$\text{input}_k := \text{in1}_k - \text{in2}_k \quad \text{phase}_k := \text{input}_k \cdot \text{elgf}_k$$

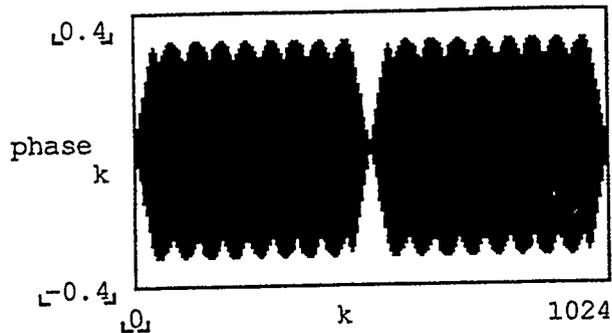
Display Signals:



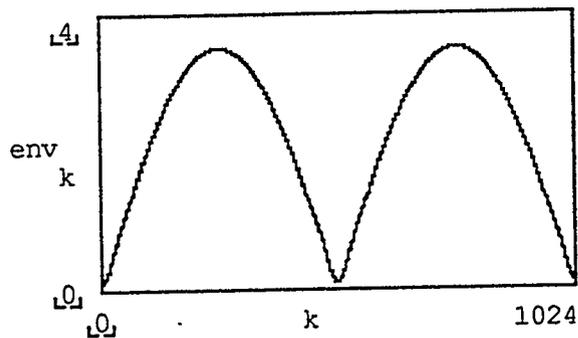
max(input) = 1.411
min(input) = -1.411



max(elgf) = 1.014
min(elgf) = 0.223



max(phase) = 0.317
min(phase) = -0.317



max(env) = 3.506
min(env) = 0.117

Normalize the phase signal before multiplication by the envelope:

norm := max(phase) norm = 0.317

$$\text{phase}_k := \frac{\text{phase}_k}{\text{norm}}$$

max(phase) = 1

min(phase) = -1

Multiply the normalized phase signal by the ideal envelope:

$$\text{main_out}_k := \text{phase}_k \cdot \text{env}_k$$

max(main_out) = 3.487

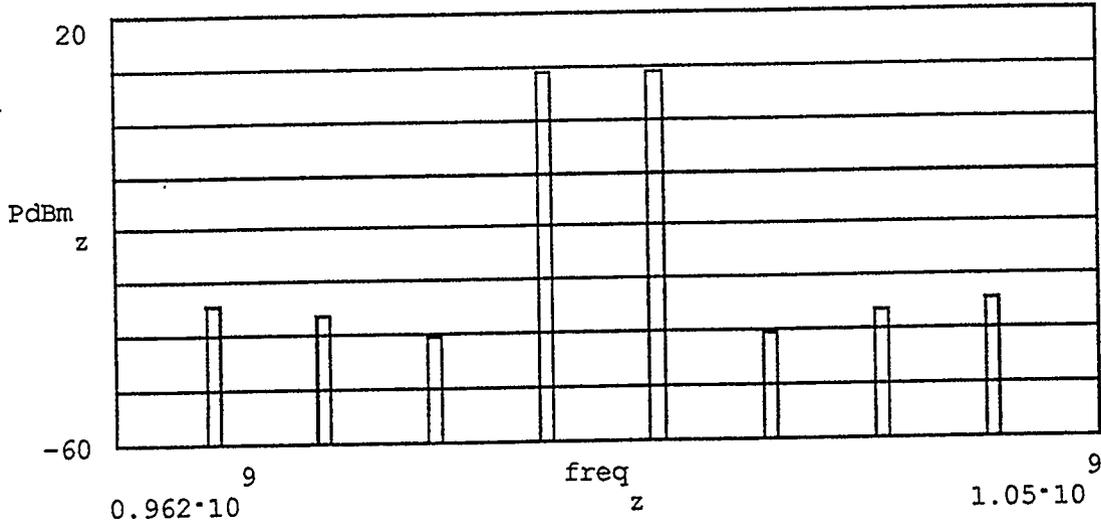
min(main_out) = -3.487

Determine resulting IMD's in frequency spectrum:

$$F := \frac{\text{fft}(\text{main_out})}{\sqrt{\text{num_pts}}} \quad x := \frac{\text{num_pts}}{2} \quad z := 0 \dots x$$

$$\text{freq}_z := \frac{z}{\text{num_pts} \cdot T_s} \quad \text{freq}_1 = 1.25 \cdot 10^6 \quad \text{freq}_x = 2.56 \cdot 10^9$$

$$\text{PdBm}_z := 20 \cdot \log \left[\frac{|F_z|}{V_{1\text{dBm}}} \right]$$



$$d := 776,784 \dots 832$$

$$\text{freq}_d$$

9 10	PdBm d
0.97	-34.231
0.98	-36.468
0.99	-40.451
1	8.814
1.01	8.814
1.02	-40.451
1.03	-36.468
1.04	-34.231

Level of IMD's Below Fundamentals:

$$\text{PdBm}_{800} - \text{PdBm}_{776} = 43.045 \quad \text{-IMD7}$$

$$\text{PdBm}_{800} - \text{PdBm}_{784} = 45.282 \quad \text{-IMD5}$$

$$\text{PdBm}_{800} - \text{PdBm}_{792} = 49.265 \quad \text{-IMD3}$$

$$\text{PdBm}_{800} = 8.814 \quad \text{P1}$$

$$\text{PdBm}_{808} = 8.814 \quad \text{P2}$$

$$\text{PdBm}_{808} - \text{PdBm}_{816} = 49.265 \quad \text{+IMD3}$$

$$\text{PdBm}_{808} - \text{PdBm}_{824} = 45.282 \quad \text{+IMD5}$$

$$\text{PdBm}_{808} - \text{PdBm}_{832} = 43.045 \quad \text{-IMD7}$$

A.2. Delay Analysis (delay = 6 deg, e = 0.9 deg)

Generate the Phase Signal for Input:

Enter Power Level of one signal : $P_{in} := 7$ dBm <=====

$$V_{1dBm} := 0.31622776$$

$$V_{in} := V_{1dBm} \cdot 10^{\frac{P_{in}}{20}} = 0.708$$

$$V_P := 2 \cdot V_{in} = 1.416$$

Enter limiter threshold: $V_T := 0.022241$ V <=====

$$A := \frac{V_P}{V_T} = 63.661 \quad N := 1$$

$$e := \text{asin} \left[\frac{N}{A} \right] \cdot \frac{180}{\pi} = 0.9$$

Calculate the Ideal Envelope Fourier Coefficients:

Enter order of series and peak value of envelope:

$$\text{env_order} := 18 \quad B := 3.5 \quad m := 2, 4 \dots \text{env_order}$$

$$b_0 := 2 \cdot \frac{B}{\pi} \quad b_m := 2 \cdot \frac{B}{\pi} \left[\frac{1}{m+1} - \frac{1}{m-1} \right]$$

Calculate the ELGF Fourier Coefficients for the Phase Extractor:

$$\text{elgf_order} := 126 \quad n := 2, 4 \dots \text{elgf_order} \quad j := 2, 4 \dots \text{elgf_order}$$

$$a_0 := \frac{1}{\pi} \left[\frac{2 \cdot e}{N} + \frac{1}{A} \ln \left[\frac{1 + \cos(e)}{1 - \cos(e)} \right] \right] \quad a_0 = 0.058$$

$$a_n := \frac{2}{\pi} \left[\frac{\sin(n \cdot e)}{n \cdot N} + \frac{1}{A} \ln \left[\frac{\cos\left[\frac{e}{2}\right] \cdot \sin\left[\frac{\pi - e}{2}\right]}{\cos\left[\frac{\pi - e}{2}\right] \cdot \sin\left[\frac{e}{2}\right]} \right] \right] + \frac{-4}{A} \left[\sum_j \left[\frac{\cos((j-1) \cdot e)}{j-1} \right] \cdot (j \leq n) \right]$$

Confirm that last coefficient is contributing less than 1% to series:

```
ser1 := env_order, env_order - 2 .. env_order - 8
ser2 := elgf_order, elgf_order - 2 .. elgf_order - 20
```

$$\text{chk1}_{\text{ser1}} := 100 \cdot \frac{|b_{\text{ser1}}|}{|b_2|} \qquad \text{chk2}_{\text{ser2}} := 100 \cdot \frac{|a_{\text{ser2}}|}{|a_2|}$$

ser1	chk1
18	0.929
16	1.176
14	1.538
12	2.098
10	3.03

ser2	chk2
126	0.947
124	1.143
122	1.348
120	1.562
118	1.785
116	2.018
114	2.262
112	2.515
110	2.78
108	3.056
106	3.343

Generate Input Signals:

Enter the number of points to represent waveform, freq 1
& freq 2, and number of envelope cycles and time delay (deg)
to generate input signals:

```
num_pts := 4096 f_1 := 1.0000 * 10^9 f_2 := 1.01 * 10^9
num_cycles := 8 env_delay := 6
```

$$T_{\text{diff}} := \frac{\text{num_cycles}}{f_2 - f_1} \quad T_s := \frac{T_{\text{diff}}}{\text{num_pts}} \quad \omega_0 := 2 \cdot \pi \cdot \left[\frac{f_2 - f_1}{2} \right]$$

$$k := 0 \dots \text{num_pts} - 1 \quad \tau := \text{env_delay} \cdot \frac{\pi}{180}$$

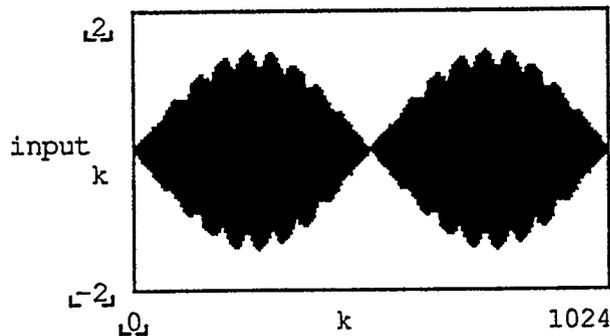
$$\text{env}_k := b_0 + \sum_m b_m \cdot \cos \left[\omega_0 \cdot m \cdot k \cdot T_s + \tau \cdot m \right]$$

$$\text{elgf}_k := a_0 + \sum_n a_n \cdot \cos \left[\omega_0 \cdot n \cdot k \cdot T_s \right]$$

$$\text{in1}_k := V_{\text{in}} \cdot \sin \left[2 \cdot \pi \cdot f_1 \cdot k \cdot T_s \right] \quad \text{in2}_k := V_{\text{in}} \cdot \sin \left[2 \cdot \pi \cdot f_2 \cdot k \cdot T_s \right]$$

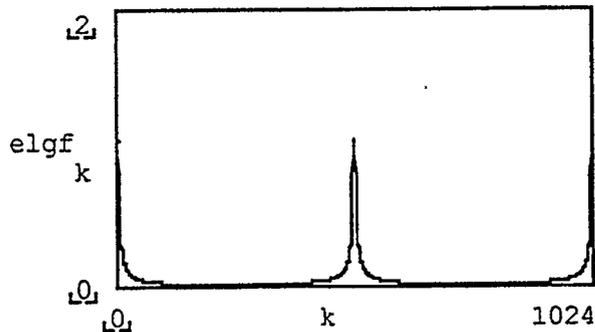
$$\text{input}_k := \text{in1}_k - \text{in2}_k \quad \text{phase}_k := \text{input}_k \cdot \text{elgf}_k$$

Display Signals:



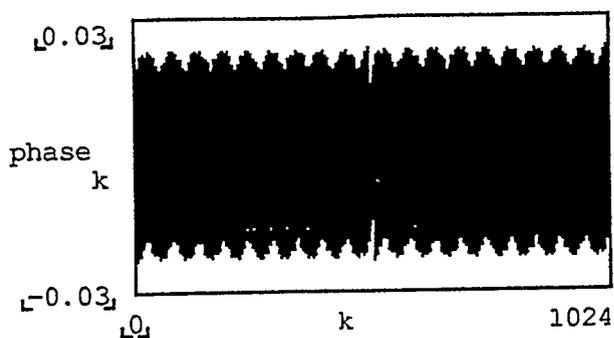
$$\max(\text{input}) = 1.411$$

$$\min(\text{input}) = -1.411$$



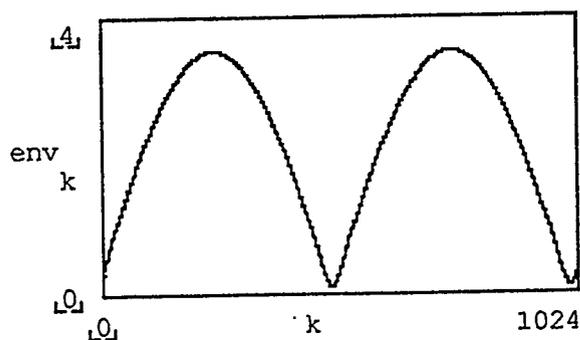
$$\max(\text{elgf}) = 1.062$$

$$\min(\text{elgf}) = 0.015$$



`max(phase) = 0.023`

`min(phase) = -0.023`



`max(env) = 3.506`

`min(env) = 0.117`

Normalize the phase signal before multiplication by the envelope:

`norm := max(phase)`

`norm = 0.023`

$$\text{phase}_k := \frac{\text{phase}_k}{\text{norm}}$$

`max(phase) = 1`

`min(phase) = -1`

Multiply the normalized phase signal by the ideal envelope:

$$\text{main_out}_k := \text{phase}_k \cdot \text{env}_k$$

`max(main_out) = 3.355`

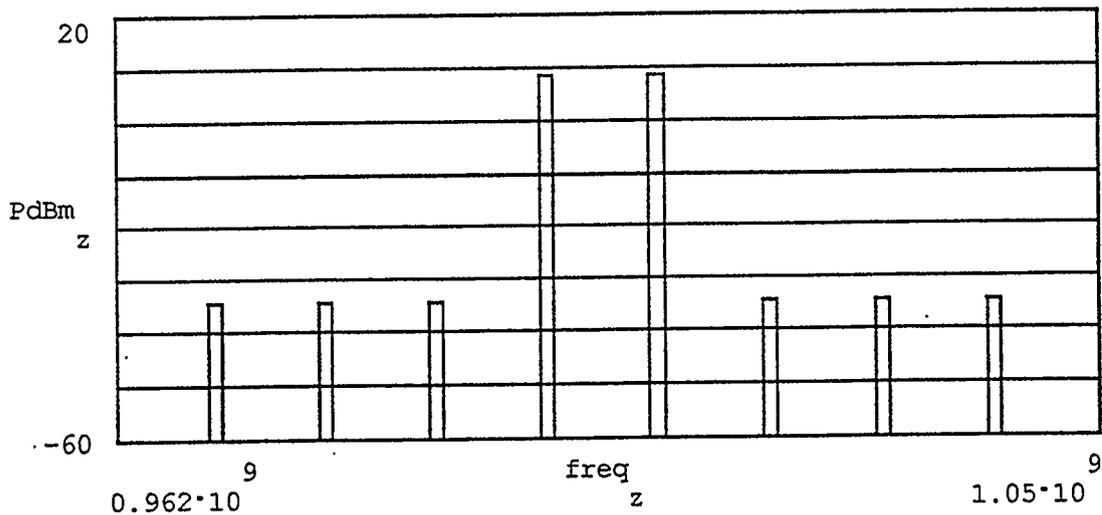
`min(main_out) = -3.352`

Determine resulting IMD's in frequency spectrum:

$$F := \frac{\text{fft}(\text{main_out})}{\sqrt{\text{num_pts}}} \quad x := \frac{\text{num_pts}}{2} \quad z := 0 \dots x$$

$$\text{freq}_z := \frac{z}{\text{num_pts} \cdot T_s} \quad \text{freq}_1 = 1.25 \cdot 10^6 \quad \text{freq}_x = 2.56 \cdot 10^9$$

$$\text{PdBm}_z := 20 \cdot \log \left[\frac{|F_z|}{V_{1\text{dBm}}} \right]$$



$$d := 776,784 \dots 832$$

$$\frac{\text{freq}_d}{d}$$

9 10	PdBm d
0.97	-34.386
0.98	-34.369
0.99	-34.354
1	8.414
1.01	8.414
1.02	-34.354
1.03	-34.369
1.04	-34.386

Level of IMD's Below Fundamentals:

PdBm 800	- PdBm 776	= 42.8	-IMD7
PdBm 800	- PdBm 784	= 42.782	-IMD5
PdBm 800	- PdBm 792	= 42.768	-IMD3
	PdBm 800	= 8.414	P1
	PdBm 808	= 8.414	P2
PdBm 808	- PdBm 816	= 42.768	+IMD3
PdBm 808	- PdBm 824	= 42.782	+IMD5
PdBm 808	- PdBm 832	= 42.8	-IMD7

A.3. Frequency Analysis (cutoff freq = 6.25 fundamental)

Generate the Phase Signal for Input:

Enter Power Level of one signal : $P_{in} := 7$ dBm <=====

$$V_{1dBm} := 0.31622776$$

$$V_{in} := V_{1dBm} \cdot \frac{P_{in}}{20}^{-10} = 0.708$$

$$V_P := 2 \cdot V_{in} = 1.416$$

Enter limiter threshold: $V_T := 0.022241$ V <=====

$$A := \frac{V_P}{V_T} = 63.661 \quad N := 1$$

$$e := \text{asin} \left[\frac{N}{A} \right] \quad e^{-\frac{180}{\pi}} = 0.9$$

Calculate the Ideal Envelope Fourier Coefficients:

Enter order of series and peak value of envelope:

$$\text{env_order} := 18 \quad B := 3.5 \quad m := 2, 4 \dots \text{env_order}$$

$$b_0 := 2 \cdot \frac{B}{\pi} \quad b_m := 2 \cdot \frac{B}{\pi} \left[\frac{1}{m+1} - \frac{1}{m-1} \right]$$

Calculate the ELGF Fourier Coefficients for the Phase Extractor:

$$\text{elgf_order} := 126 \quad n := 2, 4 \dots \text{elgf_order} \quad j := 2, 4 \dots \text{elgf_order}$$

$$a_0 := \frac{1}{\pi} \left[\frac{2 \cdot e}{N} + \frac{1}{A} \ln \left[\frac{1 + \cos(e)}{1 - \cos(e)} \right] \right] \quad a_0 = 0.058$$

$$a_n := \frac{2}{\pi} \left[2 \cdot \frac{\sin(n \cdot e)}{n \cdot N} + \frac{1}{A} \ln \left[\frac{\cos\left[\frac{e}{2}\right] \cdot \sin\left[\frac{\pi - e}{2}\right]}{\cos\left[\frac{\pi - e}{2}\right] \cdot \sin\left[\frac{e}{2}\right]} \right] \right] + \frac{-4}{A} \left[\sum_j \left[\frac{\cos((j-1) \cdot e)}{j-1} \right] \cdot (j \leq n) \right] \dots$$

Confirm that last coefficient is contributing less than 1% to series:

```
ser1 := env_order, env_order - 2 .. env_order - 8
```

```
ser2 := elgf_order, elgf_order - 2 .. elgf_order - 20
```

$$\text{chk1}_{\text{ser1}} := 100 \cdot \frac{\left| \frac{b}{\text{ser1}} \right|}{\left| \frac{b}{2} \right|}$$

$$\text{chk2}_{\text{ser2}} := 100 \cdot \frac{\left| \frac{a}{\text{ser2}} \right|}{\left| \frac{a}{2} \right|}$$

ser1	chk1
18	0.929
16	1.176
14	1.538
12	2.098
10	3.03

ser2	chk2
126	0.947
124	1.143
122	1.348
120	1.562
118	1.785
116	2.018
114	2.262
112	2.515
110	2.78
108	3.056
106	3.343

Generate Input Signals:

Enter the number of points to represent waveform, freq 1

& freq 2, and number of envelope cycles to generate

input signals:

```
num_pts := 4096 f1 := 1.0000*109 f2 := 1.01*109
num_cycles := 8
```

$$T_{\text{diff}} := \frac{\text{num_cycles}}{f_2 - f_1} \quad T_s := \frac{T_{\text{diff}}}{\text{num_pts}} \quad \omega_0 := 2 \cdot \pi \cdot \begin{bmatrix} f_2 & -f_1 \\ 2 & 1 \end{bmatrix}$$

$$k := 0 \dots \text{num_pts} - 1$$

$$\text{env}_k := b_0 + \sum_m b_m \cdot \cos[\omega_0 \cdot m \cdot k \cdot T_s]$$

$$\text{elgf}_k := a_0 + \sum_n a_n \cdot \cos[\omega_0 \cdot n \cdot k \cdot T_s]$$

$$\text{in1}_k := V_{\text{in}} \cdot \sin[2 \cdot \pi \cdot f_1 \cdot k \cdot T_s] \quad \text{in2}_k := V_{\text{in}} \cdot \sin[2 \cdot \pi \cdot f_2 \cdot k \cdot T_s]$$

$$\text{input}_k := \text{in1}_k - \text{in2}_k \quad \text{phase}_k := \text{input}_k \cdot \text{elgf}_k$$

Transform Envelope to Frequency Domain for Filtering:

$$\text{ENV} := \frac{\text{fft}(\text{env})}{\sqrt{\text{num_pts}}}$$

Define frequency Response of the Modulator:

$$f_0 := \frac{\omega_0}{2 \cdot \pi} \quad f_0 = 5 \cdot 10^6$$

$$x := \frac{\text{num_pts}}{2} \quad z := 0 \dots x \quad \text{freq}_z := \frac{z}{\text{num_pts} \cdot T_s}$$

$$j := \sqrt{-1} \quad s_z := j \cdot \text{freq}_z \quad \delta := 1 \cdot 10^{-21}$$

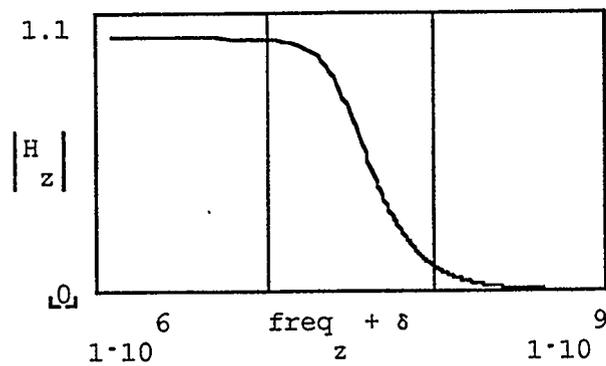
Enter cutoff frequency relative to the fundamental and filter coefficients:

$$\Omega_0 := 6.25 \cdot f_0 \quad b_0 := 1.00237729 \quad b_1 := 1.415893565 \quad b_2 := 1$$

$$H_z := \frac{b_0}{b_2 \cdot \left[\frac{s}{z} \right]^2 + b_1 \cdot \left[\frac{s}{z} \right] + b_0}$$

Filter Envelope:

$$ENV_z := ENV_z \cdot H_z$$



Convert filtered envelope to the time domain for further processing:

$$env := \text{ifft}(ENV) \cdot \sqrt{\text{num_pts}}$$

Normalize the phase signal before multiplication by the envelope:

$$\text{norm} := \max(\text{phase}) \qquad \text{norm} = 0.023$$

$$\text{phase}_k := \frac{\text{phase}_k}{\text{norm}}$$

$$\max(\text{phase}) = 1$$

$$\min(\text{phase}) = -1$$

Multiply the normalized phase signal by the ideal envelope:

$$\text{main_out}_k := \text{phase}_k \cdot \text{env}_k$$

$$\max(\text{main_out}) = 3.329$$

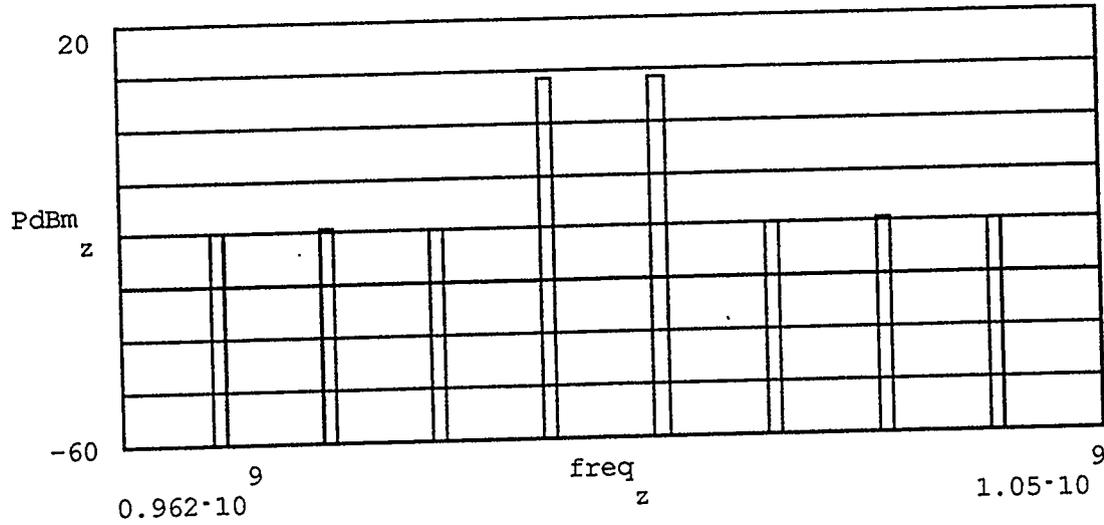
$$\min(\text{main_out}) = -3.38$$

Determine resulting IMD's in frequency spectrum:

$$F := \frac{\text{fft}(\text{main_out})}{\sqrt{\text{num_pts}}} \quad x := \frac{\text{num_pts}}{2} \quad z := 0 \dots x$$

$$\text{freq}_z := \frac{z}{\text{num_pts} \cdot T} \quad \text{freq}_1 = 1.25 \cdot 10^6 \quad \text{freq}_x = 2.56 \cdot 10^9$$

$$\text{PdBm}_z := 20 \cdot \log \left[\frac{|F_z|}{V_{1\text{dBm}}} \right]$$



d := 776,784 ..832

freq
d

9 10	PdBm d
0.97	-19.927
0.98	-19.149
0.99	-19.76
1	8.356
1.01	8.356
1.02	-19.76
1.03	-19.149
1.04	-19.927

Level of IMD's Below Fundamentals:

PdBm 800	-	PdBm 776	= 28.283	-IMD7
PdBm 800	-	PdBm 784	= 27.505	-IMD5
PdBm 800	-	PdBm 792	= 28.116	-IMD3
		PdBm 800	= 8.356	P 1
		PdBm 808	= 8.356	P 2
PdBm 808	-	PdBm 816	= 28.116	+IMD3
PdBm 808	-	PdBm 824	= 27.505	+IMD5
PdBm 808	-	PdBm 832	= 28.283	-IMD7