THE UNIVERSITY OF CALGARY

A PRECISION
DATA ACQUISITION SYSTEM

by

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ABSTRACT

The design and implementation of a precision analog-to-digital converter (ADC) circuit is presented in this thesis. The circuit uses the concepts of pulse width modulation and charge equalization to convert an analog voltage into a rectangular wave with a duty cycle proportional to the input voltage.

A simplified analog pulse width modulator (PWM) is presented to illustrate the operation and analog applications of the circuit. A high frequency clock synchronized PWM (SPWM) ADC is then presented. The SPWM ADC is implemented with discrete components and tested. Experimental results indicate that the converter is capable of achieving an overall accuracy of 4 ppm. Analysis suggests that an overall accuracy of 1 ppm (or 20 bits) can be achieved by using digital correction. An examination of noise limitations for the SPWM is presented together with measurements of the resolution of the converter. These measurements indicate that the SPWM ADC is capable of resolving approximately 50 nanovolts.

The SPWM is interfaced to a microcontroller-based data acquisition unit (DAU) to realize a compact, versatile system useful in several instrumentation applications. The development of the DAU is described in detail in this thesis.

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DEDICATION

To Wanda

For all her support and patience

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LIST OF SYMBOLS

A_d	Operational Amplifier differential gain
A_N	Nulling amplifier gain
A_M	Main amplifier gain
B	Bandwidth
C	Capacitance
$CMRR$	Operational Amplifier common-mode rejection ratio
$\overline{E_{no}}$	Root-mean-square output noise voltage
e_j	Noise voltage source
f	Frequency
f_{CH}	Operational amplifier auto-zeroing clock frequency
f_R	PWM operating frequency
$H_j(f)$	Analog transfer function
i_k	Noise current source
I_{B-}	Operational amplifier negative input bias current
m	Number of PWM periods within a single conversion period
n	Number of clock periods within a single PWM period
N	SPWM output count

LIST OF SYMBOLS (Continued)

$R_N(l)$	Auto-correlation function
R	Resistance
r_d	Difference between high and low output resistance of logic gate
r_h	Output resistance of logic gate in high state
r_l	Output resistance of logic gate in low state
S_e	Noise voltage spectral density
S_i	Noise current spectral density
T	Temperature
T_c	SPWM high frequency clock period
$T_{convert}$	ADC conversion time
T_p	PWM output pulse width
T_o	PWM period
T_{high}	Time that SPWM output is high
t_d	Difference between SPWM output rise and fall times
t_F	SPWM output fall time
t_R	SPWM output rise time
V	Large signal voltage

LIST OF SYMBOLS (Continued)

V_{os}	Operational amplifier offset voltage
V_{out}	Output voltage
V_R	PWM reset square wave
V_{ref}	Reference or supply voltage
V_t	PWM input voltage
V_{th}	Logic gate switching threshold voltage
v	Small signal voltage
v_n	Amplifier null adjustment input
v_{noise}	Nulling amplifier input referred noise voltage
$Z_K(f)$	Analog transfer impedance
ε	Error
σ	Standard deviation or rms error
μ	Mean value
ω	Angular frequency

CHAPTER 1

INTRODUCTION

Analog-to-digital converters (ADC's) are a fundamental component of data acquisition and control systems. An ADC converts an analog voltage (or current) into a digital representation of the input value. The digital value can then be processed to provide information about a physical variable being measured. In addition, the digital value can be transmitted or mathematically manipulated without loss of information.

In low speed instrumentation applications, integrating or charge balancing converters are normally used. Integrating converters use the averaging property of integration to measure the average value of an input voltage (or current) over a measured time interval. This type of converter has the advantages of simplicity and high accuracy at low cost when compared to high speed conversion methods such as successive approximation. Other advantages of integrating converters include high input impedance, high noise rejection, an inherently monotonic output (no missing output codes), and they can usually be constructed without the require-

ment of using precision components[1].

Integrating converters are implemented using a number of different methods. In general, however, integrating techniques use the principles of integration and charge equalization and consist of an active integrator and a reset circuit which controls the charging of the integrator. Some of these techniques are described briefly below.

The most popular integrating technique employed in commercial ADC's is called dual-slope integration. In this method, the analog input charges a capacitor for a fixed time interval. The capacitor is then discharged by a constant current. The discharge time will be proportional to the analog input and by enabling a counter during the discharge time, it is possible to obtain an output count proportional to the input level. Dual-slope converters have the advantages of simplicity and moderate requirements on component stability. Disadvantages of this method include a variable conversion time, inherently unipolar operation, and poor resolution near the zero level[1].

A second popular technique, called quantized feedback[1], uses digital circuitry to feed quantized units of charge back to the integrating capacitor in response to the sampled state of a comparator. Unlike dual-slope converters, this method is characterized by a fixed conversion time, inherently bipolar operation, and a zero level which occurs naturally between minus full scale and plus full scale[1]. The

major disadvantage of the quantized feedback method is its complexity in comparison to other integration techniques.

A voltage-to-frequency converter (VFC) can also be used to realize an analog-to-digital converter[2]. Most VFC's use a charge balancing scheme to convert a voltage into a pulse train with a frequency proportional to the input voltage. Frequency or period measurement using a high frequency clock can then produce a digital representation of the input. VFC's are particularly useful for transmitting results digitally over cables or when the actual output frequency is desired. The main disadvantage of VFC's in ADC implementations is that they have a conversion time which is a function of the input voltage.

A pulse width modulator (PWM) uses VFC principles to convert a voltage into a pulse train with a constant period and a duty cycle or pulse-width which is proportional to the input voltage. Pulse width modulation has many of the useful characteristics of a VFC and, as an added advantage in ADC implementations, the conversion time can be fixed.

The subject of this thesis involves the implementation of a precision pulse width modulator (PWM) and high resolution analog-to-digital converter. The PWM described here has an output waveform with a pulse-width-to-period ratio that is precisely equal to the ratio of the input voltage to a reference voltage. The PWM is useful in ADC applications as well as in analog computation circuits such

as analog multipliers, squaring, and square root circuits. Implementation of an ADC using the PWM results in several of the advantages of the techniques described above including high resolution and accuracy, a fixed conversion time, and a minimal requirement of precision parts.

The basic analog PWM circuit consists of an RC integrator and several logic gates and can be constructed using two integrated circuits, a resistor, and a capacitor. The operation of the analog PWM is investigated in chapter 2 and shown to be nearly independent of circuit components. Several applications of the PWM are presented together with measurements on an analog multiplier circuit incorporating the analog PWM.

Minor modifications of the analog PWM allow the circuit to be used in high resolution applications such as A/D conversion. These modifications and applications are considered in chapter 3. The synchronized PWM (SPWM) ADC is compared to other A/D conversion techniques and design considerations are addressed in an attempt to achieve high accuracy. Measurements on an implementation of the SPWM ADC are also presented in this chapter.

A typical application of the SPWM circuits described here is in oilfield pressure measurements. In this application, resolution and noise are a primary concern. Chapter 4 considers the problem of noise and resolution with respect to the SPWM. An examination of operational amplifier noise reduction techniques is also

presented along with measurements of the resolution of the SPWM ADC.

ADC's are normally embedded within a complete data acquisition system. Chapter 5 describes the development of a microcontroller-based precision data acquisition unit (DAU) incorporating the SPWM converter. The result is an inexpensive, yet flexible and compact system.

Chapter 6 is a summary of this work. Also included are recommendations for further research relating to the circuits described in this thesis.

CHAPTER 2

ANALOG PULSE WIDTH MODULATOR

2.1 Introduction

The implementation of a precision analog pulse width modulator (PWM) is investigated. The basic PWM described here utilizes an RC integrator and charge balance concepts [1], to produce a rectangular wave with a duty cycle proportional to an input voltage. In addition, the circuit can be modified to provide voltage gain and signal linearization.

The PWM is useful in applications which require the transmission of analog signals via two wire line or fibre optic cable. The analog PWM can also be used to realize a precision single quadrant multiplier by amplitude modulating the PWM output with a second signal voltage and averaging the resulting signal.

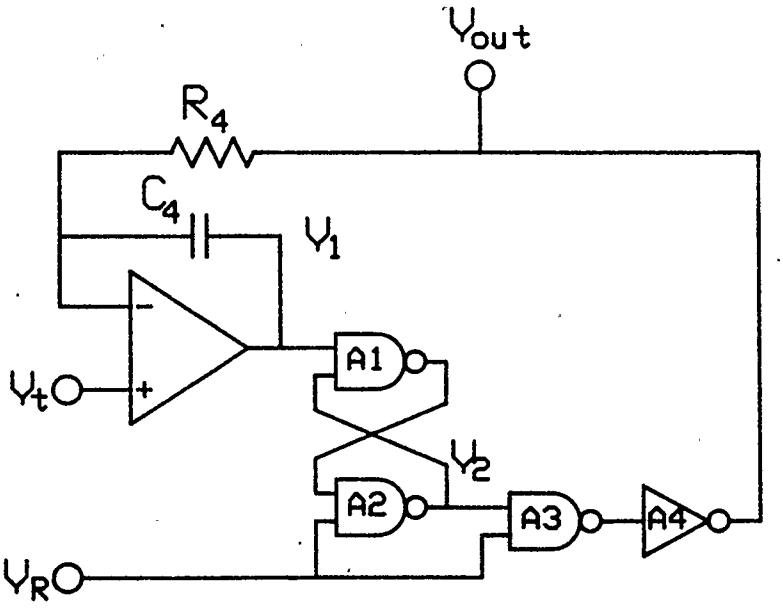
This chapter describes the operation of the analog PWM and applications of the circuit. As an example of the precision that can be achieved with the PWM, results of tests on an analog multiplier circuit are presented.

2.2 Basic Analog PWM

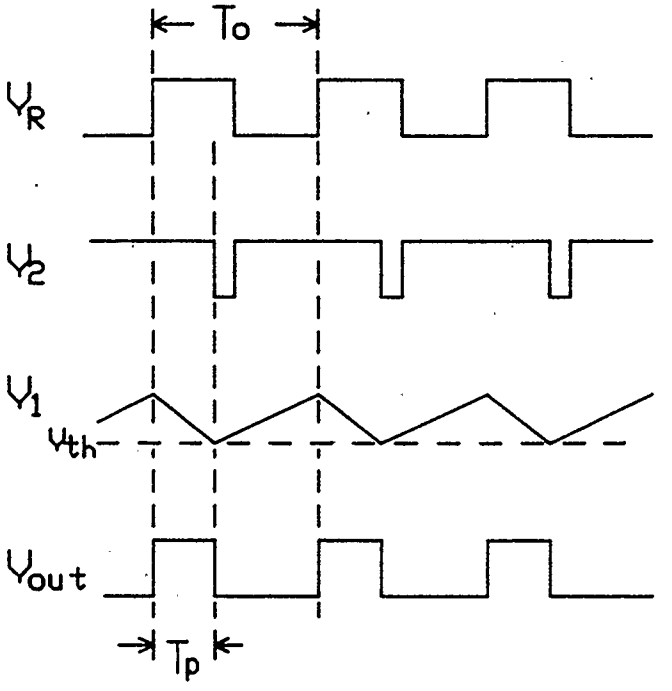
A simple low parts count analog pulse width modulator can be constructed as shown in Fig. 2.1(a). The circuit consists of an RC active integrator, a reset-set (RS) flip-flop (A1,A2), and gating logic (A3,A4). For single supply operations, all components are powered from a single voltage reference V_{ref}. If R_4 is large in comparison to the output resistance of the inverter (A4), then the output high level will be equal to V_{ref} and the output low level will be equal to zero volts.

The operation of the basic PWM is shown in Fig. 2.1(b). Initially, the input reset clock, V_R, is low and forces the output (V_{out}) low, causing the output of the integrator (V_1) to ramp towards V_{ref} at a rate proportional to the input, V_t. During this time, V_1 and V_2 are both high with respect to the switching threshold (V_{th}) of the Nand gate (A1). When V_R switches to V_{ref}, V_{out} goes high and V_1 starts to ramp towards zero. Upon V_1 reaching the switching threshold of A1, V_2 goes low, causing the output (V_{out}) to go low, and V_1 will again ramp towards V_{ref}. V_2 will be held low until V_R switches low and consequently the output will remain low until V_R switches back to V_{ref}. This completes a full cycle of the PWM.

The relationship between the input and output can be determined by considering the charge balance for the capacitor, C_4, as follows :



(a)



(b)

Figure 2.1 - Analog pulse width modulator; (a) Circuit diagram; (b) Timing diagram.

$$-\frac{T_o V_t}{R_4} + \frac{T_p V_{ref}}{R_4} = 0 \tag{2.1}$$

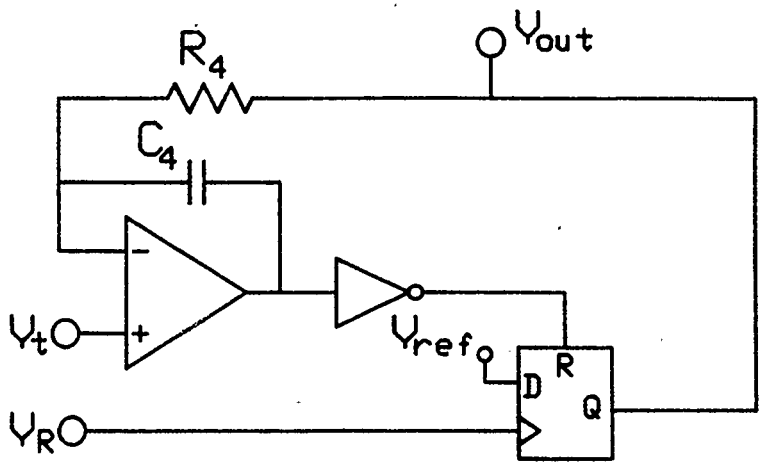
where T_o is the period of V_R and T_p is equal to the time that the output pulse is high. It then follows that :

$$\frac{T_p}{T_o} = \frac{V_t}{V_{ref}}, \tag{2.2}$$

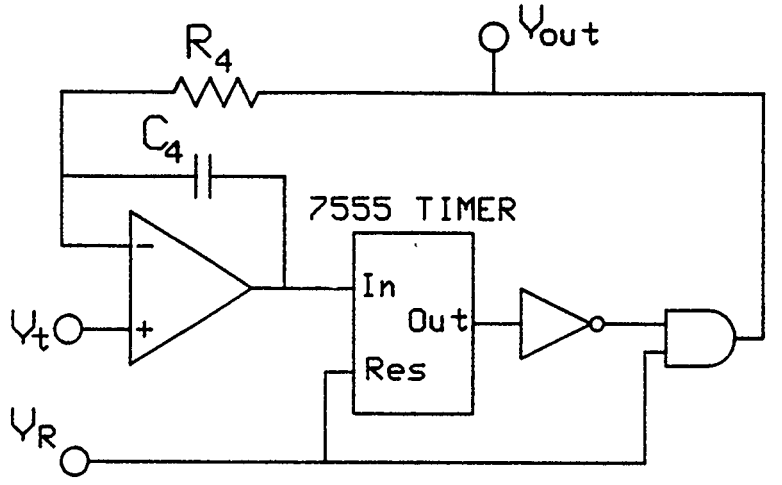
ie., the pulse width-to-period ratio, or duty cycle, is exactly equal to the ratio of the input voltage to the reference voltage.

Implementation of the analog pulse width modulator requires the following considerations:

(1) For the circuit of Fig. 2.1(a), V_R is typically a square wave. Careful analysis of the circuit indicates that the maximum input voltage for proper operation of the circuit is $\frac{V_{ref}}{2}$. Fig. 2.2(a) provides an implementation of the circuit which will operate from the negative to the positive supply rail regardless of the duty cycle of V_R. Alternatively, the maximum input voltage can be preset by setting the duty cycle of V_R to the desired maximum input ratio $\frac{V_t}{V_{ref}}$. For example, if V_R is a rectangular wave of 70% duty cycle, the maximum input voltage, V_t, for proper operation, will be 0.7 V_{ref}.



(a)



(b)

Figure 2.2 - (a) Analog PWM with full scale operating range; (b) 7555 Timer version of analog PWM.

(2) To a first approximation, $\frac{T_p}{T_o}$ is independent of the passive components R_4 and C_4. However, R_4 and C_4 must be selected in conjunction with the period T_o in a manner which assures that the triangular waveform at the output of the integrator remains within the operating range of the operational amplifier. A simple analysis indicates that selecting R_4 and C_4 so that $R_4 C_4 \geq \frac{T_o}{2}$ will provide proper operation.

(3) Careful analysis indicates that the switching threshold, V_{th}, of the Nand gate (A1) does not affect the output pulse width if the switching threshold is stable. However, if the switching threshold tends to drift and the amount of slewing of the output of the integrator is small, there will be a reduction in resolution. This can be minimized by selecting C_4, R_4, and T_o appropriately. In addition, the circuit can be implemented using a CMOS 7555 timer chip as shown in Fig. 2.2(b). The 7555 timer has the advantage of high gain comparators which provide a highly stable switching point.

2.3 PWM with Gain and Linearization

Voltage gain can be provided by connecting a resistor R_1 between the negative input terminal of the op amp and ground as shown in Fig. 2.3(a). The charge

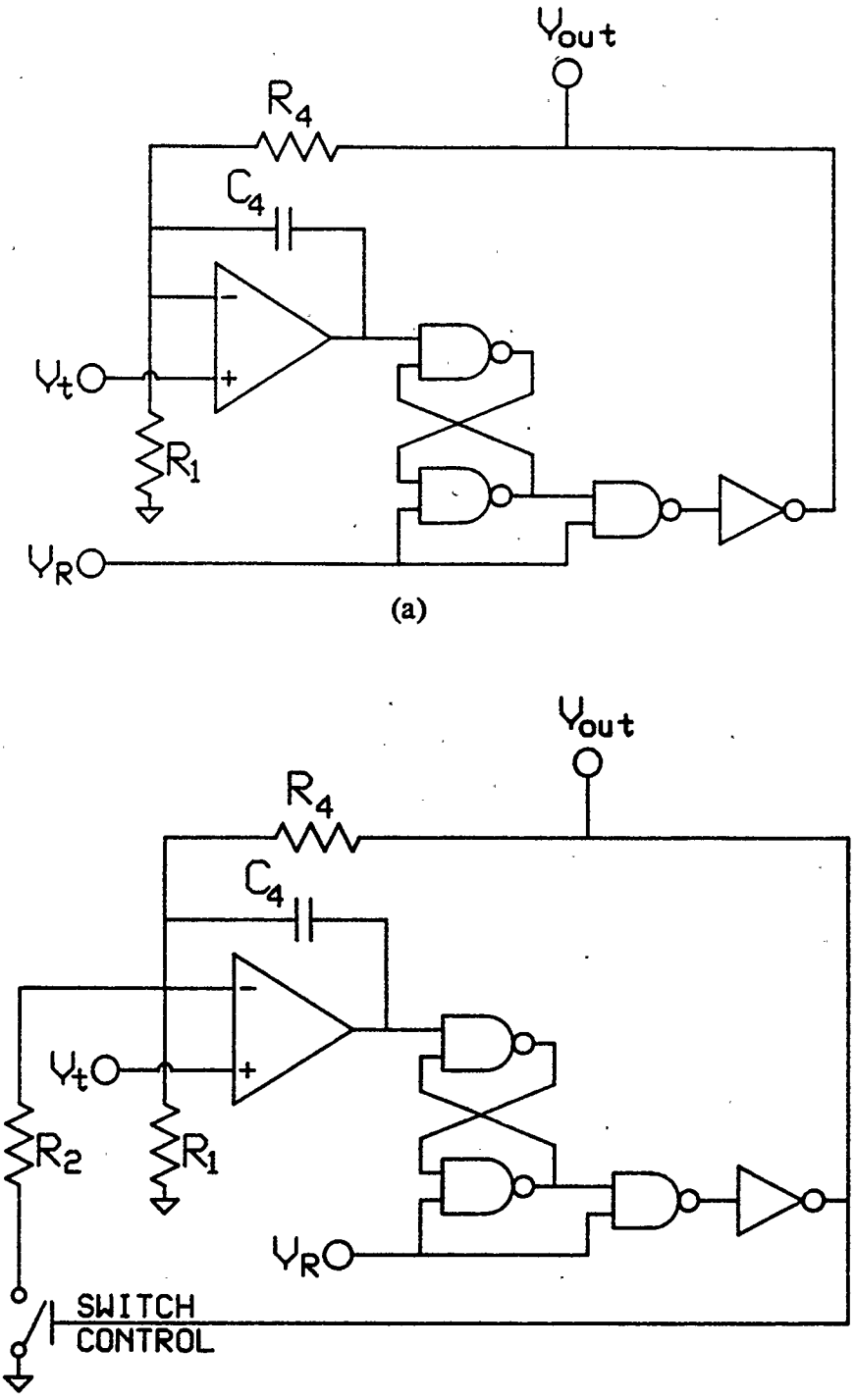


Figure 2.3 - Analog PWM with (a) gain; (b) gain and linearization.

balance for C_4 can then be rewritten as

$$-\frac{T_o V_t}{R_4} - \frac{T_o V_t}{R_1} + \frac{T_p V_{ref}}{R_4} = 0, \tag{2.3}$$

so that

$$\frac{T_p}{T_o} = \frac{V_t}{V_{ref}}\left[1 + \frac{R_4}{R_1}\right]. \tag{2.4}$$

In this case, the output pulse width depends on the ratio of the resistors R_4 and R_1.

A typical application of the PWM is where the input is a temperature transducer with an output voltage that is a nonlinear function of the temperature T. For example, the voltage-temperature characteristic for an ice-point referenced copper-constantan thermocouple is given by

$$\frac{V_t}{V_{ref}} = \frac{a\,T}{1 + b\,T}, \tag{2.5}$$

where a and b are constants[2]. In such an application the PWM can be modified to give a direct indication of the temperature T. This is achieved by connecting a second resistor R_2 between the negative terminal of the op amp and ground via a switch which is closed during the time that V_{out} is high, as shown in Fig. 2.3(b). Rewriting the charge balance equation for C_4 gives :

$$-\frac{T_o V_t}{R_4} - \frac{T_o V_t}{R_1} - \frac{T_p V_t}{R_2} + \frac{T_p V_{ref}}{R_4} = 0, \tag{2.6}$$

and thus,

$$\frac{T_p}{T_o} = \frac{\frac{V_t}{V_{ref}}\left[1 + \frac{R_4}{R_1}\right]}{1 - \frac{V_t}{V_{ref}}\left[\frac{R_4}{R_2}\right]}. \tag{2.7}$$

Alternatively, if R_2 is connected during the time that V_{out} is low, it is easy to show that

$$\frac{T_p}{T_o} = \frac{\frac{V_t}{V_{ref}}\left[1 + \frac{R_4}{R_1} + \frac{R_4}{R_2}\right]}{1 - \frac{V_t}{V_{ref}}\left[\frac{R_4}{R_2}\right]}. \tag{2.8}$$

Then, if R_2 is connected when V_{out} is high, a and b are both positive, and $\frac{R_4}{R_2}$ is chosen to be equal to $\frac{b}{a}$, it is easy to show that:

$$\frac{T_p}{T_o} = a\,T\,(1 + \frac{R_4}{R_1}). \tag{2.9}$$

Thus, linearization is achieved, although at the expense of making the result dependent on resistance ratios.

2.4 PWM and Bridge Applications

The analog pulse width modulator is particularly well suited for use with resistance bridge transducers as shown in Fig. 2.4(a). For this circuit, the charge balance for C_4 can be written as :

$$T_o V_{t+}\left(\frac{1}{R_{t-}} + \frac{1}{R_4}\right) - \frac{T_o V_{t-}}{R_{t-}} - \frac{T_p V_{ref}}{R_4} = 0, \tag{2.10}$$

where V_{t+}, V_{t-}, R_{t+}, and R_{t-} are defined as follows :

$$V_{t+} = \frac{R_6 V_{ref}}{R_5 + R_6};$$

$$V_{t-} = \frac{R_8 V_{ref}}{R_7 + R_8};$$

$$R_{t+} = \frac{R_6 R_5}{R_6 + R_5};$$

$$R_{t-} = \frac{R_7 R_8}{R_7 + R_8},$$

and are shown in the equivalent circuit of Fig. 2.4(b). Then, if $R_5 = R_8 = (R - \Delta R)$ and $R_6 = R_7 = (R + \Delta R)$, it is possible to show that :

$$\frac{T_p}{T_o} = \frac{2\Delta R R_4}{R^2}, \tag{2.11}$$

provided that $\left[\frac{\Delta R}{R}\right]^2 \ll 1$.

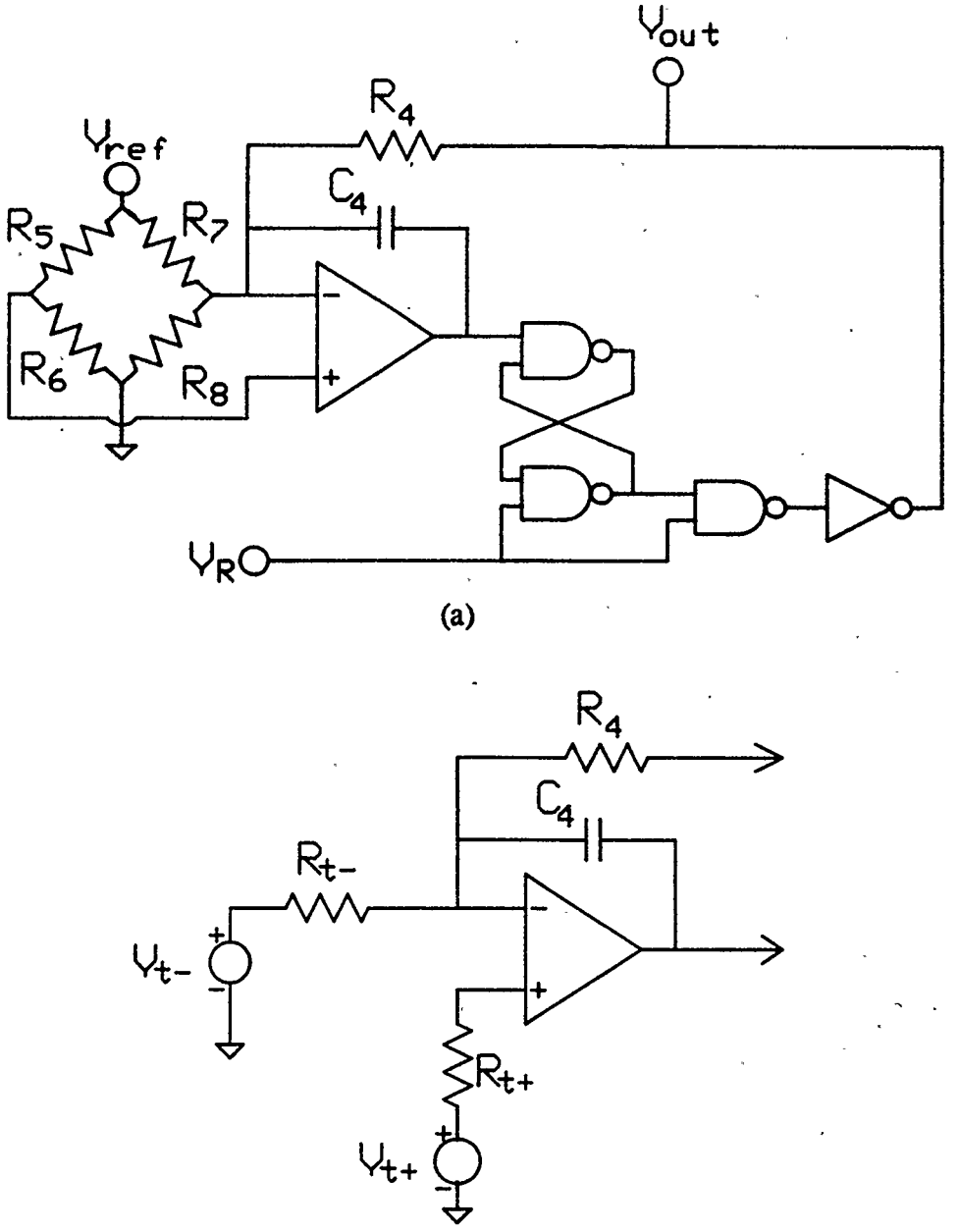


Figure 2.4 - (a) Analog PWM in bridge application; (b) Thevinen equivalent of bridge circuit.

2.5 Analog PWM Multiplier

Analog multipliers play an important role in instrumentation and signal processing[3]. For example, pulse amplitude modulation (PAM) is realized by multiplying an analog signal by a rectangular wave, as depicted in Fig. 2.5. Other applications of analog multipliers include analog division, squaring and square root functions.

The analog PWM provides the basis for a precision single quadrant multiplier. This is accomplished by amplitude modulation of the output pulse train by a second signal voltage. Such an arrangement is shown in Fig. 2.6(a). The CMOS switches connect the output of the multiplier circuit to the second signal voltage when the output of the PWM is high, and to ground when the PWM output is low. Waveforms for the integrator output, PWM output, and the switch outputs are shown in Fig. 2.6(b).

For the circuit shown in Fig. 2.6(a), the average value of the multiplier output is given by:

$$V_{out} = \frac{1}{T_o}[V_{t2}T_p + 0(T_o - T_p)]. \qquad (2.12)$$

Substitution of equation (2.2) results in:

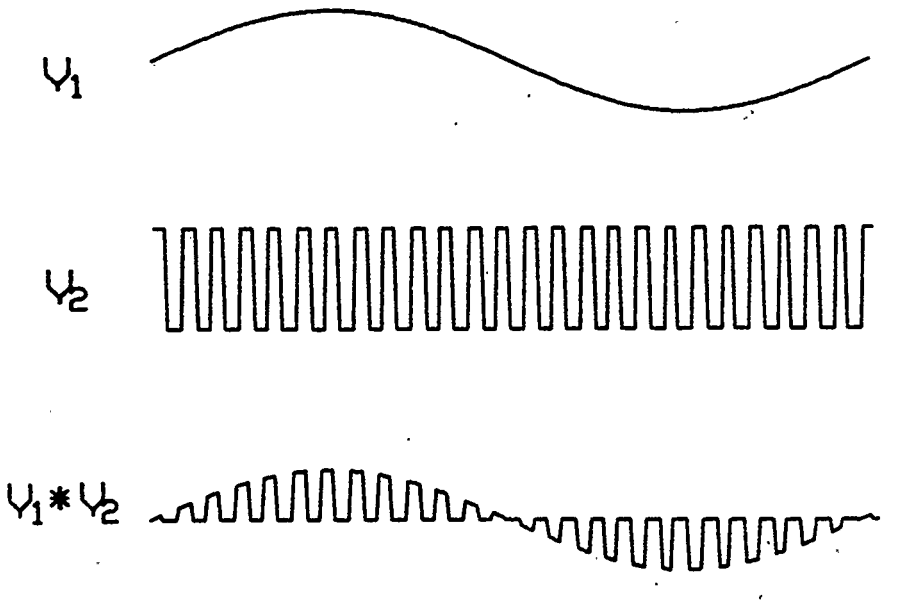
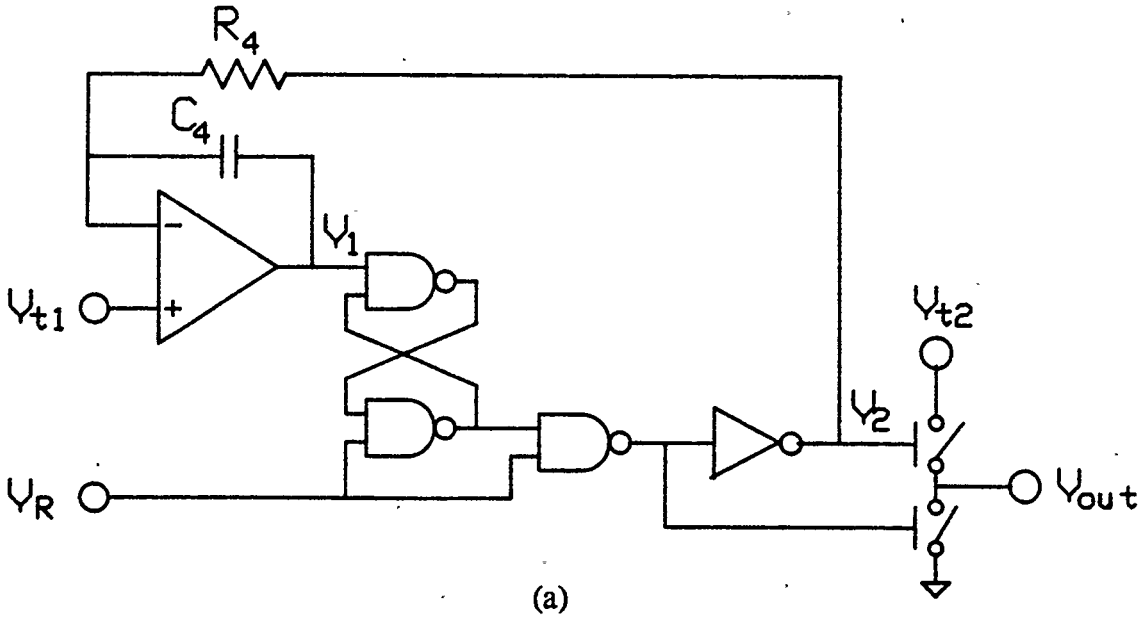
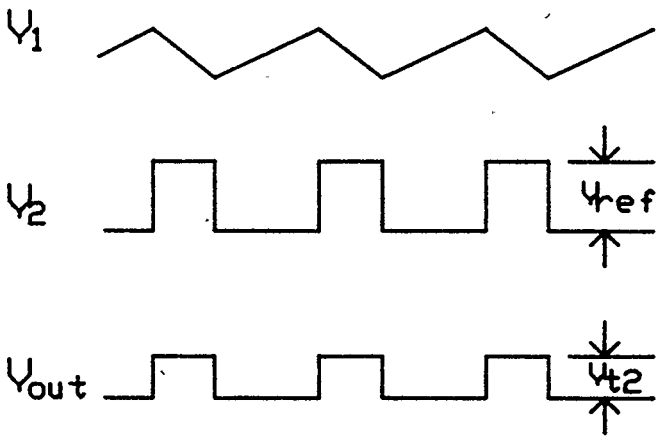


Figure 2.5 - Pulse amplitude modulation.



(a)



(b)

Figure 2.6 - (a) Single quadrant analog multiplier using PWM; (b) Analog multiplier waveforms.

$$V_{out} = \frac{V_{t1} V_{t2}}{V_{ref}}. \tag{2.13}$$

A dc/low frequency multiplier can then be realized by low pass filtering the output of the multiplier. A further application of the PWM multiplier is the transmission of two variables simultaneously along a single transmission line. The receiver can then determine the value of each variable by extracting the duty cycle and the amplitude of the received waveform.

2.6 Analog PWM Multiplier Measurements

The performance of the analog PWM was tested by implementing the circuit shown in Fig. 2.7. The multiplier was tested by measuring the output voltage of the multiplier, V_{out}, for various values of the input voltages, V_{t1} and V_{t2}. A power supply voltage, V_{ref}, of 10 volts was selected. Component values for C_4 and R_4 were chosen as 8.2 nanoFarads, and 330 kilohms, respectively. Finally, an operating frequency ($\frac{1}{T_o}$) of 244 Hz was selected for the PWM. The ICL7650 operational amplifier was chosen on the basis of a low dc offset voltage and an input voltage range that includes the negative supply rail.

Results appear in Figs. 2.8 and 2.9 and they indicate a maximum error of approximately 0.01% of full scale. This corresponds to a maximum error of 1

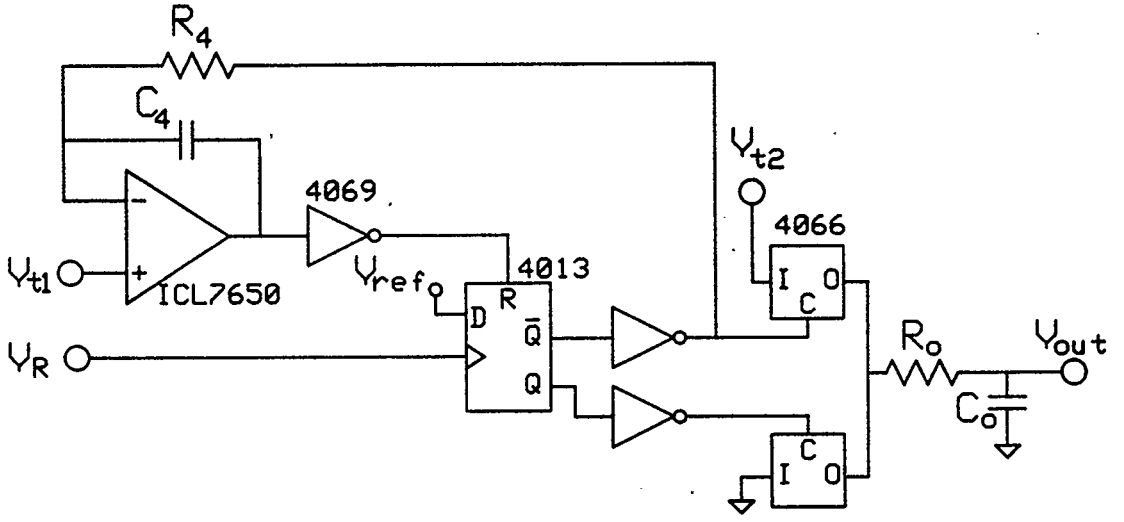


Figure 2.7 - Analog multiplier test circuit.

millivolt for a full scale voltage of 10 volts. Fig. 2.8 illustrates the effect of the modulating input, V_{t2}, on the multiplier error. Effectively, V_{t2} will multiply errors generated by the PWM and therefore the multiplier error will be linearly related to V_{t2}. A possible source of error that arises from the multiplier output switches is the difference in the analog switch resistances. However, the test results shown in Fig. 2.8 indicate that this source of error is small, and as a result the error is linearly related to V_{t2}.

Fig. 2.9 illustrates the effect of the PWM input, V_{t1}, on the multiplier error. The sources of error for the PWM include, (i) op amp non-idealities such as dc offset voltage and input bias currents; and (ii) the difference between the output high and output low resistance of the PWM output gate. An analysis of these errors is postponed until chapter 3, where they will be considered in detail. It is noted here that it is possible to reduce the error by nearly two orders of magnitude by considering the source of the errors and redesigning the circuit appropriately. What has been demonstrated here is that a highly accurate and relatively component insensitive analog multiplier can be implemented with minimal concern for circuit non-idealities.

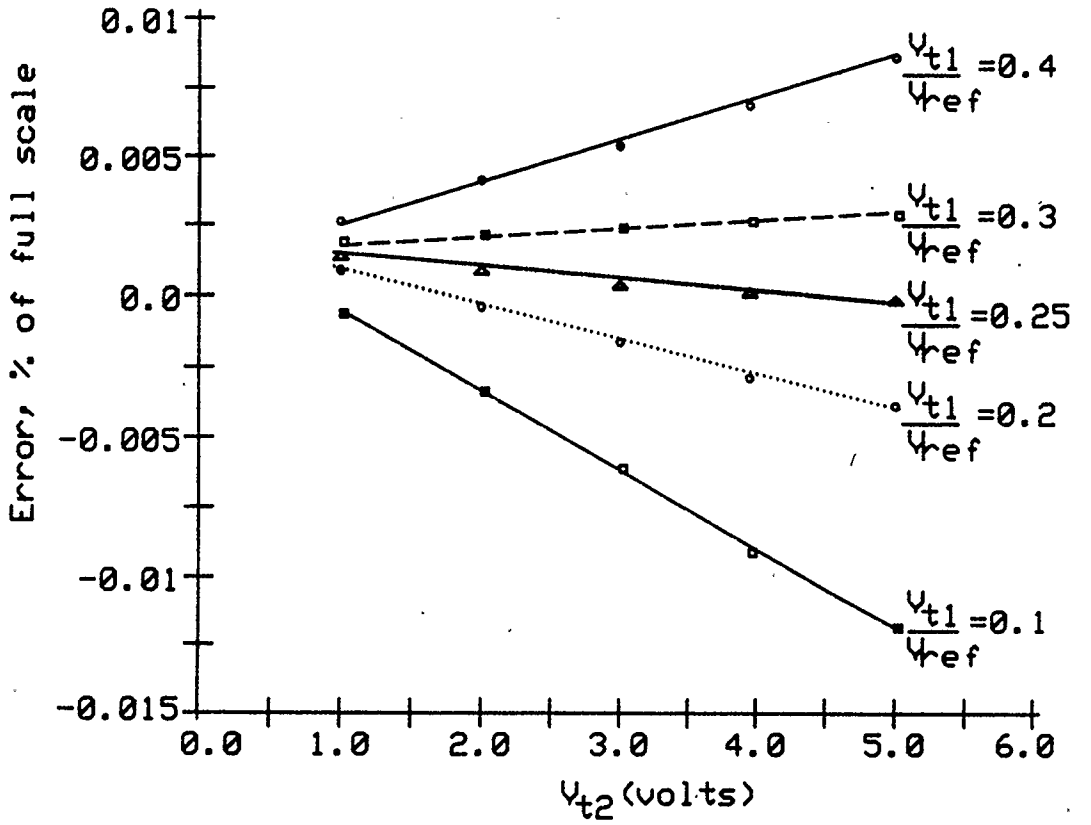


Figure 2.8 - Analog multiplier error as a function of amplitude modulating input

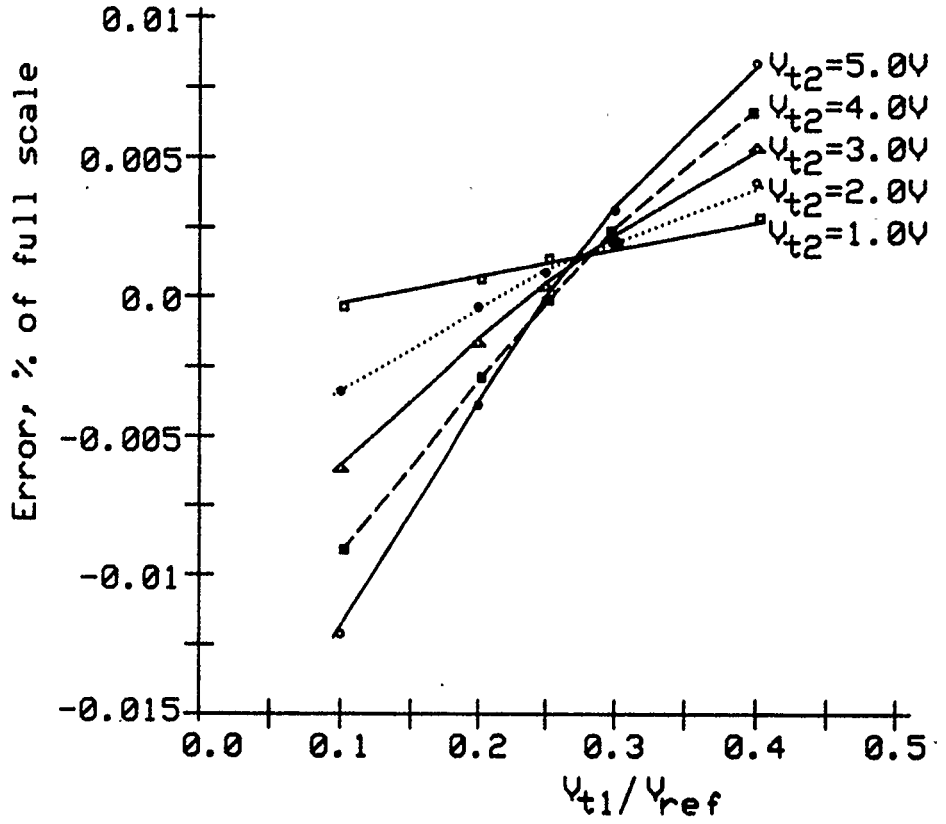


Figure 2.9 - Analog multiplier error as a function of PWM input

CHAPTER 3

SYNCHRONIZED PULSE WIDTH MODULATOR AND HIGH RESOLUTION ANALOG TO DIGITAL CONVERTER

3.1 Introduction

The analog PWM of Chapter 2 is useful in circuit applications where the output signal is used to drive other analog circuitry. However, if it is desirable to use the output to drive digital logic, the PWM can be modified by synchronizing the output with a high frequency clock. By doing so, it is possible to implement an analog - to - digital converter (ADC) with an overall accuracy of the order of a few parts per million.

This chapter discusses the operation and performance of the synchronized pulse width modulator (SPWM) and the realization of an SPWM ADC. The SPWM ADC is compared to other high resolution conversion techniques in an

attempt to show advantages and disadvantages of the circuit. Finally, design considerations for the SPWM will be presented together with measurements on an ADC implementation of the synchronized PWM.

3.2 Synchronized PWM Circuit

The basic configuration for the synchronized PWM is shown in Fig. 3.1. In this circuit, the output inverter of the analog PWM is replaced by a D-type flip flop which synchronizes the output with a high frequency clock. The high frequency clock is also used to generate the input reset clock, V_R, via a divide by N binary counter.

The operation of the synchronized PWM is shown in Fig. 3.2. The major difference between the synchronized PWM described here and the analog PWM of chapter 2 is that the output, V_{out}, is synchronized by the clock. This has the effect of quantizing the charge balance relationship for the circuit.

The analytical consequence of these changes can be determined by considering the charge balance for C_4 for a large number of PWM periods. If m periods of the reset clock, V_R, are considered, there will be an approximate charge balance for C_4 as follows:

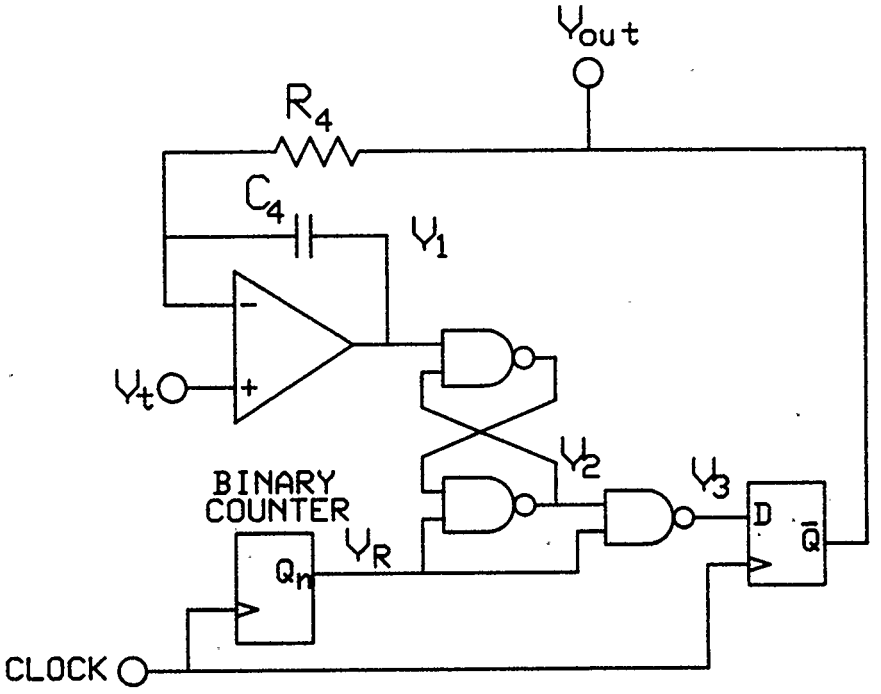


Figure 3.1 - Synchronized pulse width modulator circuit diagram.

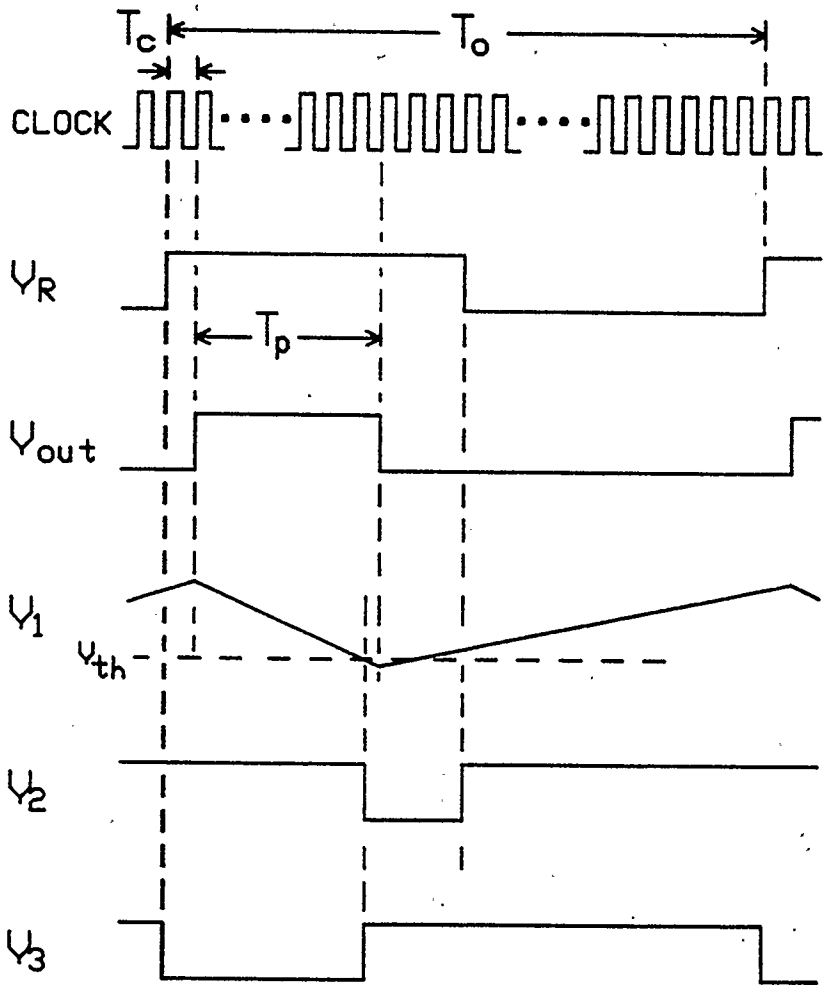


Figure 3.2 - Timing diagram for synchronized PWM.

$$-\frac{m\,T_o\,V_t}{R_4}+\frac{N\,T_c\,V_{ref}}{R_4}=0, \tag{3.1}$$

where T_o is the period of V_R, m is the number of periods of V_R, and $N\,T_c$ is the total time for which V_{out} is high during the time $m\,T_o$. It then follows that,

$$\frac{N\,T_c}{m\,T_o}=\frac{V_t}{V_{ref}}, \tag{3.2}$$

and if $T_o = n\,T_c$ then

$$\frac{N}{m\,n}=\frac{V_t}{V_{ref}}; \tag{3.3}$$

ie., N gives a direct indication of the input voltage ratio $\frac{V_t}{V_{ref}}$. The maximum quantization error in this case will be ± 1 part in N.

3.3 Synchronized PWM Applications

The pulse width modulator applications and features discussed in chapter 2 pertain directly to the synchronized PWM. However, the charge balance equations must be modified to account for quantization effects.

For example, the charge balance equation for the synchronized PWM with gain is given by,

$$-\frac{m T_o V_t}{R_4} - \frac{m T_o V_t}{R_1} + \frac{N T_c V_{ref}}{R_4} = 0, \tag{3.4}$$

which leads to the result,

$$\frac{N}{m n} = \frac{V_t}{V_{ref}}(1 + \frac{R_4}{R_1}). \tag{3.5}$$

Similarly, the linearization and bridge transducer applications presented in chapter 2 can be implemented using the synchronized PWM. The charge balance relationship for these applications will be modified in a manner analogous to that shown above.

3.4 Analog to Digital Conversion

The synchronized PWM can be incorporated into an analog to digital converter (ADC) by accumulating the output count, N, in a counter during the period $m T_o$ as shown in Fig. 3.3. This will give a direct indication of the input voltage ratio, $\frac{V_t}{V_{ref}}$. Since N will be determined to within ± 1 count, the resolution of the converter will then be ± 1 part in $\frac{m n V_t}{V_{ref}}$.

Implementation of an ADC using the synchronized PWM has two advantages over voltage-to-frequency (VFC) based implementations. First, the synchronized

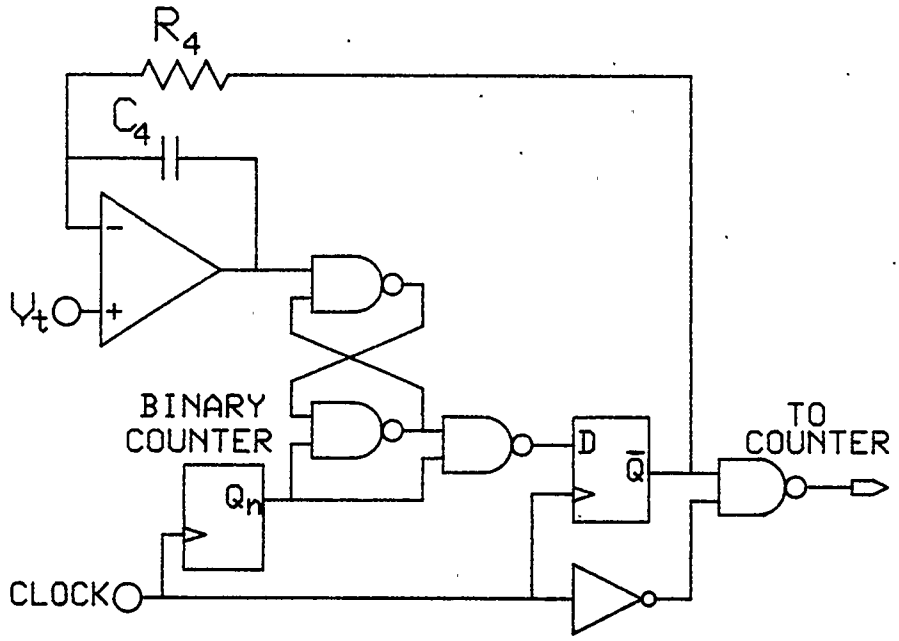


Figure 3.3 - Synchronized PWM analog-to-digital converter.

PWM has a fixed conversion time ($T_{convert}$) equal to $m\,n\,T_c$, which is independent of the input voltage. In general, VFC's have a conversion time that is either an integral number of VFC periods or equal to a fixed time plus the time required for the VFC to complete a full period[2]. These differences are illustrated in Fig. 3.4. The conversion time for the SPWM ADC (Fig. 3.4(a)) is fixed and equal to a fixed number of periods of the reset clock, ie. $T_{convert} = m\,T_o$. For a single counter VFC ADC (Fig. 3.4(b)), the conversion time is equal to a fixed number of VFC periods multiplied by the average value (T_{oavg}) of the VFC output period. Thus the conversion time is variable and dependent on the input voltage. For a two counter VFC ADC (Fig. 3.4(c)), the conversion time will vary about the time T_{switch}. The variation T_x from T_{switch} will depend on both the VFC input voltage and the time that T_{switch} is activated. The fixed conversion time of the SPWM is advantageous when interfacing the ADC to a microprocessor system.

The second advantage over VFC implementations is that the synchronized PWM output count N provides a direct indication of $\frac{V_t}{V_{ref}}$. VFC implementations normally use an inverse counting scheme. That is, the ADC count is inversely related to the measured input. Arithmetic logic is then required to convert the count to a value which gives a direct indication of the input voltage.

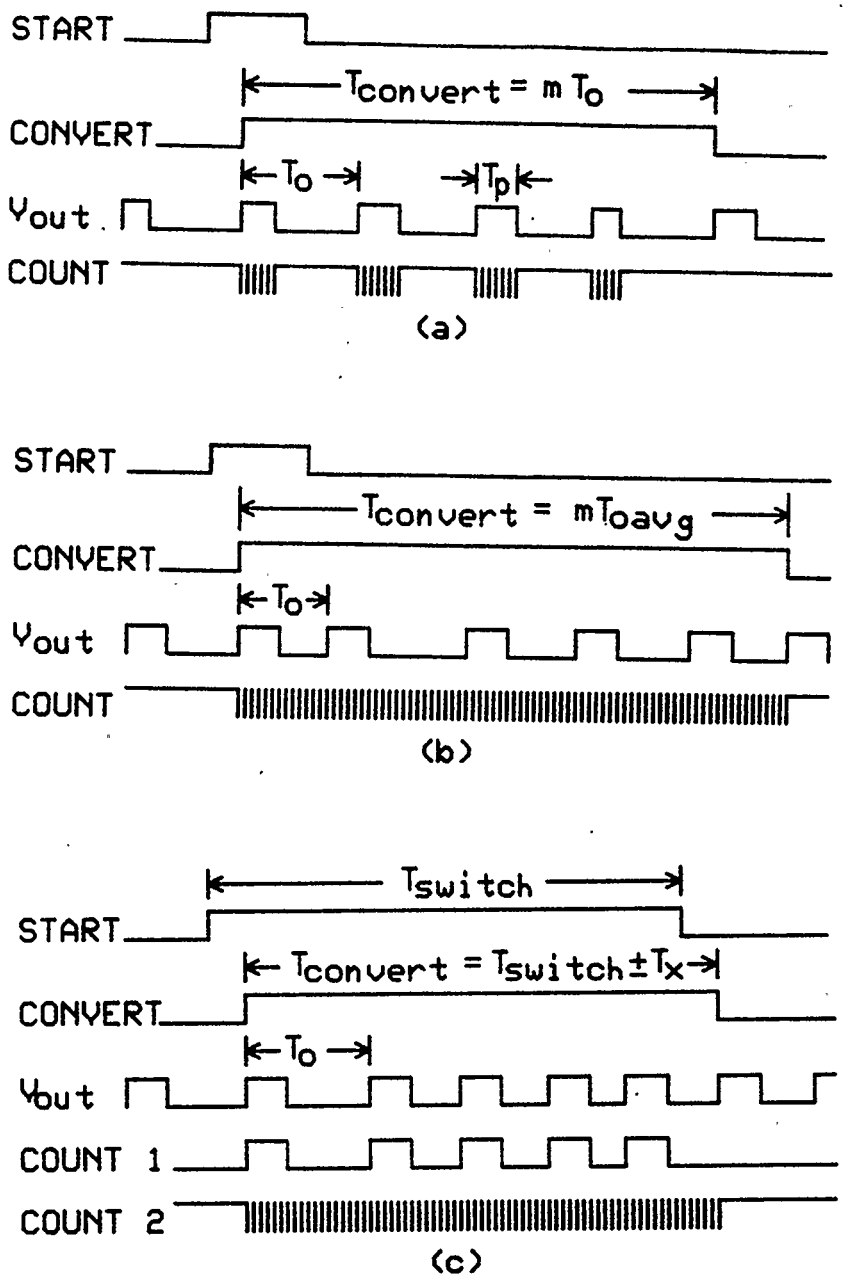


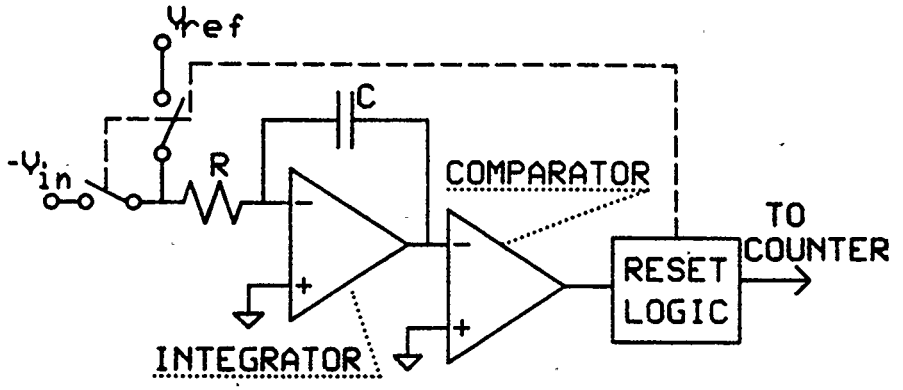
Figure 3.4 - Comparison of conversion time for (a) SPWM ADC; (b) VFC with one counter; (c) VFC with two counters.

Unfortunately, the resolution of the converter is effectively 1 part in N, and therefore the resolution of a SPWM ADC will decrease for small values of $\frac{V_t}{V_{ref}}$. In a VFC implementation N is inversely related to the input and thus will actually increase for small input voltages.

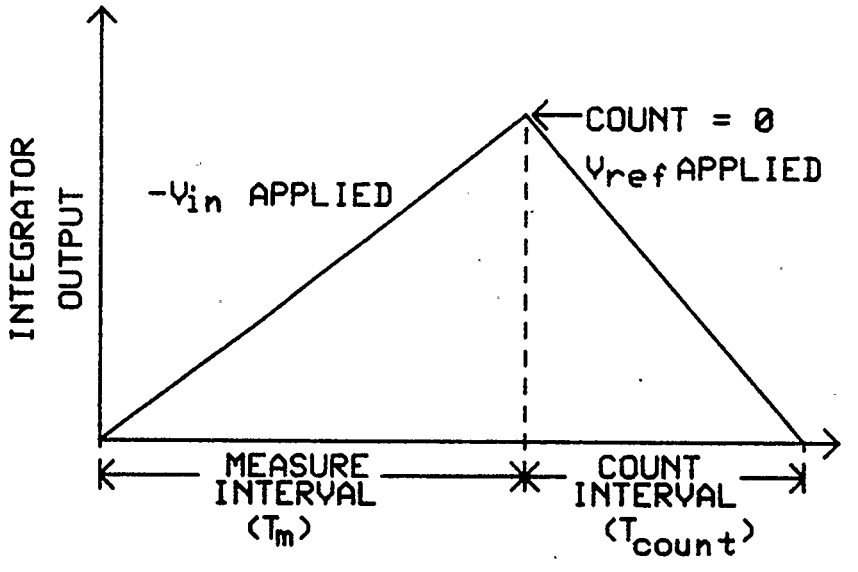
It is instructive to compare the SPWM ADC to the dual slope conversion ADC. Dual slope conversion is the most popular technique used in high resolution ADC's[4]. This is largely due to its simplicity of implementation[1]. The operation of a typical dual slope converter is illustrated in Fig. 3.5. The converter has a two-phase cycle, consisting of a measurement interval and a count interval. During the measurement interval, the analog input, $-\frac{V_{in}}{R}$, charges the integrating capacitor for a preset time interval, T_m, making the accumulated capacitor charge proportional to the analog input. During the count phase, a reference current, $\frac{V_{ref}}{R}$, discharges the capacitor. A counter is used to measure the discharge time, T_{count}. It is easy to show that the transfer function for a dual slope converter is,

$$\frac{N}{m} = \frac{V_{in}}{V_{ref}}; \tag{3.6}$$

where $N = \frac{T_{count}}{T_{CLK}}$, $m = \frac{T_m}{T_{CLK}}$, and T_{CLK} is the clock period. The conversion



(a)



(b)

Figure 3.5 - Dual slope converter; (a) Simplified circuit diagram; (b) Integrator output showing two stage conversion.

time of the converter will be $(N + m)T_{CLK}$, or

$$T_{convert} = (1 + \frac{V_{in}}{V_{ref}})m\,T_{CLK}. \tag{3.7}$$

Inspection of eqn 3.6 indicates that a dual slope converter output provides a direct indication of the input. However, unlike the synchronized PWM, the dual slope converter has a variable conversion time. Finally, the resolution of a conversion using the dual slope technique will be reduced as the input is reduced, as is the case for the synchronized PWM ADC.

In summary, the synchronized PWM has the advantages of a fixed conversion time and an output count which is a direct indication of the input. It has the disadvantage of reduced resolution for small input voltages.

3.5 Synchronized PWM Design Considerations

In Chapter 2, it was shown that an analog multiplier based on the pulse width modulator could be constructed with a maximum error of the order of 0.01% of full scale. This was accomplished with a minimal concern for circuit non-idealities. However, 0.01% error corresponds to 13 bits of linearity in an ADC context, which is inadequate for converter applications such as digital multimeters, where the required accuracy is of the order of 18 bits. Therefore, it is desirable to attempt to reduce these errors. This section discusses the major sources of error of

the synchronized PWM ADC and the modifications required to minimize these errors. It is noted that these design considerations also apply to the analog PWM of chapter 2.

Operational Amplifier Non–Idealities

Errors due to operational amplifier non-idealities can be accounted for by considering the effects on the charge balance relationship of the circuit. If the dc offset voltage, common mode gain, and input bias currents are considered, the charge balance for C_4, assuming single supply operation, can be rewritten as follows:

$$\frac{m\,n\,T_c\,V_t^{'}}{R_4} - m\,n\,T_c\,I_{B-} - \frac{N\,T_c\,V_{ref}}{R_4} = 0, \tag{3.8}$$

where,

$$V_t^{'} = V_t + V_{os} + \frac{(\frac{V_{ref}}{2} - V_t)}{CMRR};$$

$CMRR$ = amplifier common mode rejection ratio;

V_{os} = amplifier input offset voltage;

I_{B-} = amplifier negative input bias current,

as shown in Fig. 3.6(a). It follows from (3.6) that,

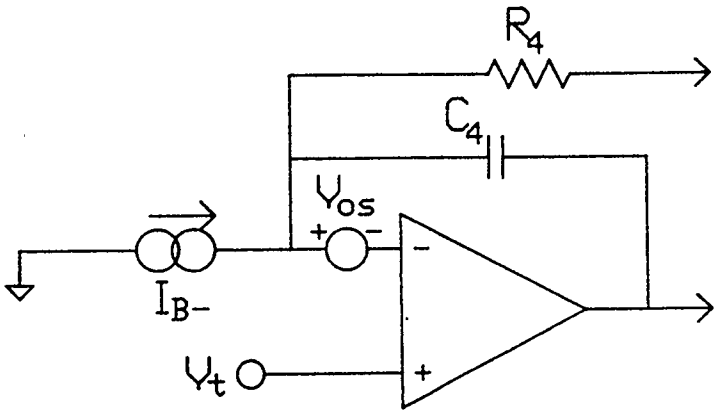
$$\frac{N}{m\,n} = \frac{V_t}{V_{ref}} + \frac{V_{os}}{V_{ref}} + \frac{\frac{1}{2} - \frac{V_t}{V_{ref}}}{CMRR} - \frac{I_{B-}R_4}{V_{ref}}, \tag{3.9}$$

and thus the error, ε_{OA}, due to op amp non-idealities will be,

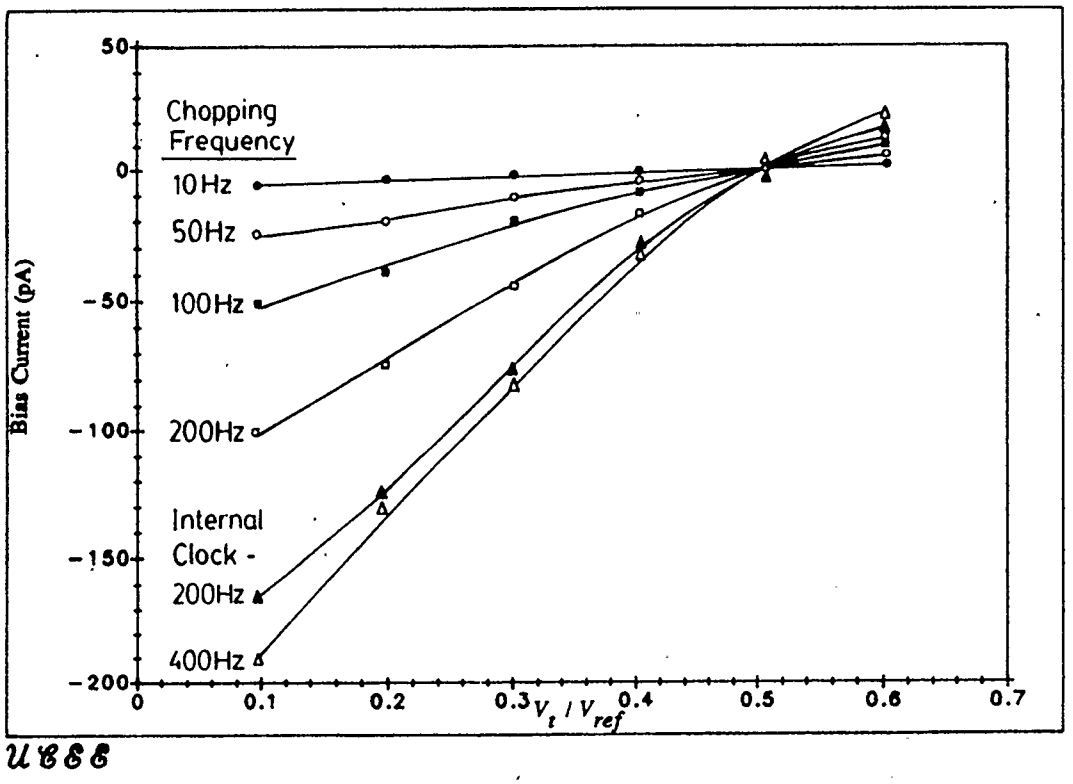
$$\varepsilon_{OA} = m\,n\left[\frac{V_{os}}{V_{ref}} + \frac{\left[\frac{1}{2} - \frac{V_t}{V_{ref}}\right]}{CMRR} - \frac{I_{B-}R_4}{V_{ref}}\right]. \tag{3.10}$$

As an example, suppose an auto-zeroing amplifier such as the ICL 7650 is used in a configuration consisting of a 10 volt power supply, ie., V_{ref} = 10 volts, and with $R_4 = 330\ k\Omega$. The offset voltage, V_{os}, may be as high as $5\,\mu V$, $CMRR$ will be as low as 120 dB, and I_{B-} may be as high as 100 pA[5]. The maximum error due to these op amp non-idealities will then be approximately 4 parts per million (ppm).

Actual measurements of the amplifier input currents for the ICL7650 are shown in Fig. 3.6(b)[2]. Inspection of these measurements indicate that the input currents are a function of both the common mode input voltage and the amplifier auto-zeroing clock frequency, f_{CH}. In addition, at common mode inputs near the negative supply rail, the input currents actually exceed the 100 pA maximum specification.



(a)



(b)

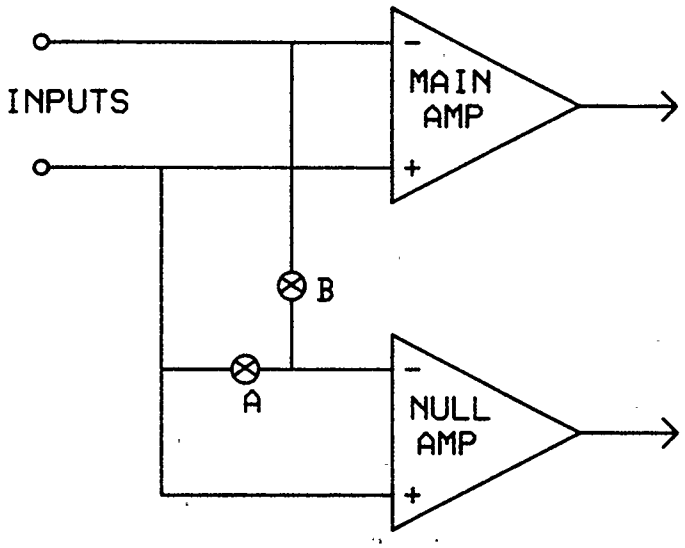
Figure 3.6 - (a) SPWM amplifier showing non-ideal effects; (b) Input current measurements for ICL7650.

The cause of these input currents can be understood by considering the input scheme of the operational amplifier (see Fig. 3.7(a)). The ICL7650 uses an auto zeroing scheme to significantly reduce the dc input offset voltage[5]. This is accomplished by comparing the inverting and noninverting input voltages in a nulling amplifier that alternately nulls itself and the main amplifier. The switching of inputs is achieved using analog switches.

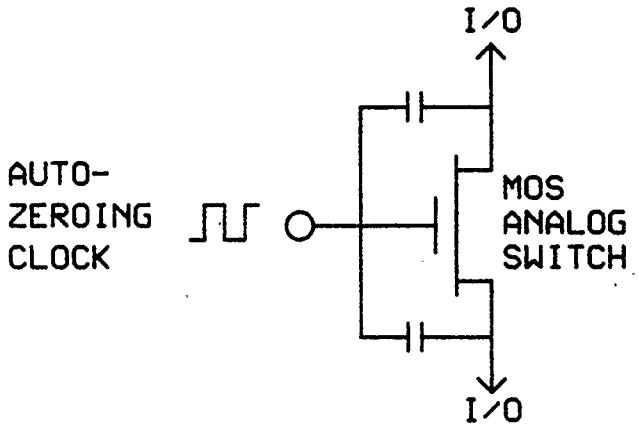
These switches are subject to two non-ideal mechanisms which lead to effective input currents. They are: (1) clock feedthrough due to capacitive coupling and (2) channel charge pumping. Capacitive coupling is the result of the gate-source and gate-drain capacitances of the MOSFET switches, which couple the clock voltage onto the signal path. Channel charge pumping is a result of inversion layer charge being held in the channel of a switch when it is on. When the transistor is turned off, the channel charge is injected into the loads at the source and drain of the switch[6].

The magnitude of the amplifier current due to these mechanisms will be linearly related to the auto zeroing clock frequency, assuming that the same amount of charge is transferred onto the signal path during each transition of the clock.

The relationship between the common mode input voltage and the amount of charge can be explained by considering the switch arrangement illustrated in Fig 3.7(b). When the clock signal switches small voltage spikes due to clock



(a)



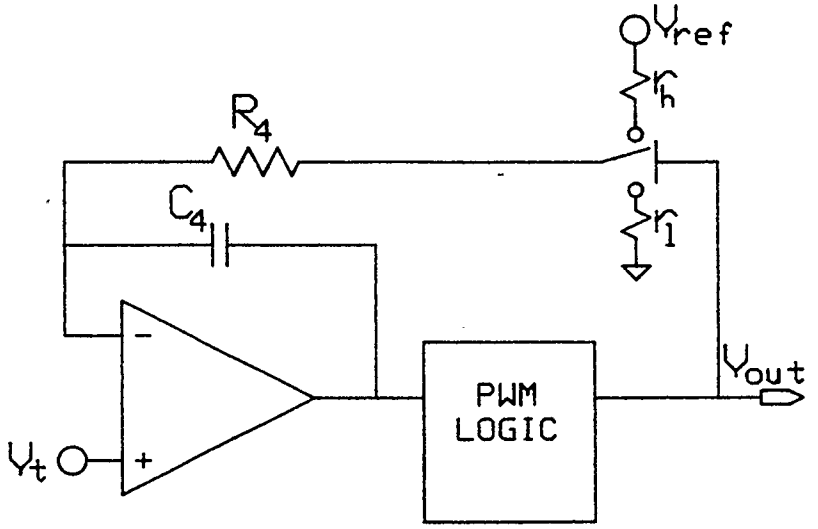
(b)

Figure 3.7 - (a) Input scheme for ICL7650 op amp; (b) MOS analog switch showing capacitive coupling.

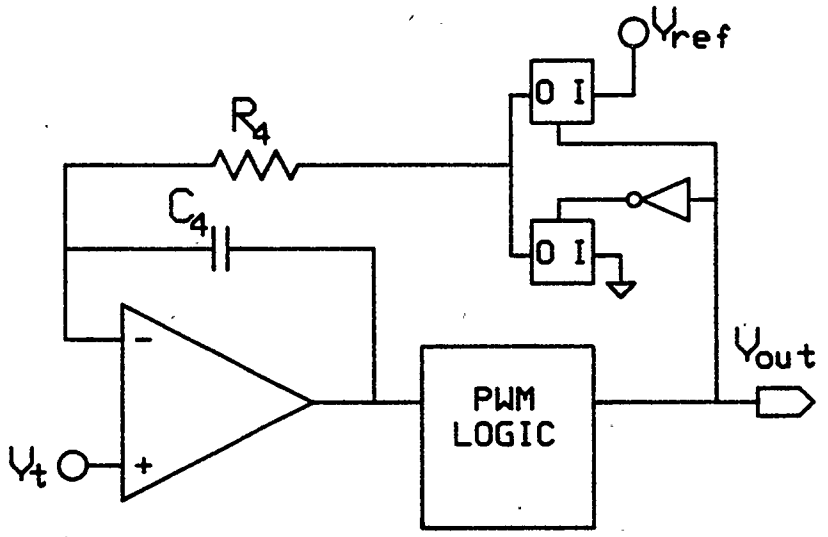
feedthrough will appear at the input and output of the switch. The charge is then dissipated through the external circuit. The shape and size of the spikes depend on the transition of the clock (low-to-high or high-to-low) and the steady state voltage of the input and output points. More specifically, the magnitude of the spike will be proportional to the difference between the final voltage of the clock signal and the steady state voltage of the switch input and output. Thus, for the op amp considered here, a low common mode input will cause a larger spike during the positive transition of the clock signal than during the negative transition. As a result, an effective input current will flow outwards from the amplifier inverting input terminal for common mode inputs below half scale (ie. $V_{CM} < \frac{V_{ref}}{2}$) and an effective input current will flow into the inverting input terminal for common mode inputs above half scale (ie. $V_{CM} > \frac{V_{ref}}{2}$). These conclusions are supported by the results of Fig. 3.6(b).

Logic Gate Output Resistance

The output of the synchronized PWM can be modelled as two resistances and an ideal switch as shown in Fig. 3.8(a). Here, r_h and r_l correspond to the on resistances of the MOS transistors used to realize the PWM output. In this case, the charge balance for C_4 can be rewritten as:



(a)



(b)

Figure 3.8 - (a) SPWM showing effect of finite output resistance; (b) SPWM with analog switches at output.

$$\frac{N T_c V_t}{R_4 + r_h} + \frac{(m n T_c - N T_c) V_t}{R_4 + r_l} - \frac{N T_c V_{ref}}{R_4 + r_h} = 0, \tag{3.11}$$

and so,

$$\frac{N}{m n} = \frac{\dfrac{V_t}{V_{ref}}}{1 - \left[\dfrac{r_d}{R_4 + r_h}\right]\left[1 - \dfrac{V_t}{V_{ref}}\right]}; \tag{3.12}$$

where $r_d = r_h - r_l$.

Then, the error, ε_{RO}, due to the output resistance of the PWM will be,

$$\varepsilon_{RO} \approx m n \frac{V_t}{V_{ref}}\left[1 - \frac{V_t}{V_{ref}}\right]\frac{r_d}{R_4 + r_h}. \tag{3.13}$$

For example, if a single gate of a CMOS 4069 inverter is used where $r_d \approx 60\,\Omega$, and $R_4 = 330\,k\Omega$, then the resulting maximum error will be approximately 45 ppm for $\frac{V_t}{V_{ref}} = \frac{1}{2}$. The error can be reduced substantially by increasing R_4 (if $R_4 = 3\,M\Omega$ for the same circuit, the maximum error will be 5 ppm), or by reducing r_d. Reduction of r_d can be achieved by either paralleling a number of inverter gates (the 4069 consists of six gates), or by using two low resistance CMOS switches as illustrated in Fig. 3.8(b). By reducing r_d to 10 ohms (six inverters in

parallel), and using a value of $3M\Omega$ for R_4, a maximum error of less than 1 ppm can be achieved.

Finite Rise and *Fall Time of Output*

The error due to the finite rise and fall times of the output can be estimated by considering the output pulse as shown in Fig. 3.9. The charge balance for C_4 can then be rewritten as,

$$\frac{T_o V_t}{R_4} - \frac{(T_{high} + \frac{t_R + t_F}{2}) V_{ref}}{R_4} = 0, \tag{3.14}$$

which results in

$$\frac{V_t}{V_{ref}} = \frac{T_{high} + \frac{t_R + t_F}{2}}{T_o}. \tag{3.15}$$

The counter arrangement will measure a count corresponding to the time $T_{high} + t_R$. Thus, for each period of the SPWM the count will be in error by an amount $\frac{t_R - t_F}{2T_o}$. It is possible to show that the converter output count will be,

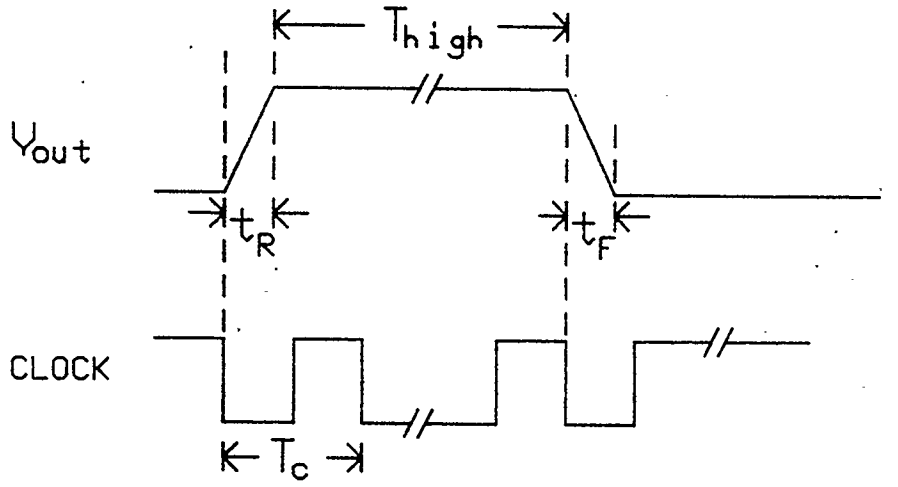


Figure 3.9 - Effect of finite rise and fall times at SPWM output.

$$N = m\,n\,\frac{V_t}{V_{ref}} + \frac{m\,n}{2T_o}(t_{Favg} - t_{Ravg}), \tag{3.16}$$

where t_{Favg} and t_{Ravg} correspond to the average rise and fall times, respectively. It follows that the error, ε_{RF}, due to finite rise and fall times will be,

$$\varepsilon_{RF} = \frac{m\,n}{2} t_d f_o, \tag{3.17}$$

where $t_d = t_{Favg} - t_{Ravg}$ and f_o is the PWM frequency. For example, if $t_d = 50$ ns and $f_o = 250Hz$, then the error will be approximately 7 ppm.

The total error, then, due to circuit non-idealities will be,

$$\varepsilon_{TOT} = \varepsilon_{OA} + \varepsilon_{RO} + \varepsilon_{RF}. \tag{3.18}$$

Then, for example, if a 7650 op amp is used such that $I_{B\_}$ is reduced to $10pA$ (by selecting $f_{CH} = 10$ Hz), $R_4 = 3M\Omega$, $f_o = 250Hz$, $r_d \approx 10\Omega$, and $t_d \approx 3ns$ (definitely achievable), the maximum error can then be determined as follows,

$\varepsilon_{OA} \approx 4$ ppm;

$\varepsilon_{RO} \approx 1$ ppm;

$\varepsilon_{RF} \approx$ ½ ppm;

$$\varepsilon_{TOT} = \varepsilon_{OA} + \varepsilon_{RO} + \varepsilon_{RF} \approx 5ppm.$$

This corresponds to 18 bits of accuracy. By noting the estimated errors, and compensating for them using digital logic, it is possible to achieve up to 20 bits of accuracy.

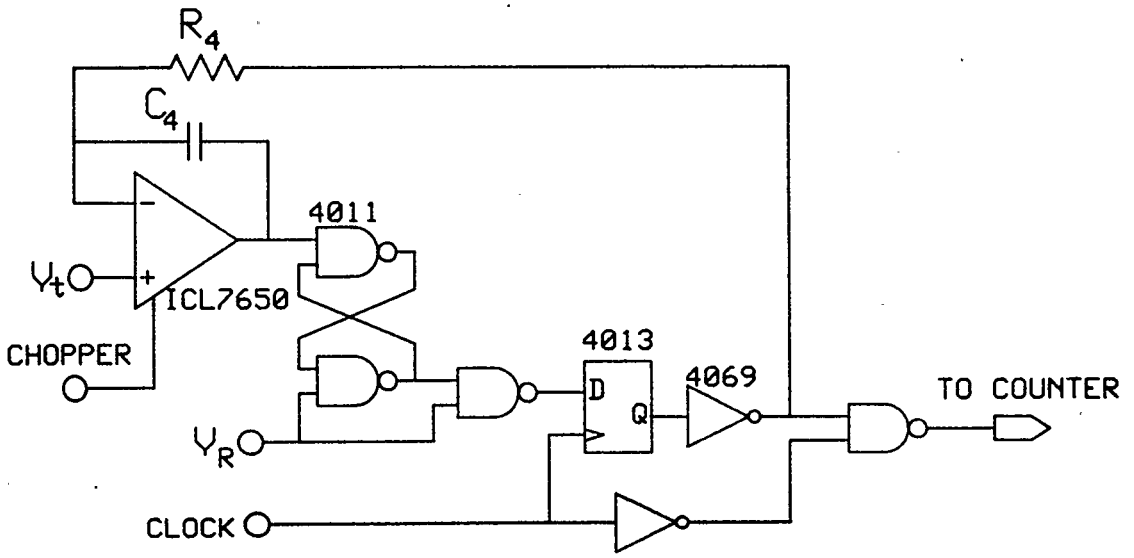
3.6 Synchronized PWM ADC Measurements

The synchronized PWM ADC was tested using the circuit implementation shown in Fig. 3.10(a). Note that the following additions to the circuit of Fig. 3.1 were made in an attempt to achieve optimum results :

(i) Six CMOS 4069 inverter gates were used at the output of the synchronized PWM, thus reducing r_d to approximately 10 ohms, as discussed above.

(ii) An external clock was connected to the amplifier auto zeroing input. This was done to observe the effect of various auto zeroing configurations and in particular to observe the effect of clock feedthrough on the performance of the circuit.

In addition to the above changes, the ADC was tested for various component values (R_4 and C_4), and at different operating frequencies (f_o) to determine an optimal circuit configuration. A clock frequency (f_c) of 2.0 MHz was chosen in consideration of speed limitations of the CMOS integrated circuits used to realize



(a)

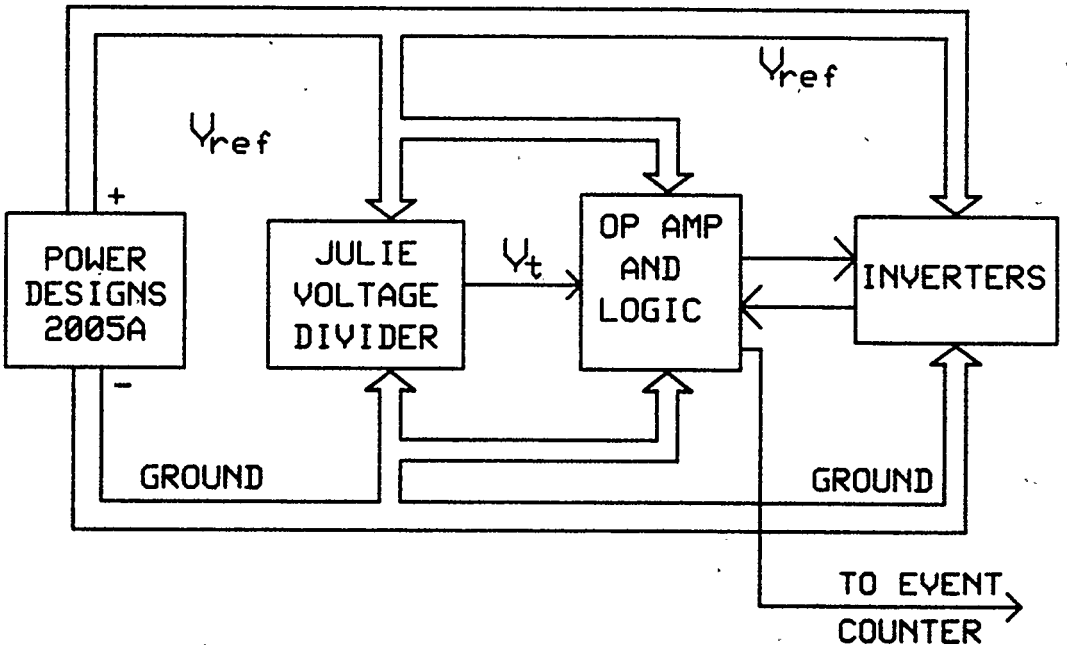


Figure 3.10 - (a) SPWM ADC test circuit; (b) Measurement system.

the ADC.

In an attempt to achieve maximum accuracy, the measurement system shown in Fig. 3.10(b) was utilized. The Julie voltage divider[7] provides an output voltage ratio $\frac{V_{out}}{V_{in}}$ that is accurate within 0.1 ppm. The Power Designs 2005A provides a stable reference power supply. In addition to precision equipment the circuit was laid out in such a manner to minimize any errors generated by the measurement system itself. Since the supply voltages of the PWM output gate effectively define the reference and zero voltages, the CMOS inverter was connected as close as possible to the voltage divider input in an effort to minimize the voltage drop from the divider to the inverter.

Test results for the synchronized PWM are provided in Fig's. 3.11 thru 3.14. Fig. 3.11 illustrates the effect of various amplifier auto zeroing clock frequencies. It is apparent that operating the op amp auto zeroing clock at very low frequencies (less than 30 Hz), significantly reduces the error due to amplifier input currents. These results also agree with the amplifier input current measurements given in Fig. 3.6(b).

Fig. 3.12 shows the error for two different values of the feedback resistance R_4. These measurements were taken with the auto zeroing clock frequency set to 15 Hz. Assuming a difference in rise and fall times of $t_d = 8\,ns$, and that input

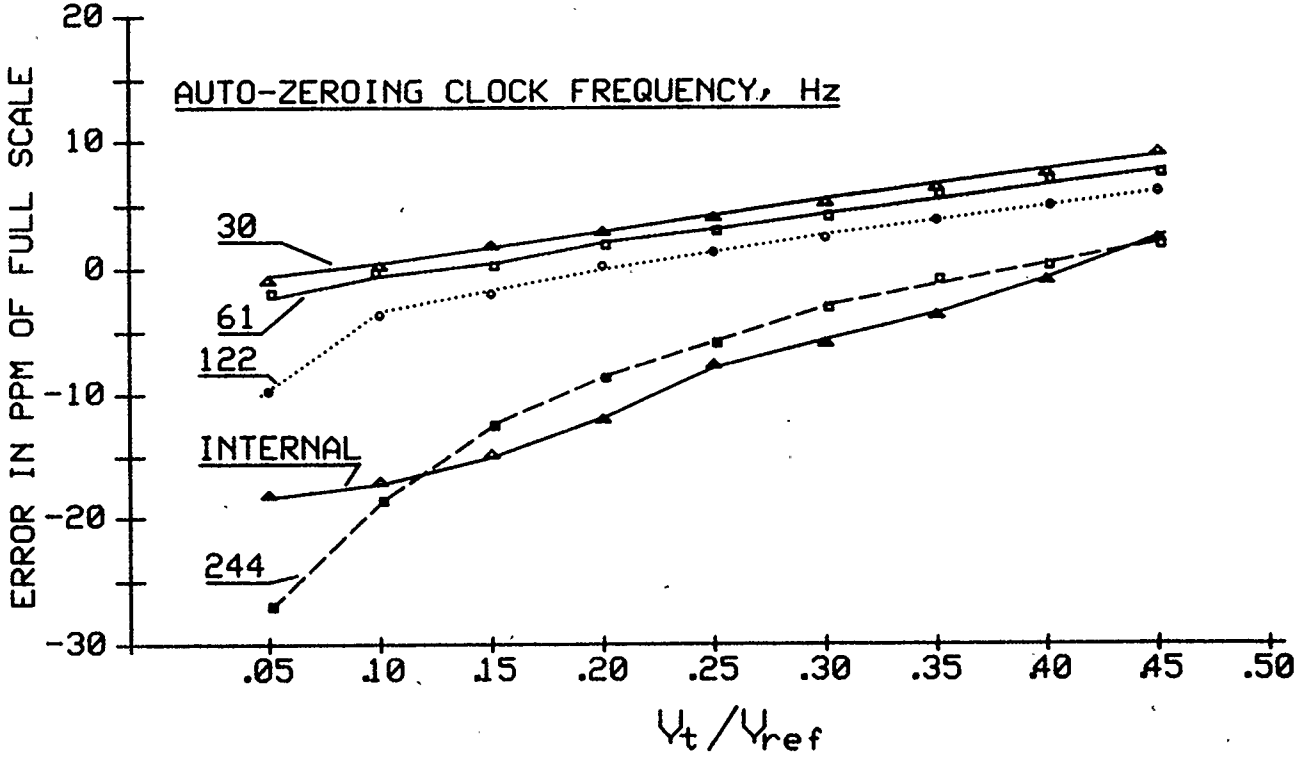


Figure 3.11 - SPWM ADC error for different auto-zeroing clock frequencies.

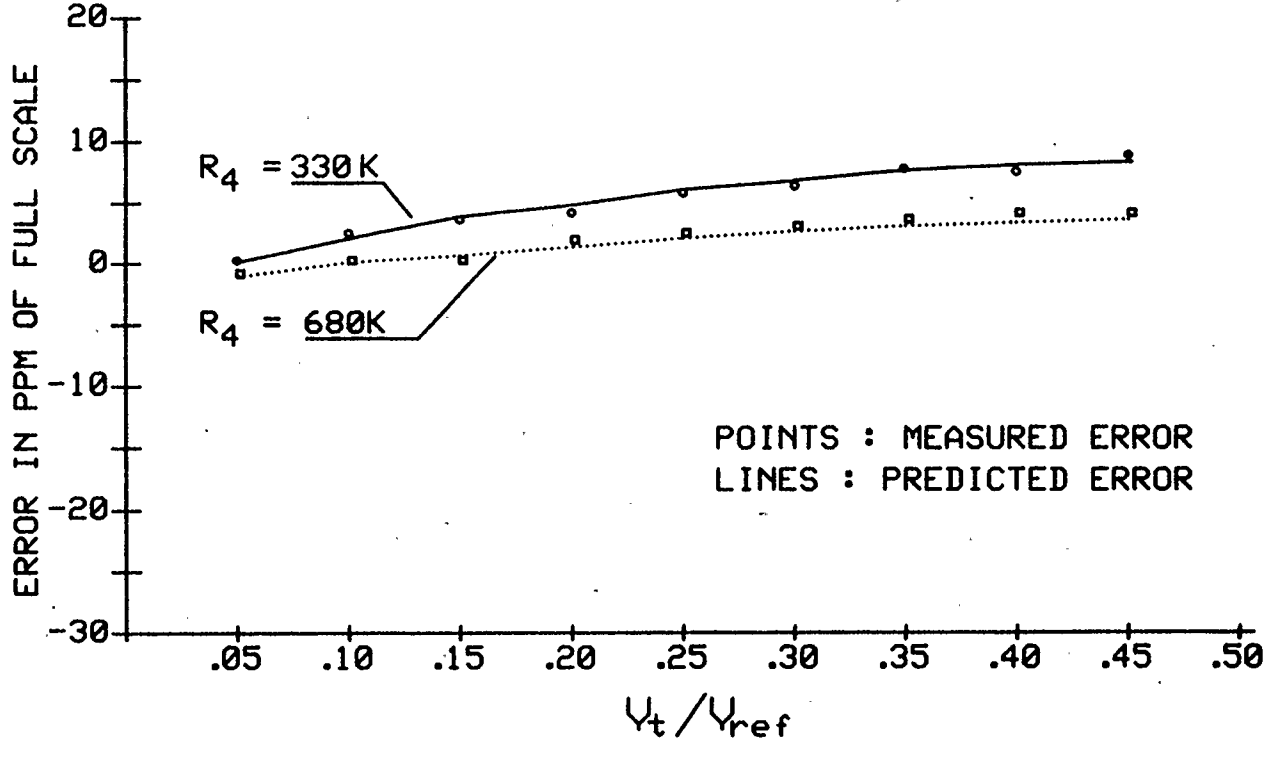


Figure 3.12 - SPWM ADC error for different feedback resistance.

current errors are negligible, it is possible to predict the error to within 1 ppm, as shown by the plotted lines.

Fig's 3.13 and 3.14 illustrate the effect of the PWM frequency on the performance of the circuit. The results of Fig. 3.13 were obtained with $R_4 = 330\,k\Omega$ and using the 200 Hz internal oscillator of the amplifier for the auto zeroing clock. As would be predicted by eqn. 3.16, the result of changing the PWM frequency is to shift the error. The results of Fig 3.13 suggest an approximate value of 8 ns for t_d.

Fig. 3.14 shows results for a circuit configuration of $R_4 = 5.1\,M\Omega$ and an amplifier auto zeroing clock frequency of 7.5 Hz. For this large resistance, the error contribution due to input currents becomes significant when $I_{B-} = 1pA$. Thus, the input current is likely the major source of error for such a configuration. In this case, the estimated value of t_d is 3 ns.

Comparison of Fig's 3.13 and 3.14 suggests that the pulse shape is affected by the value of R_4. This conclusion is quite reasonable if it is noted that the rise and fall times depend on the loading of the output gate. It is then logical to assume that the difference in rise and fall times would also vary with the load.

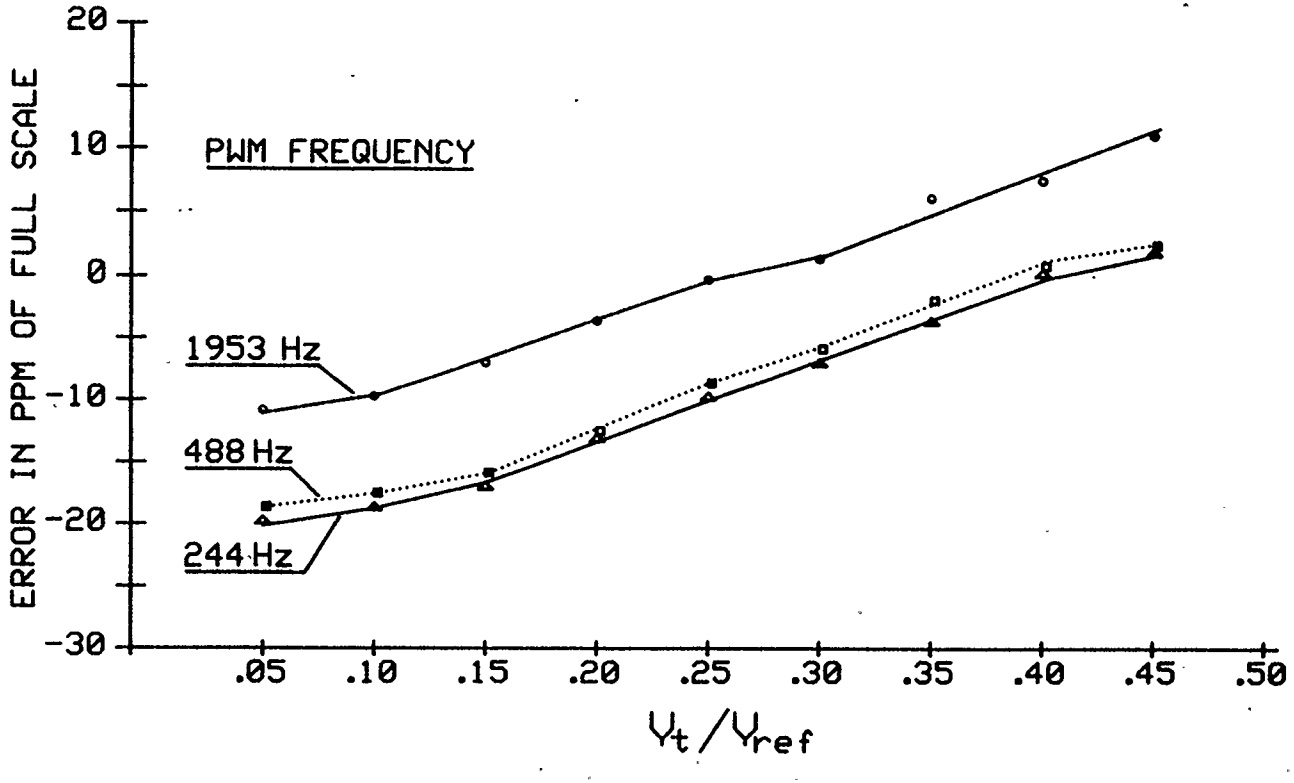


Figure 3.13 - SPWM ADC error for different operating frequencies (using internal auto-zeroing clock).

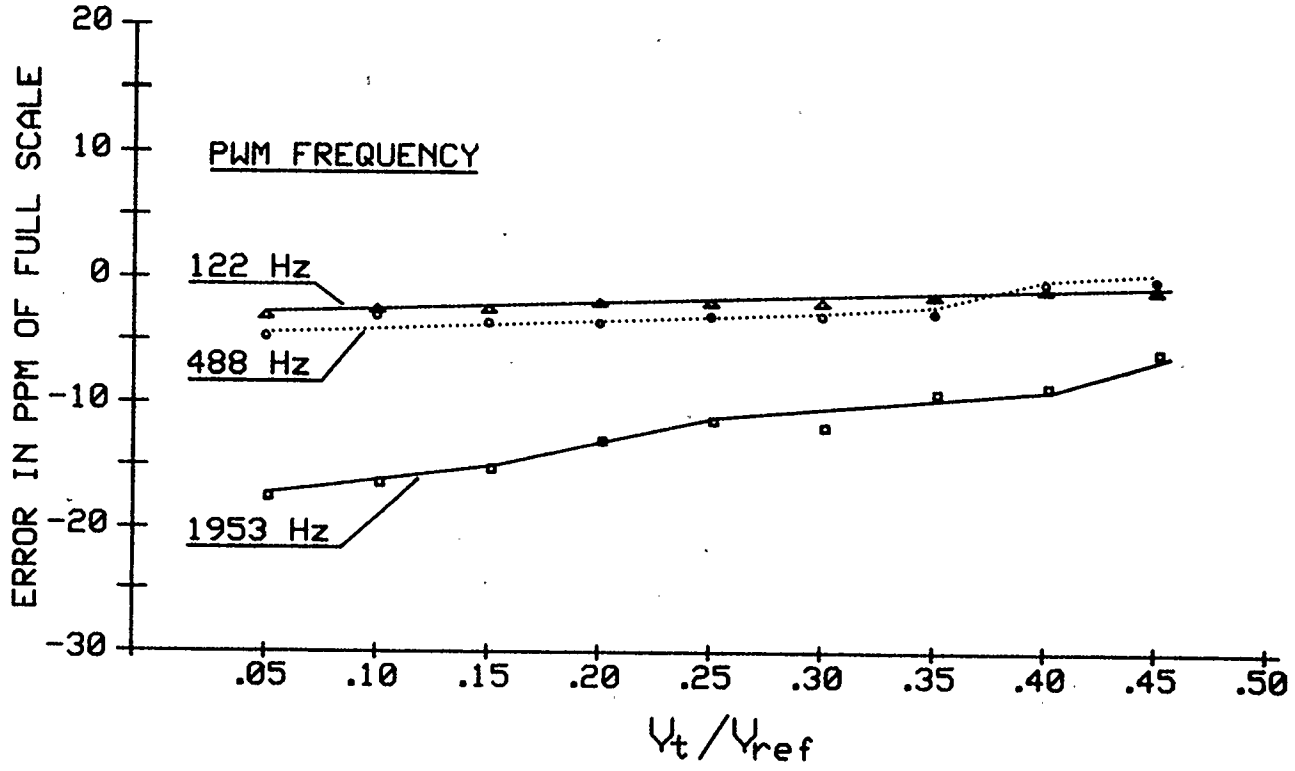


Figure 3.14 - SPWM ADC error for different operating frequencies (using 15 Hz auto-zeroing clock frequency).

3.7 Summary of Synchronized PWM Measurements

The results of tests on the SPWM ADC suggest several conclusions which can be summarized as follows:

(1) The synchronized PWM can be constructed such that the maximum error is approximately 4 ppm. This corresponds to 18 bits of linearity, achieved without calibration.

(2) For the ICL7650 operational amplifier, the parasitic effects of clock feedthrough and channel charge pumping contribute significant errors when operating the amplifier auto zeroing scheme normally. By reducing the auto zeroing frequency to less than 30 Hz, it is possible to reduce these errors to a negligible value. It is then possible to estimate the value of remaining errors using equations 3.10, 3.13, and 3.17. Digital correction of the ADC output count can then be used to achieve an overall accuracy of approximately 1 ppm, corresponding to 20 bits of accuracy.

(3) The actual value of t_d is difficult to directly measure or determine analytically. Alternatively, it is suggested that t_d be estimated from measurements of the ADC, with known values of I_{B-} and r_d.

(4) The error due to the resistance of the PWM output gate, r_d, is inversely

proportional to the magnitude of R_4. However, the error due to amplifier input currents is directly proportional to R_4. Therefore, it is necessary to compromise when selecting a value for R_4. It is easier to measure r_d and therefore to estimate the error due to r_d. It then follows that a more accurate estimation of the error can be achieved by selecting a moderate value for R_4.

(5) The presented results were all taken using the same amplifier and inverter pair. Measurements taken using different components gave similar but not identical results. In particular, measurements of the inverter output resistances showed significant differences for different manufacturers.

(6) Variation of the integrating capacitor, C_4, showed no effect on the error of the circuit, as expected. However, resolution was significantly improved when C_4 was chosen small enough such that the integrator output ramped between the switching threshold of the nand gate and the positive supply rail.

CHAPTER 4

RESOLUTION AND NOISE LIMITATIONS

4.1 Introduction

Analog-to-digital converters can be characterized by several performance criterion. For integrating converters, such as the SPWM ADC, three parameters are of particular interest. These are linearity, accuracy, and resolution, with the design objective being highly linear operation, high accuracy, and high resolution. The linearity and accuracy of the SPWM ADC were examined in chapter 3 where experimental results indicated an overall linearity of 4 ppm and the capability to digitally correct the error to achieve an accuracy of 1 ppm.

Resolution refers to the smallest change that the ADC input can detect that will result in a change in the ADC output[9]. Theoretically, the resolution of a converter depends on the number of quantization levels of the ADC. For example, an ADC with a full scale output count of one million will have a theoretical resolution of 1 ppm. Thus, the theoretical resolution can be increased by increasing the number of quantization levels. For the SPWM ADC, this can be accomplished by

increasing the conversion time or by increasing the frequency of the high frequency synchronization clock.

In practical systems resolution is limited by external interference and internal noise. An example of external interference in an A/D converter is coupling of digital noise into the analog circuitry via the analog/digital interface. In most cases, the effects of external interference can be minimized by proper circuit design and layout[10]. Internal noise, however, is an inherent characteristic of electronic systems and is observable in both active and passive devices. Internal noise cannot be eliminated, although its effect on electronic circuit performance can be minimized. In practical circuits the internal noise provides a physical limitation to the achievable resolution.

This chapter addresses the problem of noise and resolution with respect to the synchronized PWM. A discussion of internal noise sources leading to a noise model for the SPWM will be presented. The noise reduction techniques of two types of operational amplifiers will be examined along with noise power spectral density measurements of the ICL7650 op amp. A discussion of the various factors affecting the resolution will be included in an attempt to determine the practical resolution of the SPWM ADC. These expectations will then be compared to actual measurements of an SPWM ADC implementation.

4.2 Noise Model of SPWM

Noise associated with active and passive devices is a result of three phenomena : (1) thermal noise in resistive material, caused by the random motion of electrons due to thermal agitation; (2) shot noise in active devices, which is due to the discrete particle nature of carriers in current carrying devices; and (3) flicker noise or $1/f$ noise, which refers to several phenomena that exhibit a power spectral density that is approximately inversely proportional to frequency[11].

Thermal noise and shot noise are both approximately white in nature, that is, the power spectral density is constant and independent of frequency. The spectral density of thermal noise is proportional to both the temperature and the device resistance. The spectral density of shot noise is proportional to the dc current level. Flicker ($1/f$) noise is the predominant noise source at low frequencies. The $1/f$ phenomena is characterized by a non-Gaussian amplitude distribution and a power spectral density that follows a $\frac{1}{f^{\alpha}}$ law[12].

Predicting the actual noise performance of a particular circuit is accomplished by modelling the theoretical noise sources as equivalent noise voltage and noise current generators. If the noise generators are assumed to be independent of each other (ie. uncorrelated), it is possible to estimate the total noise output of the circuit. Circuit conditions can then be modified so that the noise performance and

signal-to-noise ratio are optimized.

Fig. 4.1(a) illustrates the equivalent noise model for a resistor of resistance R. The noise spectral density of a resistor is defined as

$$S_R = 4kTR; \tag{4.1}$$

where k is Boltzman's constant and T is the absolute temperature[13]. The power spectral density is normally expressed in $volts^2/Hz$.

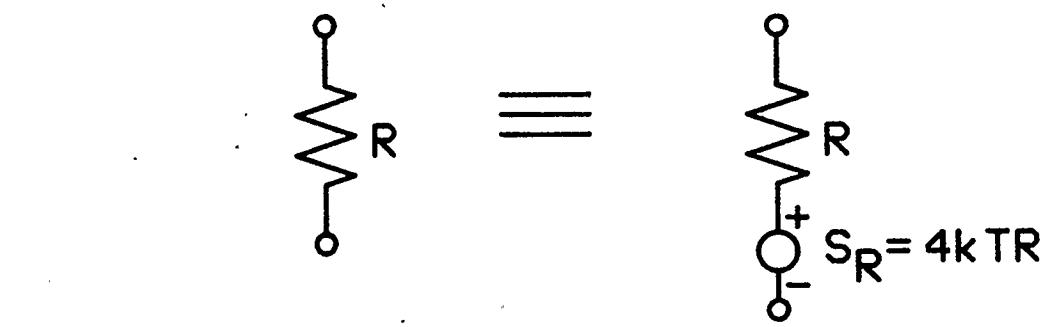
An equivalent noise model for an operational amplifier is illustrated in Fig. 4.1(b)[11]. In this case, all of the noise sources internal to the device are referred to the amplifier inputs and represented as two noise current generators and a single noise voltage generator. The spectral density of each generator depends on the type of device (bipolar, MOSFET, or JFET) and the amplifier design. For the purpose of analysis, these generators are modelled as follows:

(a) input noise voltage generator (e_{na}), $S_{ena} = S_e$;

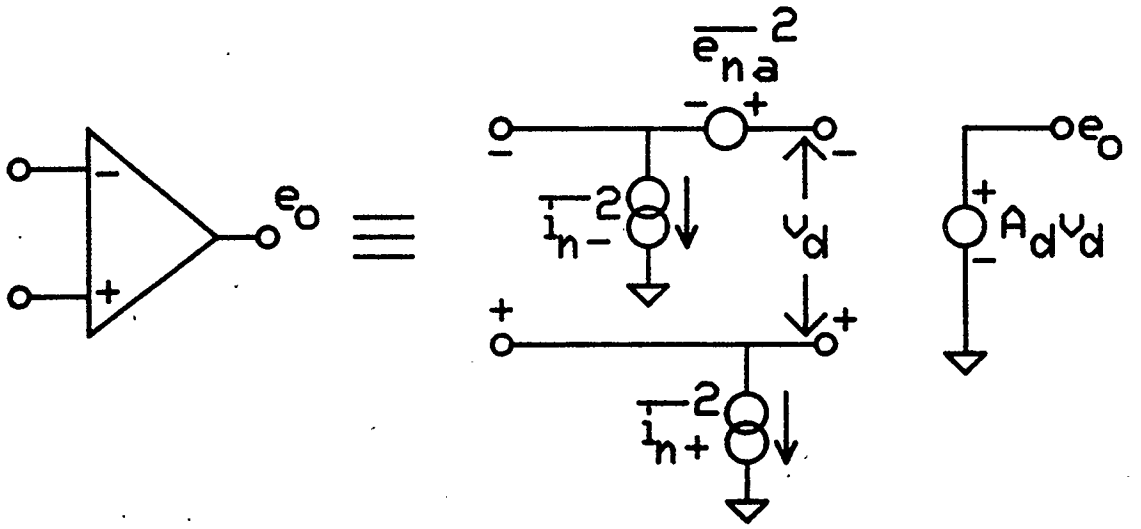
(b) negative input noise current generator (i_{n-}), $S_{i-} = S_i$;

(c) positive input noise current generator (i_{n+}), $S_{i+} = S_i$;

where S_e and S_i are the respective spectral density functions of the noise sources. The differential gain A_d of the amplifier, is assumed to have the form



(a)



(b)

Figure 4.1 - Equivalent noise models for (a) resistor; (b) operational amplifier.

$$A_d = \frac{A_{do}}{1 + j\frac{f}{f_o}} \tag{4.2}$$

where A_{do} is the dc gain and f_o is the pole frequency of the amplifier assuming a dominant pole model.

The contribution to the output noise voltage spectral density, S_{eo}, due to an individual noise voltage source, e_j, is given by

$$S_{eo} = S_{ej} |H_j(f)|^2 \tag{4.3}$$

where S_{ej} is the noise voltage spectral density of the source e_j and $H_j(f)$ is the transfer function from the source to the output. Similarly, the contribution to the output noise voltage spectral density, S_{io}, due to an individual noise current source, i_k, is given by

$$S_{io} = S_{ik} |Z_k(f)|^2 \tag{4.4}$$

where S_{ik} is the noise current spectral density of the source i_k and $Z_k(f)$ is the transfer impedance from the noise source to the output. The total output noise voltage spectral density is simply the sum of the individual output noise components. The mean-square output noise voltage, $\overline{E_{no}{}^2}$, is then given by

$$\overline{E_{no}{}^2}(f_l, f_h) = \sum_j \int_{f_l}^{f_h} S_{ej} |H_j(f)|^2 df + \sum_k \int_{f_l}^{f_h} S_{ik} |Z_k(f)|^2 df ; \quad (4.5)$$

where f_l and f_h are the low and high ends of the frequency range of interest.

Considering the above models, it is possible to develop an equivalent noise model for the SPWM as illustrated in Fig. 4.2. Note that only the amplifier section of the SPWM has been considered here. Using this model it is possible to estimate the output noise of the SPWM amplifier due to the internal noise sources. Table 4.1 provides a list of transfer functions and transfer impedances for the noise sources identified in Fig. 4.2. The output noise spectrum due to each source is determined by evaluating equations 4.3 and 4.4. The contribution to the mean-square output noise voltage is determined by evaluating eqn. 4.5.

In MOSFET amplifiers (and in most op amps), the output noise contribution due to the input noise current sources is extremely small in comparison to the contribution due to the input noise voltage source[11], and therefore can usually be neglected. Similarly, thermal noise generated in small resistors ($R < 100\,k\Omega$) will be small in comparison to the op amp input noise voltage, and in general can also be neglected. This assumption is used throughout the remainder of this chapter.

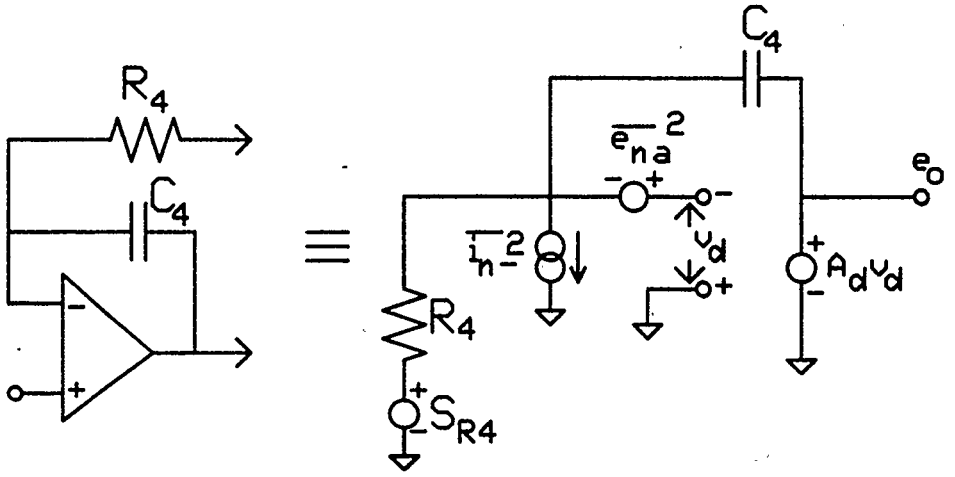


Figure 4.2 - Equivalent noise model for SPWM amplifier.

Table 4.1 - Transfer Functions and Transfer Impedances for SPWM Amplifier Noise Sources

Noise Source	Transfer Function or Transfer Impedance
R_4	$\frac{A_{do}}{D}$
e_{na}	$\frac{A_{do}(1 + j\omega C_4 R_4)}{D}$
i_{n-}	$\frac{A_{do} R_4}{D}$
i_{n+}	0

where,

$$D = 1 - (\frac{f}{f_P})^2 + j \frac{f}{f_P Q} ;$$

$$f_P^2 = \frac{f_o}{2\pi R_4 C_4} ;$$

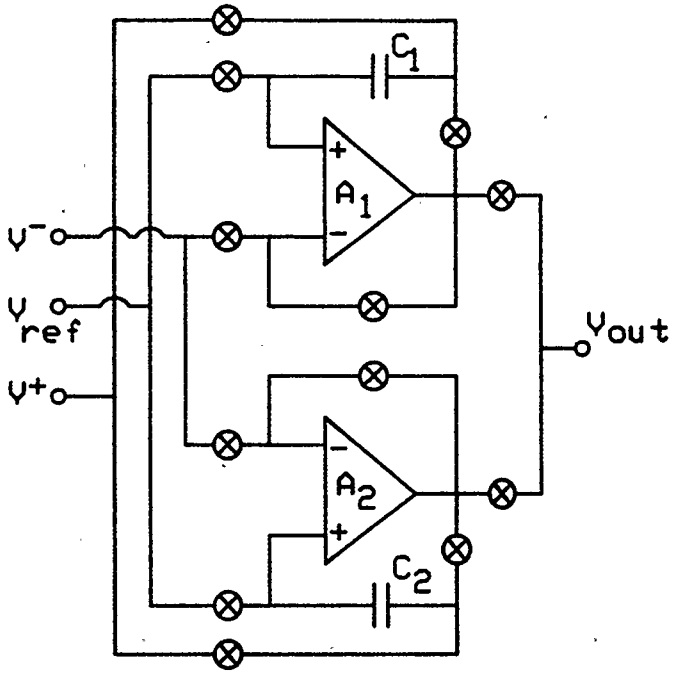
$$Q = \frac{1}{[\sqrt{2\pi f_o R_4 C_4}]^{-1} + (1 + A_{do})\sqrt{2\pi f_o R_4 C_4}} .$$

4.3 Noise Spectrum for SPWM

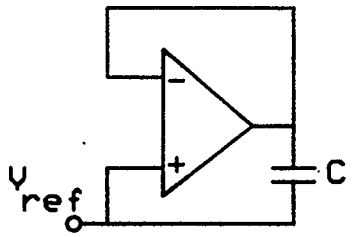
In low frequency systems, $1/f$ noise in active devices is the major source of internal noise. However, two types of operational amplifiers, chopper stabilized and commutating auto-zeroing (CAZ), use dc input offset reduction schemes which also have the effect of reducing low frequency noise. As a result, these types of op amps are ideal for precision low frequency applications.

The CAZ scheme is illustrated in Fig. 4.3(a)[14]. In this scheme two amplifiers are periodically switched between two modes of operation. In the auto-zeroing mode (Fig. 4.3(b)), the op amp is in a follower configuration and charges the capacitor to the input offset voltage plus the instantaneous low frequency noise voltage. In the signal processing mode (Fig. 4.3(c)), the capacitor is connected in series with the amplifier positive input terminal. If the switching of the op amp modes is done at a much higher frequency than the frequency of the $1/f$ noise, the effect will be to significantly reduce the dc offset and the low frequency noise.

A simplified block diagram of the ICL7650 op amp is provided in Fig. 4.4(a)[5]. This scheme consists of a main amplifier, which is always in the signal path, and a nulling amplifier which alternately nulls itself and the main amplifier. A model of the internal amplifiers is illustrated in Fig. 4.4(b). The input offset voltage (v_{os}) is modelled as an extra input to the amplifier. In addition, the amplifier includes an offset null adjustment (v_n) and the normal differential inputs



(a)



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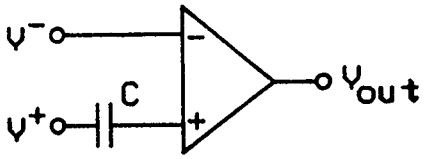
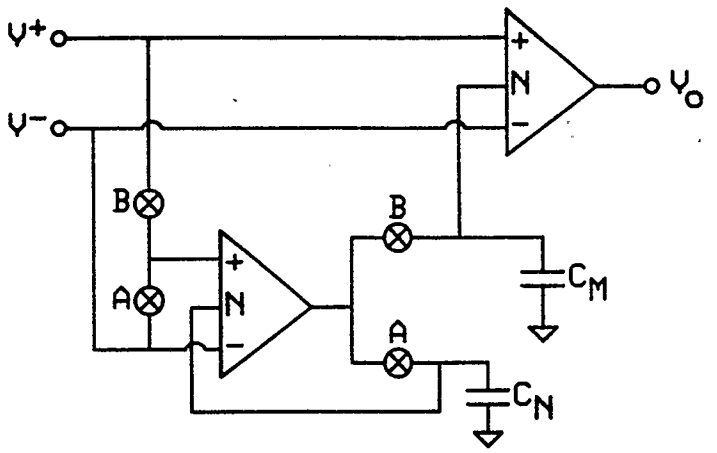
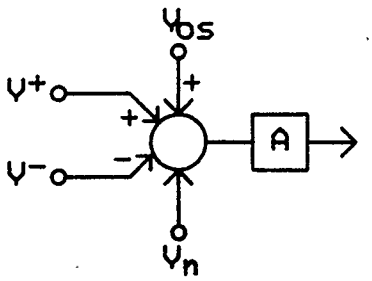


(c)

Figure 4.3 - CAZ operational amplifier; (a) block diagram; (b) auto-zeroing mode; (c) signal processing mode.



(a)



(b)

Figure 4.4 - ICL7650 operational amplifier; (a) simplified block diagram; (b) Internal model of individual amplifiers.

(v^+ and v^-).

The two operational modes are illustrated in Fig. 4.5. During the first phase (Fig. 4.5(a)), the nulling amplifier inputs are shorted and a voltage nearly identical to the offset of the nulling amp (v_{osn}) will be stored on the capacitor, C_N. This voltage is fed back to the amplifier null adjust input, reducing the effective offset voltage by a factor equal to the gain (A_N) of the nulling amplifier. That is, the input referred effective offset voltage of the nulling amplifier is given by

$$v_{os}\,(eff) = (\frac{1}{A_N + 1})\,v_{osn}\,. \tag{4.6}$$

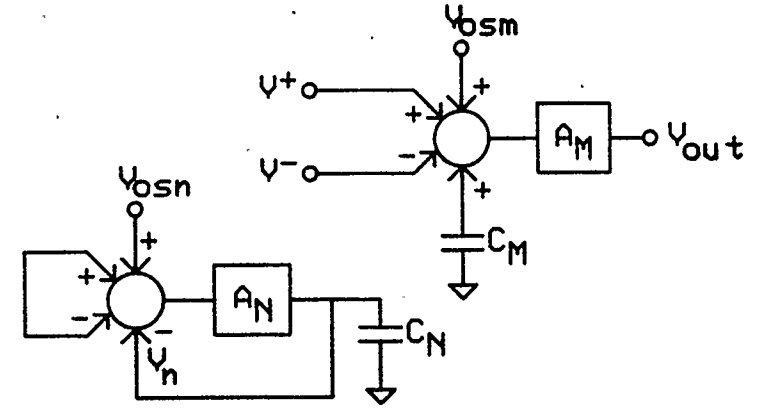
During the second phase (Fig. 4.5(b)), the nulling amp senses the differential inputs, amplifies the difference, and stores the result on C_M. The system output voltage is given by

$$v_{out} = A_M\,[v^+ - v^- + v_{osm} + A_N\,(v^+ - v^- + v_{os}\,(eff))] \tag{4.7}$$

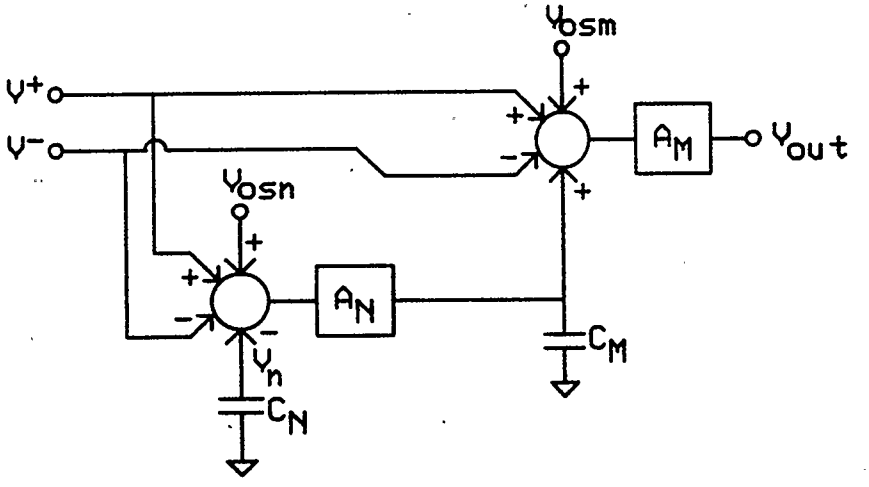
where A_M is the open loop gain of the main amplifier. It is then easy to show that

$$v_{out} = A_M\,A_N\,[v^+ - v^- + \frac{v_{osm} + v_{osn}}{A_N}], \tag{4.8}$$

provided $A_N \gg 1$. The effective offset is therefore the sum of the two amplifier offsets divided by the open loop gain of the nulling amplifier.



(a)



(b)

Figure 4.5 - ICL7650 op amp during (a) clock phase 1; (b) clock phase 2.

In order to demonstrate the reduction of low frequency noise, it is useful to analyze the nulling amplifier during two successive auto-zeroing clock phases as shown in Fig. 4.6. During Phase A (Fig. 4.6(a)), the nulling amplifier attempts to null itself by measuring the error due to the amplifier noise and dc offset. In this case, $v_1(t)$ is given by

$$v_1(t) = A_N\,(v_{noise}(t) - v_1(t)) \tag{4.9}$$

and it is easy to show that

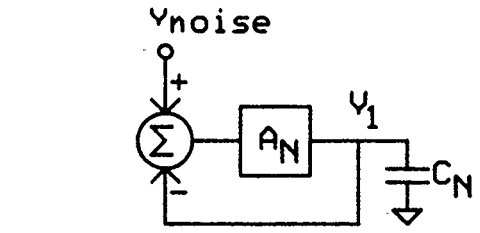
$$v_1(t) \approx v_{noise}(t). \tag{4.10}$$

This voltage is stored on C_N at the end of the autozeroing phase. During Phase B (Fig. 4.6(b)) the nulling amp is cascaded with the main amplifier. In this case, $v_1(t)$ can be shown to be

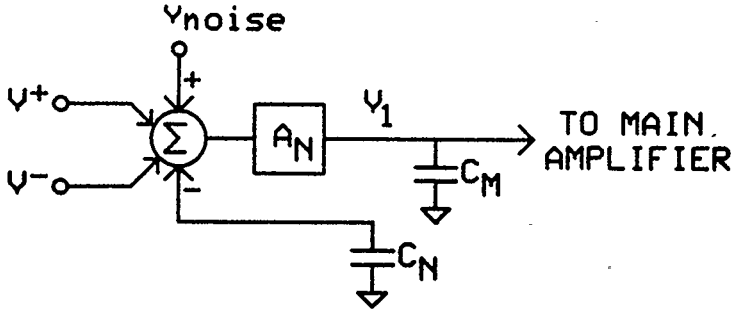
$$v_1(t) = A_N\,[v^+ - v^- + v_{noise}(t) - v_{CN}(t)], \tag{4.11}$$

where $v_{CN}(t)$ is the final voltage stored on C_N during Phase A.

Thus, comparing equations 4.10 and 4.11, the auto-zeroing scheme samples the noise (and the dc offset) during the first phase, and samples the signal plus the adjusted noise during the second phase. This arrangement can be approximated by the system shown in Fig. 4.6(c).



(a)



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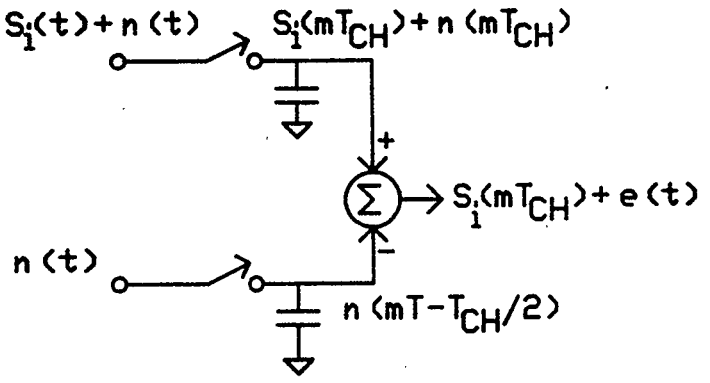


(c)

Figure 4.6 - Noise model for ICL7650 op amp; (a) Clock phase A; (b) Clock phase B; (c) Simplified analytical model.

The output signal of the system described by Fig. 4.6(c) corresponds to the sum of the input signal plus the corrected error of the system. The output error, then, is given by

$$e\,(mT_{CH}) = n\,(mT_{CH}) - n\,(mT_{CH} - T_{CH}/2). \tag{4.12}$$

The mean-square error, σ_e^2, corresponds to the mean-square output noise voltage and is given by

$$\sigma_e^2 = \overline{n^2\,(mT_{CH})} + \overline{n^2\,(m\,T_{CH} - T_{CH}/2)} - 2\overline{[n\,(m\,T_{CH})\,n\,(m\,T_{CH} - T_{CH}/2)]}. \tag{4.13}$$

Each of the right hand terms of eqn. 4.13 correspond to the auto-correlation function, $R_N\,(l)$ [15], of the noise signal and thus 4.13 can be rewritten as

$$\sigma_e^2 = 2R_N\,(0) - 2R_N\,(T_{CH}/2). \tag{4.14}$$

Examination of eqn. 4.14, leads to the observation that the output error will be smaller when the input error (ie. noise) between two successive auto-zeroing clock phases is well correlated, that is $R_N\,(0) \approx R_N\,(T_{CH}/2)$. This will be the case if the noise consists of predominantly low frequency components.

As an example, consider the case where $n\,(mT_{CH}) = A_n\,cos\,(\omega_n\,mT_{CH})$. $R_N\,(0)$ will be given by $A_n^2/2$, and $R_N\,(T_{CH}/2)$ will be given by

$$R_N(T_{CH}/2) = \frac{A_n^2}{2} cos\left[\frac{\omega_n T_{CH}}{2}\right], \tag{4.15}$$

and therefore, eqn. 4.14 can be rewritten as

$$\sigma_e^2 = \frac{A_n^2}{2}\left[1 - cos(\frac{\pi f_N}{f_{CH}})\right]; \tag{4.16}$$

where f_N is the frequency of the input noise signal $n(mT_{CH})$. Fig. 4.7 shows the output error, σ_e^2, as a function of the frequency, f_N, for the case where $A_n = \sqrt{2}$. It can be seen from Fig. 4.7 that low frequencies ($f_N \ll f_{CH}$) are attenuated significantly, while frequencies near the auto-zeroing clock frequency (f_{CH}) are actually enhanced.

It should be noted here that the system described above is only an approximation of how the ICL7650 auto-zeroing scheme operates. The approximations are valid when considering frequencies below the auto-zeroing clock frequency. Inspection of Fig. 4.6(b) and eqn. 4.11 indicate that the output noise signal, due to the nulling amplifier, is continuous during clock phase B, and not sampled as suggested by the simplified noise model. If the noise signal contains frequency components approaching the auto-zeroing clock frequency, there will be somewhat more output noise than that predicted by eqn. 4.16. Also, for frequency components above the auto-zeroing clock frequency, there will be an aliasing effect

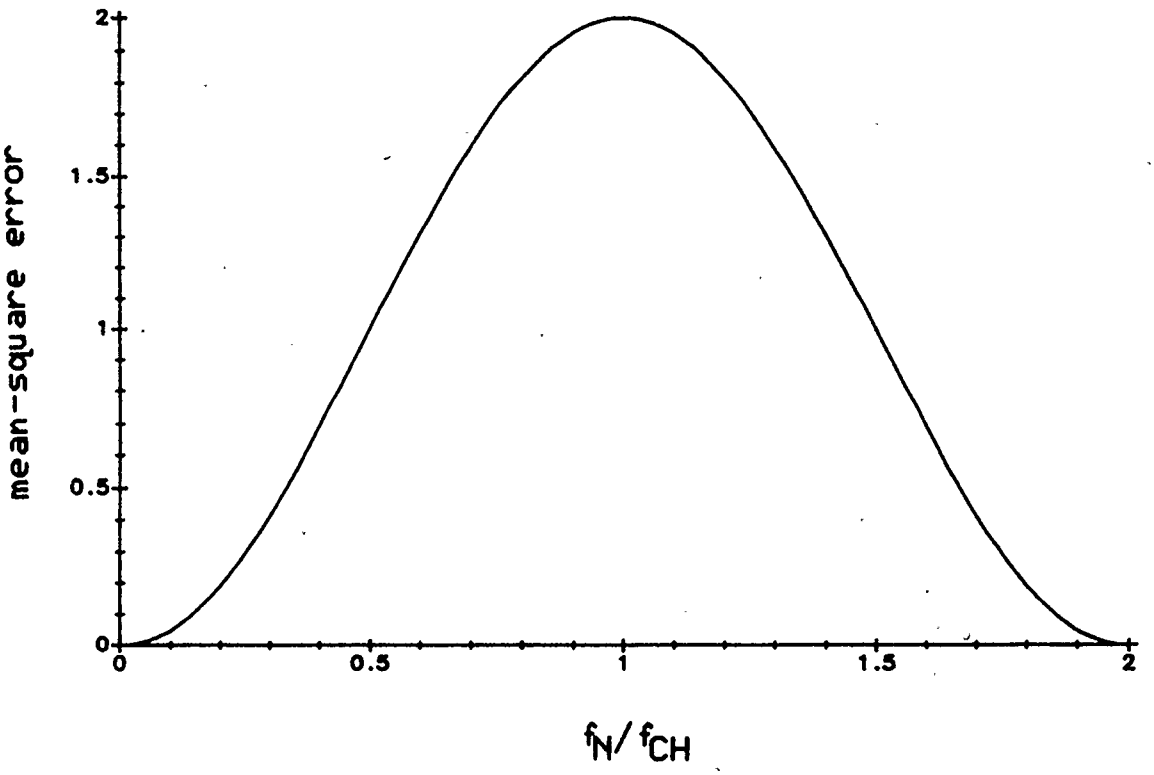


Figure 4.7 - Mean-square error as a function of input noise frequency, f_N.

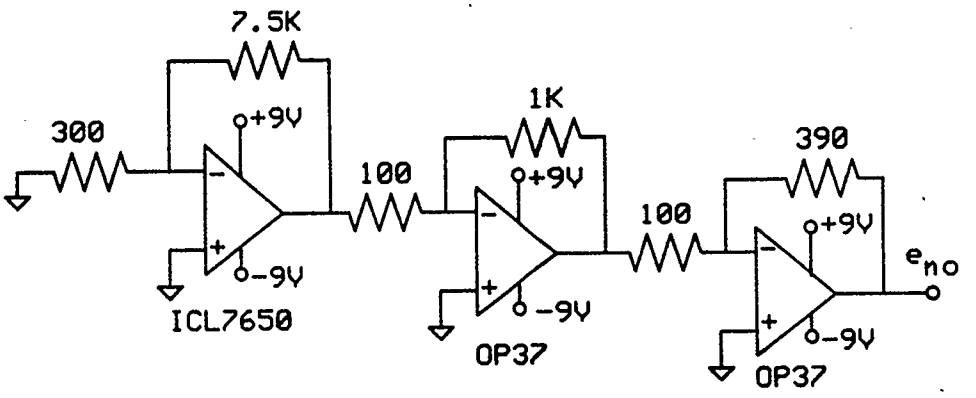
caused by the sampling of the auto-zeroing scheme. Analysis of these mechanisms is difficult and beyond the scope of this thesis.

In order to verify the theoretical consequences of the auto-zeroing scheme described here, output noise measurements were performed on the test circuit illustrated in Fig. 4.8(a). Amplifier noise power spectrum measurements were carried out using an HP5423A Structural Dynamic Analyzer[16]. In addition, measurement of the rms output noise voltage was done using a Data Precision model 3600 true rms digital multimeter.

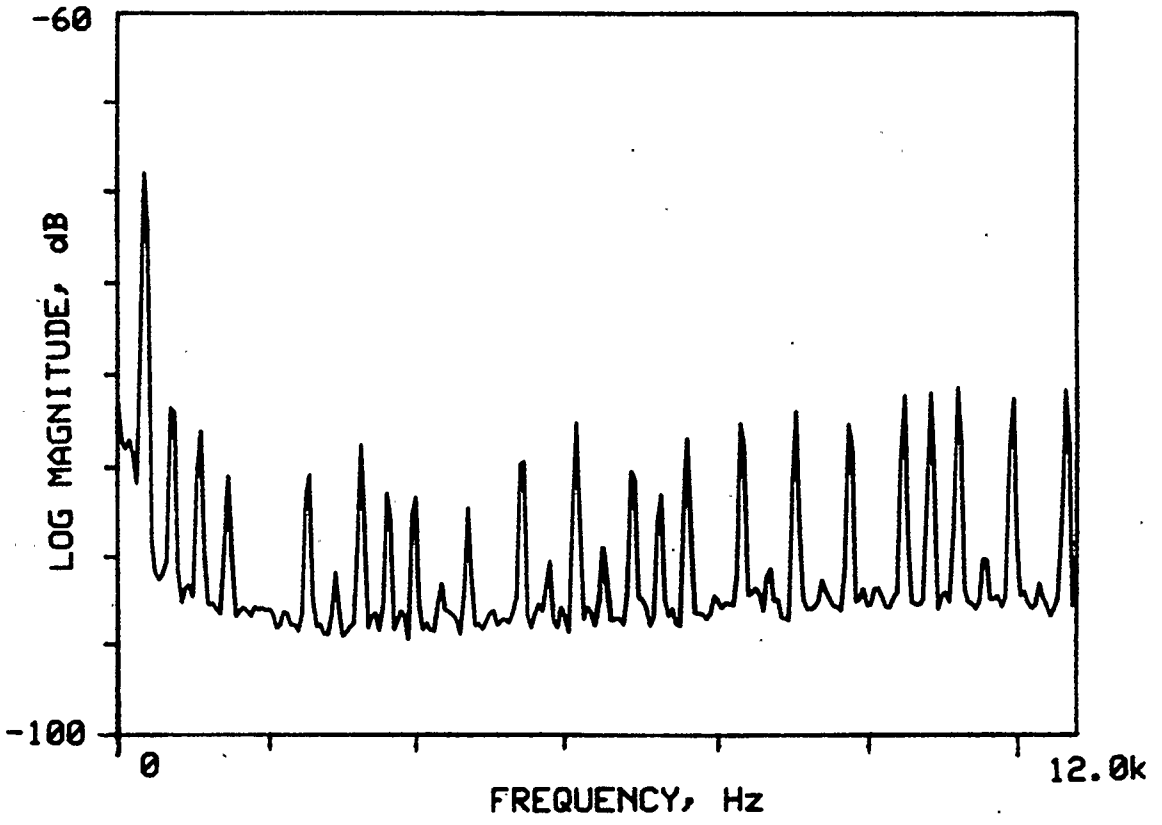
Fig. 4.8(b) illustrates the output noise power spectrum of the test circuit for a measurement bandwidth of 12.3 kHz. The evenly spaced spikes correspond to the auto-zeroing clock frequency (f_{CH}) and its harmonic frequencies. Fig. 4.9 shows the same circuit using a measurement bandwidth of 1.6 kHz. Here the auto-zeroing clock frequencies are distinct from the remainder of the noise spectrum.

Fig. 4.10 shows the output noise power spectrum for a measurement bandwidth of 12 Hz. In this case, the noise spectrum is relatively flat, indicating that the low frequency ($1/f$) noise components have been attenuated.

The results of the noise spectrum measurements indicate that the ICL7650 auto-zeroing scheme does attenuate low frequency noise, as predicted in the above discussion. In addition, the amplifier output noise is concentrated in frequencies near the auto-zeroing clock frequency and its harmonics (as predicted above).



(a)



(b)

Figure 4.8 - (a) Test circuit for ICL7650 noise spectral density measurements; (b) Measured output noise spectrum for 12 kHz bandwidth (referred to 1 V^2/Hz).

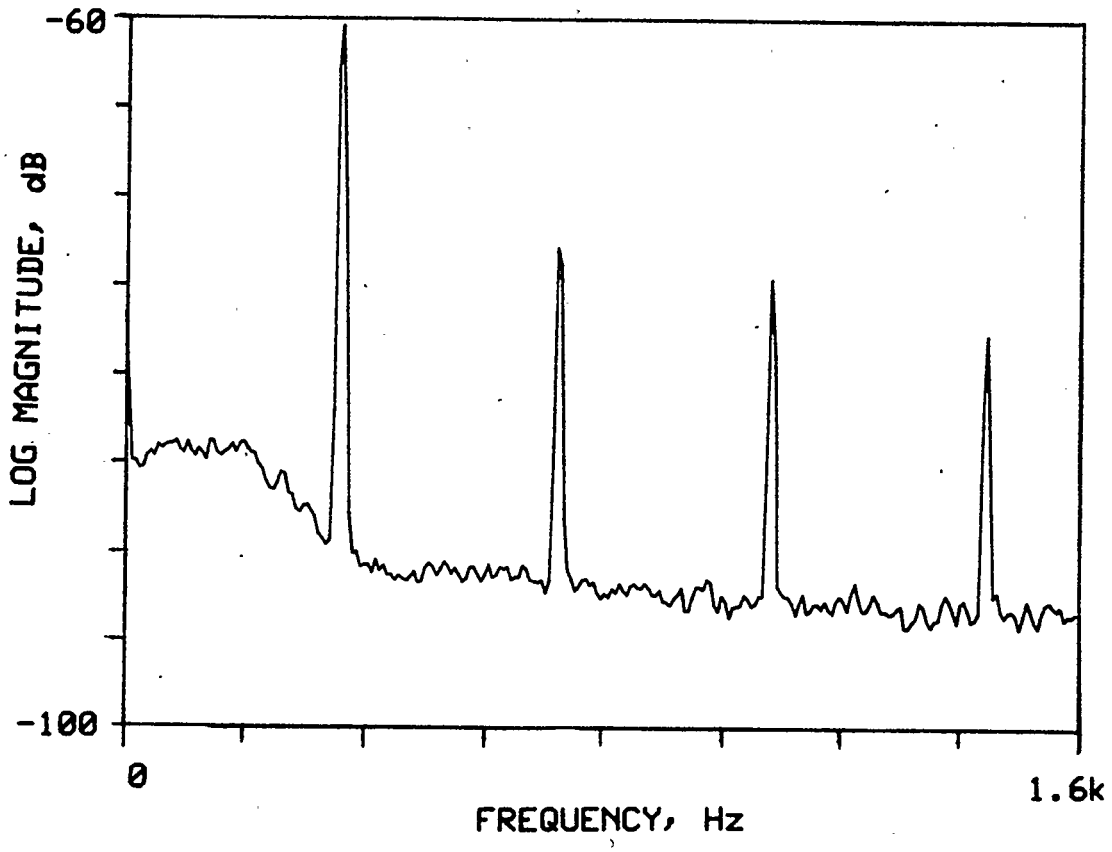


Figure 4.9 - Measured output noise spectrum for 1.6 kHz bandwidth (referred to 1 V^2/Hz).

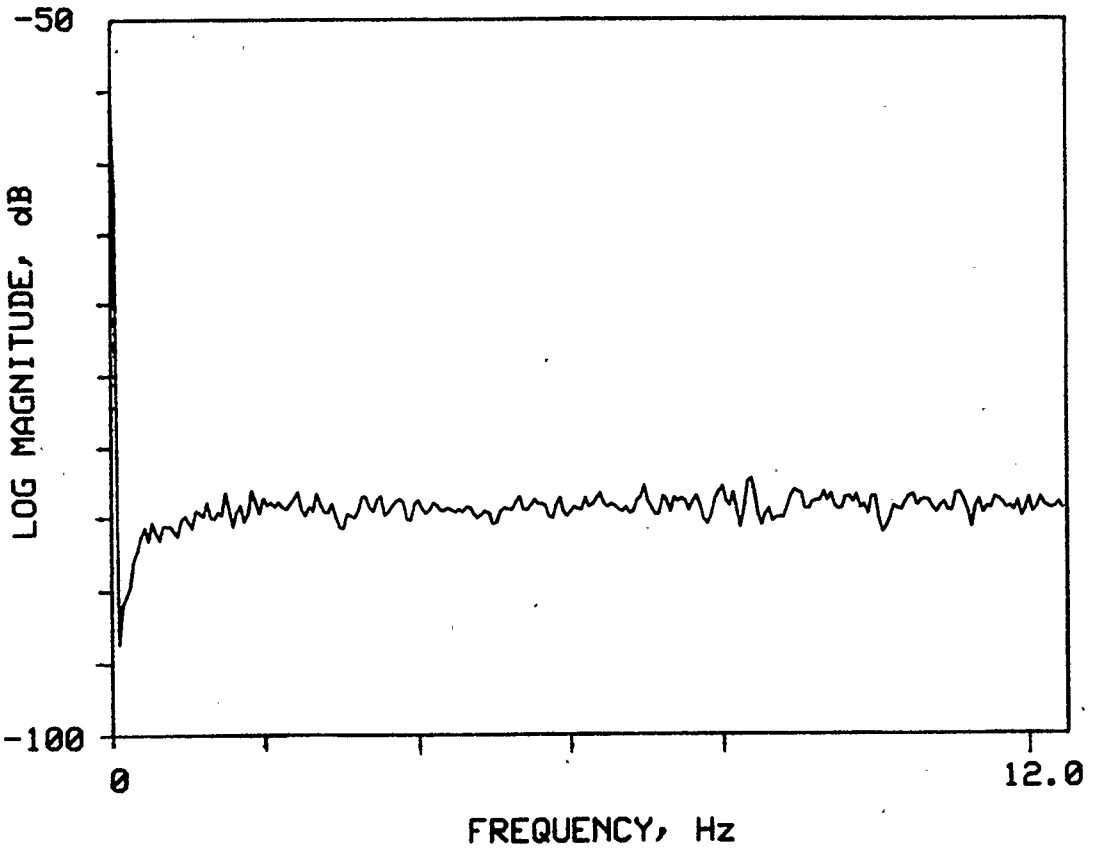


Figure 4.10 - Measured output noise spectrum for 12 Hz bandwidth (referred to 1 V^2/Hz).

The amplifier input referred noise voltage power spectral density, S_{ena}, can be determined from the noise power measurements by using eqn. 4.3. The transfer function of the test circuit is

$$H_{TEST}(f) \approx \frac{A_o}{1 + j\frac{f}{f_o}}, \tag{4.17}$$

where $f_o \approx 40$ kHz and $A_o \approx 1000$. The input referred noise spectral density, S_{ena}, will then be

$$S_{ena}(f) = \frac{S_{eout}(f)}{|H_{TEST}(f)|^2}, \tag{4.18}$$

where $S_{eout}(f)$ is the measured output noise power spectral density. Since the noise frequencies of interest are well below the cutoff frequency (f_o) of the test circuit, S_{ena} can be approximated by

$$S_{ena}(f) \approx \frac{S_{eout}(f)}{A_o^2}. \tag{4.19}$$

Thus, $S_{ena}(f)$ for the range $f \leq 12$ Hz can be estimated from Fig. 4.10 to be

$$S_{ena}(f \leq 12\,Hz) \approx 3.1 \times 10^{-15}\ volts^2/Hz. \tag{4.20}$$

4.4 Synchronized PWM Resolution Considerations

As discussed previously, the resolution of the SPWM will be largely limited by the input noise voltage of the operational amplifier. There are, however, several other factors which will also affect the resolution of the converter.

The choice of passive components (R_4 and C_4) will affect the resolution in two ways. First, the resistor and capacitor affect the integrator transfer function, $H(f)$. For example, the transfer function for the amplifier input referred noise voltage, e_{na}, is given by

$$H_{en}(f) = A_{do} \frac{(1 + j\frac{f}{f_1})}{1 - (\frac{f}{f_P})^2 + j\frac{f}{f_P Q}}; \qquad (4.21)$$

where,

$$f_P{}^2 = \frac{f_o}{2\pi R_4 C_4};$$

$$Q = \frac{1}{(1 + A_{do})\sqrt{2\pi f_o R_4 C_4} + [\sqrt{2\pi f_o R_4 C_4}]^{-1}};$$

and

$$f_1 = \frac{1}{2\pi R_4 C_4}.$$

The magnitude response, $|H_{en}(f)|^2$, will be given by

$$|H_{en}(f)|^2 \approx \frac{A_{do}^2\left[1+(\frac{f}{f_1})^2\right]}{1+\left[\frac{f}{f_P Q}\right]^2+\left[\frac{f}{f_P}\right]^4}; \qquad (4.22)$$

assuming $Q \ll 1$. Fig. 4.11 shows the magnitude response $|H_{en}(f)|^2$ for the case where, $A_{do} = 1.0\times10^7$, $f_o = 0.01\,Hz$ (as estimated from ICL7650 specifications), $R_4 = 3.0\,k\Omega$, and for C_4 = 1.0, 10.0, and 100.0 nF. Fig. 4.11 indicates that the noise bandwidth is reduced as the value of the feedback capacitance, C_4, is increased. This suggests that the resolution should improve for larger values of C_4, assuming that R_4 remains constant.

The resistor - capacitor combination will also determine the amplitude of the triangular wave at the integrator output. Analysis of the SPWM indicates that the amplitude of the integrator output triangle wave is inversely proportional to both the operating frequency f_R and the RC integrator time constant. That is,

$$AMPLITUDE \;\alpha\; \frac{1}{f_R R_4 C_4}. \qquad (4.23)$$

Thus, increasing R_4C_4 will decrease the amplitude of the triangular wave. If the amplitude of the output triangle wave is small, the stability of the threshold detection gate of the SPWM will significantly affect the resolution of the converter.

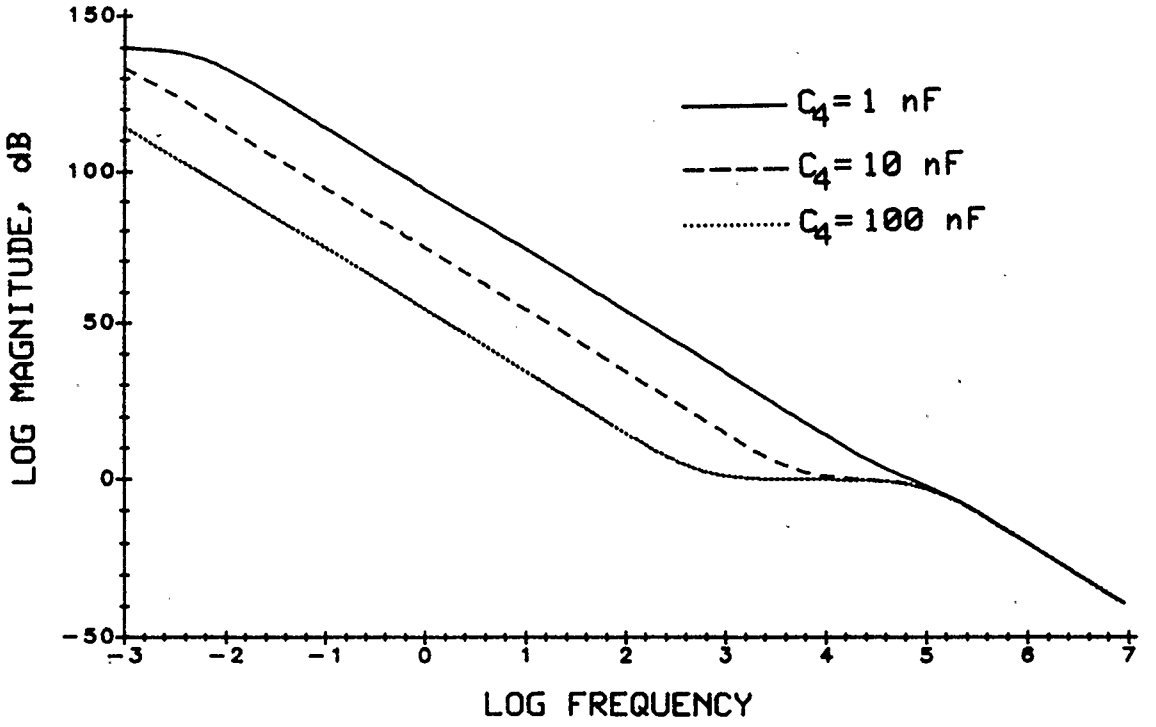


Figure 4.11 - SPWM output magnitude $|H_{en}(f)|^2$ for different feedback capacitance.

A second factor which will affect the SPWM resolution is the auto-zeroing clock frequency (f_{CH}) of the SPWM amplifier. This can be seen by reconsidering eqn. 4.16 (restated here for convenience) :

$$\sigma_e^2 = \frac{A_n^2}{2}\left[1 - cos\left[\frac{\pi f_N}{f_{CH}}\right]\right]. \qquad (4.16)$$

If f_{CH} is increased, the low frequency noise will be attenuated by a greater amount. In addition, the low frequency bandwidth over which the noise is attenuated is also increased. If the circuit is bandlimited (as is the case for the SPWM), increasing the auto-zeroing clock frequency will reduce the amplifier output noise and therefore improve the resolution of the converter. This relationship is illustrated in Fig. 4.12, where eqn. 4.16 is plotted for several values of f_{CH}.

A third factor which will influence the resolution is the conversion time, $T_{convert}$. This can be seen intuitively by noting that the circuit noise is averaged over the total conversion period. If the average noise over a long time period is zero, it then follows that increasing the conversion time will decrease the average value of the noise over the conversion period, and thus lower the error due to the noise.

An estimate of the rms error of the converter can be obtained by considering the following. Assume a signal, $x(t)$, with a true mean value μ_x. For a single

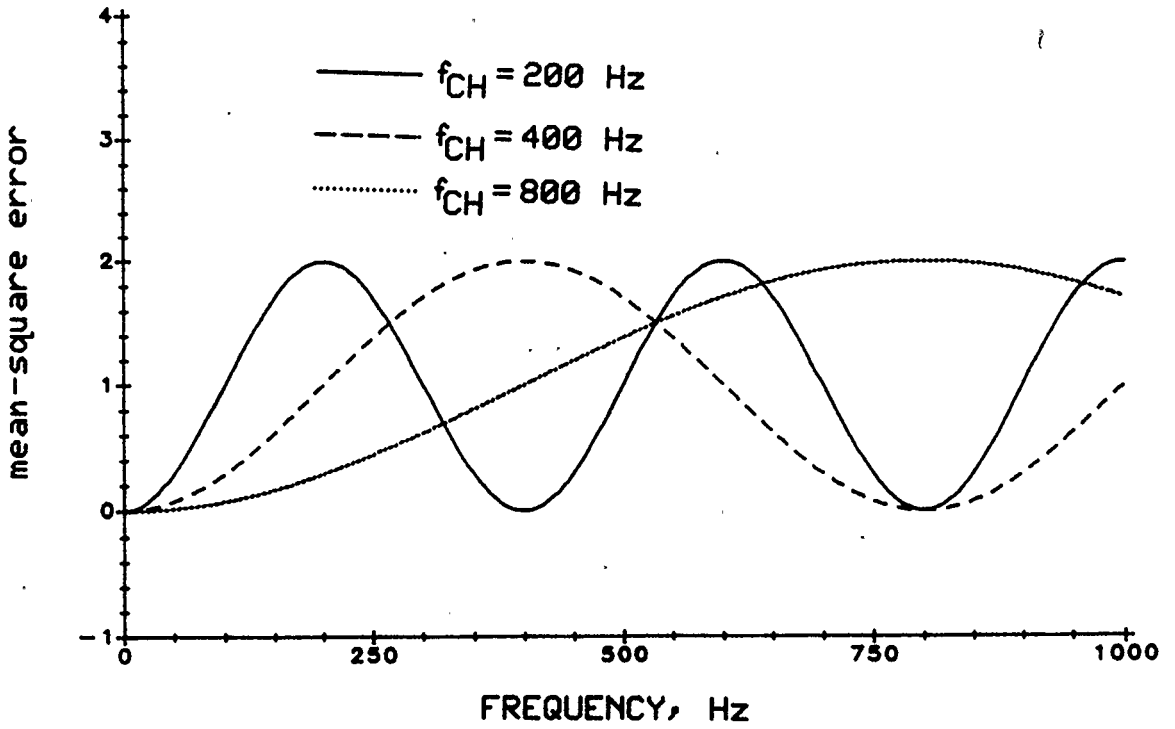


Figure 4.12 - Mean-square error for different auto-zeroing clock frequencies.

conversion, the estimated mean value, μ_{xe}, will be given by

$$\mu_{xe} = \frac{1}{T_{convert}} \int_0^{T_{convert}} x(t)\,dt, \tag{4.24}$$

and the error in the estimate will be

$$e_x = \mu_x - \mu_{xe}. \tag{4.25}$$

If μ_{xe} is unbiased (the average value of $e_x = 0$), the mean square error will be given by the variance of μ_{xe}. For the case where $x(t)$ is bandlimited white noise, the variance of μ_{xe} can be approximated by[17]

$$var[\mu_{xe}] = \frac{\sigma_x^2}{2B\,T_{convert}}, \tag{4.26}$$

where B is the bandwidth and σ_x^2 is the variance of μ_x. If $\mu_x \neq 0$, the normalized standard error or rms error is given by

$$\varepsilon = \frac{\sqrt{var[\mu_{xe}]}}{\mu_x} = \frac{\sigma_x}{\sqrt{2B\,T_{convert}}\,\mu_x}. \tag{4.27}$$

Inspection of eqn 4.27 indicates that the rms error will be proportional to $\frac{1}{\sqrt{2T_{convert}}}$.

In terms of the SPWM ADC, the rms error is given by

$$\varepsilon_{SPWM} = \frac{1}{\sqrt{2T_{convert}}} \frac{\sqrt{S_{ena}}}{V_t}. \tag{4.28}$$

Thus, for example, if $S_{ena} = 3.1 \times 10^{-15}\ volts^2/Hz$ (from eqn. 4.20), $V_t = 36\ mV$, and $T_{convert} = 0.5$ seconds, the predicted rms error will be

$$\varepsilon_{SPWM} = 1.6 \times 10^{-6}. \tag{4.29}$$

which corresponds to a resolution of 1.6 parts per million.

The operating frequency of the SPWM, f_R, will also affect the converter resolution. If the operating frequency is increased (assuming $T_{convert}$ remains constant), then the number of times that the triangular wave crosses the switching threshold of the SPWM RS flip flop will also increase. If the variability of the threshold voltage is modelled as a noise voltage, then the average noise voltage will approach zero as the number of threshold crossings increases. This leads to the conclusion that the resolution will improve if the SPWM operating frequency is increased.

4.5 Synchronized PWM Resolution Measurements

The resolution of the SPWM ADC was tested using the circuit implementation shown in Fig. 4.13. Note that this implementation is a SPWM with gain. The ADC output count, N, for the circuit is given by

$$N = m\,n\left[1+\frac{R_4}{R_1}\right]\frac{V_t}{V_{ref}}. \tag{4.30}$$

Component values of $R_4 = 300\,k\Omega$ and $R_1 = 3\,k\Omega$ were selected in order to provide a gain of approximately 100. The actual resistors used were low temperature coefficient precision resistors. This was done to minimize measurement error due to thermal drift. The circuit input voltage, V_t, was a constant dc value of approximately 36 millivolts, in an attempt to simulate a pressure transducer with a full scale output of about 36 millivolts. The SPWM was laid out to minimize external interference and powered from a regulated dc supply of 10 volts.

Eqn's. 4.24 - 4.29 indicate that the resolution can be determined from the rms error. For the SPWM ADC, the rms error corresponds to the standard deviation of the output count, N, for a large number of conversions. For example, eqn. 4.29 suggests that the expected standard deviation of N should be 1.6 ppm for a conversion time of 0.5 seconds.

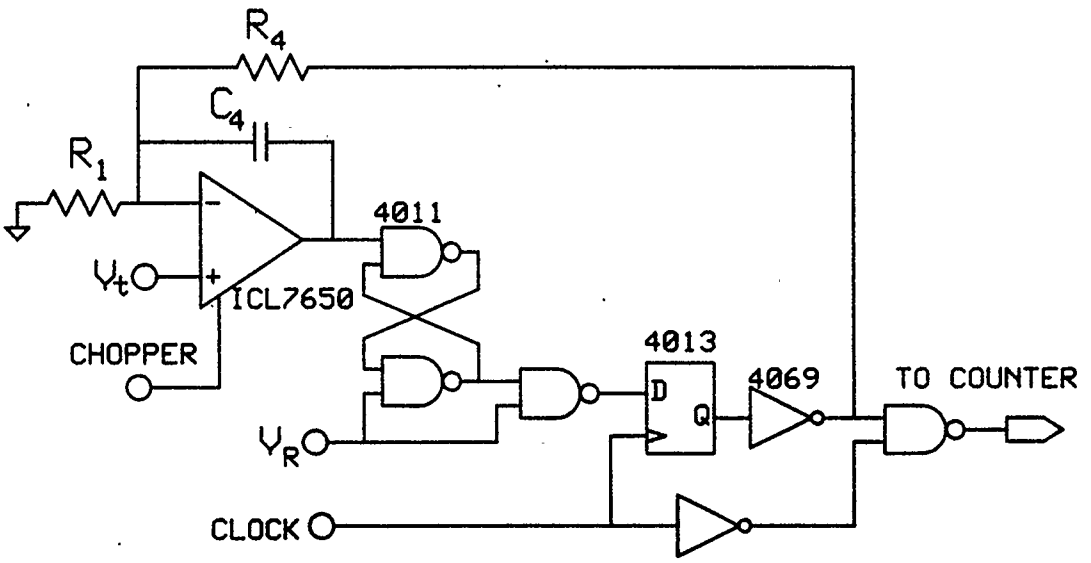
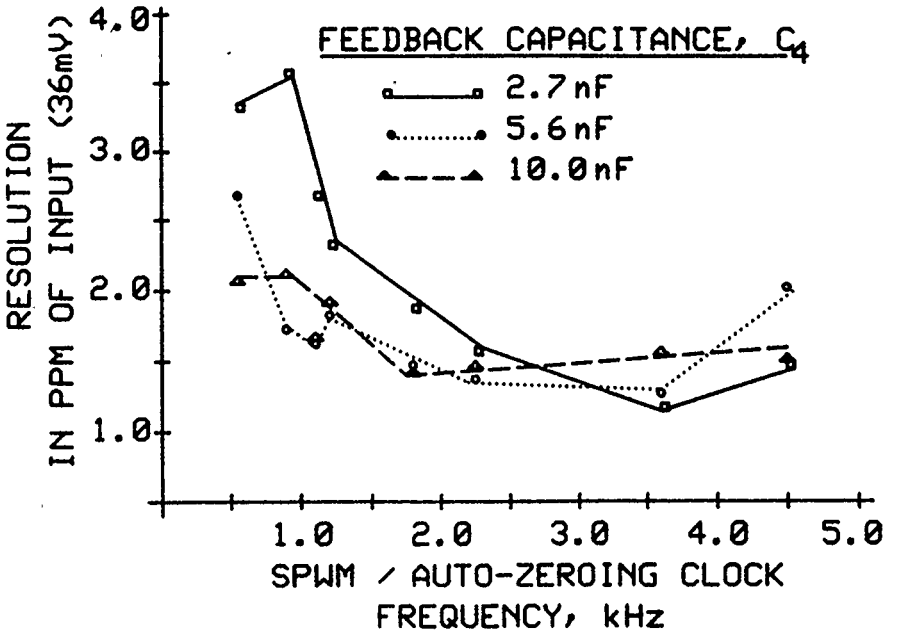


Figure 4.13 - Test circuit for SPWM ADC resolution measurements.

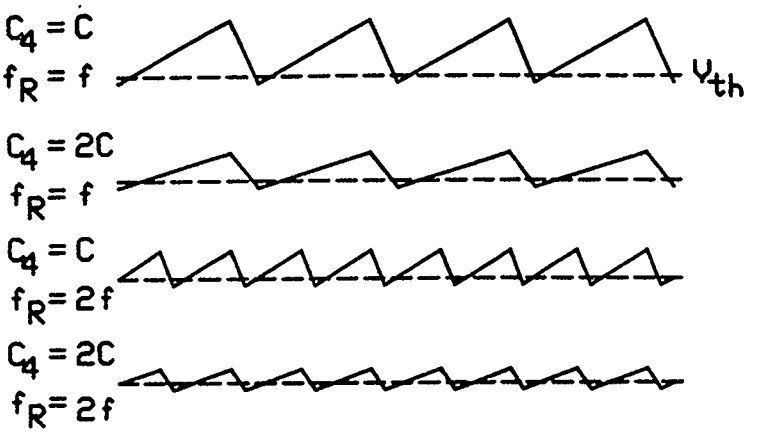
The resolution was tested under several different operating conditions to determine the significance of various parameters, including the auto-zeroing clock frequency, f_{CH}, the SPWM operating frequency, f_R, the feedback capacitor, C_4, and the conversion time, $T_{convert}$.

Test results are given in Fig. 4.14 thru Fig. 4.16. Fig. 4.14(a) shows the effect of C_4 for different SPWM operating frequencies. At lower operating frequencies, the resolution is better for larger values of C_4, indicating that the narrower bandwidth, due to the larger capacitance, is significant at lower operating frequencies ($f_R < 2\,kHz$). For operating frequencies above 2 kHz, the resolution is somewhat better when a smaller capacitor is used.

An explanation for this result can be obtained by considering the integrator output waveform for different values of both C_4 and f_R as illustrated in Fig. 4.14(b). If C_4 is large, the output voltage will ramp slowly and the SPWM will be more sensitive to instabilities in the threshold level than for a smaller capacitance. If the frequency is increased, the amplitude of the triangle wave will decrease. As a result, the likelihood of a false detection will increase, since the output voltage will be near the threshold voltage for a proportionally longer time. The larger number of false detections will lead to a reduction in the resolution of the converter.



(a)



(b)

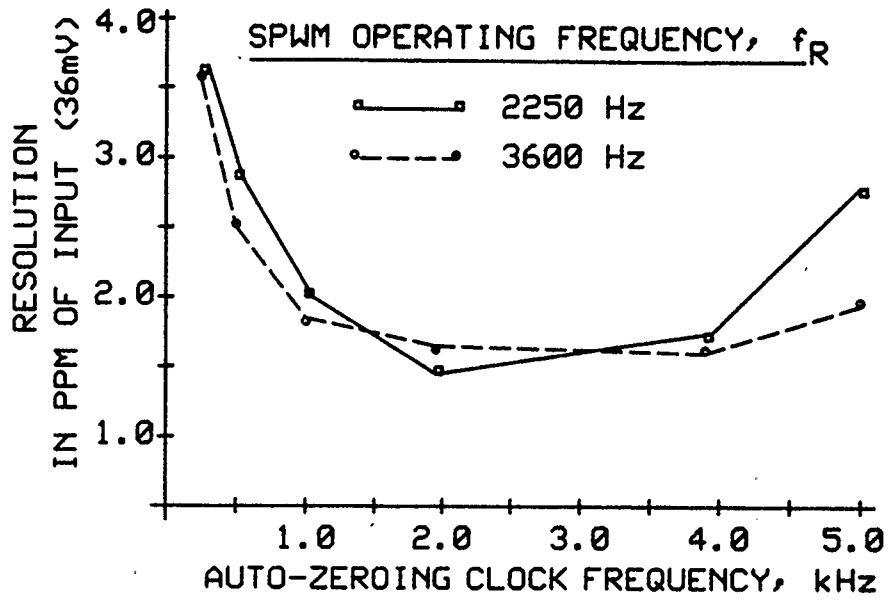
Figure 4.14 - (a) SPWM resolution for different feedback capacitance; (b) Effect of C_4 and operating frequency on SPWM integrator output.

Fig. 4.15(a) shows the effect of the auto-zeroing clock frequency, f_{CH}, on the resolution. As expected, the resolution improves as the clock frequency is increased from 244 Hz to about 2 kHz. However, the error increases for higher auto-zeroing clock frequencies ($f_{CH} = 3.9\,kHz\,,\ 7.8\,kHz$). This is possibly due to fluctuations in the amplifier input currents caused by clock feedthrough.

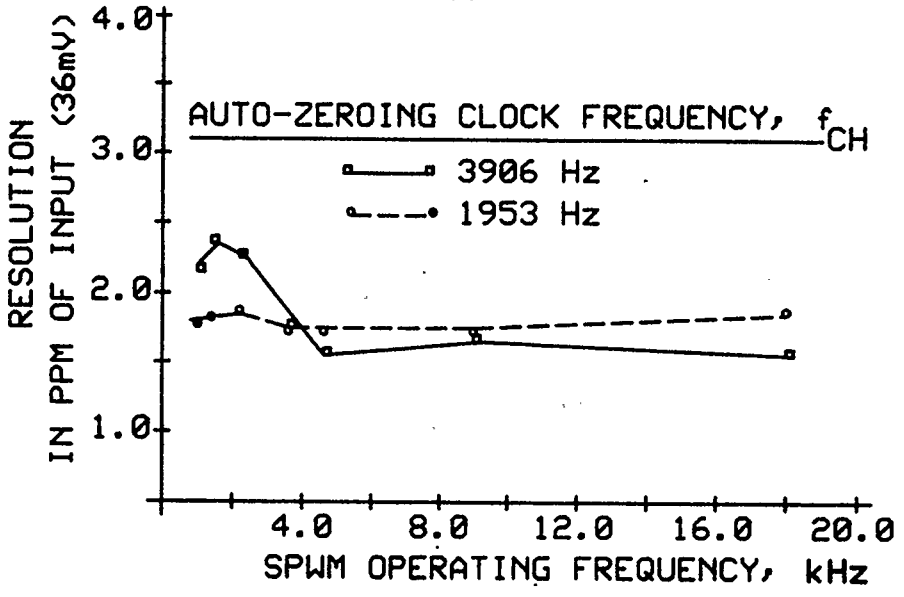
Fig. 4.15(b) shows the relationship between the SPWM operating frequency, f_R, and the resolution. The results indicate that the resolution improves slightly at higher SPWM frequencies, supporting the theory of the previous section.

Fig. 4.16 compares the resolution for different conversion times to that predicted by eqn. 4.28 assuming (1) the power spectral density, S_{ena}, from eqn. 4.20, and (2) using the measured resolution for a conversion time of 0.555 seconds and eqn. 4.28 to predict the resolution for longer conversion times. The experimental results show a fair agreement with theoretical expectations. Differences can be partially accounted for by noting that the amplifier output noise is not white as assumed by eqn. 4.28.

The results indicate that the input referred noise voltage of the ICL7650 op amp (as determined from the noise voltage power spectrum measurements of section 4.3) is the major noise source in the SPWM ADC. Other sources of error include the stability of the threshold detection gate, fluctuations in the amplifier input currents due to clock feedthrough, and various extraneous noise sources such



(a)



(b)

Figure 4.15 - SPWM resolution for (a) different auto-zeroing clock frequencies; (b) different operating frequencies.

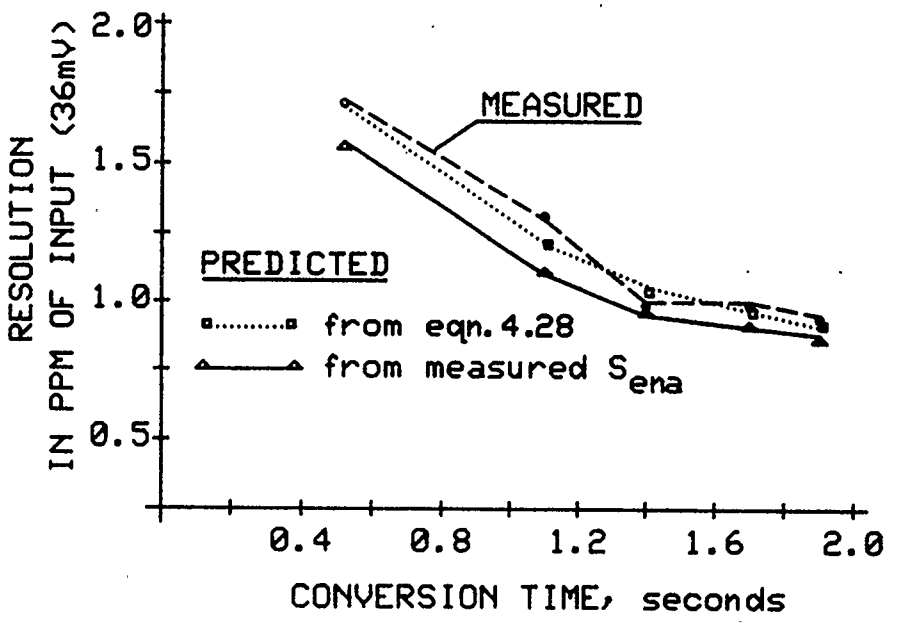


Figure 4.16 - SPWM resolution as a function of conversion time.

as the analog/digital interface of the measuring system.

The experimental results are summarized as follows :

(1) Resolution of the SPWM is affected by the passive components (R_4, R_1, C_4) of the circuit. It was found that a choice must be made between minimizing the noise bandwidth and maximizing the amplitude of the triangular waveform at the output of the integrator. If the SPWM is operated at low frequencies (f_R < 2kHz), the feedback capacitance C_4 should be selected to reduce the noise bandwidth. At higher SPWM operating frequencies, C_4 should be selected to maximize the amplitude of the integrator output triangle wave.

(2) The resolution can be improved by increasing the amplifier auto-zeroing clock frequency (f_{CH}) and/or by increasing the SPWM operating frequency (f_R).

(3) Increasing the conversion time will improve the ADC resolution and the amount of improvement can be approximately predicted using eqn. 4.28.

(5) If the operating frequency and auto-zeroing clock frequency are the same (ie. $f_R = f_{CH}$) and set to a moderate frequency (approximately 3 kHz), the resolution will be slightly improved in comparison to having different operating and auto-zeroing clock frequencies. By doing so, the overall achievable resolution for the SPWM ADC with a gain of 100 and a conversion time of 0.9 seconds is about 1.3

ppm. This corresponds to a resolvability of approximately 50 nanovolts.

CHAPTER 5

A PRECISION DATA ACQUISITION UNIT

5.1 Introduction

In chapters 3 and 4, a precision analog-to-digital converter was presented. In practical systems, the ADC is embedded within a complete digital control or acquisition unit. This may be as simple as a digital multimeter (DMM), where the ADC output is converted to a decimal value and then displayed. Alternatively, the ADC might be a subset of a data acquisition unit (DAU). The DAU may then serve as a remote terminal unit (RTU) for a large remote control system.

In a DAU, the digital circuitry serves a number of purposes which may include :

- data conversion
- ADC calibration, error correction, and control
- communication and data transfer

- diagnostic analysis

The type of digital system required depends on the operating conditions and the particular application. Normally, a DAU is developed according to a list of specifications. These specifications include environmental considerations such as size, power consumption, and temperature limitations, as well as performance and functional criterion.

This chapter presents the development of a microcontroller based data acquisition unit incorporating the synchronized PWM ADC. System specifications are presented along with possible alternatives, followed by a discussion of the DAU architecture chosen. As an example of the error compensation capabilities of the DAU, temperature sensitivity measurements for the SPWM ADC will be presented. Finally, recommendations for improvement of the DAU will be given.

5.2 DAU Specifications

As suggested in the introduction, the DAU specifications can be divided into two types, environmental and performance/functional. Typically, a trade-off between these two is necessary. It is therefore useful to consider both specifications in detail.

Environmental

A typical application of the synchronized PWM ADC is in oilfield pressure measurements where the ADC input is the output of a pressure transducer[18]. As a result, it is possible that the DAU would be contained in a compact battery operated unit. It is also likely that the DAU would be required to withstand temperatures over a large range (for example, $-55°C$ to $125°C$). Considering these possibilities, the DAU environmental specifications can be listed as follows :

- compact in size (minimum component count)
- low power consumption (CMOS components)
- power down capabilities
- military temperature specifications.

Performance / Functional

The SPWM ADC is a low frequency converter with a 20 bit resolution conversion time of about 1 second. Therefore, a high speed DAU is not a key specification in this design. Of greater concern are functional capabilities as discussed below:

(1) Communications Interface

A communcations interface is an essential feature which allows the DAU to transfer data and control information to and from a remote host computer. This is

normally accomplished using a Universal Asynchronous Receiver Transmitter (UART) via an RS-232 serial interface[19].

(2) Timers/Counters

The SPWM ADC requires counters to produce waveforms for its operation. In addition, timer/counters are used to generate baud rates for the serial interface and to implement a real time clock.

(3) Versatile Interface

A typical remote terminal unit (RTU) may include several peripheral devices such as multiple converters and/or digital inputs and outputs. Providing a versatile interface makes the DAU easily expandable.

(4) Memory Accessability

In certain applications, the DAU may be required to take readings for a long period of time and store data onboard. It is therefore desirable that the DAU have the capability of accessing a large data memory.

(5) Processing Capabilities

Although high speed numerical processing is not a requirement of the DAU, the ability to implement simple arithmetic is necessary for various purposes including calibration and measurement.

(6) Development Time

Previous discussion suggests that the DAU should be flexible and expandable. This is important if the same basic unit is to be used for different applications requiring various options. In consideration of this, a simple low cost system with a short development time is best.

Based on these specifications, one of two approaches can be used to develop a DAU. They are (1) a microprocessor-based implementation, or (2) a microcontroller-based implementation.

A microprocessor-based DAU would have the advantage of speed. In addition it would have a fairly flexible interface and large memory accessability. However, additional peripheral devices would be required to realize functions such as serial communications and time measurement. The additional components lead to a larger system with increased power consumption.

A microcontroller-based DAU solves the problem of system size by integrating several functions on one chip. In addition, a microcontroller-based system would have the advantages of flexibility, low cost, and short development time[20]. In consideration of these advantages, a microcontroller-based implementation was chosen.

Several commercial microcontrollers are available which would realize the given specifications. Microcontrollers are available in 8 and 16-bit variations and

common features include A/D converters, serial communications interface, programmable memory(PROM), random access memory (RAM), and 16-bit timer/counters[20].

For the purpose of the DAU specified, the Intel 80C31 was considered to be the optimum device, based on cost, functionality, and availability. Although more power is available in other devices (Intel 8096 and the Motorola 68HC11 for example), the 80C31 provides a serial interface, two timer/counters, a flexible interface, and arithmetic processing capabilities sufficient to realize the given specifications. The 80C31 is a ROMless CMOS version of the industry standard Intel 8051[20].

5.3 Microcontroller Architecture

An architectural block diagram of the Intel 80C31 microcontroller is provided in Fig. 5.1. A comprehensive description of the architecture and operation of the 80C31 can be found in the Microcontroller Handbook[21]. The following is a discussion of key features important to the design of the data acquisition unit (DAU).

Memory Organization

Certain versions of the 8051 family include on-chip program memory (ROM or EPROM). For the purpose of building a prototype system, an 80C31, which has

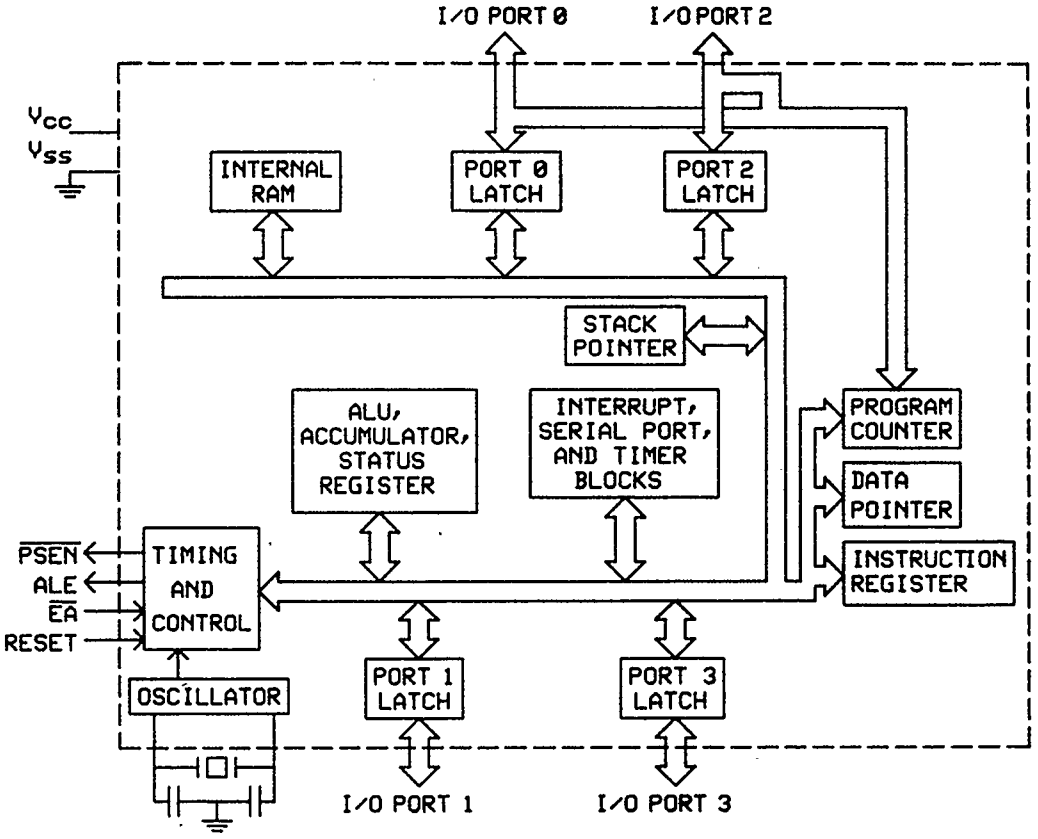


Figure 5.1 - Intel 80C31 Simplified Block Diagram.

no internal program memory, is used. If the DAU were to be mass produced, the logical alternative to the 80C31 is the 80C51 which includes 4 kbytes of internal read only memory (ROM).

The 80C31 can directly access up to 64 kbytes of external program memory plus 64 kbytes of external data memory. The DAU was designed with the intention of downloading program software to external RAM. Considering this, the external memory is organized such that the same physical memory can be used for both data storage and program storage purposes.

In addition to external RAM accessability, the 80C31 has 128 bytes of internal RAM. This RAM is divided into 32 registers, 16 bytes of bit addressable memory, and 80 bytes of scratch pad memory. The DAU utilizes this memory for various purposes including temporary storage of computational results, a program stack, and ADC control.

The 80C31 also has a number of special function registers (SFR) which contain information regarding various functions of the microcontroller. Some of these SFR's are discussed in the following sections.

I/O Structure

The 80C31 includes four bidirectional, 8-bit I/O ports. These ports consist of a latch and I/O circuitry. Each port can be configured as a general purpose I/O port. Alternatively, three of the I/O ports can be configured to implement specific

functions.

For the DAU, Port 0 is configured as a time multiplexed address/data bus for access to external memory. Port 2 is used to provide the high order address byte for external memory access. This allows the microcontroller to directly access 64 kbytes of external memory. The configuration of Ports 0 and 2 is similar to the time multiplexed bus of 8 and 16-bit microprocessor architectures.

Port 3 provides external access to several of the microcontroller's internal functions including serial communications, interrupts, and timer/counters. Two of the Port 3 pins also provide control for external memory access. A list of Port 3 pins and functions is included in Table 5.1. It is not necessary to use these pins as given in Table 5.1. For example, the timer/counter input pins, T0 and T1, can be used as external timer/counter inputs. However, for the DAU, Timer 0 is used to realize a real time clock, and Timer 1 is used to generate baud rates. The clock mechanism for both of the timers is obtained from the internal oscillator and thus the external timer inputs are not used. This leaves these inputs available for other purposes as desired by the application.

Port 1 provides an additional 8 I/O pins which can be configured as inputs, outputs, or both. For the DAU, four of these pins were used to operate the SPWM ADC.

Table 5.1 - Alternate Functions of 80C31 Port 3 Pins

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (Timer/Counter 0 input)
P3.5	T1 (Timer/Counter 1 input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Table 5.2 summarizes the usage of all four ports with respect to the DAU. Note that six of the I/O pins have been left unused. This allows for the possibility of further expansion.

Timer / Counters

The 80C31 has two 16-bit timer/counter registers : Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters. In the "timer" function, the register is incremented every machine cycle, that is, it is operated by the internal oscillator. In the "counter" function, external inputs (T0 and T1) are used to increment the register.

The timers are controlled individually via the special function register TMOD. Each timer can be programmed into one of four operating modes. These operating modes, and in particular their application to the DAU, are described briefly below.

In Mode 0, the timer register is configured as a 13-bit register. When the count rolls over from all 1s to all 0s it sets a timer interrupt flag. Mode 1 is identical to Mode 0, except that the register is extended to 16 bits. Mode 1 is used in the DAU to realize a real time clock for time measurement purposes.

In Mode 2, the timer is configured as an 8-bit counter with an automatic reload value as specified by the high order byte of the timer register (T_{hi}). When the count overflows, the timer interrupt flag is set and the contents of T_{hi} are

Table 5.2 - DAU Utilization of 80C31 I/O Ports

Port Pin(s)	Name & Function
P0.0 - P0.7	AD0 - AD7 (Multiplexed Address/Data Bus)
P2.0 - P2.7	A8 - A15 (High Byte of Address Bus)
P1.0	Trigger (Initiate ADC Conversion)
P1.1	Count_Out (ADC counter overflow)
P1.2	CHEN (ADC amplifier external clock enable)
P1.3	f_{CH} (external ADC amplifier auto-zeroing clock)
P1.4 - P1.7	NOT USED
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4 - P3.5	NOT USED
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

loaded into the counter. This mode is used in the DAU to generate baud rates for serial communications.

In Mode 3, the operation of Timers 0 and 1 is different. Timer 1 will hold its count when switched into Mode 3. Effectively, the counter is disabled. Timer 0 in Mode 3 establishes the timer register as two separate 8-bit counters. This allows the 80C31 to appear as if it has three separate counters. Mode 3 is not used in the DAU.

Serial Interface

The 80C31 serial port is full duplex, meaning it can transmit and receive data simultaneously. It is also receive buffered, that is, reception of a second byte can begin before a previously received byte has been read from the receive register. Control of the serial port is achieved via the SFR register SCON. The serial port has four operating modes described briefly below.

In Mode 0, the serial port operates as an 8-bit shift register. Modes 2 and 3 establish the serial port as a 9-bit UART, the only difference being that in Mode 3 the baud rate is controlled by Timer 1, whereas in Mode 2, the baud rate is fixed.

In Mode 1, the serial port operates as an 8-bit UART, with the baud rate controlled by the Timer 1 overflow. This mode of operation is used in the DAU.

The 80C31 also has a special provision for multiprocessor communications. This is accomplished via an additional control bit which enables or disables the

serial port interrupt, depending on the state of the final received bit of a data transmission. Thus, a single microcontroller unit could serve as one of several slave processors controlled by a master processor.

Interrupts

The 80C31 provides 5 interrupt sources as illustrated in Fig. 5.2. Each interrupt can be individually enabled or disabled. In addition, the user can specify priority levels for the interrupts. Each interrupt and its application to the DAU is described briefly below.

The external interrupts, $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$, can be selected as either level-activated or transition activated, depending on the respective control bits in the SFR register TCON. These two interrupts are used in the DAU to (1) detect the end of a PWM period during an A/D conversion ($\overline{\text{INT0}}$), and (2) detect the end of an A/D conversion ($\overline{\text{INT1}}$).

The Timer 0 and Timer 1 interrupts are generated by overflows of the respective counters. Since Timer 1 is used for baud rate purposes, its' interrupt flag is disabled. The Timer 0 interrupt routine is used to update the real time clock.

The serial interrupt flags, RI and TI, are used to detect either the reception of a complete data byte (RI) or the end of the transmission of a data byte (TI). These interrupts are used to control serial communications between the DAU and a host computer.

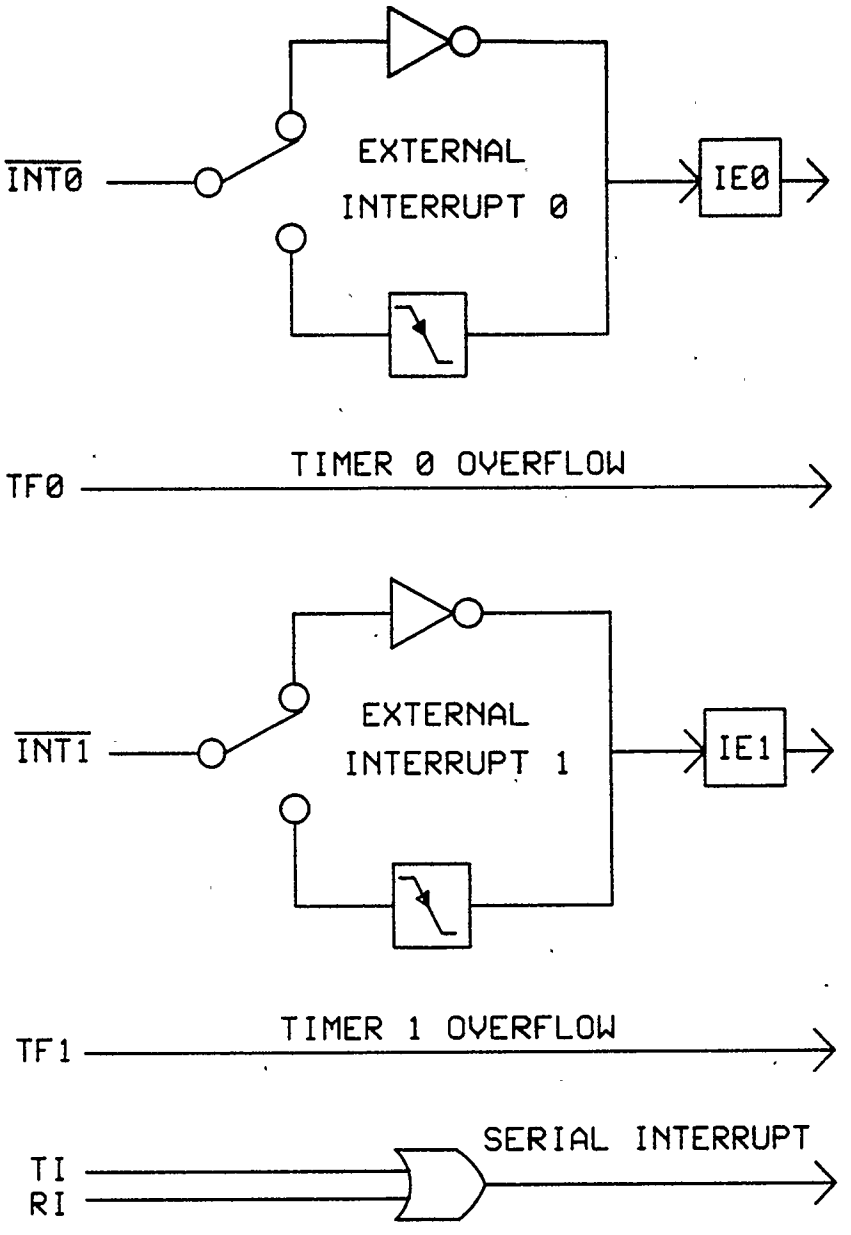


Figure 5.2 - 80C31 Interrupt Sources.

Power Saving Modes of Operation

The 80C31 provides two modes of low power operation in which the majority of the microcontroller circuitry is disabled. This is useful in applications where continuous operation is either not necessary or not desirable due to power limitations.

Using software control the microcontroller can be placed in an IDLE mode. In this mode, all circuitry is disabled except for the interrupt, timer, and serial port functions. Termination of the IDLE mode is accomplished by either the activation of an enabled interrupt or by a hardware reset. The power supply current in the IDLE mode is approximately 30% of the supply current under normal operation.

The other low power mode of operation is called POWER DOWN. In this mode, the on-chip oscillator is stopped, stopping all functions. Data in internal RAM and the internal registers is held. The power supply can also be reduced to 2 volts. POWER DOWN is initiated by software and terminated by a hardware reset. In the POWER DOWN mode of operation, the power consumption is approximately 1% of the normal operating power consumption.

5.4 DAU Architecture

A functional block diagram of the DAU is provided in Fig. 5.3. Since the 80C31 includes numerous integrated functions, a minimal amount of support

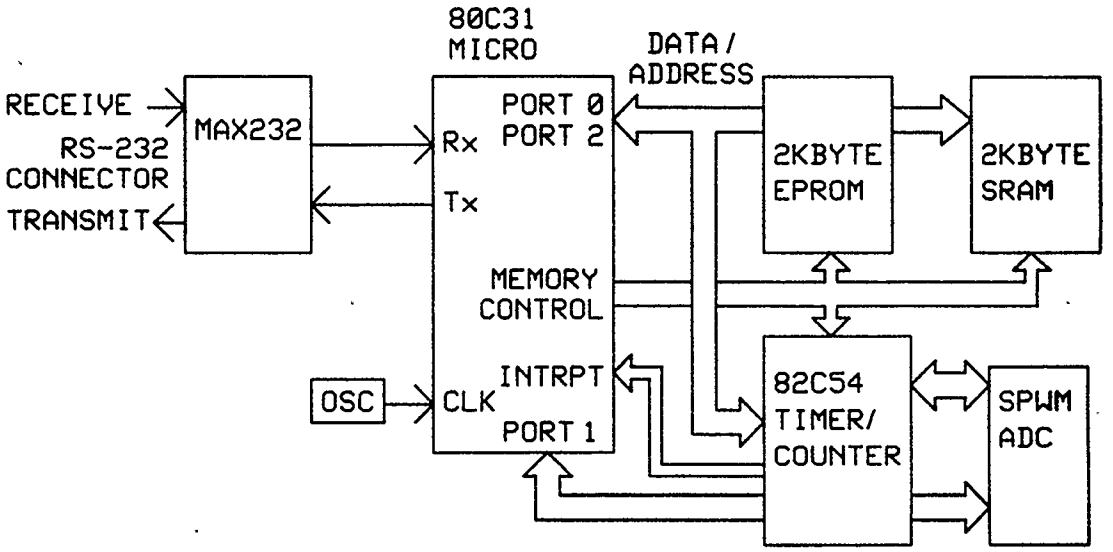


Figure 5.3 - DAU Block Diagram.

circuitry is required to realize a complete DAU. These additional functional blocks are described below.

Serial Line Interface

The RS-232 communications interface requires line drivers capable of shifting TTL/CMOS (0 to +5 volt) levels to RS-232 levels (-9 to +9 volts). The Maxim "MAX232" accomplishes this without the additional requirement of ±9 volt power supplies. In addition, the MAX232 provides both receive and transmit functions. This allows the serial interface to be implemented in a single chip[22].

Programmable Timer/Counter

The synchronized PWM ADC requires counters to (1) generate the PWM reset square wave, (2) count the number of PWM periods, $m\,T_o$, to complete a conversion, and (3) count the time, $N\,T_c$, that the PWM output is high. Considering these requirements, an Intel 82C54 Programmable Interval Timer is incorporated into the DAU. The 82C54 has three independent 16-bit counters as illustrated in Fig. 5.4. Each counter can be programmed into one of six timer modes allowing the 82C54 to be used as an event counter, real time clock, rate generator, and digital one-shot as well as several other applications[23].

For the purpose of the DAU, two modes of operation are of interest. These are (1) square wave mode and (2) hardware retriggerable one shot. In the square

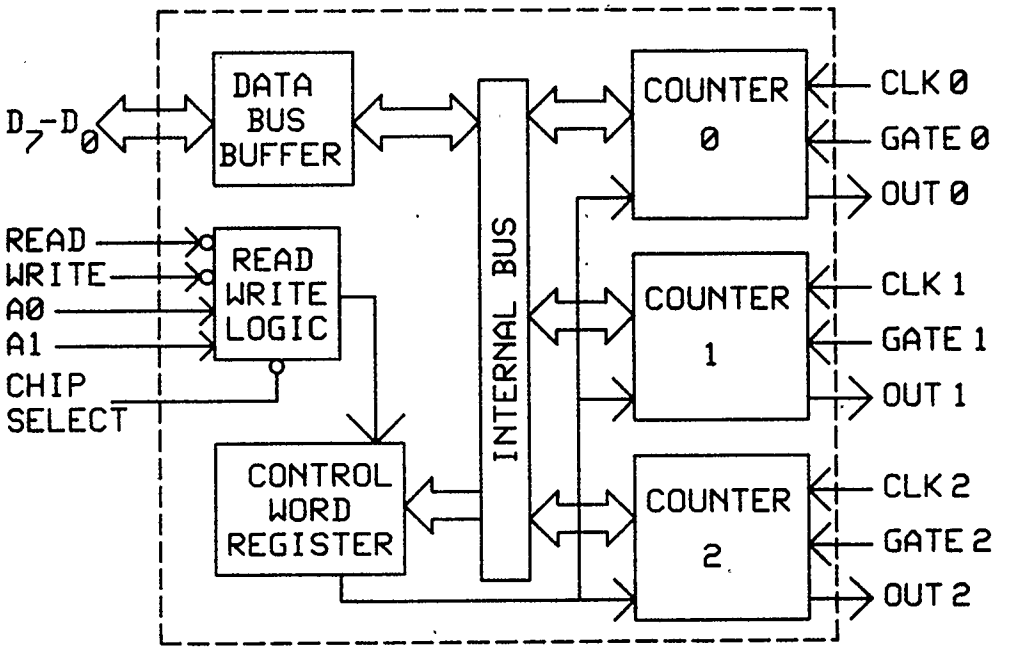


Figure 5.4 - Functional Block Diagram of 82C54 Timer/Counter.

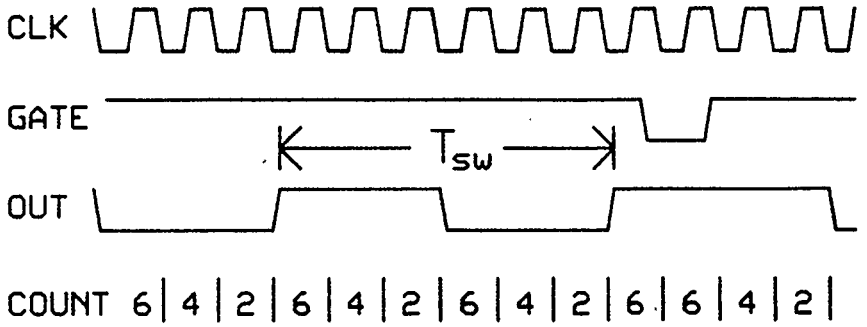
wave mode, the counter counts down two counts per clock cycle. Each time the count reaches zero, the initial count, n, is reloaded into the counter and the output is toggled. This mode is illustrated in Fig. 5.5(a). The period of the square wave, T_{SW}, can be shown to be,

$$T_{SW} = n\, T_{CLK}, \tag{5.1}$$

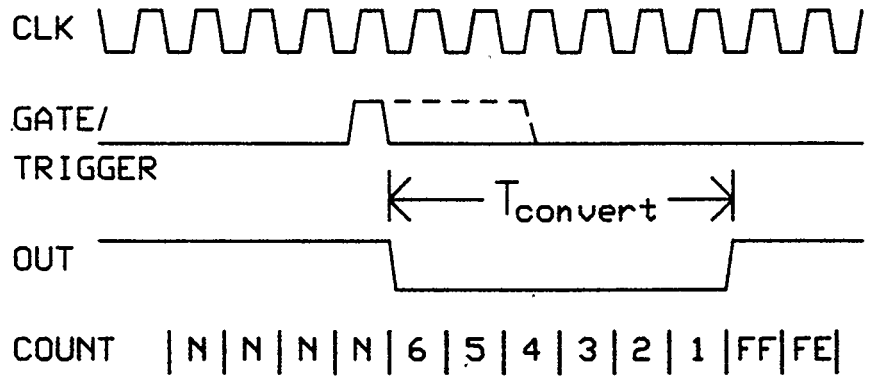
where T_{CLK} is the period of the input clock waveform. The square wave mode of operation is used in the DAU to generate the PWM input waveform V_R and also to measure the time $N\, T_c$ that the synchronized PWM output is high.

The hardware retriggerable one-shot mode is illustrated in Fig. 5.5(b). In this mode, the output is initially high. The output goes low on the first clock pulse following the trigger to begin the one-shot pulse. The output will remain low until the counter reaches zero. The GATE input of the counter serves as the trigger input. The time that the output is low is determined by the input clock period, T_{CLK}, and the initial count m.

The hardware one-shot mode is used in the DAU to produce a conversion time, $T_{convert}$, for the ADC. The microcontroller generates the trigger signal and the PWM square wave input is used as the clock input. The conversion time will then be a fixed number of PWM periods and is selected by programming the count m so that,



(a)



(b)

Figure 5.5 - 82C54 Programmable Timer Modes; (a) Square wave mode (n = 6); (b) Hardware one shot mode (m = 6).

$$T_{convert} = m\, T_o, \tag{5.2}$$

where T_o is the PWM operating frequency. It follows from eqn. 5.1 that the conversion time will be

$$T_{convert} = m\, n\, T_{CLK}. \tag{5.3}$$

The full scale resolution of the converter in this case will be one part in $m \times n$.

In summary, the 82C54 serves three purposes in the DAU. First, one counter is used to generate the synchronized PWM input square wave. A second counter, configured in a hardware one-shot mode, is used to fix the ADC conversion time. Finally, the third counter is used to measure the ADC output count, N.

Synchronized PWM ADC

The synchronized PWM ADC is implemented as shown in Fig. 5.6. Five signals are generated by the microcontroller (CHEN, f_{CH}, V_c) and the 82C54 timer (V_R, $V_{convert}$), and two are returned by the ADC (V_{count}, $\overline{V_{convert}}$). Signal descriptions for the ADC interface are provided in Table 5.3.

The SPWM is constructed on a separate printed circuit card and utilizes a separate 10 volt power supply. The SPWM is interfaced to the digital circuitry via two TTL/CMOS level shifters. The level shifters also provide power supply isolation between analog and digital circuitry.

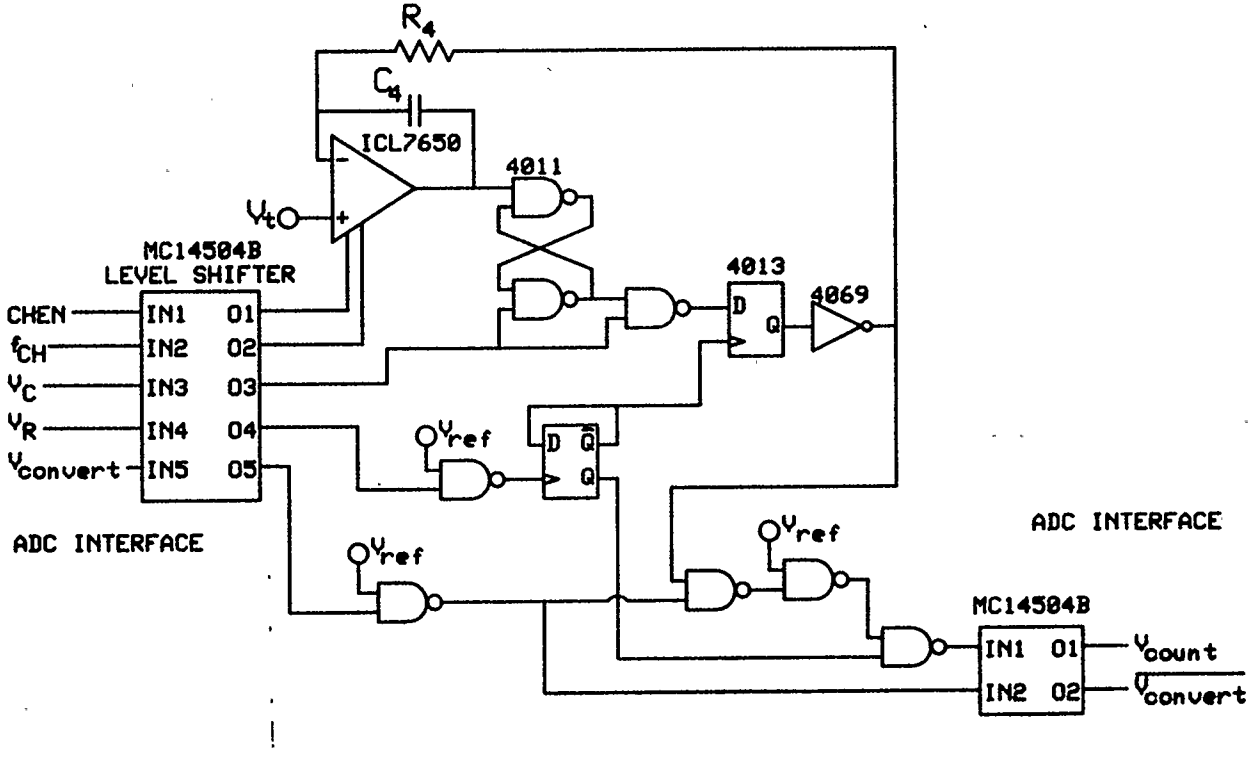


Figure 5.6 - Synchronized PWM ADC and DAU Interface.

Table 5.3 - DAU/ADC Interface Signal Descriptions

Signal Name	Description
ADC Inputs	
CHEN	ADC Operational amplifier external chopper enable
f_{CH}	ADC Operational amplifier external chopper input
V_C	SPWM high frequency clock
V_R	SPWM input square wave
$V_{convert}$	ADC Conversion active signal
ADC Outputs	
V_{count}	ADC output count clock
$\overline{V}_{convert}$	Inverted conversion active signal

5.5 DAU Calibration Example

A valuable function of the digital circuitry in the DAU is to provide calibration and error correction of analog circuitry. The synchronized PWM is subject to several sources of error as discussed in chapter 3. By quantifying these errors, it is possible to compensate digitally to reduce the errors to a negligible value.

In addition to the error sources considered in chapter 3, the SPWM is subject to additional errors due to thermal drift. Temperature changes will affect the amplifier dc offset voltage and input currents, as well as the on resistance of the PWM logic gates.

Theoretical estimation of the thermal drift of the SPWM is beyond the scope of this thesis. However, it is a useful exercise to measure the thermal drift error and use the measurements to provide error correction to the SPWM ADC under different operating temperatures. Then, in a field application, an additional temperature transducer could be incorporated into the DAU. Temperature measurements made by the transducer would then be used to estimate the SPWM ADC error due to thermal drift.

Results of temperature measurements for the SPWM ADC are presented in Fig. 5.7. Inspection of the results indicates that the thermal drift is non-linear and small. The maximum measured thermal drift error is approximately 0.4 ppm/$^{\circ}C$.

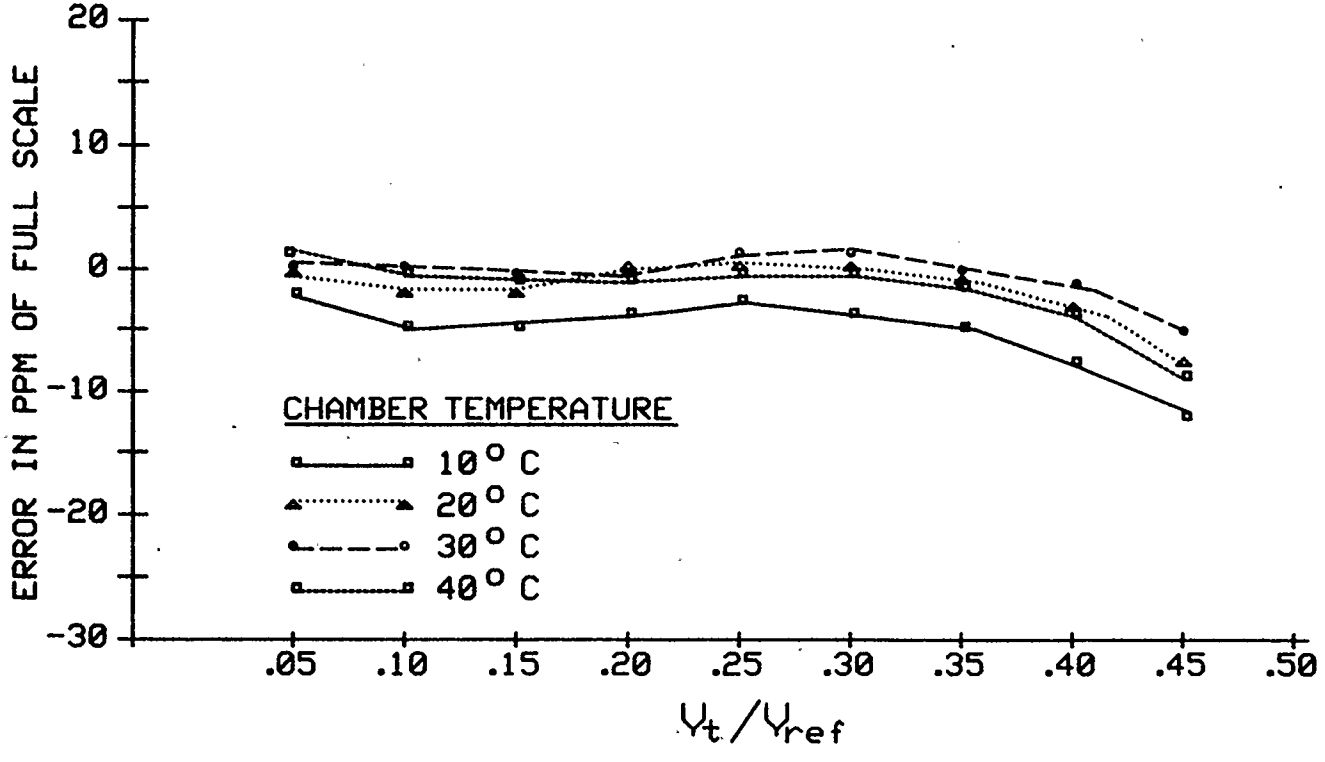


Figure 5.7 - SPWM ADC error for different temperatures.

Since the thermal drift error is non-linear, it is unsatisfactory to simply scale ADC results by a factor determined by a temperature measurement. A more effective approach is to use the ADC reading and a temperature measurement to select an entry from a look-up table maintained in the DAU memory (RAM or ROM). The entry in the look-up table corresponds to the estimated ADC error. For example, the measured ADC error for an input $\frac{V_t}{V_{ref}} = 0.05$ at a temperature of $10°C$ is -2 ppm. Thus, for a reading of $N = 50{,}000$ (assuming $m \times n = 10^6$), and a temperature of $10°C$, the corresponding entry in the DAU look-up table would indicate an error of -2 ppm. The value of N would then be adjusted to produce a more accurate representation of $\frac{V_t}{V_{ref}}$.

The size of the memory look-up table depends on the desired ADC accuracy. Noting that the maximum measured thermal drift is $0.4\ ppm/°C$, the resolution of temperature required to achieve 20 bit accuracy (1 ppm) is $2°C$. That is, if the temperature is determined to within $2°C$, the maximum error after thermal compensation will be 0.8 ppm.

Examination of the results of Fig. 5.7 indicates that a minimum resolution for $\frac{V_t}{V_{ref}}$ of 0.01 would enable the ADC error to be estimated within 1 ppm. Thus, the look-up table would require

$$M = 100\frac{(T_{\max} - T_{min})}{2^{\circ}C} \tag{5.4}$$

entries, where $T_{\max}$ and $T_{\min}$ are the maximum and minimum temperatures of interest. As an example, a look-up table containing 3500 entries would provide 20 bit linearity over the temperature range $0-70\,^{\circ}C$.

5.6 Summary and Recommendations

The development of a microcontroller based data acquisition unit (DAU) incorporating the synchronized PWM ADC has been considered. The performance and functional capabilities of the DAU satisfy the given specifications and the error correction capabilities of the DAU have been demonstrated by considering thermal drift errors of the SPWM ADC.

After comprehensive testing of the DAU and examination of current trends in microcontroller products, it is worthwhile to compile a list of suggestions which would upgrade the quality of the DAU. These suggestions are presented below.

(1) Although the voltage level shifters and separated analog and digital power supplies provide some power supply isolation, oscilloscope and voltage measurements indicated that a significant amount of digital noise was coupled into the analog circuitry. This noise was reduced by additional decoupling and regulation of the analog supply. An alternative solution which would provide complete isolation

between analog and digital circuitry is optical coupling of common signals. Optoisolators are a common feature in integrated ADC's and they eliminate the problems caused by common analog and digital grounds[24].

(2) The Intel 80C31 has the functional capabilities to satisfy the specifications for a high resolution data acquisition unit with the exception of the additional counters required to implement the SPWM ADC. These counters are provided by the Intel 82C54 programmable interval timer. There are, however, several available microcontrollers that provide the functional capabilities of the 80C31 plus additional counters which would eliminate the need for the 82C54 timer. In particular, the National Semiconductor Corp. HPC16040 microcontroller contains 8 16-bit timers. In addition, the HPC16040 is a full 16-bit microcontroller with 52 general purpose I/O lines (as compared to 32 for the 80C31), is available in extended temperature range tolerances, and is fabricated in a low power CMOS process[25]. The drawbacks of the HPC16040 (higher cost and lack of available development resources to the author) were reasons why it was not used in the original development of the DAU.

(3) The 8051 series of microcontrollers is the industry standard. In consideration of this, Intel has made a version of the 80C51 (the 80C31 is a ROMless version of the 80C51) its first available standard cell for use in development of application specific integrated circuits (ASIC)[26]. Using an ASIC approach would allow the

DAU described in this chapter to be integrated into a single package (with the exception of the analog circuitry), providing an extremely compact acquisition system.

(4) In a separate development, Dallas Semiconductor Corp. has produced a version of the 80C51, called the DS5000, which incorporates a 32k x 8 static RAM and a lithium battery into a single 40-pin microcontroller package[27]. This allows the microcontroller program memory to be reprogrammed automatically and remotely via the serial communications channel. The lithium battery maintains the static RAM and also provides protection against power lossage. The incorporation of RAM and battery backup into a single package also results in a space savings, a desirable feature for applications requiring compact systems.

All of the above suggestions would be worthwhile to pursue if the DAU were to be produced on a large scale. The flexibility of the microcontroller architecture allows for expansion or modifications at a minimal cost. Applications of the DAU are extensive, varying from oilfield measurements to industrial monitoring of equipment. The flexibility of the DAU described here allows both applications to be realized without major redesign.

CHAPTER 6

Conclusions and Suggestions for Further Research

In this thesis, the design and implementation of a precision analog-to-digital converter (ADC) circuit has been presented. The circuit uses the principles of pulse width modulation and charge balancing to convert an analog input voltage into a rectangular wave with a duty cycle proportional to the input voltage.

The pulse width modulator (PWM) can be implemented so that the output duty cycle is 'instantaneously' proportional to the input voltage. This analog PWM is useful in analog applications such as analog multiplication and can also be modified to provide gain and linearization. Measurements on an analog multiplier circuit showed that an overall accuracy of 0.01% was achievable with minimal concern for circuit non-idealities.

By synchronizing the PWM output with a high frequency clock, it is possible to implement a high resolution ADC with an overall linearity of 4 ppm. Detailed analysis of the SPWM ADC indicated that digital correction could be applied to the converter to achieve an accuracy of 1 ppm corresponding to 20 bits of

accuracy.

The resolution limitations of the SPWM were theoretically examined and experimentally measured. It was found that the resolution was limited by operational amplifier noise. Measurements showed that the SPWM ADC was capable of resolving voltages on the order of 50 nanovolts, demonstrating the circuit's usefulness in low signal level applications.

The SPWM was interfaced to a microcontroller-based digital system to realize a precision data acquisition unit (DAU). The DAU is a compact, low power system useful in several applications. The DAU was capable of communicating with a remote computer, and was used to digitally calibrate the SPWM ADC.

Temperature sensitivity of the SPWM was briefly considered and it was found that the SPWM had a thermal drift of approximately 0.4ppm/°C. However, since the SPWM is useful in field applications such as oilfield pressure and temperature measurements, a detailed study of the temperature performance of the SPWM ADC would be valuable.

The data acquisition unit constructed was a flexible, compact system. However, a greater savings in space could be achieved by integration of the DAU into two IC's (one analog and one digital).

Integration of the SPWM requires careful consideration of the effects of circuit non-idealities on the performance of the SPWM ADC, as discussed in chapter

3. In particular, the SPWM requires an operational amplifier with a very low dc offset, very low amplifier input currents, and low amplifier noise. Some of the methods used to achieve these characteristics have been discussed in this thesis.

Integration of the digital circuitry could be accomplished using a standard cell or semi-custom approach. As discussed, the microcontroller presented in this thesis (Intel 80C31) is available through Intel as a standard cell. The functional capabilities of the 80C31 are such that a minimal amount of support circuitry is needed to realize a complete DAU. In consideration of this, the development of an integrated DAU using a standard cell approach would be straight forward and cost effective.

REFERENCES

[1] G. Grandbois and T. Pickerell, "Quantized Feedback Takes Its Place in Analog-to-Digital Conversion", *Electronics*, Oct. 13, 1977, pp. 103-107.

[2] C.O. Li, "High Precision Voltage-to-Frequency Converters", M.Sc. Thesis, University of Calgary, Calgary, August 1987.

[3] R.J. Higgins, *Electronics with Digital and Analog Integrated Circuits,* Prentice Hall, Inc., Englewood Cliffs, N.J., 1983.

[4] M. Riezmann, "High-Resolution Arrives for ADC Chips and Hybrids", *Electronics*, Jan. 7, 1988, pp.133-138.

[5] Intersil Inc., *Data Book*, California, 1981.

[6] W. Wilson, H. Massoud, E. Swanson, R. George and R. Fair, "Measurement and Modelling of Charge Feedthrough in n-Channel MOS Analog Switches", *IEEE Journal of Solid-State Circuits,* vol. SC-20, pp.1206-1213, Dec. 1985.

[7] *Instruction Manual for VDR-106/7 Primary Standard Voltage Divider,* Julie Research Laboratories, New York.

[8] *Analog Product Data Book,* Harris Corporation, 1986.

[9] Bernard Loriferne, *Analog-Digital and Digital-Analog Conversion,* Heyden and Son Ltd, London, England, 1982.

[10] P. Garret, *Analog I/O Design*, Reston Publishing Company, Inc., 1981.

[11] O.A. Onwuachi, "Noise in Operational Amplifier Circuits", M.Sc. Thesis, 1985.

REFERENCES (Continued)

[12] P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits,* John Wiley and Sons, New York, 1984.

[13] A. Van der Ziel, *Noise in Measurements*, John Wiley and Sons, New York, 1976.

[14] R.K. Wong, "An Integrated Voltage-to-Frequency Converter", M.Sc. Thesis, University of Calgary, Calgary, April 1987.

[15] B. Widrow and S. Stearns, *Adaptive Signal Processing,* Prentice-Hall Inc., Toronto, 1985.

[16] Hewlett-Packard, *HP-5423A Structural Dynamic Analyzer-Introduction to Operation,* vol. 1, California, 1979.

[17] Bendat and Piersol, *Measurement and Analysis of Random Data,* John Wiley and Sons, Inc., New York, 1966.

[18] "Award for Instrument System", Oil Week, Sept. 11, 1978, p. 29.

[19] S. Liebson, *The Handbook of Microcomputer Interfacing,* TAB Books, Inc., 1983.

[20] J. Bond, "8-bit Microcontrollers Specialize for Embedded Control Applications", *Computer Design*, Nov. 15, 1987, pp. 26-32.

[21] *Microcontroller Handbook*, Intel Corporation, 1986.

[22] *MAX232 Data Sheet*, Maxim, California, 1987.

[23] *Digital Product Data Book*, Harris Corporation, 1988.

REFERENCES (Continued)

[24] R.A. Pease and L. Distaso, "V-f Converter and Microcontroller Produce High-Resolution ADC", *Electronic Design*, Sept. 13, 1980, pp.103-107.

[25] *HPC* 16040 *Data Sheet*, National Semiconductor Corporation, California, 1986.

[26] "Intel Picks Up Steam After a Faltering Start", *Electronics*, Aug. 6, 1987, pp. 66-68.

[27] B.C. Cole, "Designer's Dream Machine", *Electronics*, March 5, 1987, pp. 53-57.

APPENDIX

MEASUREMENT SYSTEM

The PWM circuits described in this thesis are capable of making high resolution and high accuracy measurements. In order to determine the limits of accuracy and resolution it is necessary to perform experimental measurements using a system of comparable or better accuracy and resolution. This appendix describes the measurement systems used in this thesis. In addition, the manner in which results were obtained is also discussed.

A.1 Synchronized PWM Accuracy Measurements

The SPWM accuracy measurements were done using the experimental configuration shown in Fig. A.1. This diagram also shows the physical arrangement of power connections. Thus, the power supply voltages (V_{ref} and ground) were connected first to the voltage divider and then to the SPWM circuitry. The

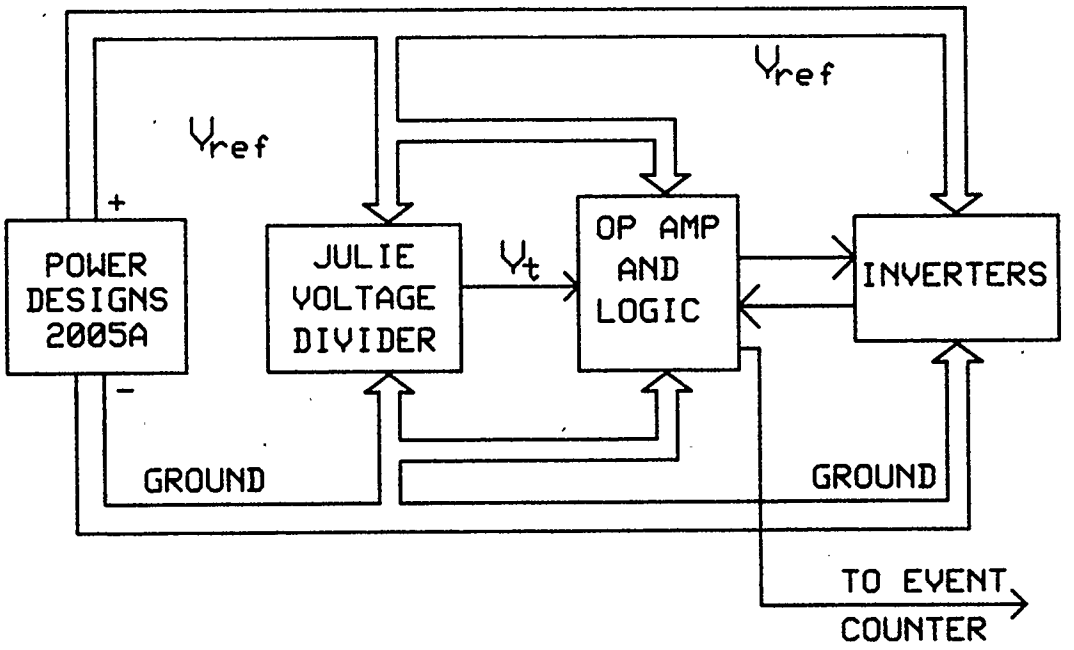


Figure A.1 - Experimental Setup for SPWM Accuracy Measurements.

printed circuit board containing the SPWM was laid out so that the power and ground traces leading to the output inverters of the SPWM were separate from the power and ground traces for the remainder of the circuitry. This minimized the voltage differences between the voltage divider inputs and the SPWM output high and low values. Wires connected between the divider and the SPWM were made as short and thick as possible in order to further reduce these differences.

The Julie voltage divider[7] specifications state that the ratio of the divider output V_{out} to the divider input voltage reference (V_{ref}) is accurate to within 0.1 ppm of V_{ref}. Since this accuracy is a factor of 10 better than that achievable by the SPWM, it is reasonable to assume that SPWM measurement errors due to the voltage divider are negligible.

The results of measurements of the SPWM accuracy are presented in chapter 3. These results were obtained by averaging the data of a large number of measurements. Typically, these measurements were taken over the course of several days, in an attempt to ensure the repeatability of the results. The graphs shown in chapter 3 indicate the error in parts per million of full scale (10 volts). Thus, an error of 1 ppm corresponds to a voltage error of 10 μV.

A.2 Synchronized PWM Resolution Measurements

The SPWM resolution measurements were done using the experimental configuration shown in Fig. A.2. The measurement system includes a voltage regulator to minimize power supply noise and in particular to reduce 60 Hz AC ripple. The SPWM input was included on the SPWM circuit board by connecting two low temperature coefficient precision resistors in a voltage divider configuration. These resistors were chosen to provide the SPWM with an input voltage of approximately 36 mV. The SPWM circuit included a gain of 100, giving the circuit a full scale input of 100 mV.

The printed circuit board was laid out in attempt to minimize voltage drops in power and ground traces. Power leads were wrapped in a twisted pair configuration to provide additional power supply decoupling. Finally, the SPWM and voltage regulator were encased in a shielded box to reduce external noise.

The SPWM output counts were stored using the DAU described in chapter 5. The DAU then transmitted the results to a microcomputer, where statistical analysis was done.

The results of measurements of the SPWM resolution are presented in chapter 4. These results were obtained as follows:

(1) Once a circuit configuration was chosen (this included selection of passive

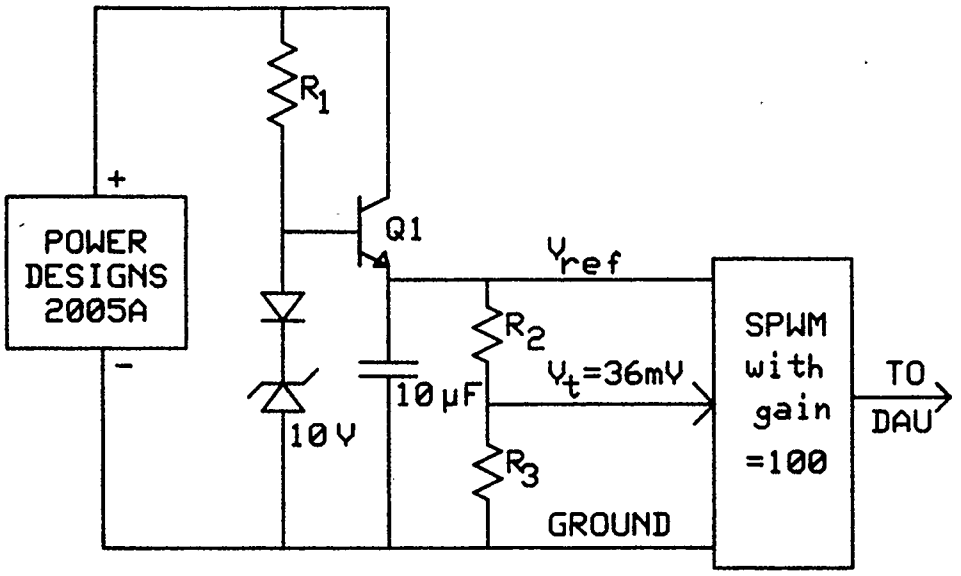


Figure A.2 - Experimental Setup for SPWM Resolution Measurements.

component values, the auto-zeroing clock frequency, and the conversion time), the SPWM was set up to do continuous conversions with a delay of approximately two seconds between conversions.

(2) The result of each conversion was transmitted to the host microcomputer. Upon the completion of approximately 250 conversions, the results were stored in a data file.

(3) The data file was then statistically analyzed to determine the mean value and the standard deviation of the data.

(4) The resolution was determined in ppm by the following relationship:

$$\text{Resolution(ppm)} = 10^6 \frac{\sigma_x}{\mu_x} \tag{A.1}$$

where σ_x and μ_x correspond to the standard deviation and mean value of the data. Thus, the graphs shown in chapter 4 indicate the resolution in parts per million of the input voltage (36 mV). The resolvability in voltage terms is determined by multiplying the resolution in ppm by the ratio of the input voltage (36 mV) to the mean value of the SPWM output count. That is,

$$\text{Resolution(volts)} = \text{Resolution(ppm)} \left[\frac{V_t}{\mu_x} \right] \tag{A.2}$$

Thus, for example, a resolution of 2 ppm, assuming an SPWM output count of 10^6 and an input voltage of 36 mV, corresponds to a resolvability of 72 nV.

The results presented in chapter 4 are typical measurements rather than averages of several data files. The resolution for a given circuit configuration was measured several times (usually on different days). The presented results include the results of only one data file for each circuit configuration. Additional data was recorded to determine the reliability of the results.