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A Broadband Variable-Gain Amplifier and a Broadband Self-Calibrated High-Sensitivity Power Detector for the Square Kilometre Array

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A Broadband Variable-Gain Amplifier and a Broadband Self-Calibrated High-Sensitivity Power Detector for the Square Kilometre Array

by

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A THESIS

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Abstract

The Square Kilometre Array (SKA) is an international project to design and construct the next generation ultra-sensitive radio telescope. Depending on the final configuration, the SKA will require millions of receivers ideally fabricated in a low cost semiconductor process. This thesis presents a study of using CMOS technologies, which are the most common and less expensive semiconductor option, to implement a variable gain amplifier (VGA) with a linear-in-dB performance and an RMS power detector (PD) for a mid-frequency SKA receiver.

Two linear-in-dB VGAs were designed and experimentally verified in this work. The first VGA meets most of the SKA specifications except bandwidth and linear-in-dB range. The second VGA uses a bandwidth extension technique and a low threshold voltage transistor to achieve a maximum tunable gain range of 34 dB and the linear-in-dB range of 28.5 dB within $\pm$1 dB error, an upper 3 dB cutoff frequency of 2.1 GHz and a power consumption of 1.1mW. Both S11 and S22 are less than -10 dB from 100 MHz up to 4.2 GHz. This VGA achieved the lowest power consumption among comparable VGAs published to date.

A differential broadband self-calibrated RMS PD using the MOSFET square-law characteristics was proposed and experimentally verified in this work. After automatically compensating mismatches between all circuit components by adjusting input transistor bulk voltage, the proposed PD circuit showed the highest sensitivity and lowest power consumption of all PDs published prior to this work. The PD operates over an input power range from -48 dBm to -11 dBm with output voltage offset less than 0.95 dB for the SKA mid-frequency range with an input-referred P_{1dB} of -11 dBm, 3 dB bandwidth of 1.8 GHz and power consumption of only 1.2 mW. This PD meets all requirements of the mid-frequency SKA receiver. This power detector was embedded within the receiver and fabricated in a TSMC 65nm CMOS process. Measurement results showed an input power range from -40 dBm to -20 dBm with power consumption of 1.5 mW.

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For Jie, my lovely boys Yibo and Kinsey, and my parents

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Glossary

Acronom	Definition
ADS	Advanced Design Systems
AC	Alterating current
HEMT	High Electron Mobility Transistor
PVT	Process, Voltage and Temperature
SSFoM	Survey speed figure of merit
BSIM	Berkeley Short-Channel IGFET Model
PGA	Programmable gain amplifier
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct current
DUT	Device under test
GaAs	Gallium Arsenide
HEMT	High Electron Mobility Transistor
InP	Indium Phosphide
IP3	Third order intercept point
IIP3	Input referred IP3
OIP3dB	Output referred IP3
P1dB	1 dB compression point
IP1dB	Input referred P1dB
OP1dB	Output referred P1dB
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
LNA	Low noise amplifier
NF	Noise figure
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
ADC	Analog-to-digital converter
VGA	Variable gain amplifier
PD	Power detector
RFIC	Radio Frequency Integrated Circuit
SKA	Square Kilometre Array
VLA	Very Large Array
VNA	Vector network analyzer

Chapter 1

Introduction

For the past decades, astronomers have put more and more efforts to further their understanding of key important phenomena in the Universe, including some pertaining to the birth and death of the Universe itself [1]. With the current radio telescopes, which have provided astronomers with invaluable information, it became apparent that some basic scientific questions still could not be answered [2]. Radio astronomers are recognizing that when all other known methods to increase sensitivity have been employed, the only way left to continue the historical trend of advances in radio telescope sensitivity, shown in Fig. 1.1, is by increasing the telescope collecting area [3].

Driven by sensitivity requirements, the Square Kilometre Array (SKA), which is the world's next generation ultra-sensitive radio telescope, is to provide much higher sensitivity than current radio telescopes. The international community of physicists and astronomers

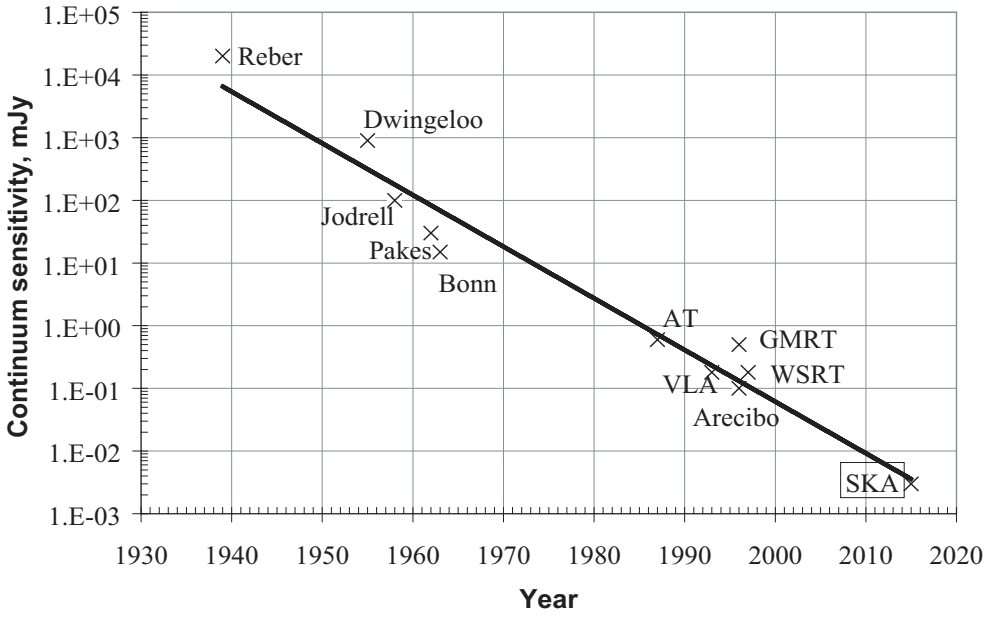


Figure 1.1: Sensitivity of radio telescopes for 60 s of integration time, where1 $Jy = 10^{-26} W/(Hz \cdot m^2)$. The new radio telescope discussed in this work is the Square Kilometre Array (SKA) telescope. Adopted from [3].

has identified a set of Key Science Programs (KSPs) to address fundamental issues in modern astronomy, physics, and astrobiology [2, 4]. The six major KSPs, which will realize significant return from the SKA project, are as follows [4, 5]:

- Probing the Dark Ages and the Epoch of Reionization.
- Strong Field Tests of Gravity Using Pulsars and Black Holes.
- Galaxy Evolution, Cosmology, and Dark Energy.
- The Origin and Evolution of Cosmic Magnetism.
- The Cradle of Life.

1.1 Square Kilometre Array

According to the requirements of the KSPs, the frequency range of the SKA must cover from 70 MHz to 30 GHz [1, 2, 6, 7]. The SKA will be realized using three different receptor types and configurations [5, 8]:

- A low-frequency Array ("SKA-low"): It covers frequency range from 70 - 450 MHz and is realized using a dipole array that provides wide-field imaging capabilities for three-dimensional mapping of the cosmic web. SKA-low is mainly used to address observations for 21 cm hyperfine line of neutral hydrogen from the Epoch of reionization and earlier with high redshift. It is also suitable to observe low radio frequency of pulsars, magnetized plasma both in the Galaxy and intergalactic space, radio recombination lines, and potentially extrasolar planets.
- A mid-frequency Array ("SKA-mid"): It covers frequency range from 0.35 - 13.8 GHz and is devided into 5 bands, which cover frequency range from 0.35-1.05GHz, 0.95-1.76GHz, 1.65-3.05GHz, 2.80-5.18GHz and 4.6-13.8GHz, respectively. SKA-mid is based on a large-N array of dish reflectors outfitted with single-pixel feed receivers,

possibly enhanced by field-of-view expansion systems, such as phased-array feeds, to increase survey speed. SKA-mid will observe radio pulsars and observations of the 21-cm hyperfine line of neutral hydrogen from the local Universe, to moderate redshifts. It will performe high sensitivity observations of continuum emitting objects. It will also be suitable for conducting various spectral lines, in addition to the 21-cm hydrogen line, many classes of radio transients, magnetized plasmas both in the Galaxy and intergalactic space, and potentially proto-planetary disks.

- A high-frequency Array ("SKA-high"): It covers frequency range from $0.7 \sim 30\,\mathrm{GHz}$, is based on a dish array.

The current design plans for the SKA antennas is to have antennas densely distributed in the central region of the telescope and then extended to the outside region sparsely in groups along five spiral arms. The space between these groups will be wider gradually from the center [8]. An artist's concept of the telescope footprint is shown in Fig. 1.2. Two locations that have been chosen are the Australian Outback with mainly a low-frequency apperture array and mid-frequency array of dishes equipped with Phased-Array Feed (PAFs) and South Africa with a mid-frequency array of parabolic reflectors (dishes) and high-frequency dishes array [1, 5].

1.1.1 Sensitivity

The SKA sensitivity, which is defined as A_e/T_{sys} , where A_e is the effective area of all antennas and T_{sys} is the system noise temperature at the terminals of each antenna [1, 2], should be at least $10^4\,m^2/K$ to meet the science objectives. It is two orders of magnitude larger compared with the sensitivity of the Expanded Very Large Array (EVLA) of $\sim 270\,m^2/K$ [1, 2]. The weakest signal that the SKA telescope will detect in a specified observing time is proportional to T_{sys}/A_e.

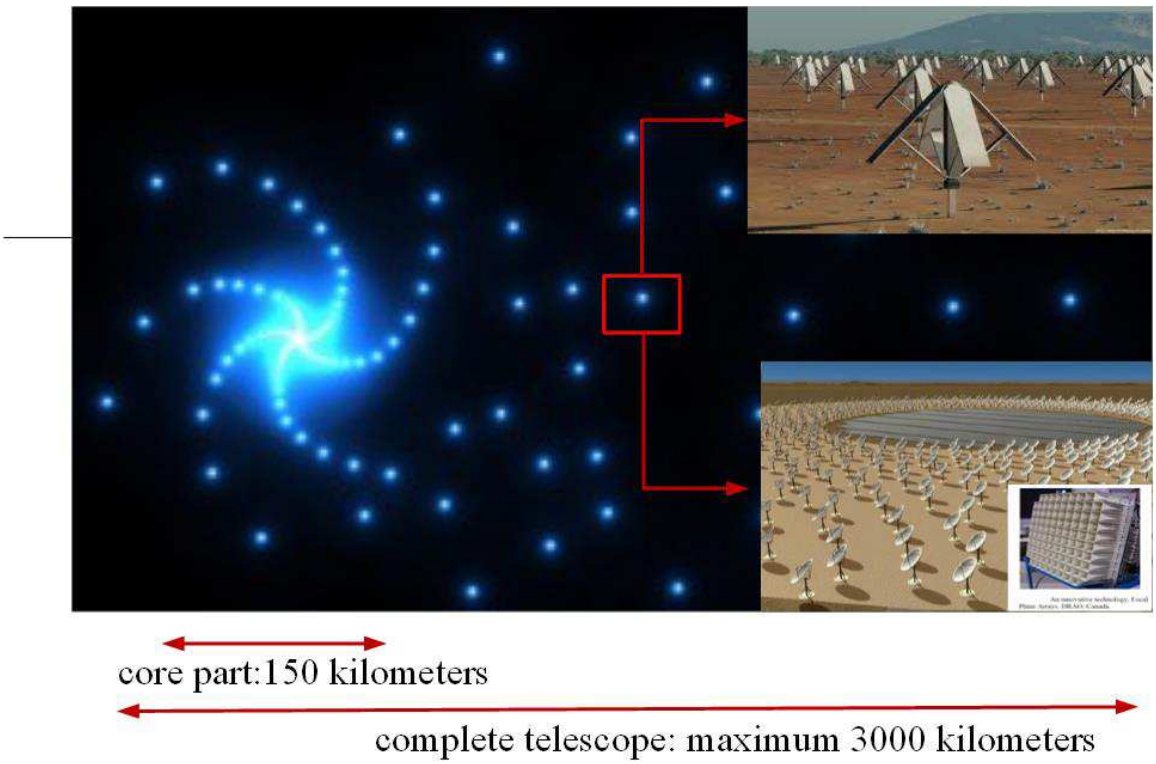


Figure 1.2: Footprint of SKA telescope configuration. Maximum space between two antenna is 3000 kilometres. @ 2014 skatelescope.org

1.1.2 Survey speed

SKA survey speed figure-of-merit (SSFoM) is defined as the rate at which an area of sky much larger than the telescope field of view (FoV) can be surveyed for sources stronger than the specified limit [1], and is proportional to the ratio of Ω to the time required to detect a point-source of specified strength $(A_e/T_{sys})^2\,\Omega$, where Ω is the solid angle of the antenna over which the sensitivity of the antenna is greater than 0.5 of the maximum sensitivity [1, 2]. For the SKA this must be at least $3\times10^9\,deg^2m^4K^{-2}$ at wavelengths longer than 20 cm [1, 2]. As can be seen, both the sensitivity and survey speed are proportional to A_e/T_{sys} and $(A_e/T_{sys})^2$, respectively. Decreasing the noise components in the system, especially in the first-stage low-noise amplifier (LNA) connected to each antenna element, improves sensitivity and survey speed.

1.1.3 System noise temperature

A system noise temperature less than 40 K is the key objective for the SKA telescope [1, 9], of which 10 K is estimated for the antenna and receiver input interconnection losses, 15 K is for the receiver chain and the remainder is allocated for sky noise, spillover and noise-coupling/mismatch [1, 9].

Traditionally, to achieve the required noise performance, LNAs needed to be cooled [1]. However in the SKA, the receivers are spread over a very large area, and cooling is seen as very expensive and complex. At ambient temperatures in a frequency range from 700 MHz to 1.4 GHz, it is possible to design LNAs with a noise figure as low as 0.2 dB, i.e. noise temperature of 14 K [10]. Therefore, the development of ambient-temperature LNAs with very low noise temperature is the most likely solution for the SKA low-frequency and mid-requency receivers. When frequency is lower than 300 MHz, the sky noise will dominate the system noise and ambient-temperature LNA designs are less challenging to be suitable for the SKA [1].

1.2 SKA receiver

Historically, a radio telescope only had a few receivers, which were implemented with exotic GaAs or InP cryogenically cooled HEMT transistors [4]. In the SKA project, since the focal-plane arrays and aperture arrays require millions of receivers, the significant cost associated with the large number of receivers impacts the choice for low-cost and ultra-low-noise fabrication technologies with low DC power consumption. Based on one of the estimates, power consumption of 0.1 W/receiver will add € 1M/year to the operating cost of the SKA [11]. Complementary Metal-Oxide-Semiconductor (CMOS) technologies are the least expensive semiconductor option per transistor for manufacturing integrated circuits due to their large integration capabilities. Over the past few years, CMOS technologies have become very competitive to more exotic GaAs technologies and are considered as en-

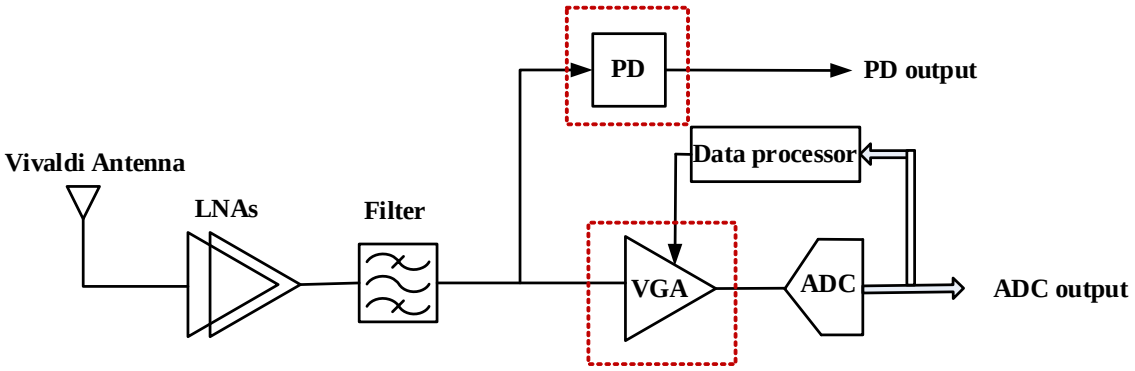


Figure 1.3: Conceptual SKA receiver topology.

abling technologies for the SKA not only because of their large volume manufacturing and high levels of integration but also because of their improved RF performance. Our research group is working on a fully integrated CMOS receiver to meet the 0.7 GHz to 1.4 GHz frequency range for SKA phased-array requirements, with goal extending this work further to conform with the SKA aperture array requirements. The conceptual direct-sampling SKA receiver architecture proposed by our research group is shown in Fig. 1.3, where the dashed rectangles label the work described in this thesis. Weak incoming signals, dominated by the background noise and the receiver thermal noise, are collected by telescope Vivaldi antenna elements, amplified by the LNA and gain stages, identified as LNAs in Fig. 1.3 [10, 12], filtered by a bandpass filter, and fed into a variable gain amplifier (VGA) [13, 14] before entering the analog-to-digital converter (ADC) [15]. In this receiver architecture, the power detector (PD) is used to measure the total received power before the VGA in order to preserve this information, required for some astronomical observations.

There is a large number of receivers to be used in the SKA. Process, voltage and temperature (PVT) variations will cause receiver gain deviate from what is expected, thus affecting the amount of power delivered to an ADC. To process the signal that may vary significantly in amplitude, a high performance ADC with a large dynamic range and high-speed, which is very expensive and hard to design, is needed. As an alternative, an automatic gain-control circuit (AGC) circuit is normally employed [13, 16, 17] in a receiver to tune receiver gain due to PVT variations and provide the optimum signal level for the ADC. This relaxes the

Table 1.1: Relevant SKA receiver specifications

Description	Specification
Frequency range	0.7 GHz~1.4 GHz (Hydrogen with redshift of zero to unity, SKA-mid band1 and band2)
Noise temperature	< 40 K
Power consumption	<350 mW
Gain	>70 dB
OP1dB 1dB gain compression output power	>-8 dBm (ADC limited)
IP1dB 1dB gain compression input power	>-80 dBm (Input power limited)

ADC requirements. To complete the closed-loop form of a conventional AGC, the VGA control signal is generated at the SKA control center by analyzing the ADC output during the telescope calibration cycle.

The LNA, which is the first stage of the receiver, needs to consume sufficient power to provide very low system noise temperature and high gain to guarantee that the telescope achieves the required sensitivity and survey speed. The power consumption of the LNA cannot be reduced significantly without affecting the telescope performance. The reduction in the VGA and PD power consumption is an important consideration. As the semiconductor fabrication processes keep changing with time, to keep the research work useful in future projects, the designs discussed in this work should be scalable to new CMOS processes with only minimum transistor resizing while keeping the same circuit topologies. The main SKA receiver requirements are summarized in Table 1.1.

1.2.1 LNA and gain stages

The LNA and the gain stages have been designed by other group members. The LNA lowest noise figure can reach to 0.2 dB and the gain stages have gain of 70 dB in the 700 MHz-1.4 GHz range [10, 12].

Table 1.2: VGA performance specifications

Description	Specification
Process	CMOS
Power supply	1.2 V Max
Frequency range (GHz)	0.7 -1.4
Gain range (dB)	-10 - +10
Linear-in-dB	Yes
Linear-in-dB error	$\pm$1dB (max)
Power consumption (mW)	$\leq$5
Inputs/Outputs	Differential/Differential

1.2.2 Variable-gain amplifier

The VGA discussed in this work was designed for SKA receivers, and will be used to precisely adjust the overall receiver gain to compensate for changes in input power levels and PVT variations. In the SKA receivers, linear-in-dB performance is desirable as it makes AGC settling time independent of receiver input signal power [2, 18, 19]. To achieve this behavior, an active circuit with exponential behavior is required. To the authors knowledge all measured -3 dB bandwidths of broadband, low-power (<5 mW) and linear-in-dB VGAs published to date are all less than 1 GHz [20–23], which are unusable for SKA receivers due to upper frequency gain roll-off. In this work, a low-power linear-in-dB VGA with broad bandwidth was researched to meet the SKA mid-frequency application requirements. The VGA specifications are summarized in Table. 1.2.

1.2.3 Power detector

The PD discussed in this work was designed to measure the total received power before the VGA in order to preserve this information required to further analyze the astronomical phenomena. The input signal of the SKA receiver is mainly a noise-dominated signal with very low power level (-95 dBm). As the LNA and gain stages before the PD already have 70 dB of gain and increasing this gain is difficult while maintaining circuit stability, a high sensitivity PD is needed. There are a number of PD publications to date [24–28]. But, due

Table 1.3: PD performance specifications

Description	Specification
Process	CMOS
Power supply	1.2 V Max
Operating frequency (GHz)	0.7-1.4
Detection range (dB)	25
Sensitivity (dBm)	<-35
Linearity error for specified input range	$\pm$1dB (max)
Power consumption (mW)	$\leq$5
Inputs/Outputs	Differential/Differential

to the power consumption, bandwidth or sensitivity, none of the circuits can meet the SKA PD requirements. This work discusses a design of a PD for direct use in an SKA receiver. The requirements of the PD are specified in Table 1.3.

1.2.4 Analog-to-digital converter

A 4-bit, 10 Giga Sample/Second ADC has already been designed by one of our group members [15].

1.3 Thesis layout

The rest of the thesis is divided into six Chapters.

In Chapter 2, broadband VGA topologies are reviewed and advantages and disadvantages of each circuit are discussed. After that, the linear-in-dB function realization methods and bandwidth extension techniques are discussed. Cascaded VGA chain bandwidth and gain optimization methods are described at the end of the Chapter.

Chapter 3 follows by presenting two linear-in-dB VGAs. The pseudo-exponential approximation function and the bandwidth extension techniques discussed in Chapter 2 are used in the VGAs to achieve linear-in-dB performance and broad bandwidth while having low power consumption. Simulation and measurement results of both VGA circuits are reported.

In Chapter 4, different power detection methods are reviewed and compared. Their advantages and limitations are also discussed. It is identified that power detection using MOSFET square-law characteristics is the most superior of all the detection methods. Three PD circuits using MOSFET square-law characteristics are discussed at the end of this Chapter showing the advantages of those circuits and limitations for using in the SKA receiver project.

Chapter 5 follows by proposing a differential, broadband PD circuit, which uses MOSFET square-law characteristics and has a self-calibrated function that compensates for component mismatch and allows the PD to achieve the highest sensitivity compared with all published PDs. The PD circuit and circuits used for calibration are described in this Chapter. The simulation and measurement results are shown at the end of the Chapter.

In Chapter 6, measurement results of the PD embedded into an SKA receiver are reported.

Chapter 7 summarizes the proposed work and emphasizes the future work.

1.4 Contributions

The work in this thesis resulted in the following publications:

Paper [13] discussed a low-power broadband AGC amplifier targeted for use in the SKA receiver. The AGC was composed of an input power-match circuit, a linear-in-dB output VGA, a PD, an error amplifier, a comparator and a loop filter. The input operating range of the AGC is from -50 dBm to -20 dBm. The total power consumption of the AGC is 1.5 mW. This AGC is not described in this thesis, because the SKA receiver VGA will be controlled from the SKA control center, and the SKA receiver will not require a fully integrated closed-loop AGC.

Paper [14] presented a CMOS inductorless broadband linear-in-dB VGA circuit for use in the SKA receiver and is covered in Section 3.2.

Paper [29] reported a CMOS broadband linear-in-dB VGA circuit with active inductor

loads to extend the -3 dB bandwidth of the VGA in [14]. This work is covered in Section 3.3.

Paper [30] proposed a self-calibrated 65 nm CMOS broadband self-calibrated high-sensitivity power detector for use in the SKA and is covered in Chapter 5.

The PD, which is embedded in the receiver, is discussed in Chapter 6 and has not been published yet but this work is in preparation for publication.

The VGA, which is embedded in the SKA receiver and was completed by the author and other group members, was discussed in Chapter 6 and a paper is in preparation to discuss this circuit.

Chapter 2

Broadband Linear-in-dB VGA techniques

This Chapter starts with the review of basic VGA topologies and different tuning techniques employed in a VGA design. Section 2.2 reviews linear-in-dB function realization methods. Bandwidth extension techniques are described in Section 2.3. Bandwidth and gain optimization of a cascaded VGA chain is analyzed in Section 2.4. Section 2.5 is the summary of discussions of the topics presented in this Chapter.

2.1 Variable gain amplifiers

Many VGA topologies that are based on different semiconductor processes (such as bipolar, BiCMOS, and CMOS) have been introduced over the years [20, 31–35]. CMOS VGAs are generally preferred due to their lower costs and ease of integration with other CMOS analog and digital system components. As this work also requires the VGA to be embedded in CMOS SKA receivers, only CMOS VGAs are discussed in this thesis.

Depending on its gain-control signal, a VGA is defined either as a digitally controlled VGA, which is normally called a programmable-gain amplifier (PGA), or an analog controlled VGA, which provides a continuous gain control. PGAs with fine programmable gain steps have been proven to be valuable solutions in terms of noise and linearity [31, 36, 37]. PGAs often use binary weighted resistors or capacitors for gain control [33, 38–40]. A high-precision PGA requires a large number of such resistors or capacitors, which are area consuming. Moreover, fast-switching digital signals can generate glitches when the VGA gain is adjusted [22]. However, analog-controlled VGAs avoid signal phase discontinuity and switching noise [20], and they also reduce the large number of control bits used in PGAs. Therefore, analog-controlled VGAs are mostly preferred in high-resolution applications and are adopted in this work. To the author's knowledge, all VGA gain-tuning approaches can be classified into one of three types:

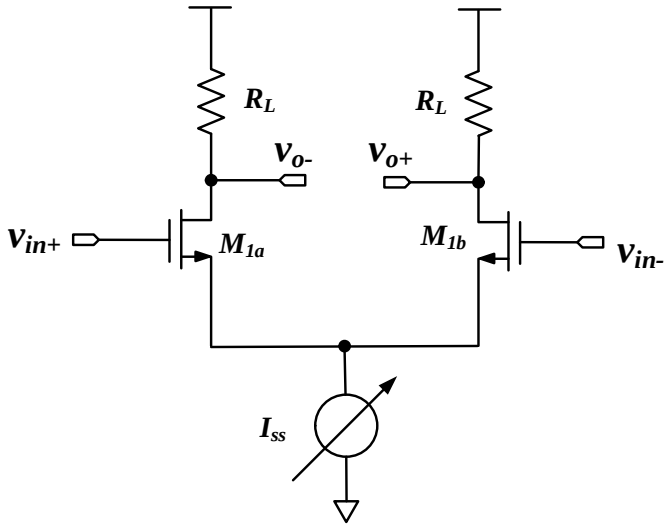


Figure 2.1: Transconductance-tuning common-source differential amplifier.

- Transconductance-tunable VGAs
- Load-tunable VGAs
- Feedback-coefficient-tunable VGAs

2.1.1 Tranconductance-tunable VGAs

The most straightforward way of tuning amplifier gain is by tuning the transconductance of the circuit that sets the gain of an amplifier [20, 32, 41, 42]. For a simple amplifier, the circuit transconductance is the input transistor's transconductance, which can be controlled by changing bias current. An example circuit is shown in Fig. 2.1 that is a common-source differential pair amplifier. The voltage gain of this amplifier is expressed by

$$A_v = g_{m1a,1b} \cdot R_L = \frac{2I_{ss}}{V_{GS} - V_t} R_L \tag{2.1}$$

where $g_{m1a,1b}$, V_{GS} and V_t are the transconductance, gate-source voltage, and threshold voltage of transistors M_{1a} and M_{1b}, respectively. The gain is varied by adjusting $g_{m1a,1b}$ through controlling DC current I_{ss}. This circuit is very simple and has gain-independent bandwidth. The disadvantage of the circuit is in its linearity, which is a measure of the

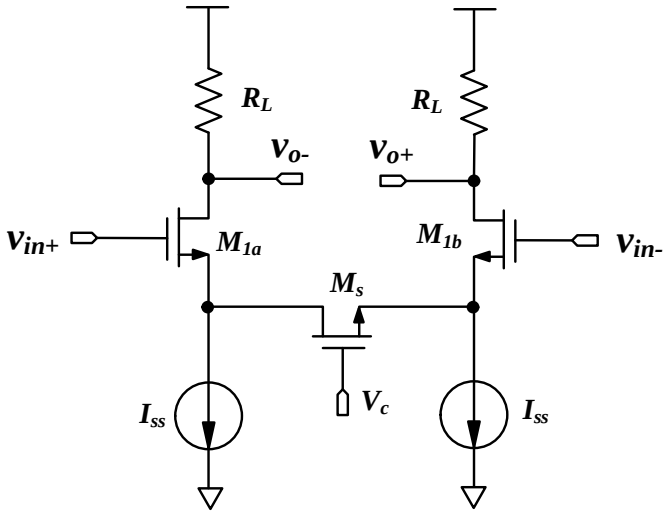


Figure 2.2: Transconductance-tuning common source differential amplifier with source-degeneration.

deviation of the gain from the ideal characteristic. Because of short channel effects of $M_{1a,1b}$, not captured in (2.1), the bias current I_{ss} non-linearly affects $g_{m1a,1b}$, which makes the gain linearity highly dependent on I_{ss}.

Generally, for complicated amplifier circuits the amplifier transconductance is not equal to the amplifier input transistor transconductance, and the amplifier gain is controlled by varying the amplifier equivalent transconductance. An example of an equivalent transconductance-tunable VGA circuit is shown in Fig. 2.2 , which is a common-source differential pair with source degeneration. The voltage gain of the VGA in Fig. 2.2 is A_{v1}:

$$A_{v1} = G_m \cdot R_L = \underbrace{\frac{-g_{m1a,1b}}{1+0.5g_{m1a,1b}R_s}}_{G_m} \cdot R_L \tag{2.2}$$

where G_m is the equivalent transconductance of the whole circuit, R_s is the channel resistance of MOS transistor M_s, which is biased in the triode region and acts as a variable resistor

$$R_s = \frac{1}{\mu_n C_{ox} (W/L)_{M_s} \left(V_c - V_{th,M_s} - V_{s,M_1}\right)}, \tag{2.3}$$

where μ_n, C_{ox} are the carrier mobility and the gate oxide capacitance per unit area of M_s, respectively, V_{th,M_s} is threshold voltage, $(W/L)_{M_s}$ is the ratio of the width to the length of M_s, V_c is the gate voltage of M_s, and V_{s,M_1} is the source voltage of M_1. The amplifier gain is adjusted by changing V_c, which changes R_s and thus changes G_m while $g_{m1a,1b}$ do not change with V_c. Comparing to the circuit in Fig. 2.1, this circuit linearity is limited by M_s rather than non-linear performance of $g_{m1a,1b}$ which depends on $I_{ss.}$ Linearity of M_s can be improved by using different threshold voltage transistors in parallel or the same threshold voltage transistors with different control voltage levels [21]. Also using low threshold voltages helps with improving the variable gain range and linearity, which is verified in Chapter 3. Fig. 2.2 has better linearity compared with Fig. 2.1 at a cost of losing voltage gain because of the source degeneration resistor.

Both circuits have gain-independent bandwidth, which is the important advantage of transconductance linearly tunable VGAs for broadband and large variable gain-range applications. In order to have a linear-in-dB function between the gain and the control signals, exponential-function conversion blocks are needed. These convert the input control signal to exponentially-scaled control signals I_{ss} or V_c.

2.1.2 Load-tunable VGAs

Another type of VGA is a load-tunable VGA. The most general load-tunable VGA is a current-steering VGA [35, 43, 44]. An example of such a circuit is shown in Fig. 2.3. In Fig. 2.3, differential cascode transistors M_{2a}, M_{2b}, M_{3a}, and M_{3b} steer currents from and to the loads R_{La} and R_{Lb}, which adjusts the amplifier gain [35]. The voltage gain of this circuit is

$$A_v = \frac{W_3 g_{m1a,1b} R_{La,Lb}}{W_2 (V_{cp} - V_s - V_{t,2})} \cdot (V_{dd} - V_{cn}) \tag{2.4}$$

when M_{2a}, M_{2b} and M_{3a}, M_{3b} are biased such that

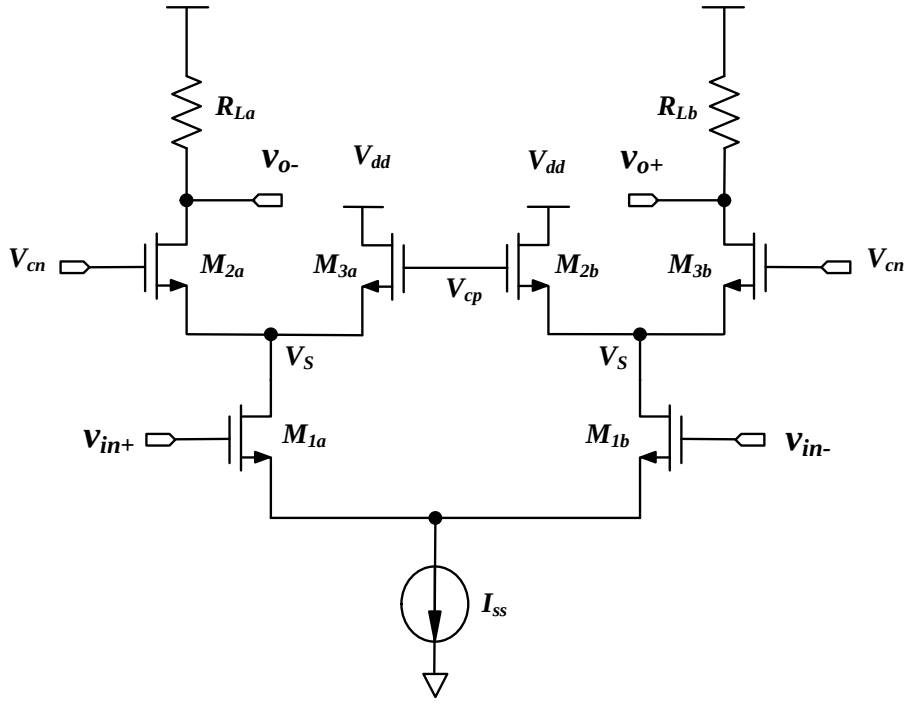


Figure 2.3: Current-steering load-tunable VGA. G_m control is obtained by varying V_{cn}.

$$\frac{W_3}{W_2} \cdot \frac{V_{dd} - V_s - V_{t,3}}{V_{cp} - V_s - V_{t,2}} = 1, \tag{2.5}$$

where W_2, W_3 and $V_{t,2}$, $V_{t,3}$ are channel widths and threshold voltages of M_{2a}, M_{2b} and M_{3a}, M_{3b}, respectively, V_{dd} and V_s are the power supply voltage and the source voltages of $M_{2a,2b}$, $M_{3a,3b}$. Equation (2.4) indicates a linear relationship between the voltage gain A_v and the control voltage V_{cn}.

The circuit shown in Fig. 2.4 can be thought of as a variant of Fig. 2.3, where the additional transistors M_{3a} and M_{3b} for steering current away from loads have been omitted. The VGA gain is controlled by changing the gate voltage of M_{2a} and M_{2b}. In this topology, if V_{cn} is set to make M_{2a} and M_{2b} operate as in the deep triode region, i.e. as a resistor, then this amplifier works as a conventional common-source amplifier. But as V_{cn} is tuned to the point at which M_{2a} and M_{2b} move into the saturation region, this amplifier becomes a cacode amplifier, which has increased output impedance and hence increased gain. This circuit has been reported in the literature and it is attractive for its simplicity [45].

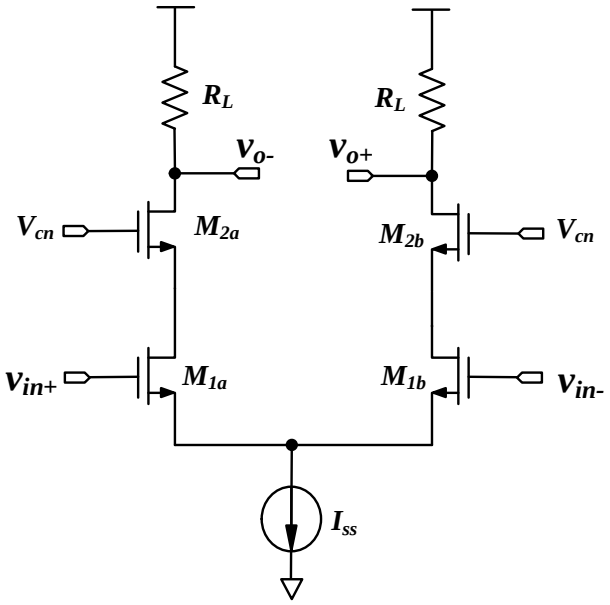


Figure 2.4: Cascode load-tunable VGA.

Based on the discussion, both topologies in Fig. 2.3 and Fig. 2.4 have a stack of three transistors and a load resistor. This relatively large stack-up of transistors can suffer headroom problems when used in a low-voltage environment. Meanwhile, these two VGAs have a gain-dependent bandwidth due to the gain-dependent load resistance, and thus are not suitable for broadband applications.

2.1.3 Feedback-tunable VGAs

The third type of VGA is an amplifier with a built-in tunable negative feedback [46]. A typical VGA circuit with variable feedback is a differential pair circuit as shown in Fig. 2.5. The gain of the circuit is

$$A_v \approx g_{m1a,1b} \cdot R_L + \frac{R_L}{R_F} \tag{2.6}$$

where $g_{m1a,1b}$ are transconducatnces of M_{1a} and M_{1b}. By varying the value of the feedback resistor R_F, the amplifier gain is linearly adjusted. The feedback resistor in this circuit provides bias voltage to M_{1a} and M_{1b}, and sets the output DC voltage.

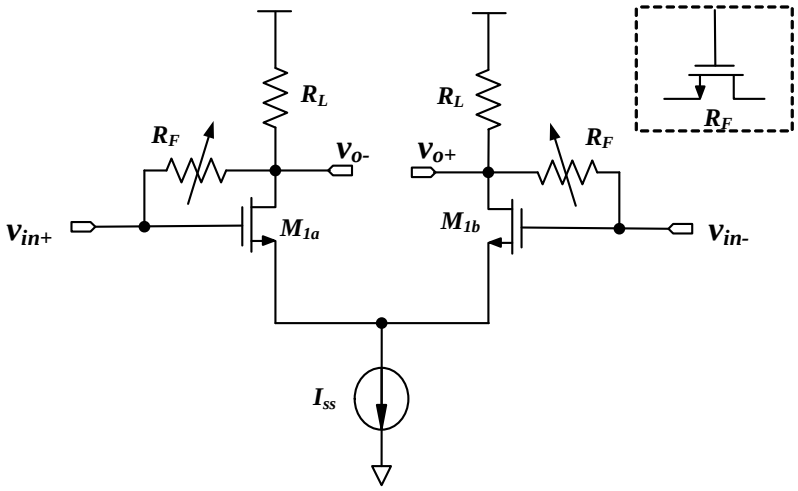


Figure 2.5: Negative-feedback differential VGA.

A variable resistor R_F can be implemented with a MOS transistor, and can be varied by altering the gate voltage of the MOS transistor working in the triode region. Then (2.6) can be rearranged as

$$A_v \approx g_{m1a,1b}R_L + \mu_n C_{ox}\left(V_{GS,R_F} - V_{t,R_F}\right)\left(\frac{W}{L}\right)_{R_F} \times R_L \tag{2.7}$$

where V_{GS,R_F} is the gate-to-source voltage and $(W/L)_{R_F}$ is the ratio of the width to the length of the transistor used to implement R_F. The gain A_v has a linear relationship with V_{GS,R_F}, which acts as the control voltage for the amplifier.

For this amplifier topology, the input impedance is low compared to that of VGAs discussed in Sections 2.1.1 and 2.1.2, and this may reduce the gain of the VGA driver stages [47]. Also this circuit may have potential stability problems and a limited variable range [47].

2.1.4 Summary

Based on discussion of the three types of VGAs, load-tunable VGAs have gain-dependent bandwidth, negative-feedback VGAs load preceding stages and thus limit their gain, and, therefore, transconductance-tunable VGAs are usually favored for broadband VGA designs

even though they suffer from low linearity and limited gain range. All circuits demonstrate a linear relationship between their gains and control voltages. In order to have a linear-in-dB relationship between the gains and control voltages, which means gains represented in the dB scale have a linear relationship with control signals represented on a linear scale, exponential function circuits are needed and discussed next.

2.2 Exponential function approaches

2.2.1 Exponential function using transistor intrinsic performance

There are many ways to realize an exponential function in CMOS technology. One way is to use a MOSFET biased in the subthreshold region where MOS transistors exhibit an exponential relationship between their drain I_D currents and gate-source voltages V_{GS} [48]:

$$I_D = I_0 e^{\left(\frac{V_{GS}}{\zeta V_T}\right)}, \tag{2.8}$$

where $\zeta > 1$ is a non-ideality factor, $V_T = kT/q$, k is Boltzmann's constant, T is the absolute temperature, I_0 is saturation current, and q is the magnitude of the electron charge. The subthreshold biasing, however, has drawbacks associated with high noise and low bandwidth [49].

Another possible method is to use parasitic bipolar transistors in standard CMOS processes to generate the desired exponential function. In this case, the exponential function is generated using the relationship between the collector current I_c and the base-emitter voltage V_{BE} as

$$I_c = \beta_{DC} I_R e^{\left(\frac{V_{BE}}{V_T}\right)}, \tag{2.9}$$

where β_{DC} is current gain, I_R is the saturation current. This relationship is strongly dependent on the temperature and fabrication processes. Therefore, various compensation techniques that guard against the temperature and process variations are required to have

an accurate signal power control mechanism. In addition, temperature compensation is needed to control the output level over a wide dynamic range [22]. The advantage of the bipolar transistors is the large variable gain range of more than 30dB, which is superior to what is possible with other methods [35].

However, while bipolar circuits naturally provide exponential behavior, in recent publications there has been a move to using elaborate MOSFET circuits that provide the required exponential or pseudo-exponential functions.

2.2.2 Pseudo-exponential function based on Taylor expansion

A popular pseudo-exponential function approximation, called pseudo-exponential function approximation-I, is based on Taylor series expansion of

$$e^{-2x} \approx \frac{1-x}{1+x} = y. \tag{2.10}$$

In (2.10), x is a variable and has a nearly exponential relationship with y for $x \ll 1$. The useful range for x is limited by the maximum deviation between y and e^{-2x}. This approximation can provide y with a linear-in-dB range of 17 dB with a maximum deviation of ±0.6 dB when x is set between -0.45 to 0.45 as shown in Fig. 2.6 [32]. The advantages of this approximation are in its simple function form and ease of realization with a real circuit, while the tunable range is a limitation for high-dynamic-range applications. The dynamic-range limitation can be solved by using multiple cascaded stages.

To improve the gain-control range of an individual stage, another pseudo-exponential approximation, called pseudo-exponential function approximation-II, also based on Taylor expansion was proposed by [50]

$$e^{2ax} = \frac{\mathrm{e}^{ax}}{e^{-ax}} \cong \frac{\left[k+(1+ax)^2\right]}{\left[k+(1-ax)^2\right]} = y, \tag{2.11}$$

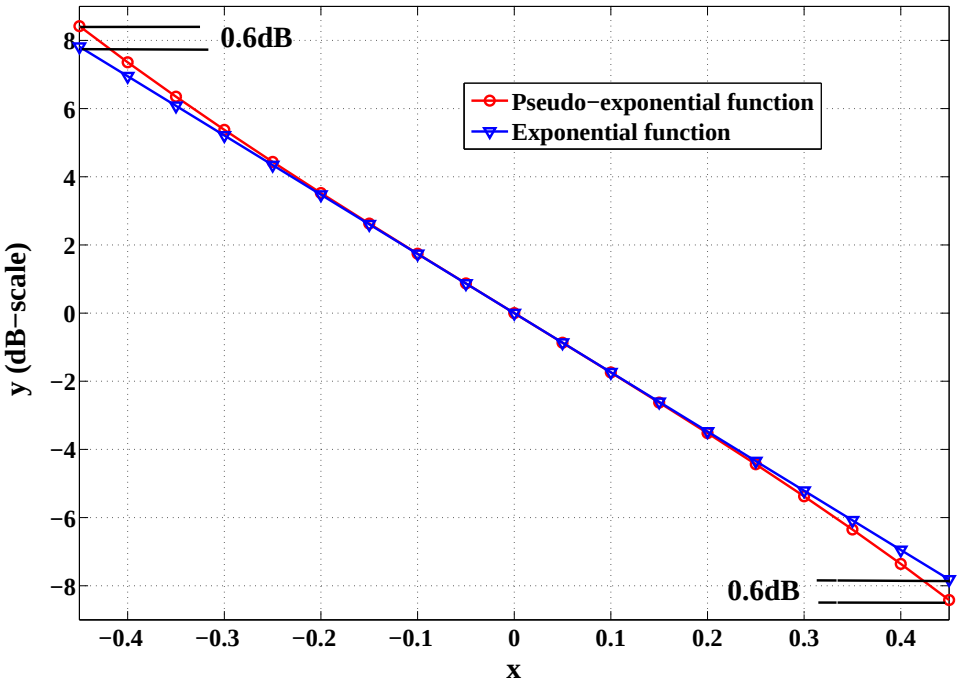


Figure 2.6: Linear-in-dB range of Pseudo-exponential function approximation-I.

and has also been used in [20]. where a and k are constants and x is the independent control variable. For $k = 1$, the numerator and the denominator of (2.11) are the second-order Taylor series approximations of the exponential function. For k less than 1, the linear-in-dB range of (2.11) can be extended dramatically as shown in Fig. (2.7) by the line with cross markers ($k = 0.25$) and the line with square markers $(k = 0.15)$. As shown in Fig. 2.7, for $k = 0.15$, the linear-in-dB range can be extended to more than 60 dB with a maximum deviation of ±0.5 dB, which has a dramatic improvement compared with pseudo-exponential function-I, $(1+ax)/(1-ax)$, and second-order Taylor series approximation $\frac{1}{2}\left[1+(1+ax)^2\right]$. Moreover, the input range of x is also wider than with the second-order Taylor series approximations. The limitation is that there are two parameters, a and k, defined by circuit parameters, which are hard to balance in real circuit designs.

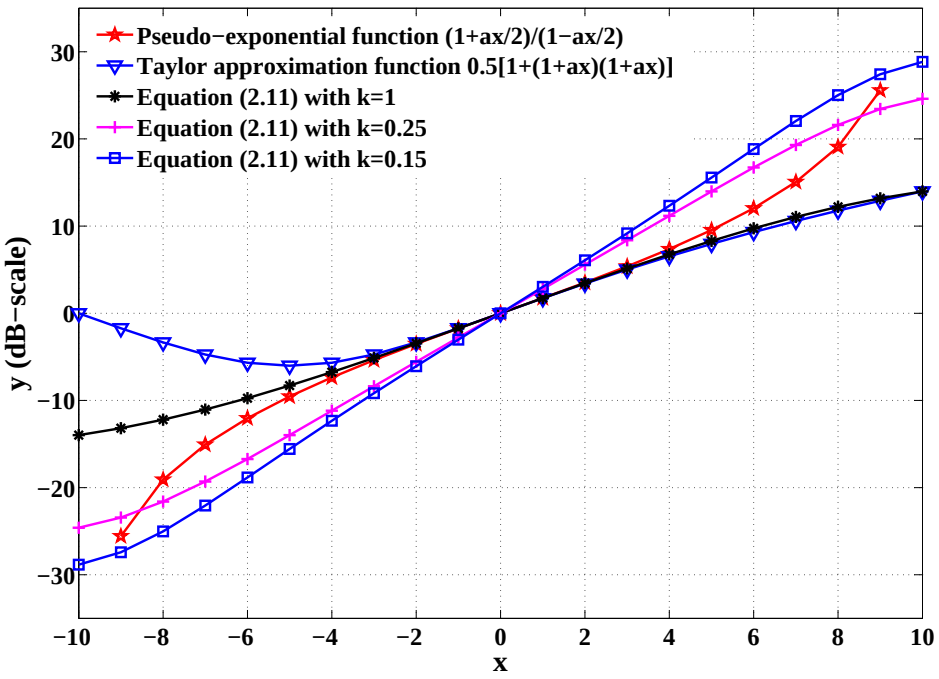


Figure 2.7: Pseudo-exponential function approximation-II as function of different parameters.

2.2.3 Exponential-function realization based on a linear function

Another exponential approximation was proposed for a linear-in-dB VGA in [21]. The exponential function is described as:

$$e^x = \lim_{n\to\infty}\left(1+\frac{x}{n}\right)^n \tag{2.12}$$

where x in an independent variable and n is an integer. As n increases and x decreases, the approximation error decreases rapidly and becomes negligible. The expression for this approximation consists of linear equations and can be easily implemented as a circuit.

The exponential approximation can be reduced to

$$e^x \approx \left(1+\frac{x}{n}\right)^n \tag{2.13}$$

for $x \approx 0$. Applying (2.13) in a VGA design, e^x and the independent variable x can be

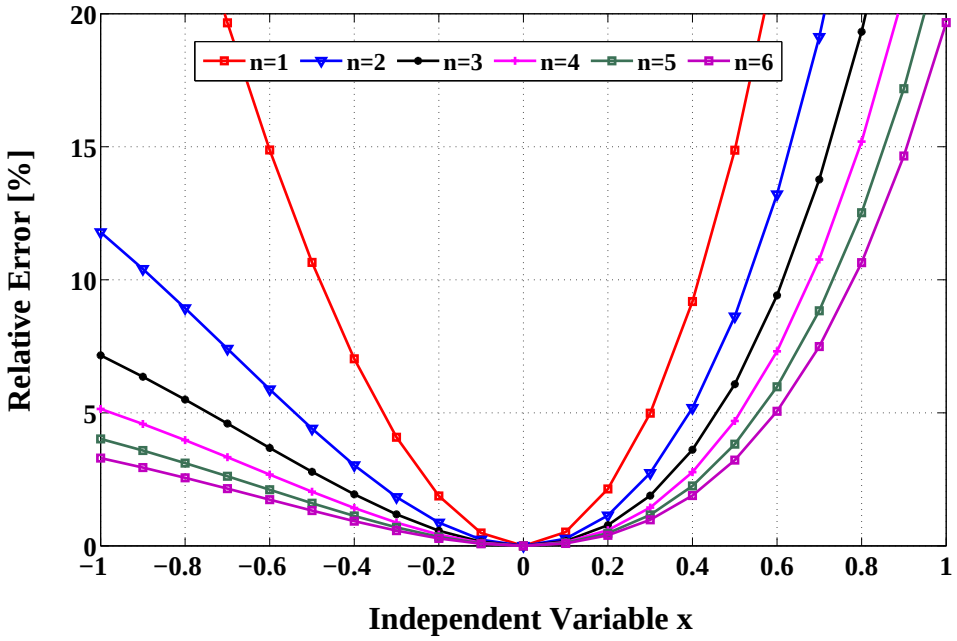


Figure 2.8: Relative error of the proposed exponential function in (2.13).

defined as gain and the gain-controlling input variable, respectively. Fig. 2.8 shows the error of the exponential approximation function (2.13) with exponential function e^x for various x and n. To rewrite (2.13) another way, consider a regular linear equation

$$y = a\,(x+b)\,, \tag{2.14}$$

where a is the slope of the linear equation and b is the offset in the negative x direction. By raising (2.14) to the power of n, we have

$$\begin{aligned} a^n(x+b)^n &= a^n\,(x+b+n-n)^n \\ &= a^n n^n \left(1+\frac{x+b-n}{n}\right)^n \\ &\approx a^n n^n e^{x+b-n}, \quad for \quad x \approx n-b. \end{aligned} \tag{2.15}$$

As we can see from (2.15), the exponential approximation in (2.13) can be obtained by

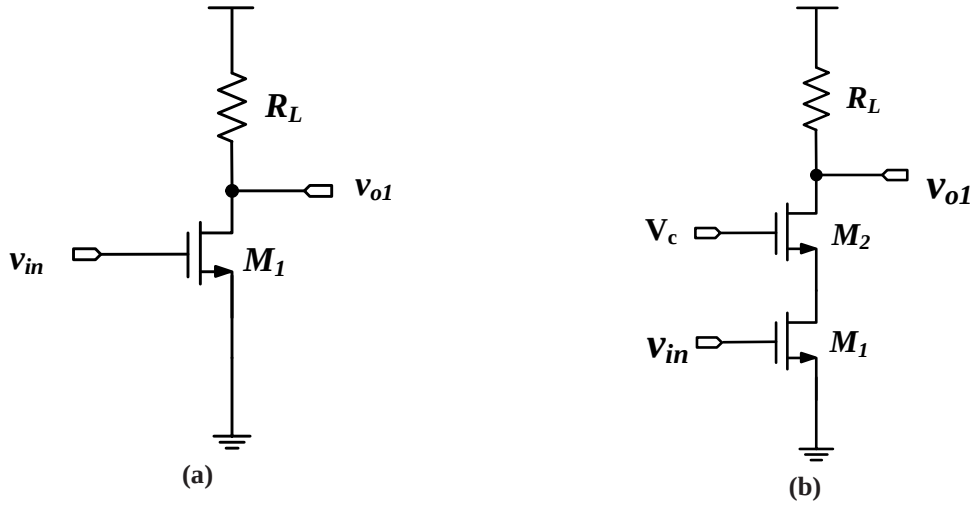


Figure 2.9: (a) A common-source amplifier circuit. (b) A common source cascode amplifier circuit.

assigning an index n. As seen from (2.13) and Fig. 2.8, to decrease the approximation error, *n* should be large. However, in a practical implementation, the maximum value of *n* is limited, so further linear-in-dB compensation techniques are needed to get high resolution linear-in-dB performance [21].

2.3 Broadband VGA techniques

The required VGA topology using in the SKA receiver operating from 0.7 GHz to 1.4 GHz must have wide bandwidth, which is independent of the VGA gain. In this Section, broadband VGA circuit and bandwidth extension techniques are described.

2.3.1 Cascode topology

The theory of improving bandwidth of the amplifier using cascode topology is to suppress the Miller effect of the input transistor, which increases the input capacitance and decreases amplifier bandwidth [51]. Fig. 2.9(a) shows a conventional common-source amplifier cir-

cuit. The input capacitance of this amplifier can be represented as

$$C_{in} = C_{gs,M_1} + \underbrace{C_{gd,M_1}(1+g_{m1}R_L)}_{\text{Miller-effect capacitance}} \tag{2.16}$$

where C_{gs,M_1} and C_{gd,M_1} are the gate-source and gate-drain capacitances of M_1, and g_{m1} is the transconductance of M_1. The Miller-effect capacitance dramatically increases the input capacitance, especially when the magnitude of the amplifier gain $(g_{m1}R_L)$ is high. This large input capacitance limits the bandwidth when impedance of the signal-source is not zero.

To suppress the Miller effect, a cascode transistor M_2 is added as shown in Fig. 2.9(b). In this case, the impedance looking into the drain of M_1 is lowered to $\sim 1/g_{m2}$. In this case, the gain from the gate to drain of M_1 is $-g_{m1}/g_{m2} \approx -1$, and the input capacitance of the amplifier in Fig. 2.9(b) reduces to

$$C_{in} = C_{gs,M1} + 2C_{gd,M1} \tag{2.17}$$

thus increasing the circuit bandwidth. The addition of M_2 however does not affect the gain of the amplifier.

A drawback of adding M_2 is that the cascode transistor reduces the headroom of the circuit. A low headroom could be an issue for low-voltage supply circuits due to reduced voltage swing at their outputs. Also the cascode transistor generates a high frequency pole at the drain of M_1, which may offset some of the bandwidth gained by the reduction of the input capacitance.

2.3.2 Capacitive degeneration

Another method for widening frequency response is to add source degeneration capacitance such that the transconducatnce of the circuit, G_m, increases at high frequencies to

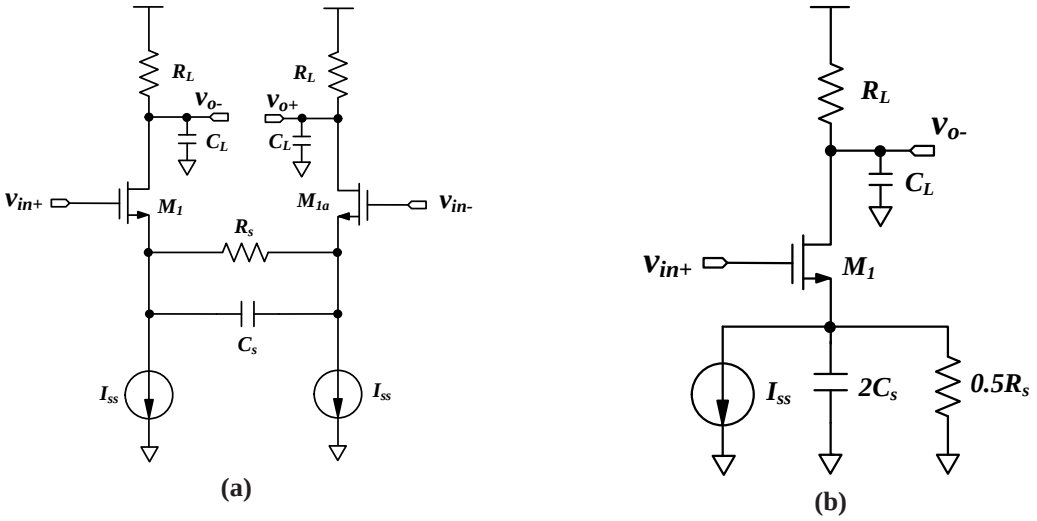


Figure 2.10: (a) Capacitive degenerated differential amplifier circuit**.** (b) Half of capacitive degenerated differential amplifier circuit.

compensate the gain roll-off due to poles at the output node. An example circuit employing capacitive source degeneration is shown in Fig. 2.10.

According to the analysis of the half-circuit, the transconducatnce of the circuit, G_m, can be expressed as

$$G_m = \frac{g_m\left(R_sC_ss+1\right)}{R_sC_ss+1+0.5g_mR_s} \tag{2.18}$$

and the whole transfer function of the amplifier is then

$$A_v = G_mZ_{out} = \frac{g_mR_L\left(R_sC_ss+1\right)}{\left(R_sC_ss+1+0.5g_mR_s\right)\left(1+R_LC_Ls\right)}. \tag{2.19}$$

From (2.19), this circuit has two poles and one zero, which are located at

$$z_1 = \frac{1}{R_sC_s}, \tag{2.20}$$

$$p_1 = \frac{1}{R_LC_L}, \tag{2.21}$$

$$p_2 = \frac{1+0.5g_mR_s}{R_sC_s}. \tag{2.22}$$

p_1 is generated at the output node of the amplifier and is the dominant pole. If the zero

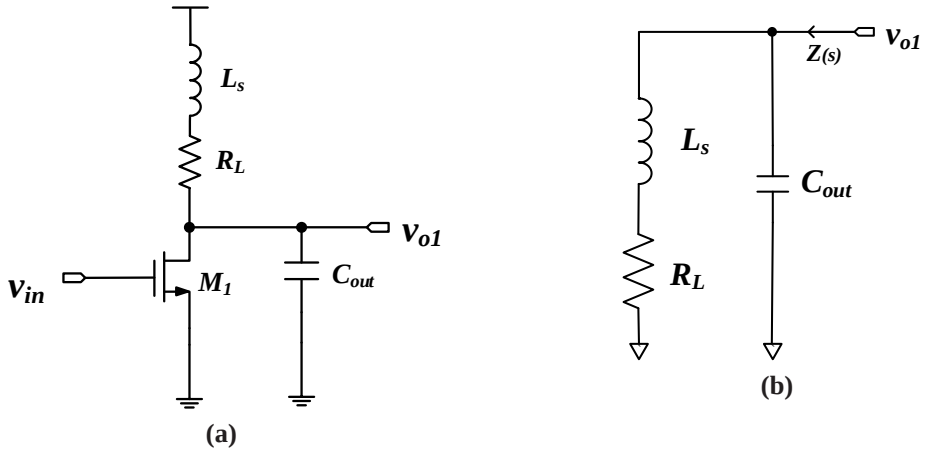


Figure 2.11: (a) Shunt-peaked amplifier. (b) Model of the shunt-peaked amplifier output network.

z_1 is placed such that it cancels the pole p_1, the -3 dB bandwidth can be extended to p_2, which is located at a higher frequency. If z_1 and p_1 cannot completely cancel each other, they generate a peak in the gain response. Using this technique, the bandwidth extension is obtained at the cost of DC gain of the amplifier. The advantage of this circuit is that the gain can be controlled by varying R_s and the input transistor transconductance**.**

2.3.3 Shunt peaking

To compensate the output capacitance of the amplifier, which forms the dominant pole that limits its bandwidth, an inductor can be added at the output node to reduce the effect of the output capacitance and thus to increase the amplifier gain roll-off frequency [52, 53].

In order to explain the operating theory of a shunt-peaked load and to optimize the shunt-peaked amplifier for maximum bandwidth, a common-source amplifier with an inductive load shown in Fig. 2.11 is analyzed. The output impedance of the output *RLC* network, which models the equivalent output impedance of the amplifier, may be written as

$$Z_{out}(s) = (sL_s + R_L) \parallel \frac{1}{sC_{out}} = \frac{R_L\left[s\left(L_s/R_L\right)+1\right]}{s^2C_{out}L_s + sR_LC_{out} + 1}. \tag{2.23}$$

The magnitude of the gain of the amplifier is the product of transconductance g_m of M_1 and

the magnitude of $Z_{out(S)}$ found from

$$|Z_{out}(j\omega)| = R_L \sqrt{\frac{(\omega L_S/R_L)^2 + 1}{(1-\omega^2 C_{out} L_s)^2 + (\omega R_L C_{out})^2}} \tag{2.24}$$

The term in the numerator in (2.24) increases with frequency, which causes the amplifier gain to increase. Furthermore, the term $\left(1-\omega^2 C_{out} L_s\right)$ in the denominator also contributes to increasing $|Z(j\omega)|$ for frequencies below the $L_s C_{out}$ resonance frequency. Both of these terms extend the amplifier bandwidth.

To demonstrate a procedure of selecting L_s for given R_L and C_{out}, a factor ξ is introduced as

$$\xi = \frac{R_L C_{out}}{L_s/R_L}. \tag{2.25}$$

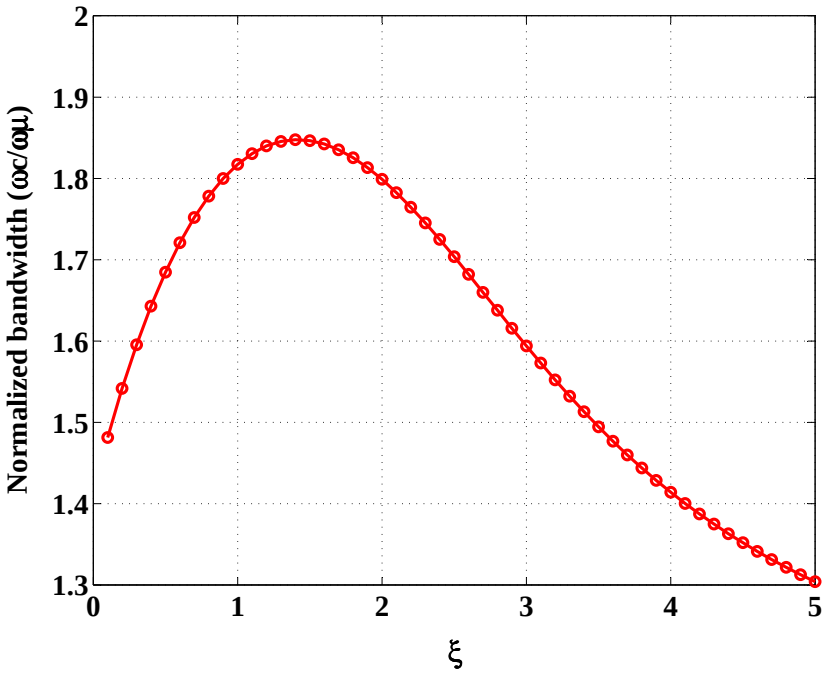
Rearranging (2.24) and normalizing it by R_L gives

$$\frac{|Z_{out}(j\omega)|}{R_L} = \sqrt{\frac{(\omega\tau)^2 + 1}{(1-\omega^2\tau^2\xi)^2 + (\omega\tau\xi)^2}}, \tag{2.26}$$

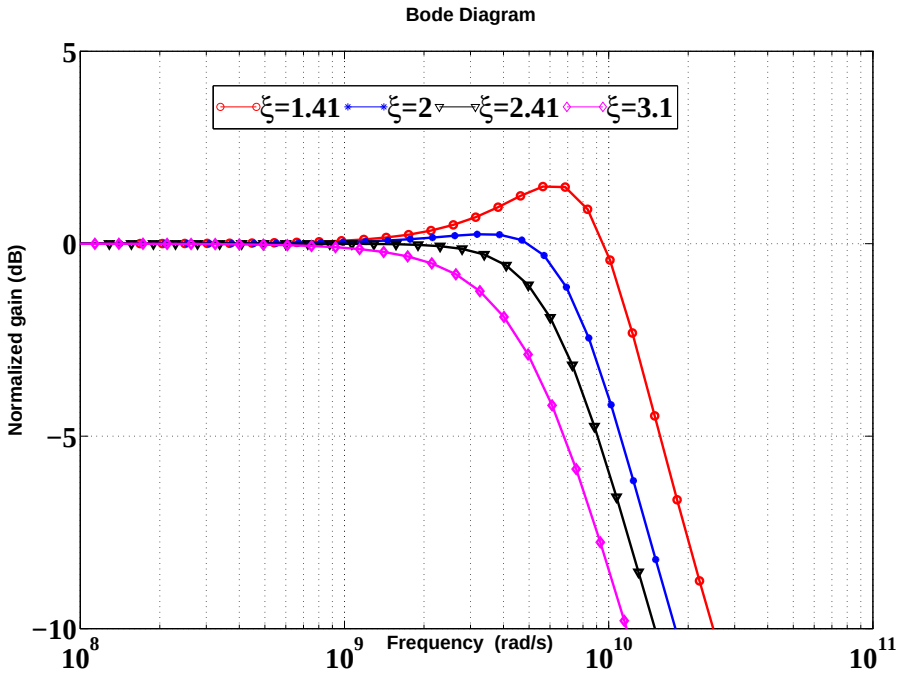
where $\tau = L_s/R_L$. The normalized bandwidth, which is the ratio of the compensated -3 dB bandwidth, ω_c, to the uncompensated -3 dB bandwidth ω_u is

$$\frac{\omega_c}{\omega_u} = \sqrt{\left(-\frac{\xi^2}{2} + \xi + 1\right) + \sqrt{\left(-\frac{\xi^2}{2} + \xi + 1\right) + \xi^2}}. \tag{2.27}$$

The relationship between normalized bandwidth and ξ is shown in Fig. 2.12(a) and the frequency responses are shown in Fig. 2.12(b). The maximum bandwidth extension of 1.85 at $\xi = 1.45$ is achieved albeit with a 20% peak in the frequency response. The maximally flat frequency response happens when $\xi = 2.41$, which leads to a bandwidth extension of 1.72. These simulation results are summarized in Table 2.1.



(a)



(b)

Figure 2.12: (a) Normalized bandwidth versus factor ξ. (b) Frequency response of shunt-peaked amplifier for different ξ.

Table 2.1: Relationship between ξ and bandwidth extension and the peak in the frequency response

Condition	ξ	Normalized bandwidth	Normalized peak in frequency response
Maximum bandwidth	$\sim$1.41	$\sim$1.85	1.19
$\lvert z_{out}\rvert = R_L$ $@\omega = 1/R_L C_{out}$	2	$\sim$1.8	1.03
Maximum flat frequency response	$\sim$2.41	$\sim$1.72	1
Best Group delay	$\sim$3.1	$\sim$1.6	1
No inductive peaking	∞	1	1

2.4 Bandwidth of a cascaded VGA chain

Owing to the limitations of the control range, when a large dynamic range is required, multiple-stages are often used. When multiple stages are cascaded to form a high-frequency wide-input-dynamic-range VGA, the bandwidth requirements on each stage increase. For a cascade of n identical gain stages, the -3 dB bandwidth of the whole VGA chain is

$$\omega_{3dB} = \omega_p \sqrt[m]{2^{1/n} - 1} \tag{2.28}$$

where ω_p is the single stage VGA bandwidth, n is the number of cascaded stages and m equals to 2 for first-order stages and 4 for second-order stages [53, 54].

The ratio of the gain-bandwidth product of the whole VGA chain, GBW_{tot}, and an individual stage, GBW_s, is given by

$$\frac{GBW_{tot}}{GBW_s} = A_{tot}^{(1-1/n)} \times \sqrt[m]{2^{1/n} - 1} \tag{2.29}$$

where A_{tot} is the total cascaded VGA chain gain. This result provides guidance on how to optimize the individual stage GBW_s and number of stages n for a desired GBW_{tot} of the chain with identical individual stages. Fig. 2.13 plots the individual stage GBW_s requirement for a cascade of n first-order ($m = 2$) and second-order ($m = 4$) gain stages with an

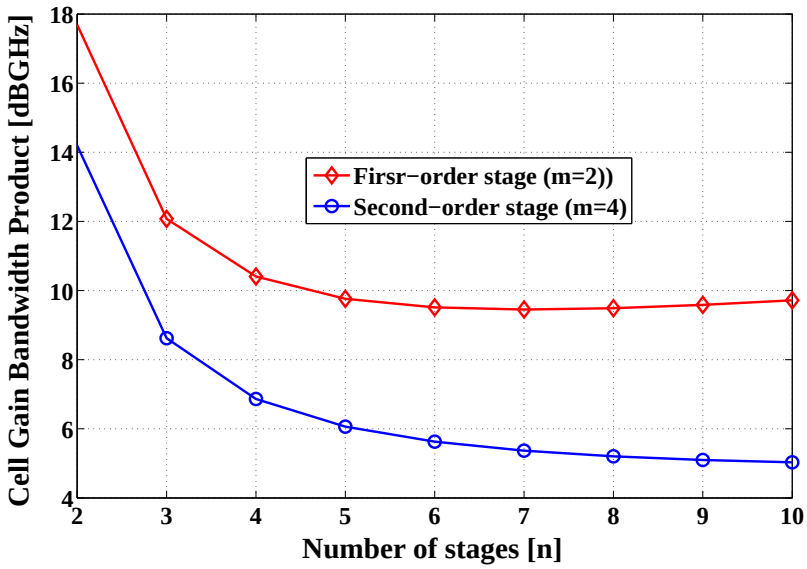


Figure 2.13: Relationship between *n* and *m* for a 40 dB chain voltage gain and 1.8 GHz bandwidth.

expected total gain of 40 dB and bandwidth of 1.8 GHz. From Fig. 2.13, the first-order stage needs higher gain-bandwidth product while the second-order stage relaxes the gain-bandwidth product of each stage. For an overall gain-bandwidth product and larger number of gain stages *n*, there is less gain-bandwidth requirement for each gain stage, but the lower gain-per-stage leads to rapid accumulation of noise. Therefore, the trade-off between *n* and the overall noise requirement must be considered when choosing the number of cascade stages. In general, for reasonable noise figure, *n* should be less than 5.

2.5 Conclusions

This chapter started with the discussion of broadband VGA topologies, which included transconductance-tunable VGAs, load-tunable VGAs, and feedback-tunable VGAs. The Chapter then proceeded with the discussions of exponential-function realization approaches and bandwidth extension techniques, which can be used to extend a VGA bandwidth. In the last Section of the Chapter, a bandwidth optimization method was discussed for a cascade of VGAs.

Based on discussion, the most suitable VGA topologies for broadband applications are the transconductance-tunable VGAs that have the potential of providing gain-independent bandwidth. For realization of the exponential function, the intrinsic exponential characteristics of bipolar transistors and MOSFET transistors in subthreshold have temperature-dependent performance and high noise performance, respectively, which limit their application. The pseudo-exponential function approximation-II based on the Taylor series expansion method discussed in Section 2.2.2 can provide very large gain range, but has two variables in its characteristic equation and needs complicated circuits to realize the function, which may not be optimum for low power consumption with a variable gain range of less than 60dB. The exponential function based on the linear function discussed in Section 2.2.3 needs additional linear compensation techniques to obtain high resolution linear-in-dB performance. This compensation adds to power consumption. The pseudo-exponential function approximation-I in Section 2.2.2 is relatively simple and easy to realize using a simple circuit with very low power consumption, which is an important consideration for the SKA receiver design, and was adopted in this thesis.

After the exponential function discussion, the Chapter continued with discussion of VGA bandwidth extension techniques, which included cascode, capacitive degeneration and shunt peaking. The shunt peaking technique was selected due to its flexible bandwidth control performance.

At the end of the Chapter, bandwidth requirements of a single stage for a casade of n identical VGAs are discussed. This will be revisited in this thesis when cascading VGAs to increase their tunable range.

Chapter 3

Broadband VGAs for an SKA receiver

Based on the discussion of broadband linear-in-dB VGA realization techniques in Chapter 2, this Chapter presents two VGA circuits for application in an SKA receiver. The proposed VGA circuit unit cell is presented in Section 3.1. Using this block, the first designed VGA circuit is described in Section 3.2. The design procedure and parameter optimization are discussed and experimental results are provided. To further extend VGA bandwidth, the second VGA, which is based on the first one, with a bandwidth extension technique is presented in Section 3.3, and experimental results are reported to verify the design expectations.

3.1 Proposed VGA circuit unit cell

A circuit that realizes the pseudo-exponential transfer characteristic between the input voltage and the output current is shown in Fig. 3.1(a) and its small-signal model is shown in Fig. 3.1 (b). If the transconductance of M_a, g_{ma}, is set to be twice the transconductance of

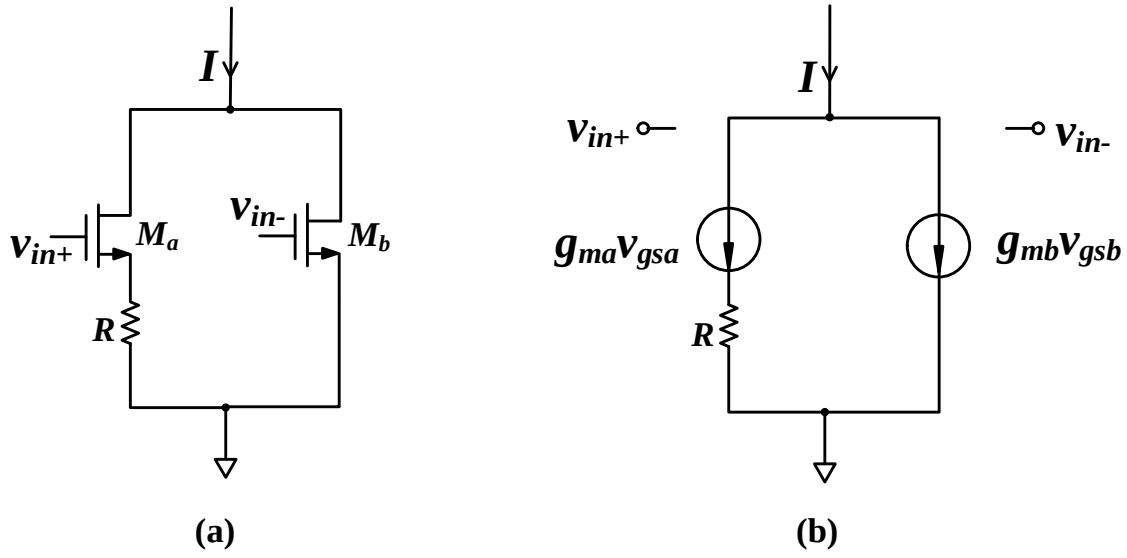


Figure 3.1: Pseudo-exponential function generator and its small signal model (g_{ds}'s are ignored).

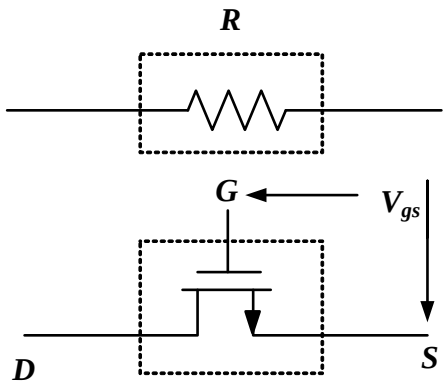


Figure 3.2: MOS realization of resistor.

M_b, g_{mb}, according to the small-signal model analysis, the transconductance of the whole circuit, G_{ms}, can be written as

$$G_{ms} = \frac{I}{v_{in+} - v_{in-}} = \frac{1}{2} g_{ma} \left(\frac{1 - g_{ma}R}{1 + g_{ma}R} \right). \tag{3.1}$$

This equation has the same form as

$$e^{-2x} \approx \frac{1-x}{1+x} = y, \tag{3.2}$$

which was discussed in Section 2.2.2. The term $g_{ma}R$ in (3.1) is equivalent to x in (3.2), and controls the range of G_{ms}. Note that an accurate linear-in-dB approximation ($\pm 1\,dB$ error) in (3.2) only happens when $|x| \leq 0.45$ as shown in Fig. 2.6. Applying this to (3.1) means that only small $g_{ma}R$ values give G_{ms} a desirable linear-in-dB approximation from pseudo-exponential characteristics. Another important parameter of this VGA is voltage gain, which is proportional to G_{ms}. Large G_{ms} requires large g_{ma} as in (3.1). To have large g_{ma} while keeping $g_{ma}R$ within the desired range for a desirable pseudo-exponential transfer function, small R must be used.

In standard CMOS processes, R is easily realized using a MOS transistor as shown in Fig. 3.2 working in triode with its channel resistance modeled by

$$R = \left(\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t) \right)^{-1} \tag{3.3}$$

where V_{gs} and V_t are the gate-to-source voltage and the threshold voltage of the transistor, respectively, and W and L are the transistor channel width and length. When the gate-source voltage, V_{gs}, on the triode transistor varies by ΔV, the resultant change in its channel resistance can be expressed as

$$\Delta R = \left(\frac{1}{K_1 V_{od}^2 + K_1 \cdot V_{od} \cdot \Delta V} \right) \cdot \Delta V \cdot \left(\frac{W}{L} \right)^{-1}, \tag{3.4}$$

where K_1=$\mu_n C_{ox}$, $V_{od} = V_{gs1} - V_t$, and V_{gs1} is minimum gate-source voltage to turn the triode transistor on. This change in resistance affects the VGA transconductance range as

$$\Delta G_{ms} = \frac{2g_{ma}^2}{2 + g_{ma}R} \cdot \frac{1}{[(1 + g_{ma}R)/(2\triangle R) + g_{ma}]}. \tag{3.5}$$

Equations (3.3) and (3.4) show that both R and ΔR are inversely proportional to (W/L) and therefore large (W/L) results in small R and ΔR. However, according to (3.5), the small ΔR also results in a low gain range of the VGA. Therefore, when the VGA is designed for the maximum gain with large g_{ma}, a small variable gain range results. This suggests that the gain and variable gain range are traded off. This trade-off was exploited in this thesis to significantly decrease the power consumption of our design relative to the VGA in [32].

3.2 Proposed VGA circuit I

3.2.1 VGA schematic design

The proposed differential linear-in-dB VGA circuit using the building block of Fig. 3.1 is shown in Fig. 3.3. The differential input is applied to $M_{1,4}$ and $M_{2,3}$, which correspond to two pairs of M_a and M_b in Fig. 3.1. M_9 and M_8 are loads for $M_{1,4}$ and $M_{2,3}$ respectively. This differential circuit provides the possibility to bias the transistors M_{1-4} using current

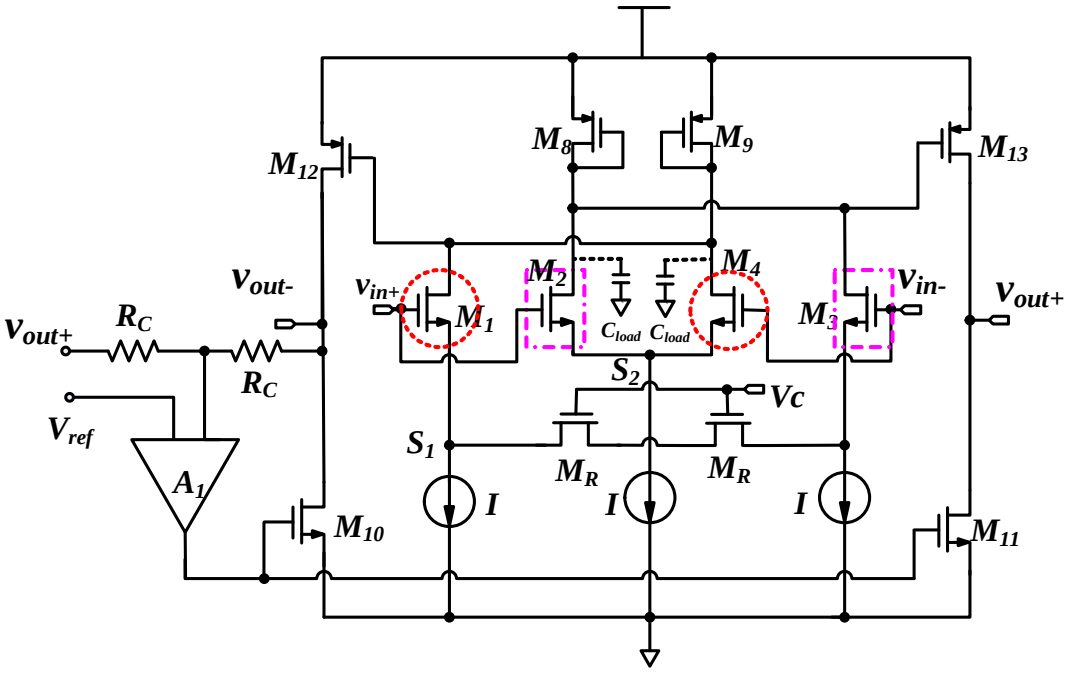


Figure 3.3: Differential linear-in-dB VGA circuit.

sources I, which are realized with common-source MOS transistors working in the saturation region. Instead of resistive loads in [32], diode-connected $M_{8,9}$ serve as active loads in this design to increase the voltage headroom at low power supply voltage. Two M_R working in the triode region are variable resistors R in Fig. 3.1. The VGA control voltage V_c adjusts the resistance R and the VGA gain. In order to further increase the VGA gain, second stage amplifiers, which are formed by M_{10-14}, are added. Also a common-mode feedback circuit, which includes two resistors R_C and an amplifier A_1, are used to compensate the PVT variation of the VGA.

In order to simplify the analysis, the small-signal model of half of the circuit is shown in Fig. 3.4. With M_{1-4} sized the same to keep the same input capacitance for all inputs, the biasing is set to provide $g_{m1,3} = 2g_{m2,4}$. In such a case, the small-signal analysis shows that the differential VGA transconductance, defined as $G_{m,}$ is double G_{ms} in (3.1). The VGA single-ended output resistance, seen at the drain of $M_{8,9}$ is

$$R_{out} = \frac{r_{o1,3} \cdot r_{o2,4}}{r_{o1,3} \cdot (1 + g_{m1,3}R) + r_{o2,4}} \parallel \left(\frac{1}{g_{m8,9}}\right) \tag{3.6}$$

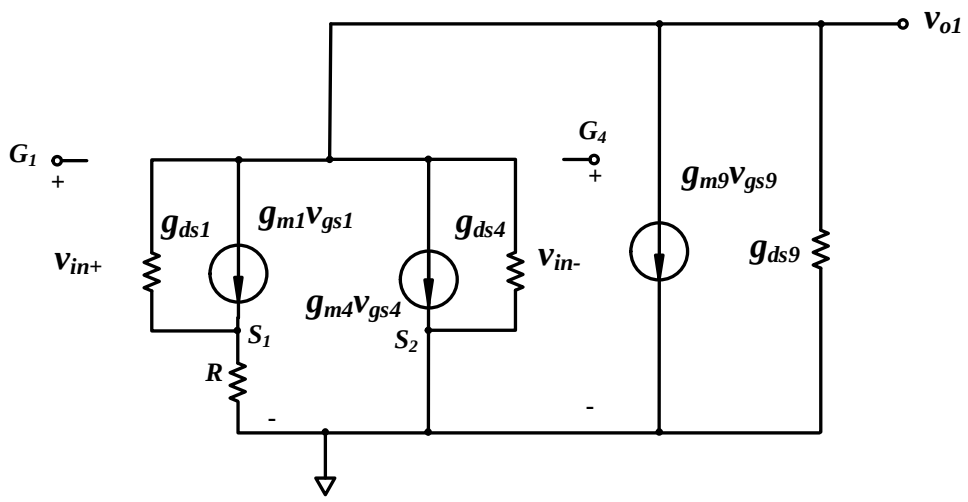


Figure 3.4: Small signal model of differential linear-in-dB VGA(half circuit).

where r_{o1-4} are the output resistances of M_{1-4} and $g_{m1,9}$ are transconductances of $M_{1,9}$. The total single-ended output resistance of the VGA is reduced by the $g_{m1,3}R$ product and a parallel combination with $1/g_{m8,9}$. This lowered resistance results in wide bandwidth. A substitution of R from (3.3) into (3.1) gives a relationship between VGA G_m and M_R gate-source voltage, V_{gs}, as

$$G_m = 2G_{ms} = g_{m1,3} \cdot \left(\frac{1-\alpha(V_{gs}-V_t)}{1+\alpha(V_{gs}-V_t)} \right) \tag{3.7}$$

where $\alpha = \mu_n C_{ox} \frac{W}{g_{m1,3}L}$, $V_{gs} = V_c - V_s$ is the gate-to-source voltage of M_R and V_c is the gate voltage of M_R and is also the VGA gain control voltage. Therefore, as discussed in Section 3.1, by adjusting V_c the pseudo-exponential behavior of the output current with input voltage is obtained. With M_{10-13} providing extra gain, the gain of the whole VGA can be written as:

$$A_V = \frac{g_{m1,3}}{g_{m8,9}} \cdot \left(\frac{1-\alpha(V_{gs}-V_t)}{1+\alpha(V_{gs}-V_t)} \right) \cdot \left(\frac{g_{m12,13}}{g_{ds12,13}+g_{ds10,11}} \right) \tag{3.8}$$

where $g_{m12,13}$ are the transconductance of $M_{12,13}$ and $g_{ds10-13}$ are the output conductances of M_{10-13}.

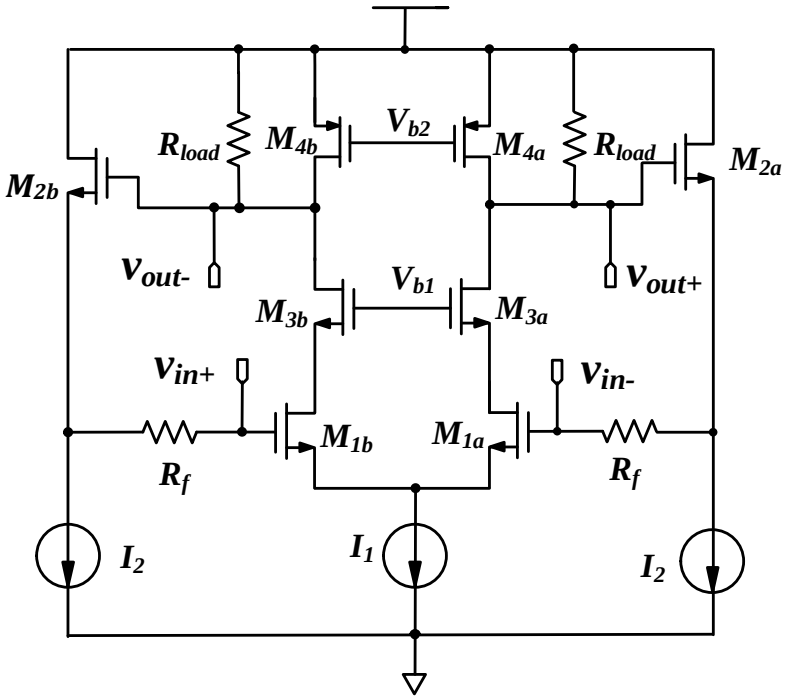


Figure 3.5: Input power-match circuit.

In order to measure the VGA circuit, an input match circuit with low noise figure is also designed in this work as shown in Fig. 3.5. A common-source cascode amplifier with active feedback through $M_{2a,2b}$ and R_f's is used to accomplish input power match to 100 Ω differential resistance from 0.7 GHz to 1.4 GHz while providing additional gain. $M_{4a,4b}$ are used as current sources reducing the voltage drop across R_{load}. The input match is achieved when [46]

$$g_{m2a,b} = \frac{1}{R_s \cdot (1 + g_{m1a,b} \cdot R_{load}) - R_f}, \tag{3.9}$$

where R_s and R_f are the signal-source resistance and the feedback resistance, respectively, and $g_{m1a,b}$ and $g_{m2a,b}$ are the transconductances of $M_{1a,1b}$ and $M_{2a,2b}$, respectively.

According to the small signal analysis, the noise factor of the input match circuit is given by [46]:

$$F = 1 + \frac{\gamma_1}{g_{m1a,b}R_s} + \frac{R_f}{R_s\left(1+A_v\right)^2} + \frac{\gamma_2}{1+A_v}\left[1 - \frac{R_f}{R_s\left(1+A_{v)}\right)}\right] + \frac{\gamma_1}{g_{m1a,b}R_sA_v} + \gamma_{bias}g_{m,bias}R_s\left[\frac{R_f}{R_s\left(1+A_v\right)}\right]^2 \tag{3.10}$$

where γ is the thermal excess noise factor, and A_v is the open-loop gain of the amplifier. Once the input is power matched, the dominant term in (3.10) is the second term, which is the contribution of $M_{1a,1b}$. Larger $g_{m1a,b}$ produces lower noise figures but narrower bandwidth due to larger capacitance. Note that this dominant term is independent of R_f, which can be used to tune the input power match. However, as seen from (3.10) sufficiently large R_f may increase the noise figure. The lowest noise for the lowest current consumption is therefore achieved for $R_f = 0$. The noise contribution of the bias current I_2 can be reduced by using a longer-than-minimum channel length device, and sizing the transistor for a relatively high overdrive voltage. Since the feedback device draws low current, its noise contribution is small.

The output buffer in Fig. 3.6 is used to match VGA output to a 100 Ω differential load to allow VGA measurements. This buffer and the input match circuit are not required when the VGA is integrated in an SKA receiver.

3.2.2 Two-stage cascaded VGA chain

As discussed in Section 2.2.2, the selected pseudo-exponential function approximation function provides the linear-in-dB range of 17dB with a maximum error of ±0.6 dB. In order to have more than 20 dB variable gain range, which is the specification for an SKA receiver, two of the proposed VGA circuits in Fig. 3.3 were cascaded as shown in Fig. 3.7. Differential 100 Ω input and output match circuits are included on chip.

In order to extend the -3 dB bandwidth beyond 1.4 GHz, according to (2.28), for a second-order VGA, the minimum bandwidth needs to be larger than 1.75 GHz for a cascade

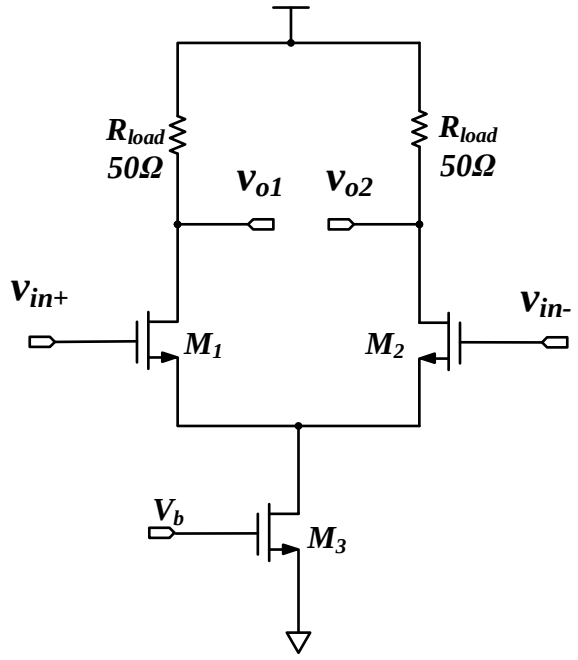


Figure 3.6: VGA output buffer.

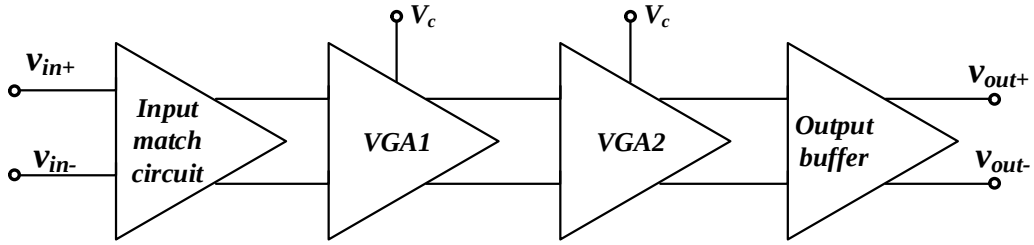


Figure 3.7: 2-stage VGA topology with input and output match circuits.

of two VGAs. If input match and output buffer circuits, which are not needed when the VGA is embedded in an SKA receiver, are considered, there are four cascade stages. Using (2.28), a 2.2 GHz -3 dB bandwidth requirement for each stage is obtained.

3.2.3 Simulation and measurements results

This design was fabricated in ST 65nm triple-well CMOS technology, and the chip micrograph is shown in Fig. 3.8. The fabricated circuit occupies $80.1\mu\text{m} \times 148.3\mu\text{m}$ of area. The simulated and measured input reflection coefficient (S11) of the VGA preceded by the input match circuit are shown in Fig. 3.9. Measurement results show that S11 is less than -12.5 dB across the mid-frequency range of the SKA receiver. As the input match circuit

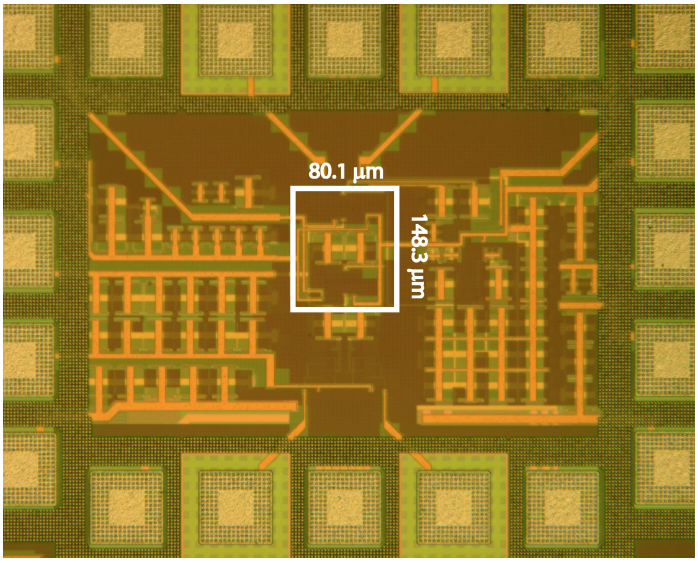


Figure 3.8: Micrograph of fabricated VGA.

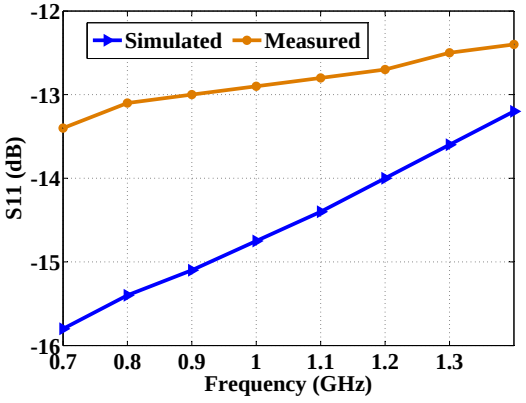


Figure 3.9: Input reflection coefficient S11 of the VGA over the SKA mid-frequency bandwidth.

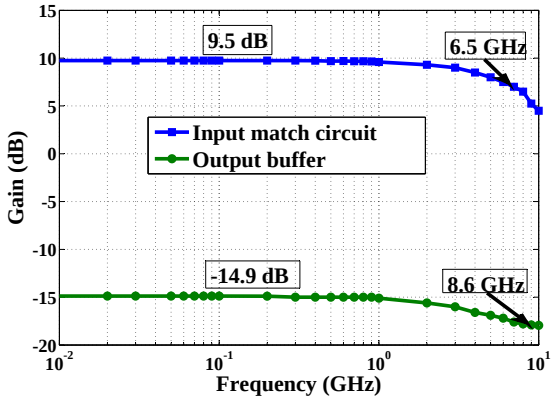


Figure 3.10: Gains of input match circuit and the output buffer of two stages VGA circuit.

and the output buffer are embedded with the VGA circuit, their gain cannot be measured separately. Only simulation results are provided as shown in Fig. 3.10 and cannot be verified by measurement results directly. The input match circuit provides a DC gain of 9.5 dB and -3 dB bandwidth of 6.5 GHz while the output buffer alone has gain of -14.9 dB and -3 dB bandwidth of 8.6 GHz. Since the output buffer is only added for measurements, its low gain is not a concern and is the result of using small current for low power consumption.

The simulated frequency responses of the VGA with and without output buffer are

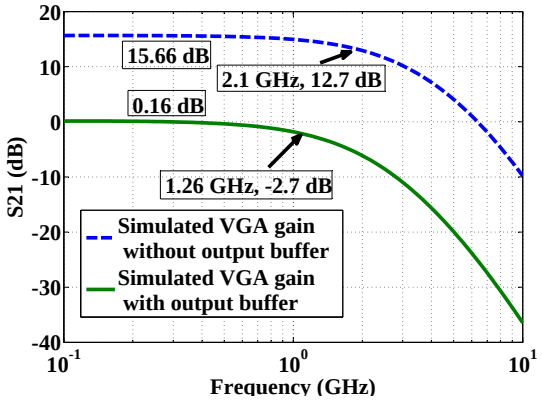


Figure 3.11: Comparison of simulated VGA bandwidth with and without output buffer.

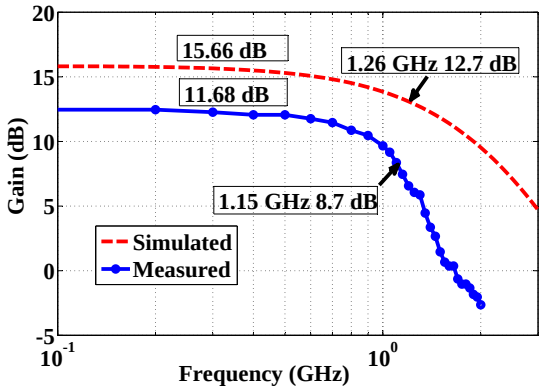


Figure 3.12: Comparison of simulated and measured de-embedded VGA gain.

shown in Fig. 3.11, resulting in -3 dB bandwidths of 1.26 GHz and 2.1 GHz. The output buffer decreases the VGA -3 dB bandwidth to 1.26 GHz, which is in line with the measurement result of 1.15 GHz for the implemented VGA as illustrated in Fig. 3.12. The main reason for lower bandwidth than expected is the capacitive loading of the output buffer. The maximum de-embedded gain of the two-stage cascaded VGA is 11.7 dB, which is 5 dB lower than in the simulations. This gain decrease is likely caused by the process variations. According to corner simulations, the measured gain is close to SS (slow slow) models instead of TT (typical typical) models that are shown in Fig. 3.12. However, since the buffer is not needed in an SKA receiver, the VGA bandwidth is expected to be sufficiently wider than 1.15 GHz, when integrated in the receiver.

Fig. 3.13 presents a comparison of simulated and measured gain ranges of the VGA at frequencies of 0.7 GHz and 1.4 GHz with the buffer gain de-embedded. The measured maximum tunable gain range is from -13 dB to 10 dB at 0.7 GHz and -19 dB to 6 dB at 1.4 GHz when external control voltage varies between 0.5 V and 1 V. The linear-in-dB variable gain range has larger deviation from the expected linear-in-dB performance when control voltage becomes small, which corresponds to the VGA accepting low input power and operating in a high gain mode. Low input power increases source voltage of M_{1-4} in

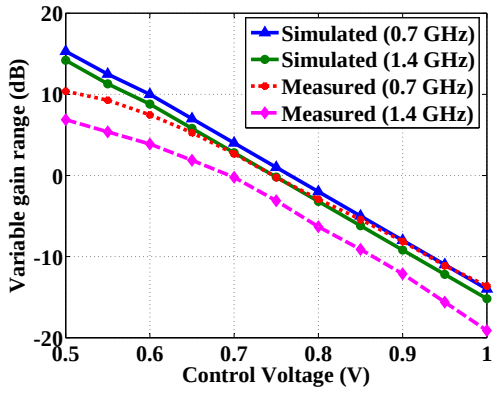


Figure 3.13: Comparison of simulated and measured VGA gain range versus external control voltage.

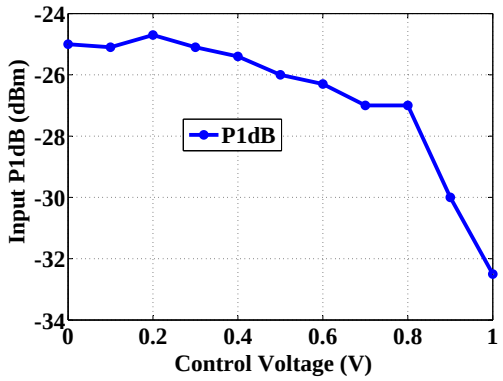


Figure 3.14: Measured VGA input P1dB at 0.7 GHz.

Fig. 3.3 while low control voltage further decreases the gate-source voltage of transistor M_R and moves M_R from the triode region to the subthreshold region. The linear relationship between M_R channel resistance and control voltage is no longer correct, which causes the gain of the VGA to depart from the expected linear-in-dB performance. Fig. 3.14 shows the input P_{1dB} versus the control voltage. The minimum input P_{1dB} is -32 dBm for the VGA with the input match circuit. When the gain of the input match circuit is de-embeded, input P_{1dB} of the VGA is approximately -22.5 dBm. The input dynamic range of this VGA is from -40 dBm to -15 dBm for a constant output power level of -27 dBm. The power consumption of the core VGA is 1 mW, which is much lower than in [32, 54]. The input and output match circuits consume 7 mW.

3.3 Proposed VGA circuit II

As discussed in Section 3.2.3, the measured VGA bandwidth was less than 1.4 GHz, which cannot meet the requirement of the SKA mid-frequency-range receiver. Also, the linear-in-dB range had large deviation from the expected linear-in-dB performance, which was due to the non-linearity of the variable resistance of M_R. In order to improve the bandwidth and linearity while increasing the maximum VGA gain as well, an improved VGA circuit

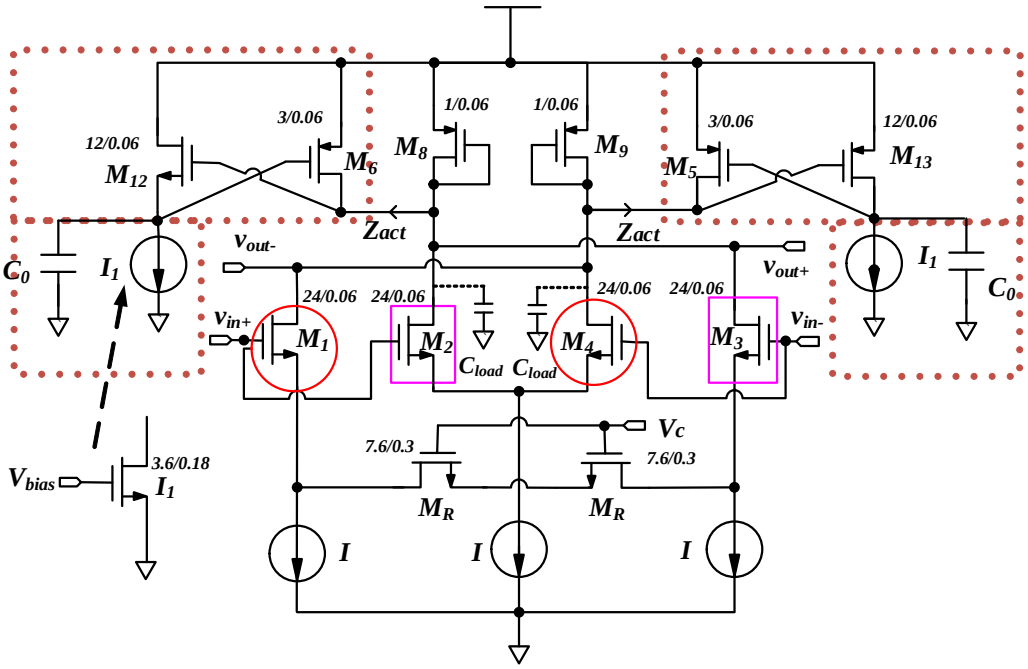


Figure 3.15: VGA with active-inductor loads. Dashed lines around cross-coupled-pair circuits indicate the active-inductor networks.

is discussed in this section.

3.3.1 Active inductor-load VGA

An improved VGA based on Fig. 3.3 is shown in Fig. 3.15. M_{1-4}, $M_{8,9}$ and current source I all appear in Fig. 3.3. A low-threshold-voltage transistor, instead of the standard threshold voltage transistor, M_R, is used in this circuit to improve the linear-in-dB gain range and its linearity. The circuits identified by the dashed lines form inductors, which are added at the output nodes to resonate out the VGA output node capacitance and to improve the VGA bandwidth. Transistors $M_{5,6}$, $M_{8,9}$ and $M_{12,13}$, the capacitors C_0 and the current sources I_1 are VGA loads.

The small-signal equivalent impedance of the active inductor circuit, Z_{act}, shown in Fig.

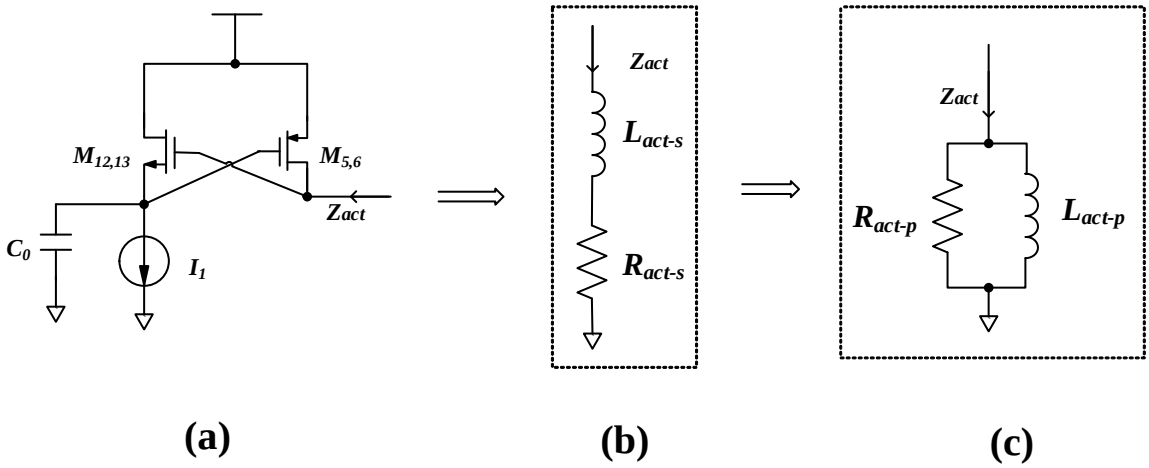


Figure 3.16: (a) Active load inductor circuit. (b) Series equivalent network. (c) Parallel equivalent network.

3.16(a), can be written as [23]

$$Z_{act} = \underbrace{\frac{1}{g_{m5,6}}}_{R_{act-s}} + \underbrace{\frac{sC_0}{g_{m5,6}g_{m12,13}}}_{L_{act-s}}, \tag{3.11}$$

where $g_{m5,6}$ and $g_{m12,13}$ are the transconductances of transistors $M_{5,6}$ and $M_{12,13}$, respectively. This impedance appears as a resistor, R_{act-s}, in series with an inductor, L_{act-s}, as shown in Fig. 3.16(b). It can also be presented by an equivalent parallel network with resistor R_{act-p} in parallel with an inductor L_{act-p} as shown in Fig. 3.16(c), where

$$L_{act-p} = \frac{1}{g_{m5,6}}\left(\frac{C_0}{g_{m12,13}} + \frac{g_{m12,13}}{C_0}\cdot\frac{1}{\omega^2}\right), \tag{3.12}$$

$$R_{act-p} = \frac{1}{g_{m5,6}}\left(\frac{\omega_0^2 C_0^2}{g_{m12,13}^2} + 1\right), \tag{3.13}$$

and

$$\omega_0 = \frac{1}{\sqrt{L_{act-p}C_{load}}}, \tag{3.14}$$

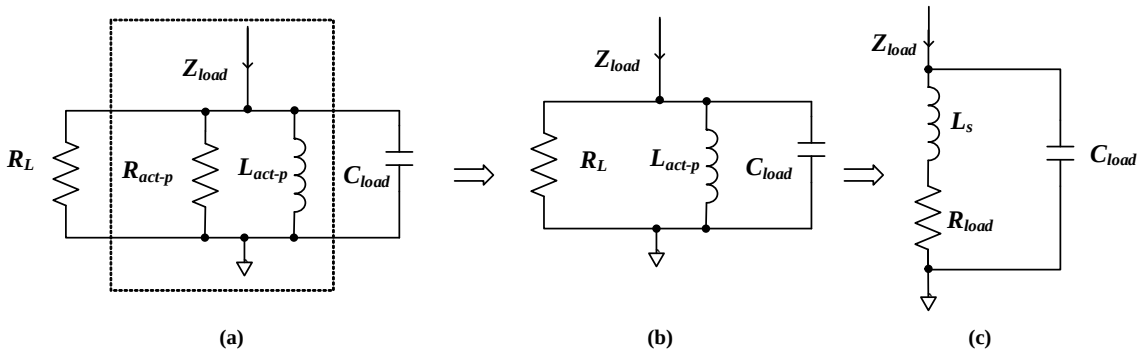


Figure 3.17: (a) VGA load equivalent circuit. (b) Simplified VGA load for $R_L \ll R_{act-p}$. (c) Equivalent Z_{load} of network in (b).

where ω_0 is the resonant frequency of the VGA output node with a total capacitance of

$$C_{load} = C_{gs,M8(9)} + C_{db,M8(9)} + C_{db,M2(4)} + C_{db,M1(3)} + C_{gd,M12(13)} + C_{db,M6(5)} + C_{out}. \tag{3.15}$$

In (3.15), C_{gs}, C_{db} and C_{gd} are the gate-source, drain-substrate and gate-drain capacitances of transistors, respectively, and C_{out} is capacitance at the VGA load (not shown in Fig. 3.15). C_{load} in Fig. 3.15 is larger than the total capacitance in Fig. 3.3 because of the additional active load for bandwidth extension. But as C_{load} is resonated out by the active inductor, it is not a factor affecting the VGA bandwidth. With the active inductors connected to the VGA loads, the total impedance at each of the VGA loads, Z_{load}, can be represented as in Fig. 3.17(a), where $R_L = 1/g_{m8,9}$. Since $R_{act-p} \gg R_L$, then Z_{load} circuit can be equivalent to $R_L \parallel L_{act-p} \parallel C_{load}$ as shown in Fig. 3.17(b). This circuit can be converted to $(sL_s + R_{load}) \parallel C_{load}$, as shown in Fig. 3.17(c). Impedance Z_{load} can be expressed as

$$\begin{aligned} Z_{load} &= \frac{1}{sC_{load}} \parallel \frac{1}{R_L} \parallel R_{act-p} \parallel sL_{act-p} \\ &\approx \frac{1}{sC_{load}} \parallel \frac{1}{R_L} \parallel sL_{act-p} = (sL_s + R_{load}) \parallel \frac{1}{sC_{load}} \\ &= \frac{R_{Load}\left[s\left(L_s/R_{Load}\right)+1\right]}{s^2 C_{load} L_s + sR_{Load}C_{out} + 1} \end{aligned} \tag{3.16}$$

where the same transformations as in Fig. 3.17 are carried out and

$$L_s \approx L_{act-p} = \frac{1}{g_{m5,6}} \left(\frac{C_0}{g_{m12,13}} + \frac{g_{m12,13}}{C_0} \cdot \frac{1}{\omega^2} \right) \tag{3.17}$$

and

$$R_{load} = \frac{g_{m8,9} \left[(\omega_0 C_0)^2 + g_{m12,13}^2 \right]}{\left(g_{m5,6} g_{m12,13} \omega C_0 \right)^2}. \tag{3.18}$$

Based on (3.16), the output impedance of the circuit in Fig. 3.15 has two poles and one zero. The zero is used to cancel out one of the poles and to extend the VGA bandwidth. The equivalent circuit in Fig. 3.17(c) is exactly the same as the load of the shunt-peaked amplifier discussed in Section 2.3.3. Therefore, the method described in Section 2.3.3 can be used here to optimize the VGA bandwidth by an appropriately setting

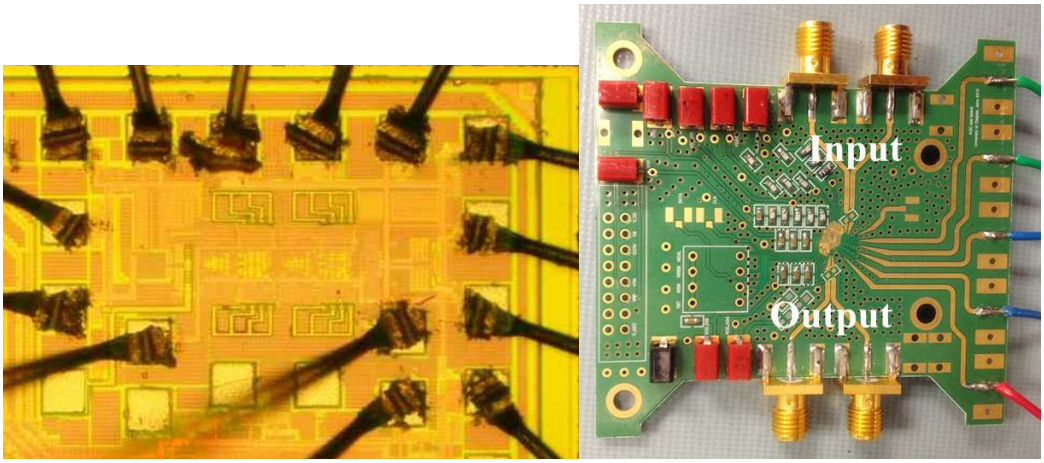
$$\begin{aligned} \xi &= \frac{R_{load} \cdot C_{load}}{L_s / R_{load}} \\ &= \left(\frac{g_{m8,9}}{\omega_0 C_0} \right)^2 \cdot \frac{C_{load}}{C_0} \cdot \left[\frac{(\omega_0 C_0)^2}{g_{m5,6} g_{m12,13}} + \frac{g_{m12,13}}{g_{m5,6}} \right]^3 \end{aligned} \tag{3.19}$$

for either the maximum bandwidth or a flat gain-frequency response.

Since the output inductor can resonate out all of the output node capacitance, the size of input transistors M_{1-4} can be increased, which also helps to improve the VGA gain. Then, the VGA gain at ω_0 is

$$A_V = g_{m1} \left(\frac{1 - \alpha (V_c - V_t - V_r)}{1 + \alpha (V_c - V_t - V_r)} \right) \cdot R_{load} \tag{3.20}$$

where $\alpha = \mu_n C_{ox} W_r / (g_{m1} L_r)$, V_t is the M_R-transistor threshold voltage, and W_r/L_r is M_R width-to-length ratio. Compared with the circuit in Section 3.2.3, the VGA gain is increased because of the transistors $M_{5,6}$, which are part of the active inductor circuit. For a fixed current I, $M_{5,6}$ draw some current away from $M_{8,9}$ thus increasing $1/g_{m8,9}$, which serve as the low frequency load resistance of the VGA. Therefore, for the same overall



(a) **(b)**

Figure 3.18: VGA circuit with bandwidth extension techniques. (a) Micrograph of fabricated VGA. (b) PCB board with the VGA chip.

gain, the second VGA stage in Fig. 3.3 can be removed, improving the circuit bandwidth.

The same input match circuit and output buffer circuit described in Section 3.2.1 were added in this design for measurements. All circuit parameters were redesigned based on a new semiconductor process used for this VGA. Especially the output buffer gain was increased by allowing it to consume more power with lower attenuation.

3.3.2 Simulation and measurement results

Two of the proposed VGA circuits in Fig. 3.15 were cascaded to double the variable gain range. This new VGA circuit was manufactured in TSMC 65 nm CMOS technology and occupies 830 um×530 um of chip area including all bond pads. The chip micrograph and the PCB board for measurement are shown in Fig. 3.18.

To show the bandwidth improvement with the active-inductor load, which can be tuned with C_0 and $g_{m12,13}$, the simulated results of the two cascaded VGAs with the input match circuit and the output buffer embedded are shown in Fig. 3.19. The VGA bandwidth is seen to increase when C_0 goes up from 75 fF to 200 fF, but the peak value of the gain also increases when C_0 exceeds 100 fF as well. From the plot, the -3 dB bandwidth increases

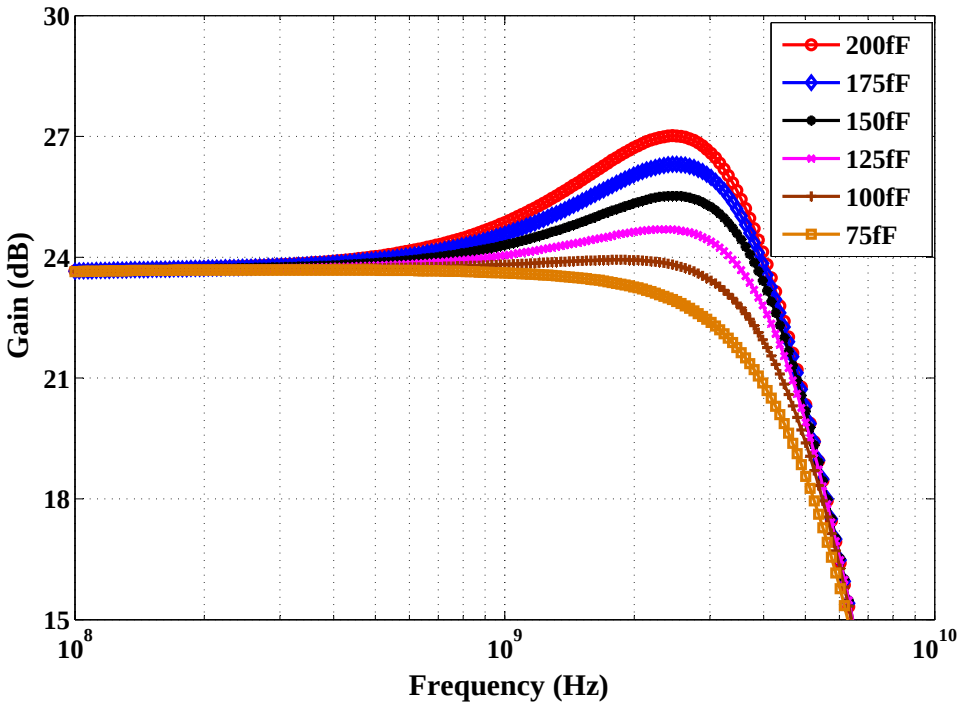


Figure 3.19: Frequency response of the VGA chain (with the input match circuit and the output buffer). Capacitance C_0 was set to 200 fF, 175 fF, 150 fF, 125 fF, 100 fF and 75 fF.

very slowly after C_0 exceeds 150 fF. In this design C_0 of 175 fF was selected to generate only a small inductance at the load of the VGA to compensate any capacitance generated from layout parasitic, resulting in a flat gain over the frequency range.

The VGA bandwidth is also related to the transconductance of transistors $M_{12,13}$ in Fig. 3.15. The simulated VGA chain bandwidth for different V_{bias} of current sources I_1 in Fig. 3.15 is shown in Fig. 3.20. From Fig. 3.20, the VGA bandwidth does not change with $g_{m12,13}$, but the peak gain does change. A V_{bias} of 550 mV was selected in this design to achieve a flat gain and required bandwidth, which is mainly controlled by C_0.

Fig. 3.21 shows the comparison of simulated and measured frequency responses of the VGA chain circuit. The peak voltage gain, S21, in the pre-layout simulation becomes flat in the post-layout simulation due to the parasitic capacitance generated in layout, which is not considered in pre-layout simulation. The two-stage cascaded VGA has a maximum measured S21 of 22.4 dB and simulated S21 of 24.2 dB, of which about 6 dB comes from

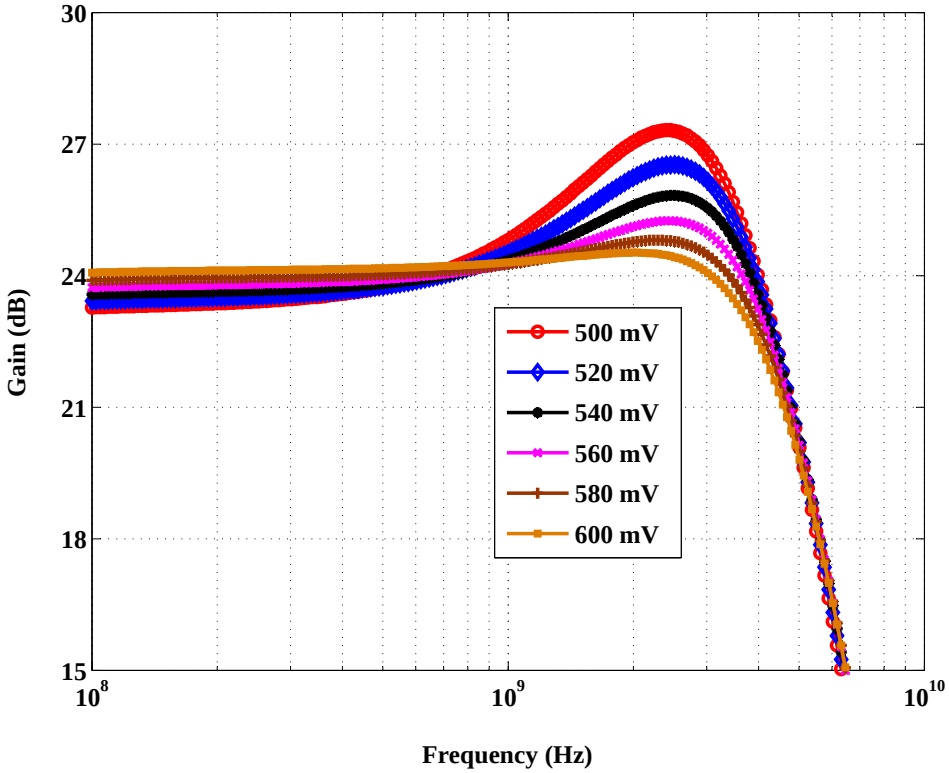


Figure 3.20: Frequency response of VGA chain (with input match circuit and output buffer) as a function of V_{bias} at maximum gain. Vbias was set to 500 mV, 520 mV, 54 0mV, 560 mV, 580 mV and 600 mV to modify $g_{m12,13}$.

the input-match circuit. The circuit has an upper -3 dB frequency of 2.1 GHz in both post-layout simulations and measurements. Compared to the same VGA topology but without the active inductors [3], the VGA bandwidth increases by an additional 1 GHz and the gain increases by 16 dB (from 0.5 dB to 16.4 dB). The DC gain difference between simulations and measurements in Fig. 3.21 is attributed to process variation and parasitics.

Fig. 3.22 shows the measured variable gain range at 0.7 GHz, 1.4 GHz, which are the low and the high frequency edges of the SKA mid-frequency range, the VGA upper -3 dB frequency edge (2.1 GHz) and a lower frequency (0.5 GHz), which might be the low frequency edge for the mid-frequency SKA in the future. Also, the ideal linear-in-dB line is shown for comparison. The VGA has good linear-in-dB performance for all frequencies shown in Fig. 3.22 when variable resistor control voltage, V_c, is varied from 0.65 V to 1 V. The maximum variable gain range is 35 dB (-12.5 dB~22.5 dB) and a linear-in-dB range of

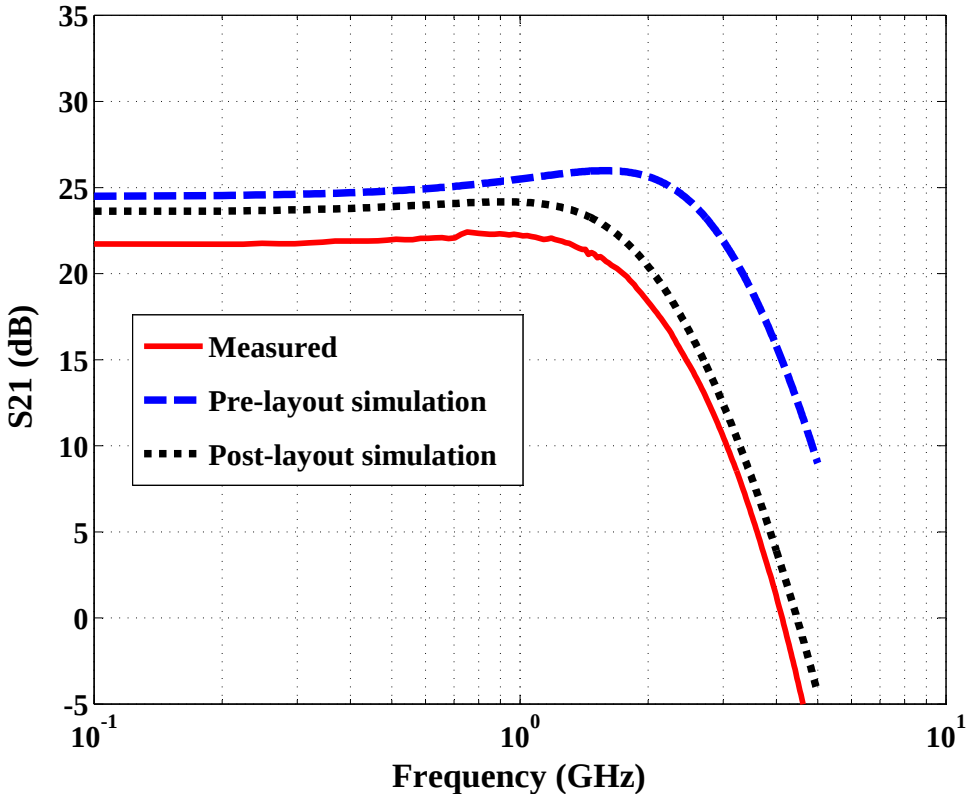


Figure 3.21: Comparison of the VGA frequency response for a pre-layout simulation, a post-layout simulation and measurement results.

28.6 dB (from -12.5 to 16.1 dB) with the maximum deviation from the ideal linear-in-dB curve of ± 1 dB are achieved. Both the variable gain range and the linear-in-dB gain range are dramatically improved compared to the VGA without the active inductor-loads.

Fig. 3.23 shows measured gain for different control voltages within the operating frequency range. The lower operating frequency of the VGA can go beyond 0.1 GHz, which is only limited by the DC blocking capacitors between the two VGA stages and the input match circuit.

Fig. 3.24 shows that the measured input-referred P_{1dB} of the VGA with embedded input match circuit is nearly -22~-23 dBm and is nearly independent of the control voltage. The input and output reflection coefficients, S11 and S22, are shown in Fig. 3.24. S11 is less than -10 dB and S22 is less than -13 dB up to 4.2 GHz. Measured *IIP*3 is -11 dBm at 1.4 GHz.

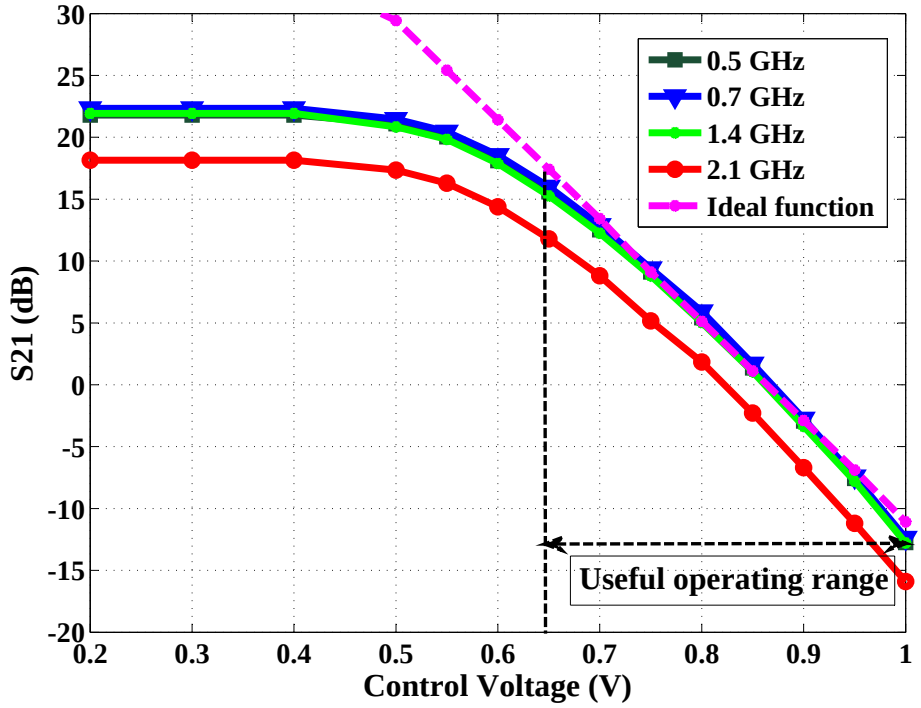


Figure 3.22: Measured variable gain range at different frequencies. 2.1 GHz corresponds to the VGA 3 dB upper frequency range.

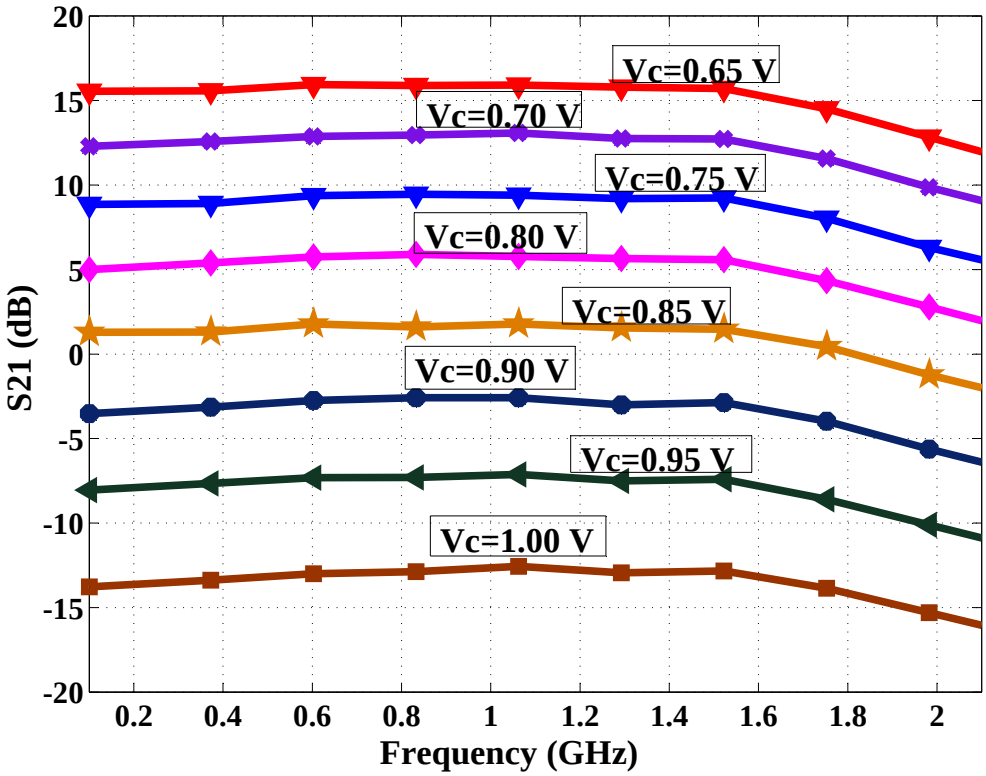


Figure 3.23: Measured gains versus frequency for different control voltages.

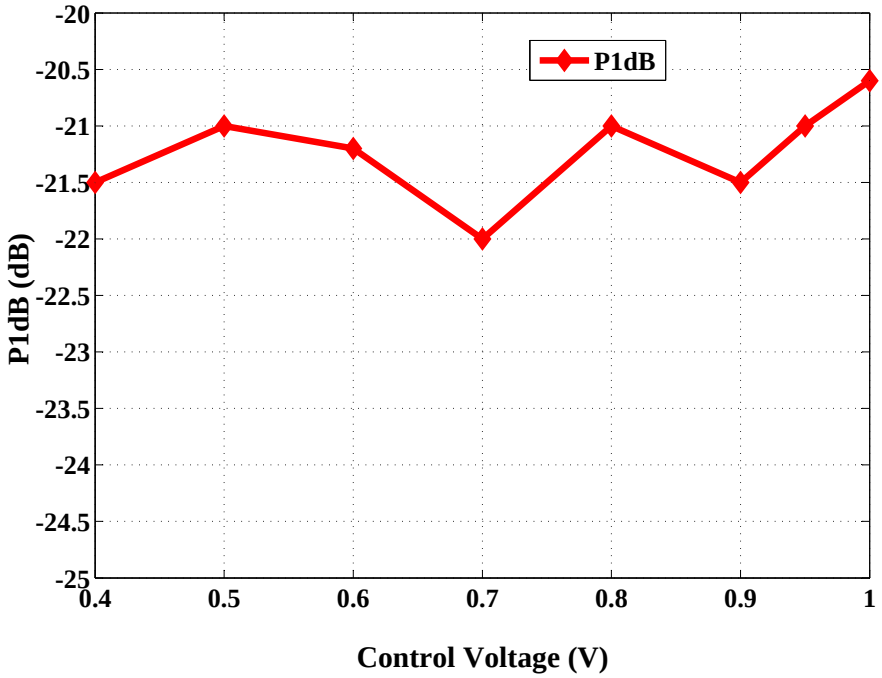


Figure 3.24: Input P_{1dB} versus control voltage.

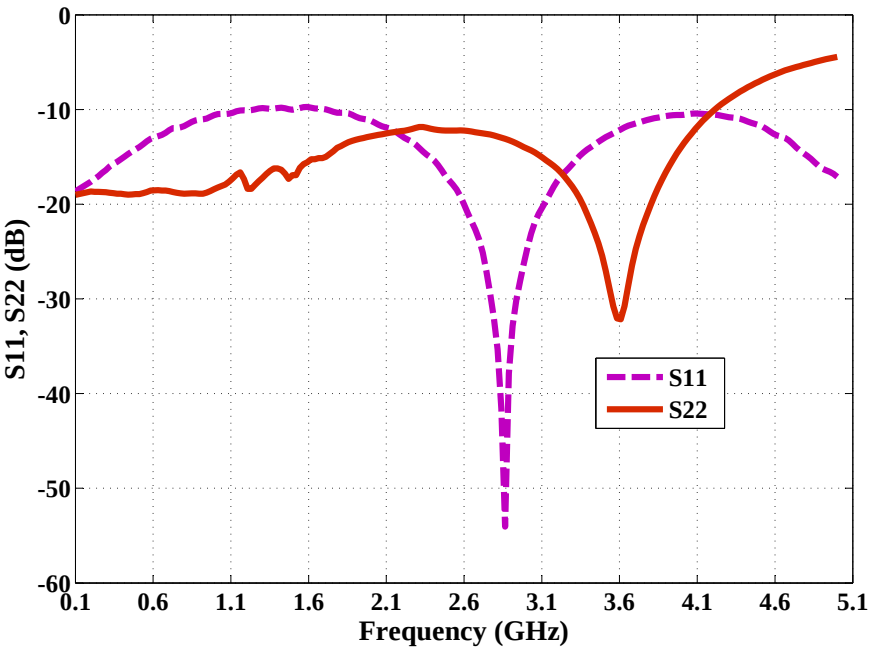


Figure 3.25: Input and output reflection coefficients

3.4 Conclusions

This chapter started with a description of the circuit cell, which is based on two NMOS transistors realizing a pseudo-exponential function. The circuit cell is the basic building

cell of the VGA. The chapter proceeded with the description and optimization procedure of the pseudo-exponential unit-cell-based broadband linear-in-dB VGA circuit to provide maximum gain and large variable gain range. A two-stage cascaded VGA was fabricated and measured to achieve more than 20 dB of tunable gain range. Other circuits required for measurements, such as a differential 100 Ω input power-match circuit and a 100 Ω differential output buffer, are also discussed. The measurements of the VGA with the input match circuit and the output buffer show good agreement with the simulation results. The slight decreases in the VGA bandwidth and the DC gain are partially due to the process variation and unknown parasitic capacitance of the traces in the circuit layout.

In order to further increase the VGA bandwidth, this chapter proceeded with a discussion of another VGA circuit, based on the first VGA but modified by adding an inductive-peaking technique implemented with an active inductor load. The active inductor circuit implementation was discussed and a parameter optimization procedure was described. The active inductor helps to increase the VGA load impedance and to increase the VGA gain. Also a low-threshold-voltage transistor instead of a standard-threshold-voltage transistor was used in the active-load VGA to increase the VGA gain range. Measurements showed good agreement with simulation results. The VGA has an upper -3 dB bandwidth up to 2.1 GHz and provides a variable gain range of 28.5 dB within 1 dB deviation from the ideal linear-in-dB behavior, along with input and the output reflection coefficients of less than -10 dB up to 4.2 GHz. The input-referred P_{1dB} is approximately -22 dBm and IIP3 is -11 dBm. The power consumption of the VGA is 1.1 mW. The active inductor load VGA meets all SKA mid-band frequency application requirements. A comparison of the VGA with other published VGAs is summarized in Table. 3.1.

By careful optimization of the gain and the linear-in-dB range of the VGA, both proposed VGAs achieved the lowest power consumption with a comparable linear-in-dB range demonstrated by recently published VGAs. The VGA with inductive-peaking technique obtained both the maximum gain and the maximum linear-in-dB range with the lowest

Table 3.1: performance of two designed VGAs in this work

Parameters	Specifications	VGA I	VGA II
Power Supply	1.2 V Max.	1.0 V	1.0 V
Process	CMOS 65 nm	CMOS 65 nm	CMOS 65 nm
Upper 3dB freq.	1.4 GHz	1.15 GHz	2.1 GHz
IP1dB	-35 dBm	-25~-32 dBm	-22 dBm
Power consumption	5 mW	1 mW	1.1 mW
Gain range	-10 dB~10 dB	-30~-5 dB (0.7 GHz) -34~-8 dB (1.4 GHz)	-12.5~16 dB
Gain error	<1dB	±2dB	±1dB
Linear-in-dB	Yes	Yes	Yes

power consumption of comparable VGAs.

Chapter 4

Power detection techniques

This chapter starts with a discussion of different power detection methods in Section 4.1 and emphasizes advantages and disadvantages of each method. Three example circuits using MOSFET square-law characteristics in the saturation region as power detectors, which have most advantages over other techniques, are analyzed in Section 4.2. The ultimate goal of this chapter is to identify a power detection method and power detection topology that is capable of achieving the broad bandwidth and high sensitivity required for an SKA mid-frequency receiver application. Section 4.3 summarizes the Chapter.

4.1 Fundamental power detection methods

The power level of an RF signal can be measured by using either the peak or root-mean-square (RMS) values of the signal. Peak detection is suitable for constant-envelope or low peak-to-average ratio signals [55–58]. RMS detection is preferred for high peak-to-average ratio signals, such as noise-dominated signals received by radio telescopes, as they are not sensitive to sporadic large peaks in magnitude. Usually, for receivers, RMS power detection is more useful than peak power detection because RMS power is a consistent and standard way to measure and compare dynamic signals independent of waveform shape. Thermal-based, diode-based and translinear-based detection methods are often used in the design of RMS power detectors [24, 58–63].

4.1.1 Thermal detection

The thermal detection method is widely used in RF measurement equipment [59] because of its broad bandwidth and good accuracy [59, 64]. In this method, heating, which is generated by the measured RF signal as it is absorbed by a resistive component, is compared to heating due to a calibrated DC signal. However, a chip-level realization of such a detector

is complicated in standard CMOS technology by thermal coupling among adjacent circuits through the silicon substrate [24, 63], and it is not suitable for integration with low-cost CMOS processes.

4.1.2 Schottky diode power detection

Schottky diodes are widely employed for power detection due to their nonlinear small-signal characteristics and favorable high-frequency performance and low cost [59, 62]. The relationship between current through a Schottky junction and the voltage across it is

$$I = I_{SAT}\left(e^{\frac{q(V-IR_S)}{nkT}} - 1\right), \tag{4.1}$$

where k is Boltzmann's constant, q is electronic charge, R_s is series resistance, T is absolute temperature, I_{SAT} is saturation current, and n is an ideality factor. All diodes follow this relationship but the Schottky junction can have significantly lower forward voltage at a given forward current compared with other PN junctions. When used as a power detector, the diode exhibits a nearly square-law relationship between I and V over a small range of bias voltages as shown in Fig. 4.1. Beyond that, the relationship is neither square nor linear (crossover region) and hard to define. Therefore, Schottky diode detectors have limited operating range for which their input voltages are less than the PN junction's turn-on voltages [59, 62, 65]. To guarantee proper bias levels, these diodes require elaborate compensation techniques to operate as true RMS detectors [63] over a large signal range. As well, (4.1) shows temperature-dependent performance of the Schottky diode. Moreover, Schottky diodes are not standard components in most CMOS technologies, and therefore custom layouts are needed for their implementation, which in turn requires additional modeling steps as they are not modeled in CMOS design kits.

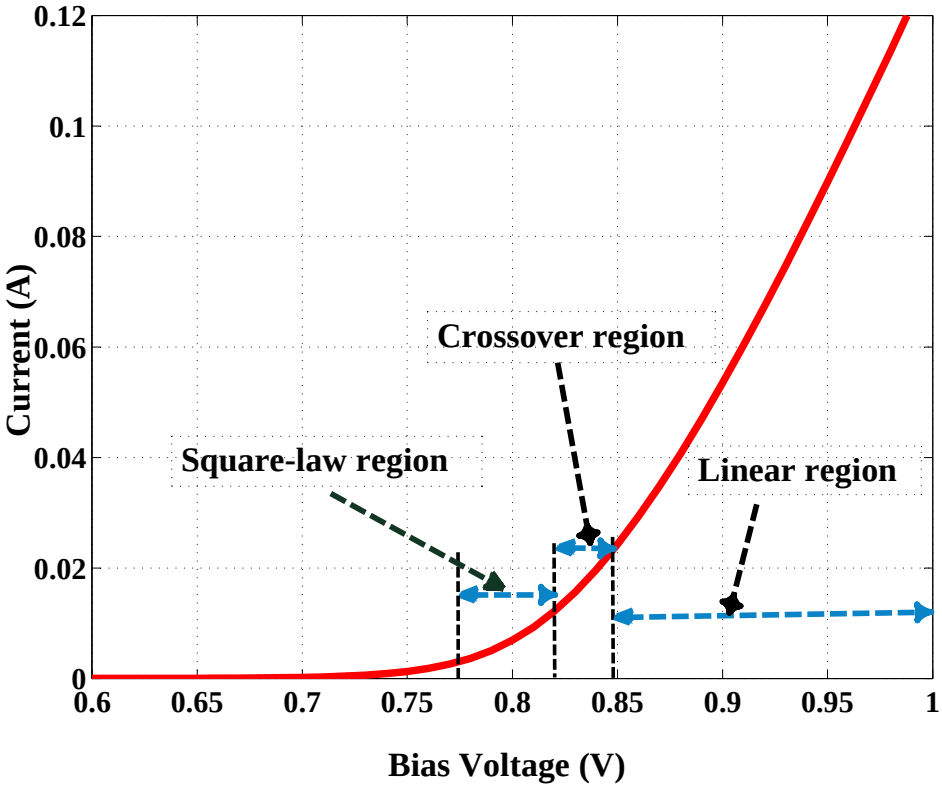


Figure 4.1: Diode forward I-V characteristics and relationship between current and voltage for different regions.

4.1.3 Bipolar transistor power detection

Bipolar transistors are also used as power detectors due to their non-linear collector current behavior with the base-emitter voltage [59, 66]. Similar to Schottky diodes, in bipolar transistors the output current has an approximately square-law relationship with input voltage at low input voltage levels and a linear relationship for high voltage levels. There also exists a crossover region between the two regions.

A widely used bipolar power detection circuit [66] is shown in Fig. 4.2. This circuit is built with a symmetric circuit topology except for its single-ended input ($v_{rf}(t)$). Capacitors C_1 and C_2 filter out the AC signal and power supply noise. The DC biases of Q_1 and Q_2 should be equal so as to cancel any DC offset errors whether the circuit is operated in either AC-coupled or DC-coupled modes. Assuming $v_{rf}(t) = V_{rf}\cos(\omega t)$, at low input

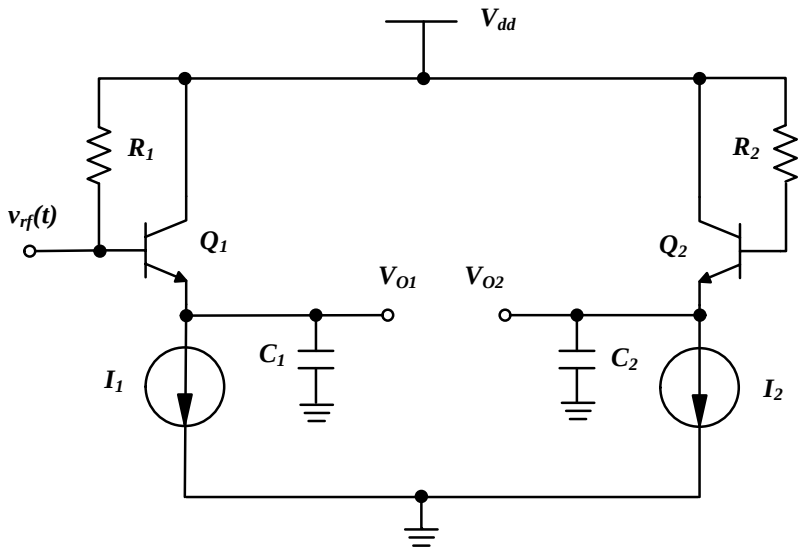


Figure 4.2: Bipolar RF power detector circuit.

power levels where Q_1 is in the square-law region [66],

$$V_o = V_{o1} - V_{o2} \cong \frac{qV_{rf}^2}{4kT}. \tag{4.2}$$

In (4.2), the output voltage is proportional to the square of AC input-signal amplitude. For this circuit, the output is temperature dependent because of the presence of T in (4.2). For high power levels [66]

$$V_o \cong V_{rf} - \frac{kT}{q} \ln \sqrt{\left(2\pi q V_{rf}\right) / \left(kT\right)}. \tag{4.3}$$

This equation shows the basic principles of large-signal detection. The output voltage varies proportionally with the AC input signal except for a nonlinear error term, which depends on signal strength and kT/q.

4.1.4 MOSFET power detection

Recent research has demonstrated that MOSFETs operating in the deep triode region can be used to realize power detectors [27, 67–69]. In addition, the square-law characteristic of

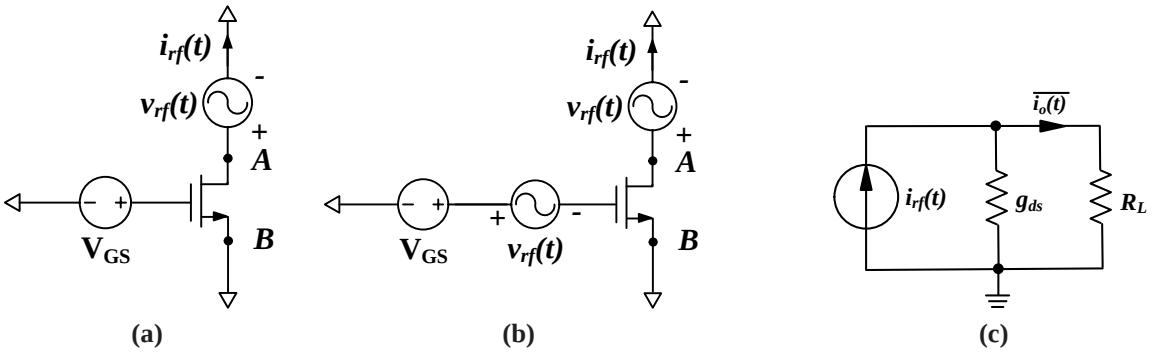


Figure 4.3: The schematic of a MOSFET as a detector in triode. (a) Single-input single-ended output. (b) Differential-input single-ended output (c) Small-signal model.

a MOSFET operating in saturation region can be used for power detection [24, 26, 34, 61, 67, 70] as well. Also, the high channel resistance of transistors operating in the saturation provides the potential for obtaining high detection resolution using the square-law characteristic of MOSFETs. A further description of power detection using MOSFET transistor performance is discussed in Section 4.1.4.1 and 4.1.4.2.

4.1.4.1 MOSFET operating in deep triode region

A simplified schematic of an NMOS transistor in triode used for RF power detection is shown in Fig. 4.3(a). In this circuit, $v_{rf}(t)$ is a zero-average RF signal. If $v_{rf}(t)$ swings in the positive direction, terminals A and B act as transistor drain and source, while if $v_{rf}(t)$ swings in the negative direction, terminals B and A act as transistor drain and source terminals, respectively. Assuming the amplitude of $v_{rf}(t)$ is much less than the overdrive voltage (V_{OD}), the instantaneous current in the transistor is given by $i_{rf}(t)$,

$$i_{rf}(t) = -k_n v_{rf}(t)\left(\frac{W}{L}\right)\left[2V_{OD} - v_{rf}(t)\right],\ v_{rf}(t) \geq 0, \tag{4.4}$$

$$i_{rf}(t) = -k_n |v_{rf}(t)|\left(\frac{W}{L}\right)\left[2\left(V_{OD} - v_t(t)\right) + |v_{rf}(t)|\right],\ v_{rf}(t) < 0, \tag{4.5}$$

where $k_n = (\mu_n C_{ox})/2$, W/L is the width-to-length ratio of the transistor, overdrive voltage $V_{OD} = V_{GS} - V_t$, V_t is transistor threshold voltage and $v_t(t)$ is the change in V_t due to body

effect. When $v_{rf}(t)$ is negative, node B acts as the source and the voltage between the source and the transistor substrate, which needs to connect to ground to avoid forward biasing PN junctions, changes with input signal and affects threshold voltage due to body effect. Threshold voltage variation at negative $v_t(t)$ is

$$v_t(t) = \gamma_{th}\left[\sqrt{|2\phi_F - |v_{rf}(t)||} - \sqrt{2\phi_F}\right]. \tag{4.6}$$

where γ_{th} is body effect coefficient and ϕ_F is the surface potential. The asymmetry in instantaneous current described by (4.4) and (4.5) results in an average current that flows from terminal B to terminal A. If $v_t(t)$ is ignored, the average current is proportional to the mean-square value of the input signal as follows [27]:

$$\overline{i_{rf}(t)} \propto k_n \cdot \left(\frac{W}{L}\right) \overline{\cdot v_{rf}^2(t)}. \tag{4.7}$$

In this situation, the nonlinearity of transistor channel resistance can produce an average current proportional to the amplitude of the RF signal.

In order to further improve power detection gain, differential inputs can be applied as shown in Fig. 4.3(b). Referring to Fig. 4.3(b), when the input signal at terminal A is also applied to the gate but in opposite polarity then the expressions from (4.4) and (4.5) are modified as follows [27]:

$$i_{rf}(t) = -k_n v_{rf}(t)\left(\frac{W}{L}\right)\left[2V_{OD} - 3|v_{rf}(t)|\right],\ v_{rf}(t) \geq 0, \tag{4.8}$$

$$i_{rf}(t) = -k_n|v_{rf}(t)|\left(\frac{W}{L}\right)\left[2\left(V_{OD} - v_t(t)\right) + 3|v_{rf}(t)|\right],\ v_{in}(t) < 0, \tag{4.9}$$

The average power-dependent current is now (4.10)

$$\overline{i_{rf}(t)} \propto 3k_n \cdot \left(\frac{W}{L}\right) \overline{\cdot v_{rf}^2(t)} \tag{4.10}$$

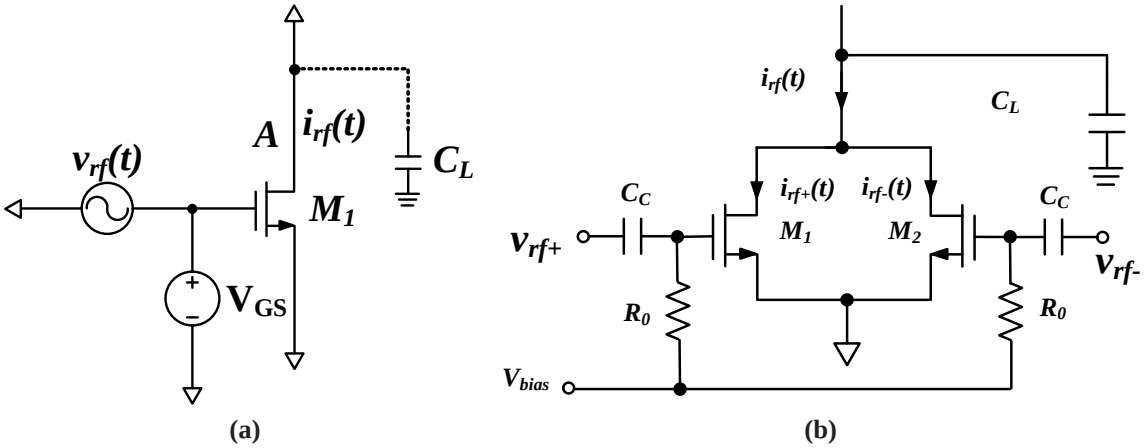


Figure 4.4: Schematic of a MOS transistor as a detector in saturation. (a) Single-input single-output. (b) Differential-input single-output.

representing an improvement over the single-ended case by a factor of 3.

Due to the low channel resistance of a MOSFET in triode, the instantaneous drain current is divided between its channel resistance and the load resistance as shown in Fig. 4.3(c), which is needed to convert output current to voltage. The accuracy of the current divider determines the average output voltage. Due to their low intrinsic gains, defined as the ratio between the output voltage and the input power, associated with low channel resistances, even very small mismatch in transistors can significantly affect the PD performance [27]. In addition, since the output of a PD is a DC signal, PVT-related offsets affect the output and require calibration to remove these offsets to improve the minimum detectable input power of the PD circuits..

4.1.4.2 MOSFET operating in saturation region

The conceptual power detection circuit based on MOSFET square-law characteristics in the saturation region is shown in Fig. 4.4(a). When the input signal $v_{rf}(t)$ is applied to the gate of the transistor, the drain current is expressed as

$$i_{rf}(t) = k_n \left(\frac{W}{L}\right)_1 \left(V_{GS} + v_{rf}(t) - V_t\right)^2, \tag{4.11}$$

where $\left(\frac{W}{L}\right)_1$ is the effective width-to-length ratio of M_1. Assuming $v_{rf}(t) = V_{rf}\cos(\omega t)$ and rearranging (4.11), one obtains

$$i_{rf}(t) = \underbrace{k_n (V_{GS} - V_t)^2 \left(\frac{W}{L}\right)_1}_{\textit{DC bias term}} + \frac{1}{2}\underbrace{k_n V_{rf}^2 \left(\frac{W}{L}\right)_1}_{\textit{Input power term}} - 2k_n V_{rf}\cos(\omega t)\left(\frac{W}{L}\right)_1 + \frac{1}{2}k_n V_{rf}^2 \cos(2\omega t)\left(\frac{W}{L}\right)_1. \tag{4.12}$$

Capacitor C_L at node A in Fig. 4.4(a) filters out most of the RF components in $i_{rf}(t)$ and only DC current, which includes a bias current term and an input power term that is related to the square of V_{rf}, remains. If the DC bias term can be removed from the filtered $i_{rf}(t)$, then the output current only includes the input-power-related term as needed.

The single input circuit can be further extended to a differential input circuit [28, 71] as shown in Fig. 4.4(b). This circuit uses a pair of same-sized NMOS transistors M_1 and M_2 biased in saturation to convert the input signals $v_{rf+}(t)$ and $v_{rf-}(t)$, where $v_{rf+}(t) = -v_{rf-}(t) = \frac{1}{2}V_{rf}\cos(\omega t)$, into currents $i_{rf+}(t)$ and $i_{rf-}(t)$. The total current $i_{rf}(t)$, shown in Fig. 4.4(b), can be expressed as

$$\begin{aligned} i_{rf}(t) &= i_{rf+}(t) + i_{rf-}(t) \\ &= \underbrace{2k_n (V_{bias} - V_t)^2 \left(\frac{W}{L}\right)_{1,2}}_{\textit{DC bias current}} + \underbrace{\frac{1}{2}k_n V_{rf}^2 \left(\frac{W}{L}\right)_{1,2}}_{\textit{Input signal power}} \\ &+ \underbrace{\frac{1}{2}k_n V_{rf}^2 \cos(2\omega t)\left(\frac{W}{L}\right)_{1,2}}_{\textit{Second harmonics}} \end{aligned} \tag{4.13}$$

where the gate-source voltage $V_{GS} = V_{bias}$, and V_t are the gate-bias voltage and the threshold voltage for transistors $M_{1,2}$, respectively. A comparison of (4.13) to (4.12) shows that they have the same terms except that the fundamental components of the input signals is not present in (4.13) since they are out of phase and cancel at the output. After adding C_L at the drain of M_1 and M_2 for filtering out the second harmonic in (4.13), only DC bias current

and a DC term proportional to the input signal power appear at the output:

$$\begin{aligned} i_{rf(DC)}(t) &= 2k_n (V_{bias} - V_t)^2 \left(\frac{W}{L}\right)_{1,2} \\ &+ \underbrace{\frac{1}{2} k_n V_{rf}^2 \left(\frac{W}{L}\right)_{1,2}}_{Input\ signal\ power} \end{aligned} \tag{4.14}$$

Comparing the two circuits in Fig. 4.4, C_L is reduced for the differential circuit because it only filters the second harmonic signal at the output instead of the fundamental and second harmonics signals in Fig. 4.4(a).

The power detection circuit using MOSFETs operating in saturation overcomes the input range limitation for diodes and bipolar transistors. The input range of a MOSFET PD operating in saturation is determined by the point where the MOSFETs enter triode when input power is high and by circuit noise and an offset due to mismatch between the PD transistors when input power is low. In contrast to power detection circuits with MOSFETs working in the triode region, a MOSFET in saturation does not suffer from low channel resistance and overcomes the disadvantages of load-dependent performance present in [27] and described above.

4.2 Square-law MOSFET power detector examples

Having discussed different ways of detecting power and determining that using MOSFET square-law characteristics when the transistors operate in saturation, this section continues with a discussion of power detector circuits based on this approach.

4.2.1 Single input differential output power detector

A very simple single-ended input, differential-output circuit using MOSFET square-law characteristics in saturation was proposed in [24, 34] and is shown in Fig. 4.5. By sizing M_1 and M_2 the same, using R_L to convert current to voltage, and taking a differential output

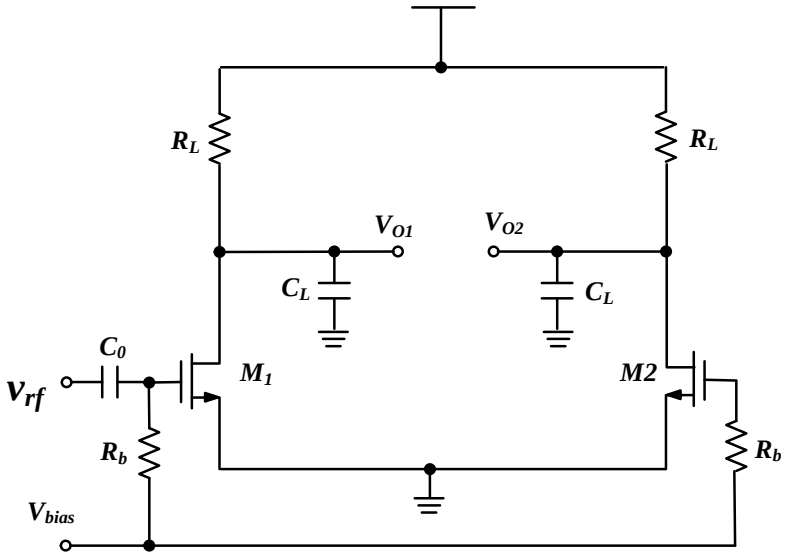


Figure 4.5: Differential output square-law MOSFET power detector.

at V_{o1} and V_{o2}, the output voltage generated by the circuit is

$$v_{out}(t) = V_{o2} - V_{o1} = \underbrace{\frac{1}{2}k_n\left(\frac{W}{L}\right)R_L}_{\textit{Power detection gain}} \times V_{rf}^2. \tag{4.15}$$

Relative to (4.14), the DC bias term is removed, and the output voltage is proportional to the input signal power. The advantage of this circuit is that it is very simple and is expected to have low power consumption and broad bandwidth. However, there are some limitations:

- The topology is not directly suitable for use in a differential input circuit.
- Large capacitance C_L is needed to remove the RF fundamental signal, second harmonic signals, and power supply noise at the output. For better filtering, larger chip area will be occupied by C_L.
- Mismatches between M_1 and M_2 and the two load resistors R_L can cause output DC offset. The offset limits PD minimum detection power because the power detector output is also a DC signal.

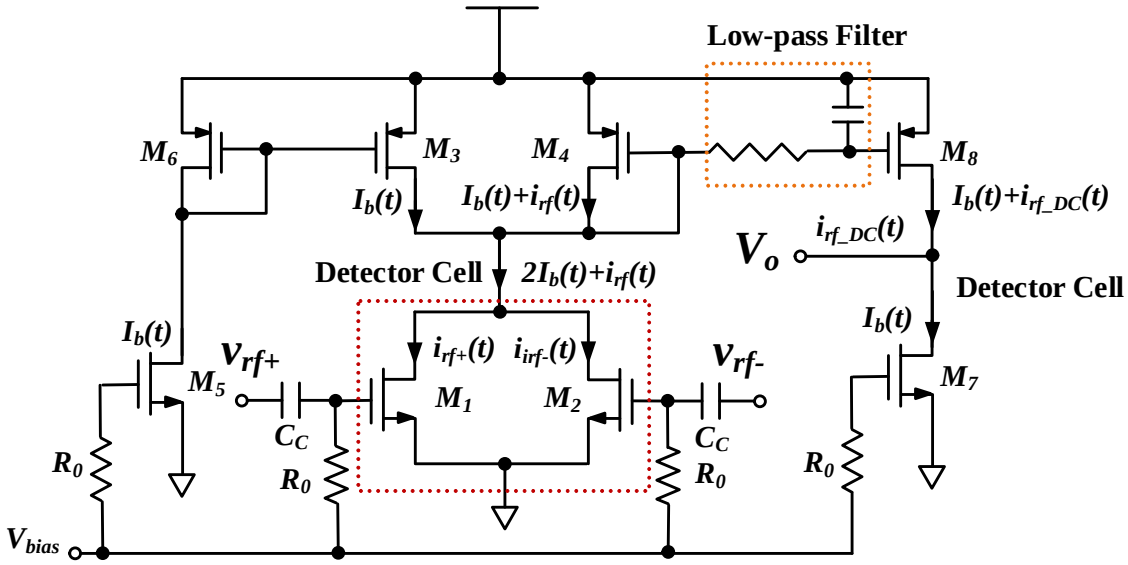


Figure 4.6: Schematic of the differential power detector.

4.2.2 Differential input single-ended output power detector

An example of a differential input, single-ended output power detection circuit using MOSFET square-law characteristics is shown in Fig. 4.6 [28]. When NMOS transistors M_1, M_2, M_5 and M_7 and PMOS transistors M_3, M_4, M_6 and M_8 are sized properly, the output voltage V_o has a square-law relationship with input signal amplitude. The easiest design approach is to size M_1, M_2, M_5 and M_7 the same and M_3, M_4, M_6 and M_8 the same. The currents flowing through each transistor are as labeled in Fig. 4.6. $I_b(t)$ is the DC bias current for transistors M_1, M_2, M_5 and M_7, $i_{rf+}(t)$ and $i_{rf-}(t)$ are currents through M_1 and M_2, which include DC bias current $I_b(t)$ and RF signal generated current $i_{rf}(t)$. A low-pass filter removes the AC signal components present in $i_{rf}(t)$, which includes both a fundamental frequency signal and a second harmonic signal, to produce a DC current representing input power:

$$i_{rf-DC}(t) = \tfrac{1}{2}k_n V_{rf}^2 \left(\tfrac{W}{L}\right)_{1,2,5,7}. \tag{4.16}$$

The limitations of this circuit are:

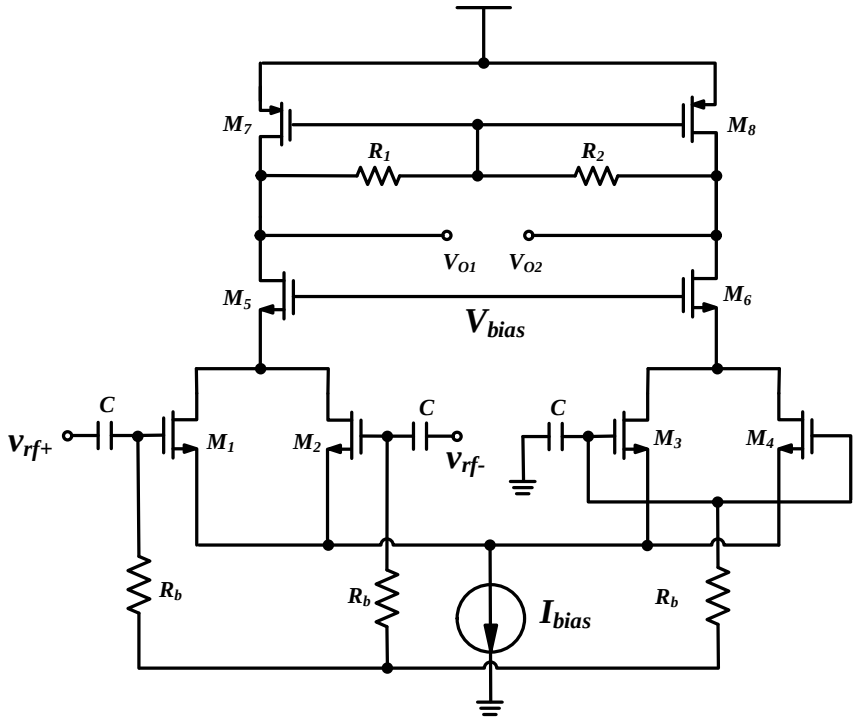


Figure 4.7: Schematic of differential-input, differential-output power detector.

- Differential input and single-ended output, which does not directly suit a differential input and differential output application.
- Power supply noise affects output through capacitance in the low-pass filter and gate-drain capacitance of M_8, $C_{gd,M8}$.
- Mismatches between same-sized transistors (four transistors with same size) are hard to compensate, which limits PD minimum detection power.

4.2.3 Differential-input differential-output power detector

Recently, a differential-input, differential-output power detector was presented in [71] and shown in Fig. 4.7. In Fig. 4.7, by sizing M_{1-4} the same, M_7 and M_8 the same, M_5 and M_6 the same, and taking differential output V_o at V_{o1} and V_{o2},

$$V_o = V_{o2} - V_{o1} = \frac{k_n}{g_{m7,8}} V_{rf}^2 \left(\frac{W}{L}\right)_{1-4}. \tag{4.17}$$

V_o has a quadratic relationship with input signal amplitude, where $g_{m7,8}$ are transconductances of M_7 and M_8. The limitations of this circuit are:

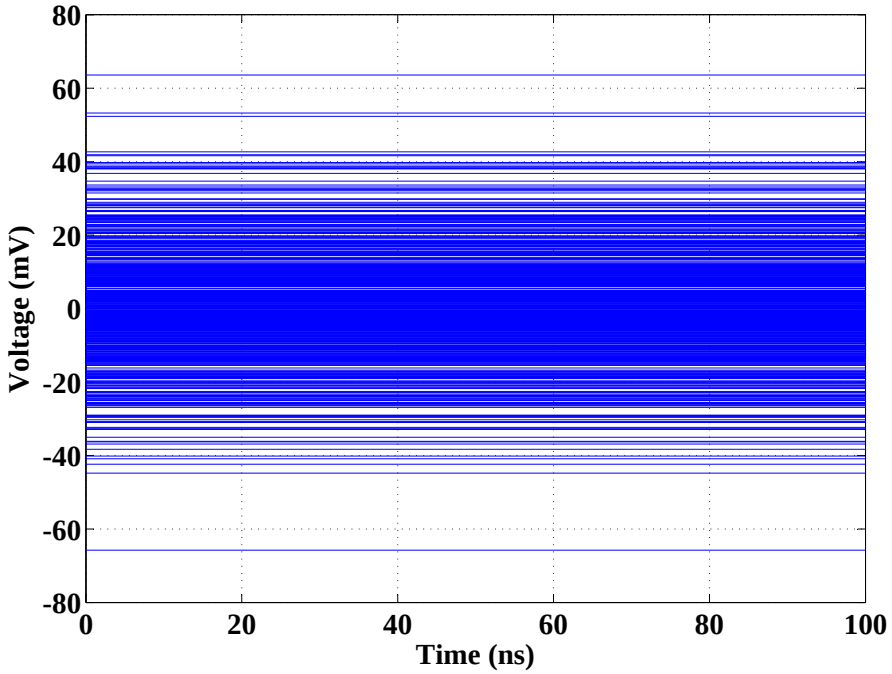
- High power supply voltage is needed because of the cascode topology and current tail transistor to implement I_{bias}. The circuit requires four transistors between the power supply and ground, which is not desirable for low voltage applications.

- The gain of this circuit is small due to the low impedance of the diode-connected load built with M_7 and M_8. It needs an additional amplifier to amplify the output signal to measurable levels when the input power levels are low. The maximum detection power is also limited by the maximum output voltage, which may cause input transistors operate in triode region.The output voltage is the power supply voltage minus the threshold voltage of the diode-connected load.

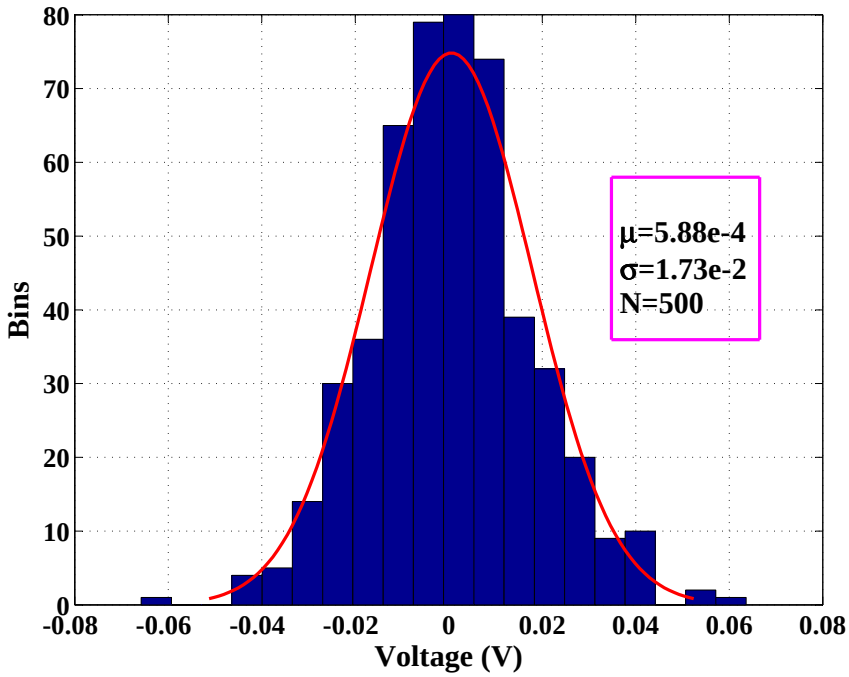
- The second harmonic signals appear at the power detector output limiting the sensitivity of the PD. Only the fundamental signal is canceled at V_{o1} due to 180 degree phase shift between differential input signals while second harmonic signals cannot be canceled as they are in-phase and appear at the power detector output.

- Mismatches between equally sized transistors are the main factors limiting the sensitivity of the power detector.

To demonstrate the effects of mismatches and second harmonics at the power detector output, the results of Monte Carlo simulation (500 runs) based on TSMC 65nm CMOS technology are presented in Fig. 4.8(a) and Fig. 4.8(b). Fig. 4.8(a) shows transient output voltages of each run and Fig. 4.8(b) shows the histogram of offset voltage distributions. The mean value is 0.6 mV, which is the expected mismatch voltage, and with standard deviation of 17.3 mV, which means 68.3% of the mismatch voltage is within this range. Thus, it is very hard to have a very high resolution PD with such a big mismatch voltage without mismatch compensation.



(a) Power detector output voltages (500 runs).



(b) Histogram of Monte carlo simulation (x axis is power detector output voltages with no input power applied, and y axis is the bin numbers).

Figure 4.8: Monte Carlo simulation of the power detector circuit in Fig. 4.7.

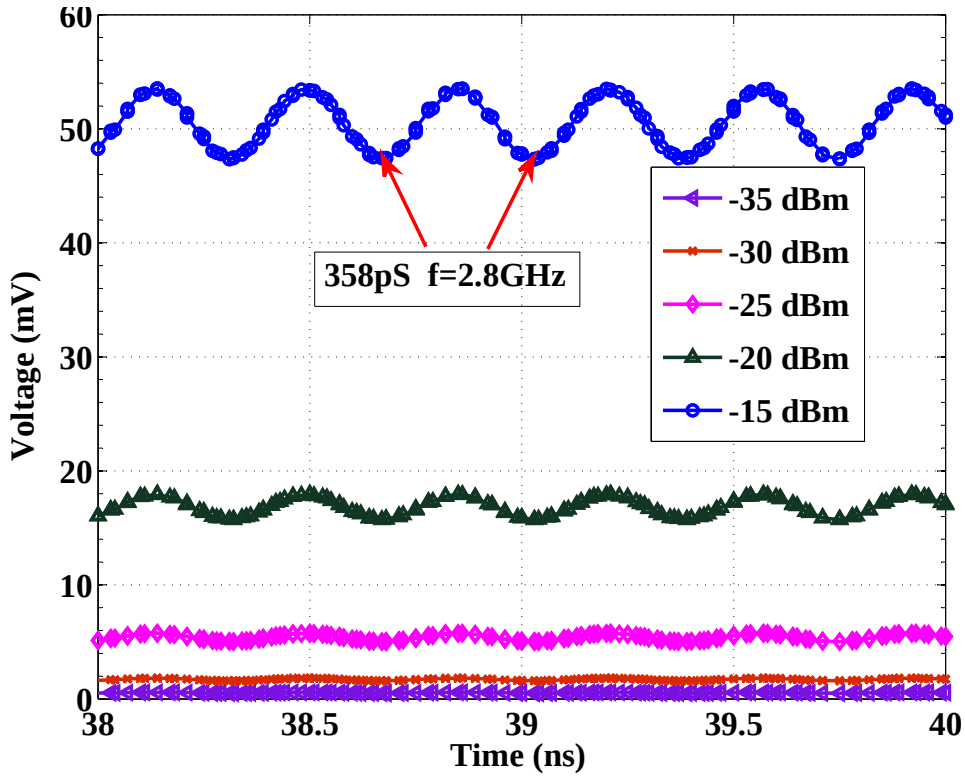
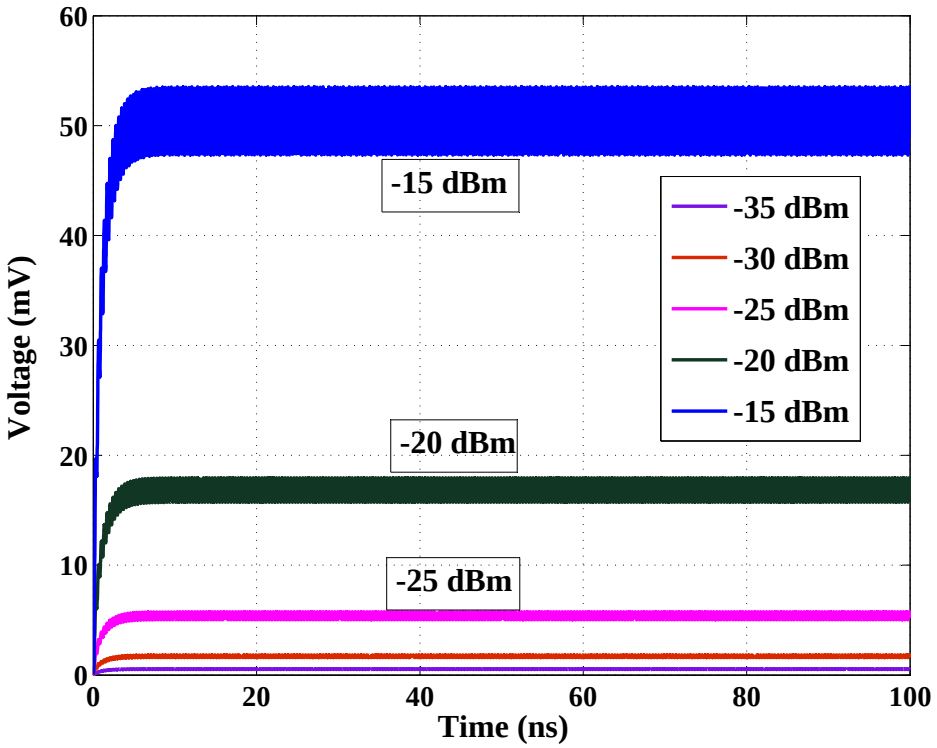


Figure 4.9: Second harmonics at different input power levels (-35 dBm, -32 dBm, -29 dBm, -26 dBm,-23 dBm, -20 dBm) at 1.4 GHz.

The second harmonic signal at the PD output is shown in Fig. 4.9 for 5 different input power levels. The output peak-to-peak voltage of the second harmonic is 6 mV for -15 dBm input power. Compared to 50 mV DC output voltage, the second harmonic is as large as 10% of the output signal. This noise signal can further limit the PD sensitivity. All these limitations make it hard to use this detector for detection of very low power inputs. The PD output voltages at different input power levels are also simulated and shown in Fig. 4.10 for future comparison with the proposed PD circuit that is discussed next in Chapter 5.

4.3 Conclusions

This chapter started with the description of fundamental power detection methods, which include thermal detection, diode detection, bipolar transistor detection, MOSFETs operating in the deep triode region, and MOSFETs operating in the saturation region. Thermal



(a)

Figure 4.10: PD output at different input power levels (-35 dBm, -32 dBm, -29 dBm, -26 dBm,-23 dBm, -20 dBm) at 1.4 GHz.

detection methods are not suitable in CMOS realizations due to the high-temperature conduction of the silicon substrate, while diode and bipolar transistor detectors are strongly temperature dependent and exhibit limited detection range.

Since a MOSFET operating in the deep triode region has low channel resistance, the output current, which represents the input power, is divided between MOSFET channel resistance and the load resistance. The accuracy of the current divider determines the average output voltage. Due to their low intrinsic gains, defined as the ratio between the output voltage and the input power, associated with low channel resistances, even very small mismatch in transistors can significantly affect the PD performance [27]. In addition, since the output of a PD is a DC signal, PVT-related offsets affect the output and require calibration to remove these offsets to improve the sensitivity of the PDs.

MOSFETs operating in the saturation region overcome the input range limitation of

diodes and bipolar transistors, do not suffer from low channel resistance, and overcome the disadvantages of load-dependent performance of MOSFETs working in the deep triode region. The MOSFET square-law power detection technique in saturation is identified as the most suitable for the desired application.

Three power detector circuits, which include one single-input differential-output circuit, one differential-input single-output circuit, and a differential-input differential-output cascode circuit, with MOSFETs in the square-law region are demonstrated in Section 4.2. These circuits suffer sensitivity limitations due to transistor mismatches. Noise from the power supply, which cannot be filtered out, makes the PD sensitivity even worse in the differential-input single-output circuit. Furthermore, these two circuits cannot be directly used for a differential-input differential-output application, which is the SKA receiver requirement. The cascode PD circuit suffers from high power supply voltage limitations, and large second harmonic components at the output, which limits the PD sensitivity.

To the author's knowledge, PD circuits published so far could not meet the SKA requirements, which include minimum detection power of -35 dBm, operation in the SKA mid-frequency range and power consumption less than 2 mW. A new PD circuit using MOSFET operating in the saturation region that can meet the requirements is proposed next in Chapter 5.

Chapter 5

Design of self-calibrated power detector circuit

In this chapter, an improved differential CMOS power detector topology based on the MOS transistor's square-law characteristic in the saturation region is presented in Section 5.1. To improve the PD sensitivity by compensating mismatches of components, mismatches between components of the proposed PD circuit are analyzed in Section 5.2. In Section 5.3, an analog self-calibration loop is proposed to compensate circuit component mismatches due to PVT variations. Section 5.4 describes all the circuits used in the calibrated PD. Experimental verification of the PD operation is demonstrated in Section 5.5. Section 5.6 summarizes the chapter.

5.1 Proposed differential power detector circuit

A CMOS PD circuit with differential-input differential-output using MOSFET square-law characteristic [71] was discussed in Section 4.2.3. This circuit needs high power supply voltage, has low gain and low sensitivity due to transistor mismatches and uncanceled second harmonic components of the input signal. All these limit its application to high sensitivity power detection.

To overcome the limitations of this circuit and make it suitable for the use in an SKA receiver, an improved differential CMOS power detector topology using MOSFET transistor square-law characteristics is proposed in this work as depicted in Fig. 5.1. This power detector is composed of the main power detection circuit and a duplicate circuit. The main power detection circuit consists of M_1, M_2, M_5, R_L and C_L, where C_L and R_L filter out the RF signals and convert current to voltage at node V_{O1}, and M_5 works as a current source, reducing voltage drop across R_L and thereby increasing PD output swing, which determines PD detection range. The techniques used in the proposed PD to overcome the limitations of the circuit presented by [71] are summarized as:

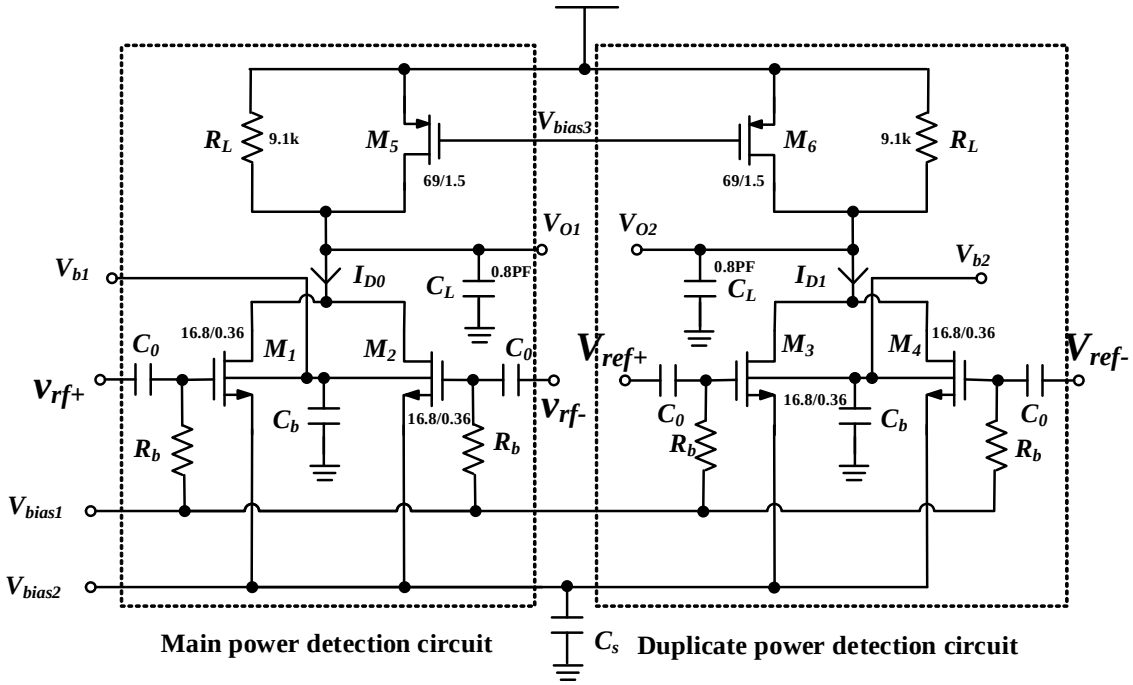


Figure 5.1: Differential power detector schematic.

- Cascode transistors are removed for low supply voltage application.
- PD loads are formed with current sources, $M_{5,6}$ paralleling with load resistors, R_L, to increase the PD gain and reduce its noise while increasing the upper limit of the detection range as well, due to lower voltage drop across R_L than across the diode-connected load in [71].
- Low-pass filters at the outputs V_{o1} and V_{o2}, formed by C_L's and R_L's, filter out the uncanceled fundamental component and second harmonic component of the input signal.
- DC bias voltages instead of current sources used at the sources of M_{1-4}, provide reverse biasing voltage between bulk terminals, which are connected to capacitors C_b instead of sources of transistors M_{1-4}. This permits mismatch compensation by using body effect of the input transistors. The detailed calibration technique is discussed in Section 5.3.

- Capacitance C_s at the source of M_{1-4}, shown in Fig. 5.1, is added to remove the second harmonic components at the sources of M_{1-4}, which, when not removed and coupled through gate-source capacitances of M_3 and M_4, may cause power-dependent fluctuations at the PD output.

In Fig. 5.1, when a differential input signal $V_{rf}\cos(\omega t)$ is applied at the gate terminals of M_1 and M_2, the total current flowing through the load formed by R_L and M_5 is I_{D0}:

$$\begin{aligned} I_{D0} &= 2k_n\left(\frac{W}{L}\right)_{1,2}(V_{GS}-V_t)^2 \\ &+ \underbrace{\frac{1}{4}k_n\left(\frac{W}{L}\right)_{1,2}\times V_{rf}^2}_{\text{Input signal power term}} \end{aligned} \tag{5.1}$$

where $V_{GS}=V_{bias1}-V_{bias2}$, and V_t is threshold voltage of transistors M_{1-4}. The second-order harmonic and the uncanceled fundamental frequency signal, which is caused by the mismatch between M_1 and M_2, are largely removed by C_L and R_L, which form a low-pass filter at the PD output. To remove the DC bias component in I_{D0}, the duplicate PD circuit, which consists of transistors M_3, M_4, M_6, R_L and C_L, is biased at the same condition as the main power detection circuit, and ideally generates the same DC bias component, I_{D1}, in the current flowing through M_3, M_4 as M_1, M_2, so that

$$I_{D1} = 2k_n\left(\frac{W}{L}\right)_{3,4}(V_{GS}-V_t)^2. \tag{5.2}$$

By measuring the differential output voltage, V_{out}, across R_L,

$$\begin{aligned} V_{out} &= V_{O2}-V_{O1} \\ &= \underbrace{\frac{1}{4}k_nR_L\left(\frac{W}{L}\right)_{1,2}}_{\xi_p(\textit{power detection gain})}\times V_{rf}^2, \end{aligned} \tag{5.3}$$

the DC bias components cancel out and the output is only dependent on V_{rf}^2, which is pro-

portional to the square of input signal amplitude. In the ideal situation, when all transistors in the main PD circuit and its duplicate are perfectly matched and noise generated in the circuit is low, the output voltage is exactly related to the input power as in (5.3). In practice, some amount of mismatch due to PVT variations is inevitable and needs to be addressed in order to increase the sensitivity and dynamic range of the PD. In this work, transistor body effect is used for circuit component mismatch compensation by modification of bulk voltages of transistors M_{1-4} to adjust threshold voltages and achieve zero voltage at the PD output after calibration.

5.2 Differential PD mismatch analysis

The dynamic range of the PD circuit described above is defined from MOSFETs entering triode when input power is high, and from the noise and an offset due to mismatch between the PD transistors when input power is low. In order to improve the sensitivity and maximize the dynamic range, the mismatches of the differential PD are analyzed to provide design insight.

First, mismatches between M_1 and M_2 are considered. In order to simplify the analysis, only threshold voltage mismatch, which is the dominant part of overall transistor mismatch, is considered. Transistor size mismatches due to manufacturing tolerances are ignored since large transistors are selected in this work. Assuming that the threshold voltages of M_1 and M_2 are not the same and are represented by V_{t1} and V_{t2}, then the currents flowing through these transistors are represented by

$$I_{ds1}^{'} = k_n \left(\frac{W}{L}\right)_{1,2} \left(V_{GS} + v_{rf+} - V_{t1}\right)^2 \tag{5.4}$$

and

$$I_{ds2}^{'} = k_n \left(\frac{W}{L}\right)_{1,2} \left(V_{GS} + v_{rf-} - V_{t2}\right)^2. \tag{5.5}$$

Similarly to (5.1), these two currents result in the total current $I_{DS}^{'} = I_{ds1}^{'} + I_{ds2}^{'}$, or

$$
\begin{aligned}
I_{DS}^{'} &= k_n \left(\frac{W}{L}\right)_{1,2} \left[(V_{GS}-V_{t1})^2 + (V_{GS}-V_{t2})^2\right] \\
&+ \frac{1}{4} k_n \left(\frac{W}{L}\right)_{1,2} V_{rf}^2 \\
&+ \frac{1}{4} k_n \left(\frac{W}{L}\right)_{1,2} V_{rf}^2 \cos(2\omega t) \\
&+ \underbrace{k_n \left(\frac{W}{L}\right)_{1,2} (V_{t2}-V_{t1}) V_{rf} \cos(\omega t)}_{\text{Fundemental component}}
\end{aligned} \tag{5.6}
$$

where V_{GS} is the gate-source voltage of transistors M_1 and M_2. The comparison of (5.6) to (5.1) shows that the mismatches in M_1 and M_2 result in the appearance of the fundamental component of the input signal at the output. Capacitor C_L at the output node filters out this signal and the second harmonic signals, and as in (5.1) only the DC current $I_{DS(DC)}^{'}$ component remains

$$
\begin{aligned}
I_{DS(DC)}^{'} &= k_n \left(\frac{W}{L}\right)_{1,2} \left[(V_{GS}-V_{t1})^2 + (V_{GS}-V_{t2})^2\right] \\
&+ \frac{1}{4} k_n \left(\frac{W}{L}\right)_{1,2} V_{rf}^2.
\end{aligned} \tag{5.7}
$$

The first term in (5.7) is the DC bias current that can be rearranged to resemble (5.1) by introducing an equivalent threshold voltage V_{T1} discussed in Appendix A.

$$
I_{DS(DC)}^{'} = k_n \left(\frac{W}{L}\right)_{1,2} \left[(V_{GS}-V_{T1})^2\right] + \frac{1}{4} k_n \left(\frac{W}{L}\right)_{1,2} V_{rf}^2. \tag{5.8}
$$

$$
V_{T1} = V_{GS} - \sqrt{V_{GS}^2 - V_{GS}(V_{t1}+V_{t2}) + \frac{1}{2}\left(V_{t1}^2 + V_{t2}^2\right)}. \tag{5.9}
$$

Identical analysis applies to M_3 and M_4 for the duplicate PD and the DC current through

that circuit is

$$I''_{DS(DC)} = \quad k_n \left(\tfrac{W}{L}\right)_{3,4} \left[(V_{GS} - V_{t3})^2 + (V_{GS} - V_{t4})^2\right] \tag{5.10}$$

and can be rearranged to resemble (5.1) by introducing an equivalent threshold voltage V_{T2}

$$I''_{DS(DC)} = k_n \left(\frac{W}{L}\right)_{3,4} \left[(V_{GS} - V_{T2})^2\right] \tag{5.11}$$

$$V_{T2} = V_{GS} - \sqrt{V_{GS}^2 - V_{GS}(V_{t3} + V_{t4}) + \frac{1}{2}\left(V_{t3}^2 + V_{t4}^2\right)}. \tag{5.12}$$

Mismatch between V_{T1} and V_{T2} can be adjusted by adjusting the bulk voltages, V_{b1} and V_{b2}, of M_{1-4}. There are also likely mismatches between M_5 and M_6 and the two R_L's. The proposed calibration technique in Section 5.3 is designed to set $V_{O1} \approx V_{O2}$ by adjusting the bulk voltages of V_{b1} and V_{b2}, thus correcting offsets due to all components in both the main and the duplicate circuits.

A comparison of the output voltage of the proposed circuit and the circuit in [71] is shown in Fig. 5.2. The simulation results show an improvement of the PD gain and reduction of the second harmonics in the proposed PD. The proposed PD output is very clean even at high input power level. Monte carlo simulation results of the proposed circuit are shown in Fig. 5.3. The standard deviation of the PD output mismatch voltage is 10.9 mV, which can be compensated by the calibration that is discussed in the following section.

5.3 Self-calibrated system for power detector

To compensate the offset at the PD differential output and to improve its sensitivity, this work proposes a calibration process that uses MOSFET source-bulk voltage, V_{SB}, to tune

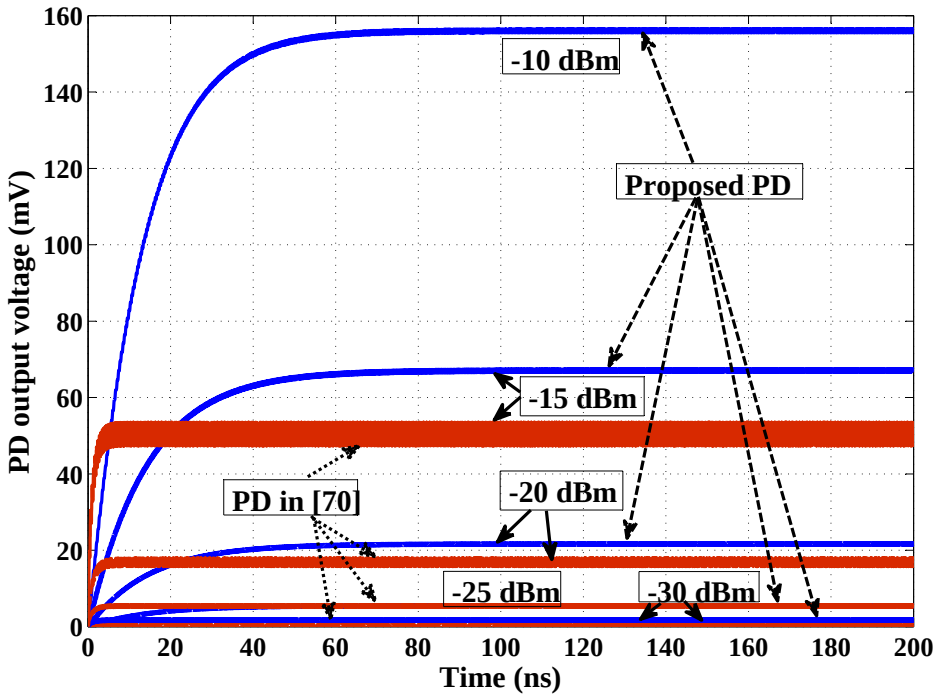


Figure 5.2: Simulation results of power detector output voltage at different input power levels (-30 dBm, -25 dBm,-20 dBm, -15 dBm,-10 dBm). The arrow lines point to the curves representing performances of circuit in [70] and proposed power detector characteristics with same sized input transistors.

MOSFET threshold voltages by making use of the well-known dependence of V_t on V_{SB}

$$V_t = V_{T0} + \gamma_{th}\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right), \tag{5.13}$$

where γ_{th} denotes the body effect coefficient, ϕ_F is Fermi voltage, and V_{T0} is the intrinsic threshold voltage. The proposed calibrated PD-circuit block diagram is illustrated in Fig. 5.4. It is formed by a differential-input power-match amplifier $Amp0$, a PD circuit from Fig. 5.1, a high-gain amplifier $Amp1$, and two sets of switches S_1 and S_2.

During the calibration mode, the switch set S_1 is turned OFF, cutting off the RF signal from the PD, and the switch set S_2 is turned ON connecting the amplifier $Amp1$ outputs to V_{b1} and V_{b2}, which are bulk terminals of $M_{1,2}$ and $M_{3,4}$ respectively as labeled in Fig. 5.1. Any unwanted DC voltage difference at nodes V_{O1} and V_{O2} due to mismatches between the main PD circuit and the duplicate PD circuit is amplified by $Amp1$ and fed back to the bulk

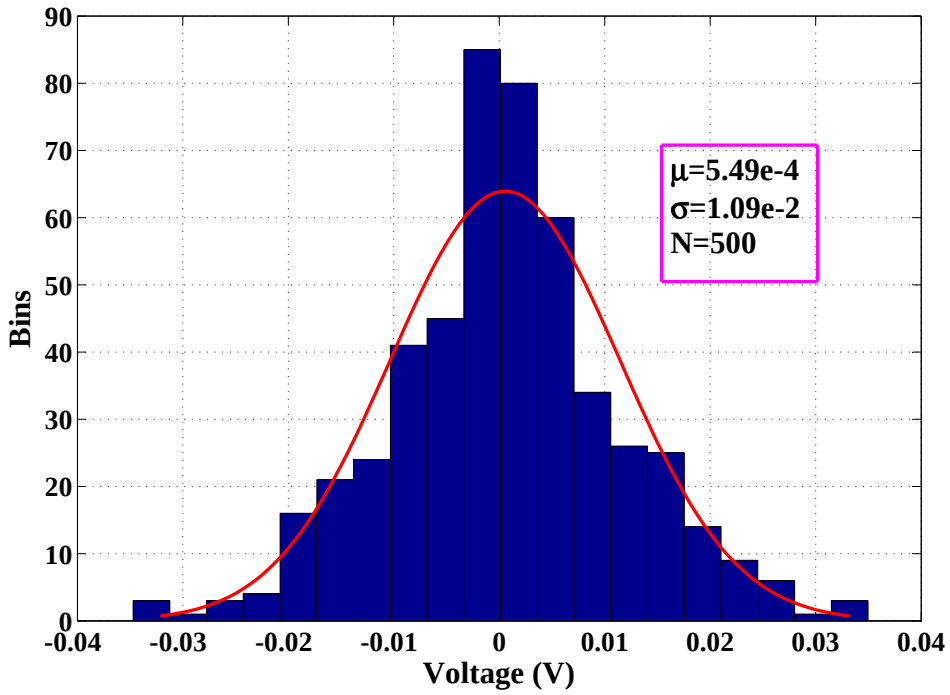


Figure 5.3: Histogram of Monte carlo simulation (x axis is power detector output voltages with no input power, and y axis variable is numbers located at each voltage).

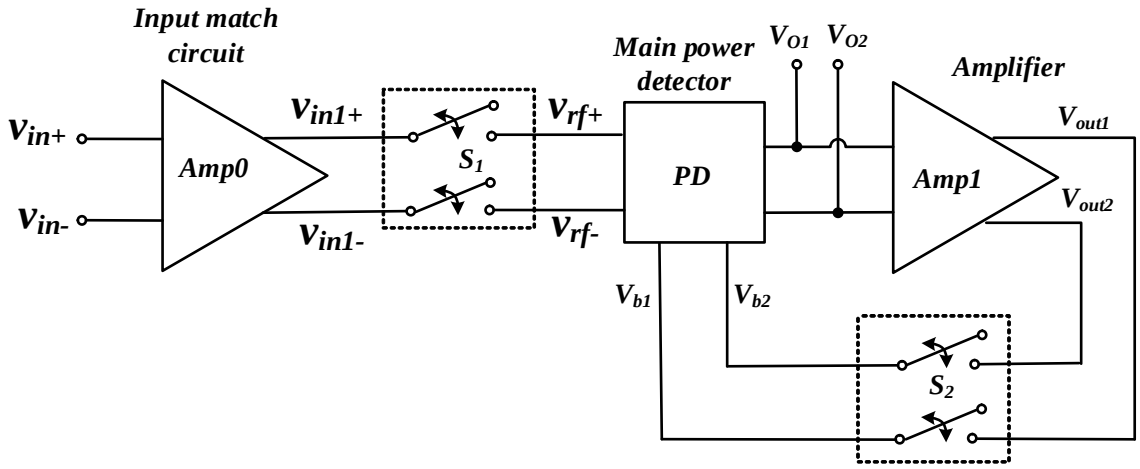


Figure 5.4: Self-calibrated-PD circuit block diagram.

terminals of $M_{1,2}$ and $M_{3,4}$ so as to force the differential voltage V_{O1} - V_{O2} to zero. Once calibration is completed, the switch set S_2 turns OFF to open the feedback loop and the switch set S_1 turns ON to connect the amplified input signals to the PD input. Note that the *Amp*1 output voltage is selected based on Monte Carlo simulations to avoid forward

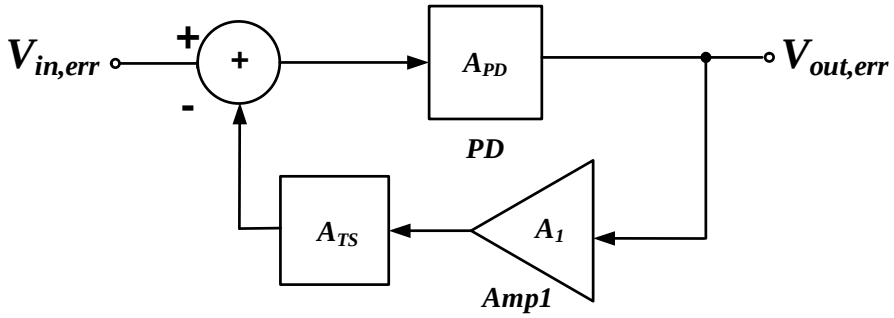


Figure 5.5: PD calibration block diagram.

biasing the bulk-to-source PN junctions of the PD input transistors for all process corners and all possible operating conditions.

Compared with the offset cancellation method in [27], the calibration method described here is expected to achieve higher sensitivity as the inevitable charges injected by the switches S_2 appear at the bulks of the PD input transistors instead of their gates as in [27]. Since the gain from bulk to drain of a MOSFET is much lower than the gain from gate to drain, the charge injection effect is reduced. Also large capacitors C_b at the bulk terminals reduce the charge injection problems further without affecting the PD bandwidth.

5.3.1 PD sensitivity

PD sensitivity, which is defined as the minimum power level the PD can detect, is limited by calibration accuracy of the system, PD noise, switch charge injection, and the PD calibration rate.

5.3.1.1 PD calibration accuracy

The PD calibration accuracy is mostly dependent on the loop gain of the calibration system, which is shown in a simplified form in Fig. 5.5. In this diagram $V_{in,err}$ represents the input-referred error due to all mismatches in the PD circuit and $V_{out,err}$ represents the output DC error after calibration. Blocks PD and $Amp1$ represent the same blocks as in Fig. 5.4. The block A_{TS} represents the equivalent voltage gain between the source-bulk voltage and

threshold voltage of the PD input transistors M_{1-4}. From (5.13), this technology and bias-dependent parameter is expressed as:

$$A_{TS} = \frac{dV_t}{dV_{SB}} = \frac{1}{2}\frac{\gamma_{th}}{\sqrt{|2\phi_F + V_{SB}|}}. \tag{5.14}$$

The closed-loop transfer function of the calibration system is

$$\frac{V_{out,err}}{V_{in,err}} = \frac{A_{PD}}{1 + A_{PD}A_1A_{TS}}, \tag{5.15}$$

where A_{PD} is the open-loop DC voltage gain of the PD, A_1 is the DC voltage gain of $Amp1$, and $A_{PD}A_1A_{TS}$ is the loop gain. Since the loop gain is much larger than 1, the closed-loop gain can be expressed as

$$\frac{V_{out,err}}{V_{in,err}} \approx \frac{1}{A_1A_{TS}}. \tag{5.16}$$

When calibration completes, the equivalent error in the differential RF input signal amplitude can be expressed as

$$V_{err} = \sqrt{\frac{V_{out,err}}{\xi_p}} = \sqrt{\frac{V_{in,err}}{\xi_p A_1 A_{TS}}}, \tag{5.17}$$

where ξ_p is the PD detection factor as defined in (5.3). From (5.17), V_{err}^2 is inversely proportional to A_{TS}, A_1 and ξ_p. Since A_{TS} is mainly determined by the process parameters as in (5.14), A_1 and ξ_p are the main parameters that control the calibration accuracy of the PD and should be made large. As in (5.3), ξ_p can be increased by increasing load resistor R_L and by widening M_{1-4} as seen from (5.3). These however limit the maximum detection power due to the large voltage drop across R_L, and potentially decrease the detection range. Widening M_{1-4} may increase PD power consumption, and decrease detection power as well because of the large voltage drop across R_L. Therefore, the PD calibration accuracy, power consumption, and detection range need to be traded off by choosing the proper input transistor sizes and the load resistance R_L. Another effective way for increasing

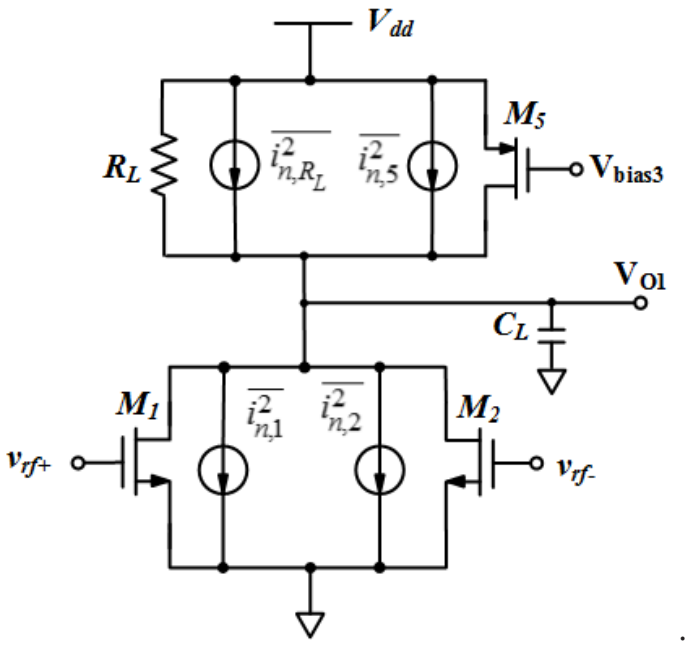


Figure 5.6: Half PD circuit with noise sources.

the calibration accuracy is by increasing A_1, the gain of $Amp1$, to increase the loop gain. According to the simulation, for a $V_{in,err} = 5\,\text{mV}$ before calibration and with $A_1 = 70\,\text{dB}$, representing the worst case gain, V^2_{err} is approximately equivalent to -64 dBm, referenced to 100 Ω differential input impedance, after calibration. This accuracy is good enough for the SKA application.

5.3.1.2 PD noise

In order to estimate the effect of noise on the PD sensitivity, the main power detector circuit in Fig. 5.1, with its noise sources, as shown in Fig. 5.6 , is considered. $\overline{i^2_{n1}}$, $\overline{i^2_{n2}}$, $\overline{i^2_{n5}}$ and $\overline{i^2_{n,RL}}$ represent mean-squared thermal noise currents of transistors M_1, M_2, M_5 and load resistor R_L, respectively. Simulations show that the thermal noise is dominant and flicker noise is not significant for our circuit and therefore is ignored in the following discussion. The

mean-squared thermal noise voltage at the PD half-circuit output V_{O1} can be expressed as

$$\begin{aligned}\overline{v_{n,O1}^2} &= 4kTR_L\left(2\gamma g_{m1,2}R_L+\gamma g_{m5}R_L+1\right)\\ &\times \left(f_n-f_s\right)\end{aligned} \tag{5.18}$$

where $\gamma \approx 2/3$ is the coefficient of MOSFET channel thermal noise, $g_{m1,2}$ and g_{m5} are transconductances of transistors $M_{1,2}$ and M_5, f_s is related to the duration of the PD detection mode, $f_n \approx \frac{\pi}{2}\frac{1}{2\pi R_L C_L}$ is the noise bandwidth of the $R_L - C_L$ filter at the PD output, k is Boltzmann's constant, and T is absolute temperature.

To determine the total input equivalent noise power, the output mean-squared noise voltage $\overline{v_{n,O1}^2}$ at V_{O1} is doubled to account for the identical noise contribution of the duplicate power detector circuit, identified in Fig. 5.1, converted to voltage and divided by the PD power detection factor to obtain the PD input-equivalent mean-squared noise voltage $\overline{v_{n,in}^2}$,

$$\begin{aligned}\overline{v_{n,in}^2} &= \sqrt{2\overline{v_{n,O1}^2}}/\xi_p \\ &= 8\sqrt{\frac{2kT\left(2\gamma g_{m1-4}+\gamma g_{m5}+R_L^{-1}\right)\left(f_n-f_s\right)}{k_n^2\left(\frac{W}{L}\right)_{1-4}^2}}.\end{aligned} \tag{5.19}$$

From (5.19), the mean-squared input-referred noise voltage can be decreased by increasing $(W/L)_{1-4}$, R_L and decreasing g_{m5}.

5.3.1.3 Switch charge injection

The switches S_1 and S_2 in Fig. 5.4 are both realized with MOS transistors, and cause charge injection when switching from On-to-Off. This charge injection cannot be calibrated out, thus generates error for the PD output if the switch is not designed properly.

The switch set S_1 as shown in Fig. 5.7 consists of CMOS transmission-gate switches

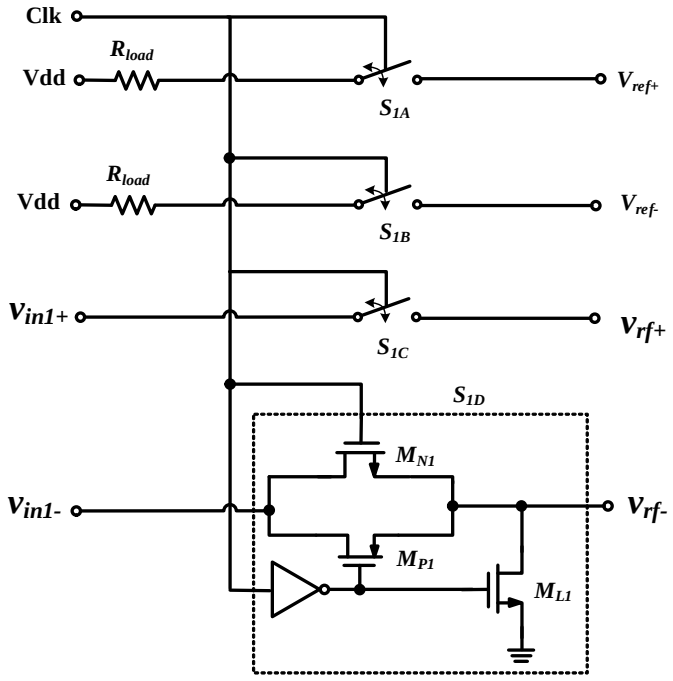


Figure 5.7: Transmission-gate switch set S_1.

$S_{1A} - S_{1D}$. S_{1C} and S_{1D} connect and disconnect the RF signal to and from the main PD input terminals. The circuit inside the dashed rectangle shown in Fig. 5.7 is the unit schematic of the transmission-gate switches $S_{1A} - S_{1D}$. Same-sized PMOS transistor, M_{P1}, and NMOS transistor, M_{N1}, are used to cancel charge injection. M_{N1} and M_{P1} have very small size to minimize feedthrough effects from drain to source. Small NMOS transistor M_{L1} is a pull-down transistor to avoid floating input terminals of PD during the calibration.

In order to remove the offsets caused by the switch charge injection to all PD input terminals during mode transitions, resistors R_{load} are added at the inputs of the reference switches S_{1A} and S_{1B}, as shown in Fig. 5.7, to emulate the signal-source resistance for v_{in1+} and v_{in1-} and thus provide the same loading to all four inputs to the PD circuit.

The second switch set, S_2, is designed with a pair of NMOS transistors with tiny size that cause very small charge injection on large C_b thus resulting in only small error voltages on the C_b's. When the differential PD output is measured, the difference due to charge injection becomes even smaller and can be ignored.

5.3.1.4 Calibration rate

As discussed above, the mismatch between the PD transistors is calibrated out by adjusting the bulk voltages of M_{1-4}. These voltages are stored on C_b's and are expected to remain constant during the PD detection mode. However, leakage currents, such as from MOSFET source-to-bulk, I_{sb}, drain-to-bulk, I_{db}, and deep nwell-to-bulk p-n junctions, I_{nb}, may affect the stored electron values on C_b's and decrease PD detection accuracy. The leakage-induced voltage variation on the $C_b's$, represented by $\triangle V_{Cb}$, depends on leakage currents, C_b, and the detection sample rate Δt as follows:

$$\triangle V_{Cb} = 2\left(I_{sb} + I_{db} + I_{nb}\right)\frac{\Delta t}{C_b}. \tag{5.20}$$

The voltage variation is mostly determined by process parameters I_{sb}, I_{db} and I_{nb}. Fast sample rate and large store capacitance C_b also help to reduce the voltage variation as well with a cost of chip area.

5.3.2 Summary

Compared to finite calibration error of PD as discussed in Subsection 5.3.1 and noise contribution discussed in Subsection 5.3.1.2, the switch charge injection error is relatively small and is ignored for simplification of analysis in this work. From the PD measurement accuracy point of view, the amplitude-squared input-referred error signal, V_{sen}^2, is a combination of V_{err}^2 found from (5.17) and input-referred noise in (5.19), and is the minimum RF input signal amplitude squared that the PD can detect. Once RF signal is added at PD input, V_{sen}^2 superimposes to the RF input signal and results in the total output voltage V_{tot} as:

$$V_{tot} = V_{O2} - V_{O1} = \underbrace{V_{rf}^2 \xi_p}_{V_{tot,rf}} + \underbrace{V_{sen}^2 \xi_p}_{V_{tot,sen}}. \tag{5.21}$$

In (5.21), $V_{tot,rf}$ and $V_{tot,sen}$ are components generated by real RF input signal and input-referred errors, V_{sen}^2, respectively. The error introduced in the PD measurement by calibration error and noise can be expressed as

$$\triangle V\,(\text{dBV}) \;=\; 20\log\left(1+\frac{V_{tot,sen}}{V_{tot,rf}}\right). \tag{5.22}$$

The maximum PD output error happens at lowest input power level, and this error decreases when increasing the input signal power level.

5.4 Circuits used in the calibrated PD

5.4.1 Amp1: folded-cascode amplifier with gain boost

To provide high open-loop gain, achieve stable closed-loop operation and power-down capability, a fully differential gain-boosted folded-cascode operational transconductive amplifier (OTA), labeled as *AMP*1 in Fig. 5.4, has been implemented as shown in Fig. 5.8. M_{F1-F2} are OTA input transistors, M_{F3-F10} form folded-loads, *AN* and *AP* are gain-boost amplifiers to obtain large gain OTA by increasing its output impedance. The schematics of *AN* and *AP* are one-stage differential pair amplifiers shown in Fig. 5.9. Diode-connected loads are used in *AN* and *AP* to move poles at output nodes to high frequency and guarantee the stability of the OTA circuit.

While there are advantages to the fully differential OTA such as rejection of the common-mode noise and even order distortions, its drawback is the need for a common-mode feedback (CMFB) circuit to reduce the effect of PVT and stabilize the DC outputs. The CMFB circuit, depicted in Fig. 5.8, is made with two identical resistors *R*, an amplifier *ACOM*, and buffers $M_{F11-F14}$, which isolate the CMFB circuit from the main amplifier output and avoid loading from feedback resistors, *R*. PMOS transistors $M_{F11-F14}$ are chosen for the buffers due to the low common-mode output voltage of the OTA. Transistors M_{S1-S2} are used to turn ON the OTA load during calibration and turn it OFF during the PD detection

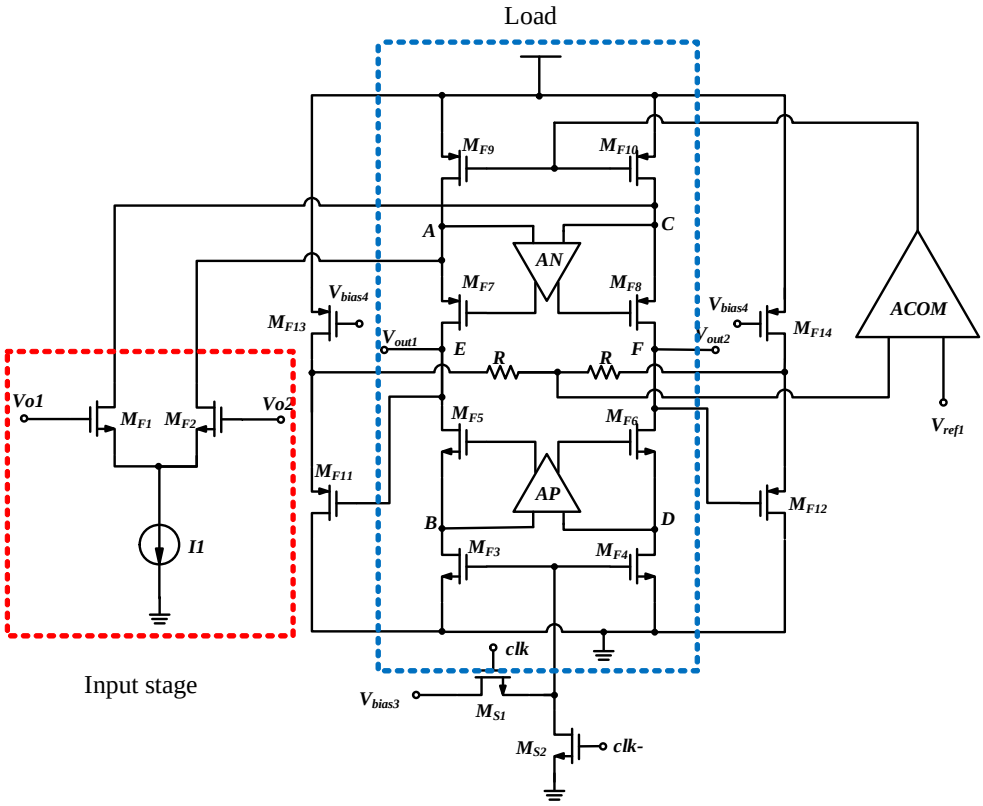
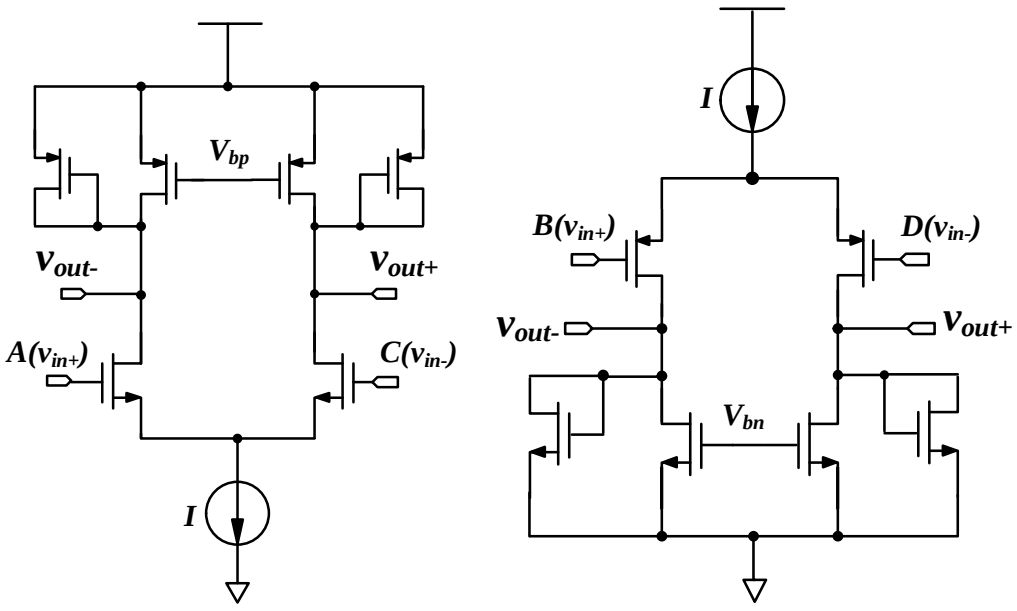


Figure 5.8: Schematic of the folded-cascode OTA with gain boosting.



(a) *AN* amplifier for gain boosting.

(b) *AP* amplifier for gain boosting.

Figure 5.9: Gain-boosting amplifiers.

to save power consumption and to prevent the folded-cascode amplifier from oscillating. As described in Section 5.3, once calibration is completed, switch set S_2 disconnects the C_b's from load nodes E and F, and the main dominant pole at OTA output moves to higher frequency, which may cause a stability problem in the folded cascode amplifier. If this stability problem is not addressed, the resultant oscillation may feed interference signals into the power detector output through parasitic capacitances and affect the PD operation. In this work, the amplifier is turned off in this mode to prevent oscillation.

The input signal to the OTA is applied to transistors M_{F1} and M_{F2}, and output voltages, V_{out1} and V_{out2}, are at nodes E and F, which are connected to the bulk terminals V_{b1} and V_{b2} as shown in Fig. 5.4. The resistances at nodes A (C) and nodes B (D) and E (F), of the amplifier can be expressed as:

$$R_{outA(C)} \approx \left(\frac{A_p g_{m_5} r_{o5} r_{o3}}{g_{m7} r_{o7}} \right) \parallel \left(g_{m_1} r_{o1} r_{oI1} \parallel r_{o9} \right), \tag{5.23}$$

and

$$R_{outB(D)} \approx \left(\frac{A_N g_{m7} r_{o7} \left(g_{m_1} r_{o1} r_{oI1} \parallel r_{o9} \right)}{g_{m5} r_{o5}} \right) \parallel r_{o3}, \tag{5.24}$$

$$R_{outE(F)} \approx \left[A_p g_{m5} r_{o5} r_{o3} \right] \parallel \left[A_N g_{m7} r_{o7} \left(g_{m1} r_{o1} r_{oI1} \parallel r_{o9} \right) \right], \tag{5.25}$$

where g_{m_1} to g_{m7} and r_{o1} to r_{o9} are transconductance and drain-source resistances of transistors M_{F1} to M_{F7} and M_{F1} to M_{F9}, respectively, and A_P and A_N are the DC gains of the gain-boosting amplifiers AP and AN, respectively. Comparison of all resistances in (5.25)-(5.24) shows that nodes $E(F)$ have the highest output resistance, which provides the high gain for the OTA. Also this resistance together with capacitors at node $E(F)$, which include the parasitic capacitances at these nodes and C_b, form the dominant pole of the OTA. The three poles associated with the OTA in the calibration mode can be expressed as follows:

$$p_1 = \frac{-1}{R_{out,E}(C_b + C_{gd5} + C_{gd7} + C_{gd11} + C_{gb11})}, \tag{5.26}$$

$$p_2 = \frac{-1}{R_{out,A}\left(C_{L,A} + C_{AN}\right)}, \tag{5.27}$$

and

$$p_3 = \frac{-1}{R_{out,B}\left(C_{L,B} + C_{AP}\right)}, \tag{5.28}$$

where

$$C_{L,A} = C_{gd9} + C_{db9} + C_{db1} + C_{gb7} + C_{gs7} + C_{gd1}, \tag{5.29}$$

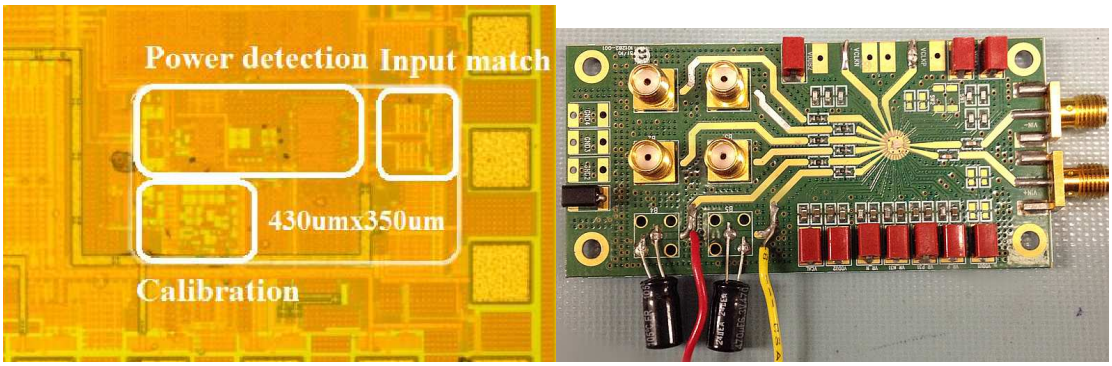
$$C_{L,B} = C_{gd3} + C_{db3} + C_{gs5} + C_{gs5}, \tag{5.30}$$

C_{AN} is the input capacitance of *AN* and C_{AP} is the input capacitance of *AP*, the C_{gs}'s, C_{gd}'s, C_{gb}'s, and C_{db}'s are the gate-source, gate-drain, gate-bulk and drain-bulk capacitances of each transistor, respectively. The second dominant pole is p_2, which is at nodes $A(C)$ due to the larger node parasitic capacitance compared to that of nodes $B(D)$ forming a pole at p_3. Gain-boosting amplifiers *AN* and *AP* also add extra poles to the system. In this design, amplifiers *AN* and *AP* were designed so that the poles at their outputs were placed at high frequencies.

During the calibration cycle, the self-calibrated PD forms a closed-loop negative feedback circuit, which includes the PD circuits, the amplifier $Amp1$ and the switch set S_2. The whole loop has four poles, three poles generated by $Amp1$ itself as discussed above, another pole, p_0, is contributed by the PD output resistance R_L and output capacitance $C_{out,PD}$

$$p_0 = \frac{-1}{R_L C_{out,PD}} \tag{5.31}$$

$$\begin{aligned} C_{outPD} &= C_L + C_{dgM_5} + C_{dbM_5} + C_{dgM_1} + C_{dbM_1} \\ &+ C_{dgM_2} + C_{dbM_2} + C_{A1}, \end{aligned} \tag{5.32}$$



(a) Chip micrograph. **(b)** PCB board.

Figure 5.10: (a) Power detector chip micrograph. (b) Test PCB board with the chip.

where C_{dgM_1}, C_{dgM_2} and C_{dgM_5} are drain-gate capacitances of transistors M_1, M_2 and M_5, respectively, and C_{A1} is the equivalent input capacitance of amplifier $Amp1$. For the PD to have high gain to overcome noise when sensing low input power, to provide filtering of the fundamental frequency at the PD output, and to reduce the offset error residual after calibration (see subsection 5.3.1,) both R_L and C_L are chosen to be large resulting in p_0 to be a low-frequency pole. The other low-frequency pole, p_1 in (5.26), is located at the output of $Amp1$ and is formed by the large capacitance C_b, which stores the calibration voltages, and the large output resistance of $Amp1$. To maintain stability of the detection loop, the pole p_1 is designed to be the dominant pole. Two other $Amp1$ poles, p_2 in (5.27) and p_3 in (5.28), are placed at higher frequencies than pole p_0, which is designed as the second dominant pole in the closed-loop, to make the closed-loop circuit stable.

5.4.2 The input match circuit

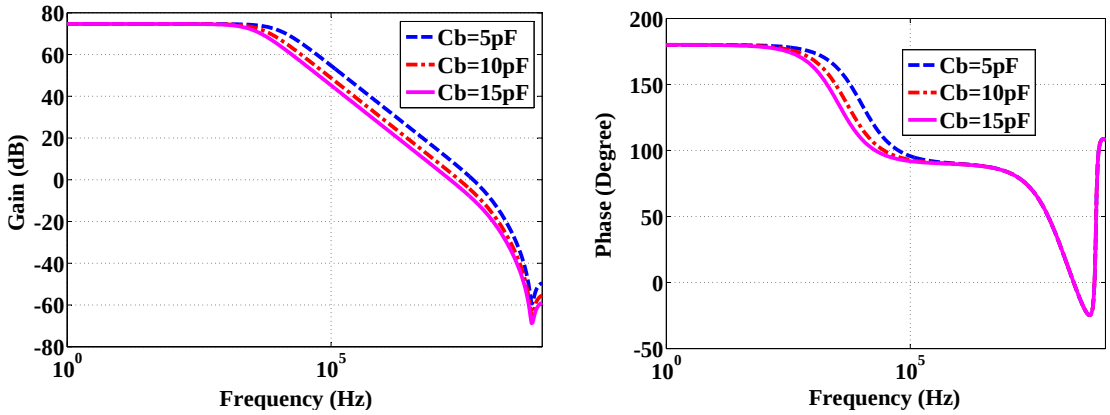
Power matching of the PD to the 100Ω differential input signal source was accomplished with a differential amplifier Amp0 [46] as shown in Fig. 3.5.

5.5 Simulations and measurement results

The power detector was fabricated in TSMC 65nm CMOS with a 1.2 V power supply. The chip micrograph and test PCB board are shown in Fig. 5.10. The fabricated circuit occupies

Table 5.1: DC bias voltage measurement results

Simulated	Measured
450 mV	444 mV
500 mV	501 mV
550 mV	553 mV
900 mV	899 mV
400 mV	408 mV
720 mV	717 mV



(a) Gain **(b)** Phase

Figure 5.11: Simulated (a) typical-corner gain and (b) typical-corner phase of the folded-cascode gain-boosted amplifier with load capacitances C_b of 5 pF, 10 pF and 15 pF.

430 μm $\times$ 350 μm including the input match circuit. The total power consumption is 7 mW. 1.2 mW is consumed by the power detector and the folded-cascode amplifier circuit, and the other 5.8 mW is consumed by the input match circuit, which will not be needed once the power detector is embedded in the SKA receiver chain. All the bias voltages are generated on chip. A comparison of design bias voltage and measured results is summarized in Table. 5.1.

Fig. 5.11 shows the simulated gain of the folded-cascode amplifier $Amp1$ for three different C_b's. This amplifier provides 75 dB of DC gain as shown in Fig. 5.11(a). The minimum phase margin is 60° with C_b of 5 pF, and 75° with C_b of 15 pF, which is the value used in the final design for storage of the calibration voltage. The second pole location is independent of C_b and is at 98 MHz. The total power consumption of the amplifier circuit

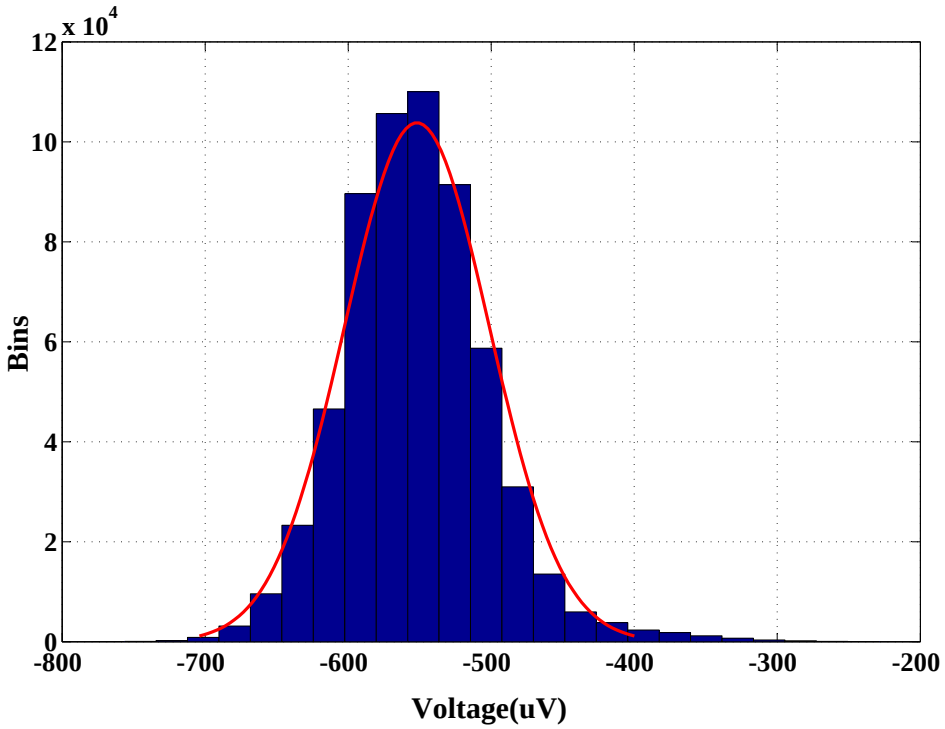


Figure 5.12: PD noise distribution.

is 0.61 mW.

Fig. 5.12 shows the histogram of the PD output noise obtained from measurement of the differential output voltage of the PD when the input is turned off and calibration is disabled. The measurements show that the noise exhibits an approximate Gaussian distribution with standard deviation of $50.7\,\mu$V and a mean of $510\,\mu$V. Since the calibration was turned off for this measurement, the mean value, i.e. the DC offset, is not zero. From these measurements, the estimated input-equivalent noise power is $-48.3\,$dBm, which is close to a simulation result of $-49.3\,$dBm. Note that the simulated input-match circuit's noise figure is approximately 4 dB and its gain is 6 dB, therefore due to the large noise of the PD the input-match circuit has negligible effect on the noise performance of the complete circuit.

Figs. 5.13 and 5.14 show the measured PD differential output voltage during calibration and detection modes for different input power levels with the input signal frequency set to 1.4 GHz. The minimum detected power was approximately $-48\,$dBm. The PD output set-

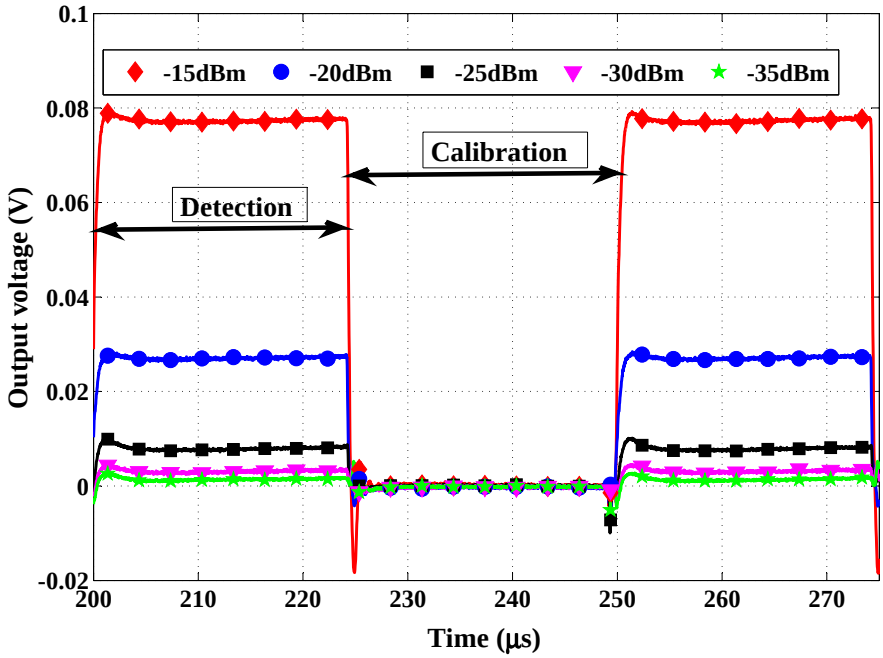


Figure 5.13: Power-detector output voltage at input power levels of -20 dBm, -25 dBm, -30 dBm and -35 dBm.

tles in less than 5 μs after the detection mode is turned on. Similarly, calibration completes in less than 5 μs.

Fig. 5.15 shows the measured output voltage versus the input power at different frequencies. The PD output voltage (dBV) shows a linear relationship with input power from -48 dBm to -11 dBm with ± 0.95 dB error at frequency range from 0.5 GHz to 1.8 GHz, which defines the -3 dB bandwidth of the PD. Note that the maximum detection level is limited by the input-referred $P_{1dB} = -11$ dBm of the input-match circuit. The -3 dB bandwidth of the power detector is approximately 1.8 GHz as seen from the PD frequency response in Fig. 5.16.

Fig. 5.17 shows the PD detection accuracy with different input power levels at 0.7 GHz, 1.0 GHz and 1.4 GHz, which covers the SKA mid-frequency range. The maximum detection error is 0.95 dB at input power of -48 dBm and this error decreases when input power increases. The effect of bulk leakage currents on the PD output was also measured and shown in Fig. 5.18. It is observed that when the source terminal voltage of the PD input

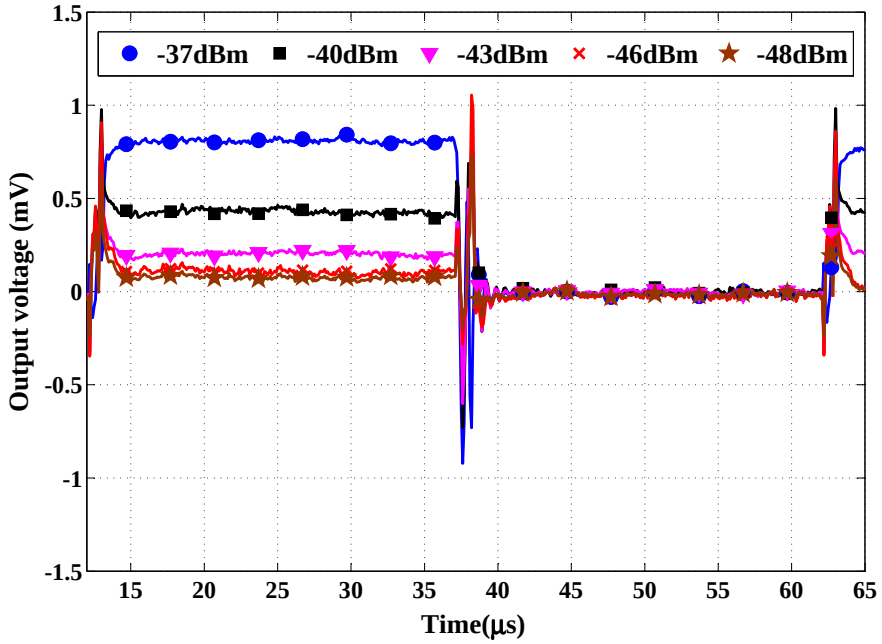


Figure 5.14: Power-detector output voltages at input power levels of -37 dBm, -40 dBm, -43 dBm, -46 dBm and -48 dBm.

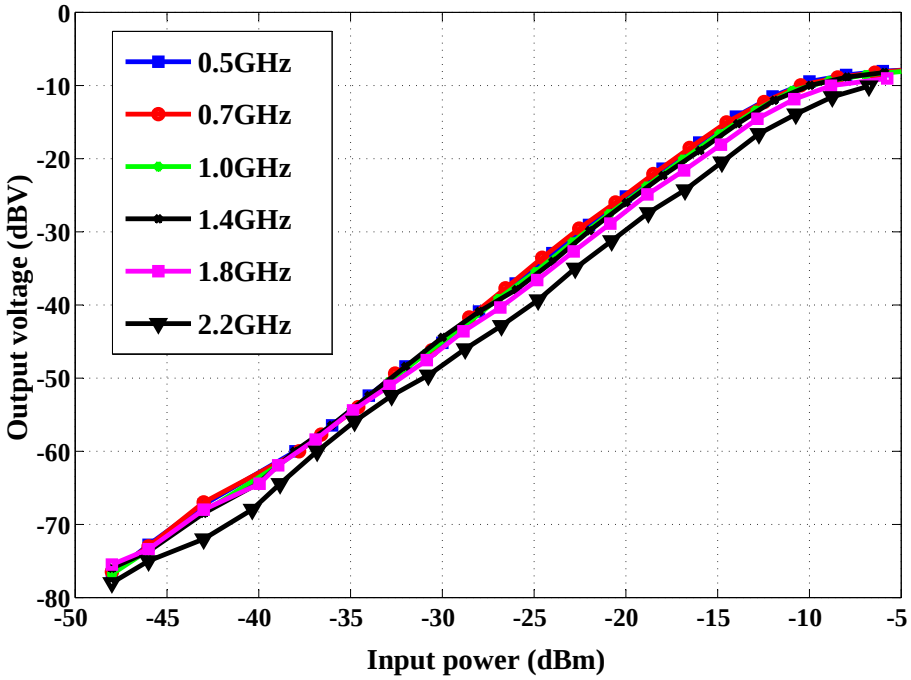


Figure 5.15: Output voltage versus input power at frequencies: 0.5 GHz, 0.7 GHz, 1.0 GHz, 1.4 GHz, 1.8 GHz and 2.2 GHz.

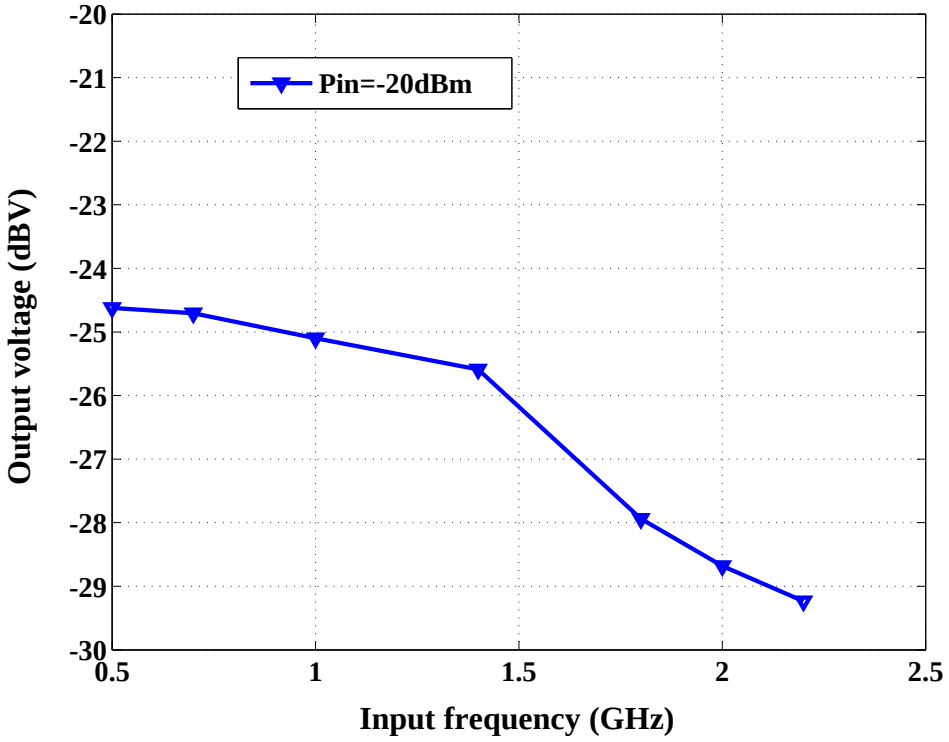


Figure 5.16: The power-detector frequency response measured with a -20 dBm signal.

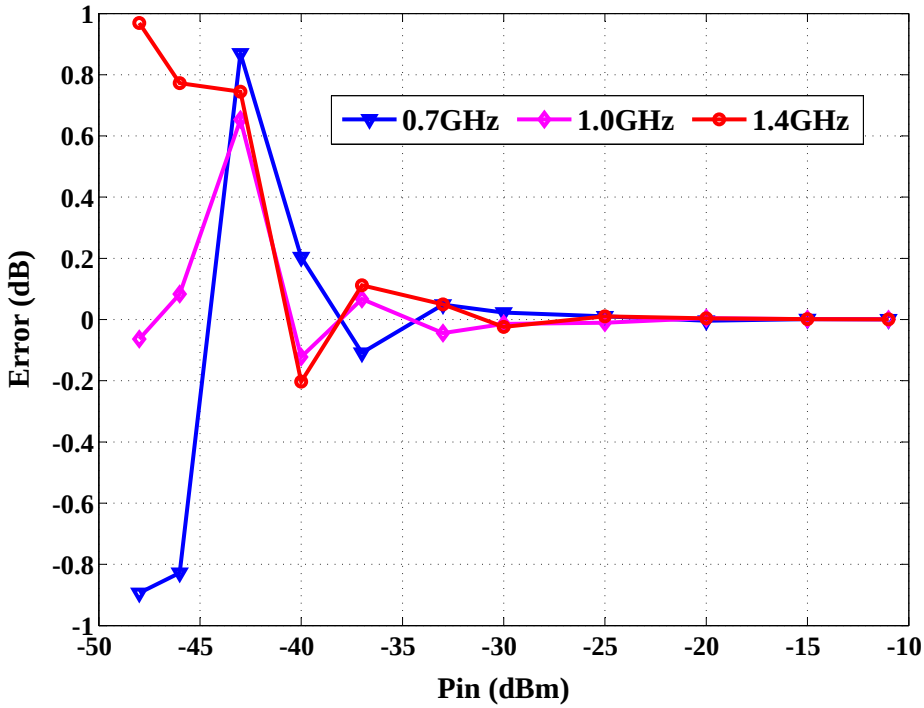


Figure 5.17: Power-detection error at 0.7 GHz, 1.0 GHz and 1.4 GHz.

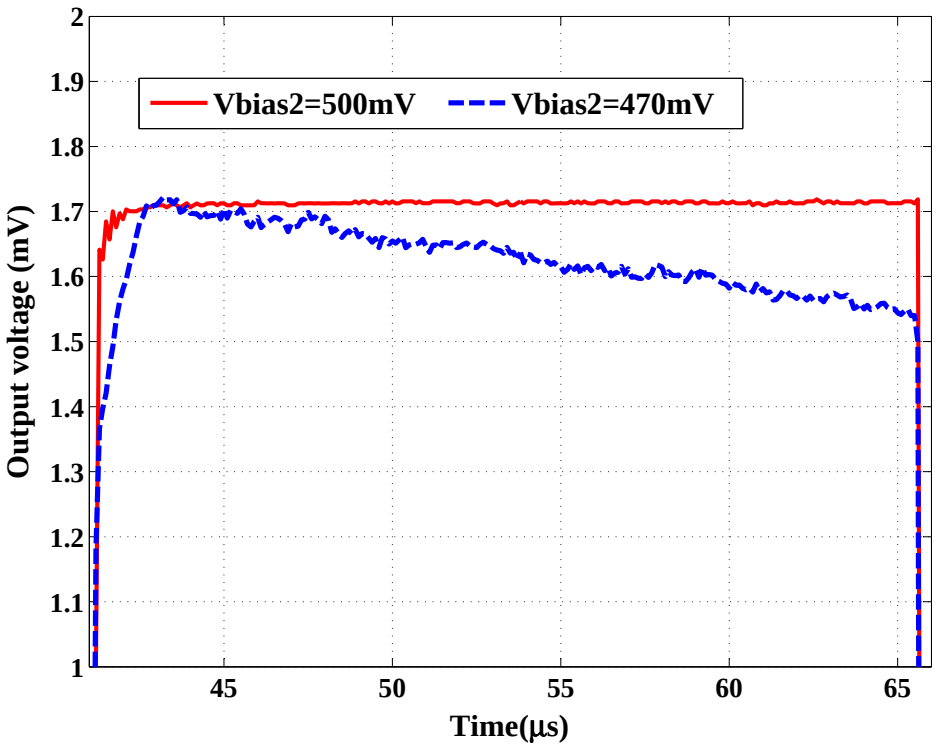


Figure 5.18: Bulk-leakage effect on the PD output.

Table 5.2: Performance summary and comparison

Parameters	This work	[28]	[24]	[25]	[27]	[26]
Process (CMOS)	65nm	65nm	0.13um	0.13um	0.18um	40nm
Sensitivity (dBm)	-48	-25	-35	-33	-39	-10.5
Detection range (dB)	37	25	20	43	20	32.5
Operating frequency (GHz)	0.5-1.8	N/A	0.125~1.4	16	3.1-10.6	5
Linearity error for specified input range	±0.95dB for 37dB ±0.5dB for 29dB	N/A	±0.5dB for 18dB	±1dB for 43dB	±2.9dB for 20dB	±0.6dB for 32.5dB
Power consumption (mW)	1.2	N/A	0.18	35.2	10.8	0.349
Circuit area (mm^2)	0.036	N/A	0.013	0.75	0.36	0.009
Calibrated	Yes	No	No	No	Yes	No
Measured	Yes	No	Yes	Yes	Yes	Yes
Inputs/Outputs	D/D*	D/S*	S/D*	S/S*	D/D*	D/S*

* D: differential, S: Single-ended

transistors, V_{bias2}, is set properly the discharge of C_b is reduced and the PD output voltage is kept constant over time. Fig. 5.19 shows the power-detector input reflection coefficient, which is less than -9.8 dB from 100 MHz to 5 GHz. The summary of the performance of this proposed PD circuit and other recently published PD circuits is shown in Table 5.2.

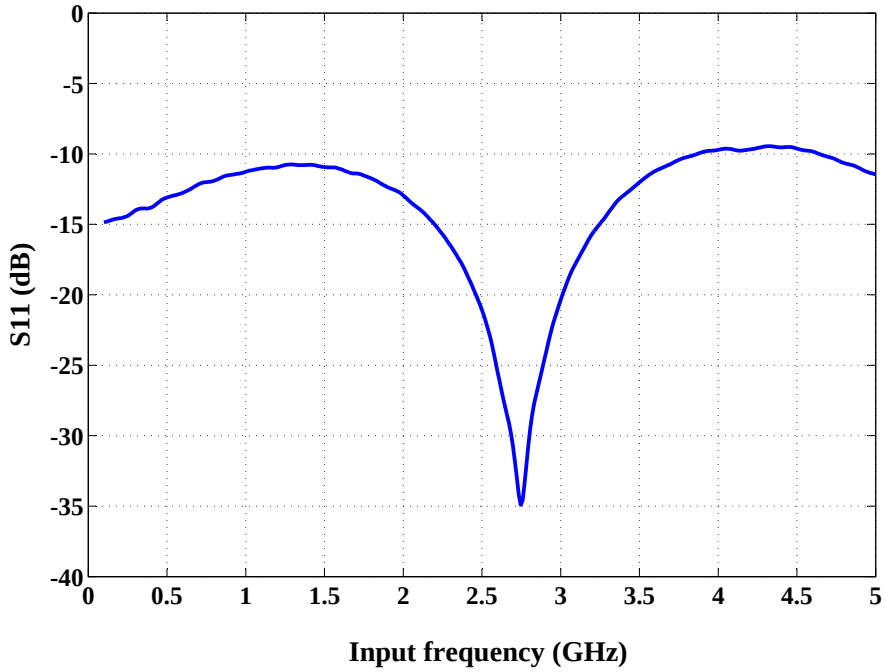


Figure 5.19: Input reflection coefficient.

5.6 Conclusions

In this chapter, an analog self-calibrated high-sensitivity broadband differential CMOS power detector using MOSFET square-law characteristics in saturation was proposed for use in an SKA receiver. All input-referred mismatches, which include input transistor mismatches, load transistor mismatches and resistor mismatches, are compensated by adjusting the power detector input transistor bulk voltages. The advantage of the proposed calibration technique over a conventional auto-zero method is that the switch charge injection, which cannot be calibrated out, appears at the bulk terminal instead of the gate terminal of the input transistors, since the transistor gains from bulk to drain are much less than from gate to drain, and so the charge injection does not affect the output significantly.

In this chapter, a high-gain folded cascode OTA with gain boosting was used for calibration. The OTA senses the mismatches at PD output, amplifies, and generates a compensation voltage at the PD input transistor bulk terminals to compensate mismatches. This amplifier provided 75 dB DC gain with less than 0.1mW power consumption. This high

gain dramatically increases the calibration accuracy. Effects of noise and switch charge injection on sensitivity were also discussed.

This power detector operates over an input power range from -48 dBm to -11 dBm with output voltage error of less than 0.95 dB and input-referred P_{1dB} of -11 dBm, determined by the input match circuit. The -3 dB bandwidth of the power detector is about 1.8 GHz, which covers the SKA mid-frequency range from 0.7 GHz to 1.4 GHz. The power consumption is only 1.2 mW for the PD itself.

Chapter 6

SKA receiver design with the embedded PD

In Chapter 5 the implemented self-calibrated RMS PD was discussed and was shown to achieve all requirements listed in Table 1.3. The last step of the work is to embed the PD in an SKA receiver. In this chapter the receiver designed with all blocks embedded, which include PD, low noise amplifier (LNA) and analog-to-digital converter (ADC), is discussed. In order to enable integration into the receiver, some changes were made in the PD compared with the PD circuit discussed in Chapter 5 as discussed in Section 6.2. Layout design considerations are also described in this section. Section 6.3 presents the measured results of the PD embedded in the receiver using a signal generator and noise sources. The last stage amplifier in the receiver before the ADC is a VGA. However, a different VGA designed by other members of our team was used instead of the VGA discussed in Chapter 3, because noise measurements showed that for accurate noise parameter measurements gain compression of much less than 0.1 dB was required. Therefore, the linear-in-dB requirement was removed in favor of linearity.

6.1 SKA receiver topology

The SKA receiver topology that was designed and fabricated is shown in Fig. 6.1. The

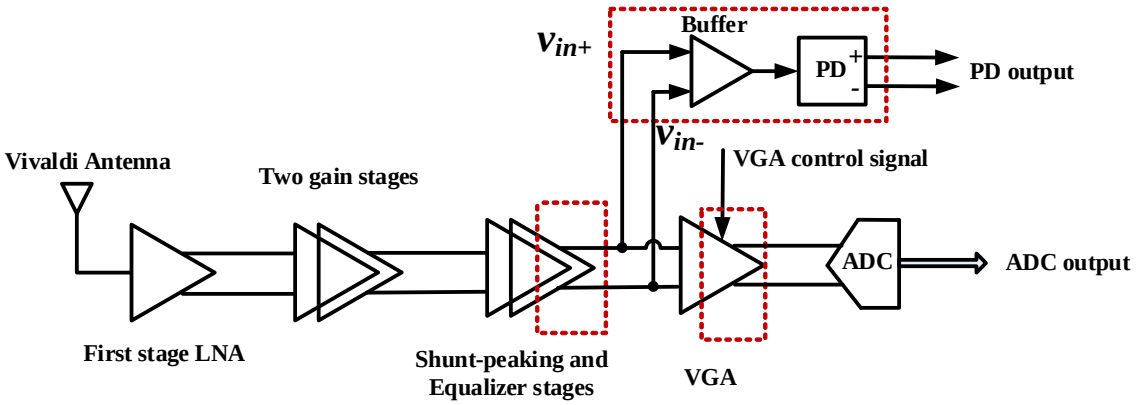


Figure 6.1: Designed SKA receiver topology with all blocks embedded.

first stage is an LNA, which is a noise-cancelling LNA, converts the single-ended input to a differential output. After the LNA, there are five stages (three gain stages, an equalizer stage and a VGA stage) to amplify the received input signal to required levels for the ADC. The last stage before the ADC is a VGA as shown in Fig. 6.1, which also functions as an output buffer, providing 100 Ω differential output match for measurement of receiver chain performance without the ADC. The ADC used in the design is a 5-bit 5 Gs/s ADC designed by one of the group members. As mentioned in Chapter 1, the power detector in the SKA receiver is used to measure the total received power before the VGA in order to preserve the total received power information required for some astronomical observations. In order to avoid loading the second-last gain stage, a buffer is added between the output of the second last gain stage and the power detector input as shown in Fig. 6.1.

The whole receiver chain was completed by our research group members working together. The author completed the PD, the buffer circuit, and also layed out the shunt-peaking and equalizer stages and VGA stage. Other work was completed by group members [Dr. Leonid Belostotski, Aaron Beaulieu, Donuwan Navaratne, and Yongsheng Xu]. The dashed rectangles indicate my contributions to the whole receiver design.

6.2 PD circuit embedded in receiver

6.2.1 PD circuit topology

The PD circuit embedded in the SKA receiver is shown in Fig. 6.2, The dashed rectangles indicate the new and updated blocks compared with the circuit in Fig. 5.4 that was discussed in Chapter 5. The input match circuit designed for measuring the PD separately was replaced by an input buffer to isolate the main PD circuit from the receiver chain. In this PD, an amplifier, $Amp2$, is added after the main PD circuit to further amplify the PD output voltage of a few micro-volts, which is hard to measure at the PD output due to noise and resolution of the oscilloscope, to millivolt levels at the $Amp2$ output. The reason that the output is not taken from the output of amplifier $Amp1$ is because $Amp1$ is a folded-cascode

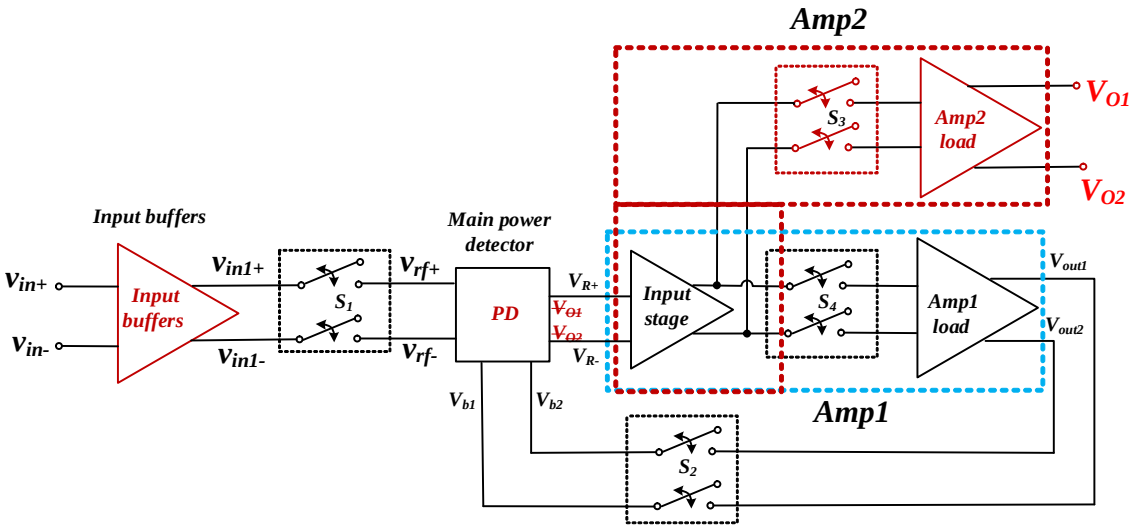


Figure 6.2: Self-calibrated PD topology used in the SKA receiver.

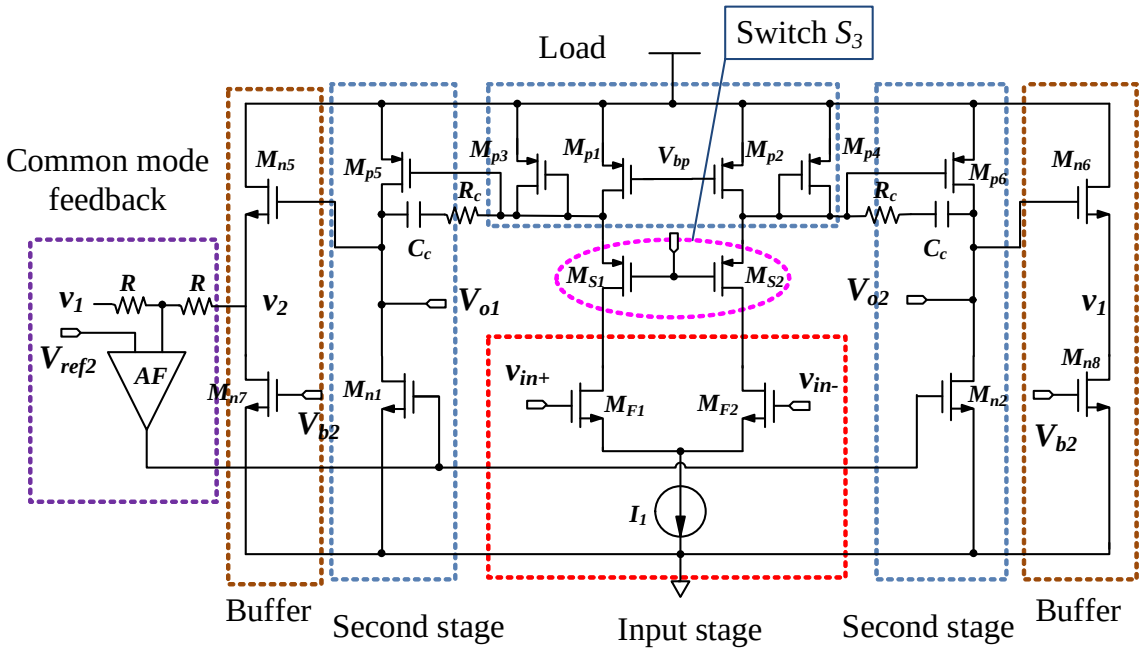


Figure 6.3: Two stage amplifier (*Amp*2).

gain-boosted amplifier that provides large loop gain for high accuracy calibration and thus has a very limited output swing, which would limit the PD detection range.

*Amp*2 in this work was designed using a two-stage differential OTA as shown in Fig. 6.3. The second stage of *Amp*2 was designed as a common-source amplifier providing maximum output swing, which is presented as ΔV_o

$$\triangle V_o = V_{dd} - V_{ds,M_{n1,n2}} - V_{ds,M_{p5,p6}} \tag{6.1}$$

where $V_{ds,M_{n1,n2}}$ and $V_{ds,M_{p5,p6}}$ are overdrive voltages of transistor $M_{n1,n2}$ and $M_{p5,p6}$, respectively. A common-mode feedback circuit formed by 2 R's and amplifier AF was designed to compensate $Amp2$ output operating point changes due to PVT variations. The buffers after the output stage composed of M_{n5}, M_{n7} and M_{n6}, M_{n8} are used to isolate the common-mode feedback circuit from the output to avoid a decrease in voltage gain.

In order to compare the resultant detection range with that PD output, $\triangle V_o$ is referred back to the $Amp2$ input, represented by $\triangle V_{in}$, which is the main PD output, by dividing by the gain of $Amp2$,

$$\triangle V_{in} = \triangle V_o / A_{amp2}. \tag{6.2}$$

The maximum output swing at the main PD circuit, shown in Fig. 6.4 is $\triangle V_{PD}$,

$$\triangle V_{PD} = V_{dd} - V_{ds,M_{5,6}} - V_{ds,M_{1,2}} - V_{R_s} \tag{6.3}$$

where $V_{ds,M_{5,6}}$ and $V_{ds,M_{1,2}}$ are overdrive voltages of transistors $M_{5,6}$ and $M_{1,2}$, and V_{R_s} is the voltage drop across R_s. $\triangle V_o$ and $\triangle V_{PD}$ are of the same order and $\triangle V_{in}$ is much smaller than $\triangle V_{PD}$ due to the gain of $Amp2$, which is in the order of 40 dB in this design. So, $Amp2$ reduces the minimum detected power while also reducing the maximum detection range.

As described in Chapter 5, mismatches of the circuit components of the main PD circuit and input-referred mismatch of $Amp1$ are calibrated during the PD calibration cycle while mismatches of $Amp2$, which is not in the calibration path, cannot be calibrated and are amplified during the PD detection cycle creating offsets at V_{o1} and V_{o2}. In order to minimize this offset, $Amp1$ and $Amp2$ are designed to share the same input stage, shown in Fig. 6.2, which is the main source of mismatch, but with different loads. Switches S_3 and S_4 are used

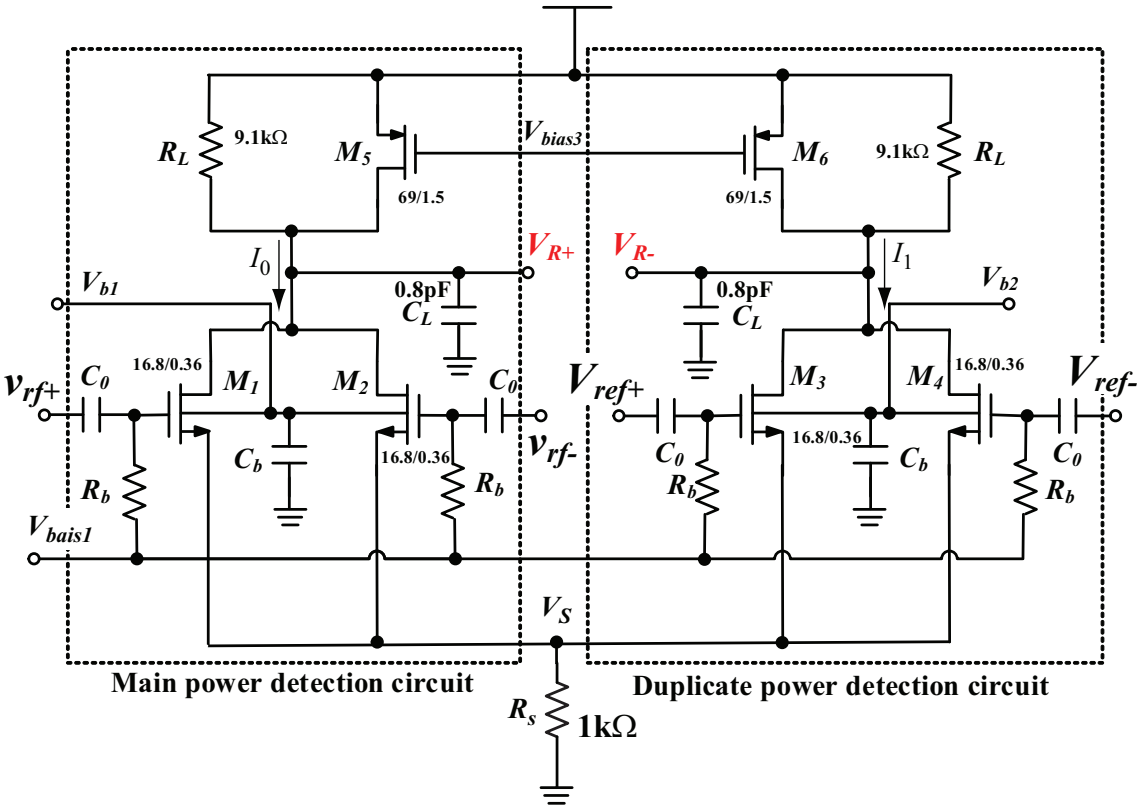


Figure 6.4: PD circuit that was embedded in the SKA receiver.

to switch loads between the calibration cycle and detection cycle. These switches are in the signal path and realized with MOSFET transistors. Transistor sizes are very carefully selected to have small resistance and to provide only small charge injection. The transistor sizes of the two sets of switches are chosen the same, which mostly cancels the charge injection during transition between calibration and detection.

For the main PD circuit, shown in Fig. 6.4, the input transistors $M_1 - M_4$ sources are connected to ground through a 1kΩ resistor to generate 500 mV source voltage instead of directly connecting an off chip voltage source as was used for the PD in Chapter 5. This reduces the number of bondpads. Due to the chip area limitation, the capacitance at the sources of $M_1 - M_4$ is also removed and only two bondpads connected to V_{o1} and V_{o2} are kept in the final layout. The input signal is supplied from the SKA receiver input.

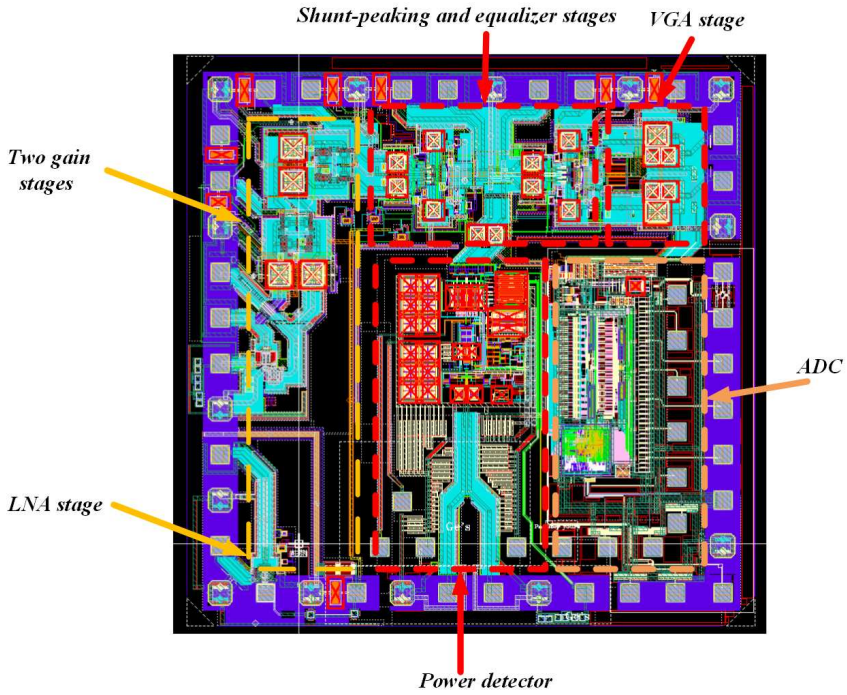
6.2.2 Layout considerations

The whole receiver was designed in a TSMC 65 nm GP CMOS process, and the chip layout is shown in Fig. 6.5(a). The chip area is $1.2 \times 1.5\ mm^2$ including all bondpads. Fig. 6.5(b) shows PCB board with the receiver chip embedded used for measurements listed in this Chapter.

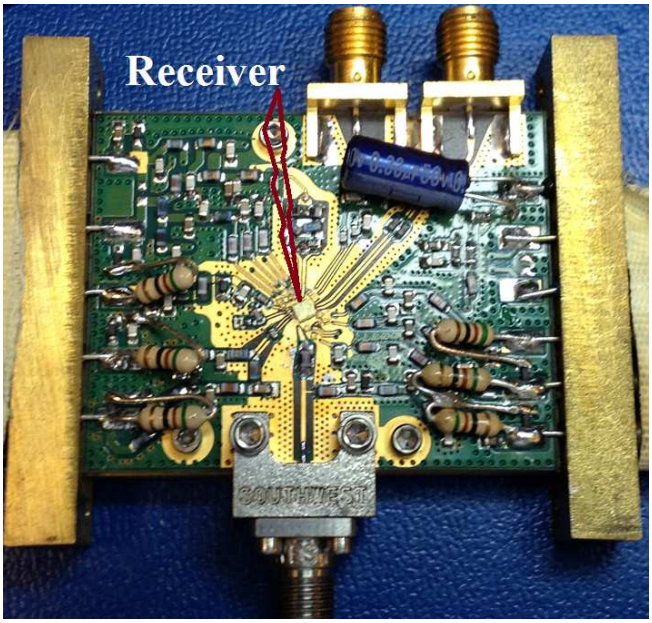
For layout design, most of the components from design kits were edited for suitable application in this receiver. The transistor layout, available in the design kit, was modified such that the gate fingers were contacted on both sides reducing gate resistance, which is very important for low noise circuits. Standard MIM capacitance was also modified by adding shielding metal underneath the bottom plate to reduce noise pick-up from the substrate. The large-width transistors were split into multiple transistors in parallel, reducing gate resistance and allowing for current to flow into the drain evenly while having comparable parasitic capacitance. Signal traces and power supply paths were drawn consisting of multiple metal layers and with maximum number of via connections to reduce the trace inductance and current density.

For better transistor match, common centroid layout is preferred, which can reduce the process variation effects on transistors [72]. Two transistors with a common centroid layout used in the PD are shown in Fig. 6.6. Transistor 1 on the left-top and Transistor 1 on the right-bottom form one large transistor with drain, source and gate terminals connected, and Transistor 2 on the left-bottom and Transistor 2 on the right-top form another large transistor. These two large transistors are the same size and are expected to be well matched. This method needs very careful layout considerations at high frequency operation because of the long signal traces adding parasitic capacitance.

All signal traces were isolated from the substrate using metal strips, which reduce substrate noise pick-up [73]. The importance of substrate shielding has been verified previously with a measured noise figure increase of > 0.1 dB in an SKA LNA that did not employ substrate shielding [74]. Thus, all signal traces were shielded to avoid substrate noise



(a)



(b)

Figure 6.5: (a) Receiver layout (b) Receiver chip embedded on PCB board.

pick-up. An example of the shielding employed under the lines carrying the RF signals is shown in Fig. 6.7. The RF signal trace shown in Fig. 6.7 was surrounded by multiple metal layer paths, which were left floating and not connected to the IC substrate in this design.

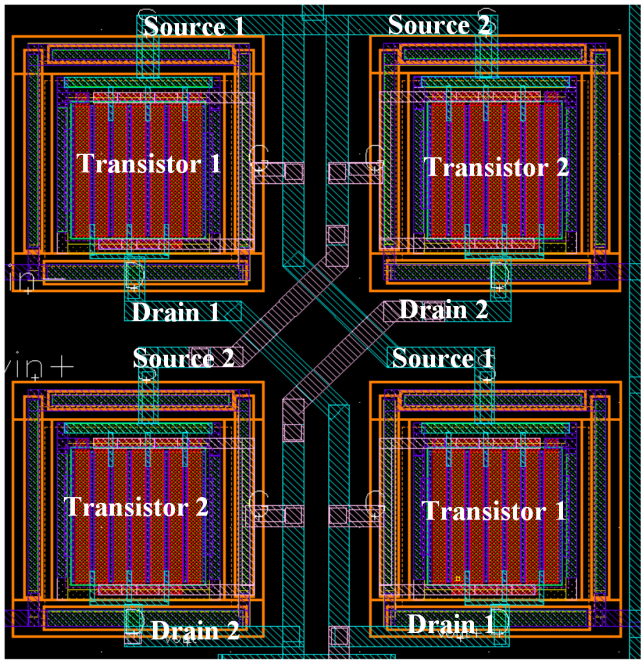


Figure 6.6: Transistor layout design example.

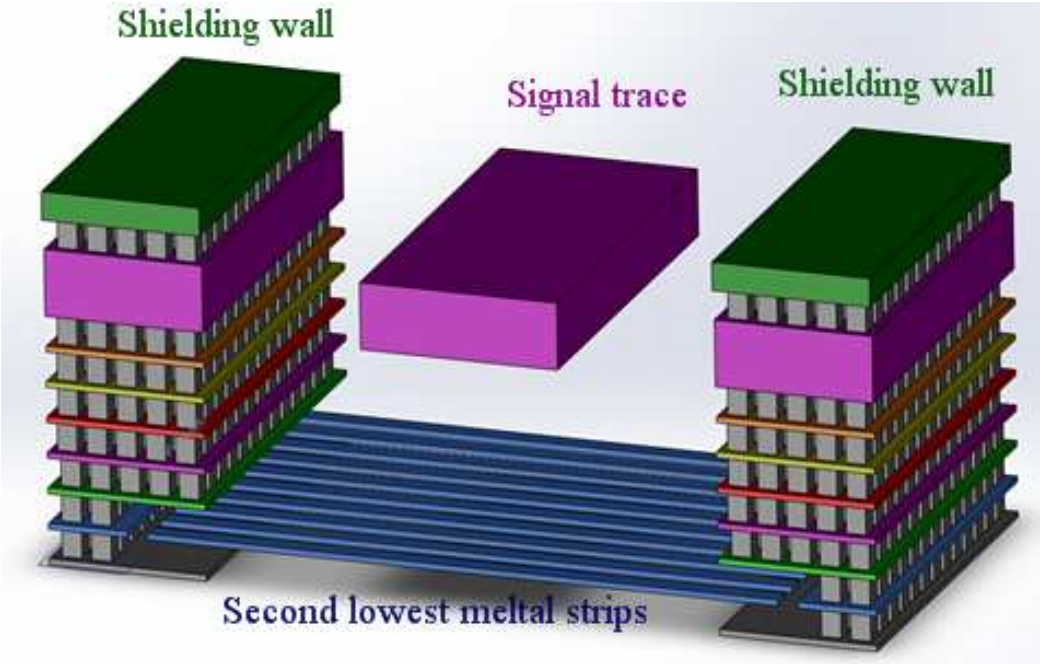


Figure 6.7: Signal trace shielding.

All metal layers from bottom metal to top metal were connected with a large number of vias. The floating thin metal strips on the second lowest layer were added across signal paths between the two shielding walls to provide shielding of the substrate [73, 75]. The shielding walls were left floating as that provided better noise isolation than when directly connected to the substrate, as verified by former measurements results. A large number of ground bond pads were connected together and bonded to a circuit board to provide a good RF ground. This provides a low-impedance path for RF ground currents between the signal ground on the die and the circuit board. All grounded structures were well interconnected to minimize the resistance path for the RF ground currents.

6.3 Measurement results of the embedded PD

The power detector was measured by connecting a noise source to the SKA receiver input. The available noise power at the receiver input was adjusted by adding attenuators between the input noise source and the receiver input. The input-referred equivalent noise temperature, T_a of the attenuator is calculated using

$$T_a = T_o \left(\frac{1}{G_a} - 1 \right), \tag{6.4}$$

where $T_o = 290K$, G_a is the attenuator gain. The total noise power, P_{in}, at the receiver input is calculated by

$$P_{in} = k\,(T_s + T_a)\,BG_a \tag{6.5}$$

where T_s is noise source temperature, k is Boltzmann's constant and B is integrated noise bandwidth.

Two noise sources were used in this measurement. The first noise source was Agilent's MY44420986 with cold noise temperature, T_c, of 302.9K, which corresponds to -83.79 dBm over 1 GHz noise bandwidth, and average Excess Noise Ratio (ENR) of 4.95 dB.

Table 6.1: Input noise power at the SKA receiver input.

Index	Attenuator gain	Input referred noise temperature of attenuators (K)	Total input noise temperature of receiver (K)	Input noise power (dBm)
1	0 dB	N/A	1250	-77.6
2	-1 dB	77.05	1054	-78.4
3	-2 dB	174.06	898.4	-79.1
4	-3 dB	296.19	774.8	-79.7
5	-4 dB	449.93	676.7	-80.3
6	-5 dB	643.50	598.7	-80.8
7	-6 dB	887.17	536.8	-81.3
8	-7 dB	1193.9	487.6	-81.7
9	-8 dB	1580.12	448.5	-82.0
10	Noise off	N/A	302.9	-83.8
11	-8 dB	1580.12	262.6	-84.4
12	-7 dB	1193.9	253.7	-84.6
13	-6 dB	887.17	242.49	-84.8
14	-5 dB	643.50	228.38	-85.0
15	-4 dB	449.93	210.61	-85.4
16	-3 dB	296.19	188.24	-85.9
17	-2 dB	174.06	160.08	-86.6
18	-1 dB	77.05	124.6	-87.7
19	0 dB	N/A	80	-89.6

The noise source hot temperature was calculated by using

$$T_s = ENR \times 290\,K + T_c. \tag{6.6}$$

The second noise source used for measurement was a Maury Microwave Liquid Nitrogen noise source, which provides low noise power with a noise temperature of approximately 80 K.

The total noise powers at the input of the SKA receiver from the two noise sources and different attenuators are summarized in Table. 6.1. The data in rows 1-10 and 11-19 were calculated with Agilent's MY44420986 and Maury Microwave Liquid Nitrogen noise sources, respectively. The two noise sources can provide input power ranging from -89.57 dBm to -77.6 dBm as shown in the last column of Table. 6.1.

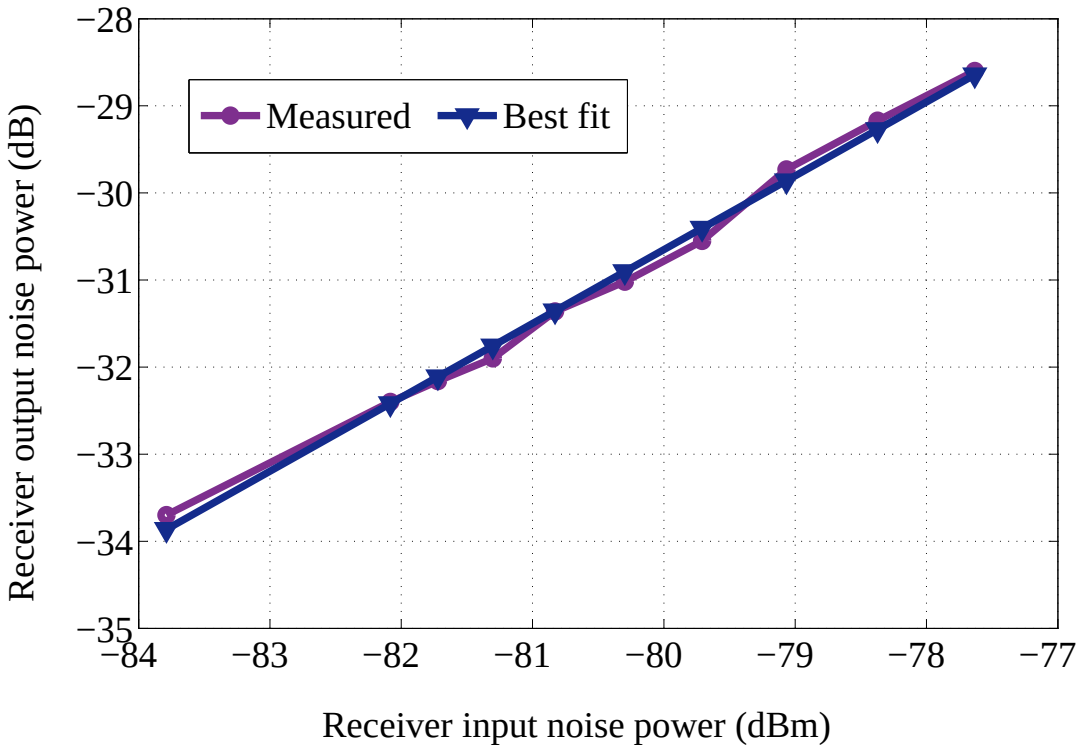


Figure 6.8: Receiver output power versus input noise power for Agilent's MY 44420986 noise source.

6.3.1 Receiver linearity measurement

The power detector is located before the VGA stage, which is the last stage of the receiver. In the following measurements, VGA gain was set to 0 dB to set the power detector input power to be the same as the receiver output power. Before proceeding with the PD measurements, the receiver linearity was checked with Agilent's MY44420986 noise source followed by different attenuators. The measurement results are shown in Fig. 6.8. The receiver output power achieved a good linear relationship with the input noise power with a slope of 0.85. The reason that the slope is 0.85 rather than 1 is because the power meter adds its own noise to the measured signal. This power meter noise power produces an offset in measurements, which affected low power more than high power level.

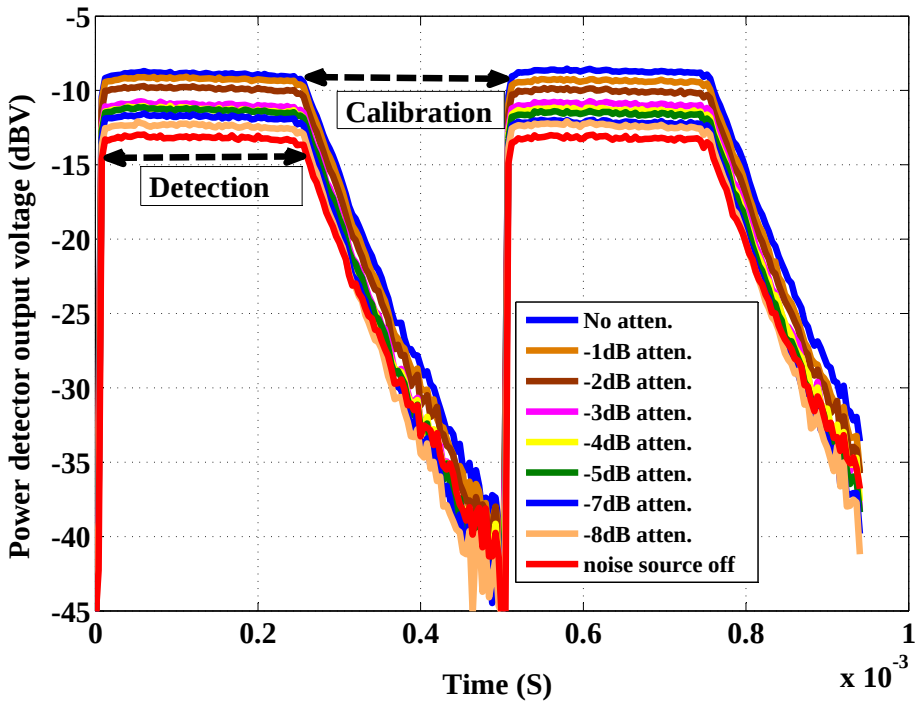


Figure 6.9: Power detector output voltage at different input signal power level (noise power). The top blue line shows PD output voltage at the maximum noise temperature with no attenuator added and the red line at bottom is the PD output voltage at the lowest noise temperature. All curves between from top to bottom are in order of 1 dB, 2 dB, 3 dB, 4 dB, 5 dB, 6 dB, 7 dB and 8 dB attenuations of the maximum noise temperature.

6.3.2 PD measurements

The time domain measurement results of the PD using Agilent's MY44420986 noise source followed by different attenuators is shown in Fig. 6.9. The PD had a short detection time but very long calibration time that was caused by the second stage of the $Amp2$, which was OFF during the calibration cycle and its leakage current discharged the output nodes. The calibration was completed by $Amp1$ and had less than $5\mu s$ response time as measured in Chapter 5. Fig. 6.10 shows power detector output voltage at different noise power levels. The PD output voltage (dBV) shows a good linear relationship with the input noise power with slope rate of 0.73 dBV/dBm. The non-unity slope is caused by the noise floor of the oscilloscope used for measuring the power detector output.

As described in Section 6.3.1, the power detector input power equals to the receiver

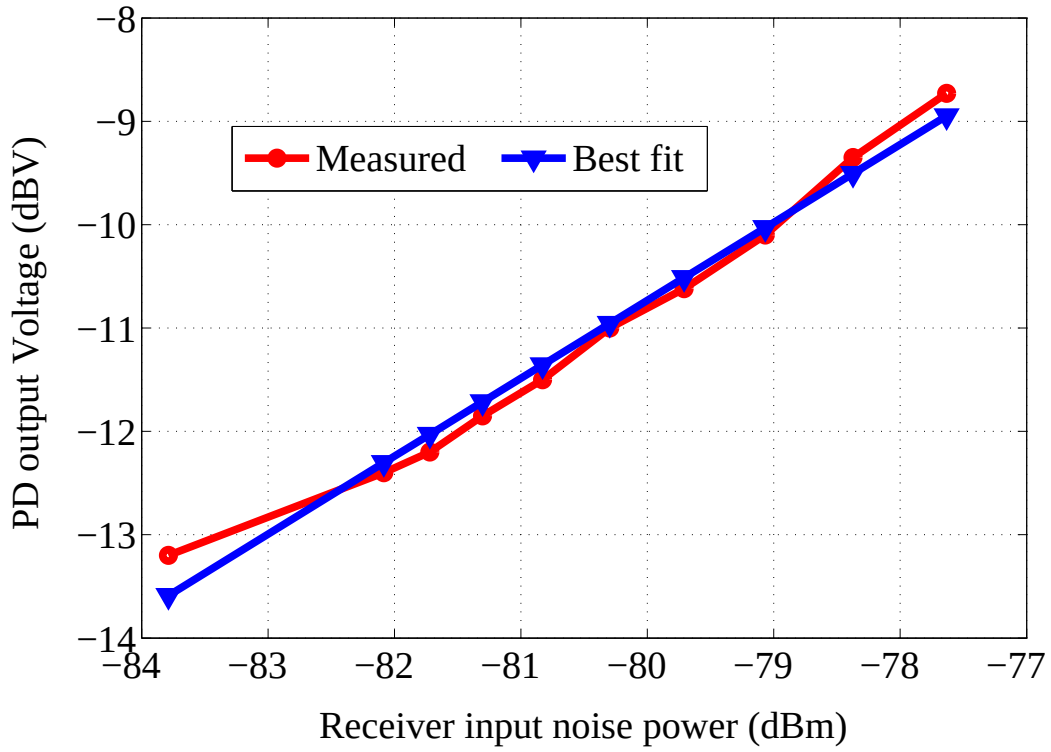


Figure 6.10: PD output voltage versus input power for Agilent's MY 44420986 noise source.

output power as the VGA gain is set to 0 dB. The PD transfer function between the output voltage (dBV) and the input power with Agilent's MY44420986 noise source is presented in Fig. 6.11. The output voltage showed good linear performance with its input signal power. In order to check the linear performance of the whole input power range, Fig. 6.12 shows the PD output voltage when the input noise power is generated with Liquid Nitrogen and Agilent's MY44420986 noise sources. The PD output voltage (dBV) showed linear performance with the input power with a slope of 0.78 dBV/dBm that is the power detector gain, and achieved a maximum deviation from best fit curve of 0.6 dB within the whole input power range, of 12 dB.

The maximum measurable noise power of the receiver is determined by maximum noise power of the noise source, which is -76.2 dBm in this measurement. A signal generator was used to measure the maximum detection power level. The PD detector output voltage at different power levels set by the signal generator is shown in Fig. 6.13. The maximum de-

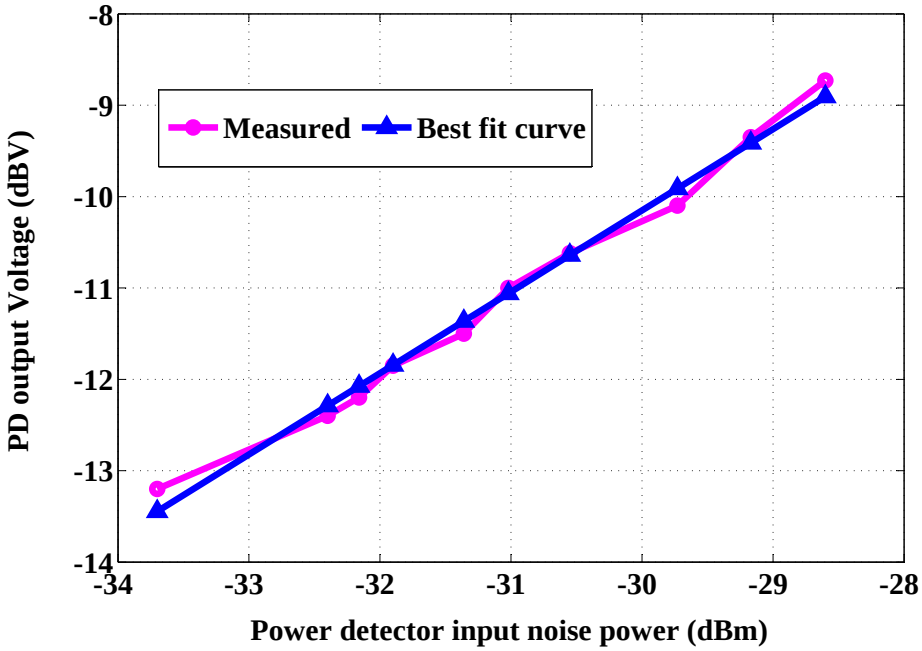


Figure 6.11: PD output voltage versus receiver output power at the maximum input noise temperature using Agilent MY 44420986 noise source and attenuators. The receiver output with the VGA gain set to approximately 0 dB, equals to the power detector input power.

tection power level is -70 dBm and saturates when the power is higher. Thus, the detection range of the PD is from -89.6 dBm to -70 dBm as shown in Fig. 6.14. If the gain of the LNA and the gain stages before the PD was de-embedded, the power detection range of the power detector is approximately from -39.6 dBm to -20 dBm.

6.4 Conclusions

The design considerations of the SKA receiver and power detector were discussed in this chapter. The whole receiver design was completed by many members of our research team. The author completed layout of the shunt-peaking gain stage, the equalizer and the VGA blocks, and the PD circuit, which was also designed by the author, together with two other group members who completed the whole chip layout for integration.

In order to make the PD more suitable to use in the receiver, changes were made to the PD circuit including the replacement of the input match circuit with an input buffer for

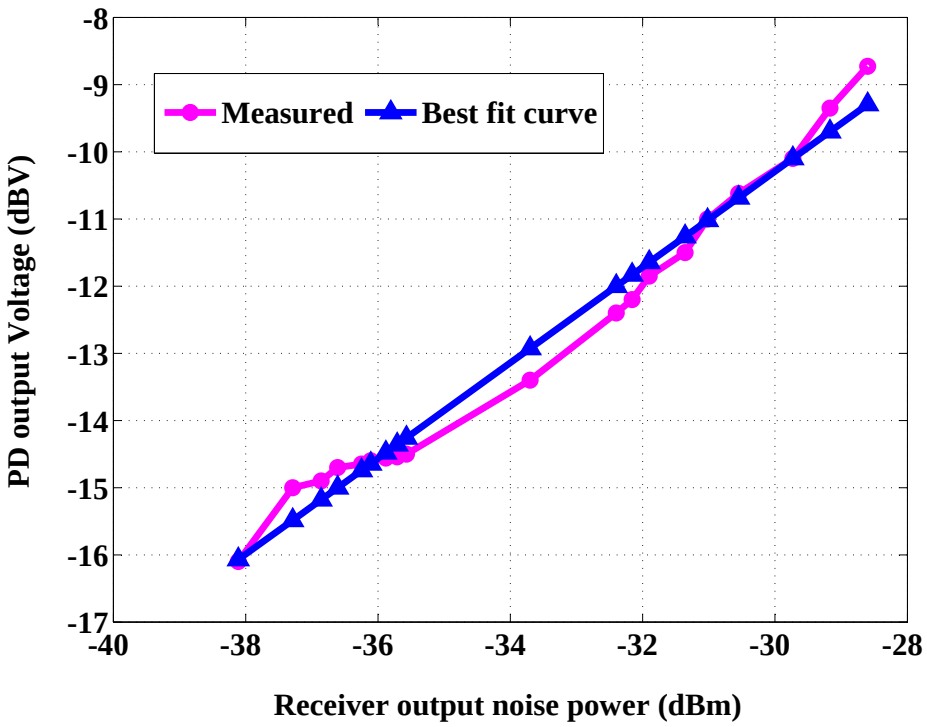


Figure 6.12: PD output voltage versus receiver output power for the whole input noise power range. This power is measured at receiver output with the gain of the last stage VGA set to approximately 0 dB.

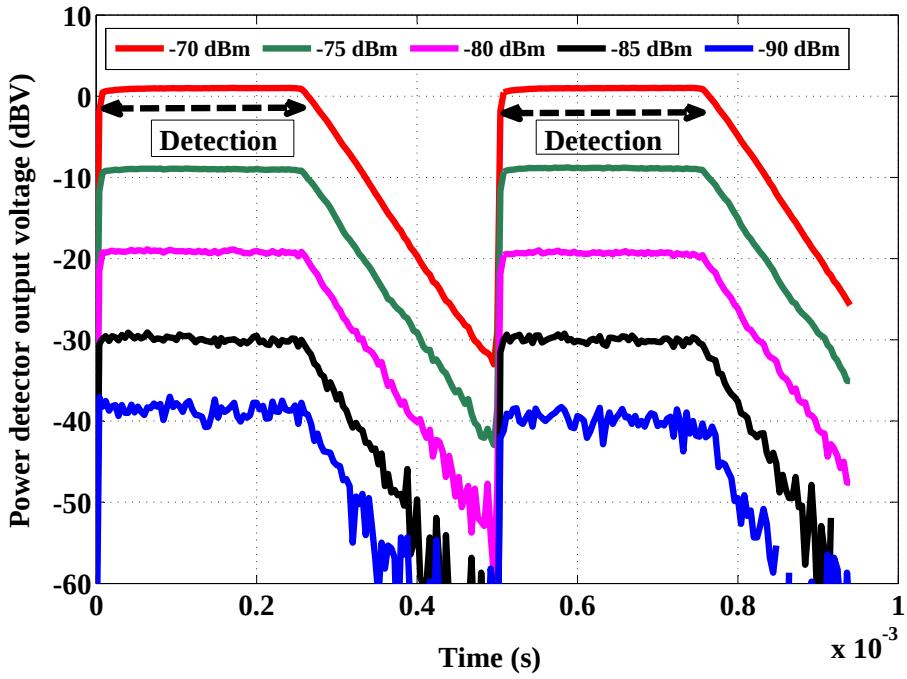


Figure 6.13: Power detector output with input signal power supplied from a signal generator.

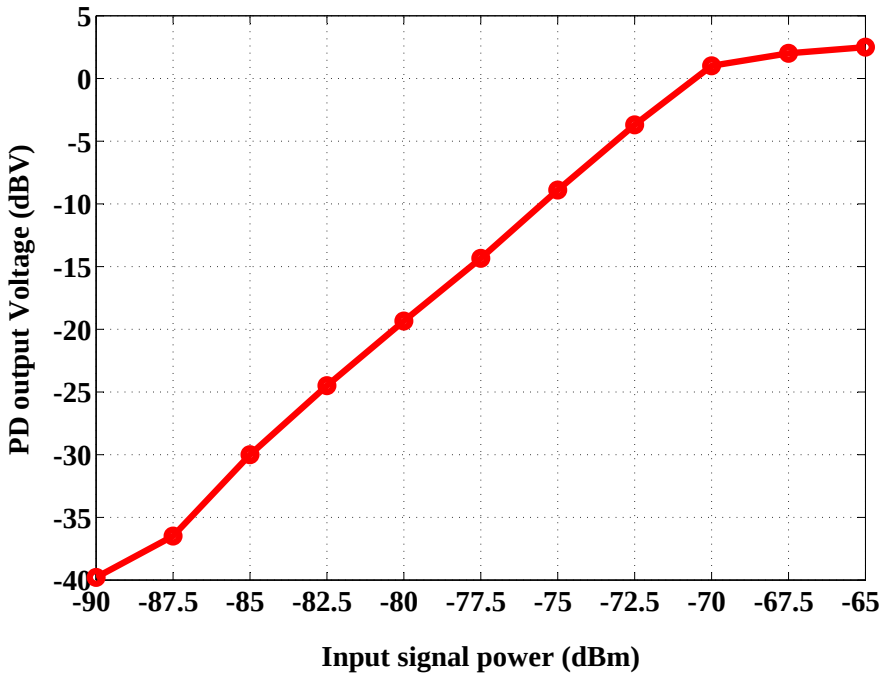


Figure 6.14: Power detector output with input signal supplied from a signal generator.

isolation of the PD from the receiver chain and avoiding loading the receiver gain stage output and lowering the receiver gain. In addition, an amplifier was added after the main PD output to amplify the very low output voltage at the PD output. This amplifier shared the same input stage with the calibration amplifier. The shared input stage reduces an offset due to uncalibrated offset on the added amplifier.

Measurement results show that the PD circuit is capable of detecting the expected SKA-receiver input power specified in Table 1.3. The lowest noise power that the PD can detect is -39.6 dBm with a power detection range of from -39.6 dBm to -20 dBm. The total power consumption of the PD was about 1.5 mW.

Chapter 7

Conclusions and future work

7.1 Thesis summary

This thesis presented two low-power and broadband linear-in-dB VGA circuits and a high-sensitivity broadband analog self-calibrated RMS PD circuit for use in an SKA radio telescope receiver. The VGA circuit with an active inductor load and the self-calibrated PD circuit achieved the specifications shown in Tables1.2 and 1.3. To achieve these performances, many different design approaches were investigated.

In Chapter 2, broadband VGA topologies were reviewed and the transconductance-tunable VGA topology was selected because of gain-independent bandwidth and suitability for broadband applications. Approaches for realizing a linear-in-dB function were discussed and the pseudo-exponential approximation function was selected due to its simple format and ease of realization. Then, the bandwidth extension techniques were investigated and finally a shunt-peaking technique was used in the VGA for extending the VGA bandwidth.

In Chapter 3, an ST 65 nm CMOS low-power-consumption linear-in-dB VGA with transconductance-tunable topology was designed and verified experimentally. This VGA achieved a variable gain range of 26 dB and a -3 dB bandwidth of 1.15 GHz while consuming 1mW. This VGA met most of the requirements for the SKA application except for the bandwidth and gain error. The second VGA with a shunt-peaking bandwidth-enhancement technique and a linearity improvement technique was designed and fabricated in TSMC 65nm CMOS technology. The measurement results showed a variable gain range of 32 dB and a linear-in-dB range of 28 dB while having a maximum gain deviation of at most ± 1 dB from the ideal linear-in-dB behavior, a -3 dB bandwidth of 2.1GHz and consumed 1.1 mW. Both input reflection coefficient, S11, and output reflection coefficient, S22, were less than -10 dB up to 4.2 GHz. Comparison of this VGA with other publications was summarized

in Table 7.1 .

In order to design an RMS PD for the SKA application, the possible power detection methods were reviewed in Chapter 4. Advantages and disadvantages of each detection method were analyzed. Finally, MOSFET square-law behavior, which has more advantages than other techniques, was selected as the power detection method in this work. Monte carlo simulation results of one of the PD circuits based on the square-law behavior were reported, showing that mismatches between PD components caused significant offset in the PD output. This offset cannot be tolerated in very high sensitivity PDs without any mismatch compensation.

A high sensitivity analog self-calibration RMS power detection circuit using the MOSFET square-law characteristic was proposed in Chapter 5. Self-calibration using transistor bulk terminals to adjust the PD input transistor threshold voltages was proposed to compensate all input-referred offset. In contrast to conventional auto-zero amplifier compensation, the proposed compensation method can largely remove the charge injection effects, by moving charge injection terminals to the low gain nodes. This PD, fabricated in TSMC 65 nm CMOS, achieved a sensitivity of -48 dBm and a -3 dB bandwidth of 1.8 GHz, which covers the mid-frequency range of SKA. The power consumption was 1.2 mW. The PD performance and the comparison of the PD with other published circuits were summarized in Table. 7.2.

Chapter 6 discussed the SKA receiver design in which the PD was embedded. When the PD was embedded in the receiver, an amplifier was added after the PD circuit to increase the output signal strength. Layout design of the receiver was discussed in Section 6.2.2. The measured results of the PD in the SKA receiver showed an input detection range from -39.6 dBm to -20 dBm with maximum error of 0.6 dBV at the PD output. The power consumption of the PD was 1.5 mW.

Table 7.1: Performance of two proposed VGA in this work and comparison with other published designs

Parameters	Spec.	**VGA I**	**VGA II**	[22]	[54]	[76]	[77]
Power Supply	1.2 V Max.	**1.0 V**	**1.0 V**	1.8 V	1.0 V	1.8 V	1.8 V
CMOS Process	65 nm	**65 nm**	**65 nm**	180 nm	90 nm	180 nm	180 nm
Upper 3dB freq. (GHz)	1.4	**1.15**	**2.1**	900	2.2	2	2.2
IP1dB (dBm)	-35	**-25~-32**	**-22**	-59~-11	-55~-15	N/A	-5
Power (mW)	5	**1**	**1.1**	11.4	2.5	40	19.8
Gain range (dB)	-10~10	**-30~-5 (0.7 GHz) -34~-8 (1.4 GHz)**	**-12.5~16**	-39~55	-10~50	-16~34	-13.5~13.5
S11 (dB)	<10	**<10**	**<10**	N/A	N/A	N/A	N/A
Gain error	<1dB	**±2dB**	**±1dB**	N/A	N/A	N/A	N/A
Linear-in-dB	Yes	**Yes**	**Yes**	Yes	No	No	Yes

Table 7.2: Performance of the proposed PD and comparison with other published designs

Parameters	**This work**	[28]	[24]	[25]	[27]	[26]
Process (CMOS)	**65 nm**	65 nm	130 nm	130 nm	130 nm	40 nm
Sensitivity (dBm)	**-48**	-25	-35	-33	-39	-10.5
Detection range (dB)	**37**	25	20	43	20	32.5
Operating frequency (GHz)	**0.5-1.8**	60	0.125~1.4	16	3.1-10.6	5
Linearity error for specified input range	**±0.95dB for 37dB ±0.5dB for 29dB**	N/A	±0.5dB for 18dB	±1dB for 43dB	±2.9dB for 20dB	±0.6dB for 32.5dB
Power consumption (mW)	**1.2**	N/A	0.18	35.2	10.8	0.349
Circuit area (mm^2)	**0.036**	N/A	0.013	0.75	0.36	0.009
Calibrated	**Yes**	No	No	No	Yes	No
Measured	**Yes**	No	Yes	Yes	Yes	Yes
Inputs/Outputs	**D/D***	D/S*	S/D*	S/S*	D/D*	D/S*

* D: differential, S: Single-ended

7.2 Future work

This thesis presents two linear-in-dB VGA circuits for use in the SKA receiver. The accuracy of linear-in-dB range of the VGA is limited by the variable resistance. To further increase the range, the resistor linear range can be increased by using different threshold transistors in parallel or by using the same type of transistors but controlling each transistor with different voltages to extend the transistor channel resistance linear range. Also the source-degenerated topology results in a low gain in each VGA stage. Increasing the gain of each VGA stage is another direction to be considered to improve the performance of the VGA.

Although the self-calibration power-detection circuit has very high sensitivity, it could be further improved by reducing the PD offset voltage due to the detection amplifier. The calibration system calibrated all the mismatches of the PD circuit and the calibration amplifier. The input-referred offset of the detection amplifier, which is different from the calibration amplifier although they shared same input stage transistors, was only partially calibrated due to the gain difference between these two amplifiers. The next step of the work is to reuse the calibration amplifier as a detection amplifier as well, and calibrate all the offset at the PD output to further increase PD sensitivity while keeping the PD output swing. Also the second-order harmonics of the input signal, which cannot be canceled at the PD output, need to be filtered out at the source of the PD input transistors. Otherwise, the DC operating points of the power detector change with input power and result in sensitivity decreasing due to the different threshold voltages between PD RF input transistors and DC reference transistors.

Twelve of the SKA receivers described in Section 6 are being prepared for testing in an advanced focal array demonstrator [78, 79] to verify its suitability for radio astronomical applications. Once successfully verified, the receivers will need to be prepared for a larger volume production for a performance verification on the SKA antennas. While the receiver

already achieves very low noise temperature, it may also be of interest to investigate the cooling of the receiver to improve its noise even further.

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Appendix A

Equivalent threshold voltage derivation

Fig. A.1 shows a circuit unit with two parallel transistors with different threshold voltage. The object of discussion is to derive an equivalent threshold voltage, which can use as both transistors threshold voltage. Assume the same sized transistors M_1 and M_2 have threshold voltage of V_{t1} and V_{t2}, thus the currents flow through M_1 and M_2 are I_1 and I_2,

$$I_1 = k_n \left(\frac{W}{L}\right)_{1,2} (V_{GS} - V_{t1})^2, \tag{A.1}$$

$$I_2 = k_n \left(\frac{W}{L}\right)_{1,2} (V_{GS} - V_{t2})^2. \tag{A.2}$$

For simplification, the channel length modification effect is ignored. The total current, I_D, is

$$\begin{aligned} I_D &= I_1 + I_2 \\ &= k_n \left(\frac{W}{L}\right)_{1,2} \left[(V_{GS} - V_{t1})^2 + (V_{GS} - V_{t2})^2\right] \end{aligned} \tag{A.3}$$

Assume there exists an equivalent voltage, V_{T1}, for both M_1 and M_2, that with the same bias voltage V_{GS}, the total current flow through M_1 and M_2 can be the same as with different

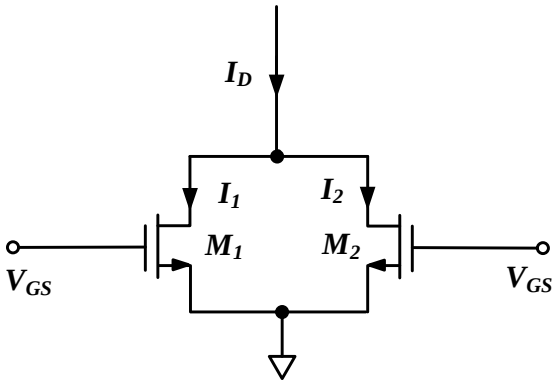

Figure A.1: Two parallel transistors with different threshold voltages

threshold voltage V_{t1} and V_{t2} for M_1 and M_2

$$I_D = 2k_n \left(\frac{W}{L}\right)_{1,2} [V_{GS} - V_{T1}]^2 . \tag{A.4}$$

Comparison of (A.3) to (A.4) gives that

$$2\,(V_{GS} - V_{T1})^2 = (V_{GS} - V_{t1})^2 + (V_{GS} - V_{t2})^2 . \tag{A.5}$$

Rearrange (A.5) results in

$$2\,(V_{GS} - V_{T1})^2 = 2V_{GS}^2 - 2V_{GS}\,(V_{t1} + V_{t2}) + \left(V_{t1}^2 + V_{t2}^2\right) \tag{A.6}$$

and

$$V_{T1} = V_{GS} - \sqrt{V_{GS}^2 - V_{GS}\,(V_{t1} + V_{t2}) + \frac{1}{2}\left(V_{t1}^2 + V_{t2}^2\right)}, \tag{A.7}$$

which is the equivalent threshold voltage for both M_1 and M_2.