UNIVERSITY OF CALGARY

Optimization of Voltage Steps in Cascaded H-Bridge Inverters

by

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A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE

DEGREE OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

CALGARY, ALBERTA

SEPTEMBER, 2008

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UNIVERSITY OF CALGARY

FACULTY OF GRADUATE STUDIES

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Abstract

In this thesis the design of multilevel cascaded H-bridge inverter topologies that can reduce harmonic distortion in the output waveform is investigated. The harmonic reduction methods investigated may be applicable to the integration of renewable energy sources in an electric utility power system. In multilevel inverters, a reduction in total harmonic distortion can be achieved by increasing the number of levels in the inverter output staircase waveform. The two approaches investigated avoid the use of an increased number of dc voltage sources or active semiconductor components. Both techniques are analyzed and harmonic equations are derived. Also presented is a gradient based optimization to determine the switching instances of transistor gating functions in order to minimize total harmonic distortion of the inverter output voltage waveform.

Acknowledgements

I would like to express my sincere thanks to my supervisor Dr Ed Nowicki for his kind guidance and supervision throughout the work done in this thesis.

My thanks are also due to my fellow students Nacer Benaifa and Hussien Bierk at the University of Calgary for their help and assistance during the preparation of this work.

Dedication

To my beloved family

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List of Symbols

Symbol	Definition
AC	Alternating current waveform
DC	Direct current waveform
PWM	Pulse width modulation
Vdc	Value of dc voltage source
THD	Total harmonic distortion
Vi	Value of the ith voltage source
H(1)	Peak value of the fundamental
RMS	Root mean square value of an ac waveform
θi	The ith switching angle in the first quarter of a staircase waveform
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate commutated thyristor
GTO	Gate turn-off thyristor
AI	Artificial intelligence
NN	Neural network
SPWM	Sinusoidal pulse width modulation
IPD	In-phase disposition modulation
POD	Phase opposite disposition modulation
APOD	Alternative phase opposite disposition modulation
THPWM	Third harmonic pulse width modulation
DSP	Digital signal processor
EMI	Electromagnetic interference
ASD	Adjustable speed drive
dv/dt	Rate of change of the voltage with time
VAr	Reactive power regulation
Vai	The output voltage of the ith H-bridge circuit
v(t)	Output voltage of the multilevel inverter
Si	The ith switch in a multilevel inverter
M	The total number of dc voltage sources in the multilevel inverter
H(n)	Amplitude of the nth harmonic of the waveform
ω	Angular frequency of a sinusoidal waveform
CPU	Central processing unit
PIC	The microcontroller used in the practical set up of the system
RISC	Reduced instruction set computer
EEPROM	Electrically erasable programmable read only memory
CMOS	Complementary metal oxide semiconductor

RAM	Random access memory
di/dt	Rate of change of the current with time
C	Capacitor
L	Inductor
R	Resistor
.m	Extension for executable MATLAB files

Chapter One: Introduction

1.1 Developments in Power Electronics and Renewable Energy Sources

Power electronics is concerned with the system engineering of power converters that contain semiconductor switching components. A power converter transforms voltage and/or current waveforms from one form (e.g. low or high ripple dc, low or high frequency ac, square or sinusoidal ac, etc.) to another form [1]. Over the past fifty years there has been rapid growth in power electronics research, as new high power, light weight; high efficiency power semiconductor components have replaced many of the older rotary machine power converters and heavy bulky transformers and inductors. The growth of the power electronics industry is likely to grow more rapidly in the foreseeable future [2]. Research work in the power electronics discipline, and industry applications of high power converters, are gaining more attention and support from community, industry and government institutions, especially as related to renewable energy sources such as biomass electric power generation, photo-voltaic (solar) cells, and wind electric power systems that employ novel rotary generators [3].

The field of high power semiconductor technology and related applications plays a great role in industry and our everyday life. Processes, appliances and vehicles that were once primarily mechanical in nature are now moving toward hybrid electro-mechanical designs, or in some cases, all-electrical designs. Not long ago, active solar cells were quite costly and considered useful for limited applications such as satellites orbiting the

earth. However, achievements in semiconductor solar cells have made it possible to introduce higher efficiency and lower cost components. A typical commercial solar panel today has an efficiency of about 20% at a retail cost of approximately $5000 per kW. Recently, a 40% efficiency solar panel was introduced which could lead to photovoltaic systems that can produce energy at a cost of around 10 cents per kilowatt-hour[1]. Wind electric power generation is becoming accepted as the most economic and environmentally sensitive form of alternative energy (though environmental issues require a balanced multi-faceted solution). One important role of power electronics in renewable energy systems is the conversion of dc voltage or current into near-sinusoidal ac power. In some cases, such as wind electric power, a semiconductor based rectifier is employed as a front-end power converter to create a dc-link. In particular, power electronics is finding applications in the conversion of electrical power from active solar panels or wind generators for the purpose of integrating that power into an electric utility grid. Such an application, sometimes referred to as distributed generation, is gaining popularity around the world, in Canada and in Alberta.

Projects exploiting natural energy resources are receiving both national and international attention in recent years. Right now, Great Britain is planning to use the tidal sea waters as an alternative source of energy[2]. Project planners hope this will be the basis for more projects perhaps with a goal of obtaining 20% of the country's need of electrical power

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[1] "Solar Cell Breaks the 40% efficiency Barrier" Renewable Energy World.Com online, Dec. 7 2006 http://www.renewableenergyworld.com/rea/news/story?id=46765&src=rss

[2]The Rise of British Sea Power, *The Independent*, UK, 23 March 2008, http://www.independent.co.uk/environment/green-living/the-rise-of-british-sea-power-799630.html

from a marine source. Here in Calgary, ENMAX is working on some projects, including wind powered electrical generation, which can increase "the propagation of green technology", as stated by the president of the company[3].

As more "green" electric power sources are being developed, one of the key technical issues is the research and development of high-performance, efficient, reliable, and cost effective means to convert power from a dc voltage (as is available from some alternative energy sources) into an ac power form, capable of being connected to the ac power grid, or driving off-line loads such as ac motors or appliances. This thesis addresses the need for high performance dc to ac power converters.

1.2 Harmonics in Power Systems

The system that converts power from a dc form into an ac form is the power inverter [1]. Much research work has been performed to improve the basic inverter structure or enhance the quality of the output waveform of these inverters. Among the many inverter structures available in the inverter family is the multilevel inverter. The work in this thesis is devoted to the improvement of the techniques used in multilevel inverter design to reduce the harmonic content of the output waveform of these inverters. Ideally, the output of an inverter should be purely sinusoidal, but in practice the power waveform contains unwanted frequency components.

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[3] *Schulich Engineer*, Fall 2007.

Motors, electronic equipment and appliances are affected differently by harmonics; depending on their internal circuitry and method of operation. For example, incandescent lights and most types of household heaters and stoves are not affected at all[4]. On the other hand, induction motors windings can be overheated by harmonics, causing degradation of insulation and loss of life. Harmonics in an electrical grid system may overload electrical power distribution equipment; like transformers, and resonate with power correction capacitors and are responsible for other undesirable effects [4].

The IEEE 519 Standard gives specifications for accepted levels of harmonics in power systems. For example, according to this standard [4], a maximum of 5% Total Harmonic Distortion in a given voltage supply is regarded acceptable in the petrochemical industry, with no single harmonic exceeding 3% of fundamental. The IEEE 519 Standard and emerging standards provide industry and academia with motivation to improve the quality of ac power inverters.

With recent advances in the field of multilevel inverters [1,3] it is possible for multilevel inverters to meet the IEEE 519 Standard with fewer dc sources. In this thesis we investigate these recent advances and provide harmonic analyses and suggest a gradient based technique to optimize the gating function of the transistors in a multilevel inverter with the objective of minimizing total harmonic distortion (THD).

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[4] "Harmonic Distortion in the Electric Supply System" University of Wollongong, Integral Energy Technical Note 3, March 2000.
http://www.elec.uow.edu.au/iepqrc/files/technote3.pdf

1.3 Thesis Outline

Following Chapter One, the thesis is divided into four more chapters. Chapter Two presents a literature survey of the main research trends in the field of the multilevel inverter design. The various improvements and advances in design, topologies, modulation techniques and harmonic reduction procedures are reviewed. The three main topologies are introduced in brief. Modulation techniques are reviewed in general. Advantages and applications of the multilevel inverter are introduced. No mathematical treatment of the subject is given in this chapter.

In Chapter Three, circuit details and mathematical analysis of two techniques [1,3] are presented (independently derived by the author, but also known in the literature). The main harmonic analysis equations and mathematical details to minimize harmonic distortion are described. Derivation of the harmonic equations for the presented techniques and simulation results done using MATLAB are given. The search for the values of angles that give minimum THD is presented using a gradient search technique.

Chapter Four provides details of the practical implementation of the proposed system. The implementation is done using bipolar transistors as switches and a microcontroller to activate and deactivate semiconductor switching operations. Experimental results are shown and compared to theoretical expectations.

Chapter Five presents the conclusions of the thesis along with suggestions for possible future work.

Chapter Two: Literature Review

2.1 Introduction

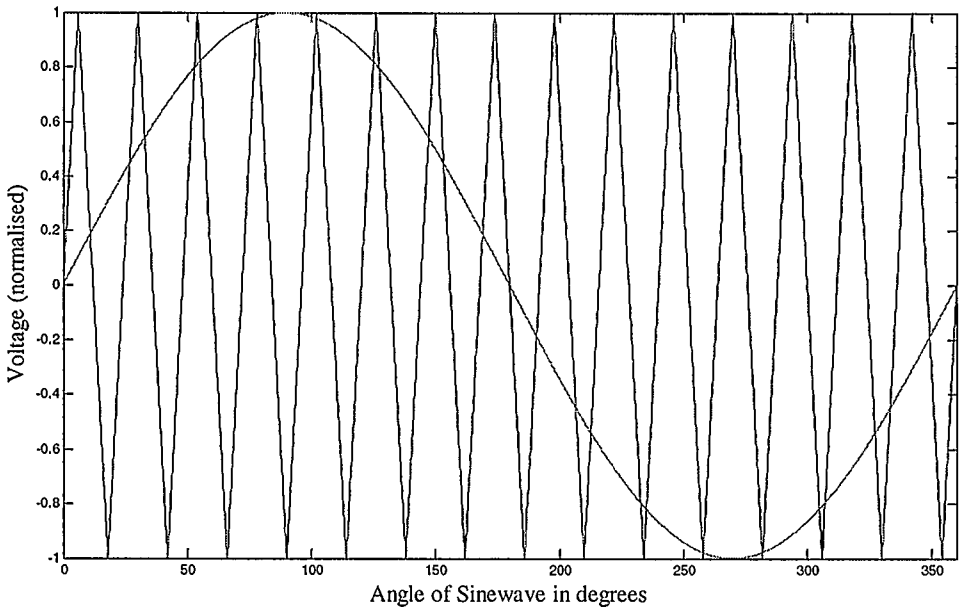
Multilevel inverters were introduced to industry in the early 1980s, although the concept of these converters was developed earlier in the 1970s [1]. The general concept is based on using a high number of active components to achieve power conversion in small voltage steps [2]. Since their first introduction, many design structures, topologies and modulation techniques have been devised as advancements to improve the performance of these power converters. What follows in this chapter is a look at the research work done by others on this kind of converter as improvements to their basic operation. More details on some of the topologies and techniques used are given in the next chapter. It is worthwhile to begin with some notes about the terminology used in the literature. The term inverter is used to define a circuit that converts a fixed dc voltage to an ac voltage (single or three-phase) with variable magnitude and frequency as used in motor drives, or with relatively constant magnitude and fixed frequency as might be used in grid-tie applications [3]. On the other hand, the term converter is sometimes used (especially in Europe) to refer to a circuit that could operate in an inverter or rectifier mode [1]. Below are definitions of two-level and multilevel inverters.

2.2 Two-Level and Multilevel Inverters

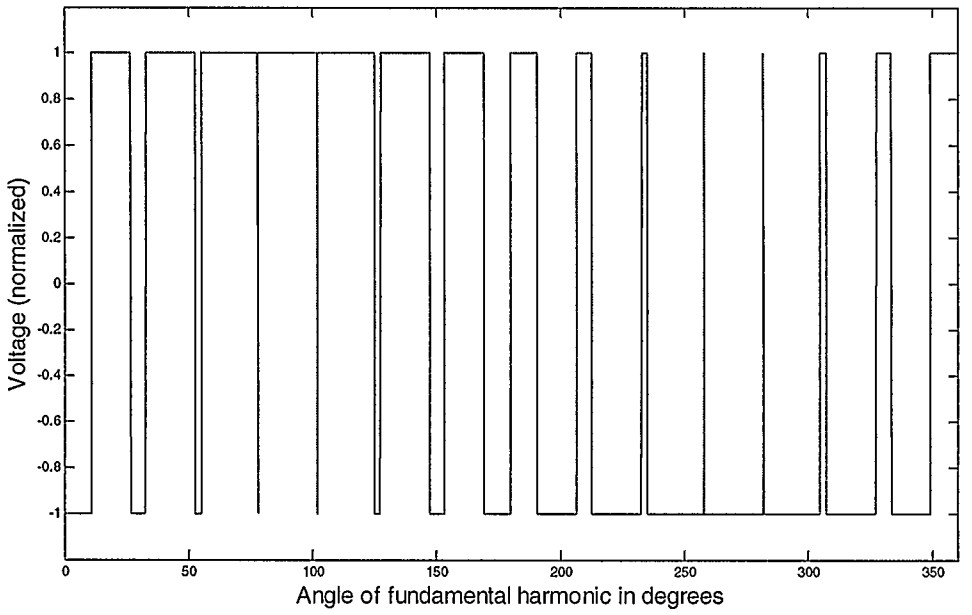
The term multilevel inverter is used in contrast with the two-level inverter. Fig. 2.1-a shows the signal waveforms related to the generation of the output waveform of a

conventional two-level inverter [4]. The technique used here, as is commonly used in industry, is pulse width modulation (PWM). The sinusoidal (reference or modulating) waveform is compared with a triangular (carrier) waveform. When the sinusoidal signal is greater than the triangular waveform, the output of the inverter is set (switched) to be equal to a constant dc voltage (Vdc), usually taken from a battery or a capacitor. When the magnitude of the sinusoidal signal is smaller than that of the triangular signal, the output of the inverter is set to be equal to the negative value of the same constant dc voltage (-Vdc). This process will yield the waveform shown in Fig. 2.1-b. The fundamental frequency component of this output waveform is the same as the sinusoidal modulating waveform. Actually, a harmonic-free sinusoidal component at the output of the inverter is the ultimate goal of the power conversion process. However, this sinusoidal component is usually distorted by harmonics due to the switching process. These harmonics will be "pushed up" to the higher end of the output spectrum by the carrier frequency, which is usually kept large enough for the harmonics to be filtered out by the appropriate filtering components. It is seen from the figure that the instantaneous value of the output waveform of the inverter alternates between the two dc values throughout one sinusoidal cycle of the fundamental sinusoidal reference waveform.

The total harmonic distortion (THD) is one of the criteria used as an indicator of the harmonic contents of a waveform. If H(1) is the peak value of the fundamental, and H(i) designates the peak value of the *i*th harmonic; then THD can be obtained using the following formula [4]:



(a)



(b)

Fig. 2.1: PWM technique to generate a sinusoidal signal. (a) output generating process (b) output voltage waveform.

$$THD = \sqrt{\frac{\sum_{i=2}^{\infty}\{H(i)\}^2}{\{H(1)\}^2}} \quad (2.1)$$

As the name implies, the output waveform of a multilevel inverter can have three voltage levels or more. A three level inverter has an output waveform that has one of the following voltage levels: Vdc, 0 or -Vdc. A quasi-square wave, or modified square wave as it is called in industry (common in sub-kilowatt inverters), is an example of a possible output of such an inverter [5]. A more advanced multilevel inverter output waveform is shown in Fig. 2.2. This is an example of a five level waveform. In the positive half cycle the output waveform is switched to a value, say V1 at an angle θ1, then at angle of θ2 the output is switched to V1+V2, where both values of V1 and V2 can be taken from two dc voltage sources or two capacitors. The values of V1 and V2 can be equal in magnitude, or they can have different values. The method with which this kind of signal is generated depends on the topology and structure of the inverter circuit. Many variations of switching angle values, number of voltage levels and specific values of the dc voltage sources contribute to the different design approaches and techniques used in the literature. Among the many research ideas and design techniques pursued so far, the work that is of interest to the research done in this thesis can be categorized into the following groups: the work done to introduce new topologies and structures, the research achievements to reduce harmonic contents of the output waveform; which is done either by reduction of the overall harmonic contents or by selective harmonic elimination

approaches (which intend to eliminate a specific number of harmonic frequencies rather

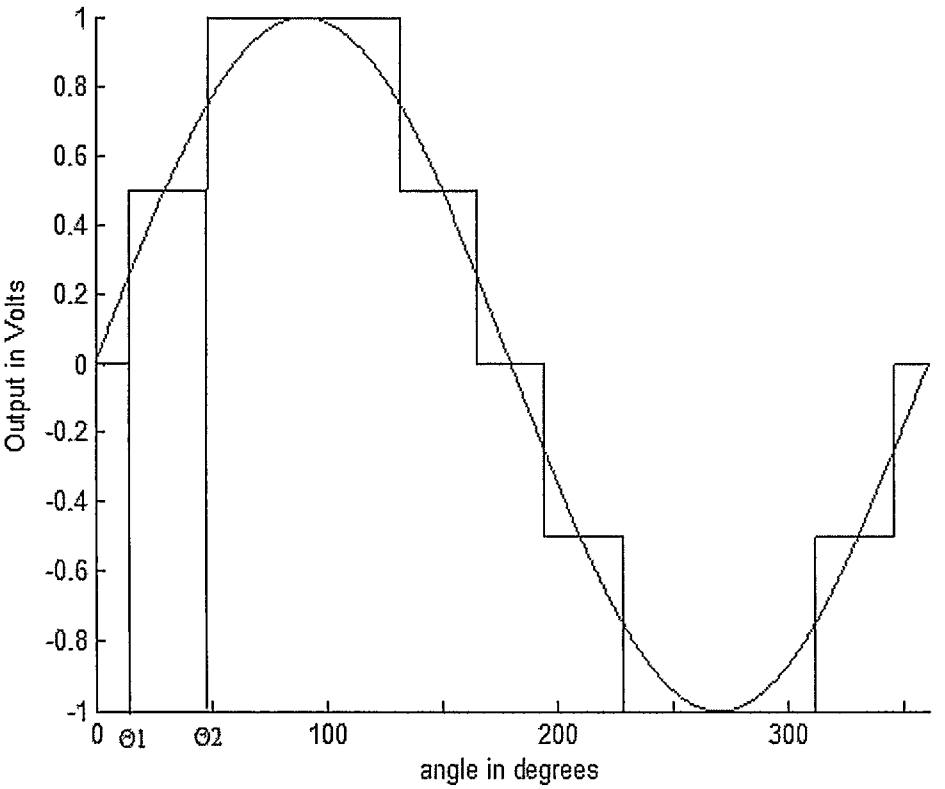


Fig. 2.2: Typical waveform of a multilevel inverter output (Voltage is normalized)

than reducing all the harmonic as a whole), modulation techniques, and the advantages of multilevel inverters. These subjects are addressed in the following sections.

2.3 Topologies and Structures of Multilevel Inverters

The early research work done by Nabae, Takahashi and Akagi [6] is a turning point in the improvement of multilevel inverters for practical applications [7 - 9]. The authors describe a three level converter that consists of two capacitor voltages in series and use the center tap as the neutral point. What they describe as neutral-point-clamped PWM

inverter is the basis for the diode-clamped topology of the multilevel inverter design. The diode-clamped topology can be used for a higher number of levels in the output waveform [7]. For a few years after 1980 no interest was shown in the literature in multilevel structures, but in the late eighties there was more research work done on these power converter systems [9].

Meynard and Foch described what they call "A novel versatile multilevel commutation cell" in 1992 [10]. The structure was introduced as being safer, simpler in control requirements and delivering purer output waveforms. The authors show how the new technique can be used in inverters and generalize its use to any number of switches. What was introduced in their work as a multilevel commutation cell was the basic structure for the flying capacitor multilevel inverter topology [1].

The third major improvement to the structure of the multilevel inverter is the cascaded-inverter with separate dc voltage sources developed by Marchesoni, Mazzucchelli and Tenconni [11-13]. It was reported also by Tenconi, Carpita and Bacigalupo [9], referring to their structure as the "modular converter", differentiating it from the other multilevel converter structures. This inverter was introduced as a topology that can avoid extra clamping diodes or voltage balancing capacitors. Each dc source is associated with a full-bridge inverter consisting of four switching devices. The ac terminal voltages of different level inverters are connected in series to constitute the ac output of the multilevel inverter. This topology requires the least number of components among all multilevel converters to achieve the same number of voltage levels.

In addition to these three basic topologies, other structures have been proposed. Many of the other topologies are not more than a minor modification to the original ones or they may use a combination of two or more of the basic topologies, which can be categorized as "hybrid" converter circuits [1]. One such structure consists of an H-bridge unit whose legs are made from diode clamped circuits [2], which is a combination of the cascaded H-bridge and diode clamped topologies. The "hybrid" term is sometimes used in conjunction with the use of different types of semiconductor switches in the same inverter topology. An example of that is the use of insulated gate bipolar transistors (IGBT) in the same inverter together with the integrated gate commutated thyristor (IGCT) for high-power applications [14]. This kind of design is tailored to multilevel inverters operating in a PWM mode, where some of the switching devices of the higher voltage cells have to operate at high frequency during some time intervals. The achievement is that the higher power cells operate at low frequency and only the lowest power cell operates with high frequency PWM. Another hybrid topology uses IGBTs, exploiting their voltage blocking capability, together with Gate turn-off (GTO) thyristors utilizing their switching speed and high voltage capabilities [15]. An attempt was made to give a unified definition to hybrid multilevel inverters as "those systems composed of several series-connected cells that present different dc voltage levels, modulation strategies, topologies, and/or semiconductor technologies operating in synergism" [16]. This definition was exemplified by a hybrid system that contains all three basic topologies in one inverter design. Another hybrid multilevel inverter for driving electric vehicles uses a single dc source at one level and capacitors for the rest of the levels [17].

This is done to overcome the difficulty of needing many dc sources for all the levels. Another topology was introduced concerning power requirements of the main circuit for a five level inverter that utilizes a special type of switch as an auxiliary component in the main power circuit [18]. The switch is inserted between the voltage source and the rest of the switching components in the circuit. The main goal of this configuration is to reduce the number of high power components in the inverter circuit.

Generally speaking, the hybrid techniques which use combinations of multilevel power converters give flexibility and versatility to the design structure of the system to fit the specific application it is intended to be used in. Finally, the symmetry property of these converters is worth mentioning. These converters can be classified according to the values of dc sources involved; if they are equal, the converter is called symmetric. If the dc sources used have different values, the term asymmetrical is used [19].

Other than the hybrid technology in multilevel inverters, specific kinds of techniques were sometimes developed to overcome certain drawbacks of the conventional approaches used in multilevel power converters. One approach uses a special kind of circuit that can charge a bank of capacitors in parallel and discharge them in series [20]. The main purpose of this topology is to overcome the requirements of separate dc voltage sources or a complicated capacitor-voltage balancing circuit for active power transfer. In another approach a fault diagnostic system based on artificial intelligence (AI) techniques is proposed [21]. The system uses neural network (NN) classification as a modeling tool and measures the output waveforms to identify the type and location of occurring faults

[22]. These efforts do not imply a real change in the basic topology design of these inverters; however they represent the progress in research work to improve the general design of these systems.

2.4 Modulation Techniques

Topologies and modulation techniques are sometimes very much related in multilevel inverter design to the extent that makes it difficult in some instances to differentiate between each other. However, two main modulation techniques can be found in most kinds of power converters: the non PWM techniques and the PWM techniques. The simplest and most obvious modulation scheme in a multilevel inverter system is the staircase (or step) modulation [3]. This is the one previously introduced and shown in Fig. 2.2; it is also known as the fundamental switching frequency modulation technique. Calculations can be done to find the specific values of the switching angles so as to minimize the harmonic contents of the resultant waveform. This is to be explained in more details later.

The method of PWM introduced earlier for the two-level inverter in Fig. 2.1-b can be extended to the multilevel concept. Carrara [23] developed the analysis of such a technique which is called sinusoidal pulse width modulation SPWM. To generate N odd levels of SPWM output, one modulating sinusoidal signal is needed, together with N-1 triangular carrier signals having the same frequency and amplitude and are aligned so that the bands they occupy are contiguous. The same number of carriers will be present above

and below the zero level. These carriers are compared instantaneously one by one with the sinusoidal signal in a fashion similar to bi-level PWM; the results of all the comparisons are added together to give the output multilevel PWM waveform. These carrier phases can be the same (in-phase disposition IPD), or they can be in phase for those above the zero value reference but in opposition with those below (phase opposite disposition POD), or they can be in opposition to each other alternatively (alternative phase opposite disposition APOD). For each of these three cases there is a different shape of output waveform. This description is actually for the kind of carrier based PWM technique categorized as the level shifted multicarrier SPWM technique. The other type of the SPWM technique is the phase shifted multicarrier modulation. In this kind of modulation all the carriers have the same frequency and amplitude, but there is a phase shift between any two adjacent carrier waves divided equally among the carriers to make a complete 2π cycle for all the phase shift angles. The modulating sinusoidal signal is compared with carrier waves to generate the output waveform as usual.

In addition to the popular SPWM technique, another modulation strategy also emerged. The third harmonic PWM (THPWM) technique injects a third harmonic into the reference sinusoidal signal equal to 25% of the fundamental [1]. This process makes the reference voltage somewhat flattened in the middle and is done to make it possible to increase the fundamental output voltage without having the reference signal exceed the level of the carrier signals (the condition is called over-modulation). This additional third harmonic will be present at the output phase voltage with the same phase and magnitude,

and it will be cancelled at the line to line voltage in a three phase system, which makes it applicable only in three phase systems [24]. Many other variations of the PWM technique have been reported in the literature [25-27]; they are mostly extensions of two-level and multilevel PWM techniques.

Most of the modulation techniques described so far can be used in different topologies of multilevel inverter design. However, a few exceptions have been reported [3].

2.5 Harmonics in a Multilevel Inverter Output

The output of a multilevel inverter, regardless of the modulation technique or topology used, is required to be a near-sinusoidal waveform free of harmonic distortion in the ideal condition, but this has never been the case. The desired sinusoidal output is distorted by higher order harmonics that are inherent in the output waveform due to the nature of the output generation process. Harmonic reduction is one of the main goals in the developments of any inverter design.

Two main trends can be observed in the literature regarding the harmonics problem in multilevel inverters. Harmonics can be minimized as a whole without emphasizing on specific frequency component, or a near-complete elimination of specific frequency components can be carried out [28, 29]. In the step modulation scheme, the switching angles of the staircase output waveform can be adjusted so as to minimize the harmonic content of the waveform. This can be done by running an exhaustive search method to

find the required angles, or by calculating the angles that will keep the area between the output staircase waveform and the sinusoidal desired output at a minimum [29]. Using this approach, it has been shown that for equal voltage steps of the staircase waveform, the optimal angles are found at the mean value of any two voltage steps. While for equal angle intervals and different voltage step values, the optimum angles are found to be at the mean value of any two corresponding angles. The criterion of equal area between the sinusoidal curve and the staircase waveform above and below the intersection point between the two has also been adopted [30]. Referring back to Fig. 2.2, an example of these two areas is the one below the sine wave trace and above the staircase between the angle values 0 and $\theta 1$, and the one above the sine trace and below the staircase after $\theta 1$ until they intersect at 0.5 V level before $\theta 2$. It has been shown that by using this equal area criterion, the fundamental of the staircase waveform can reasonably resemble the sinusoidal modulation waveform. However, by minimizing the total harmonic distortion (THD) of the waveform, no elimination of specific harmonics can be realized.

Elimination of selected harmonic frequencies from the output waveform is carried out by sacrificing the minimization of THD. It is done usually to remove lower order harmonics which are closer to the fundamental, and use filtering circuits to attenuate the higher order harmonics in the output stage of the inverter. This approach is strengthened by the fact that the triplen harmonics (i.e. the odd multiples of the third harmonic) are already not present on the line-to-line voltage in a three phase system [28]. One of the pioneering works in harmonic elimination was carried out by Patel and Hoft [31]; they introduced research on harmonic elimination in two and three level inverters with thyristor firing

circuits. They developed a technique to eliminate some of the harmonics in a two-level PWM inverter by chopping the basic square wave output a number of times, and a fixed relationship was derived between the number of chops and possible number of harmonics that can be eliminated. The problem is that there will be a number of equations that have to be solved to eliminate the harmonics. These equations are nonlinear and transcendental in nature and not easy to solve. They can be solved by a trial and error process, or by numerical techniques. For a three level PWM output, the method adopted was the generating (instead of chopping) of identical but opposite polarity pulse train in each half-cycle.

In the staircase modulation of the multilevel inverter, harmonic elimination can be achieved by solving a set of nonlinear transcendental equations resulting from the Fourier analysis of the output waveform. The number of these equations is equal to the number of switching angles in the first quarter of the staircase output waveform (the uprising positive part before $\pi/2$). The number of harmonics that can be eliminated is equal to the number of these equations minus one [32, 33]. For example, the number of equations for the waveform of Fig. 2.2 is just two, so only one harmonic can be eliminated in such a waveform. The solution of these transcendental equations is usually done by iterative methods. Many procedures to provide solutions to these nonlinear equations have been reported [34-37]. The problem with the numerical methods to solve the harmonic equations is that good initial guesses are required, moreover, solutions are not guaranteed. Usually the calculations of the values of the switching angles in stepped modulation is done off-line and stored in look up tables to be used in the control circuitry

of the inverter. Real time calculations are also possible and have been reported using a digital signal processor (DSP) to minimize the total harmonic distortion (THD) [38].

2.6 Advantages of Multilevel Inverters

As stated before, the multilevel inverter design enables converting of power in small voltage steps rather than operating the electronic switches between the two extreme voltage levels in the bi-level PWM approach. The switches of the subsequent levels of the circuit are connected in series across the peak output voltage and the voltage drop is shared among the switches in the different levels. This technique enables the inverter to be used in applications that need high power (larger than 1 MW) and medium voltage (2.3 kV to 6.9 kV, i.e. several kVs), where an ac drive in the megawatt range is usually connected to the medium voltage network [8]. However, this is achieved at the expense of a higher number of switching circuits realized by active components required to cover the range of the output voltage waveform. The usual structure of these inverter circuits consists of layers or multiples of switches for each level added to the output voltage. The multiple switches in the multilevel inverter in fact permit an extra degree of switching freedom. Each switch still has the same limited switching frequency, but the overall switching frequency of the multilevel inverter becomes a multiple of that of the individual switches [39]. In addition to that, the fundamental switching scheme of these inverters (when every switch is activated once in a cycle) enables the use of these inverters in applications where low electromagnetic interference (EMI) is required [40].

The cascaded topology of these converters can fit many of the needs of all-electric vehicles using onboard batteries or fuel cells to generate the sinusoidal waveform to drive the main traction motor [41]. Multilevel converters have been utilized also in the design of hybrid electric vehicles where a high voltage battery pack is used as an alternative power source and energy storage device to provide drive power during acceleration and reserve energy during vehicle braking [42]. The high volt-ampere ratings of the multilevel inverters make them uniquely suited to meet the high power requirements of heavy duty trucks and military combat vehicles (>250 KW). Development of electric drive trains for these large vehicles will result in increased fuel efficiency, lower emissions, and better performance [43].

Multilevel inverters can be used in adjustable speed drives (ASD) to overcome some of the problems related to this application. Conventional ASDs use the two-level PWM technique to generate a voltage with variable frequency and amplitude in motor speed control applications. Many problems can arise from the high dv/dt caused by this kind of PWM operation, such as motor bearing failure and motor winding insulation breakdown, in addition to other problems [43]. Multilevel inverters overcome these problems because their individual devices have a much lower dv/dt per switching.

The use of these inverters in active control of reactive power (VAr) has been also reported [44]. Static VAr generators using multilevel inverters have been widely used as reactive power controllers of power systems to replace the conventional VAr compensators that use transformers. Transformers are the most expensive part in the

system, need large area, encounter high losses, and are prone to failure. For these reasons, it is better to use multilevel inverters as a controlled reactive admittance and avoid the use of transformer based compensators. Recently, a cascaded multilevel-converter has been used to mitigate flicker; caused by feeder voltage fluctuation, in 40MVA electrical arc furnace and was successful in preventing problems in transmission and distribution systems [45].

One of the advantages of the cascaded multilevel inverter is its suitability for renewable energy sources. The cascaded multilevel inverter with its separate dc sources make it a good choice in applications that make use of renewable energy sources like wind turbines and photovoltaic cells [46]. These inverters are ideal for connecting to an ac grid with distributed energy sources composed of these renewable energy sources. This is a very important advantage in a time the world is seeking new sources of energy to save the environment and to compensate for the shortage in oil supplies and its increasing cost.

2.7 The Work Presented in This Thesis

It has been shown in this review chapter that one of the limitations of the multilevel inverter is the need for more components to increase the number of levels of the output waveform. Harmonic minimization in the output requires an increased number of output levels in the staircase waveform. A near-zero harmonic output can be achieved by having a very large number of levels in the staircase output; this requires a large number of isolated dc sources and an equivalent large number of active switching components. In

the next chapter we review two approaches to tackle this problem [1,3]. The first one increases the possible number of levels in the output waveform without the need to increase the number of active components or dc sources. This is achieved by introducing a specific switching sequence of the active components; some constraints on the magnitudes of the dc voltage sources are imposed though. Simulation results are shown and compared to the conventional approach [47]. The second proposed method introduces a switching scheme that increases further the number of levels of the output waveform keeping the same number of voltage sources and active switching components; more constraints on the dc voltage source values are imposed to make this possible. Simulation results are shown together with practical implementation results [48]. The next chapter deals with the theory related to the design requirements and harmonic analysis of the investigated techniques.

Chapter Three: The Investigated Techniques

3.1 Introduction

In this chapter, two techniques [1,3] are investigated that can minimize total harmonic distortion (THD) of the output waveform of the multilevel inverter. Both techniques (derived independently by the author) have been identified in the literature [1,3]. The topology adopted for these techniques is the cascaded H-bridge multilevel inverter structure. Both techniques increase the number of the staircase waveform levels of the inverter output without the need to increase the number of dc voltage sources or system components. To achieve that, the controller produces a specific switching sequence in each case. In doing this, some constraints on the values of the contributing dc sources are imposed. The details of these constraints depend on the specific requirement of each one of these two techniques. The first technique is included in the second one implicitly, i.e. the second one contains all the necessary requirements and procedures of the first one; in addition, it imposes more constraints on the values of the dc voltage sources and on their functioning nature to achieve the higher number of staircase levels in the output. A review of the conventional H-bridge multilevel inverter is given first; then details of both techniques are described with harmonic analysis and comparisons with the conventional approach.

3.2 The Cascaded H-bridge Voltage Source Multilevel Inverter Structure

These inverters use more than one dc voltage source and a combination of several semiconductor switches to generate an ac staircase voltage waveform. To obtain a higher number of steps for the output waveform, more voltage sources and semiconductor components are required for the system. Fig. 3.1 depicts the block diagram for such a system [1]. The power of the system can be driven from a number of separate dc sources such as batteries, or capacitors fed from dc sources, or separate renewable energy voltage sources [8]. An H-bridge switching circuit is associated with each dc voltage source. For the i-th H-bridge, the dc source voltage *Vi* is the input of the i-th H-bridge which has an output voltage of *Vai*. The total number of these bridges is *m* which is usually equal to the number of dc sources. The output voltage of the i-th H-bridge, *Vai*, can take one of three voltage values: $+Vi$, $-Vi$, or zero volts. The output voltages of the *m* H-bridge circuits are connected in series to be added together to generate the output waveform of the inverter circuit represented simply as *v(t)*.

Each H-bridge circuit contains four semiconductor switches, as shown in Fig. 3.2. The output voltage of the bridge, *Va*, can be made equal to $+V$ by turning on S2 and S3 while keeping S1 and S4 off. To make the output equal to $-V$; S1 and S4 have to be on while S2 and S3 have to be off. For a 0 volt output, S1 and S2 have to be off, while S3 and S4 on (or vice versa). Table 3.1 gives the switching conditions and the output of the bridge for each of these conditions [2], where a 1 means on (connected), and a 0 means off (disconnected). It can be noted that the switching condition of S1 is complementary to S3, and S2 and S4 are also operated in complementary fashion.

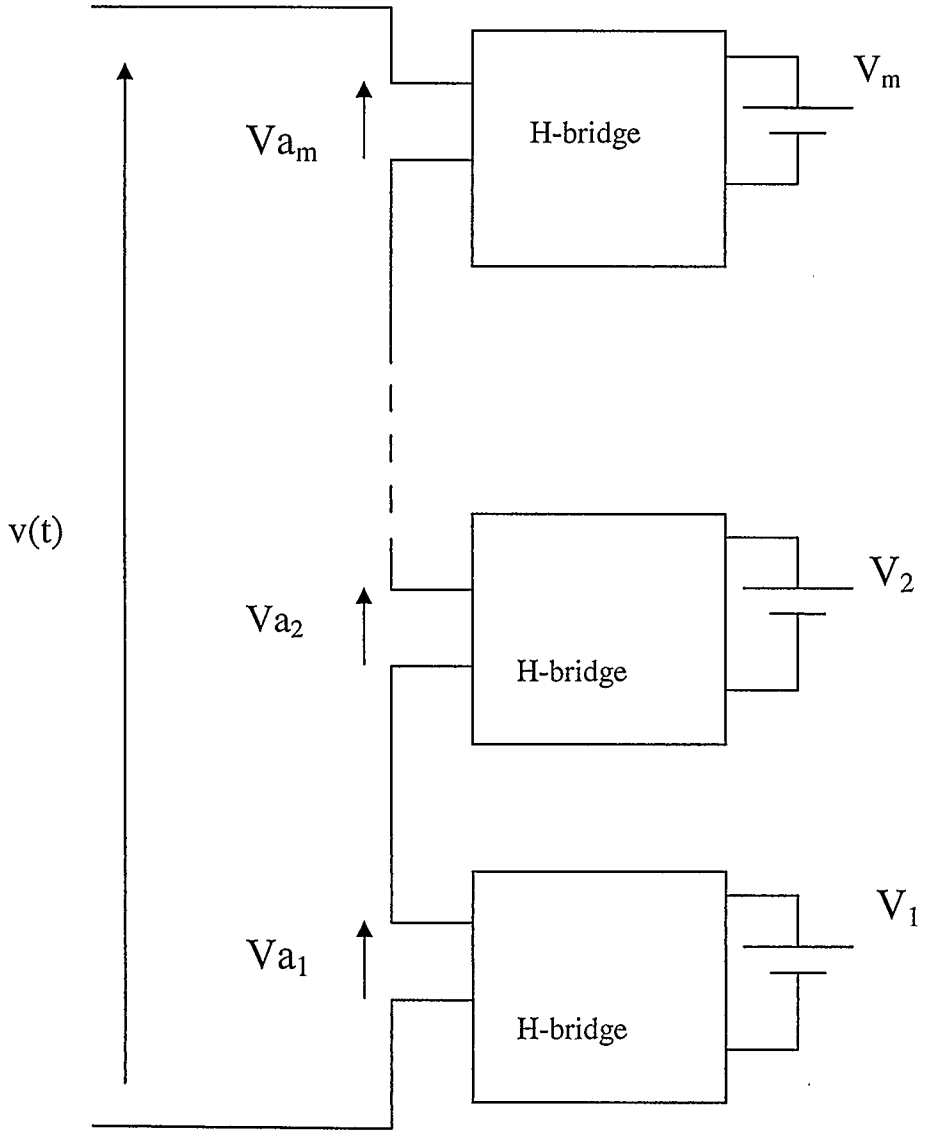


Fig. 3.1 Cascaded H-bridge multilevel inverter

The subsequent additions of the H-bridge circuit outputs generate the staircase waveform at the output of the inverter as shown in the waveform of Fig. (2.2), where this waveform can be generated by a two dc voltage source inverter. By properly selecting the switching

angles of the steps in the output waveform; (e.g. $\theta 1$ and $\theta 2$ in the waveform of Fig. 2.2), control of the harmonic contents of the output waveform can be achieved [1].

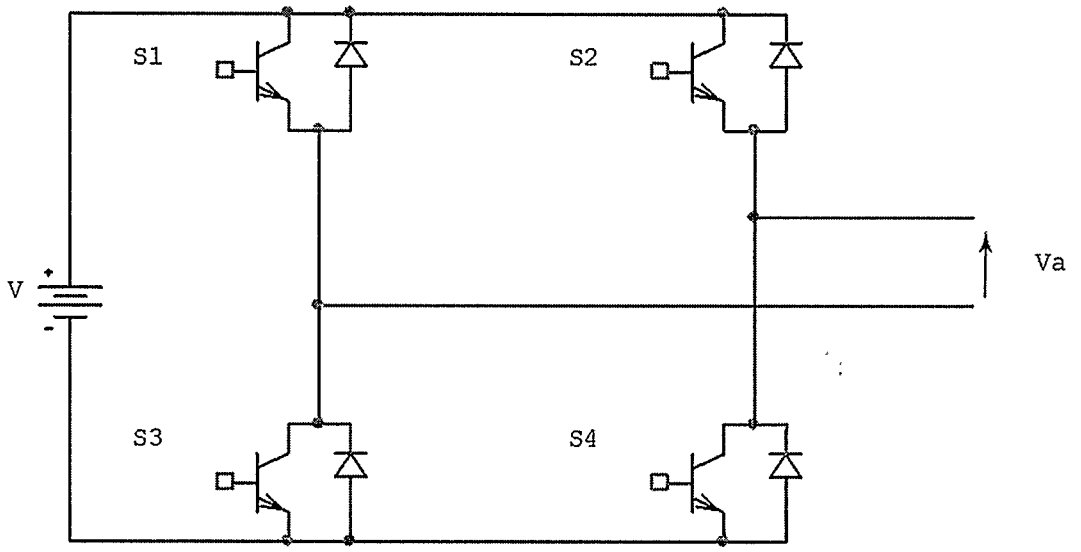


Fig. 3.2 The H-bridge switching circuit

Table (3.1) H-bridge switching states

Va	S1	S2	S3	S4
+V	0	1	1	0
-V	1	0	0	1
0	0	0	1	1
0	1	1	0	0

The number of levels possible with the conventional approach in generating the output staircase waveform is $2m+1$; where m is the total number of dc sources. This number

stems from the fact that each new level is generated by adding a new voltage source to the resultant waveform in every stage. Even with unequal voltage sources, there are still $2m+1$ staircase levels in the output waveform. With the conventional control of the cascaded H-bridge the only way to increase the number of levels in the inverter output waveform is to increase the number of dc sources and their associated H-bridge circuits.

3.3 The Technique of Single Polarity Voltage Addition in Each Half Cycle

The first method investigated here has the capability of increasing the number of levels without the need to increase the number of dc sources or the semiconductor switching components; it is done by following a specific switching pattern for the outputs of the H-bridge circuits. The basic concept is to add to the conventional levels all the possible arrangements of voltage additions with the same polarity in each half cycle. An example of how to do this can be given by studying the case of the two voltage sources illustrated in Fig. 2.2. The conventional values of the levels in the positive half cycle are *V1* followed by *V1+V2*. Whether *V1* is equal to *V2* or not would not change anything in the total number of levels of the waveform. An additional level in the positive half cycle of the waveform can be added to have a total of seven levels in the whole cycle of the output waveform. This can be done by adding the level of voltage that is equal to *V2* alone. The resultant waveform in the first quarter will consist of the levels *V1, V2* and *V1+V2*, and the same voltage values having negative polarities will be present in the second half cycle, in addition to the zero voltage level. This operation can be carried out for any number of dc voltage sources in the system; however, some conditions may be imposed

on the values of the dc voltage sources. These conditions can be deduced by inspecting the example of the two voltage sources given above and the cases of three or more sources. In order to increase the number of staircase levels, the value of *V2* in the two source example is constrained by *V2>V1*. However, for equal step values, *V2* has to be equal to *2V1*, so that the step voltage will be equal to *V1* for the three steps in the positive half cycle, where the step value here is used to designate the difference between two consecutive levels. The technique can be applied for non equal step values as well, but equal step values will well approximate the desired sinusoidal output. To formulate the constraints on the values of the dc voltage sources, it is assumed that there are *m* dc sources with a set of voltage values $\{Vi\}$, $i = 1, 2, .., m$. Each of these sources has a distinct voltage value, i.e.:

$$Vi \neq Vj, for\ all\ i\ and\ j \quad (3.1)$$

The dc source with the lowest voltage value will be given the notation *V1*, the next higher voltage source is *V2*, and so on. The highest value of the dc voltage sources in the system is *Vm*. This means

$$Vi < V(i+1), for\ all\ i \quad (3.2)$$

The other assumption imposed on the values of the dc voltage sources is:

$$V1 + V2 + \cdots + Vi \neq V(i+1), for\ all\ i \quad (3.3-a)$$

This assumption is essential when the number of dc sources is higher than two. The importance of this assumption can be understood by studying the case of three dc sources, i.e. by having *V3* in addition to *V1* and *V2*. After the three step levels of *V1*, *V2*

and *V1+V2*, the next level of the output voltage waveform will be *V3* alone; this value has to be different than the previous level, which is ensured by this equation. The same argument can be made when there are more than three voltage sources in the system. For more convenience, equation (3.3-a) can be put in a more appropriate form as follows:

$$V1 + V2 + \cdots + Vi < V(i + 1), for\ all\ i \quad (3.3 - b)$$

This form is for convenience more than for necessity. It is needed to make the level of *V3* higher than the level of *V1+V2* in the three source example; not lower than it. The same applies to examples with a higher number of voltage sources. However, the form (3.3-a) of this equation is sufficient for the technique to work.

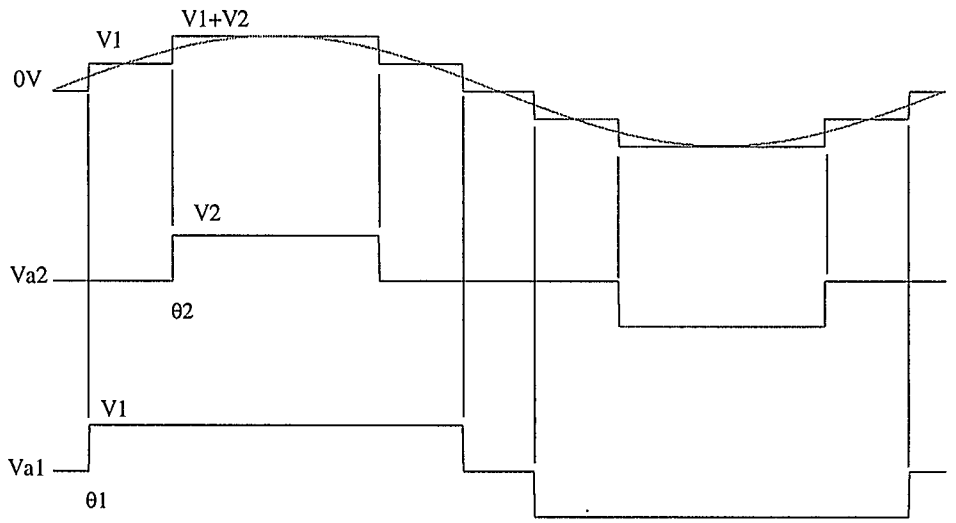


Fig. 3.3 Output waveform and switching pattern of Va1 and Va2 in the conventional approach

To illustrate how the technique works, the case of two voltage sources is presented here for the conventional and the current approach. Fig. 3.3 shows the output staircase

waveform in the case of the conventional technique together with the switching pattern of the H-bridge circuits (the square wave components are discussed in the next section). The two levels in the positive half cycle are *V1* and *V1+V2*, where *V2* is chosen here to be equal to *V1* for the equal step condition. Similar argument applies for the negative half cycle. The total number of levels is five. Fig. 3.4 depicts the output waveform and the variations of voltage outputs of the two H-bridge circuits *Va1* and *Va2* in the current technique. The additional two levels in this waveform is the $+V2$ and $-V2$ in the positive and negative half cycles, respectively. Here *V2* is chosen to be *2V1* for equal step values. It is possible to add these two more levels of *V2* alone since *V2* is higher than*V1*; according to equation (3.2). It is clear that the total number of levels for the whole cycle is seven and not five, as was the case in the traditional approach. For a total number of *m* dc voltage sources, the total number of levels obtained for the whole voltage cycle will be $(2^{m+1}-1)$ using the current technique; a considerable increase in the number of steps of the output waveform that will result in a great reduction in the harmonic distortion of the waveform, as illustrated below.

3.4 Harmonic Analysis of the First Technique

To study the harmonic contents of the output waveform, it is useful to find the equation of harmonics in the multilevel inverter first for the conventional approach to serve as a reference. In the waveforms of Fig. 3.3, the output staircase waveform is actually a resultant of the linear addition of two square waves as illustrated in Fig. 3.3; the number of square waves equal to the number of the stages (H-bridges) of the converter. The

harmonic content of this waveform is obtained by adding the harmonic contents of these two square waveforms. For a fundamental frequency of ω, and transition angles of $\theta 1$ and $\theta 2$ for the two square waveforms, the equation for Fourier series expansion of the original staircase waveform can be given as follows [1]:

$$v(t) = \frac{\sin(n\omega t)}{n} \frac{4}{\pi} \sum_{n\,odd} (V1\cos(n\theta 1) + V2\cos(n\theta 2)),\quad n = 1,3,5\ldots \quad (3.4)$$

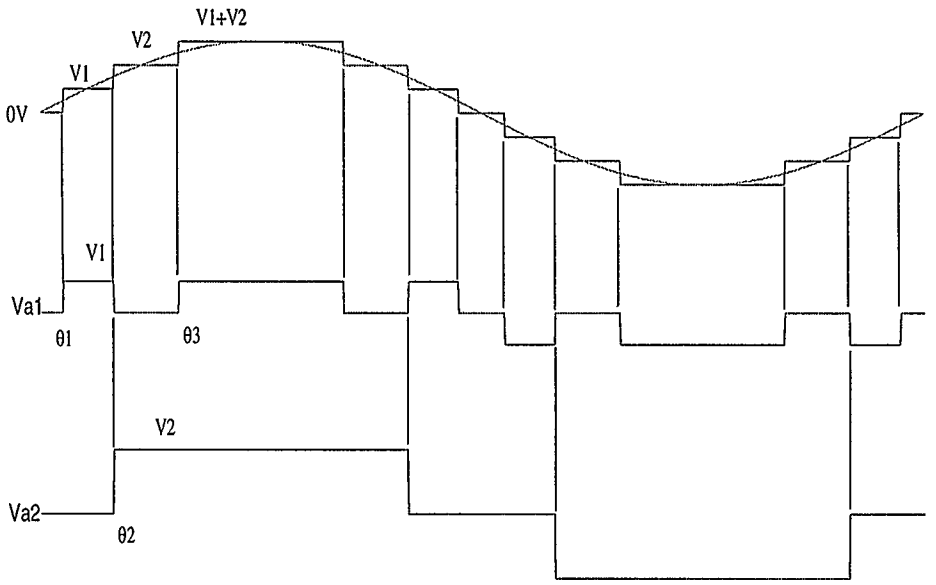


Fig. 3.4 Output waveform and switching pattern of Va1 and Va2 using the first technique

It is noted that the even harmonics are zero due to the quarter wave symmetry property of the waveform. If the number of steps is defined as the number of transitions (or angles) in the output waveform prior to $\theta=\pi/2$, then for m number of dc sources there will be m steps. The Fourier coefficients, $H(n)$, of the output waveform in this case can be given as [1]:

$$H(n) = \frac{4}{n\pi}[V1\cos(n\theta 1) + V2\cos(n\theta 2) + .. + Vm(\cos(n\theta m))]\ n = 1,3,5 \ldots \quad (3.5)$$

For equal dc voltage source values of V, equation (3.5) becomes:

$$H(n) = \frac{4V}{n\pi}(\cos(n\theta 1) + \cos(n\theta 2) + .. + \cos(n\theta m)),\quad n = 1,3,5 \ldots \quad (3.6)$$

Fig. 3.5 gives the spectrum of the five level waveform of Fig. 3.3 normalized to the first harmonic. The highest magnitude after the fundamental appears at the eleventh harmonic and equals 10.7% of the fundamental. The THD value is found to be 17.56 %.

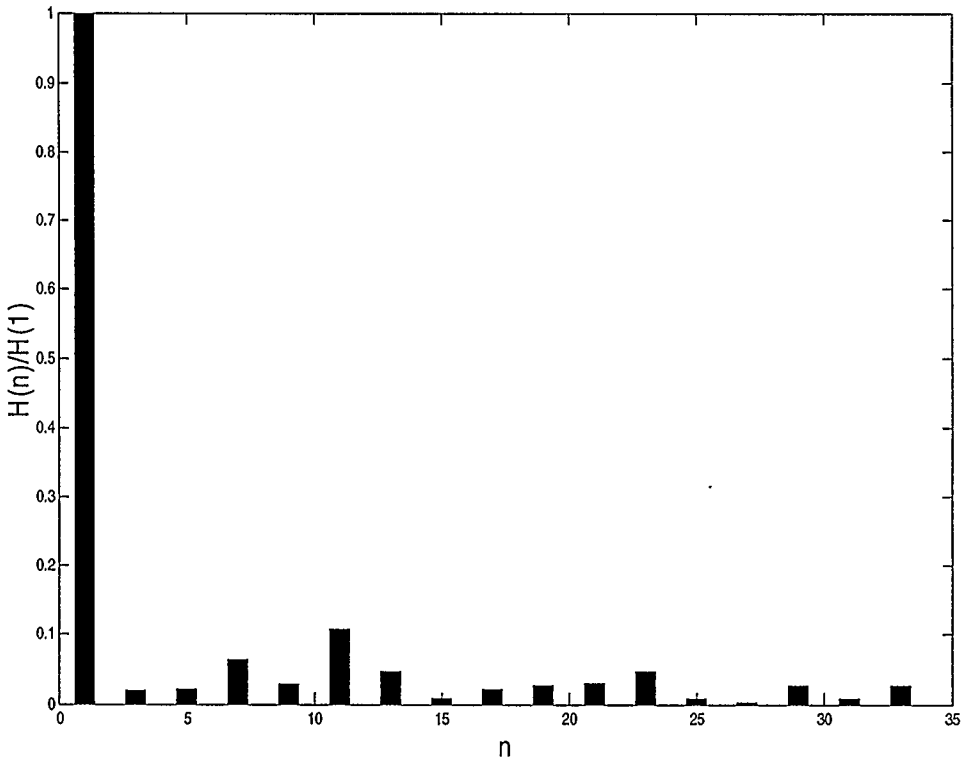


Fig. 3.5 Spectrum of the conventional staircase waveform for two voltage sources

Equation (3.5) provides a basis to find the harmonic equation for the first technique. Every value of the step voltage is multiplied by a cosine function whose argument is n

multiplied by the angle that the transition is taking place at. The step voltage here is defined as the difference between the value of the current level voltage and the one before it. This is a very important result that is necessary to derive the harmonic equations for both of the techniques that are discussed here. For the current (first) technique, a careful inspection of the waveforms in Fig. 3.4 can be made. The important point to note here is the value of the step voltage between any two levels. This is the value that will be effective in formulating the harmonic equation for this condition. The three step values in this case are: *V1* at $\theta 1$, *(V2-V1)* at $\theta 2$, and *V1* again at $\theta 3$. As stated before, the value of *V2* in the diagram is chosen to be *2V1* for the purpose of achieving equal voltage steps, however, the derivation will be done for the more general case of voltage values that comply with the equations (3.1)-(3.3) given above. According to the above discussion; the equation for Fourier coefficients of the output waveform in the case of two voltage sources and using the first technique can be given as:

$$H(n) = \frac{4}{n\pi}[V1\{cos(n\theta 1) - cos(n\theta 2) + cos(n\theta 3)\} + V2\,cos(n\theta 2)],$$

$$n = 1, 3, 5 \ldots \quad (3.7)$$

By inspecting equation (3.7) and the transitions in *Va1* and *Va2* given in Fig. 3.4, it can be noted that the positive signs preceding $cos(n\theta 1)$ and $cos(n\theta 3)$ in the first term of the equation that contains *V1* correspond to the rising edges of *Va1* at $\theta 1$ and $\theta 3$, respectively, while the negative sign preceding $cos(n\theta 2)$ in the same term corresponds to the falling edge of *Va1* at $\theta 2$. The second term in the equation that contains *V2*, has only a positive sign preceding $cos(n\theta 2)$; since there is no falling edge for *Va2* in the first

quarter of the waveform. This same argument will hold true for the case of more than two dc voltage sources. For instance, in the case of three voltage sources, the equation of the Fourier coefficients will have the first term containing *V1* multiplied by seven cosine terms associated with the seven transitions of *Va1* in the first quarter of the waveform; each of these terms will have a positive or a negative sign reflecting its condition of transition; positive for a rising edge, and negative for a falling one, i.e. we wil have the following equation:

$$H(n) = \frac{4}{n\pi}[V1\{cos(n\theta 1) - cos(n\theta 2) + cos(n\theta 3) - cos(n\theta 4) + cos(n\theta 5) - cos(n\theta 6) + cos(n\theta 7)\} + V2\{cos(n\theta 2) - cos(n\theta 4) + cos(n\theta 6)\} + V3\, cos(n\theta 4)]],$$

$$n = 1, 3, 5 \ldots \quad (3.8)$$

This pattern can be noted more clearly in the list of step voltage values given in Table (3.2). In this table, the values of the staircase output voltage waveform *v(t)* are listed up to 15 steps, i.e. for *m*=4, together with the corresponding step values. The step values are the difference between a given voltage level and the previous one. The pattern of the step voltages follows a binary sequence. For more declaration of the final compact form of the equation, the case of four voltage sources is given in the following equation:

$$H(n) = \frac{4}{n\pi}[V1\{cos(n\theta1) - cos(n\theta2) + cos(n\theta3) - cos(n\theta4) + cos(n\theta5) - cos(n\theta6) + cos(n\theta7) - cos(n\theta8) + cos(n\theta9) - cos(n\theta10) + cos(n\theta11) - cos(n\theta12) + cos(n\theta13) - cos(n\theta14) + cos(n\theta15)\} + V2\{cos(n\theta2) - cos(n\theta4) + cos(n\theta6) - cos(n\theta8) + cos(n\theta10) - cos(n\theta12) + cos(n\theta14)\} + V3\{cos(n\theta4) - cos(n\theta8) + cos(n\theta12)\} + V4\{cos(n\theta8)\}], \quad n = 1,3,5 \ldots \quad (3.9)$$

Hence, for the general case of *m* dc voltage sources, the equation for Fourier coefficients *H(n)* for the first technique can be given in a compact form as follows:

$$H(n) = \frac{4}{n\pi}\sum_{j=1}^{m} Vj \sum_{i=1}^{2^{m-j+1}-1} (-1)^{i+1} \cos\left(n\theta_{2^{j-1}(i)}\right), \quad n = 1,3,5.. \quad (3.10)$$

Table (3.2) Pattern of step values in the first technique

angle number(*i*)	voltage level	step value
1	*V1*	*V1*
2	*V2*	*V2-V1*
3	*V2+V1*	*V1*
4	*V3*	*V3-V2-V1*
5	*V3+V1*	*V1*
6	*V3+V2*	*V2-V1*

7	*V3+V2+V1*	*V1*
8	*V4*	*V4-V3-V2-V1*
9	*V4+V1*	*V1*
10	*V4+V2*	*V2-V1*
11	*V4+V2+V1*	*V1*
12	*V4+V3*	*V3-V2-V1*
13	*V4+V3+V1*	*V1*
14	*V4+V3+V2*	*V2-V1*
15	*V4+V3+V2+V1*	*V1*
16	*V5*	*V5-V4-V3-V2-V1*

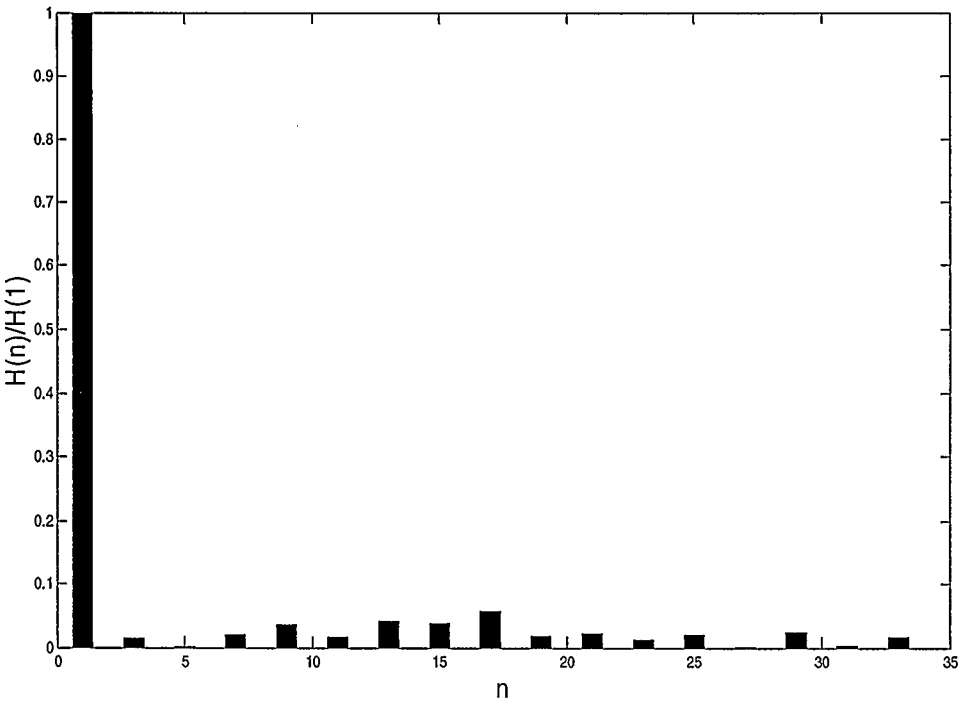


Fig. 3.6 Spectrum of the staircase waveform for two voltage sources generated by the first technique

Equation (3.10) represents the Fourier coefficient values for the staircase waveform generated by the first technique. Verification of this equation is given in Appendix C. Fig. 3.6 gives the spectrum of the output waveform generated using this method. The maximum harmonic magnitude occurs at the 17^{th} harmonic and equals to 5.7% of the fundamental. The THD is 12.21%; a reduction of approximately 30% from the case of the conventionally generated waveform. The reduction in THD will be higher in the case of more than two voltage sources.

3.5 The Technique of Dual Polarity Voltage Addition in Each Half Cycle

In the technique investigated in the previous section, it was possible to reach a number of levels equal to $(2^{m+1}-1)$. This higher number of levels was achieved by inserting all the possible combinations of voltage additions in the output waveform with the same polarity of the half wave output waveform. The second technique exploits this idea, with some modification, to obtain a larger number of voltage levels in the inverter output. In this technique, all the possibilities of positive and negative polarity voltage values are used in each half cycle of the output waveform to achieve the maximum number of levels in the inverter output. Going back to the same example of the two voltage sources, the output waveform can be made of nine levels in this case by adding the voltage level that is equal to *V2-V1*. The sequence of steps is *V1* at $\theta 1$, *V2-V1* (a new value) at $\theta 2$, *V2* at $\theta 3$, and *V2+V1* at $\theta 4$, and the symmetrical voltages with negative polarity in the negative half cycle. Four switching angles are present in the first quarter of the waveform in this case

with only two dc voltage sources. As stated before, there are more constraints with this technique; the most obvious one is that *V2-V1* should not be equal to any of the other three voltage level values. This can be formulated as follows:

$V2-V1>V1$

Also, for the case of three voltage sources, one should have:

$V3-V2-V1>V2+V1$

In general, for any number of voltage sources, this constraint may be expressed as:

$Vj-(V1+V2+...+Vj-1)>V1+V2+...+Vj-1 \quad (3.11)$

Equations (3.1)-(3.3), in addition to equation (3.11) represent the requirements imposed on the values of the dc voltage sources for the second technique. For equal step voltage values, the special case of $V_i = 3V_{i-1}$, for all i, can be used; this is to be proved later on in this chapter. The other requirement needed for this approach is related to the nature of these dc sources. All of the voltage sources, except for one with the highest voltage value, must accept current flowing in the opposite direction (i.e. sending power to the source) for some parts of the output waveform cycle. This requirement stems from the nature of the dual polarity voltage addition procedure adopted in this technique. With this technique, the number of levels of the inverter output can be as much as 3^m. For a three voltage source, for example, an output waveform of 27 levels can be generated; compared with 7 levels in the conventional case. Harmonic distortion can be reduced greatly with such an increase in the number of levels.

3.6 Harmonic Analysis of the Second Technique

Once again, the case of two voltage sources is first presented, and the general formula for any number of voltage sources can be deduced after that. Fig. 3.7 depicts the output waveform and the switching states of the H-bridge output voltages, choosing V2=3V1. It can bee seen from this figure that the waveform of Va2 is a normal square wave activated at θ2, while Va1 is activated at three of the four angles of the output waveform with positive and negative polarities. Once again, the method used previously to find the Fourier coefficients in the first technique is used here. The cosine term is multiplied by the value of the step voltage in the output waveform, and the argument of the cosine function is *n* multiplied by the angle at which this step takes place. Table (3.3) shows the values of step voltages for this technique for up to four voltage sources, i.e. providing 81 levels in the output voltage waveform. According to this table and the discussion above, the Fourier coefficients of the staircase waveform shown in Fig. 3.7 can be given as:

$$H(n) = \frac{4}{n\pi}[\{V1\}cos(n\theta 1) + \{V2 - V1 - (V1)\}cos(n\theta 2) + \{V2 - (V2 - V1)\}cos(n\theta 3) + \{(V1 + V2) - V2\}cos(n\theta 4)],$$
$$n = 1, 3, 5 \ldots \quad (3.12)$$

In this equation, the expressions that were put between curly braces {.} represent the values of the step voltages at the specified activation angles. Simplifying equation (3.12) allows us to express the harmonic coefficients in the following form:

$$H(n) = \frac{4}{n\pi}[V1\{cos(n\theta 1) - 2\,cos(n\theta 2) + cos(n\theta 3) + cos(n\theta 4)\} + V2\,cos(n\theta 2)],$$
$$n = 1, 3, 5 \ldots \quad (3.13)$$

In the case of three voltage sources, there will be angles up to θ13; as can be seen from table 3.3, where the output staircase waveform will have 27 levels. The equation for harmonic coefficients in this case can be written as:

$$H(n) = \frac{4}{n\pi}[V1\{cos(n\theta1) + cos(n\theta2) + cos(n\theta3) + .. + cos(n\theta13) - 3cos(n\theta2) - 3\,cos(n\theta5) - 3\,cos(n\theta8) - 3\,cos(n\theta11)\} + V2\{cos(n\theta2) + cos(n\theta5) + cos(n\theta8) + cos(n\theta11)$$

$$-3cos(n\theta5)\}+V3cos(n\theta5)],n = 1,3,5,..(3.14)$$

In the case of 4 voltage sources, there will be angles up to θ40, the output will have 81 levels, and the equation can be written as:

$$H(n) = \frac{4}{n\pi}[V1\{cos(n\theta1) + cos(n\theta2) + cos(n\theta3) + .. + cos(n\theta40) - 3cos(n\theta2) - 3\,cos(n\theta5) - 3\,cos(n\theta8) - 3\,cos(n\theta11) - 3\,cos(n\theta14) - 3\,cos(n\theta17) - 3cos\,(n\theta20) - .. - 3cos\,(n\theta38)\} + V2\{cos(n\theta2) + cos(n\theta5) + cos(n\theta8) + cos(n\theta11)$$

$$+cos(n\theta14)+cos(n\theta17)+..+cos(n\theta38)-$$

$$3cos(n\theta5) - 3\,cos(n\theta14) - 3\,cos(n\theta23) - 3cos\,(n\theta32)\}+V3\{cos(n\theta5) + cos\,(n\theta14)$$

$$+cos(n\theta23) + cos(n\theta32) - 3cos\,(n\theta14)\}+V4\{cos(n\theta14)\}],n = 1,3,5,..(3.15)$$

To proceed further with the derivation of the final compact form of the Fourier coefficients equation for the second technique; it is very helpful to understand the pattern

of the step voltage values shown in Table (3.3). From this pattern it is seen that the step values follow a ternary repetition mode. Also, it can be noted that the term multiplied by (-2) in equation (3.13) is repeated several times in equations (3.14) and (3.15). For the sake of simplicity of formulation, this term is put in the form of (1-3), i.e. instead of writing for example [-2Vcos(nθ)], it is written as [Vcos(nθ)-3Vcos(nθ)]. Following these rules, the equation of the Fourier coefficients for the second technique can be compactly expressed by the following form:

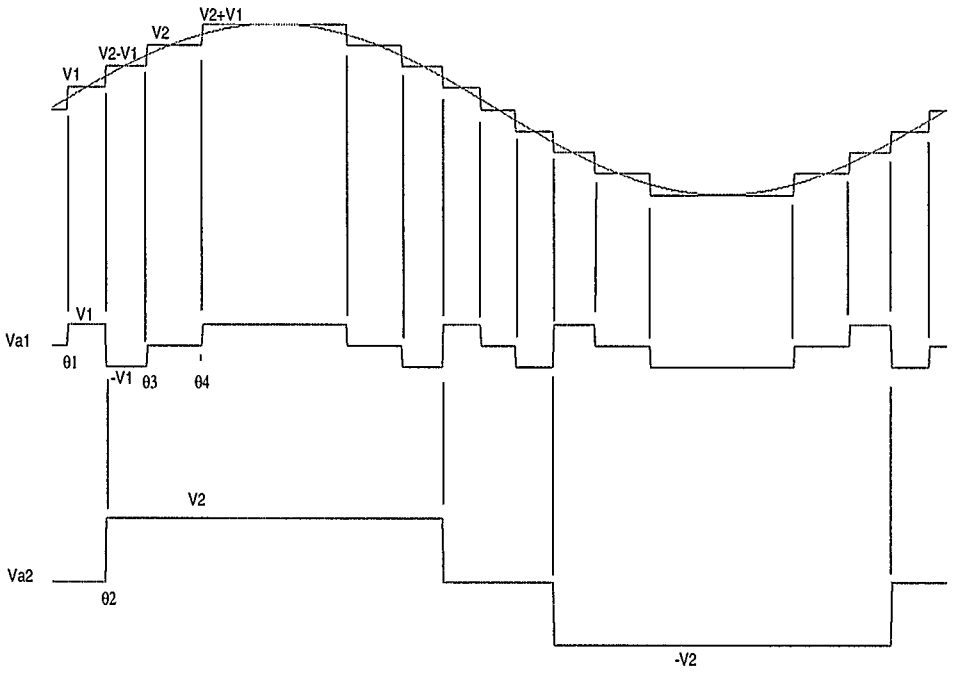


Fig. 3.7 Output voltage waveform and switching pattern for the second technique

$$H(n) = \frac{4}{n\pi}\{\sum_{j=i}^{m-1} Vj\,[\sum_{i=0}^{\frac{3^{m+i-j-3}}{2}} \cos\left(n\,\theta_{3^{j-i}i+\frac{1}{2}(3^{j-i}+1)}\right) - 3\sum_{k=0}^{\frac{3^{m-j-3}}{2}} \cos\left(n\theta_{3^{j}k+\frac{3^{j}+1}{2}}\right)]$$

$$+ V_m \cos(n\theta_{\frac{3^{m-i}+1}{2}})\}, \qquad n = 1,3,5 \ldots \quad (3.16)$$

Table (3.3) Pattern of Step Voltage Values in the Second Technique

angle number(i)	voltage level	step value
1	V1	V1
2	V2-V1	V2-2V1
3	V2	V1
4	V2+V1	V1
5	V3-V2-V1	V3-2V2-2V1
6	V3-V2	V1
7	V3-V2+V1	V1
8	V3-V1	V2-2V1
9	V3	V1
10	V3+V1	V1
11	V3+V2-V1	V2-2V1
12	V3+V2	V1
13	V3+V2+V1	V1
14	V4-V3-V2-V1	V4-2V3-2V2-2V1
15	V4-V3-V2	V1
16	V4-V3-V2+V1	V1

17	V4-V3-V1	V2-2V1
18	V4-V3	V1
19	V4-V3+V1	V1
20	V4-V3+V2-V1	V2-2V1
21	V4-V3+V2	V1
22	V4-V3+V2+V1	V1
23	V4-V2-V1	V3-2V2-2V1
24	V4-V2	V1
25	V4-V2+V1	V1
26	V4-V1	V2-2V1
27	V4	V1
28	V4+V1	V1
29	V4+V2-V1	V2-2V1
30	V4+V2	V1
31	V4+V2+V1	V1
32	V4+V3-V2-V1	V3-2V2-2V1
33	V4+V3-V2	V1
34	V4+V3-V2+V1	V1
35	V4+V3-V1	V2-2V1
36	V4+V3	V1
37	V4+V3+V1	V1
38	V4+V3+V2-V1	V2-2V1

39	V4+V3+V2	V1
40	V4+V3+V2+V1	V1
41	V5-V4-V3-V2-V1	V5-2V4-2V3-2V2-2V1

This is the compact form of the equation that gives the Fourier coefficients of the output waveform for any number of voltage sources using the technique of dual polarity half cycle addition to generate the output waveform of the inverter. This equation is derived by writing all the equations of the harmonic components according to table 3.3 and putting the resulting quantities in a rigid form; as shown above. Verification of this equation is given in Appendix C. It is noted that the highest value voltage source, Vm, appears only once in this equation, since in the output switching pattern this voltage appears like a simple square wave activated at the specified angle. This highest voltage value was excluded from the first summation in the equation. It never appears in a negative sign form in the equation. Fig. 3.8 shows the spectrum of the waveform of Fig. 3.7 normalized to the fundamental component. The highest components appear as the 17^{th} and 21^{st} harmonics and equal approximately to 3% of the fundamental. The THD in this case is 9.3%, a considerable decrease in this figure from the original 17.5% for the conventional approach. This decrease will be much higher in the case of three voltage sources; where the output waveform will consist of 27 levels compared to 7 levels in the traditional approach.

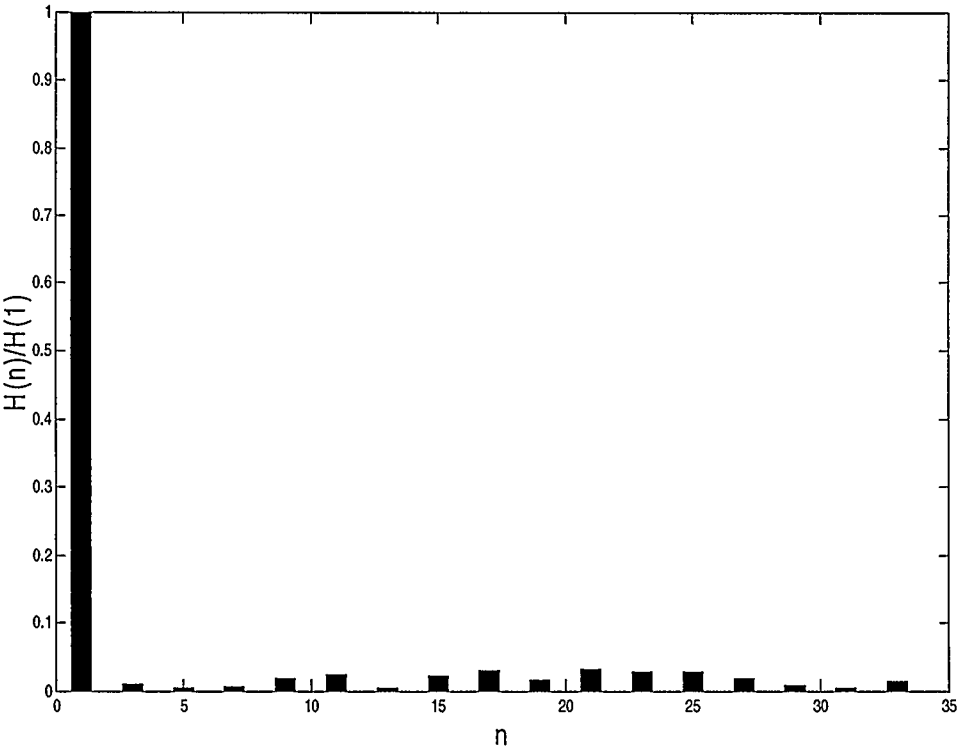


Fig. 3.8 spectrum of the output waveform generated by the 2nd technique for two voltage sources

It was stated earlier in this chapter that to obtain equal steps in the output waveform, it is required that $V_i = 3V_{i-1}$, for all i. To prove this; table 3.3 has to be studied carefully. The step values in this table are either V1, or they are the values appearing at angles θ2, θ5, θ8, θ11, θ14, ..etc which can be put in the following general formula

$V_j - 2V_{j-1} - 2V_{j-2} - ... - 2V1$

At θ2, for example, the step value is V2-2V1, putting V2=3V1, the step value will be 3V1-2V1=V1. Also at θ5, the step value is V3-2V2-2V1. Putting V3=3V2, and V2=3V1 we obtain the step value equal to

$3V2-2(3V1)-2V1$

$=3(3V1)-6V1-2V1$

$=9V1-8V1$

$=V1$

For the general case of Vj given above, the step value will be

$3V_{j-1}-2(3V_{j-2})-2(3V_{j-3})-..-2V1$

$=3^{j-1}V1-2(3^{j-2}V1)-\ldots-2(3^2V1)-2(3V1)-2V1$

$=V1[3^{j-1}-2\{1+3^1+3^2+3^3+\ldots+3^{j-2}\}]$

$=V1[3^{j-1}-(3-1)\{1+3^1+3^2+3^3+\ldots+3^{j-2}\}]$

$=V1[3^{j-1}-\{3^1+3^2+3^3+\ldots+3^{j-2}+(3^{j-1})\}+\{(1)+3^1+3^2+3^3+\ldots+3^{j-2}\}]$

$=V1[3^{j-1}-\{3^1+3^2+3^3+\ldots+3^{j-2}\}-(3^{j-1})+(1)+\{3^1+3^2+3^3+\ldots+3^{j-2}\}]$

$= V1[3^{j-1}--3^{j-1}-\{3^1+3^2+3^3+\ldots+3^{j-2}\}+\{3^1+3^2+3^3+\ldots+3^{j-2}\}+1]$

$=V1[1]$

$=V1$

This ensures equal step values that are equal to V1 for the output staircase waveform using the second technique studied in this chapter.

3.7 Analyzing the Effect of Waveform Parameters on THD

It is important to understand the effect of the parameters of the waveform on the value of the THD. The main equation for THD that is going to be used in this analysis is equation (2.1). The effect of the various parameters on the value of the THD obtained from this equation is discussed in details in this section.

For convenience; equation (2.1) is repeated here

$$THD = \sqrt{\frac{\sum_{i=2}^{\infty}\{H(i)\}^2}{\{H(1)\}^2}}$$

This equation can equivalently be written in the following form [1]:

$$THD = \sqrt{\frac{2(Vrms)^2 - \{H(1)\}^2}{\{H(1)\}^2}} \quad (3.17)$$

where Vrms is the root mean square value of the output waveform and H(1) is the peak value of the 1st harmonic. This alternative form of THD stems from the fact that the squared rms value of any waveform is equal to the sum of the squared rms values of all the harmonics of that waveform, i.e.

$$(Vrms)^2 = \sum_{i=1}^{\infty} \left[\frac{H(i)}{\sqrt{2}}\right]^2 \quad (3.18)$$

To have a good insight into the effect of the system parameters on the THD given by equation (3.17), the case of a three level waveform (with the existence of only one transition angle; θ) will be studied first, then the more general case of any number of angles can be realized in the same way. The analysis in this section will not take into consideration the way by which these waveforms are generated. They can be generated by the traditional approach, or they can be generated also by any one of the two approaches introduced earlier in this chapter. The result will be the same in any of the above cases. Fig 3.9 depicts a three level waveform with the transition angle θ taking

place at the midpoint between the two voltages: 0 and V; which is the way adopted so far in this work to represent these waveforms. The value of θ is 30.00 ° in this case. From equation (3.5), the equation of the peak value of the first harmonic of this waveform can be given by:

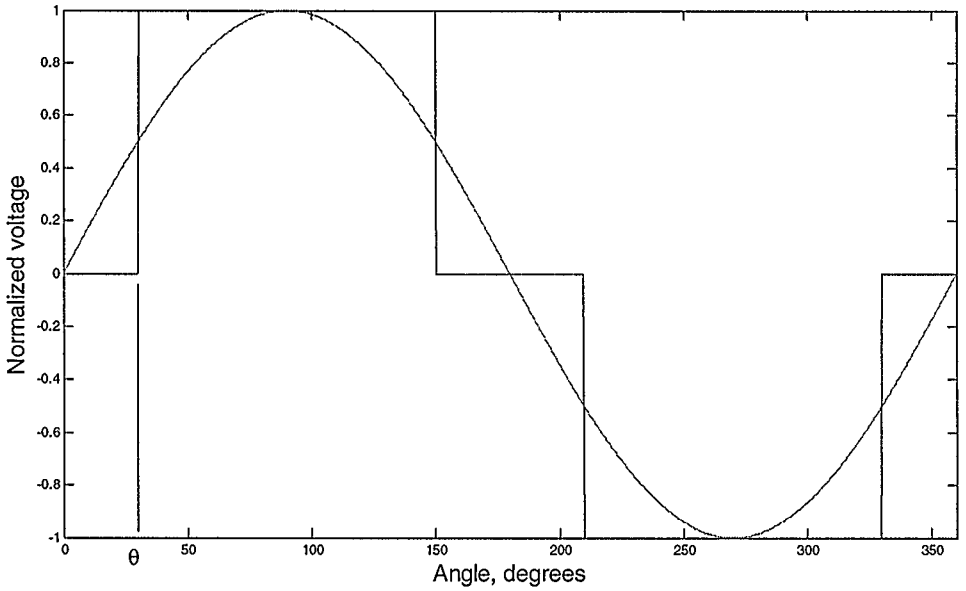


Fig. 3.9 A three level waveform having single transition angle θ

$$H(1) = \frac{4}{\pi} V \cos(\theta) \quad (3.19)$$

According to the definition of the rms value, the value of $(Vrms)^2$ for any waveform can be given as:

$$(Vrms)^2 = \frac{1}{T}\int_0^T [v(t)]^2 \, dt \quad (3.20)$$

Where *v(t)* is the instantaneous value of the voltage waveform. Going on with the derivation of the equation of the current waveform, one finally obtains:

$$(Vrms)^2=V^2(1-\frac{2\theta}{\pi}) \quad (3.21)$$

Using equations (3.19) and (3.21) and substituting into equation (3.17) we obtain:

$$THD = \sqrt{\frac{2(1-\frac{2\theta}{\pi}) - \{\frac{4}{\pi}cos(\theta)\}^2}{\{\frac{4}{\pi}cos(\theta)\}^2}} \quad (3.22)$$

which is independent of the voltage value V. Fig. 3.10 gives the graph of THD for this waveform with varying θ according to equation (3.22). The minimum THD is reached at an angle value of 23.50 ^{o} with THD=29%. The 30.00 ^{o} angle of the midpoint approach has a THD value of approximately 31%; a slight difference from the minimum value.

The next waveform that will be studied is the case of a five-level waveform. This is the waveform discussed earlier in chapter two which has two transition angles θ1 and θ2 and shown in Fig. 2.2. Assuming the two positive levels of the waveform are V1 and V1+V2, the peak of the fundamental sinusoid can be given according to equation (3.5) as follows:

$$H(1) = \frac{4}{\pi}[V1\,cos(\theta1) + V2\,cos(\theta2)] \quad (3.23)$$

Putting $V1 = V2$ we obtain:

$$H(1) = \frac{4}{\pi}V1[cos(\theta1) + cos(\theta2)] \quad (3.24)$$

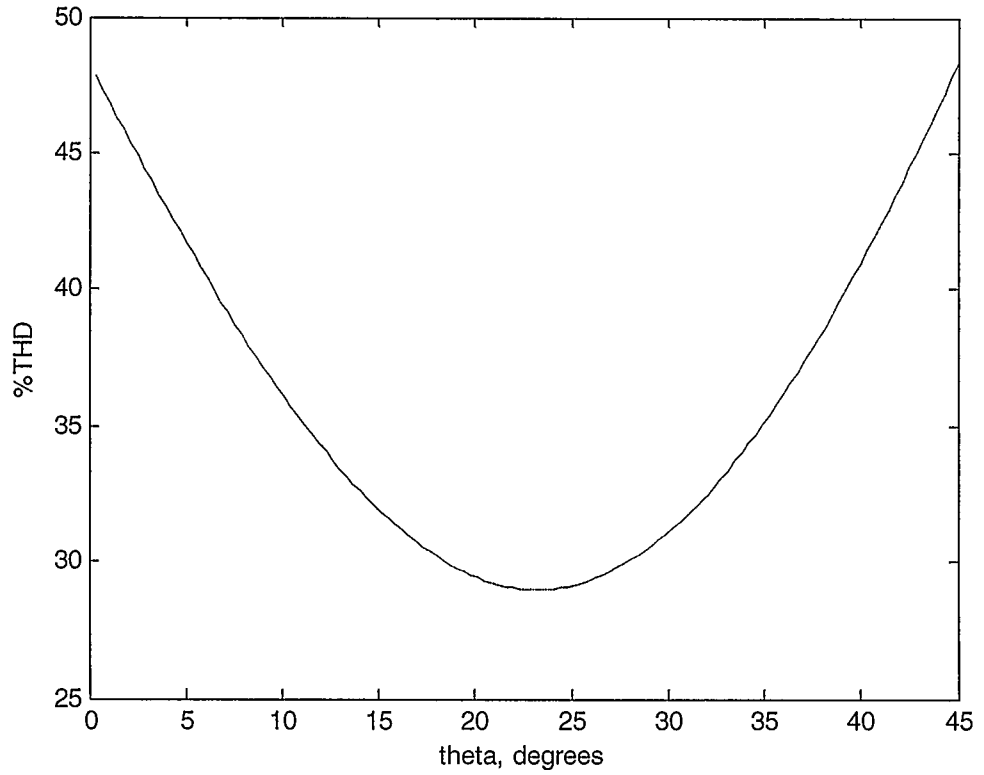


Fig. 3.10 THD of a three level voltage waveform versus the angle θ.

The squared of the rms value of this waveform can be evaluated using equation (3.20) to obtain the following final result:

$$(Vrms)^2 = \frac{2}{\pi}\left[(V1)^2(\theta 2 - \theta 1) + (V1 + V2)^2\left(\frac{\pi}{2} - \theta 2\right)\right] \quad (3.25)$$

Putting $V1=V2$, one obtains:

$$(Vrms)^2 = \frac{2}{\pi}(V1)^2\left[(\theta 2 - \theta 1) + 4\left(\frac{\pi}{2} - \theta 2\right)\right] \quad (3.26)$$

$$(Vrms)^2 = 4(V1)^2\left[1 - \frac{\theta 1 + 3\theta 2}{2\pi}\right] \quad (3.27)$$

Substituting the expressions obtained from equations (3.27) and (3.24) into equation (3.17) we obtain:

$$THD = \sqrt{\frac{8\left[1 - \frac{\theta 1 + 3\theta 2}{2\pi}\right] - \{\frac{4}{\pi}[cos(\theta 1) + cos(\theta 2)]\}^2}{\{\frac{4}{\pi}[cos(\theta 1) + cos(\theta 2)]\}^2}} \quad (3.28)$$

As in the previous case, this is also independent of V1. Fig 3.11 depicts a surface representing the THD versus the two variables θ1 and θ2. The surface has one global minimum at θ1=12.48 ° and θ2=41.82 °, with THD=16.42%. The method of midpoint voltage gives a value for THD equals 17.56%, with θ1=14.76 ° and θ2=48.60 °, which are not far away from the optimum condition.

As the number of levels and angles are increased, the plot will be an m+1 dimensional; for m angles. Just one case will be presented here which can be partially visualised by a three dimensional plot; and that is the case of a seven level waveform with three angles. The minimum THD of 11.53% for this waveform is found at θ1=9.00 °, θ2= 27.72 ° and θ3=50.76 °, the corresponding values in the midpoint voltage method are THD=12.21%, θ1=9.72 °, θ2=30.24 ° and θ3=56.52 °. Keeping one angle constant and plotting the value of THD versus the other two angles yields plots that are similar to the 3-D surface presented earlier for the case of two angles only. Fig. 3.12 depicts the surface representing THD versus θ1 and θ2 keeping θ3 fixed at 72.00 °. While Fig. 3.13 depicts THD versus θ2 and θ3 with θ1 fixed at 9.00 °.

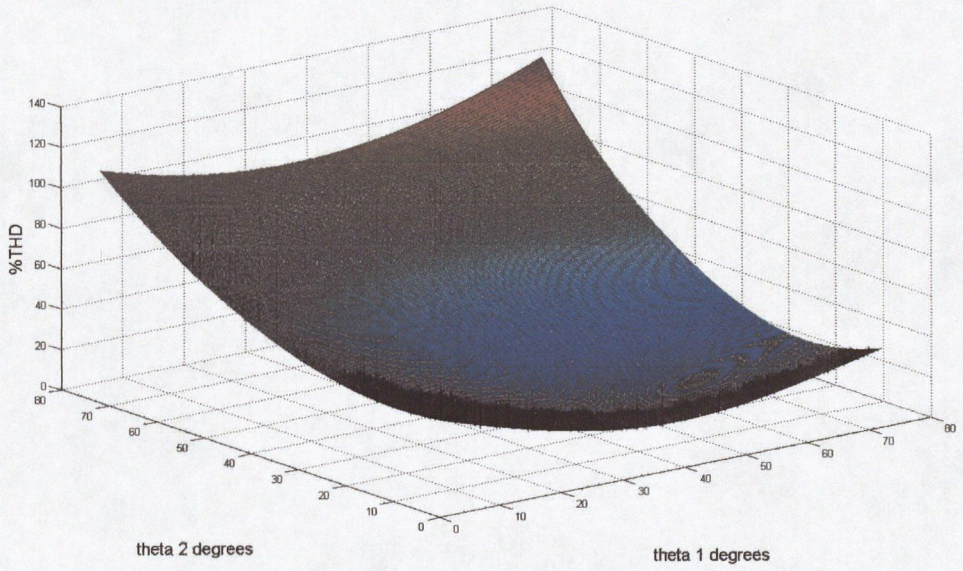


Fig 3.11 THD versus the two angles in a five level waveform

3.8 Searching for the Minimum THD Using a Search Algorithm

From the figures obtained in the previous section of THD, it is clearly understood that THD has a bowel shape that has a minimum value at some specific values of the switching angles. A search can be carried out to find this minimum point of THD, representing the optimum solution for the values of the switching angles. This search can be started from a point on the surface and proceeds iteratively to reach the optimum condition. The starting point can be chosen to be the midpoint voltage, since the values of THD for this point are very close to the optimum point, as shown in the previous section. This iterative search is important when the number of angles is three or more, since the exhaustive search will be very time consuming in such cases. The search algorithm

chosen here is the gradient search algorithm, which can be a good choice to find the minimum point of THD. This algorithm can be given in the case of a single variable θ in the following equation [49]:

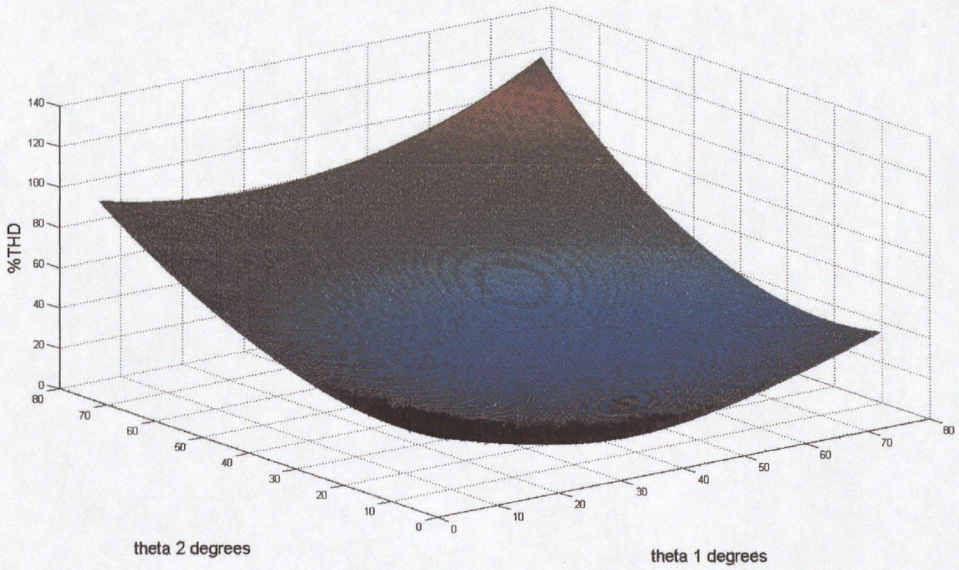


Fig. 3.12 THD with θ3 fixed at 72.00 ^{o} for a seven level waveform

$$\theta_{(k+1)}= \theta_{(k)}+\mu(-\nabla_k) \quad (3.29)$$

Where $\theta_{(k)}$ is the value of θ at the kth (the present) iteration, $\theta_{(k+1)}$ is the new value of θ, μ is a fixed step size parameter that governs stability and rate of convergence, and ∇_k is the value of the gradient at $\theta_{(k)}$. This gradient is given by the following expression in the present case:

$$\nabla_k=\frac{d(THD)}{d\theta}|\theta = \theta_{(k)} \quad (3.30)$$

To make equation (3.29) simpler, only the sign of the gradient can be taken into consideration. This will put the equation in the following form:

$$\theta_{(k+1)}= \theta_{(k)}+\mu[-sgn(\nabla_k)] \qquad (3.31)$$

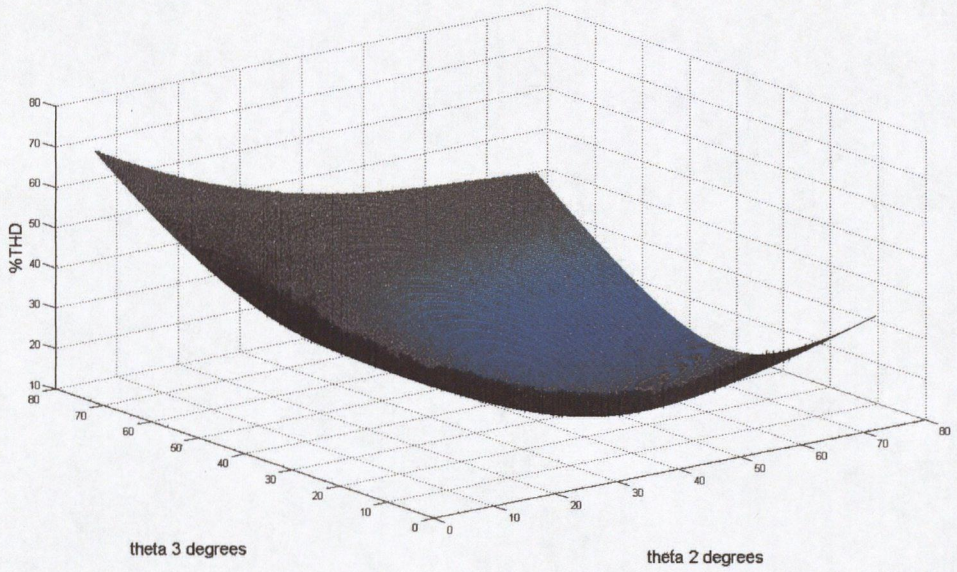


Fig. 3.13 THD for a seven level waveform with θ1 fixed at 9.00 °

This form will ensure that the angle updating is going in the right direction that minimizes THD, while keeping the step size controlled only by μ.

For the multidimensional case of more than one angle, the gradient search algorithm can be given in vector form as follows [49]:

$$\theta_{(k+1)}= \theta_{(k)}+\mu(-\nabla_k) \qquad (3.32)$$

The value of ∇_k in this case will be replaced by the partial derivatives of THD with respect to each angle. It is shown in this equation also that the value of μ is fixed for the

whole set of angles; however, it can be given separate values for each angle and treated individually for each one. The multidimensional form of equation (3.31) can be given in the following form:

$$\theta_{(k+1)} = \theta_{(k)} + \mu[-sgn(\nabla_k)] \quad (3.33)$$

where the previous scalar μ has been replaced by a vector to reflect the fact that it can have distinct values for each angle.

The search algorithm is applied first to the case of the three-level waveform having single angle θ. The result of the search process is shown in Fig. 3.14. The value of μ is taken to be 0.01 (radians) which proved successful. The search path is shown by the dotted points. The start point is chosen to be the 30.00 ^{o} midpoint voltage value.

One remark has to be made here about the value of the μ used in this search. Initially, it is chosen to be fixed at a specified value; 0.01 radians in this example. When the search moves closer to the point where the gradient value is zero, there will be a change of sign in the gradient value, since it is not expected that the search will reach exactly to the point of zero gradient. This will transfer the search from one side of the bowel-shaped curve to the other side. When this happens, the value of μ will be decreased slightly. The decrease in the step size parameter takes place whenever there is a change in the sign of the gradient. This action is carried out on the value of the step size to ensure that the search point swings around the minimum point and moving closer to the bottom point as the iteration process progresses further. The search will stop when the change in THD from a

point to the next reaches a very small value that is regarded acceptable. For example a change of THD of less than 0.001% was usually used to stop the search.

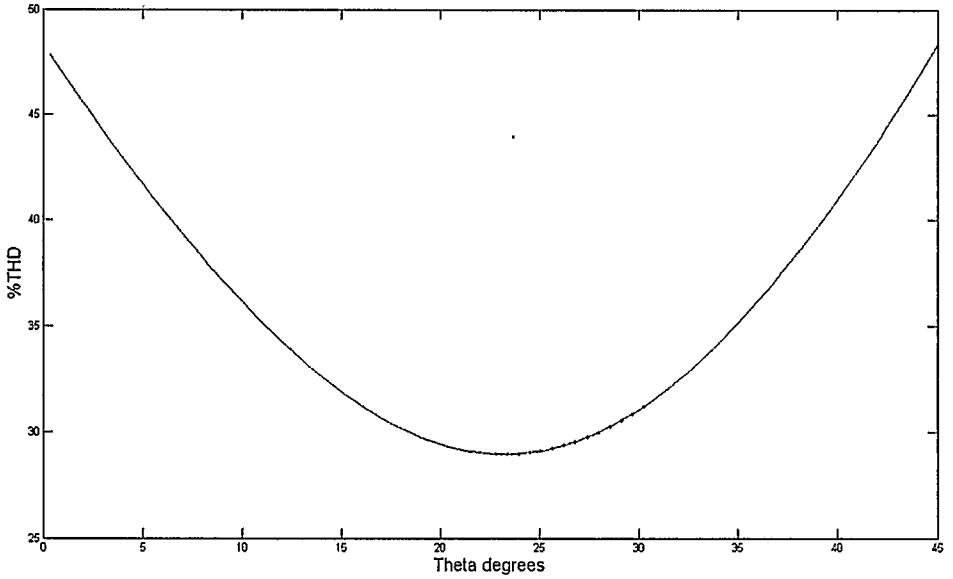


Fig. 3.14 Search path for minimum THD in a three level waveform

The next optimization case investigated is for the five-level waveform that has two angles. Fig. 3.15 depicts the search path for minimum THD for this waveform starting from $\theta 1=14.76^{\circ}$ and $\theta 2=48.60^{\circ}$ with a value of $\mu=0.0001$ radians. In this search, $\theta 1$ and $\theta 2$ are updated in each iteration according to equation (3.33). The starting value of μ is the same for both angles. However, at every turning point of an angle, the same procedure of decreasing the step size is done associated with the angle that goes through that turning point, ending in different values for the step size for each angle.

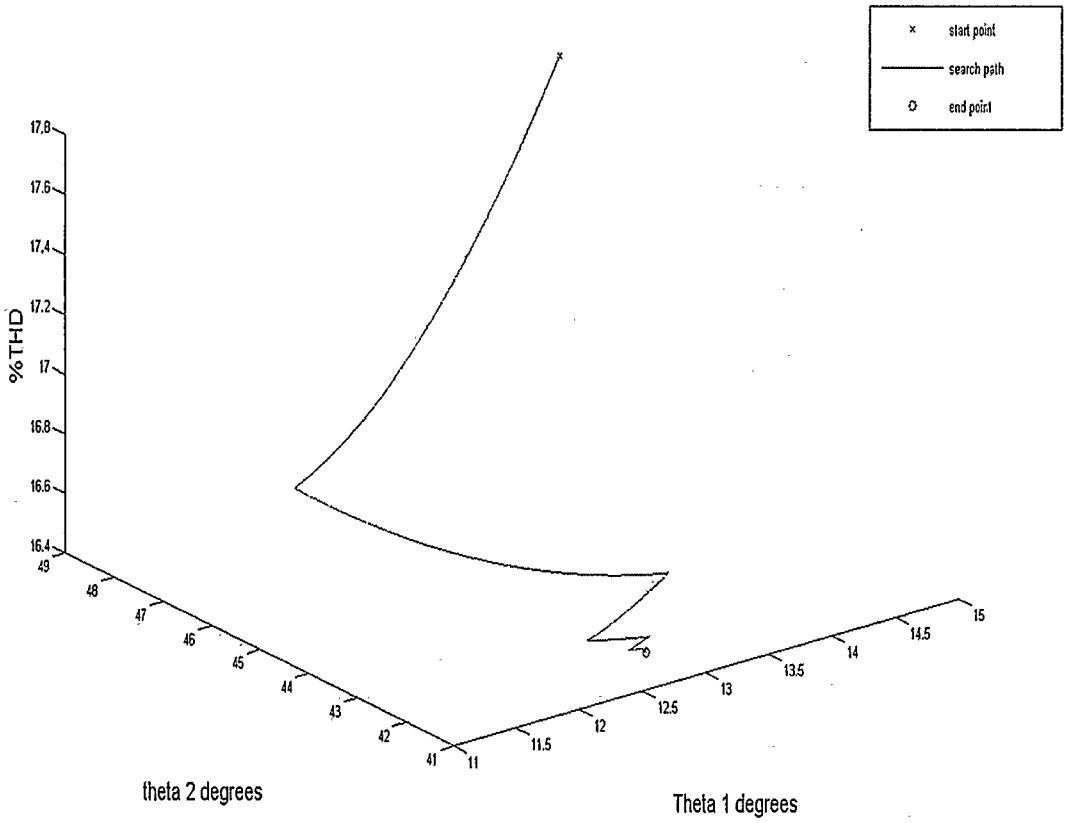


Fig. 3.15 Search path for a five-level waveform with μ=0.0001 rad.

The search paths with the same starting point are shown in Fig. 3.16 for μ=0.001 and Fig. 3.17 for μ= 0.01. In each of the three cases, the same final value of THD is reached; with a fewer number of iterations for higher values of μ.

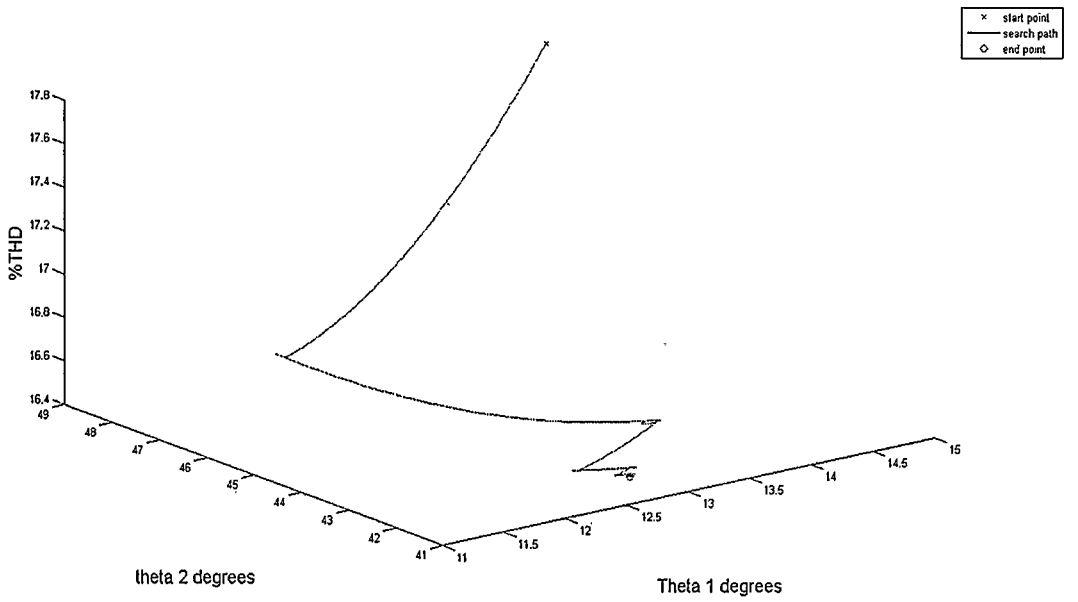


Fig. 3.16 Search path for a five-level waveform with μ=0.001 rad

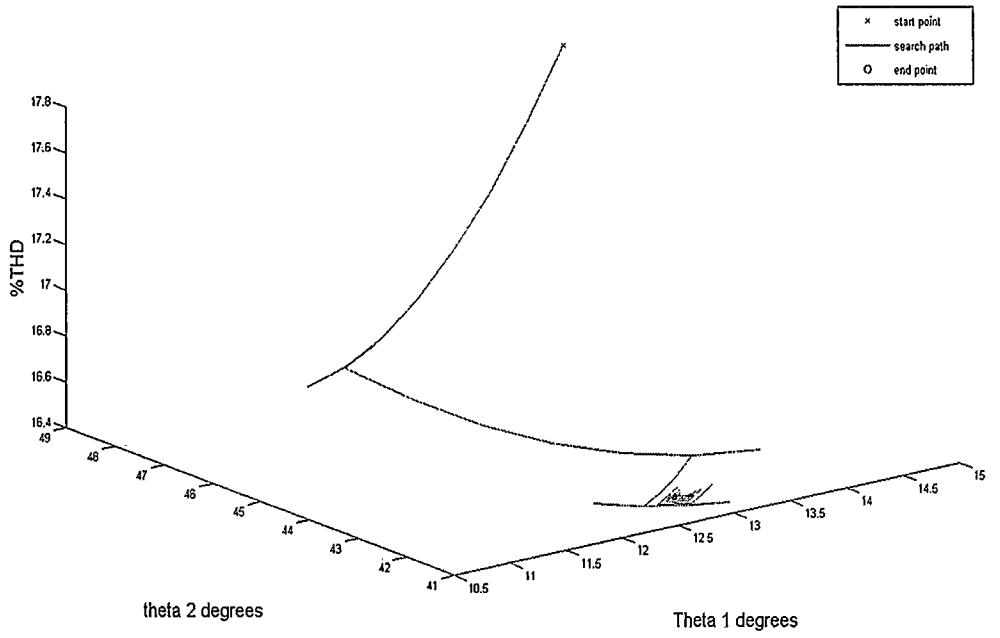


Fig. 3.17 Search path for a five-level waveform with μ=0.01 rad

The starting point in each of the above figures was chosen arbitrary. However, starting with the midpoint voltage would reduce further the number of iterations required to reach the final optimum angle values. Fig. 3.18 depicts the search path for a different starting point of $\theta 1=24.76^{\circ}$ and $\theta 2=28.6^{\circ}$ with $\mu=0.0001$ radians. Using this search algorithm, the same final value is reached every time no matter where the starting point is. This search algorithm can be used for any number of waveform levels (and hence angles) to reduce the computation effort towards reaching the minimum THD in a multilevel output waveform.

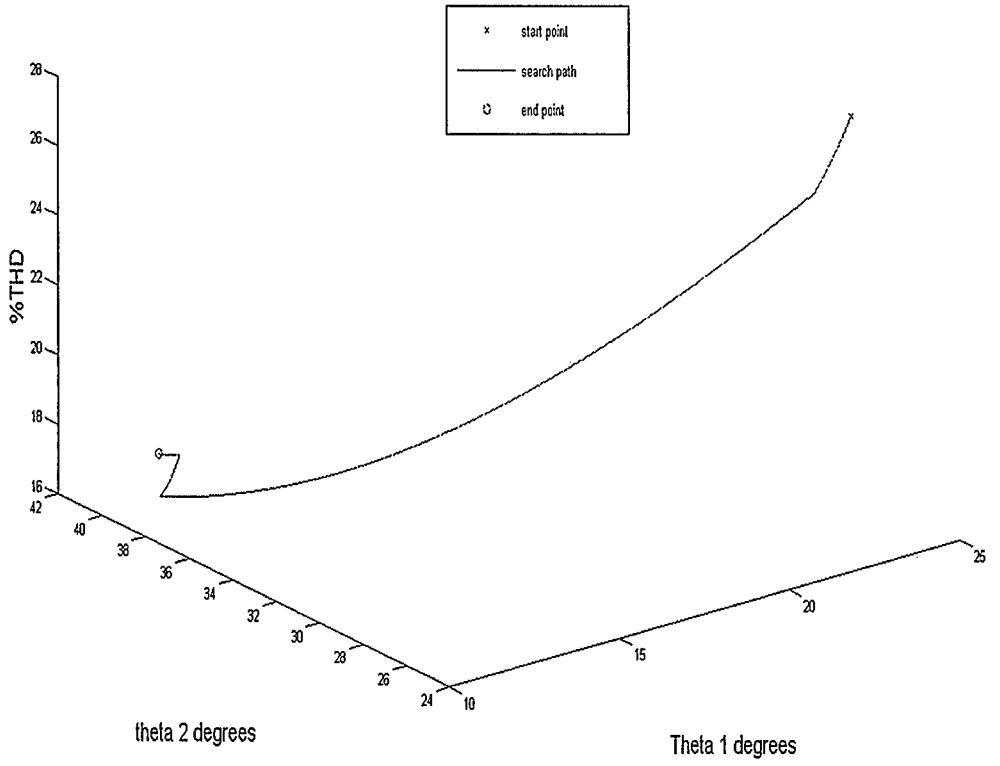


Fig. 3.18 Search path for a five-level waveform with a different starting point

Chapter Four: Practical Implementation of the System

4.1 Introduction

In this chapter the practical implementation of the second investigated technique is described in detail. The experimental set-up discussed in this chapter serves as a proof-of-concept implementation. The experimental set-up may be used for further investigations in the future. As stated in Chapter Three, the first technique is implicitly a part of the second approach, so implementing the second one will ensure that all the design requirements of the first one are fulfilled. The experimental laboratory set up is described first as a block diagram. Detailed circuit diagrams and timing figures are introduced later throughout this chapter. The topology implemented is the cascaded H-bridge voltage source multilevel inverter. Two H-bridges are used with two dc voltage sources to generate a nine-level output staircase waveform. A single chip microcomputer is used as a transistor drive controller to provide gating signals for each group of the semiconductor switches with predetermined timing sequences. Bipolar transistors are used as switching elements in the H-bridges with their necessary driving circuits. The load used is a pure resistor with an inductor of small value to simulate the traditional load in the ac load system. The inductor is chosen to be very small, putting a severe condition on the inverter, since the inductor usually suppress high frequency components in the output waveform; working in favor of the inverter circuit.

4.2 Block diagram and General Description

Fig. 4.1 depicts the basic building blocks of the practical setup. The multilevel inverter is connected to the inductive load directly. Each of the two H-bridges of the system is controlled by signals derived from a dedicated microcontroller to activate or deactivate the bipolar switching elements. This kind of modular structure may be useful in industry as well, where the addition of another dc source and H-bridge will need only the addition of another single chip microcomputer, with possible minor modifications to the timing signals subroutines, without the need to do major changes in the overall system design. For our experimental set-up both of the microcontrollers receive the same input synchronizing timing signal as a clock input from a waveform generator. A master reset signal is applied to both microprocessors simultaneously to ensure synchronized operation between the two. The microcontroller used is the PIC 16F877 manufactured by Microchip Technology Inc.

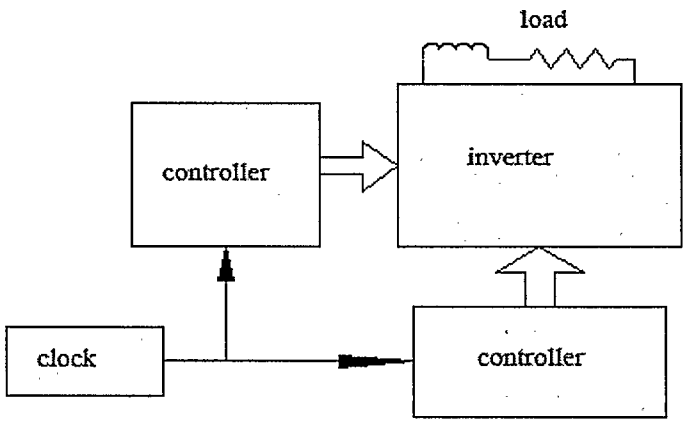


Fig. 4.1 Block diagram of the practical setup

4.3 Instruments Used in the Experimental Set-Up

The instruments used in the practical implementation of the system are as follows:

1- The digital oscilloscope used was the two-channel Tektronix TDS3032B 300 MHz with a sample rate of 2.5 Giga Samples/second for each channel.

2- High voltage differential probe; the Tektronix P5205.

3- Fluke 8050 4.5 digits, digital multi-meter.

4- Function generator; Agilent 33120A 15 MHz.

5- Fluke 39 power quality analyzer.

6- Laboratory power supplies from Brunelle Instruments and Xantrex Technology Inc.

In addition, the Microchip's PIC programmer PICSTART Plus, operated with Microchip's MPLAB Integrated Development Environment (IDE) software package is also used to program the single chip microcomputer using assembly language.

4.4 The Microcontroller PIC 16F877

This is a single chip microcomputer manufactured by Microchip Technology Inc.; the acronym stands for Programmable Intelligent Computer. These PIC's are microprocessors similar to the ones inside the personal computers, but significantly simpler, smaller and cheaper. They are optimized to deal with the real world operating relays and switches. The internal architecture of these microcontrollers consists mainly of the following components [49]:

1- The Central Processing Unit (CPU) which is the processing intelligent engine of this micro system. It performs the logic and arithmetic functions of the PIC according to the instructions stored in the program memory.

2- The program memory to store the instructions to be fetched and executed by the CPU.

3- The data memory to store the variables that the instructions are working on. The CPU reads this memory to obtain the data, and writes to this memory to store new variables or change the existing ones.

4- The input and output ports to communicate with the outside world, by transferring control signals or data to or from the surrounding circuits and systems.

5- Special purpose function blocks built inside the PIC; such as timers, analog to digital converters, and pulse width modulation circuits.

In addition to the above specifications of the internal architecture of the PIC family of microprocessors, some of the core features can be summarized as follows:

- High performance Reduced Instruction Set Computer (RISC) CPU
- 35 single word instructions for programming
- All instructions are single cycle except for branch instructions which are two-cycle
- Low power high speed CMOS FLASH/EEPROM technology
- DC-20MHz clock speed input; up to 200 ns instruction cycle
- Up to 8K x 14 words of FLASH program memory
- Up to 368x8 bytes of data memory (RAM)

- Up to 256x8 bytes of EEPROM data memory
- Wide operating voltage range: 2.0V-5.5V
- 10-bit multi-channel analog to digital converter

The outputs of each microcontroller are connected to each of the two H-bridge circuits of the system, with each transistor receiving a separate gating signal. In this way, the addition of any H-bridge circuit to the system will require only the addition of another microcontroller, reducing the software complexity. Assembly language listing and flowchart of the program used are given in the Appendix.

4.5 Practical H-Bridge Implementation

The dc voltage sources in the H-bridges have separate ground connections for each one, and the practical circuit implementation must sustain this separation, in order for the system to function properly. That is why the design has to keep the isolation between the ground of the gating signals of the switching transistors and the ground of the H-bridge circuits. An opto-coupler is used in the design to achieve this part of the job. Fig. 4.2 depicts one leg of the practical implementation of the H-bridge circuits used in the system. This leg is only half the complete H-bridge circuit. Four of these legs are required to build the complete multilevel inverter that consists of two H-bridge circuits. Gating signals for the semiconductor switches in these legs are generated by the two microcontrollers; the PIC16F877 of Microchip Technology, Inc. These signals are interfaced with the switching transistors using Fairchild Semiconductor's 4N32 general purpose 6-pin photo Darlington opto-couplers. The voltage source V2 shown is one of the

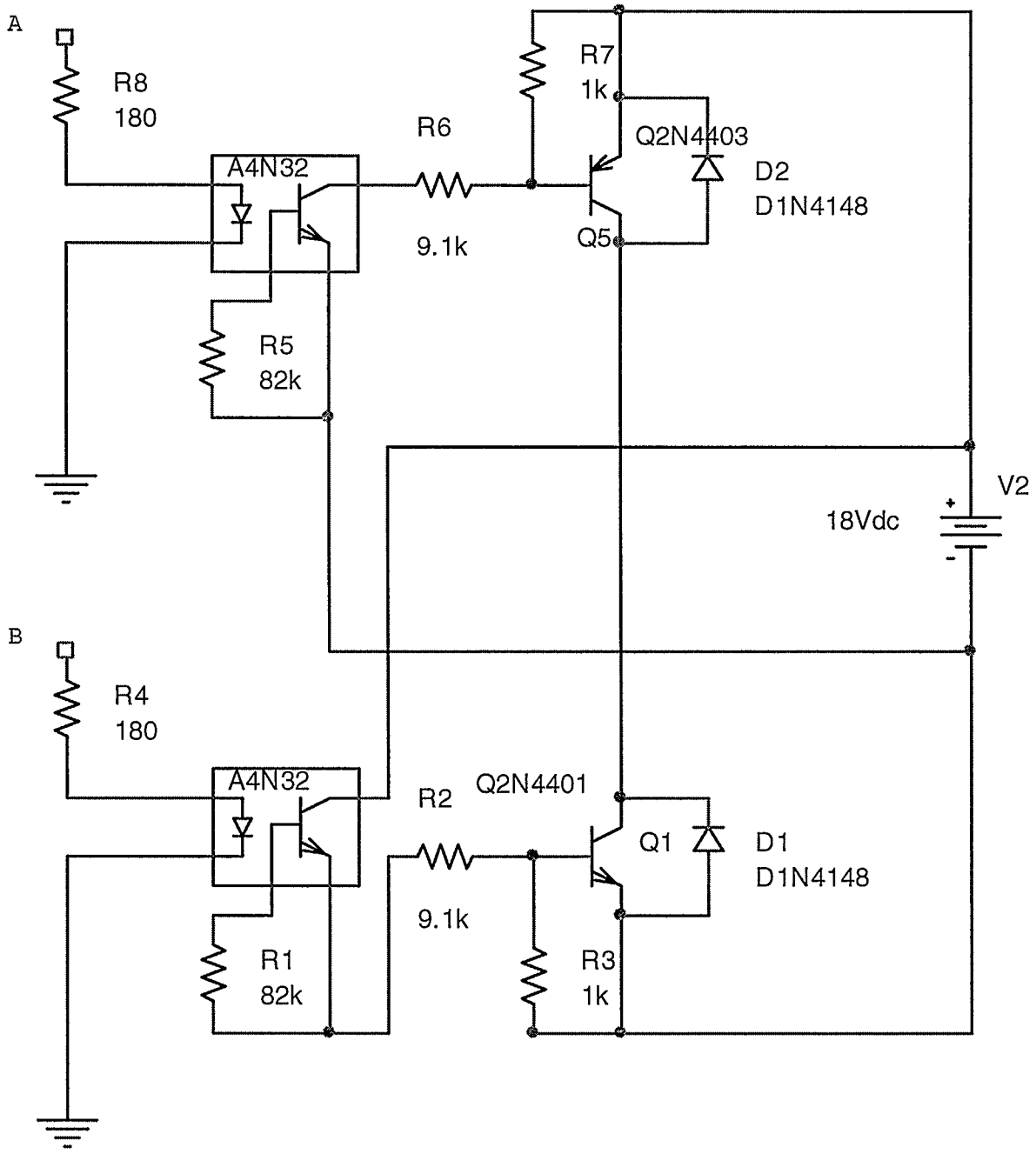


Fig. 4.2 One leg of the H-bridge used in the practical implementation of the system

two dc voltage sources used in the set up. The diodes 1N4148 are the freewheeling diodes used to bypass currents in the opposite direction of the normal transistor current direction,

thus protecting the switching transistors from damage due to the current flowing as a result of the stored energy in inductive loads while the transistors are turned off. The points A and B are the control signals originating from the microcontroller to decide the switching states of the transistors; whether on or off. The actual implementation for the V1 voltage source consisted of a power supply connected to a capacitor through a diode, to simulate a rechargeable voltage source; while V2 does not need to be rechargeable, since it is the highest value source in the system; as stated earlier in chapter 3.

4.6 Practical Results

The synchronization unit is shown in Fig. 4.3. The external clock source is implemented using the function generator, the Agilent 33120A, mentioned previously. The frequency taken from this generator is 4 MHz, this will be divided by 4 internally by the microcontroller to yield a 1 MHz clock. Thus the time period for one cycle of the microcontroller is 1 microsecond. Also, connected to both controllers is the master reset of the system, acting as another synchronizing signal that can force both microcontrollers to tart operation at the same time.

Timing of the gating signals of the H-bridges is calculated according to the approach described earlier in chapter 2, where the switching angles of the output staircase waveform has to take place at the median point between any two voltage levels. For equal voltage steps, V2 has to be equal to 3V1. In the current practical set up, V1 is chosen to

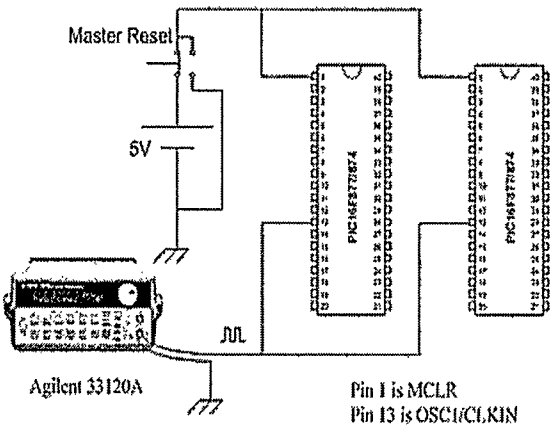


Fig. 4.3 Synchronizing the operation of the two microcontrollers

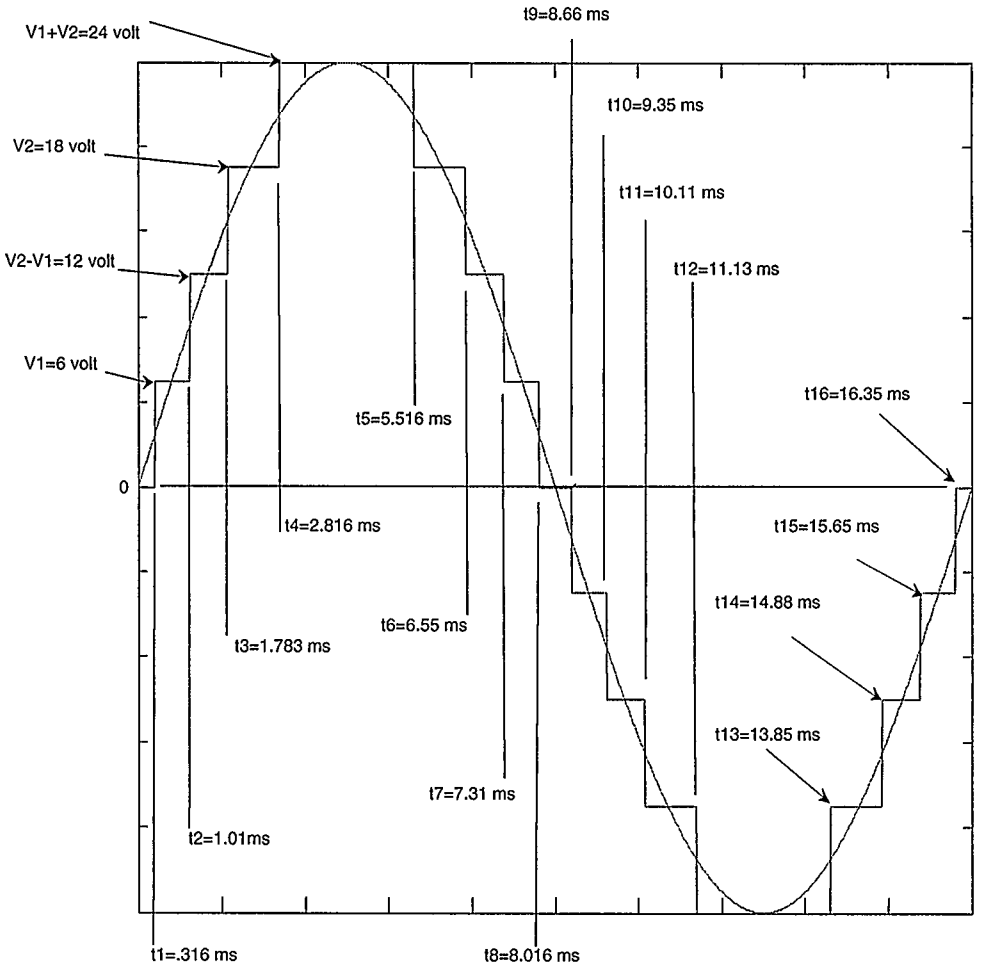


Fig. 4.4 Switching times for the practical set up (simulated waveform)

be 6V and V2=18V; the step voltage being 6V. Fig. 4.4 depicts the desired staircase waveform and its fundamental frequency component with the switching times calculated according to the median value approach described above. These times are given in the figure for a fundamental frequency of 60 Hz. The angles in degrees, according to the values of time intervals shown in Fig. 4.4 are: $\theta 1=6.84^{\circ}$, $\theta 2=21.81^{\circ}$, $\theta 3=38.51^{\circ}$ and $\theta 4=60.82^{\circ}$. Fig. 4.5 sketches the main parts of the system, represented by the two groups of switching components; where each group constitutes one H-bridge, and the two dc voltage sources; each one of them connected to an H-bridge. No freewheeling diodes or control circuitries are shown here. From this figure and Fig. 4.4, Table 4.1 is constructed.

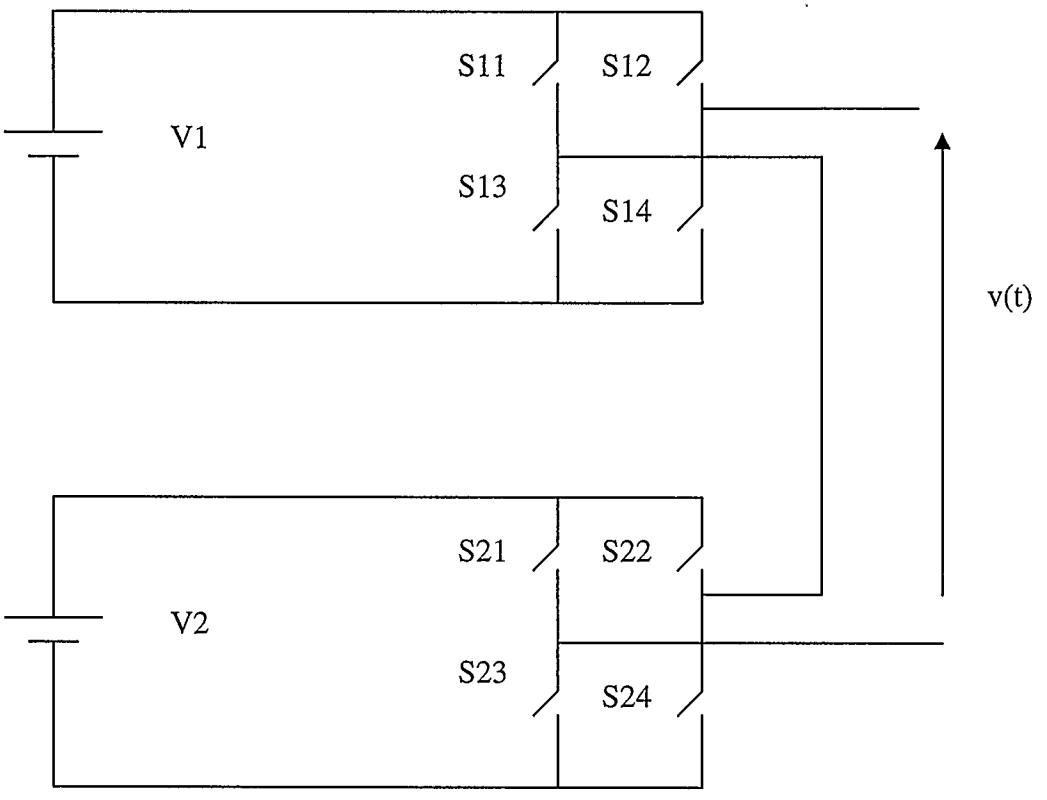


Fig. 4.5 DC voltage sources and switches of the H-bridges of the system

This table gives the states of the eight switches in the system and the exact time of each state. In this table, a "1" represents a closed switch, and "0" represents an open switch.

Table (4.1) Pattern of the States for the Switching Components of the System

Time	v(t)	S21	S22	S23	S24	S11	S12	S13	S14
t0-t1	0	0	0	1	1	0	0	1	1
t1-t2	V1	0	0	1	1	0	1	1	0
t2-t3	V2-V1	0	1	1	0	1	0	0	1
t3-t4	V2	0	1	1	0	0	0	1	1
t4-t5	V1+V2	0	1	1	0	0	1	1	0
t5-t6	V2	0	1	1	0	0	0	1	1
t6-t7	V2-V1	0	1	1	0	1	0	0	1
t7-t8	V1	0	0	1	1	0	1	1	0
t8-t9	0	0	0	1	1	0	0	1	1
t9-t10	-V1	0	0	1	1	1	0	0	1
t10-t11	-V2+V1	1	0	0	1	0	1	1	0
t11-t12	-V2	1	0	0	1	0	0	1	1
t12-t13	-V1-V2	1	0	0	1	1	0	0	1
t13-t14	-V2	1	0	0	1	0	0	1	1
t14-t15	-V2+V1	1	0	0	1	0	1	1	0
t15-t16	-V1	0	0	1	1	1	0	0	1

Equation (3.6) can be invoked here to evaluate the magnitude of any harmonics in the output waveform analytically; since we have the condition of equal voltage steps, each step is equal to V1. Knowing that there are four switching angles in the output waveform of Fig. 4.5, equation (3.6) can be rewritten in the following form

$$H(n) = \frac{4V1}{n\pi}(cos(n\theta 1) + cos(n\theta 2) + cos(n\theta 3) + cos(n\theta 4)), \text{ n=1, 3, 5, 7...} \quad (4.1)$$

Equation (4.1) gives the magnitude of the peak value of any desired harmonic frequency of order n in the output staircase waveform. The fundamental frequency component can be evaluated by setting n=1 in equation (4.1) above, this yields the following:

$$H(1) = \frac{4V1}{\pi}(cos(\theta 1) + cos(\theta 2) + cos(\theta 3) + cos(\theta 4)),$$

For the specific angle values given above in the present case, the cosine terms will add up to the value of π with a good approximation (about 1% accuracy), reducing the above expression of H(1) to the following:

$$H(1) = 4V1$$

This ensures that the switching angles chosen give the fundamental sinusoidal waveform that has a peak value of 4V1; with V1=6v, the peak of the fundamental is equal to 24V in our case. Any other desired harmonic component can be calculated similarly by substituting the order n of that harmonic in equation 4.1 using the same angle values.

The practical waveforms generated at the output of the inverter are converted into data files by the oscilloscope and taken to the computer to be drawn and analyzed by

MATLAB. Fig. 4.6 depicts the output waveform generated by the experimental set up of the system; its spectrum is shown in Fig. 4.7. The inductor value used in series with the load is chosen to be 300 μH with a load resistance of 180 Ω. It can be noted that Figs. 4.7 and 4.8 are very similar to the theoretical waveforms presented earlier in the previous chapter Figs 3.7 and 3.8. The value of THD is 9.38%. For comparison purposes, one cycle of this practical output is plotted on the same graph with the theoretical output, as shown in Fig. 4.8. The spectra of both outputs are plotted also on the same graph in Fig. 4.9 up to the 50^{th} harmonic. The results are very close to each other.

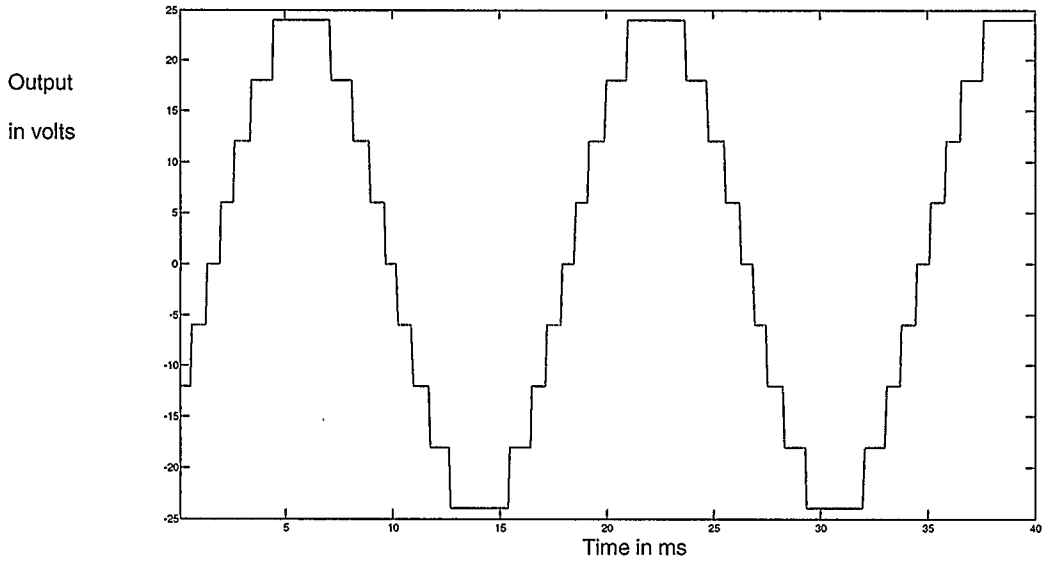


Fig. 4.6 Experimental output staircase waveform of the implemented inverter

4.7 Discussion

It might be useful to discuss some of the issues and points that may provide us more insight into the industrial environment in which these inverters are required to operate.

One of the points to be discussed here is the effect of the constraints imposed on the values of the contributing dc voltage sources, i.e. the difference in the values of the voltage sources that constitutes the main power source in the system. How practical are these constraints? And what is the effect of using such constrained voltage values on the overall performance of the proposed system? To answer these questions and others, it may be useful to go back to the original output waveform of the conventional approach

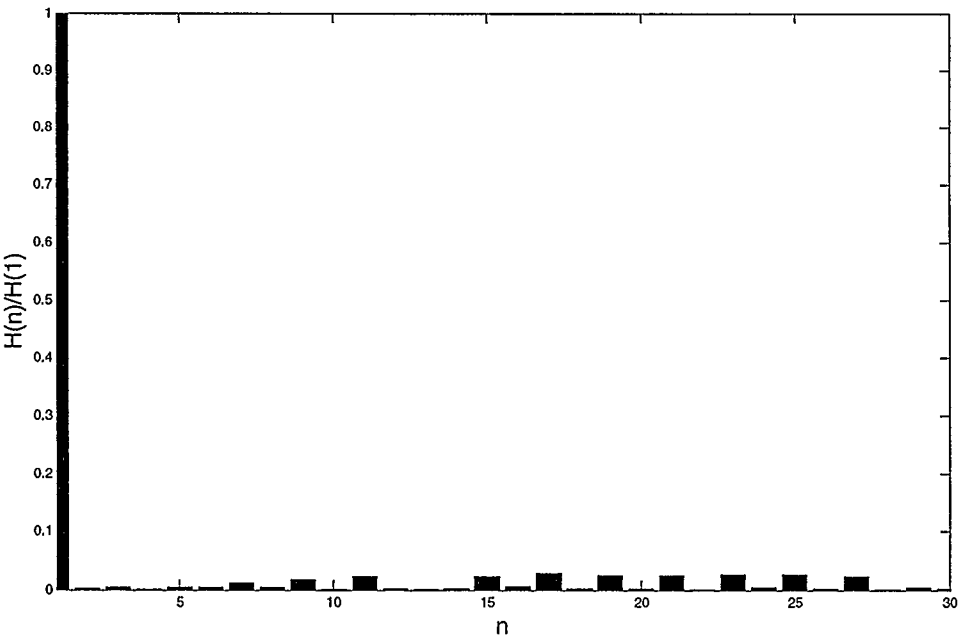


Fig. 4.7 Spectrum of the output waveform of the experimental set up

with two dc voltage sources as depicted in Fig. 2.2. It can be seen that although the two dc sources have equal voltage values, i.e. V1=V2; which makes the system modular in nature; the power drawn from the two sources are not the same. The dc voltage source of the first voltage level (H-bridge 1) will bear the majority supplied power for the system,

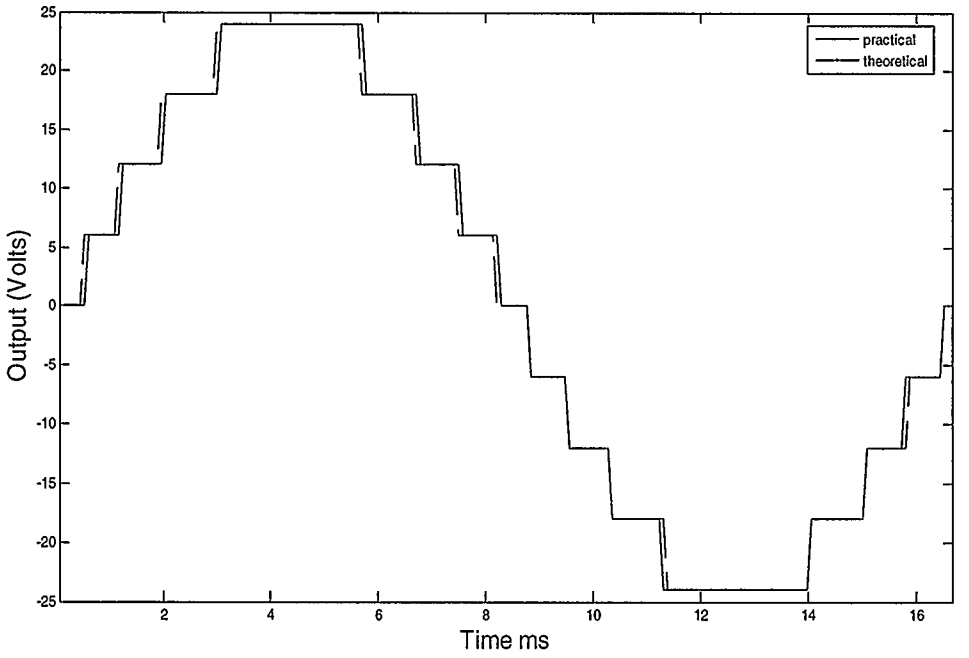


Fig. 4.8 One cycle of the practical and theoretical outputs

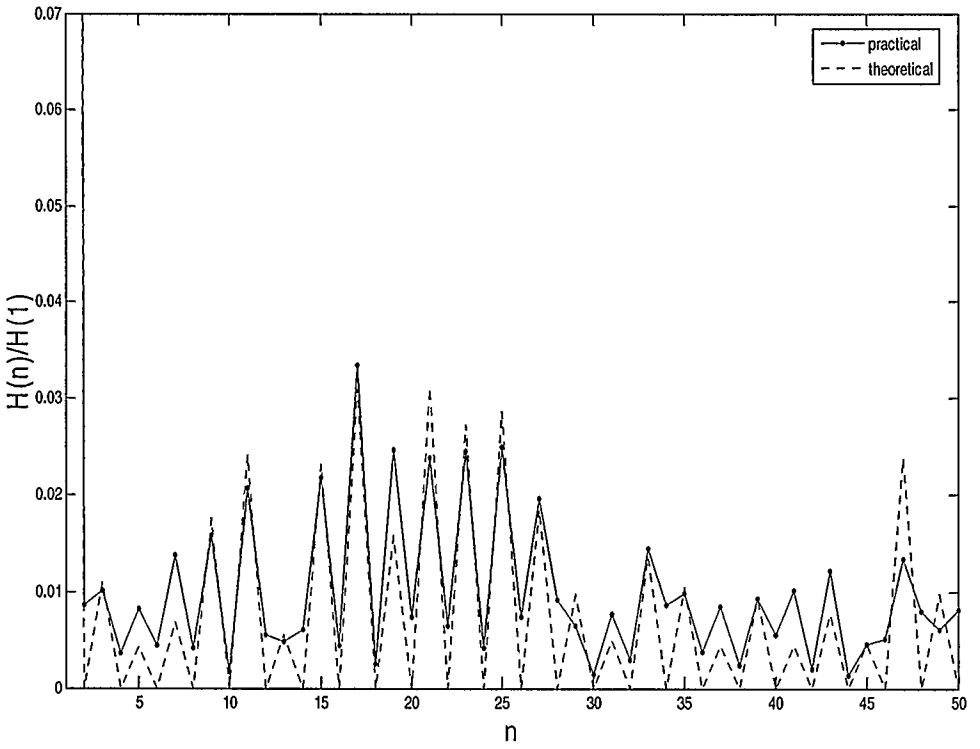


Fig. 4.9 Comparison of the spectrum of the practical and theoretical outputs

since $\theta 2 > \theta 1$; while the dc source supplying (H-bridge 2) current after $\theta 2$ and contributing to the second voltage level will have the lowest burden of power delivery; being at rest for approximately half of the sinusoidal cycle. If these two sources are identical in everything; including the nature of voltage generation (e.g. from a solar or fuel-cell source), then both may have the same Volt-Ampere ratings. This is of course inconsistent with the power delivery inequality just described. One of the solutions to this problem is the swapping of the switching pattern every half cycle to ensure equivalent power distribution among the contributing dc sources [46].

Swapping of the switching pattern as described above can only be implemented with equal dc voltage sources. Moreover, it puts additional requirements on the control circuitry. In the approach presented here, there is the difference in voltage values between any two sources that is necessary to achieve the increase in number of steps of the output waveform. The voltage sources are not identical any more with the proposed approach, nor are the power (Volt-Ampere) capabilities of each source. Most of the power drawn by the load will be taken from the voltage source having the highest voltage value among the dc sources, then comes the next lower voltage source, then the lower, and so on. These voltages now can be taken from sources that are different in nature, size; and definitely, power rating. For example, they can be taken from two solar panels, with each one having different voltage and power capability.

One of the clear advantages of the approaches presented in this thesis, which results from the increase of the output step levels, is the reduced requirements imposed on the voltage

switching capabilities of the transistors. The increase in the number of steps will divide the total voltage of the output waveform into more steps to be switched among by the transistors. This means the characteristics of the switching scheme can make it cheaper for the system to be constructed by using semiconductors having lower voltage switching ratings in the circuit. That is one of the advantages of the multilevel inverter in general. It is emphasized with the current work.

From the figures of the switching pattern of the contributing dc voltage sources for both techniques, as seen in Figs. 3.3 and 3.4, it can be noted that both techniques place greater switching frequency requirements on the lower voltage sources and less switching frequency requirements on the higher value dc voltage sources. The higher switching frequency of Va1 for example in Fig. 3.4 is justified since this is the output of the H-bridge connected to the lower voltage source, and switching lower voltages more frequently imposes a lower requirement on the switching semiconductor devices than the case of high voltage switching. The higher voltage of Va2 is switched only once in the first half cycle, as would be the case for the largest dc voltage source where more than two dc sources are present in the system.

One of the requirements of the current scheme is that the lower voltage sources have to be rechargeable. That constraint is imposed on all the contributing dc voltage sources, except the highest value source designated as Vm. In practice, and in many applications, this is the case for any dc source used in the system, even for the highest value source. For those dc voltage sources used in systems categorized as "renewable energy sources",

the dc sources are usually charged by power taken from solar, wind or other sources, storing the energy of these sources in rechargeable batteries. This means that the batteries are usually rechargeable, and this requirement is thus not a problem in practice. What can be raised here as a question of possible concern is that the system might experience power loss because the lower voltage batteries are being charged by the higher value batteries in the system (i.e., the movement of charge from one battery to another is inherently a lossy process). An important and obvious point can be made about this. In the conventional approach, much more power is being wasted with harmonics that may even be harmful to the system and its environment. Actually, in the proposed approach, the system is not consuming much power from the harmonics; since they are so small in value compared to the conventional approach.

One last comment is to be mentioned. The increase in voltage levels can introduce the possibility of eliminating specific harmonics in addition to the original objective discussed in this thesis of reducing the THD. As the number of levels is increased, the number of the angles $\{\theta i\}$ in the harmonic equations is increased also; and consequently the number of harmonic equations is increased too. This enables the elimination of more specific harmonics in the output waveform compared to the case of the traditional technique. As stated earlier in section 2.5, the number of harmonics that can be eliminated in a staircase waveform depends mainly on the number of harmonic equations that can be derived from that specific waveform; and this is mainly dependent on the number of switching angles in that waveform. The example of the 9 level practical output waveform in this chapter is clear. Instead of the capability of eliminating only one

harmonic in the five level traditional waveform using two voltage sources; three harmonics can be eliminated from the same number of voltage sources in the current approach. This can be done by appropriate choice of the values of the switching angles. Improved harmonic elimination represents another advantage of the current proposed techniques.

Chapter Five: Conclusions and Future Work

5.1 Conclusions

The work presented in this thesis may be useful for the integration of renewable energy sources into the ac power grid. The traditional method to reduce the harmonics in a multilevel inverter is to increase the number of the dc sources, as well as the number of H-bridges (or in the case of non H-bridge multilevel inverters, more semiconductor switching components are needed) in order to increase the number of levels in the output waveform. Recent advances in cascaded H-bridge design are reviewed in this thesis, that avoid the use of more dc voltage sources or more H-bridge stages to reduce the THD of the output waveform. The techniques make use of all the possible combinations of the different values of the dc voltage sources with positive and negative polarities in each half cycle to increase as much as possible the number of the output voltage levels. This increases the number of levels possible up to 3^m levels, for m dc voltage sources. This is compared to $2m+1$ levels in the conventional cascaded H-bridge approach. For two dc voltage sources, an output waveform of nine levels in the practical set up is achieved, compared to five levels with the conventional method. A considerable reduction in THD is possible with this approach. One of the prices paid for this harmonic reduction are the constraints imposed on the values of the dc voltage sources. These constraints are derived and presented in this thesis. The dc voltage sources can no longer be equal with the new approach. In addition, all but the highest value dc source must admit the flow of current in both directions (likely this is not a problem in practice). Another minor issue with the

proposed approach is the slightly intricate switching strategy of the semiconductor devices. The switching signals are different in the proposed approach compared to the conventional one. As demonstrated with a proof-of-concept practical implementation (which may be used as the basis for further investigation in the future) the switching angles for the inverter transistors can easily stored in look-up tables used by the microcontroller. The control circuitry itself does not have to be changed compared to conventional cascaded H-bridge inverter implementations.

The investigations presented in this thesis for the recent advances in cascaded H-bridge inverter design have led to the following thesis contributions:

1) The derivation of generalized harmonic equations;

2) The derivation of constraints on the dc voltage sources;

3) The development of a gradient based optimization to determine the switching instances of transistor gating signals in order to minimize the THD of the output voltage waveform; and

4) A proof-of-concept practical implementation which may be used as the basis for further investigation in the future.

5.2 Suggestions for Future Work

The work presented in this thesis did not deal with calculations of the switching angles to achieve harmonic elimination in the output spectrum, ie, the elimination of specific harmonics. The choice of switching angles for harmonic elimination is a possible

direction for future research. Perhaps the search for the values of these angles can be done using some iterative method, in a similar manner to the search described in this thesis for minimum THD. As another suggestion for possible future work, it might be of great interest to consider the use of adaptation algorithms widely used in signal processing to search for the values of these angles. This search can be done in real time, and can adjust the values of these angles practically instantaneously whenever a drift in the values of the dc voltage sources takes place, keeping the harmonic distortion in the output waveform to as low a level as possible. This kind of automatic adjustment of the switching angles can actually be part of a more general fault diagnosis system added to the main design of the inverter. The control of such activity can be done using available digital signal processors, which can be very efficient in such an application. Also worth mentioning here is the possibility of doing more research on finding new topologies that can minimize the number of semiconductor components in the system, achieving the goal of minimizing the overall cost of the inverter, and at the same time keeping the THD at the lowest attainable level.

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APPENDIX A: PIC16F877 ASSEMBLY LISTING

Following is the PIC16F877 assembly program. Fig. A.1 (a) shows a flow chart of the main program, while Fig. A.1 (b) shows flow chart of the time delay subroutine.

```
; ==================================================================
;   This program generates the gating signal (for one H-bridge) on
;   PORTA0...3, register 0x7F holds time period.
; ==================================================================
        list    p=16f877                ; list directive to define processor
        #include <p16f877.inc>          ; processor specific variable definitions
        _CONFIG _CP_OFF & _WDT_OFF & _BODEN_OFF & _PWRTE_ON &
        _XT_OSC & _WRT_ENABLE_ON & _LVP_OFF & _DEBUG_OFF
        & _CPD_OFF
        ORG     0x000                   ; processor reset vector
        clrf    PCLATH                  ; ensure page bits are cleared
        goto    main                    ; go to beginning of program
        ORG     0x004                   ; interrupt vector location
        clrf INTCON
        retfie                          ; return from interrupt

        ; delay subroutine starts
Delay
Here    decfsz 0x7F, F
        nop
        nop
        nop
        goto Here
        return
        ; delay subroutine ends

main
        bcf STATUS, RP0                 ; Bank0
        bcf STATUS, RP1                 ; initialize PORTA by
        clrf PORTA                      ; clearing output
                                        ;
        bsf STATUS, RP0                 ; Select Bank 1
```

```
        bcf INTCON, GIE          ; Configure all pins
        bsf INTCON, 4            ; as digital outputs
        movlw 0x06               ; Value used to
        movwf ADCON1             ; initialize data
        movlw 0xC0               ; direction
        movwf TRISA
        bcf STATUS, RP0          ; Select Bank 0

LoopMain
        ; beginning of one output period
        movlw b'00000011'        ; load PORTA with the binary
        movwf PORTA              ; value 00000011
        movlw .53                ; load 0x7F with 09
        movwf 0x7F
        call Delay               ; call Delay subroutine

        movlw b'00000110'
        movwf PORTA
        movlw .116
        movwf 0x7F
        call Delay
        .
        .
        .
        ; end of one output period
        goto LoopMain            ; jump to LoopMain
        END                      ; directive 'end of program'
```

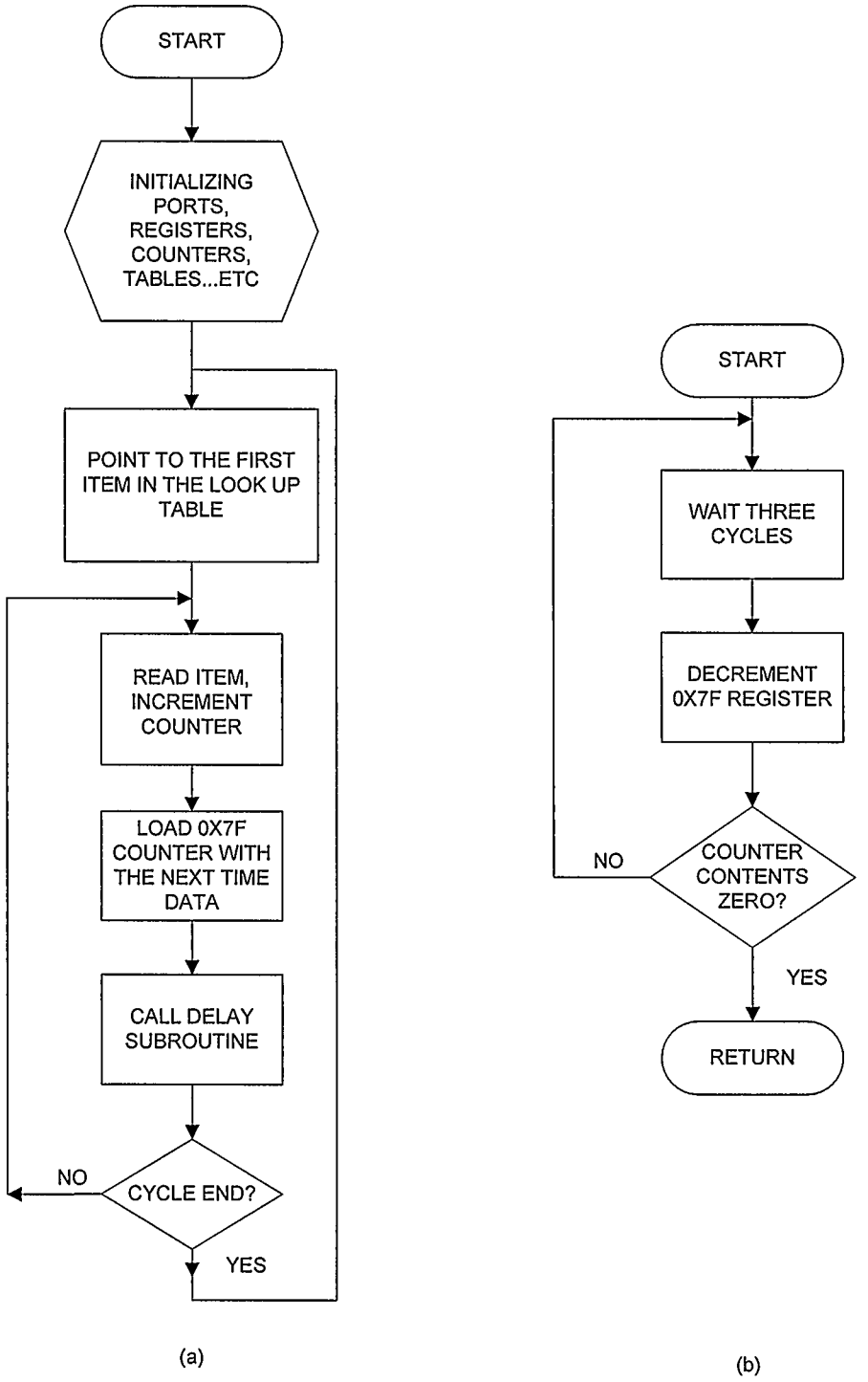

Fig. A.1 Flow chart of (a) the main PIC 16F877 program; (b) the time delay subroutine

APPENDIX B: MATLAB LISTING

In the following is a listing of MATLAB .m file for generating some signals used in the theoretical analysis and calculating the spectrum for them.

```
%clear all variables
clear
%f is frequency in Hz
f=1;
% define M number of DC voltages dcv
M=2;
% generate sinewave signal x
%define number of points for the signal, N
N=1000;
for n=1:N,
   % t is time
   t(n)=n/N;
   % define axis for the graph tt
   tt(n)=t(n)*N;
   angle(n)=t(n)*360;
   %tt_1(n)=tt(n)-1;
```

```
   x(n)=sin(2*pi*f*t(n));
end
% find spectrum
spectrum=abs(fft(x,N));
%start multilevel converter process
%first define step voltage for traditional approach vstep
 vstep=1/M;
 for n=1:N,
vstair(n)=0;
end
for n=1:N
vdc1(n)=0;
vdc2(n)=0;
end
vup=0;
vdown=0;
for n=2:N,
   if abs(x(n)-vstair(n-1))>=vstep/2.0
         if x(n)-x(n-1)>=0
            vstair(n)=vstair(n-1)+vstep;
%              toggle vdc1
         elseif x(n)-x(n-1)<0
            vstair(n)=vstair(n-1)-vstep;
```

```
            %toggle vdc1
        end
    else
        vstair(n)=vstair(n-1);
        vdc1(n)=vdc1(n-1);
        vdc2(n)=vdc2(n-1);
    end
end
figure(9);
plot (angle,vstair,'b',angle,x,'r')
axis ([0 360 -1 1])
figure (10);
spectrum_traditional=abs(fft(vstair,N));
for n=2:N
spectrum_traditional_correct(n-1)=spectrum_traditional(n);
end
for n=1:N-1
  spct(n)=(spectrum_traditional_correct(n))/(spectrum_traditional_correct(1));
end
bar(spct(1:34),'k')
axis([1 29 0 1])
title 'Spectrum of the traditional approach'
vdc1=vstep*vdc1;
```

```
vstep=0;
for n=M:-1:1,
   vstep=2^(n-1)+vstep;
   %dcv(n)= dcv(n+1)/2;
   %vstair_max=vstair_max + dcv(n)
end
vstep=1/vstep;
%start generating staicase sinewave vstair
for n=1:N,
vstair(n)=0;
end
for n=1:N
vdc1(n)=0;
end
vup=0;
%start binary sequence levels
for n=2:N,
      if  abs(x(n)-vstair(n-1))>=vstep/2.0
         if x(n)-x(n-1)>=0
            vstair(n)=vstair(n-1)+vstep;
            %              toggle vdc1
            if vup==0
               vup=1;
```

```
            else vup=0;
            end
        elseif x(n)-x(n-1)<0
            vstair(n)=vstair(n-1)-vstep;
            %toggle vdc1
            if vup==0
               vup=1;
            else vup=0;
            end
        end
    else
        vstair(n)=vstair(n-1);
    end
        if vup==1
        vdc1(n)=1;
    end
end
spectrum_new=abs(fft(vstair,N));
figure(5);
for n=2:N
spectrum_new_correct(n-1)=spectrum_new(n);
end
for n=1:N-1
```

```
spct_new(n)=spectrum_new_correct(n)/spectrum_new_correct(1);
end
bar(spct_new(1:34),'k')
title 'Spectrum of the present approach'
vdc1=vstep*vdc1;
for n=1:1000
   v1(n)=0;
end
for n=27:84,
   v1(n)=1;
end
for n=157:344,
   v1(n)=1;
end
for n=417:474
   v1(n)=1;
end
for n=527:584
   v1(n)=-1;
end
for n=657:844
   v1(n)=-1;
end
```

```
for n=917:971
   v1(n)=-1;
end
v1=.3333*v1;
figure(3);
subplot(3,1,1),plot (tt,vstair,'b',tt,x,'r')
subplot(3,1,2), plot(v1),
title 'Variations of V1', ylabel 'volts',
for n=1:1000
   v2(n)=0;
end
for n=84:417,
   v2(n)=1;
end
for n=584:917,
   v2(n)=-1;
end
v2= .6666*v2;
subplot (3,1,3), plot (v2),
title 'Variations of V2',
ylabel 'volts',
thd_old=0;
for n=3:N/2,
```

```
   thd_old = (spectrum_traditional(n)^2)+thd_old;
end
thd_old=sqrt(thd_old/spectrum_traditional(2)^2)
thd_new=0;
for n=3:N/2,
   thd_new =spectrum_new(n)^2+thd_new;
end
thd_new=sqrt(thd_new/spectrum_new(2)^2)
```

APPENDIX C: VERIFICATION OF HARMONIC EQUATIONS

A. Verification of Equation (3.10)

Equation (3.10) is shown here for convenience:

$$H(n)=\frac{4}{n\pi}\sum_{j=1}^{m}Vj\sum_{i=1}^{2^{m-j+1}-1}(-1)^{i+1}\cos\left(n\theta_{2^{j-1}(i)}\right),\qquad n=1,3,5..(3.10)$$

Consider the specific cases as follows:

m=1,

j=1 to 1,

i=1 to 1:

$$H(n)=\frac{4}{n\pi}V1\cos(n\theta 1)$$

m=2,

j=1 to 2

j=1 ,

i=1 to 3, yielding the term V1[cos(nθ1) −cos(nθ2)+cos(nθ3)]

j=2,

i=1 to 1 yielding V2[cos(nθ2)], the final equation is

$$H(n)=\frac{4}{n\pi}\{V1[\cos(n\theta 1)-\cos(n\theta 2)+\cos(n\theta 3)]+V2[\cos(n\theta 2)]\}$$

m=3

j=1 to 3

j=1

i=1 to 7, yielding

V1[cos(nθ1) −cos(nθ2)+cos(nθ3)- cos(nθ4)+cos(nθ5)-cos(nθ6)

+cos(nθ7)]

j=2

i=1 to 3 yielding

V2[cos(nθ2) −cos(nθ4)+cos(nθ6)]

j=3

i=1 to 1 yielding

V3 [cos(nθ4)], the final equation is

$$H(n) = \frac{4}{n\pi}\{$$ V1[cos(nθ1) −cos(nθ2)+cos(nθ3)- cos(nθ4)+cos(nθ5)-

cos(nθ6) +cos(nθ7)] + V2[cos(nθ2) −cos(nθ4)+cos(nθ6)] + V3 [cos(nθ4)]}

Going quickly on the case of

m=4

j=1 to 4

j=1

i=1 to 15

V1 [cos(nθ1) − cos(nθ2) + ...+cos(nθ15)]

j=2

i=1 to 7

V2 [cos $(n\theta 2) - \cos(n\theta 4) + \cdots + \cos(n\theta 14)$]

j=3

i=1 to 3

V3 [$\cos(n\theta 4) - \cos(n\theta 8) + \cos(n\theta 12)$]

j=4

i=1 to 1

V4[$\cos(n\theta 8)$]

This is consistent with the results presented in Table 3.2

B. Verification of Equation 3.16

Equation 3.16 is shown here for convenience:

$$H(n) = \frac{4}{n\pi}\{\sum_{j=1}^{m-1} Vj\,[\sum_{i=0}^{\frac{3^{m+1-j}-3}{2}} \cos\left(n\,\theta_{3^{j-1}i+\frac{1}{2}(3^{j-1}+1)}\right) - 3\sum_{k=0}^{\frac{3^{m-j}-3}{2}} \cos\left(n\theta_{3^j k+\frac{3^j+1}{2}}\right)]$$

$$+ V_m \cos(n\theta_{\frac{3^{m-1}+1}{2}})\}, \qquad n = 1,3,5 \ldots \quad (3.16)$$

m=1, only the term of Vm will be present yielding $H(n) = \frac{4}{n\pi}$V1 [cos(nθ1)]

Consider the cases for m>1:

m=2

j=1 to 1

i=0 to 3 and k=0 to 0 yielding

V1 [cos($n\theta$1) + cos($n\theta$2)+cos($n\theta$3) + cos($n\theta$4)]- 3V1 [cos($n\theta$2)]

+V2 [cos($n\theta$2)]

m=3

j=1 to 2

When j=1

i=0 to 12

k=0 to 3

The subscript of theta in the first summation is i+1= 1, 2, 3, .., 13

The subscript of theta in the second summation is 3k+2= 2, 5, 8, 11

This yields the following terms in V1

$$V1[\cos(n\theta 1) + \cos(n\theta 2) + \cos(n\theta 3) + .. + \cos(n\theta 13)] - 3V1[\cos(n\theta 2) + \cos(n\theta 5) + \cos(n\theta 8) + \cos(n\theta 11)]$$

which is consistent with Table 3.3.

When j=2

i=0 to 3 and k=0 to 0

the subscript of theta in the first summation will be 3i+2= 2, 5, 8, 11

and in the second summation it will be 9k+5=5, giving the terms in V2 to be:

$$V2[\cos(n\theta 2) + \cos(n\theta 5) + \cos(n\theta 8) + \cos(n\theta 11)] - 3V2[\cos(n\theta 5)]$$

which is also consistent with Table 3.3.

and the last term is $V3[\cos(n\theta 5)]$

m=4

j=1 to 3

when j=1

i=0 to 39

k=0 to 12

the subscript in the first summation is i+1= 1, 2, 3, …,39, 40

in the second summation it is 3k+2= 2, 5, 8, 11, 14, 17, 20, ..35, 38

This yields:

$$V1[\cos(n\theta 1) + \cos(n\theta 2) + \cos(n\theta 3) + .. + \cos(n\theta 40)] - 3V1[\cos(n\theta 2) + \cos(n\theta 5) + \cos(n\theta 8) + \cos(n\theta 11) \ldots + \cos(n\theta 38)]$$

which is consistent with Table 3.3.

j=2

.

And so on...

The last term of the equation is $V4[\cos(n\theta 14)]$