THE UNIVERSITY OF CALGARY

HIGH-PRECISION VOLTAGE-TO-FREQUENCY CONVERTERS

by

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The undersigned certify that they have read, and recommended to the Faculty of Graduate studies for acceptance, a thesis entitled, "High-Precision Voltage-to-Frequency Converters," submitted by Chun On Li in partial fulfillment of the requirements for the degree of Master of Science.

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ABSTRACT

A family of high-precision voltage-to-frequency converters (VFCs) based on the charge balance principle is presented in this thesis. VFCs serve as an important building block in instrumentation circuits and are particularly useful in analog-to-digital conversion. A basic free-running VFC is presented as an illustration of the charge balance principle and the techniques of providing voltage gain, linearization, dual-supply operation, and instantaneous voltage-to-frequency conversion from the basic circuit structure. A clock-synchronized version of the basic VFC and a clock-controlled VFC are then presented. High-precision analog-to-digital conversion utilizing the inverse-counting technique are also described. These two VFCs are implemented with discrete components and tested. They are found to provide analog-to-digital conversion with resolution of 0.1 ppm (part per-million) of full scale, maximum nonlinearity of 2 ppm of full scale, and temperature drift of 0.1 ppm per degree Celsius.

The steps for implementing the VFCs in integrated circuits are also outlined. An integrated amplifier suitable for VFC applications is designed and tested. The technique of fully integrating a high-precision VFC system using the commutating auto-zeroing scheme is also described.

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DEDICATION

to Susan

for her love and encouragement

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LIST OF SYMBOLS

f_c	System Clock Frequency
f_{in}	Input Frequency for the Frequency-to-Voltage Converter
f_{inst}	Instantaneous Output Frequency in Direct Frequency Conversion
$f_{\max}$	Maximum Input Frequency for the Frequency-to-Voltage Converter
f_o	VFC Output Frequency
$f_{o_{ave}}$	Average VFC Output Frequency
f_z	Chopping Frequency for the Chopper-Stablized Amplifier
I_B^-	Op-Amp Input Bias Current
I_Q^+	Op-Amp Non-inverting Input Current due to Charge Pumping
I_Q^-	Op-Amp Inverting Input Current due to Charge Pumping
M	Total Number of Clock Pulses within the Conversion Time when the VFC Output is High
m	Number of Clock Pulses within One VFC Pulse
N	Total Number of Clock Pulses within the Conversion Time
n	Total Number of VFC Output Pulses within the Conversion Time
r_d	Difference between the High and Low Output Resistances of Six CMOS Inverters in Parallel
r_h	Output Resistance of Six Parallel CMOS Inverters at the High State
r_l	Output Resistance of Six Parallel CMOS Inverters at the Low State
T_c	System Clock Period
$T_{convert}$	Conversion Time
T_{in}	Input Period for the Frequency-to-Voltage Converter
T_o	VFC Output Period

LIST OF SYMBOLS (Continued)

$T_{o_{ave}}$	Average VFC Output Period
T_p	VFC Output Pulse Width
$T_{p_{ave}}$	Average VFC Output Pulse Width
T_{switch}	Time for which the Convert-Command Switch is Closed
t	Temperature
t_d	Difference between the Rise and Fall Times of the VFC Output
t_f	Fall Time of the VFC Output Waveform
t_o	Instantaneous Output Period in Direct Frequency Conversion
t_r	Rise Time of the VFC Output Waveform
V_{cm}	Common-Mode Input Voltage
V_{dd}	Positive (or Higher) Power-Supply Voltage
V_{ip}	Non-inverting Input Voltage of an Operational Amplifier
V_{in}	Inverting Input Voltage of an Operational Amplifier
V_{out}	Output Voltage
V_{oave}	Average Output Voltage
V_{os}	Op-Amp Input Offset Voltage
V_{ref}	Reference (or Supply) Voltage
V_{ss}	Negative (or Lower) Power-Supply Voltage
V_t	VFC Input Voltage
V_t'	VFC Input Voltage with Op-Amp Non-ideal Effects
V_{tn}	Threshold Voltage of an N-channel Transistor
V_{tp}	Threshold Voltage of a P-channel Transistor

LIST OF SYMBOLS (Continued)

V_z	Auto-Zeroing Reference Voltage
η	Ratio of Threshold Voltage to Power-Supply Voltage of a CMOS Gate

CHAPTER 1

INTRODUCTION

1.1 Functions of Voltage-to-Frequency Converters

A voltage-to-frequency converter (VFC) is a device which produces an output waveform with characteristics dependent on its input voltage. Depending on applications, there are several kinds of VFCs with very subtle differences among their output characteristics.

The most basic function of a VFC is depicted in Fig.1.1(a), in which a dc voltage input is converted into an output pulse train in which the instantaneous frequency is linearly proportional to the input voltage. This VFC is in effect an analog-to-digital (A/D) converter that produces a serial digital output which can be transmitted over cables, optical fibers, and radio channels. Direct counting of the output with frequency counters will then provide a direct digital read-out [1]. One typical application of this VFC is in temperature and pressure sensing in oil or gas reservoirs, where non-linear transducer outputs are measured and transmitted over a long distance for processing or direct reading [2]. A free-running VFC with some form of signal linearization capability and which can be operated from a single-ended supply is best suited for this purpose.

A free-running VFC can be designed to produce an output waveform with pulse-width-to-period ratio proportional to its input voltage, as depicted in Fig.1.1(b). Since

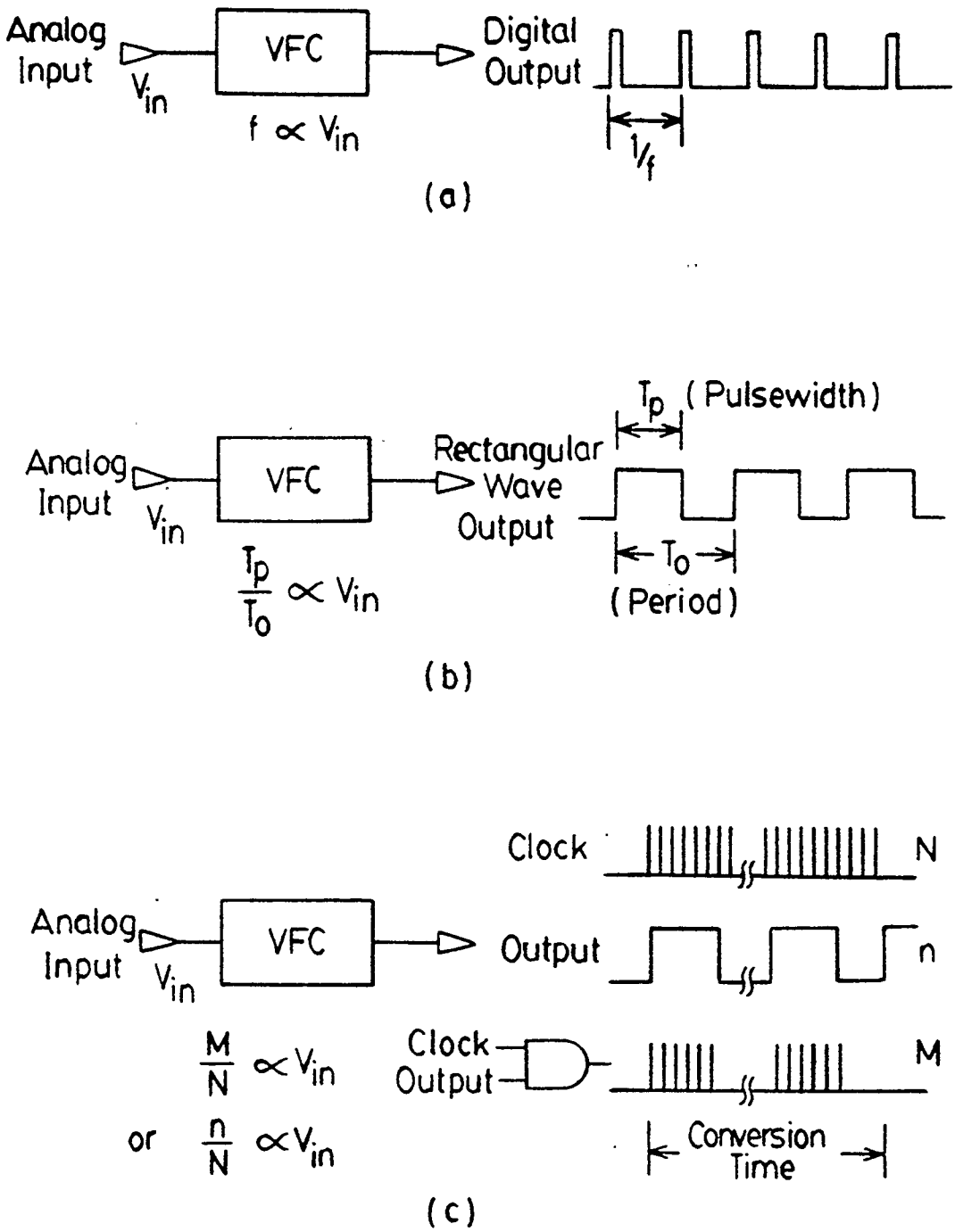


Fig.1.1 VFCs with Different Output Characteristics: VFC Output for
(a) Direct Frequency Measurement
(b) Instantaneous Pulse Width-to-Period Ratio Measurement
(c) Average Pulse Width-to-Period Ratio Measurement

such a VFC can also be designed to produce an output frequency proportional to its input voltage, it can always be used in the application described above. The additional advantage of this VFC is that it can now transmit two variables via a single output since both the pulse-width and the period can now individually convey information.

The third type and perhaps the most important type of VFCs are those with average output pulse-width-to-period ratio proportional to the input voltage over a certain conversion time, as described in Fig.1.1(c). Such a VFC is often synchronized with a high-frequency crystal clock so that the pulse-width and period can be measured to within one clock cycle. As a result, high resolution A/D conversion can be achieved if a long enough conversion time is allowed. In fact, the VFC approach has been shown to be superior (over dual-slope integration and successive approximation) in realizing A/D converters with relatively slow conversion speed [3]. Although their instantaneous output frequency may not be exactly proportional to the input voltage, the averaging nature of these VFCs makes them relatively immune to noise at only a slight cost in conversion speed. This type of VFC is best suited for digital metering and data-acquisition systems such as temperature and pressure sensing.

1.2 VFC Structures

VFCs can be implemented in a variety of ways; however, they can all be generalized to be composed of two distinctive parts: an integrator and a reset circuit. The reset circuit triggers the integrator to charge and discharge around a threshold level such that a charge balance is maintained across the integrating capacitor. A typical

implementation is shown in Fig.1.2(a) where a reset circuit is used to switch a current source onto the inverting terminal of an integrator [4]. The input voltage of this circuit, however, must be negative. A more useful version of the same circuit is shown in Fig.1.2(b), where the current source is in opposite direction of the one in Fig.1.2(a) [5,6]. In this case, the input can be positive with positive or dual supply. The same idea can be realized without using a current source by putting a switch across the integrating capacitor as shown in Fig.1.2(c) [7]. This circuit, however, is inherently non-linear due to the non-linear characteristic of the switch resistance.

All three circuits described so far use the inverting terminal of the amplifier as the input. This technique has the advantage of leaving the non-inverting terminal of the amplifier for offset trimming and avoiding the common-mode rejection problem of the amplifier. However, with the availability of chopper-stabilized operational amplifiers, the offset and CMRR problems are no longer significant. Hence integrators utilizing a non-inverting amplifier input can be used, as shown in Fig.1.2(d) [8,9]. In this way, the capacitor is charged and discharged through only one resistor and so the output frequency is independent of circuit component values. This alleviates the need for a high-precision resistor with low temperature drift which are critical for all other three cases.

The reset circuit also comes in a variety of forms. Different designs of the reset circuit lead to VFCs with different properties. Most early VFC designs use op-amp comparators to define threshold levels for the integrator output and to reset the integrator. One such design has already been shown in Fig.1.2(b). Commercial models such as the VFC651 [5] and VFC100 [6] both employ the comparator technique with only

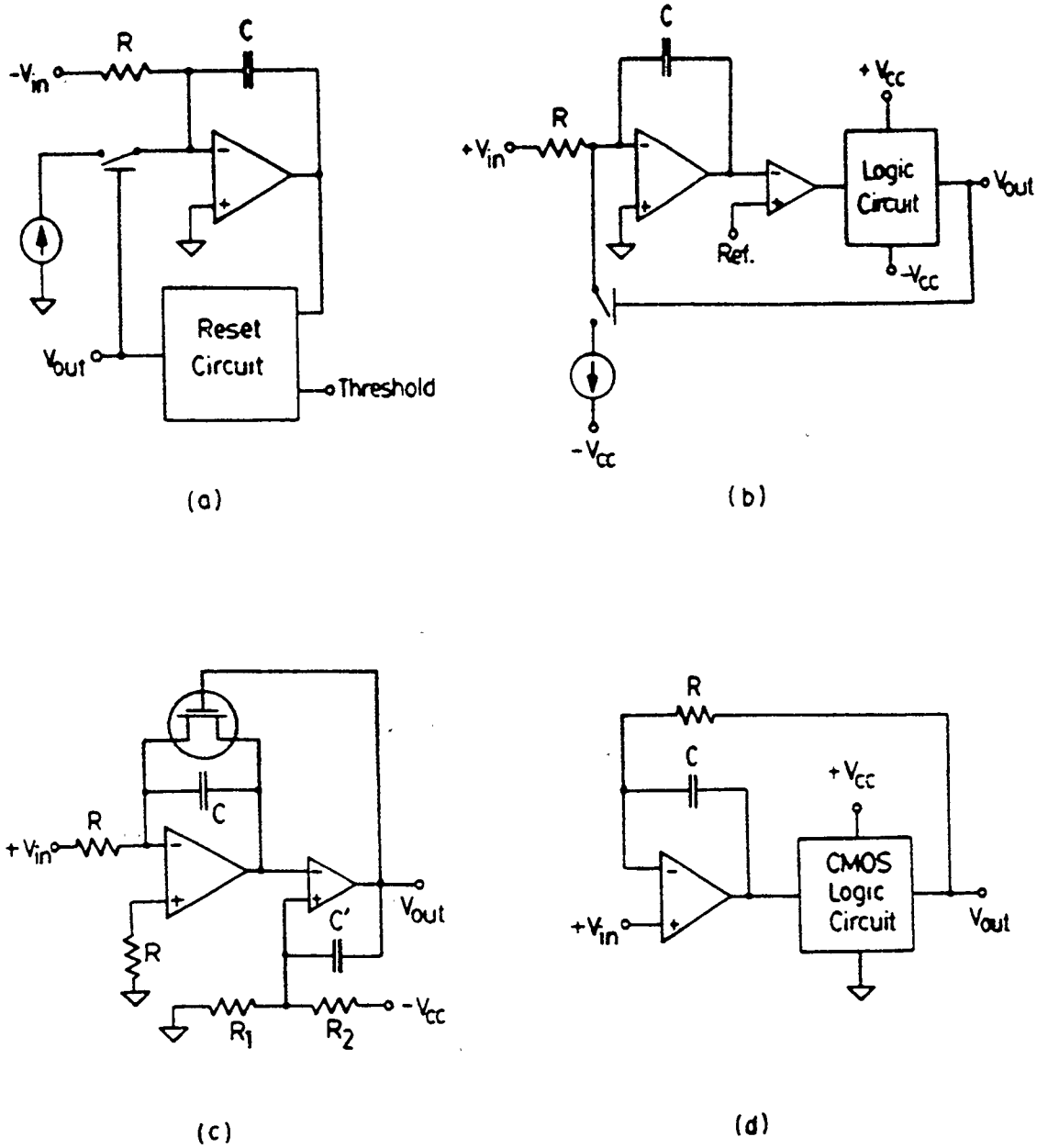


Fig.1.2 Various Forms of VFCs: VFC with
(a) Inverting-Input Integrator and Comparator Reset Circuit
(b) Same Features as (a) but Positive Input Range
(c) Switch-Controlled Integrator
(d) Non-Inverting-Input Integrator and CMOS Digital Reset Circuit

slight variations. This method has the advantage of using the analog ground as the comparator reference and hence is relatively noise-insensitive. However, the comparator output is slew-rate limited and digital gates are often required to control and implement the switch. If CMOS logic is used to implement the reset circuit, the comparator is really a redundant element since CMOS gates have high enough noise immunities to reject the normal amount of power-supply induced noise.

Consequently, it is apparent that a useful VFC may simply consist of a non-inverting integrator realized using a chopper-stabilized amplifier and a reset circuit constructed with CMOS logic as shown in Fig.1.2(d). This VFC structure is used throughout this thesis.

1.3 Design Objectives

High-precision integrated VFCs have been available for a long time [4,7,10] and recent monolithic VFCs such as the AD651 have achieved linearity error as low as 0.005% of full scale at frequencies as high as 100kHz. However, the possibilities of realizing a VFC with still higher performance have yet to be exhausted, especially with recent development in design techniques [9,11] and advancement in IC technologies.

In the quest for a VFC with high performance and simple structure, this thesis examines a few new VFC designs that are competitive with other existing designs in terms of

(1) simplicity,

(2) high resolution,

(3) high accuracy,

(4) high linearity,

(5) wide input range,

(6) wide operating-frequency range,

(7) low cost,

(8) low temperature drift,

(9) low power dissipation,

(10) capability of elementary signal handling, and

(11) provision for single or dual power-supply operations.

These design objectives serve as a guide-line in developing the new VFC circuits.

1.4 Scope of the Thesis

This thesis is organized from a designer's perspective; that is, the basic circuit principles are introduced first, more complex circuits and ideas are then discussed, and this is followed by practical considerations for implementing the circuits. Following the introduction of Chapter 1, Chapter 2 describes a basic free-running VFC circuit and its modifications, thus introducing the charge-balance principle and the one-shot resetting technique on which the more elaborate VFCs that follow are based. Also described are the techniques of providing gain and linearization and arranging for dual-supply operations for the VFCs. Chapter 3 follows the logical step of describing

a modified VFC - a clock-synchronous version - for high-resolution A/D conversion. Chapter 4 then goes on to describe the most versatile member of the VFC family - the clock-controlled VFC, which can provide almost all the functions of the other circuits plus other useful features. Chapter 5 then steps back to discuss the design considerations of all the VFCs and present some experimental measurements on the high-precision VFCs implemented with commercial components. As an important step in customizing these VFCs, Chapter 6 describes the aspects that must be considered in integrating these circuits. Finally, Chapter 7 provides a summary and conclusions.

CHAPTER 2

RC-CONTROLLED VFC

2.1 Introduction

All the VFCs to be described in this thesis employ the well known *charge balance* principle [3,4]. In this chapter, the charge balance principle will be illustrated by a basic VFC circuit [8]. This basic VFC consists of an integrator and a one-shot circuit whose pulse width is determined by a resistor-capacitor time constant. Modifications of this basic VFC to provide gain, linearization, and dual supply operation will be described. A scheme to improve the linearity of this basic VFC will also be presented.

2.2 The Basic VFC

A simple free-running VFC with an RC controlled pulse width can be constructed as shown in Fig.2.1 [8]. For single-supply operations, all components of this circuit are powered from a single reference voltage V_{ref}. If R_4 is large, the high level of V_{out} is equal to V_{ref} and the low level of V_{out} is equal to zero.

This circuit operates as shown in Fig.2.2. When V_{out} is high, the output of the operational amplifier, V_1, is ramping down towards ground. If V_4 at this moment is high, V_2 will be low and V_3 will be charging towards V_{ref}. When V_3 reaches the

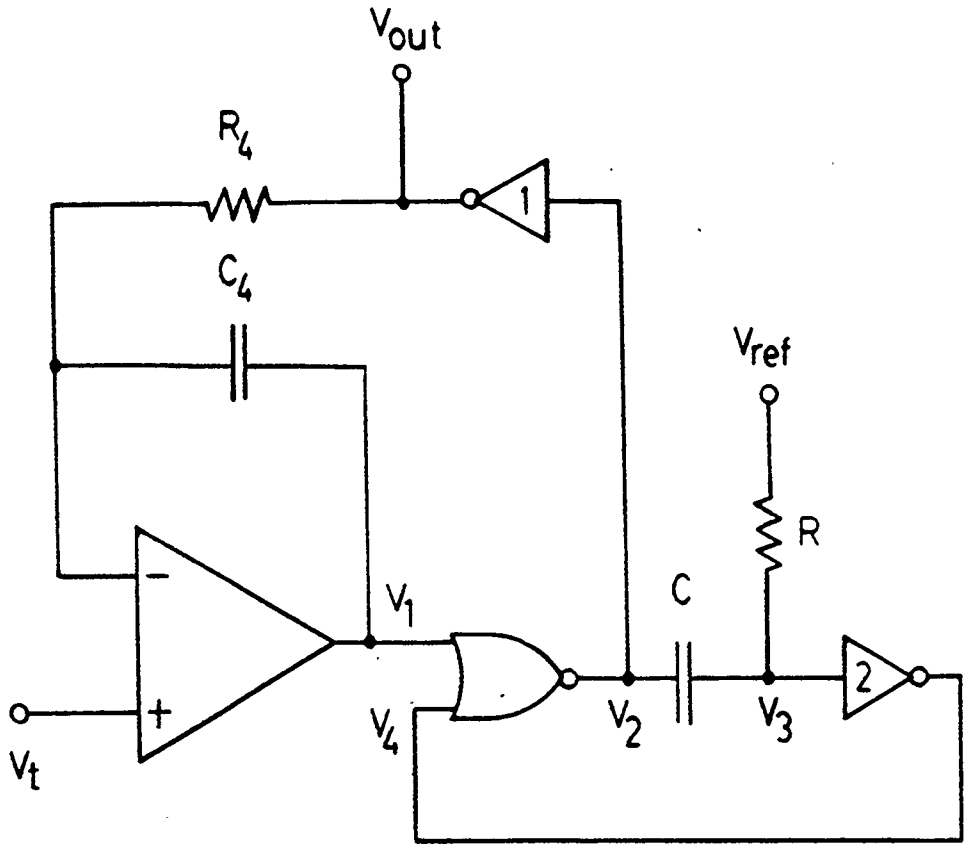


Fig.2.1 VFC with RC-Controlled Pulse Width

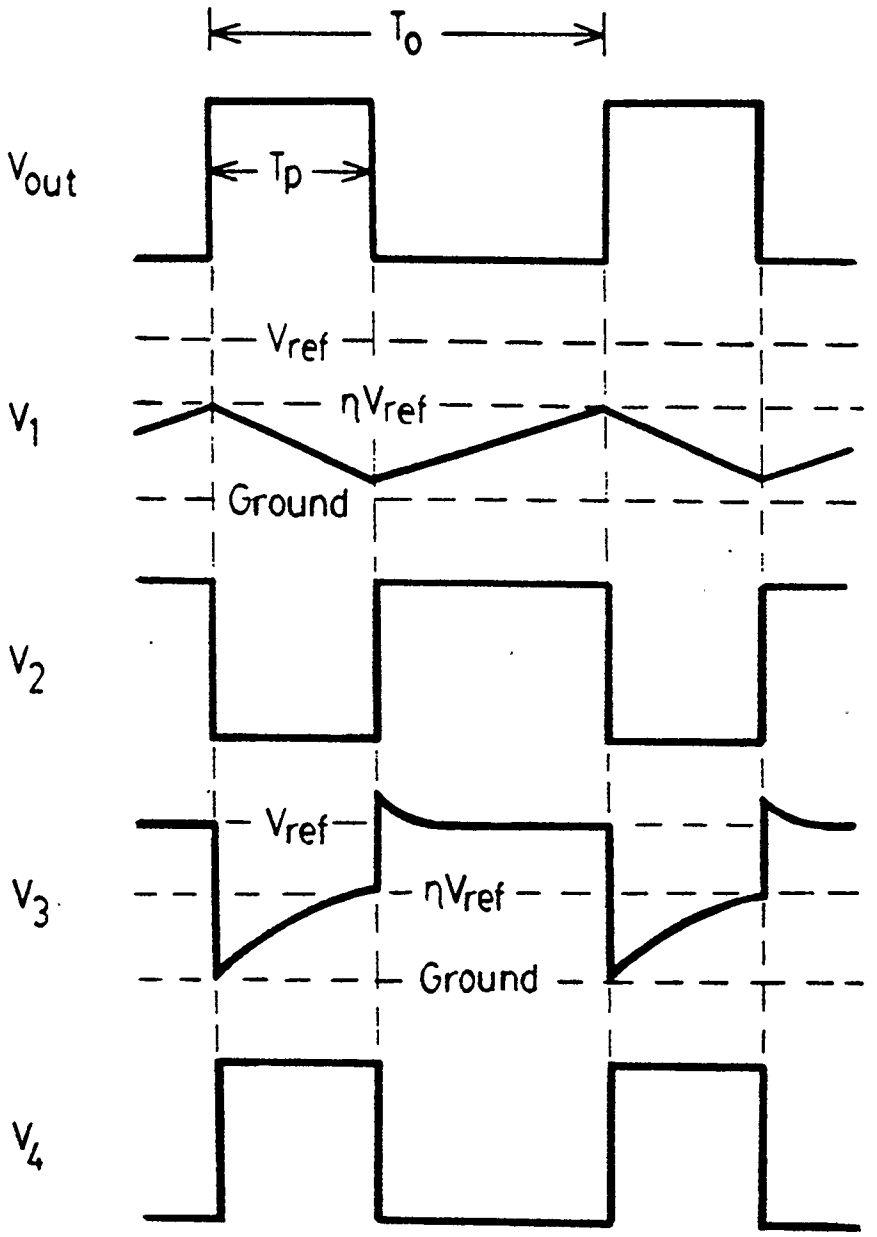


Fig.2.2 Voltage Waveforms for the RC-Controlled VFC

threshold of *inverter* 2, V_4 will go low and will turn V_2 high. Therefore, V_{out} will turn low, which will cause V_1 to ramp up. At this switching point, V_3 will jump to a level of one diode drop above V_{ref} if *inverter* 2 is a CMOS inverter with input protection diodes. As V_3 is discharging quickly towards V_{ref}, V_1 is ramping up. When V_1 reaches the threshold of the NOR-gate, it will turn V_2 low and V_{out} high; V_3 will then be pulled to ground and will start charging towards V_{ref}. Hence the cycle repeats.

The pulse width of V_{out}, T_p, is controlled by the one-shot circuit formed by R and C in accordance with

$$T_p = RC \ln\frac{1}{1-\eta} \tag{2.1}$$

where ηV_{ref} is the threshold voltage of the inverters.

The output period T_o, on the other hand, is governed by the input V_t. A charge balance equation for capacitor C_4 is given by

$$-\frac{V_t}{R_4}T_o + \frac{V_{ref}}{R_4}T_p = 0 \tag{2.2}$$

so that

$$f_o = \frac{1}{T_o} = \frac{V_t}{V_{ref}T_p}. \tag{2.3}$$

Hence the output frequency, f_o, is directly proportional to the input voltage V_t. Furthermore, Eq.(2.3) can be re-arranged to

$$\frac{T_p}{T_o} = \frac{V_t}{V_{ref}}, \tag{2.4}$$

which states that the output pulse width-to-period ratio is equal to the input-to-

reference voltage ratio, independent of circuit component values.

2.3 VFC with Gain and Linearization

Voltage gain can be provided easily if a resistor R_1 is connected to the inverting input of the operational amplifier of the basic VFC, as shown in Fig.2.3. The charge balance for capacitor C_4 is then given by

$$-\frac{V_t}{R_1}T_o - \frac{V_t}{R_4}T_o + \frac{V_{ref}}{R_4}T_p = 0 \tag{2.5}$$

so that

$$f_o = \frac{1}{T_o} = \frac{V_t}{V_{ref}T_p}(1 + \frac{R_4}{R_1}). \tag{2.6}$$

Gain can thus be provided at the expense of making f_o dependent on the resistance ratio $\frac{R_4}{R_1}$.

In applications where the input voltage to the VFC is a temperature transducer output, V_t is often a nonlinear function of the temperature t. For example, the temperature characteristics for an ice-point referenced copper-constantan thermocouple is given by

$$\frac{V_t}{V_{ref}} = \frac{at}{1 + bt} \tag{2.7}$$

where a and b are constants. In such cases, the VFC can be modified to give a direct indication of V_t as shown in Fig.2.4, where the output V_{out} is used to switch a resistor R_2 between the inverting input of the operational amplifier and ground.

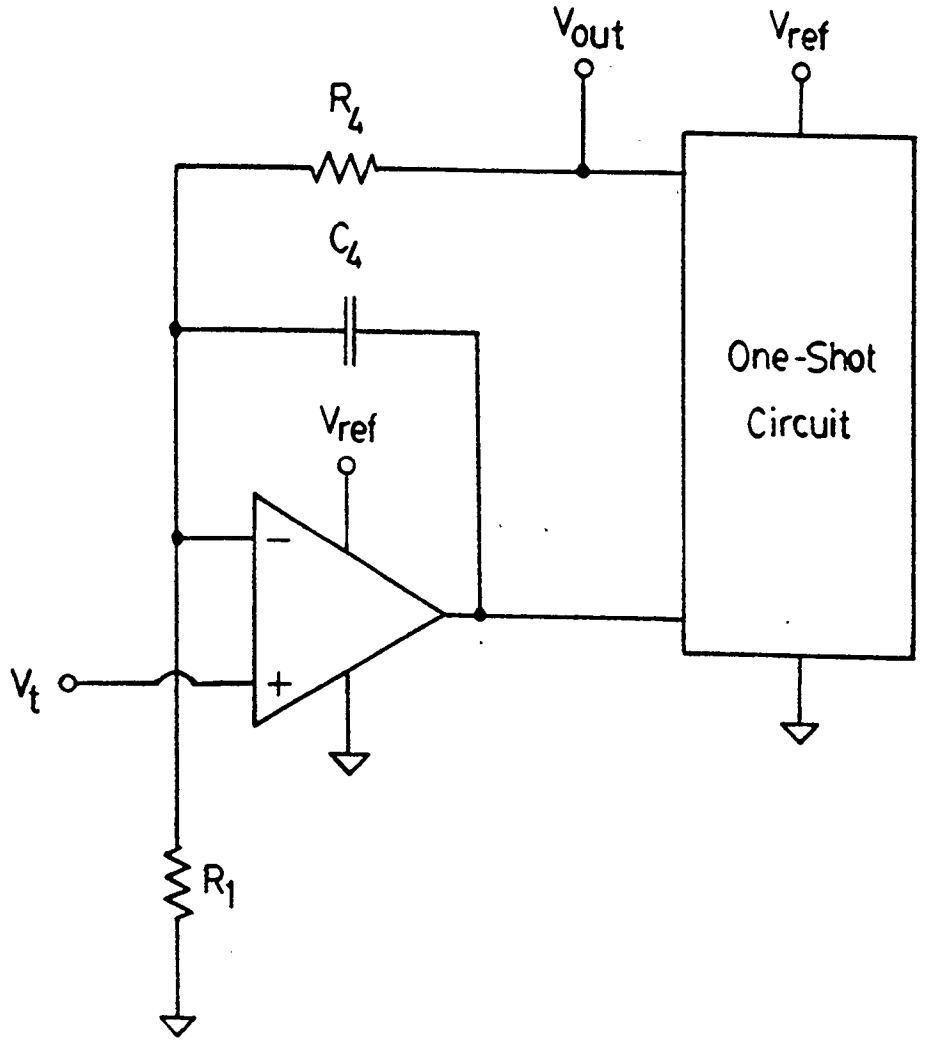


Fig.2.3 VFC with Gain

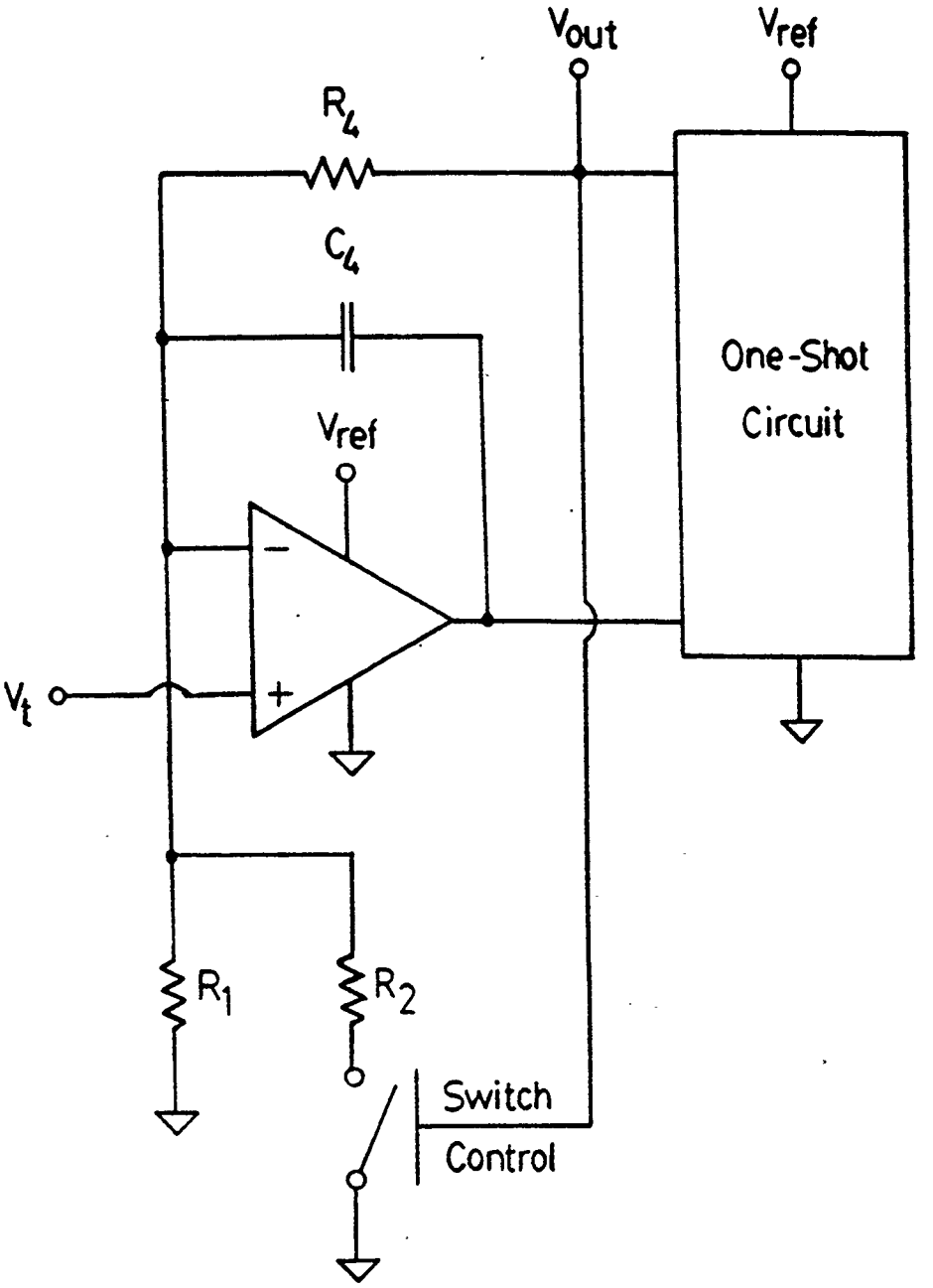


Fig.2.4 VFC with Gain and Linearization

If the switch is in place when V_{out} is high, the charge balance for C_4 must be modified to

$$-\frac{V_t}{R_1}T_o - \frac{V_t}{R_4}T_o + \frac{V_{ref}}{R_4}T_p - \frac{V_t}{R_2}T_p = 0 \tag{2.8}$$

so that

$$f_o = \frac{1}{T_o} = \frac{V_t}{V_{ref}T_p}\frac{(1+\frac{R_4}{R_1})}{(1-\frac{R_4}{R_2}\frac{V_t}{V_{ref}})}. \tag{2.9}$$

On the other hand, if the switch is in place when V_{out} is low, the charge balance for C_4 is given by

$$-\frac{V_t}{R_1}T_o - \frac{V_t}{R_2}T_o - \frac{V_t}{R_4}T_o + \frac{V_{ref}}{R_4}T_p + \frac{V_t}{R_2}T_p = 0 \tag{2.10}$$

so that

$$f_o = \frac{1}{T_o} = \frac{V_t}{V_{ref}T_p}\frac{(1+\frac{R_4}{R_1}+\frac{R_4}{R_2})}{(1+\frac{R_4}{R_2}\frac{V_t}{V_{ref}})}. \tag{2.11}$$

Consequently, if, for example, a and b are both positive and the switch is in place when V_{out} is high, Eq.(2.9) will become

$$f_o = \frac{1}{T_o} = \frac{at}{T_p}(1+\frac{R_4}{R_1}) \tag{2.12}$$

with $\frac{R_4}{R_2} = \frac{b}{a}$. Similarly, if a is positive while b is negative and the switch is in place when V_{out} is low, Eq.(2.11) will become

$$f_o = \frac{1}{T_o} = \frac{at}{T_p}(1 + \frac{R_4}{R_1} + \frac{R_4}{R_2}) \tag{2.13}$$

with $\frac{R_4}{R_2} = \frac{b}{a}$. In either case, linearization is achieved, and the choice of closing the switch during whether V_{out} is high or low depends on the form of V_t to be linearized.

2.4 Dual-Power-Supply Operation

The VFC can be modified for bipolar operation if the circuit is powered from $\pm V_{ref}$ as shown in Fig.2.5. The input V_t can now be either positive or negative. Also, a high gate output level is now V_{ref} while a low gate output level is $-V_{ref}$. The charge balance equation must then be modified to

$$-\frac{V_t}{R_4}T_o - \frac{V_{ref}}{R_4}T_o + \frac{2V_{ref}}{R_4}T_p = 0 \tag{2.14}$$

so that

$$f_o = \frac{1}{T_o} = \frac{(1 + \frac{V_t}{V_{ref}})}{2T_p}. \tag{2.15}$$

Here, a zero input voltage will produce a square wave output.

The gain and linearization features can be provided in bipolar operation in a straight-forward way. With a resistor R_1 connected from ground to the inverting terminal of the operational amplifier in Fig.2.5, the charge balance equation for C_4 will be given by

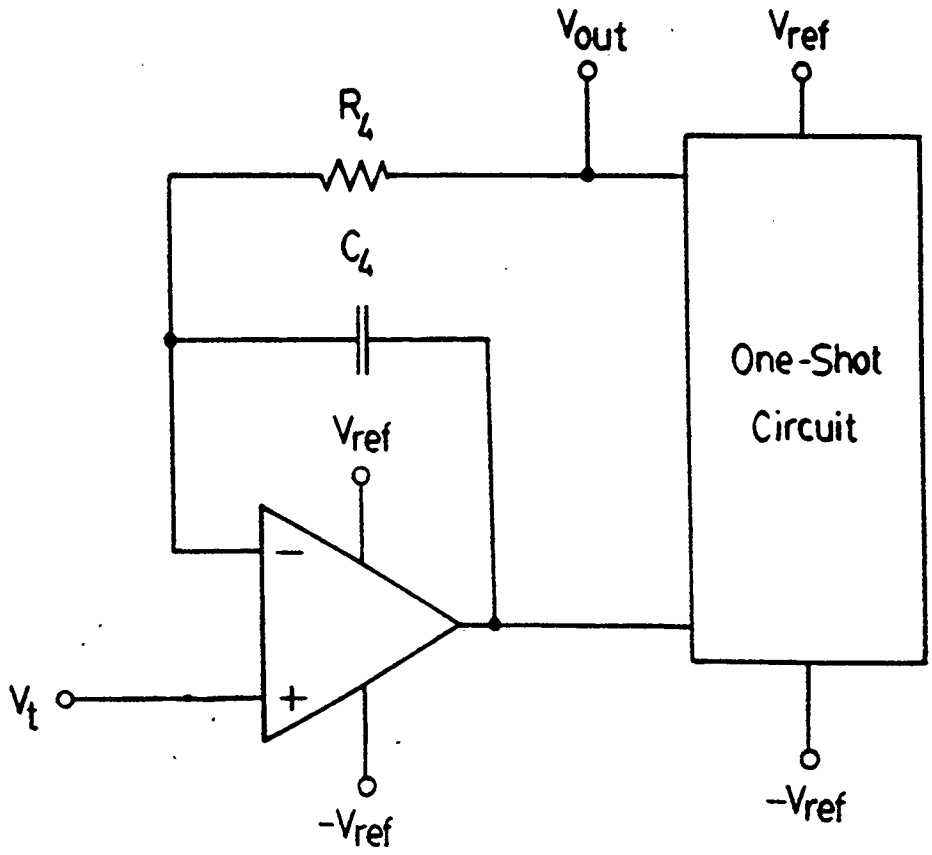


Fig.2.5 VFC with Dual-Supply Operation

$$-\frac{V_t}{R_4}T_o - \frac{V_t}{R_1}T_o - \frac{V_{ref}}{R_4}T_o + \frac{2V_{ref}}{R_4}T_p = 0 \tag{2.16}$$

so that

$$f_o = \frac{1}{T_o} = \frac{1 + \frac{V_t}{V_{ref}}(1 + \frac{R_4}{R_1})}{2T_p}. \tag{2.17}$$

In addition to R_1, if a resistor R_2 is connected to the inverting terminal of the operational amplifier from ground while V_{out} is high, the charge balance equation for C_4 is given by

$$-\frac{V_t}{R_4}T_o - \frac{V_t}{R_1}T_o - \frac{V_{ref}}{R_4}T_o + \frac{V_t}{R_2}T_p + \frac{2V_{ref}}{R_4}T_p = 0 \tag{2.18}$$

so that

$$f_o = \frac{1}{T_o} = \frac{1 + \frac{V_t}{V_{ref}}(1 + \frac{R_4}{R_1})}{2T_p(1 - \frac{R_4}{2R_2}\frac{V_t}{V_{ref}})}. \tag{2.19}$$

Similarly, if R_2 is connected when V_{out} is low, the charge balance equation is given by

$$-\frac{V_t}{R_4}T_o - \frac{V_t}{R_1}T_o - \frac{V_{ref}}{R_4}T_o + \frac{V_t}{R_2}(T_o - T_p) + \frac{2V_{ref}}{R_4}T_p = 0 \tag{2.20}$$

so that

$$f_o = \frac{1}{T_o} = \frac{1 + \frac{V_t}{V_{ref}}(1 + \frac{R_4}{R_1} + \frac{R_4}{R_2})}{2T_p(1 + \frac{R_4}{2R_2}\frac{V_t}{V_{ref}})}. \tag{2.21}$$

With dual power supplies, $\frac{V_t}{V_{ref}}$ of the form $\frac{\pm at}{1 \pm bt}$ can be linearized by switching R_2 properly. For example, if both a and b are positive, f_o can be arranged into a linear function of t by connecting R_2 while V_{out} is high. In this case, substituting $\frac{V_t}{V_{ref}} = \frac{at}{1+bt}$ into Eq.(2.19) and choosing $\frac{R_4}{R_2} = \frac{2b}{a}$ will lead to

$$f_o = \frac{1}{T_o} = \frac{1 + at(1 + \frac{R_4}{R_1} + \frac{R_4}{2R_2})}{2T_p}, \tag{2.22}$$

in which f_o is a linear function of t.

2.5 VFC with Improved Frequency Linearity

The basic VFC discussed in Section 2.2 produces an output frequency directly proportional to the input voltage *only* if the one-shot pulse width, T_p, is independent of the input voltage. However, as shown in Fig.2.2, the input at *inverter* 2 (V_3) actually goes up to one diode drop above V_{ref} at the end of T_p, and if the next pulse is required before V_3 can discharge back to V_{ref}, the next pulse will be shortened. Therefore, as V_t increases, the output pulses will become narrower. This gives rise to about one percent of non-linearity in the output frequency over the input range.

This frequency non-linearity will not affect the output pulse-width-to-period ratio but is undesirable in applications where direct frequency counting is required. The pulse width variation, however, can be reduced significantly by modifying the basic VFC with an additional one-shot circuit, as shown in Fig.2.6. This additional one-shot

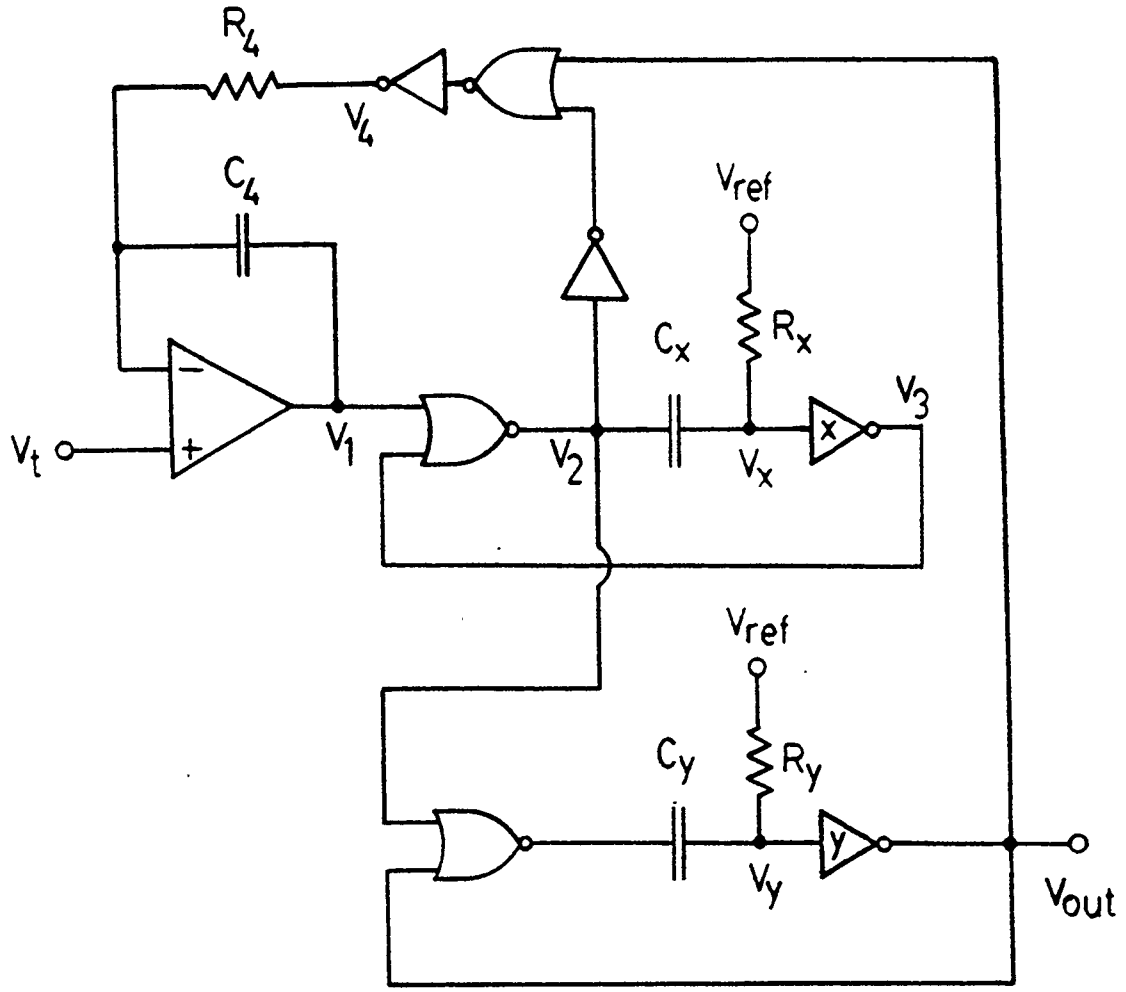


Fig.2.6 VFC with Improved Frequency Linearity

circuit is triggered when the original one-shot is off and has a time constant of about three times larger than the original one-shot, as shown in Fig.2.7. The two one-shot circuits produce a combined pulse of duration T_p to drive the integrator. That is,

$$T_p = T_{px} + T_{py} \tag{2.23}$$

with

$$T_{px} = R_x C_x \ln\frac{1}{1-\eta} \tag{2.24}$$

and

$$T_{py} = R_y C_y \ln\frac{1}{1-\eta} \tag{2.25}$$

where ηV_{ref} is the threshold level of the inverters.

Here, the input of *inverter* x (V_x) is allowed to discharge to V_{ref} with at least a time of T_{py} before it drops to ground. Therefore, it always starts charging from ground irrespective of the input voltage and so T_{px} is constant. On the other hand, since the input of *inverter* y (V_y) is always allowed a time of T_{px} to discharge to V_{ref} before it drops towards ground, it always starts charging up from the same level although this level may not be ground. Therefore, T_{py} is also independent of V_t. Consequently, T_p is independent of V_t and so the output frequency is directly proportional to the input voltage.

A typical non-linearity curve for the improved VFC is shown in Fig.2.8 for a maximum output frequency of 1 kHz. The ICL7650 chopper-stablized amplifier is used so that the offset voltage and the CMRR of the amplifier do not give rise to significant problems. Also, an input range from ground to $\frac{2}{3}V_{ref}$ can be obtained

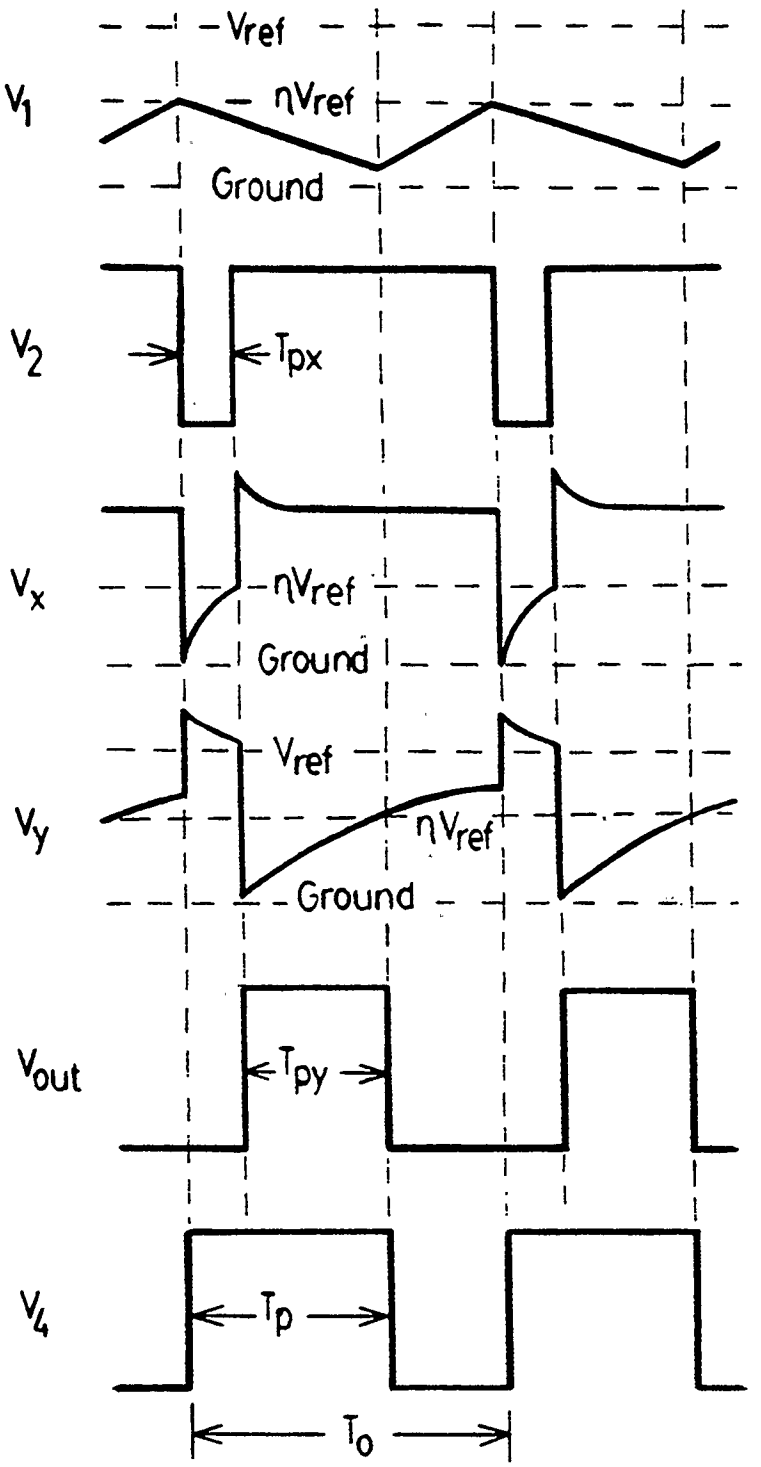


Fig.2.7 Voltage Waveforms for the Improved VFC

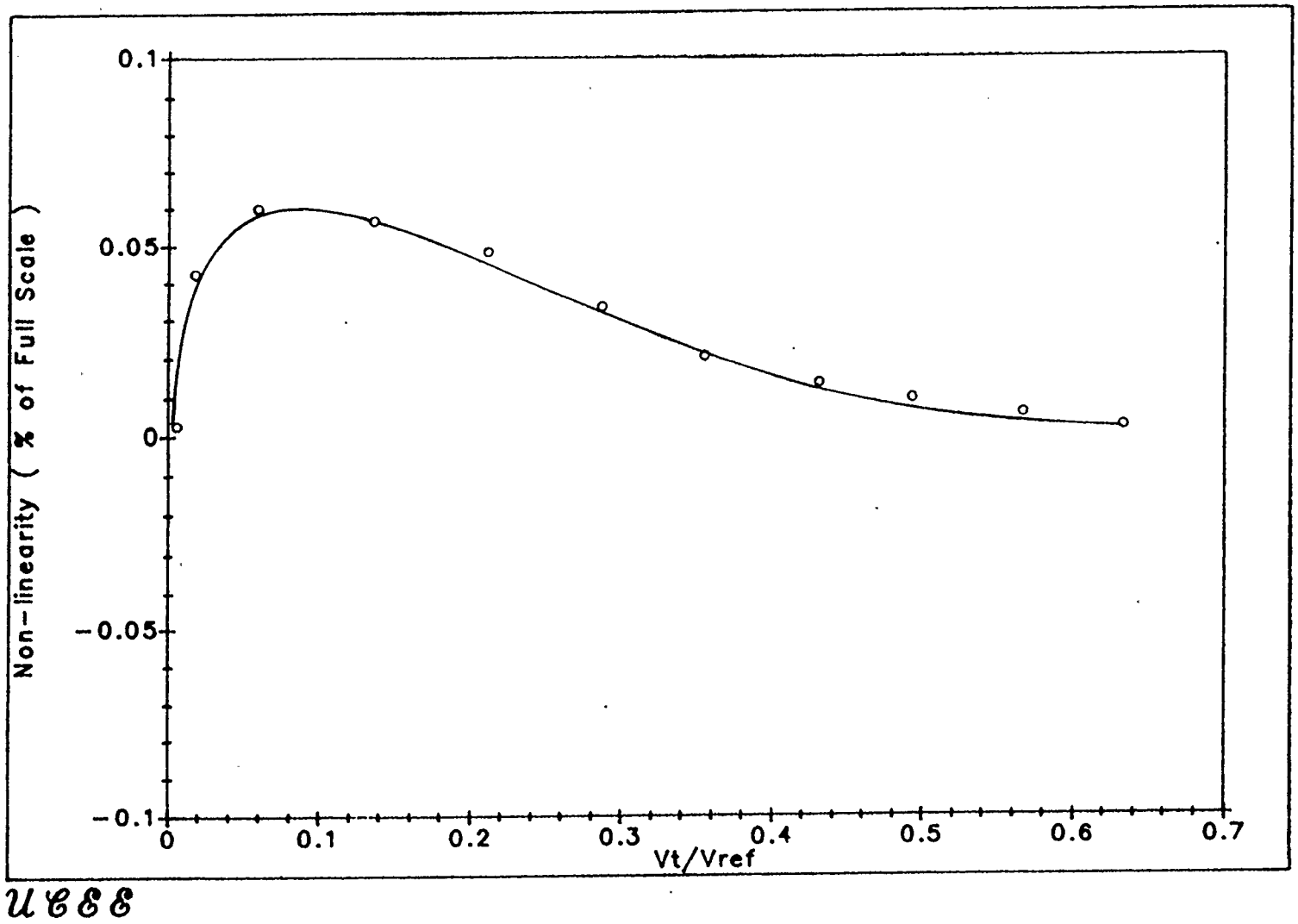


Fig.2.8 Typical Non-Linearity Curve for the Improved VFC
at Maximum Frequency of 1kHz

with this amplifier. Non-linearity is then determined by drawing a straight line between the origin and the frequency measurement at a reference voltage ($0.65V_{ref}$ in this case) and finding the deviations of the intermediate data points from this line. This method of determining linearity can be implemented easily with a micro-computer by calibrating the VFC against a reference voltage. The maximum deviations for various maximum operating frequencies are plotted in Fig.2.9 in comparison with those of the basic VFC. The improvement over the single one-shot circuit is shown to be over an order of magnitude at moderate frequencies.

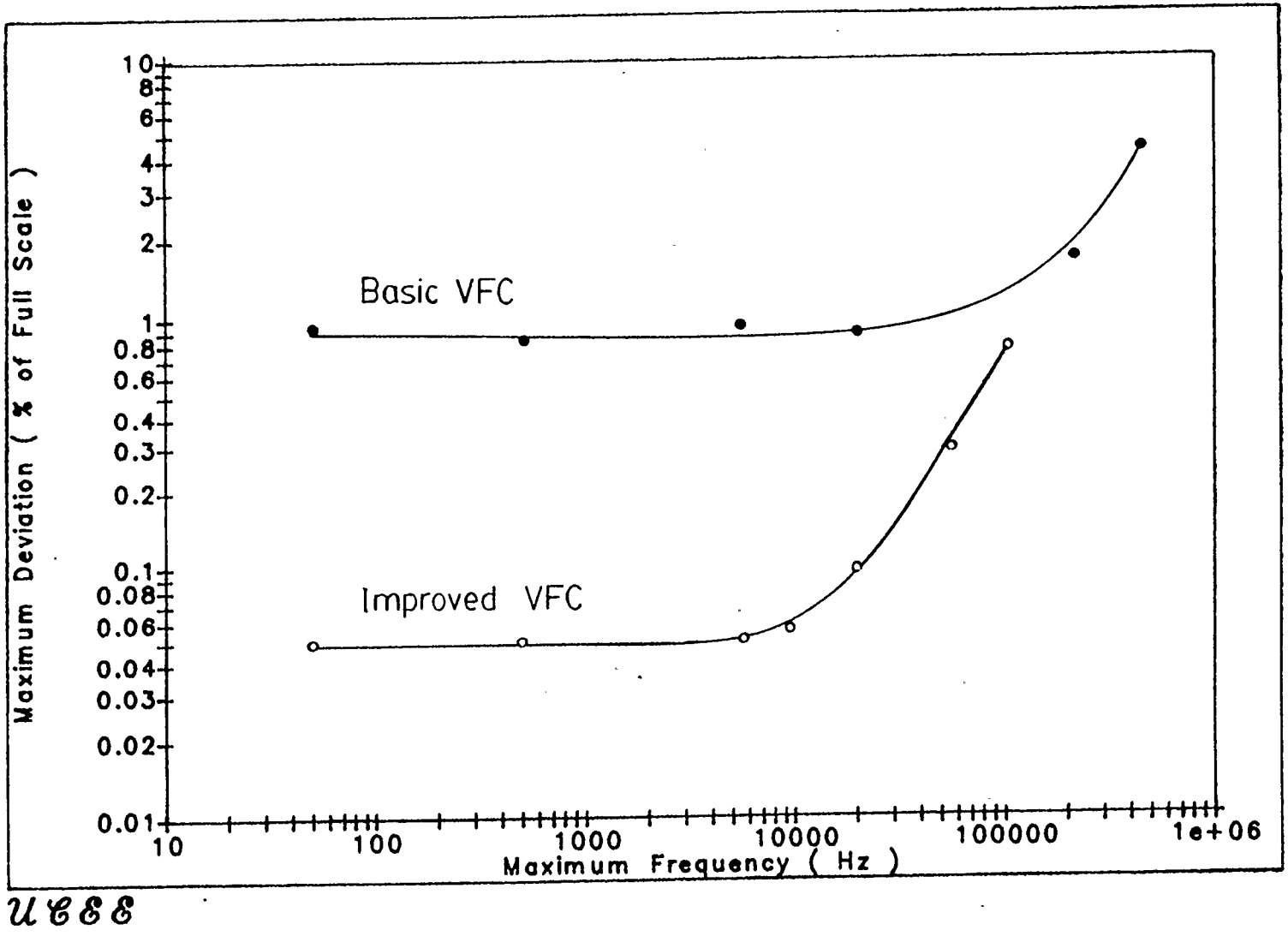


Fig.2.9 Comparison of Maximum Non-Linearity for the Basic and Improved VFCs

CHAPTER 3

SYNCHRONIZED VFC

3.1 Introduction

As mentioned in Chapter 1, VFCs with average output pulse-width-to-period ratio proportional to the input voltage are useful in high-precision analog-to-digital conversion. In order to accurately measure the pulse width and period, however, a high-frequency clock pulse must be employed to perform the digital counting as depicted in Fig.1.1(c). The one-shot pulse widths of the VFCs discussed so far in Chapter 2 are all determined by some resistor-capacitor combination and are not related to any high-frequency clock. Therefore, high-resolution measurement is possible only if the VFC pulse width is much larger than the measuring clock period. This limits the RC-controlled VFC to only low-speed A/D Conversion. High-resolution A/D conversion at high frequency is made possible by synchronizing the rising and falling edges of the VFC output pulses by a clock. The technique for implementing such a synchronized VFC will be described in this chapter. A simple analog-to-digital conversion system based on the synchronized VFC will also be described.

3.2 The Synchronized VFC

A clock-synchronized VFC with an RC-controlled one-shot circuit is shown in Fig.3.1 and its voltage waveforms are shown in Fig.3.2. This circuit operates in nearly

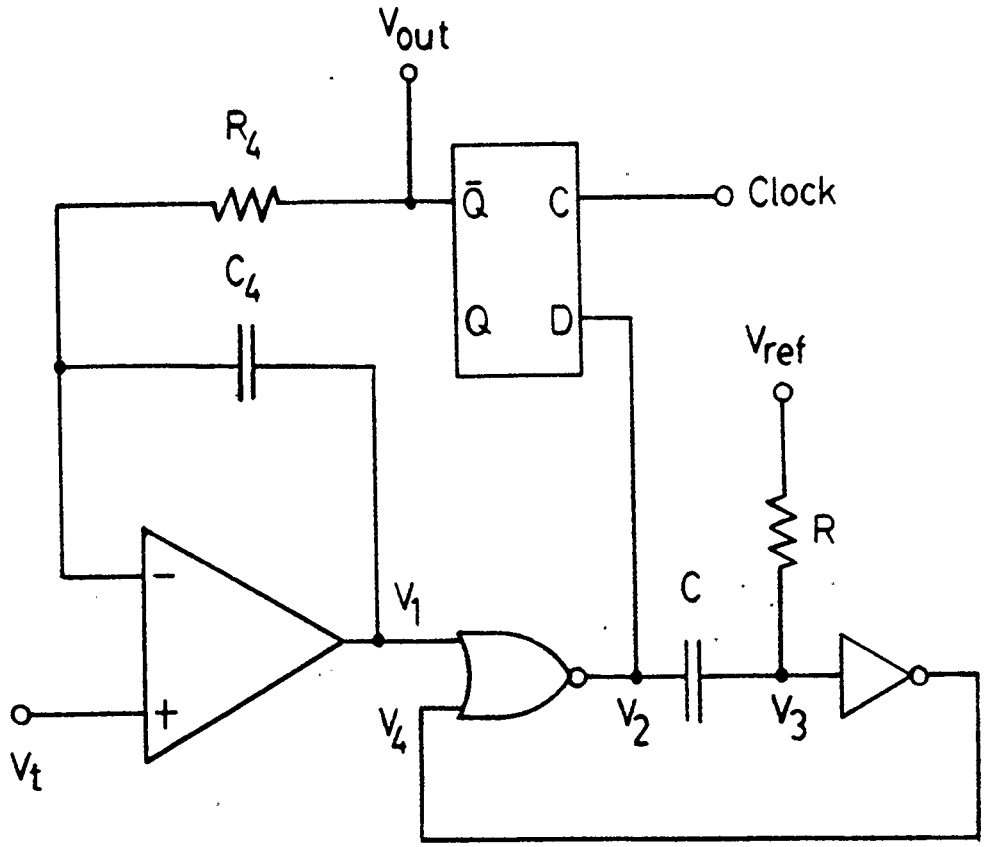


Fig.3.1 The Clock-Synchronized VFC

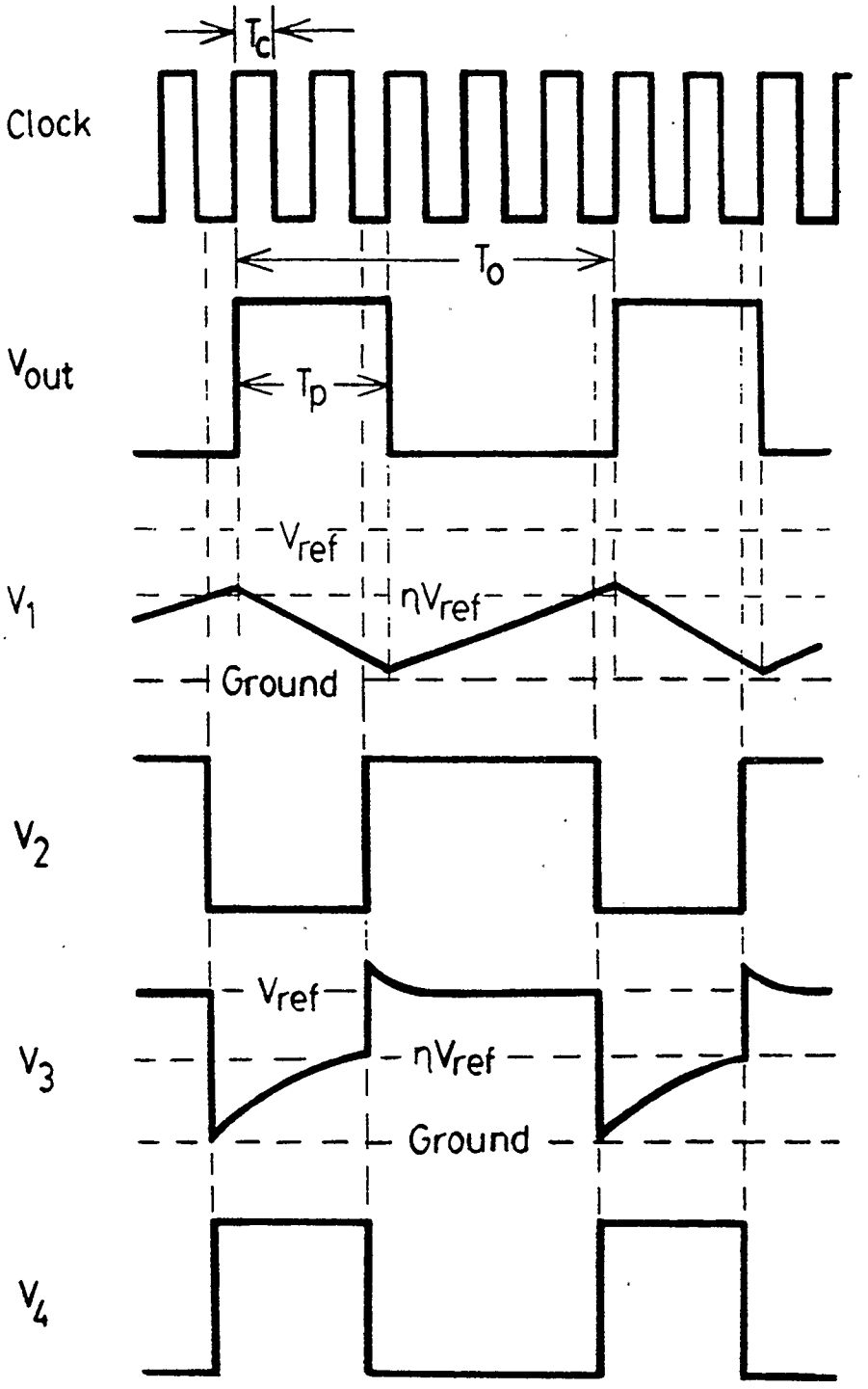


Fig.3.2 Voltage Waveforms for the Synchronized VFC

the same way as the unsynchronized VFC (of Fig.2.1); the only difference is that V_{out} now goes high or low only on rising clock edges. Although the op-amp output (V_1) may now ramp up to a level above the threshold of the NOR-gate before ramping down, the higher V_1 goes above the threshold, the less time it will take to reach the threshold on the next cycle. Therefore, over any conversion time longer than one output period T_o, the charge balance for capacitor C_4 is maintained to within one clock period T_c. That is, if there are N clock cycles within a certain conversion time and M clock cycles for which V_{out} is high within the same time, the charge balance equation for C_4 will be given by

$$-\frac{N\,T_c V_t}{R_4}+\frac{M\,T_c V_{ref}}{R_4}\approx 0 \qquad (3.1)$$

with a maximum error of $\frac{T_c V_t}{R_4}$. So, the input-to-reference voltage ratio, $\frac{V_t}{V_{ref}}$, is simply given by

$$\frac{V_t}{V_{ref}}\approx\frac{M}{N}. \qquad (3.2)$$

It should be noted that the second term of Eq.(3.1) is not subject to any error due to the fact that if the value of M varies among different conversion times, the value of N will also change to maintain the charge balance. Therefore, for every measurement, M is exact while N is subject to a maximum error of ± 1.

The average output frequency, $f_{o_{ave}}$, is given by

$$f_{o_{ave}}=\frac{M}{N\,T_{p_{ave}}}\approx\frac{V_t}{V_{ref}T_{p_{ave}}} \qquad (3.3)$$

where $T_{p_{ave}}$ is the average output pulse width. For a sufficiently long conversion time, a large number of output pulses will be measured, and so any high-frequency noise on the power-supply rail or the op-amp input will be averaged out in the $\frac{M}{N}$ measurement.

3.3 Synchronized VFC with Gain, Linearization, and Dual-Supply Operation

The features of gain, linearization, and dual-supply operation for the basic VFC in Chapter 2 can all be applied to the synchronized VFC in a straight-forward manner. The additional components are connected in the same way as in the basic VFC. The charge balance equations, however, must now be modified to approximate equations involving the total number of clock pulses (N) and the number of clock pulses when V_{out} is high (M) within a certain conversion time. For example, for the synchronized VFC with gain, the approximate charge balance equation for capacitor C_4 is given by

$$-\frac{N\,T_c V_t}{R_1} - \frac{N\,T_c V_t}{R_4} + \frac{M\,T_c V_{ref}}{R_4} \approx 0 \qquad (3.4)$$

so that

$$\frac{M}{N} \approx \frac{V_t}{V_{ref}}\left(1 + \frac{R_4}{R_1}\right). \qquad (3.5)$$

For the cases of gain with linearization and dual-supply operation, similar modifications apply to Eq.(2.8) to Eq.(2.22).

3.4 Analog to Digital Conversion

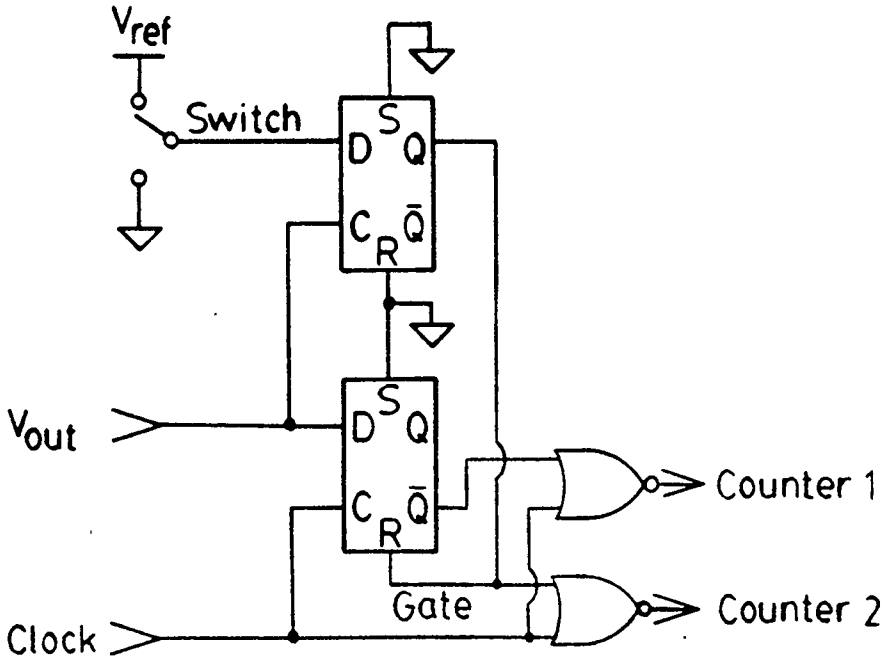
The synchronized VFC is particularly suitable for applications in high-resolution analog-to-digital conversion. Since the VFC output pulse width is an integral multiple of the synchronizing clock period, pulse-width measurements can be made precisely by using the same clock in the counting circuit. Furthermore, since the charge balance is maintained to within one clock period over a long conversion time, the resolution of the corresponding A/D conversion process will depend only on the product of the conversion time and the clock frequency, as will be shown shortly.

Analog-to-digital conversion can be achieved easily with the synchronized VFC by measuring its pulse width and period simultaneously. A simple measuring scheme is shown in Fig.3.3, in which a *convert–signal* (indicated as a *switch*) and two event counters are required. As the *Gate* is opened, *Counter* 1 counts the number of clock pulses when V_{out} is high (M) and *Counter* 2 counts the total number of clock pulses (N) within the conversion time. It should be noted that the conversion time $T_{convert}$ can be as long as $T_{o_{ave}} + T_{switch}$ and that T_{switch}, the length of the convert signal, must be greater than $T_{o_{ave}}$, where $T_{o_{ave}} = \frac{1}{f_{o_{ave}}}$.

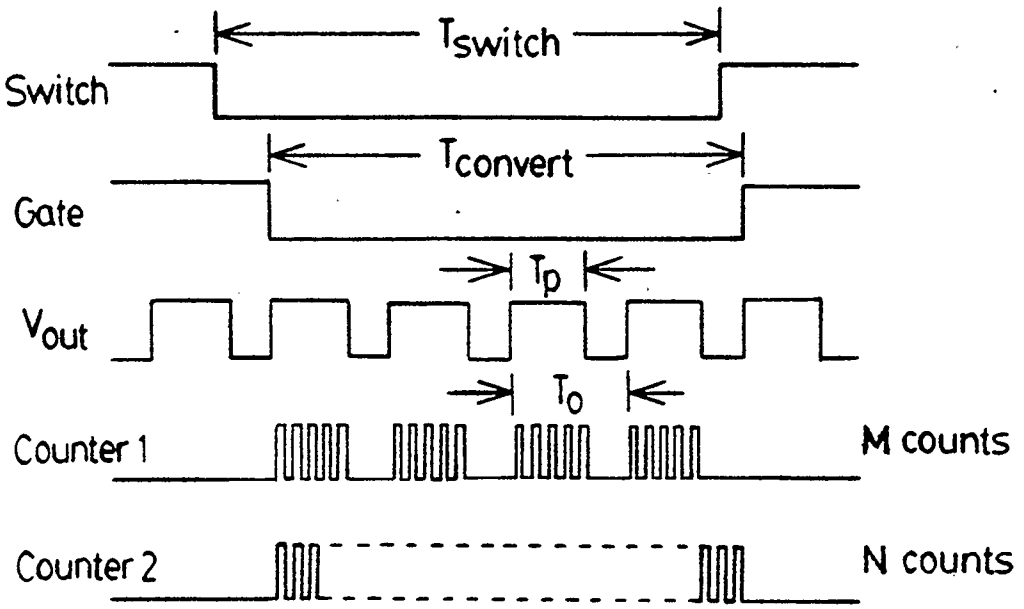
If M and N counts are registered by the two counters over a number of output pulses, the average VFC output pulse width-to-period ratio will be given by

$$\frac{T_{p_{ave}}}{T_{o_{ave}}} \approx \frac{M}{N}, \tag{3.6}$$

and so,



(a)



(b)

Fig.3.3 Pulse Width and Period Measurement Scheme: (a) Circuit Diagram and (b) Timing Diagram

$$\frac{V_t}{V_{ref}} \approx \frac{M}{N}, \tag{3.7}$$

a digital representation of the input voltage is obtained with a maximum error of ±1 count in N.

Since M is exact and $N = \frac{T_{convert}}{T_c}$, the resolution is governed only by the ratio $\frac{T_{convert}}{T_c}$, that is,

$$resolution\ in\ (\frac{V_t}{V_{ref}}) = \pm 1\ part\ in\ (T_{convert}\ f_c) \tag{3.8}$$

where $f_c = \frac{1}{T_c}$ is the clock frequency. For example, if the clock frequency is 4 MHz and the conversion time is 0.25 second, the resolution will be ±1 part per-million. In other words, 16-bit resolution with a 16-millisecond conversion time can be achieved with a 4MHz clock.

Practical implementations of the synchronized VFC and the counting system will be discussed in detail in Chapter 5.

CHAPTER 4

CLOCK-CONTROLLED VFC

4.1 Introduction

The VFCs described so far all use some form of one-shot circuit in which the pulse duration is controlled by a resistor-capacitor combination. The VFC pulse width thus produced is stable to only about 0.1 percent. Although the pulse edges may be synchronized by a high-frequency clock, as described in Chapter 3, the pulse width may vary with respect to the clock period and so pulse width measurement is necessary. As a result, at least two counting processes must be performed to obtain the average pulse width and the average period.

An alternate approach to implementing a high resolution VFC is to fix the pulse width with respect to the clock period. This can be done by controlling the VFC pulse width with a clock-driven counter and synchronizing the output period with the high-frequency clock. The pulse width is then an exact multiple of the clock period and the pulse width-to-period ratio can then be determined to within one clock period over a sufficiently long conversion time to give a prescribed resolution. This technique enables the use of a single counter in the A/D conversion process since pulse-width measurement is no longer necessary. One such clock-controlled VFC and its corresponding A/D conversion system will be described in this chapter. Some useful features and modifications of this VFC will also be discussed.

4.2 The Clock-Controlled VFC

The clock-controlled VFC is shown in Fig.4.1. and its operation is illustrated by the voltage waveforms shown in Fig.4.2. For single-ended operation, all of the circuit in Fig.4.1 is powered from V_{ref} so that a high gate level is equal to V_{ref} and a low gate level is equal to zero. Then, when V_{out} is at a low level, the output of the operational amplifier, V_1, is also low and is ramping up. When V_1 reaches the *set* threshold of *D flip flop* 2, V_2 will go low; and on the next rising clock edge, V_{out} will go high and V_1 will start to ramp down. Meanwhile, the Q output of *D flip flop* 1, V_3, will go low and this high-to-low transition will trigger the counter to count a preset multiple of falling clock edges. When the counter finishes counting, the output of the counter, V_4, will go high and reset *D flip flop* 2, which will cause V_2 to go high. Then, on the next rising clock edge, V_{out} will go low and V_1 will start to ramp up again. At the same time, the counter will be reset and hence the cycle will repeat.

The pulse width T_p here is a multiple of the clock period T_c so that

$$T_p = m\ T_c \tag{4.1}$$

where the options of $m = 1,2,4,...,2^{11}$ are available on an *MC* 14040 12-bit binary counter. For instance, $m = 4$ is used in Fig.4.1, Fig.4.2, and all subsequent examples in this chapter.

If, for a sufficiently long conversion time, there are N clock pulses with a corresponding number of n VFC output pulses, then an approximate charge balance equation for the capacitor C_4 can be written as

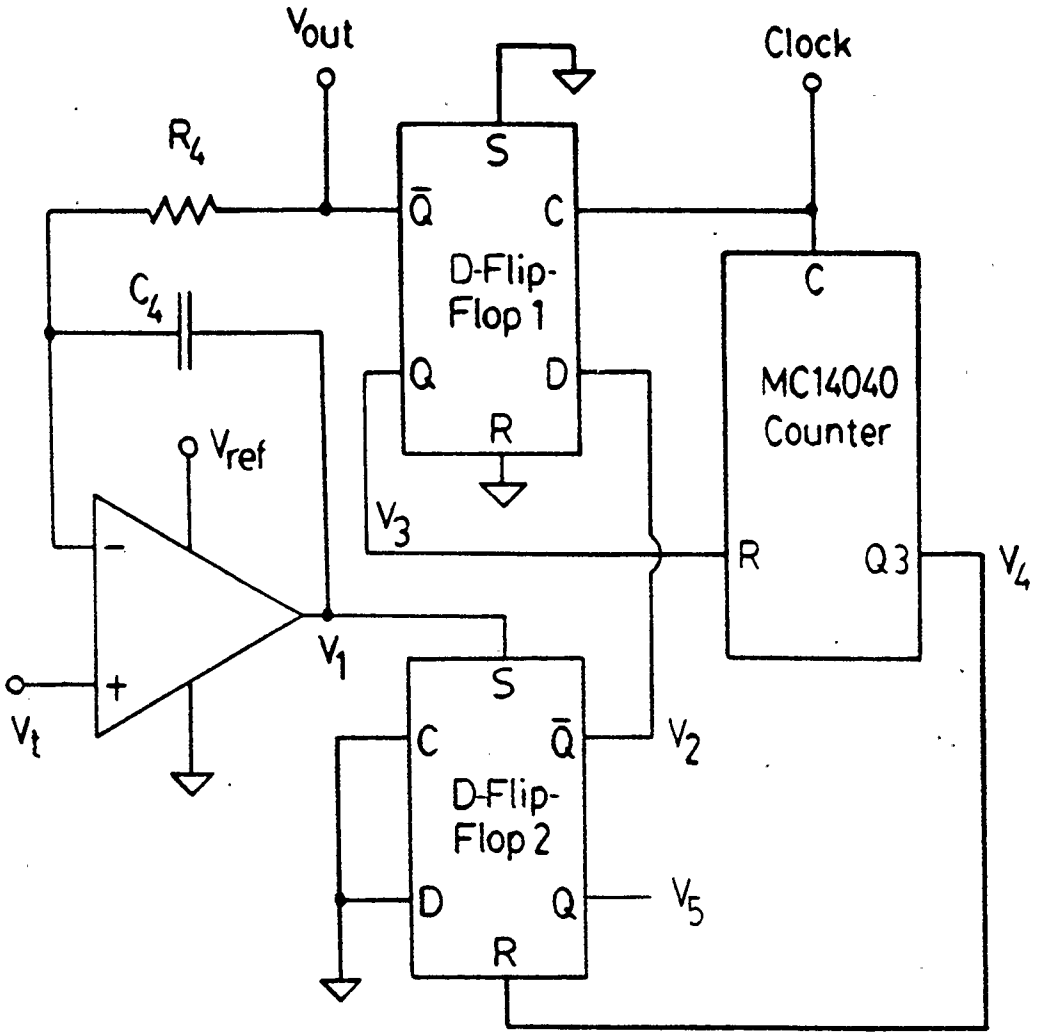


Fig.4.1 The Clock-Controlled VFC

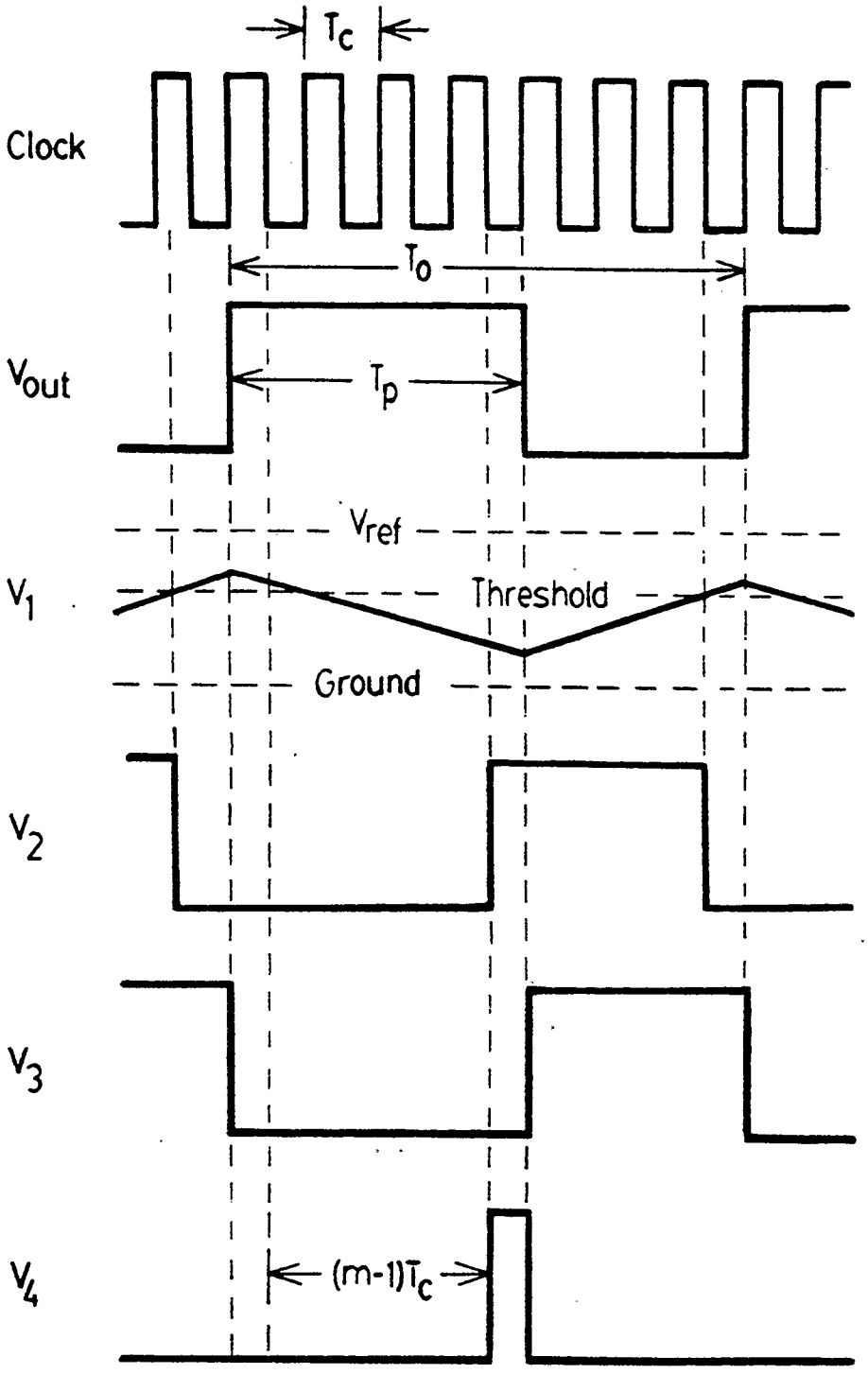


Fig.4.2 Voltage Waveforms for the Clock-Controlled VFC

$$-\frac{N\ T_c V_t}{R_4} + \frac{n\ T_p V_{ref}}{R_4} \approx 0 \tag{4.2}$$

where the maximum error for this charge balance is $\frac{T_c V_t}{R_4}$ due to the fact that the charge balance is maintained to within one clock period. Therefore,

$$f_{o_{ave}} = \frac{n}{N\ T_c} \approx \frac{V_t}{V_{ref} T_p}, \tag{4.3}$$

the average output frequency $f_{o_{ave}}$ is directly proportional to the ratio of V_t to V_{ref} with a maximum error given by

$$max.\ error\ in\ f_{o_{ave}} = \frac{V_t}{N\ T_p V_{ref}}. \tag{4.4}$$

Hence the maximum relative error in the average output frequency is equal to $\frac{1}{N}$.

4.3 Clock-Controlled VFC with Gain, Linearization, and Dual-Supply Operation

As in the cases for the synchronized VFC, the features of gain, linearization, and dual-power-supply operation for the basic VFC discussed in Chapter 2 can also be applied directly to the clock-controlled VFC. The charge balance equations, however, must now all be modified to approximate charge balance equations involving the average output frequency $f_{o_{ave}}$, the number of clock pulses N, and the number of output pulses n within a certain conversion time. For example, the charge balance equation for the clock-controlled VFC with gain is given by

$$-\frac{N\ T_c V_t}{R_1} - \frac{N\ T_c V_t}{R_4} + \frac{n\ T_p V_{ref}}{R_4} \approx 0 \tag{4.5}$$

so that

$$f_{o_{ave}} = \frac{n}{N\ T_c} \approx \frac{V_t}{V_{ref} T_p}(1 + \frac{R_4}{R_1}), \tag{4.6}$$

as compared to Eq.(2.5) and Eq.(2.6). Similar modifications apply to Eq.(2.8) to Eq.(2.22) for the cases of linearization and dual-supply operation.

4.4.Inverse Counting and A/D Conversion

The clock-controlled VFC can be used in the inverse-counting analog-to-digital conversion scheme. The inverse counting scheme requires two counters with one of them counting the number of clock pulses (N) within a certain conversion time ($T_{convert}$) and the other counting the number of VFC output pulses (n) within the same conversion time, as shown in Fig.4.3. As in the conversion scheme used by the synchronized VFC, the conversion time $T_{convert}$ here can be as long as $T_{o_{ave}} + T_{switch}$ and T_{switch}, the time when the switch is closed, must be greater than $T_{o_{ave}}$, where $T_{o_{ave}} = \frac{1}{f_{o_{ave}}}$.

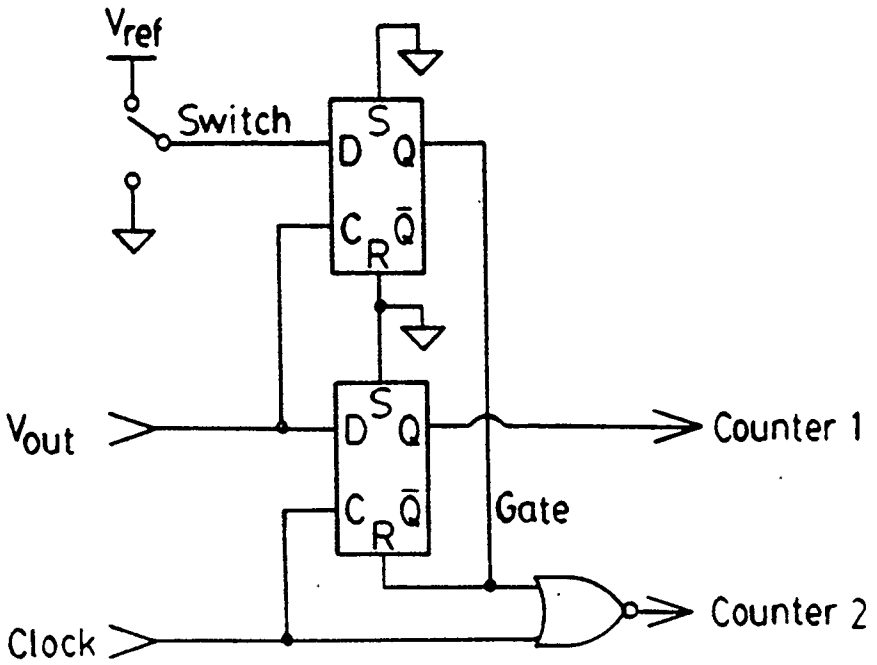
As shown in Fig.4.3(b), N and n are related to $T_{convert}$ by

$$T_{convert} = N\ T_c \approx n\ T_{o_{ave}} \tag{4.7}$$

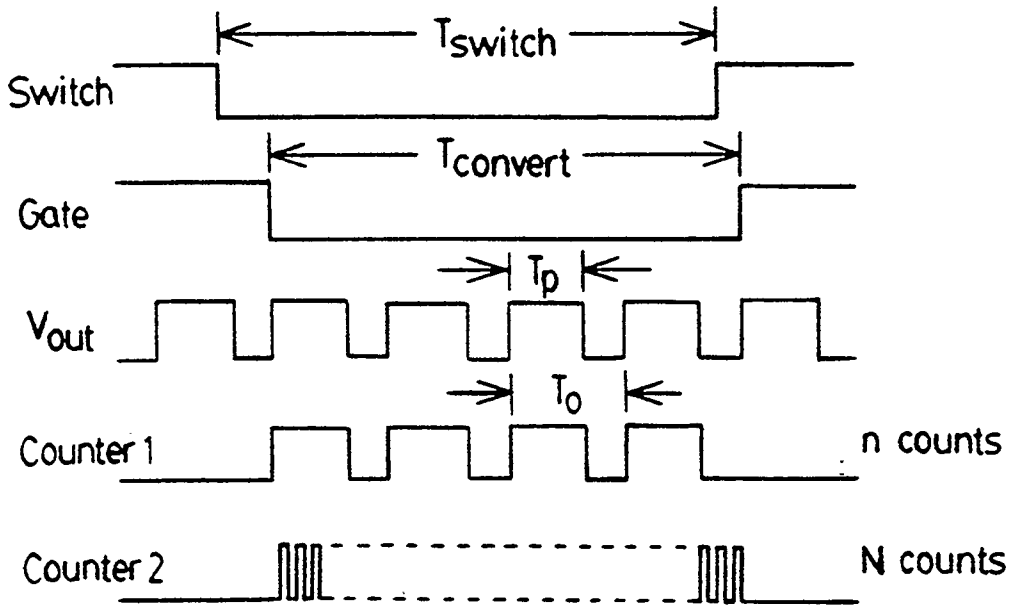
while from Eq.(4.1),

$$T_p = m\ T_c \tag{4.8}$$

So,



(a)



(b)

Fig.4.3 The Inverse Counting Scheme: (a) Circuit Diagram and (b) Timing Diagram

$$\frac{V_t}{V_{ref}} = \frac{T_p}{T_{o_{ave}}} \approx \frac{m\ n}{N}, \tag{4.9}$$

the input voltage is directly proportional to the ratio of n to N with a maximum error of ± 1 count in N for n large. Since $N = \frac{T_{convert}}{T_c}$, resolution of this counting scheme is governed by the length of the convert-command gate and the clock frequency. That is,

$$resolution\ in\ (\frac{V_t}{V_{ref}}) \approx \pm 1\ part\ in\ (T_{convert}\ f_c), \tag{4.10}$$

where $f_c = \frac{1}{T_c}$ is the clock frequency.

4.5 Single-Counter Inverse Counting Scheme

The possibility of using a single counter in the conversion process is a major advantage of this clock-controlled VFC over the synchronized VFC of the last chapter. The inverse counting method can be carried out by using a single counter as shown in Fig.4.4. In this scheme, the number of output pulses, n, to be considered is preset with a binary ripple counter in the circuit while the number of clock pulses, N, is to be counted by an external event counter. Then the ratio $\frac{V_t}{V_{ref}}$ is still given by

$$\frac{V_t}{V_{ref}} \approx \frac{m\ n}{N} \tag{4.11}$$

and the resolution is still ± 1 part in N. However, the conversion time will be given by

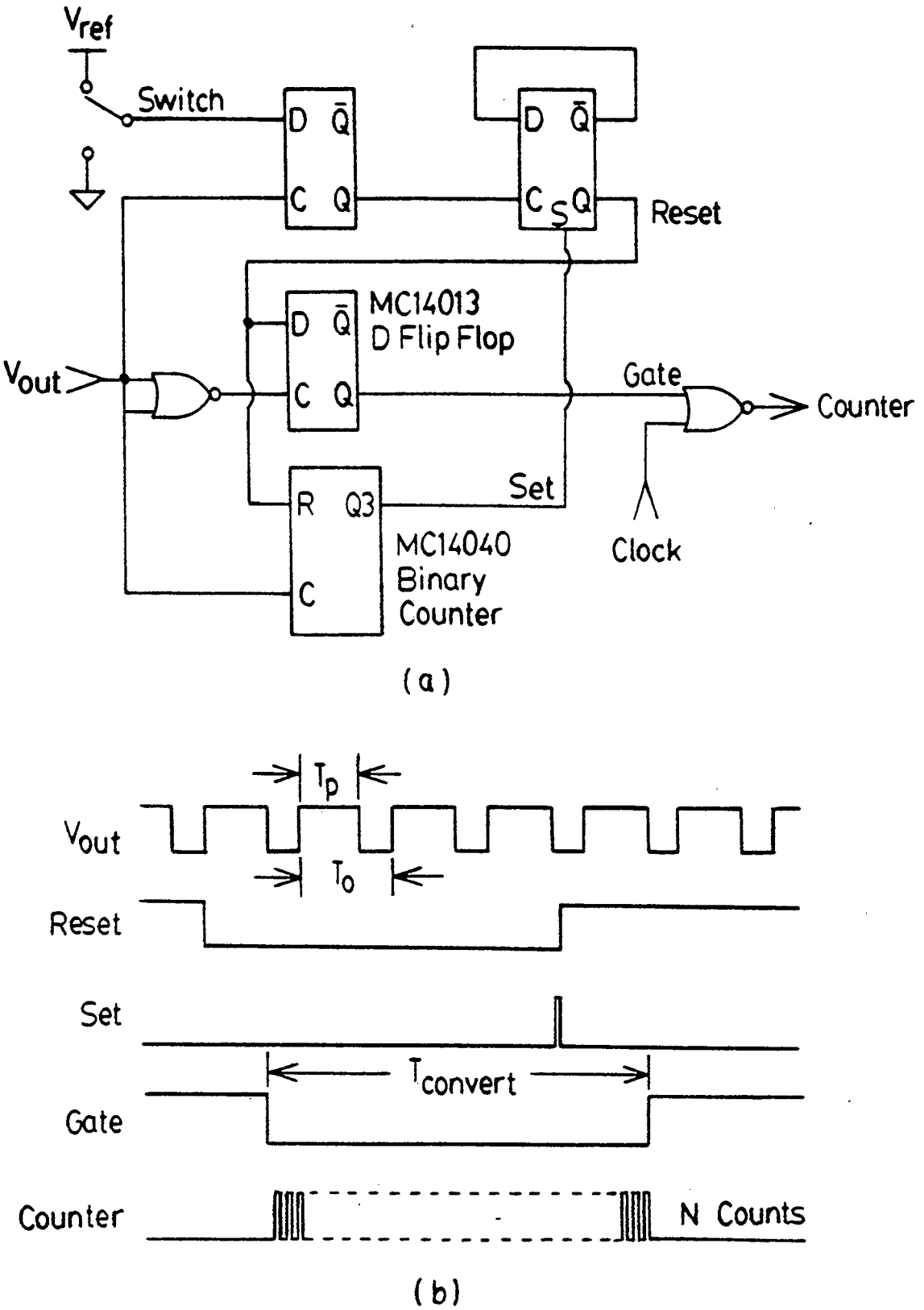


Fig.4.4 The Single-Counter Inverse Counting Scheme: (a) Circuit Diagram and (b) Timing Diagram

$$T_{convert} = n\ T_{o_{ave}} \tag{4.12}$$

and the time required for the switch to stay closed can be as large as $(n+1)T_{o_{ave}}$. Since the conversion time and the value of N now depend on the input voltage, the resolution of $\frac{V_t}{V_{ref}}$ will vary with V_t so that

$$resolution\ in\ (\frac{V_t}{V_{ref}}) = \pm 1\ part\ in\ (\frac{m\ n\ V_{ref}}{V_t}), \tag{4.13}$$

which will be a minimum at full scale.

The practical implementations of the clock-controlled VFC and its counting circuits will be discussed in detail in Chapter 5. Meanwhile, two other useful features of the clock-controlled VFC will be outlined in the remaining sections of this chapter.

4.6 Direct Frequency Conversion

Accurate *instantaneous frequency conversion* can be provided by the clock-controlled VFC without circuit modification. Instantaneous (or direct) frequency conversion means that the VFC output frequency is instantaneously proportional to the input voltage as in the improved VFC of Chapter 2. Direct frequency conversion is very useful because direct counting over a fixed period of time can be performed at the VFC output so that a numerical division is not necessary as in the case of inverse counting [1,9].

An instantaneous frequency output can be obtained from the clock-controlled VFC of Fig.4.1 by taking the Q output from D *flip flop* 2 (V_5.) The waveform of V_5 is shown in Fig.4.5 together with other related waveforms of the circuit. It can be

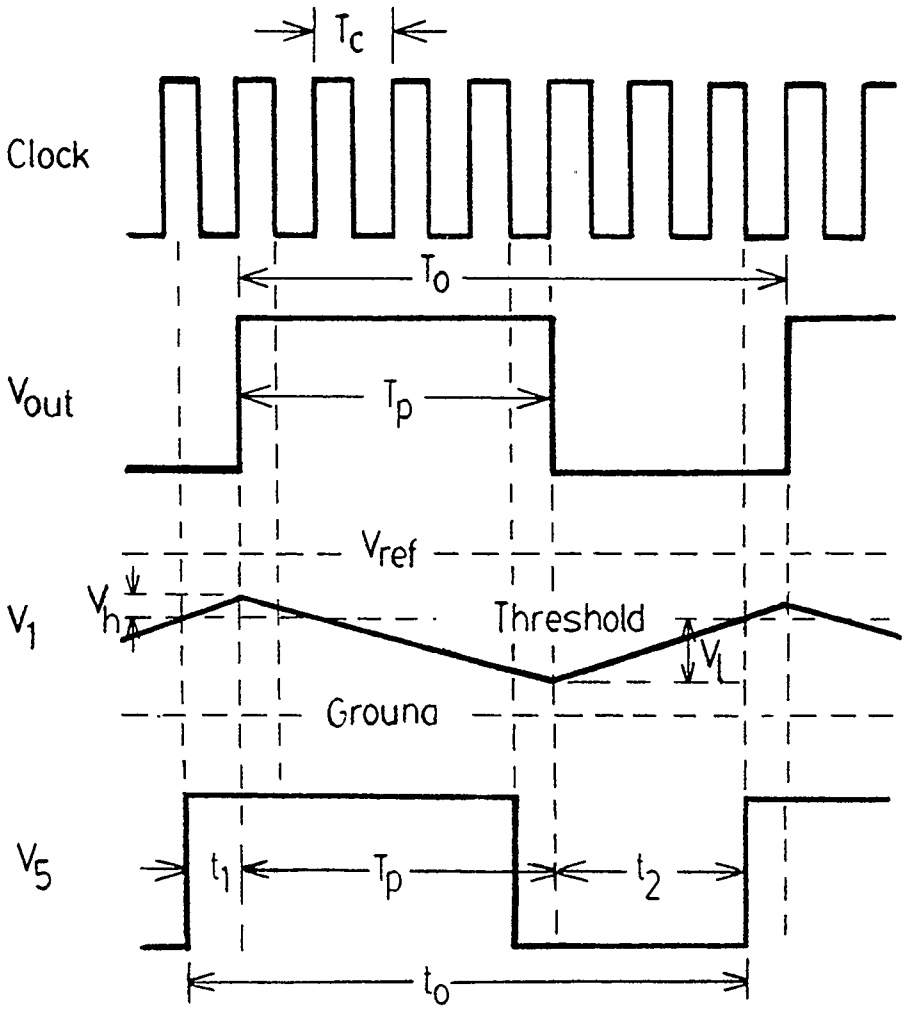


Fig.4.5 Voltage Waveforms for Direct Frequency Conversion

shown that the instantaneous frequency of V_5, denoted by f_{inst}, is directly proportional to V_t: Consider the instantaneous period t_o, where $t_o = \frac{1}{f_{inst}}$, to be sum of t_1, T_p, and t_2, as defined in Fig.4.5. Since

$$V_h = \frac{V_t}{R_4 C_4} t_1, \tag{4.14}$$

$$V_h + V_l = \frac{V_{ref} - V_t}{R_4 C_4} T_p, \tag{4.15}$$

and

$$V_l = \frac{V_t}{R_4 C_4} t_2, \tag{4.16}$$

t_o is given by

$$\begin{aligned} t_o &= t_1 + T_p + t_2 \\ &= R_4 C_4 (V_h + V_l) \frac{V_{ref}}{V_t (V_{ref} - V_t)}. \end{aligned} \tag{4.17}$$

From Eq.(4.15), it can be seen that

$$T_p = R_4 C_4 \frac{V_h + V_l}{V_{ref} - V_t} \tag{4.18}$$

so that,

$$f_{inst} = \frac{1}{t_o} = \frac{V_t}{V_{ref} T_p}. \tag{4.19}$$

Hence, an output frequency which is directly proportional to the input voltage and phase-independent of the system clock is obtained. This VFC is much more accurate than the improved VFC of Chapter 2 due to the fact that a clock-controlled pulse width is much more stable than its RC-controlled counterpart. A VFC with similar

characteristics can also be found in a recent patent [9]. However, the VFC described in [9] has a maximum input range from ground to $\frac{1}{2}V_{ref}$ only, which makes it inherently inferior to the VFC described here.

The accuracy of this VFC can be evaluated by measuring the output frequency with a frequency counter. The conversion error is found to be less than 0.001% of full scale and is basically limited by the stability of the crystal clock frequency.

4.7 Frequency-to-Voltage Converter

A frequency-to-voltage converter is useful when an analog output is required in a long-distant digital transmission system. The clock-controlled VFC can be configured as a frequency-to-voltage converter easily as shown in Fig.4.6. This circuit uses the same circuit topology as the VFC with the operational amplifier working as an output buffer. Fig.4.7 shows the voltage waveforms at different points of of the circuit.

Consider *D flip flop* 2 of the circuit in Fig.4.6. When its *reset* input (V_4) is low and its $\overline{Q}$ output (V_2) is high, a low-to-high transition at its clock input will cause V_2 to go low. Then, on the next rising clock edge, V_{out} will go high and V_3 will go low, and this high-to-low transition will initiate the counter to count a preset multiple of falling clock edges. When the counter finishes counting, its output will go high and reset *D flip flop* 2. V_2 will then go high, and on the next rising clock edge, V_{out} will go low. The cycle will thus repeat on the next rising edge of the input. Since the frequency input of this circuit is edge-triggered, the input waveform need not be symmetrical as long as its pulse width is greater than one clock period.

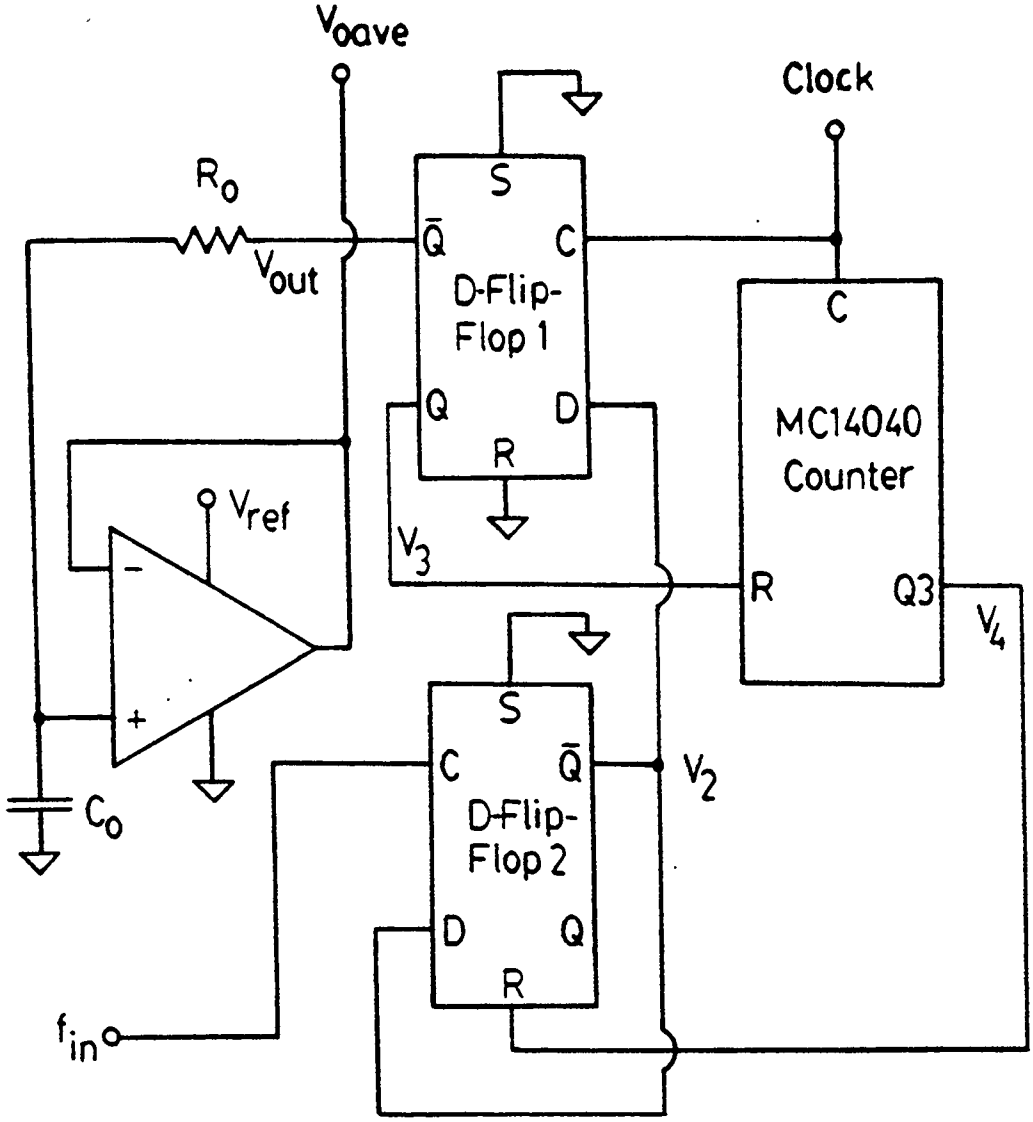


Fig.4.6 The Frequency-to-Voltage Converter

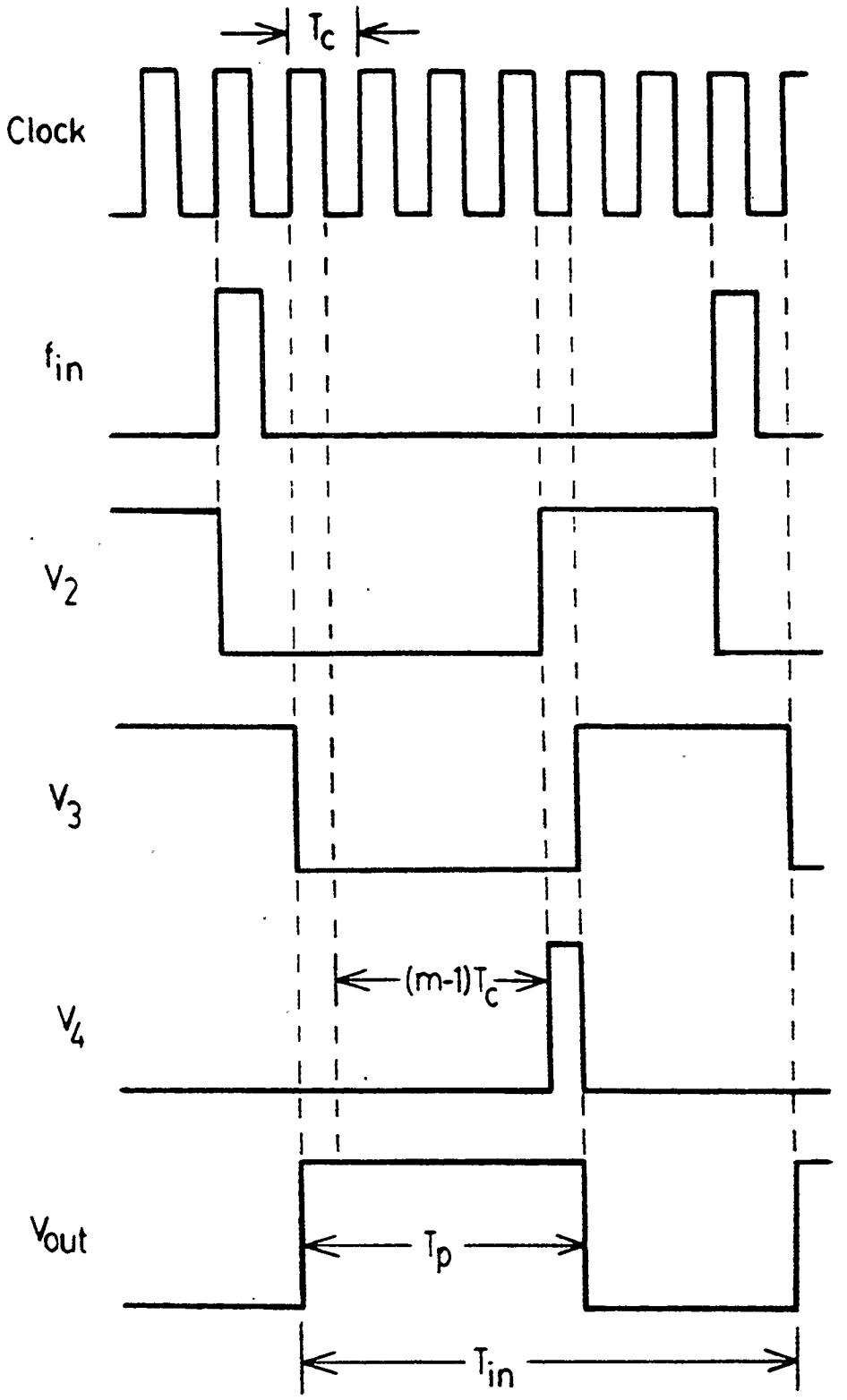


Fig.4.7 Voltage Waveforms for the Frequency-to-Voltage Converter

If R_o and C_o are large, the average output, V_{oave}, can be determined by writing the charge balance equation for C_o as

$$\frac{V_{ref}}{R_o}T_p - \frac{V_{oave}}{R_o}T_{in} = 0 \tag{4.20}$$

so that

$$\frac{V_{oave}}{V_{ref}} = \frac{T_p}{T_{in}} = \frac{f_{in}}{f_{\max}} \tag{4.21}$$

where V_{ref} is the supply voltage, $T_p = \frac{1}{f_{\max}}$ is the output pulse width, and $f_{in} = \frac{1}{T_{in}}$ is the input frequency.

The maximum (or full-scale) input frequency, $f_{\max}$, can be adjusted easily by altering T_p since

$$T_p = m\ T_c \tag{4.22}$$

where T_c is the clock period and the values $m = 1,2,4,..,2^{11}$ are available on the *MC* 14040 counter. Since the input period has to be at least one clock period larger than T_p, the input frequency range is given by

$$0 < \frac{f_{in}}{f_{\max}} < (1 - \frac{1}{1+m}), \tag{4.23}$$

Since fewer clock pulses will be included in each input cycle, the conversion error will increase as $\frac{f_{in}}{f_{\max}}$ increases. The error is also a function of the maximum input frequency due to the increasing effect of the output pulse shape on V_{oave} as frequency increases. Fig.4.8 shows the error in the average output at half-scale input

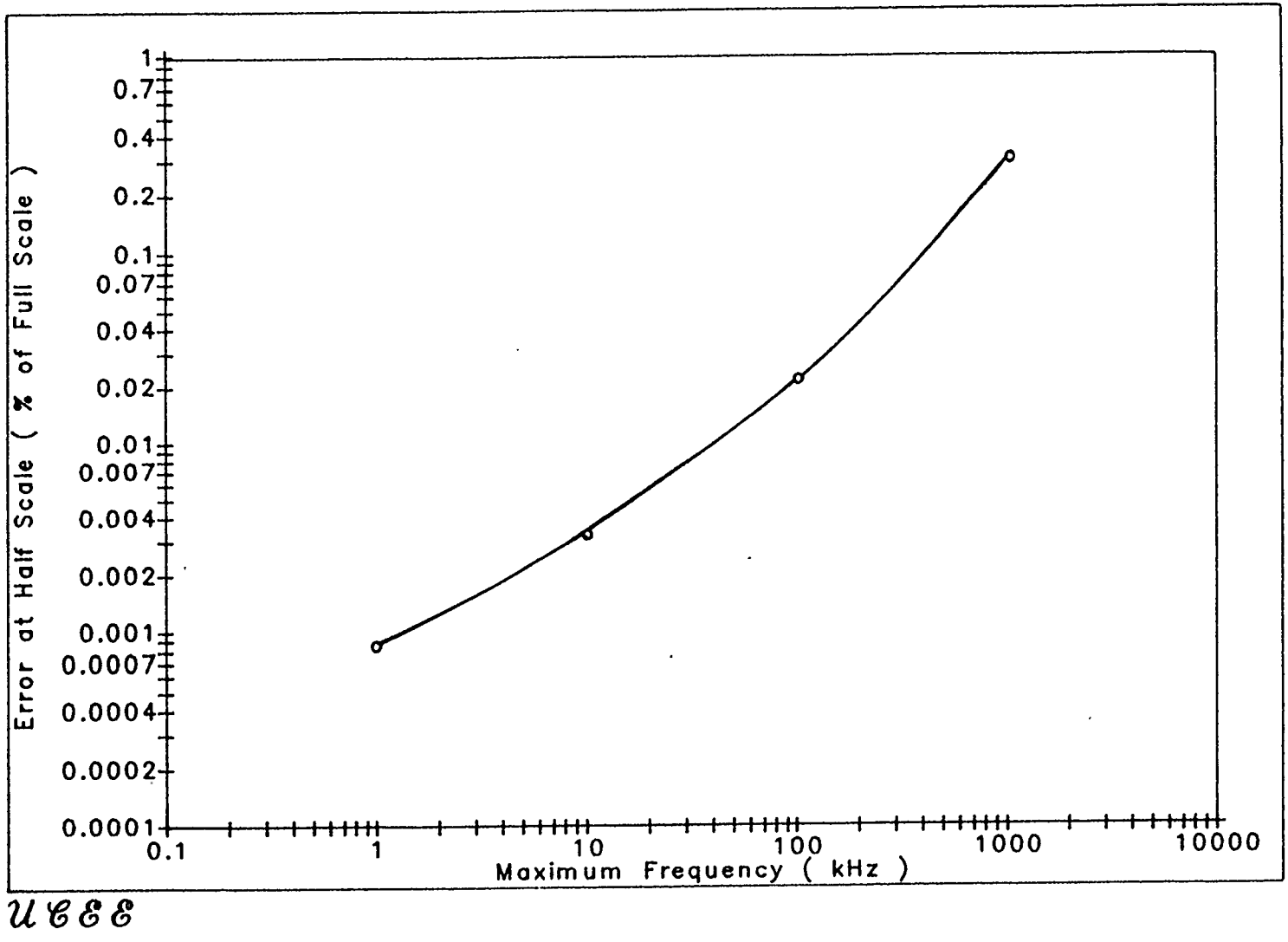


Fig.4.8 Variation of Half-Scale Conversion Error with Frequency

versus the maximum frequency. The error analysis of this frequency-to-voltage converter is similar to that of the clock-controlled VFC and will be discussed in Chapter 5.

CHAPTER 5

PRACTICAL CONSIDERATIONS

5.1 Introduction

As stated in Chapter 1, the synchronized and clock-controlled VFCs have to satisfy several performance criteria to be competitive with existing VFCs on the market. The circuit structures of the synchronized and clock-controlled VFCs are such that these circuits are simple, are capable of elementary signal linearization, and can be operated from either a single or a dual power supply. Furthermore, by using the ICL7650 chopper-stabilized amplifier, a useful input range from the negative supply to two-third of full scale is obtained, a reasonable 2mA operating current can be used, and a low component cost of about ten dollars is achieved. Thus, resolution, accuracy, linearity, operating-frequency range, and temperature stability are left to be examined. These factors will be investigated in this chapter and a summary of the VFC performance characteristics will be presented.

5.2 VFC Implementation and Testing

The practical implementations of the synchronized VFC and the clock-controlled VFC with commonly available commercial components are shown in Fig.5.1 and Fig.5.2 respectively. Notice that extra circuit components are added to the original designs in both circuits:

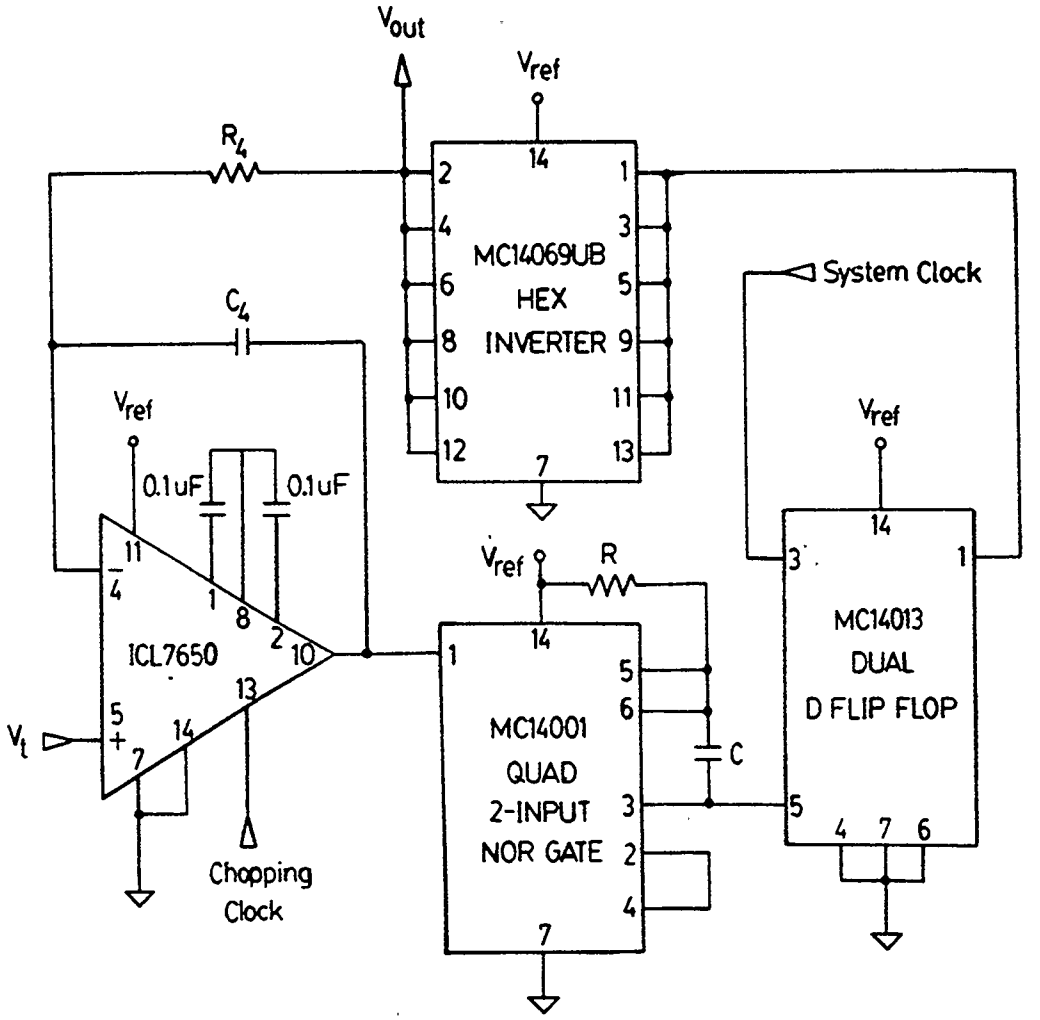


Fig.5.1 Practical Implementation for the Synchronized VFC

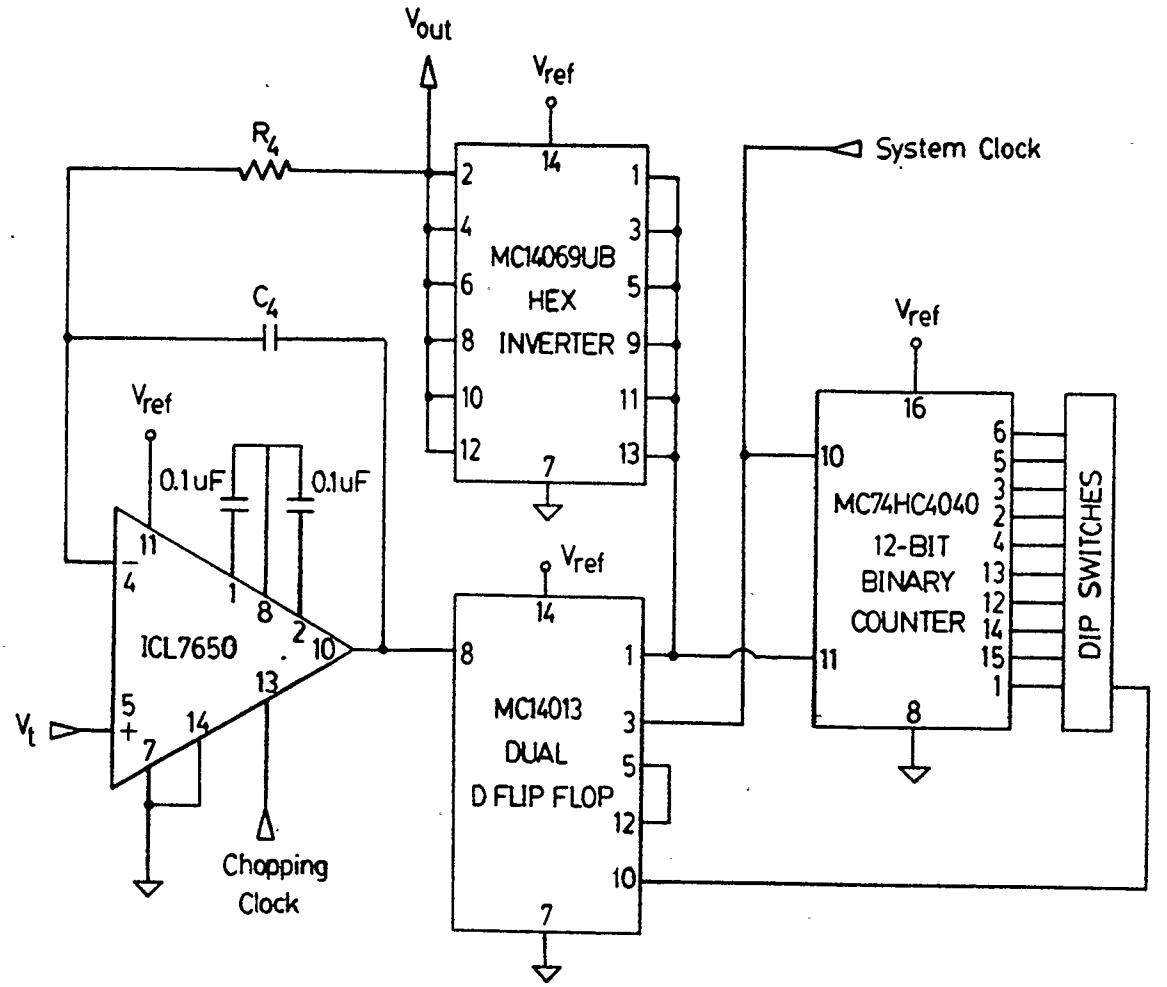


Fig.5.2 Practical Implementation for the Clock-Controlled VFC

(1) Six parallel inverters are added between the flip-flop output and R_4 in each circuit. This reduces the effect of the difference between the *high* and *low* output resistances of the CMOS gates on the VFC output waveform, as will be noted in a later section of this chapter.

(2) Switches are used to select the suitable output tap from the counter to reset the flip-flop in the clock-controlled VFC circuit. This enables the changing of operating frequency without altering the system-clock frequency.

(3) The *MC* 14040 CMOS counter is replaced by an *MC*74*HC*4040 high-speed CMOS counter. When a 4MHz system clock is used, the propagation delay from the *reset* input to some of the outputs of a low-speed CMOS counter is longer than one clock cycle. This leads to a serious error in output counting for any clock frequency greater than 1 MHz. The high-speed version does not have this problem.

(4) An external clock is used for the chopper-stablized amplifier. Thus, the effect of changing the chopping-clock frequency can be examined easily.

A useful counting circuit for both the synchronized VFC and the clock-controlled VFC (with either single or double counter conversion scheme) can be implemented as shown in Fig.5.3. Three counter outputs are provided and the selection of the appropriate one depends on the counting scheme.

Since the VFC circuits are expected to be very accurate, testing must be carried out with extreme care. A system that can produce and measure a voltage ratio (V_t/V_{ref}) to within ±1 ppm (part-per-million) of full scale is shown in Fig.5.4. The

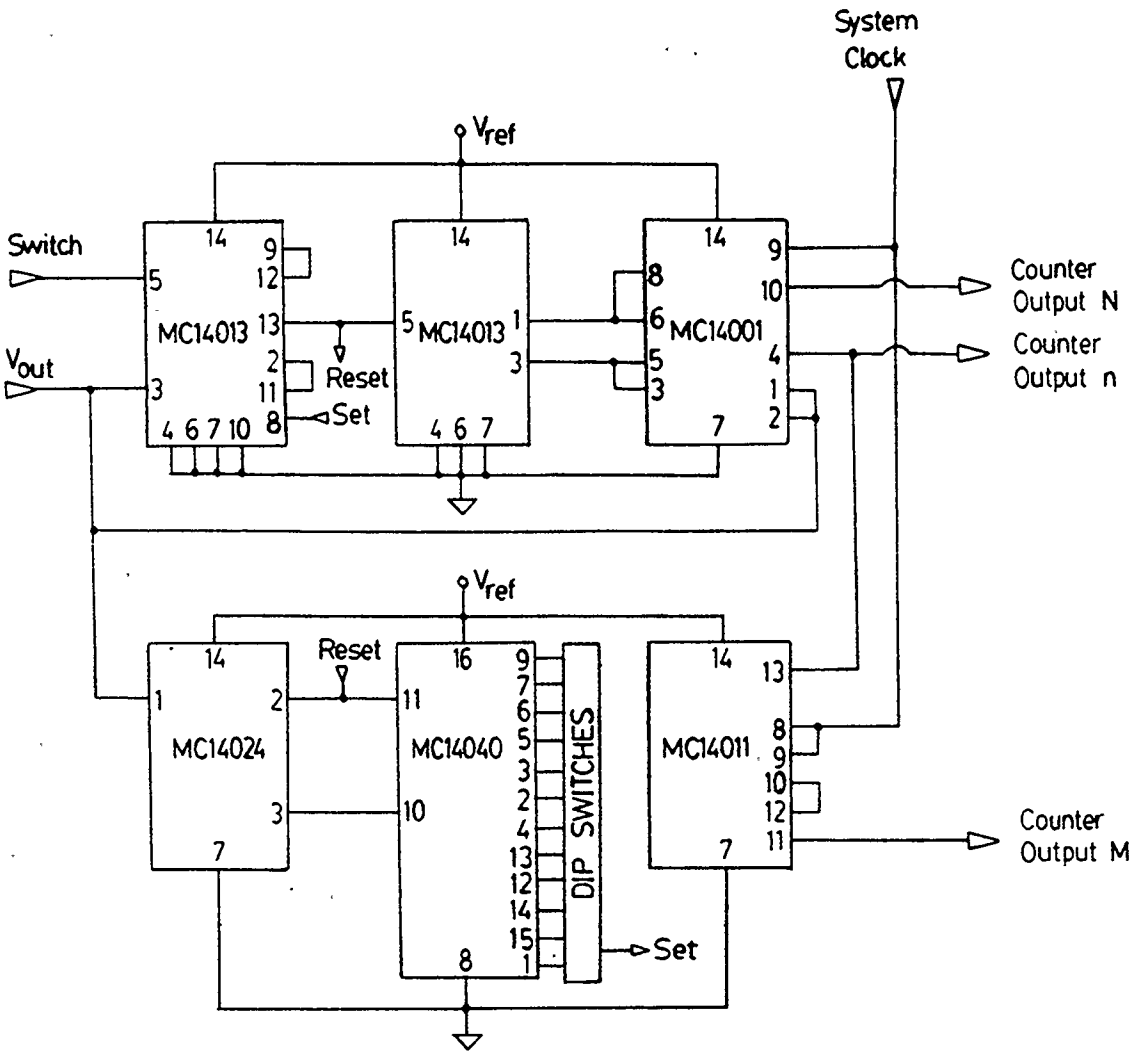


Fig.5.3 Practical Implementation of a Counting Circuit for both VFCs

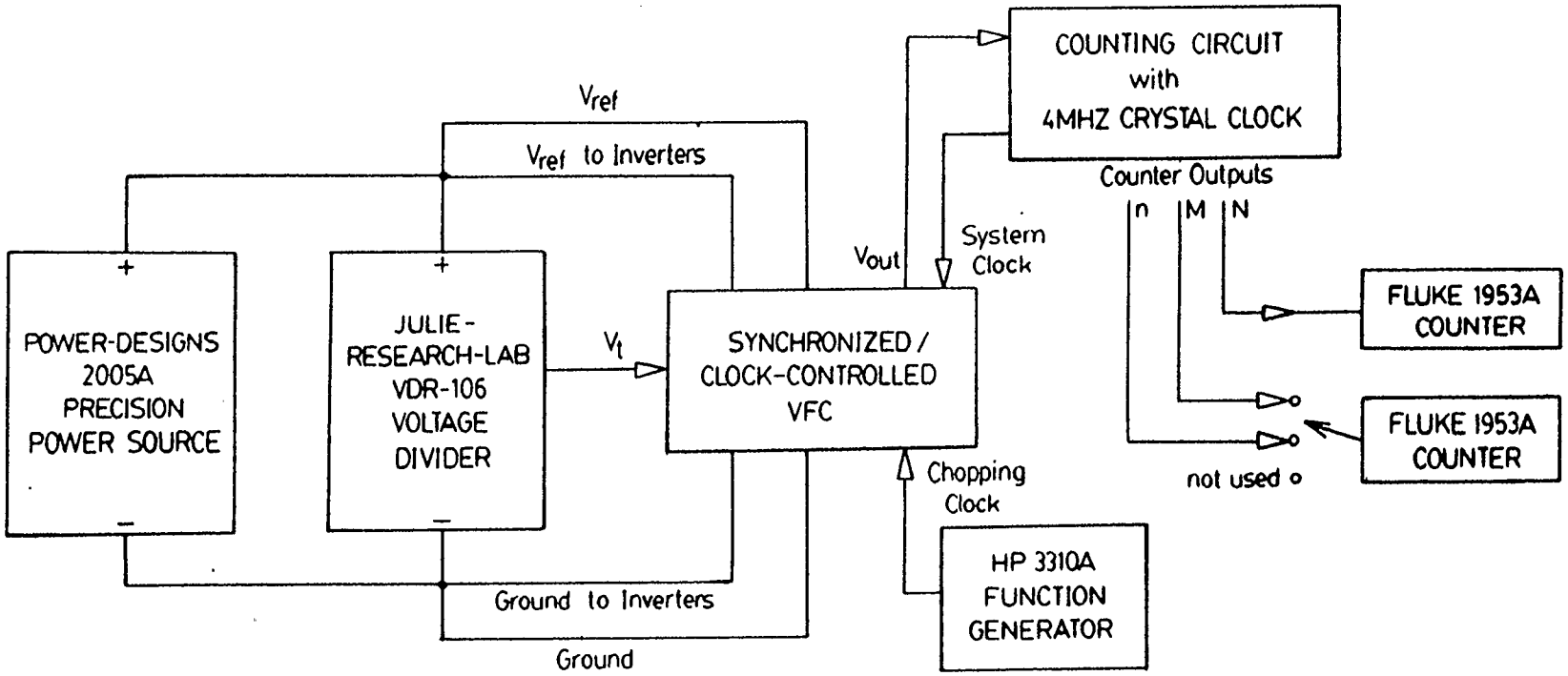


Fig.5.4 High-Accuracy VFC Measuring System

Power Designs 2005*A* precision power supply provides a stable reference to within 1mV. However, the stability of the supply voltage is not critical with this set-up since the voltage ratio V_t/V_{ref} is obtained with a voltage divider. The *Julie Research Lab. VD*−106 voltage divider is accurate to within 1 ppm of the supply voltage under all settings [12]. It should be noted that a separate pair of power-supply rails is used to power the output inverters of the VFC under test. If only a single pair of supply rails was used, the relatively large amount of current (2mA) drawn by the amplifier would have lead to a significant voltage drop along the supply rails so that the high and low levels of V_{out} would not correspond to those across the voltage divider. When this system is carefully set up (with short and thick wires and carefully laid out and by-passed power supplies), reliable measurements can then be made on the VFCs.

5.3 Performance Evaluation

In this section, some of the important properties of the VFCs - resolution, accuracy, linearity, and temperature stability - are examined. Although all experimental results presented here are based on measurements on the clock-controlled VFC because of its simplicity of single-counter conversion, all results and analyses apply equally well to the synchronized VFC.

Resolution

Theoretically, the resolution of the inverse-counting A/D conversion scheme is ±1 part in the number of counts within the conversion time.

Practically, the resolution is affected by (1) input and power-supply noise, (2) temperature drift of the amplifier offset voltage and bias current, and (3) inconsistent leakage across the integrating capacitor due to moisture, etc.. Although the VFCs are inherently immune to noise, large voltage spikes induced by the high-frequency system clock may appear at the input and the supply rails causing noticeable fluctuations. This high-frequency noise can be significantly reduced by capacitive decoupling. With decoupling, the conversion resolution is measured to be of the order of 0.1 ppm at low operating frequencies ($\leq$ 10kHz) and close to 1 ppm at frequencies as high as 1 MHz. Furthermore, with careful circuit handling, the combined instability due to mild temperature drift ($< 1^{o}C$), moisture, pick-up, etc. is of the order of 0.1 ppm, which is beyond the accuracy of the circuits.

Accuracy

The accuracy of the VFCs is affected by three major factors: (1) op-amp non-idealities, (2) output resistances of the CMOS inverters driving the integrator, and (3) imperfect output pulse shape.

The effects of the first two factors can be considered by re-writing the instantaneous charge balance equation for capacitor C_4 as follows [13]:

$$\frac{V_{ref} - V_t'}{R_4 + r_h} T_p - \frac{V_t'}{R_4 + r_l}(T_o - T_p) - I_B^- T_o = 0 \tag{5.1}$$

with

$$V_t' = V_t + V_{os} + \frac{(\frac{V_{ref}}{2} - V_t)}{CMRR} \tag{5.2}$$

where

r_h = *combined output resistance of six parallel inverters at the high state*,

r_l = *combined output resistance of six parallel inverters at the low state*,

I_B^- = *amplifier negative–input bias current*,

V_{os} = *amplifier offset voltage*, and

$CMRR$ = *amplifier common–mode rejection ratio.*

From Eq.(5.1), it can be shown that

$$\frac{T_p}{T_o} = \frac{V_t'}{V_{ref}} \left[1 + \frac{(1 - \frac{V_t'}{V_{ref}})(\frac{r_h - r_l}{R_4 + r_l}) + I_B^- \frac{(R_4 + r_h)}{V_t'}}{1 + \frac{V_t'}{V_{ref}} \frac{(r_h - r_l)}{(R_4 + r_l)}} \right] \tag{5.3}$$

so that the error due to $r_h - r_l$ (defined as r_d) is given by

$$error, fraction\ of\ full\ scale = \frac{V_t}{V_{ref}}(1 - \frac{V_t}{V_{ref}})(\frac{r_d}{R_4}) \tag{5.4}$$

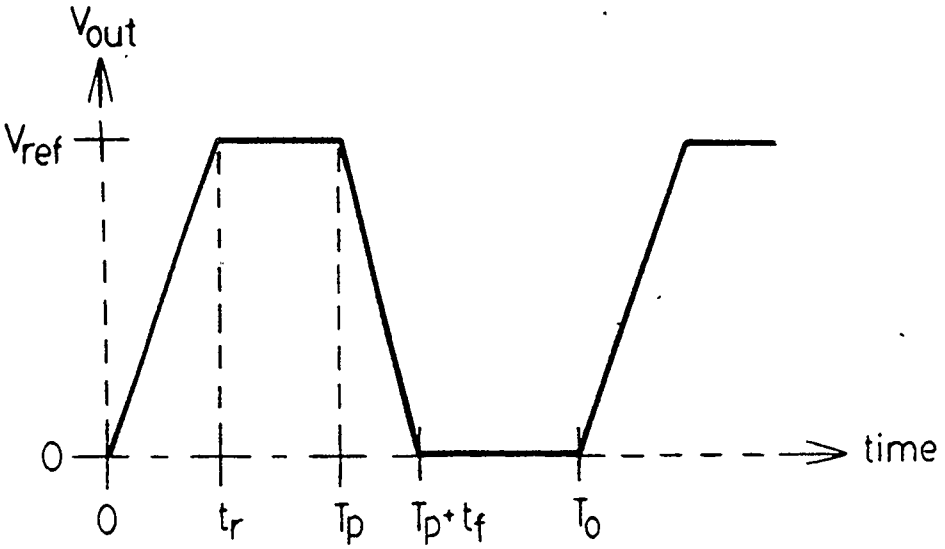
while the error due to amplifier non-idealities is given by

$$error, fraction\ of\ full\ scale = \frac{V_{os}}{V_{ref}} + \frac{(\frac{1}{2} - \frac{V_t}{V_{ref}})}{CMRR} + \frac{I_B^- R_4}{V_{ref}}. \tag{5.5}$$

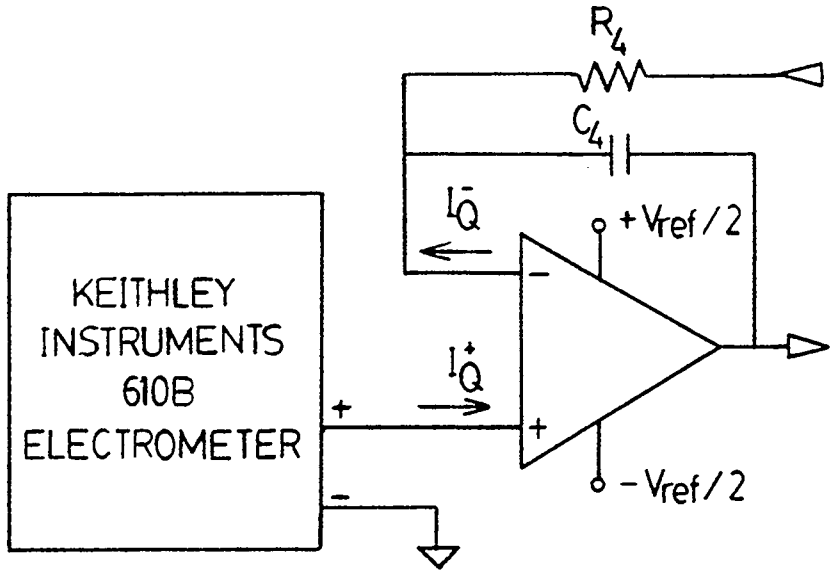
The effect of pulse shape can be considered by defining the rise and fall times (t_r and t_f) of the output inverters as illustrated in Fig.5.5(a). With other non-idealities neglected, the instantaneous charge balance equation can be written as

$$-\frac{V_t}{R_4} T_p + \frac{V_{ref}}{R_4} \left[\int_0^{t_r} \frac{t}{t_r} dt + \int_{t_r}^{T_p} dt + \int_{T_p}^{T_p + t_f} \frac{T_p + t_f - t}{t_f} dt \right] = 0 \tag{5.6}$$

so that



(a)



(b)

Fig.5.5 Non-Ideal Effects:
(a) Imperfect Output Pulse Shape due to Rise and Fall Times
(b) Currents due to Charge Pumping (and I_Q^+ Measurement)

$$\frac{T_p}{T_o} = \frac{V_t}{V_{ref}} - \frac{t_r - t_f}{2T_o}. \tag{5.7}$$

Thus the error due to pulse shape is given by

$$\begin{aligned} error, fraction\ of\ full\ scale &= -\frac{t_d}{T_o} \\ &= -\frac{V_t}{V_{ref}}\frac{t_d}{T_p} \\ &= -\frac{V_t}{V_{ref}} t_d f_{\max} \end{aligned} \tag{5.8}$$

where $t_d = \frac{t_r - t_f}{2}$ and $f_{\max} = \frac{1}{T_p}$.

Since these errors are independent of each other, they can be summed up as follows:

$$\begin{aligned} total\ error, fraction\ of\ full\ scale = \frac{V_{os}}{V_{ref}} + \frac{(\frac{1}{2} - \frac{V_t}{V_{ref}})}{CMRR} + \frac{I_B^- R_4}{V_{ref}} \\ + \frac{V_t}{V_{ref}}(1 - \frac{V_t}{V_{ref}})(\frac{r_d}{R_4}) - \frac{V_t}{V_{ref}} t_d f_{\max}. \end{aligned} \tag{5.9}$$

With the ICL7650 chopper-stablized amplifier, V_{os} is less than 5 μV and $CMRR$ is over 120dB. The combined error is thus less than 0.5 ppm for V_{ref} = 10V. The value of r_d for six MC14069 inverters in parallel is measured to be 12Ω. Thus the maximum error due to r_d is $\frac{3\Omega}{R_4}$ at $\frac{V_t}{V_{ref}} = \frac{1}{2}$, which will be 1 ppm of full scale if R_4 is set to $3M\Omega$. Furthermore, t_d is estimated to be about 3nS, which will lead to a maximum error of -1.5 ppm at full scale if $f_{\max}$ is kept at 500Hz. Thus, the total error

due to V_{os}, $CMRR$, r_d and t_d can be kept to within ±1.5 ppm of full scale with the proper choices of R_4 and f_{max}.

The bias current of the amplifier also affects the accuracy of the circuit. The specified value for I_B^- for the *ICL*7650 is 1.5pA (typical), which should give rise to an error of about 0.5 ppm of full scale with $R_4 = 3M\Omega$ and $V_{ref} = 10V$. However, preliminary testing shows convincingly that a current which is much higher than the specified value of I_B^- actually *flows out* from the negative terminal of the amplifier. This current appears to be caused by charge pumping between the two input terminals due to the auto-zeroing feature of the amplifier. This current flowing out of the negative terminal due to charge pumping (symbolized hereafter by I_Q^-) and the current flowing into the positive terminal due to charge pumping (I_Q^+) can be as high as a few hundred pico-amps and are found to be functions of V_{ref}, V_t, and the external chopping-clock frequency f_z. Currents of this magnitude are not detectable by measuring the voltage drop across a resistor with a normal voltmeter and hence a sensitive ammeter has to be used. A highly-sensative *Keithley Instruments* 610*B* electrometer was available to the author. Unfortunately, in low current measurements, the negative input terminal of this electrometer is automatically tied to the system ground. As a result, it is impossible to directly measure I_Q^- when the VFC is operating. However, by measuring I_Q^+ as shown in Fig.5.5(b), an indication of the behavior of I_Q^- can be obtained. Fig.5.6 shows I_Q^+ as functions of f_z and V_t/V_{ref} (with V_{ref} = 10V.) It shows that I_Q^+ is less than ±2pA at $V_t/V_{ref} = 0.5$ regardless of f_z but increases linearly as f_z increases or as V_t/V_{ref} moves away from 0.5. It is then logical to predict that I_Q^- behaves similarly.

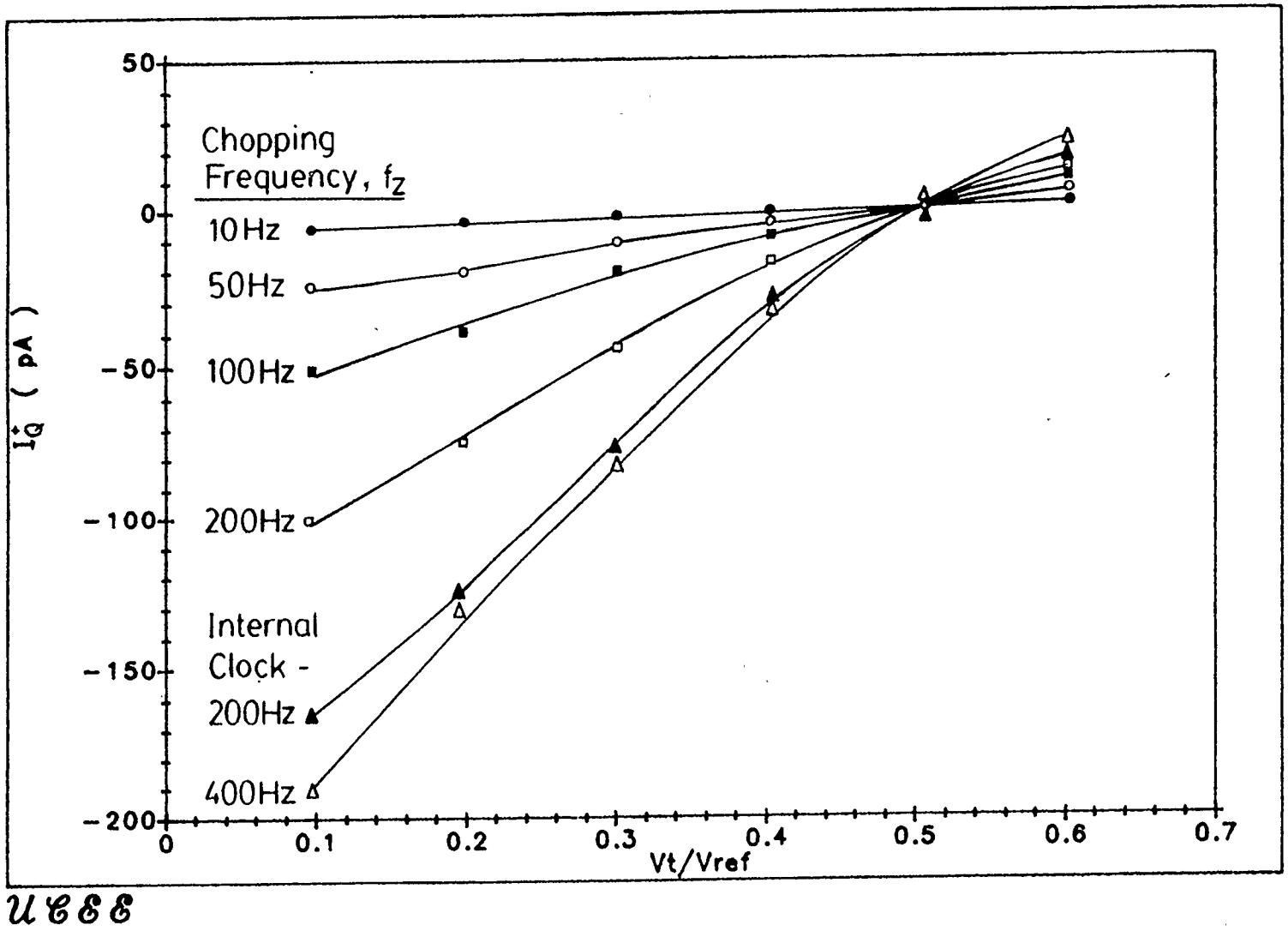


Fig.5.6 Variation of I_Q^+ with Chopping Frequency and Input Voltage

The effect of I_Q^- can be isolated by subtracting the known effects of R_4 and t_d from the measurements. Fig.5.7 shows the measured errors as f_z is varied. The circuit is operating at $f_{\max}$ = 500Hz with $R_4 = 3M\Omega$ so that the errors are mainly due to I_Q^-. By comparing Fig.5.6 and Fig.5.7, it can be seen that I_Q^- and I_Q^+ show similar functional dependencies on V_t/V_{ref} and f_z although their magnitudes are different. For example, for f_z =100Hz and V_t/V_{ref} = 0.1, the 19 ppm of full scale error shown in Fig.5.7 must have been caused by an I_Q^- of about 63pA, which is 26% higher than the 50pA measured for I_Q^+.

With the effect of I_Q^- closely determined for a number of chopping frequencies, the total error for the VFCs can be predicted by the following equation:

$$\begin{aligned} \textit{total error, fraction of full scale} = \frac{V_{os}}{V_{ref}} + \frac{(\frac{1}{2} - \frac{V_t}{V_{ref}})}{CMRR} + \frac{I_Q^- \left[\frac{V_t}{V_{ref}} f_z\right] R_4}{V_{ref}} \\ + \frac{V_t}{V_{ref}}(1 - \frac{V_t}{V_{ref}})(\frac{r_d}{R_4}) - \frac{V_t}{V_{ref}} t_d f_{\max} \end{aligned} \tag{5.10}$$

where I_Q^- is a function of V_t/V_{ref} and f_z as described in Fig.5.7. The effect of changing f_z has already been shown in Fig.5.7, while the effects of changing R_4 and $f_{\max}$ are shown in Fig.5.8 and Fig.5.9 respectively. The close fit between the measured and predicted errors in these figures shows that the total error of the VFCs can be fully described by Eq.(5.10) and can be easily minimized with proper choices of parameters. As shown in all three figures, the total error can be kept to within ±2 ppm of full scale with f_z = 10Hz, $R_4 = 3M\Omega$, $f_{\max}$ = 500Hz, and V_{ref} = 10V.

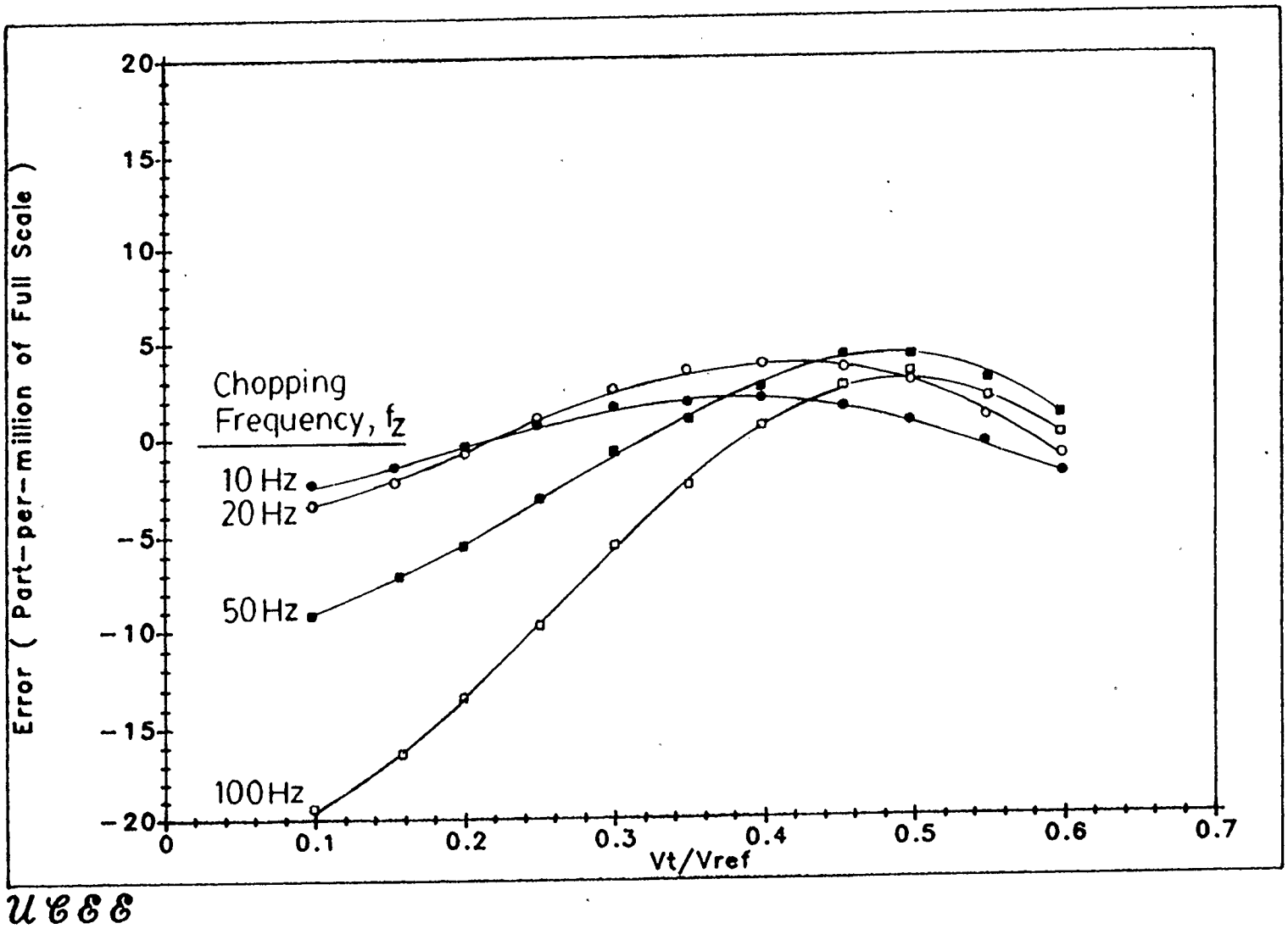


Fig.5.7 Variation of Error with Chopping Frequency and Input Voltage
(with $R_4 = 3M\Omega$ and $f_{max} = 500$Hz)

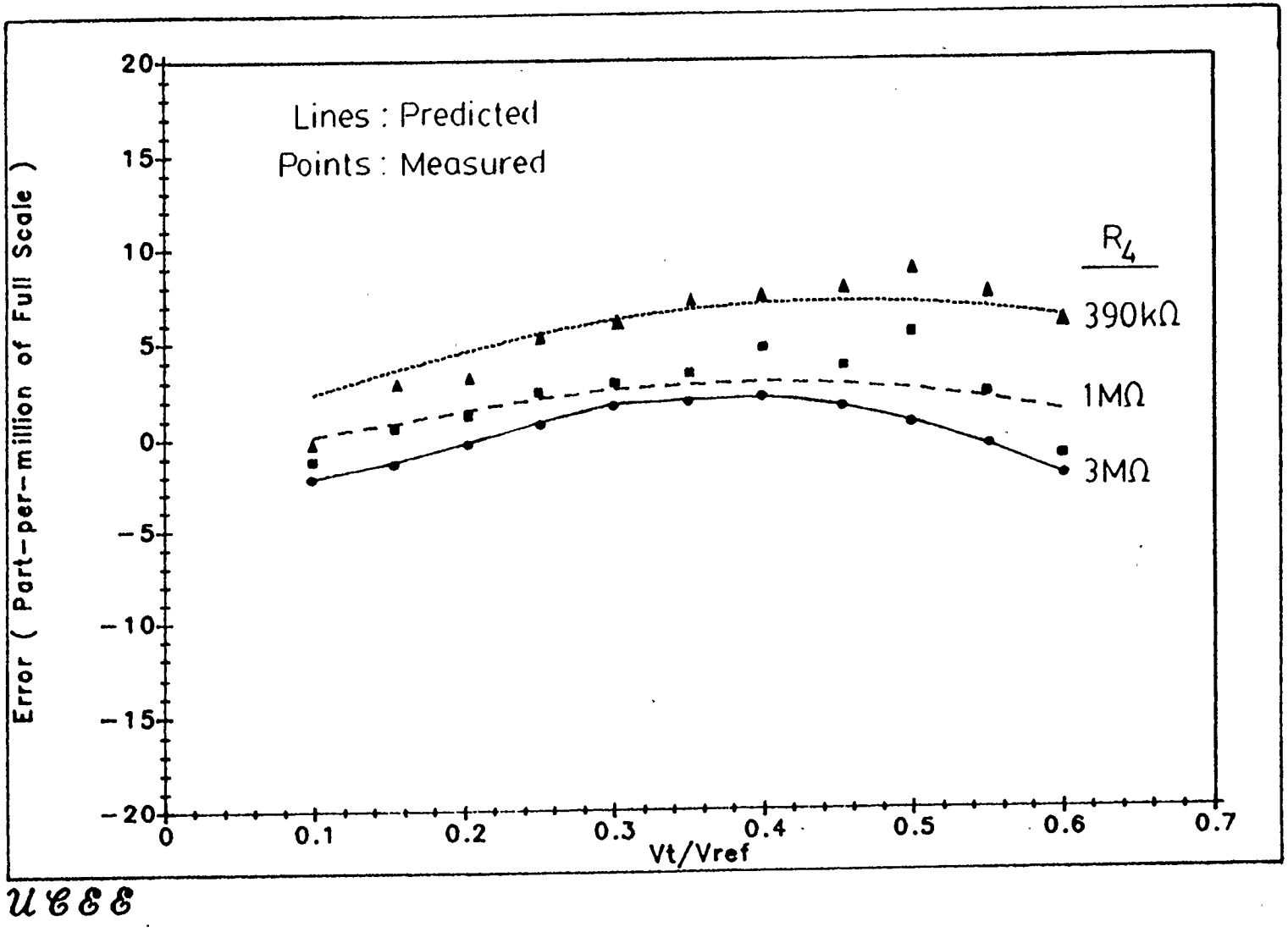


Fig.5.8 Effect of Changing R_4 (with f_z = 10Hz and f_{max} = 500Hz)

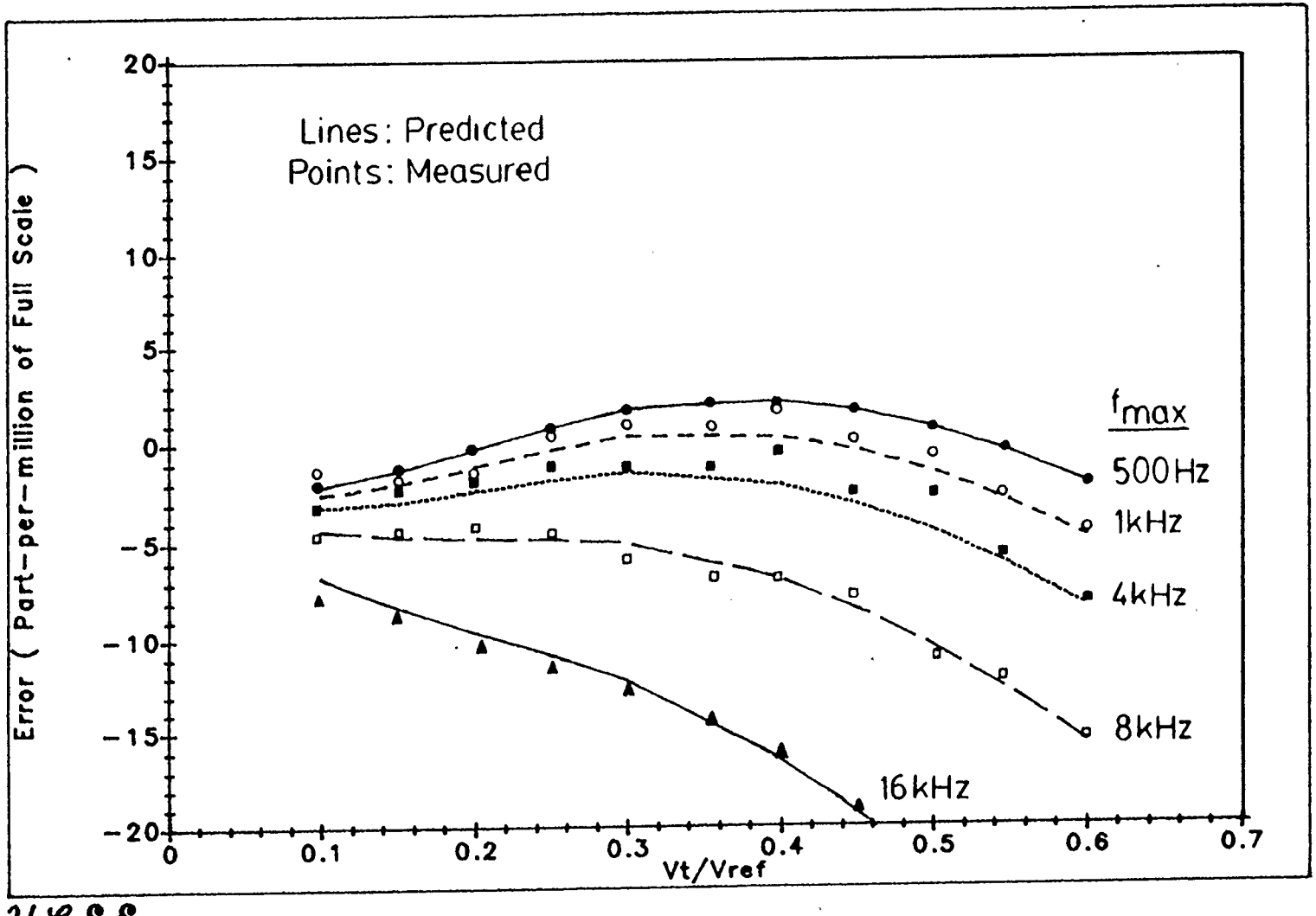


Fig.5.9 Effect of Changing f_{max} (with $R_4 = 3M\Omega$ and f_z = 10Hz)

Temperature Stability

As the ambient temperature changes, the accuracy of the VFCs is affected while the resolution remains the same as long as the temperature is stable when measurements are taken. The conversion errors as the ambient temperature varies from 0 to $70^{o}C$ (the temperature range of the amplifier) are shown in Fig.5.10. The temperature drift of error is mainly due to the fluctuation of $I_{\bar{Q}}$ and is less than 0.1 ppm/^{o}C over the temperature range tested.

Linearity and Operating-Frequency Range

In a data acquisition system, a micro-computer is often employed to count the VFC output and perform the division ($\frac{mn}{N}$ or $\frac{M}{N}$) to obtain a direct indication of the input [14,15]. Thus, simple calibration schemes can be carried out to extend the useful operating-frequency range of the system. As observed in Fig.5.9, as $f_{\max}$ increases, the conversion errors start to increase due to the effect of pulse shape; however, the errors over the input range increase in a linear fashion. If $f_{\max}$ is increased while keeping $R_4 = 3M\Omega$ and f_z = 10Hz, Eq.(5.10) becomes

$$total\ error, fraction\ of\ full\ scale \simeq -\frac{V_t}{V_{ref}} t_d f_{\max}, \tag{5.11}$$

which is a linear function of V_t/V_{ref} at a fixed maximum frequency. Thus, a simple *single–point* calibration scheme as described in Fig.5.11 can be used: A half-scale reference point can be pre-determined for a particular maximum operating frequency $f_{\max}$ by inputing the value of t_d into the computer. Next, a straight-line function is defined from V_t/V_{ref} = 0 to V_t/V_{ref} = 0.5 and stored in the computer. An error term

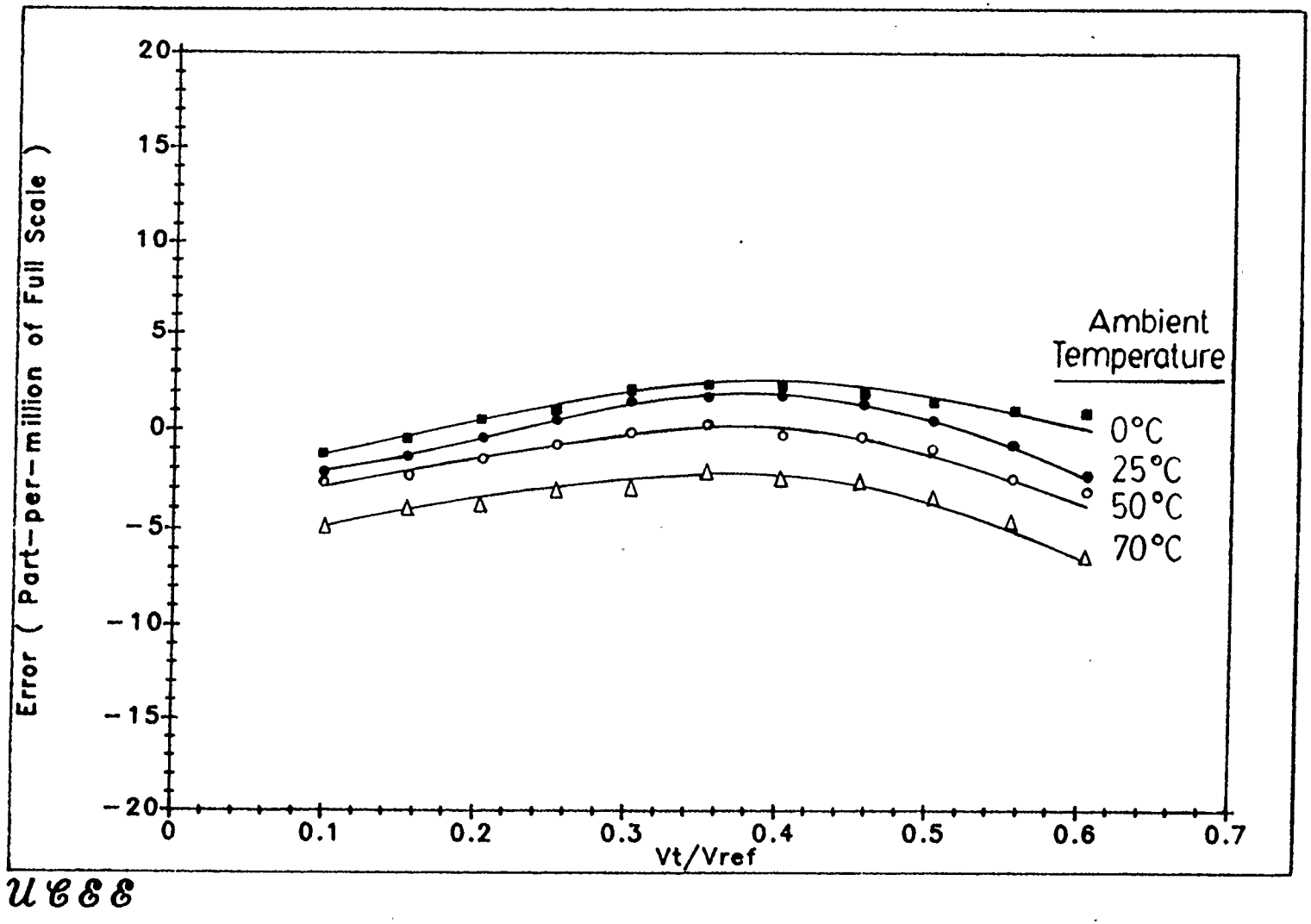


Fig.5.10 Effect of Temperature Variation

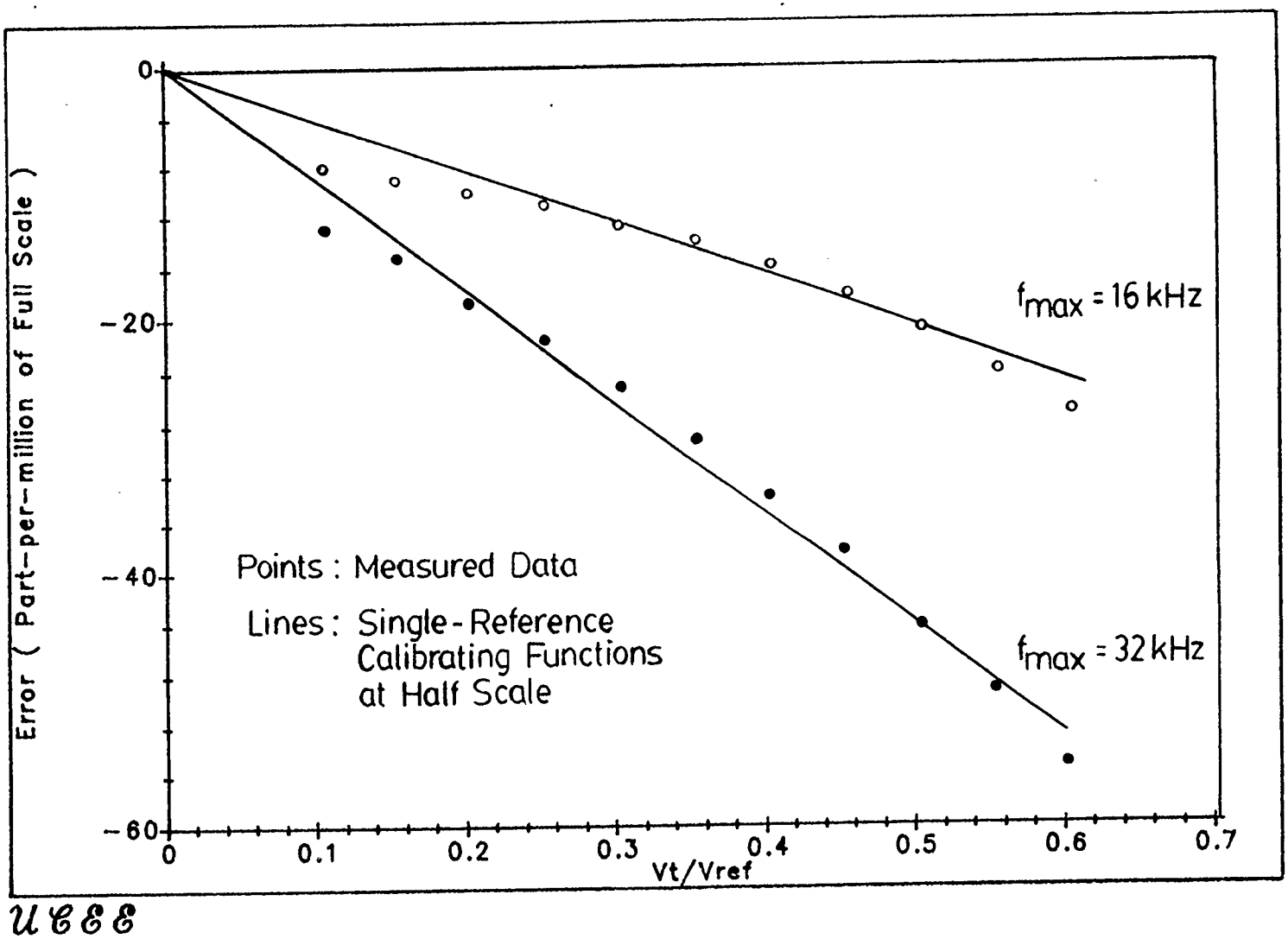


Fig.5.11 Single-Point Calibration with Reference at $V_t/V_{ref} = 0.5$

can then be subtracted from any measured data point to obtain the true input value. With this calibration scheme, non-linearity is only due to the terms $I_{\bar{Q}}R_4$ and r_d/R_4 in Eq.(5.10), which are independent of the operating frequency and can be kept to within ±2 ppm of full scale with the proper choice of R_4. Fig.5.12 shows the measured maximum deviation from linearity as a function of the maximum frequency. For f_{max} > 10kHz, linearity starts to degrade for two reasons: first, the slew rate of the amplifier starts to introduce errors and, second, the effect of output pulse shape can no longer be simply described by t_d alone. However, linearity is still within a reasonable 0.01% of full scale at frequency as high as 1MHz.

5.4 Summary of VFC Characteristics

The performance characteristics of the synchronized VFC and the clock-controlled VFC are summarized as follows:

(1) *High Resolution :* Resolution is within ±1 part in N (number of clock pulses within the conversion time) and can be as high as

$$\pm 0.1\ ppm\ of\ full\ scale \quad \text{for } f_{max} \le 10kHz \quad \text{and}$$
$$\pm 1\ ppm\ of\ full\ scale \quad \text{for } 10kHz \le f_{max} \le 1MHz.$$

(2) *High Accuracy :* Conversion error (without calibration) is not higher than

$$\pm 2\ ppm\ of\ full\ scale \quad \text{for } f_{max} \le 500Hz.$$

(3) *Low Temperature Drift:* The temperature coefficient for conversion error is

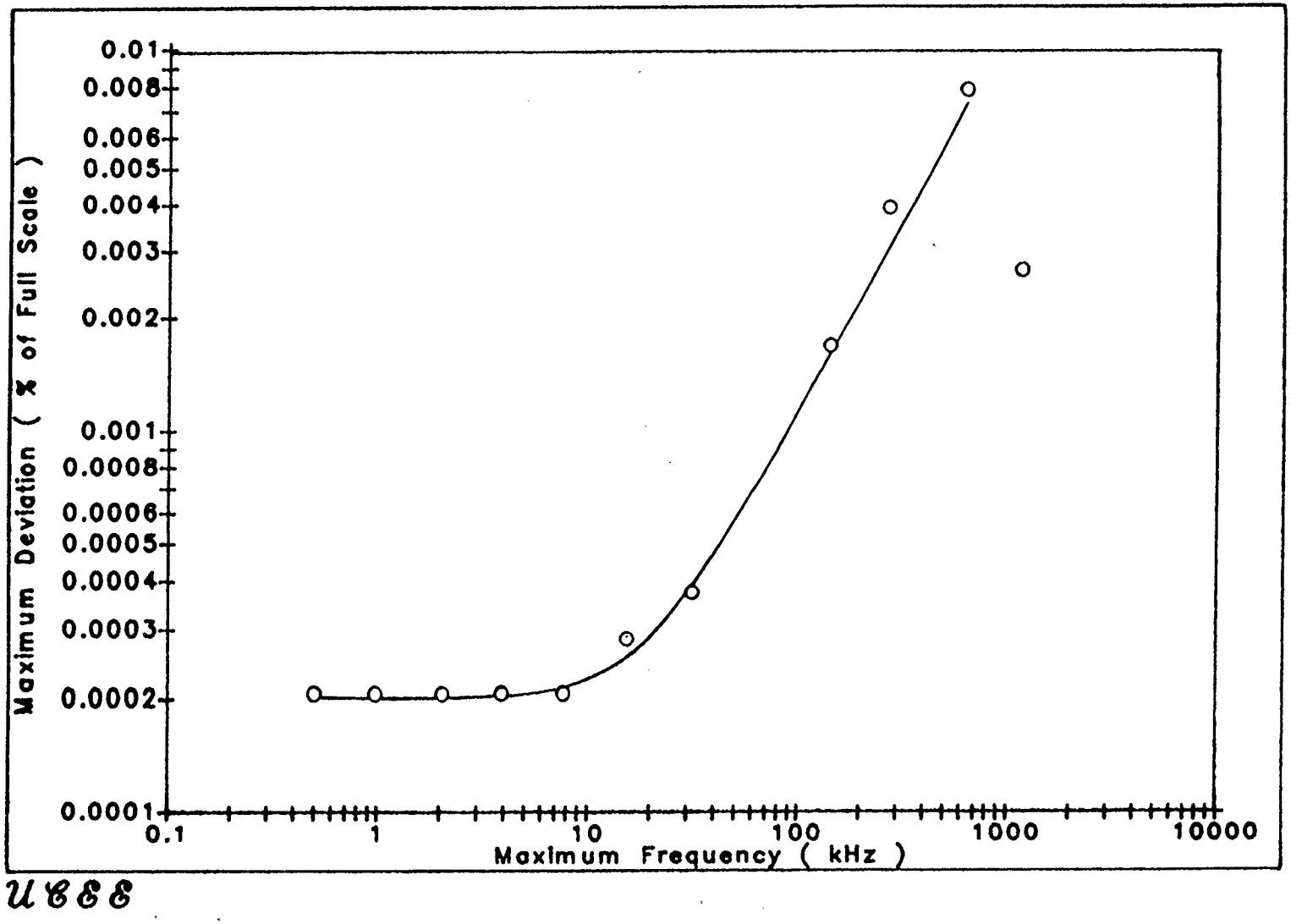


Fig.5.12 Maximum Non-Linearity as a Function of Maximum Frequency

$$0.1\ ppm/^{o}C\ \ of\ \ full\ \ scale\ \ \text{for}\ \ 0^{o}C \le temperature \le 70^{o}C.$$

(4) *High Linearity :* Maximum non-linearities (with half-scale calibration) are

$$2\ ppm\ (\ or\ 0.0002\%\ )\ of\ \ full\ \ scale\ \ \text{for}\ \ f_{\max} \le 10kHz,$$
$$0.001\%\ of\ \ full\ \ scale\ \ \text{for}\ \ f_{\max} = 100kHz,\ \text{and}$$
$$0.01\%\ of\ \ full\ \ scale\ \ \text{for}\ \ f_{\max} = 1MHz.$$

It should be noted that with the above performance characteristics, A/D converters of 19-bit accuracy, 22-bit resolution, and 0.1-ppm/^{o}C temperature coefficient can be realized easily with the synchronized VFC and the clock-controlled VFC.

CHAPTER 6

INTEGRATED VFC

6.1 Introduction

The VFCs designed in this thesis can be easily implemented with commercial components. However, in applications where the size of the circuit is critical, small-size *integrated* VFCs are preferred over those on large printed-circuit boards. Furthermore, integrated VFCs also serve as important building blocks of a variety of communication ICs. Thus, there is a need for high-performance fully integrated VFCs. This chapter outlines the major steps required to integrate a high-precision VFC system. The most important step of integrating the amplifier will be discussed in detail. The difficulties of fully integrating a high-precision system and some practical solutions will also be presented.

6.2 Requirements for an Integrated VFC System

All of the VFCs described in the previous chapters can be integrated on single chips with any analog CMOS technology. There can be two approaches to integrating the VFCs and the associated A/D conversion systems. The easier approach is to integrate the digital parts of the circuits and leave the analog parts (the operational amplifiers, the resistors, and the capacitors) as external components. The more complete approach is to integrate the amplifiers and the digital circuits together and leave

only the resistors and capacitors external. Since the second approach is a very important step to customizing these VFCs and the associated A/D converters, it will be discussed in detail in this chapter.

The block diagram of an integrated inverse-counting A/D conversion system constructed with a clock-controlled VFC with gain and linearization is shown in Fig.6.1. If the RC elements and the crystal-clock input are made external, the only critical components that affect the performance of the system are the operational amplifier and the output buffer. Although the *resolution* of the A/D converter is independent of all circuit components including the amplifier, a high-performance integrated amplifier is necessary to get a high *conversion accuracy* so that calibration can be avoided. The output buffer must be designed in a way such that t_d and r_d are minimized. This can be easily done by cascading inverter stages and making the final output transistors as large as possible. Thus, the more important step in building the VFC system is to design an integrated amplifier that satisfies the necessary performance criteria.

For an amplifier used in any of the VFC configurations, the major performance characteristics that must be considered include the common-mode input range, the common-mode rejection ratio (CMRR), the power-supply rejection ratio (PSRR), the input offset and drift, and the input bias current.

The common-mode input range of the amplifier is particularly important when the VFC is operated from a single-ended supply. Ideally, the operational amplifier in this application should have an input range of from ground to the supply rail so that low input signals can be detected. In practice, the amplifier should be able to detect inputs ranging from ground plus the offset voltage to as close to the supply voltage as

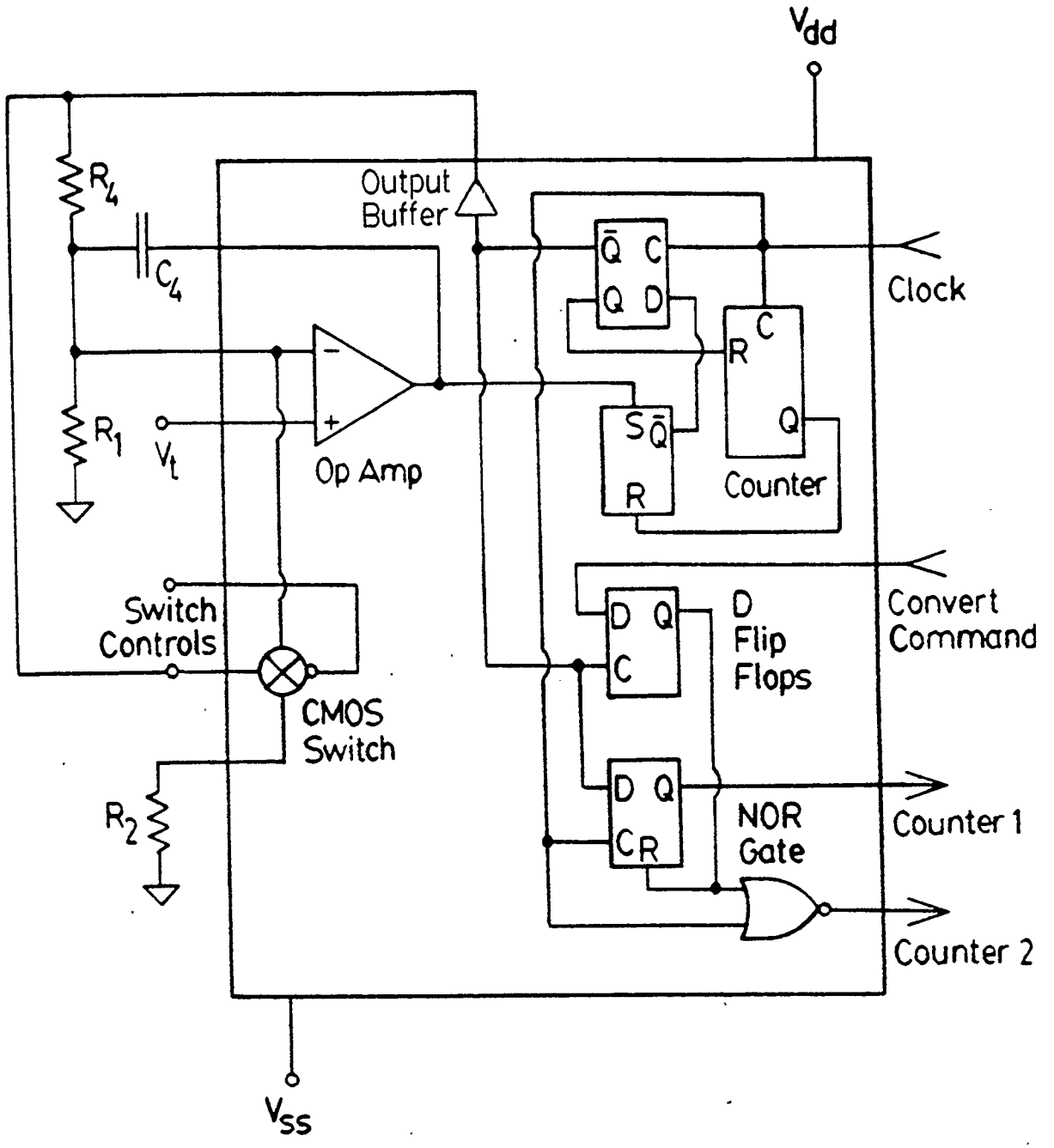


Fig.6.1 An Integrated A/D Converter Constructed with a Clock-Controlled VFC

possible. Integrated CMOS operational amplifiers with extented common-mode input range using the folded-cascode technique are well known [16,17,18]. However, such op-amp circuits extend the input range towards only one supply rail and they are often very complicated. Therefore, an op-amp circuit that provides a common-mode input range including both supply rails and is also easy to design is proposed in this chapter.

Op-amp non-idealities - offset voltage, CMRR, PSRR, and bias current - all have critical effects on the system. The input offset has two components: the systematic offset and the random offset. While systematic offset can be avoided by proper circuit design, random offset due to process variations cannot be eliminated [19]. However, more than one amplifier can be arranged together in such a way such that the overall offset of the system is significantly reduced. *Chopper Stablization* and *Commutating Auto–Zeroing* (*CAZ*) are examples of such techniques [20,21,22]. As these offset reduction techniques can be applied regardless of the op-amp input or supply voltage, they can also improve the CMRR and PSRR of the op-amp system significantly. Normally, the input bias current is not a major concern in CMOS circuits since it is usually of the order of picoamperes. However, care must be taken when applying any chopper-stablizing or auto-zeroing scheme to the integrated amplifiers; otherwise, current due to charge pumping, as observed for the *ICL* 7650, will effectively give rise to a large bias current. The provision of applying the CAZ techniques to the wide-range amplifier will be discussed at the end of this chapter.

6.3 An Experimental Integrated Amplifier with Wide Common-Mode Input Range

An operational amplifier with wide common-mode input range is useful not only in VFC circuits but also in other circuits such as voltage followers. A special op-amp design technique to extend the input range to including both supply rails is presented here. Similar to most op-amp designs, this wide-range amplifier consists of an input stage, a level-shifting stage, an output stage, and an internal frequency-compensation network. Each stage will be described in details as follows:

The Input Stage

The simplest implementation of a differential input stage is shown in Fig.6.2(a) which consists of a source-coupled pair, an active load pair, and a current source [17,19]. This configuration provides a common-mode input range from the negative supply plus the threshold voltage of the n-channel transistors to the positive supply (that is, $V_{ss}+V_{tn}$ to V_{dd}.) Although this structure suffers from poor positive power-supply rejection and low gain as compared to a cascoded structure [16], it has the advantage of simplicity, input range up to the positive supply rail, and ease of internal compensation. An alternative implementation of a simple input stage with p-channel input transistors is shown in Fig.6.2(b). Its characteristics are similar to that of the n-input structure except that its input range goes from the negative rail to the positive rail minus the threshold voltage of the p-channel transistor (V_{ss} to $V_{dd}-V_{tp}$.)

Considering the fact that each of the above input stage circuits has an input range to either supply rail, it is natural to think that if these two circuits are combined in a proper way, an input range to both supply rails should be possible. The most logical way to combine them is to tie their respective positive and negative inputs together as

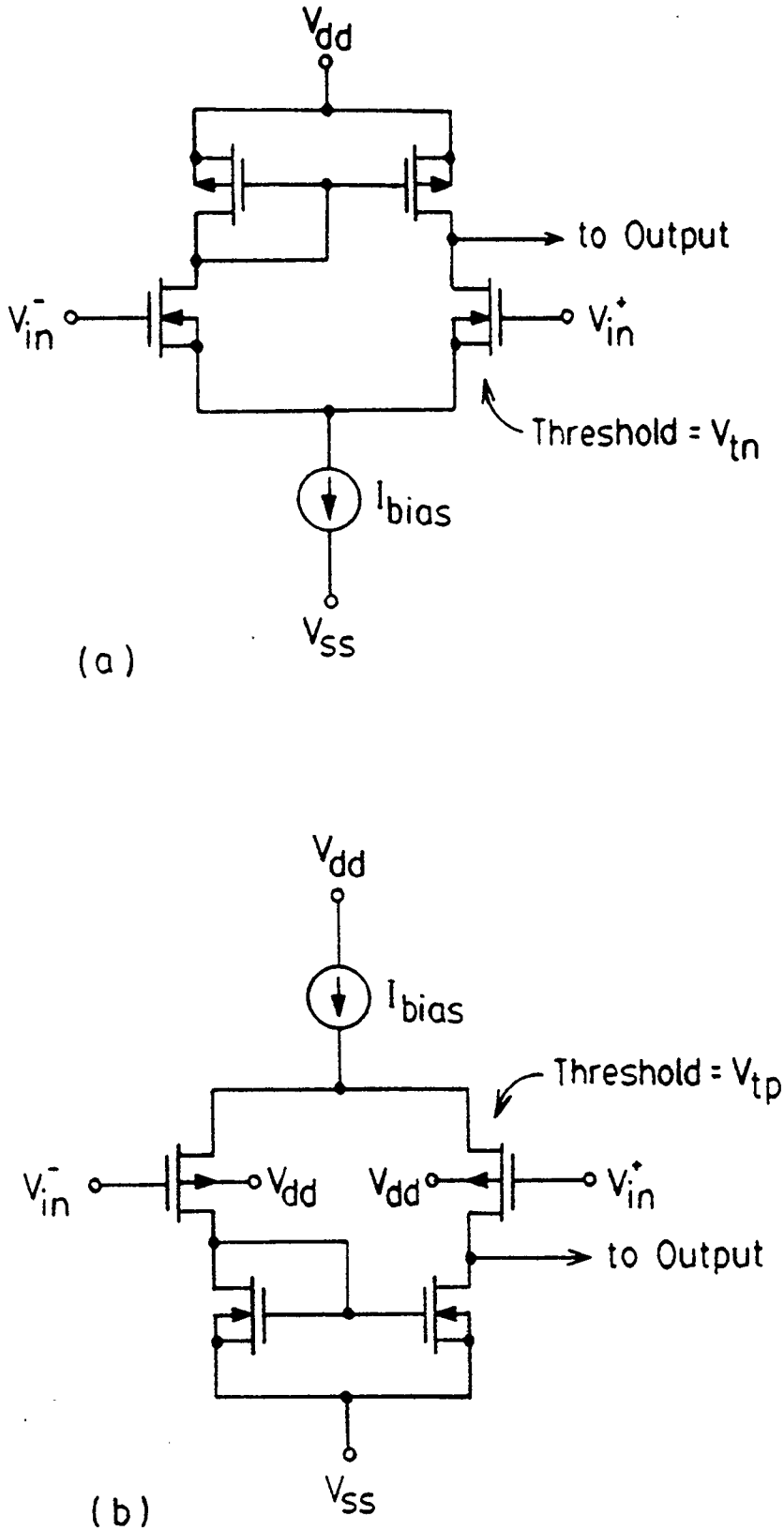


Fig.6.2 Simple Differential Input Stages with (a) N-channel and (b) P-channel Input Transistors

shown in Fig.6.3. Now if the common-mode input V_{cm} is lower than $V_{ss}+V_{tn}$, V_1 will saturate at one diode drop (of M_4) from V_{dd}; however, V_2 will be able to track the input. Similarly, if the common-mode input is higher than $V_{dd}-V_{tp}$, although V_2 will saturate at one diode drop (of M_{10}) above V_{ss}, V_1 will still be able to track the input. Therefore, the objective of the next stage will be to manipulate V_1 and V_2 to get a single-ended voltage that will vary between $V_{ss}+V_{tn}$ and $V_{dd}-V_{tp}$ in order to track a full-range common-mode input. This is done by the level-shifting stage.

The Level-Shifting Stage

The level-shifting network is shown in Fig.6.4, in which M_{16} and M_{15} track V_1 and V_2 respectively and their drains drive M_{18} and M_{19} respectively. In this way, when V_{cm} is between V_{ss} and $V_{ss}+V_{tn}$, M_{16} is cut off, M_{18} is turned heavily on, and M_{19} is able to track V_2. Similarly, when V_{cm} is between $V_{dd}-V_{tp}$ and V_{dd}, M_{15} is cut off, M_{19} is turned on, and M_{18} is able to track V_1. Now, since V_5 does not go beyond one threshold voltage to either supply, it can be used to drive a simple source-follower output stage with full output swing.

The Output Stage

The design of an amplifier output stage varies with load requirements. In applications where the output buffer is required to sink or source no more than the output bias current (most part of the quiescent operating current), a simple class A output as shown in Fig.6.5 can be used [19]. M_{21} is biased and sized to provide the necessary maximum current sink. M_{20}, on the other hand, must be biased and sized to give the

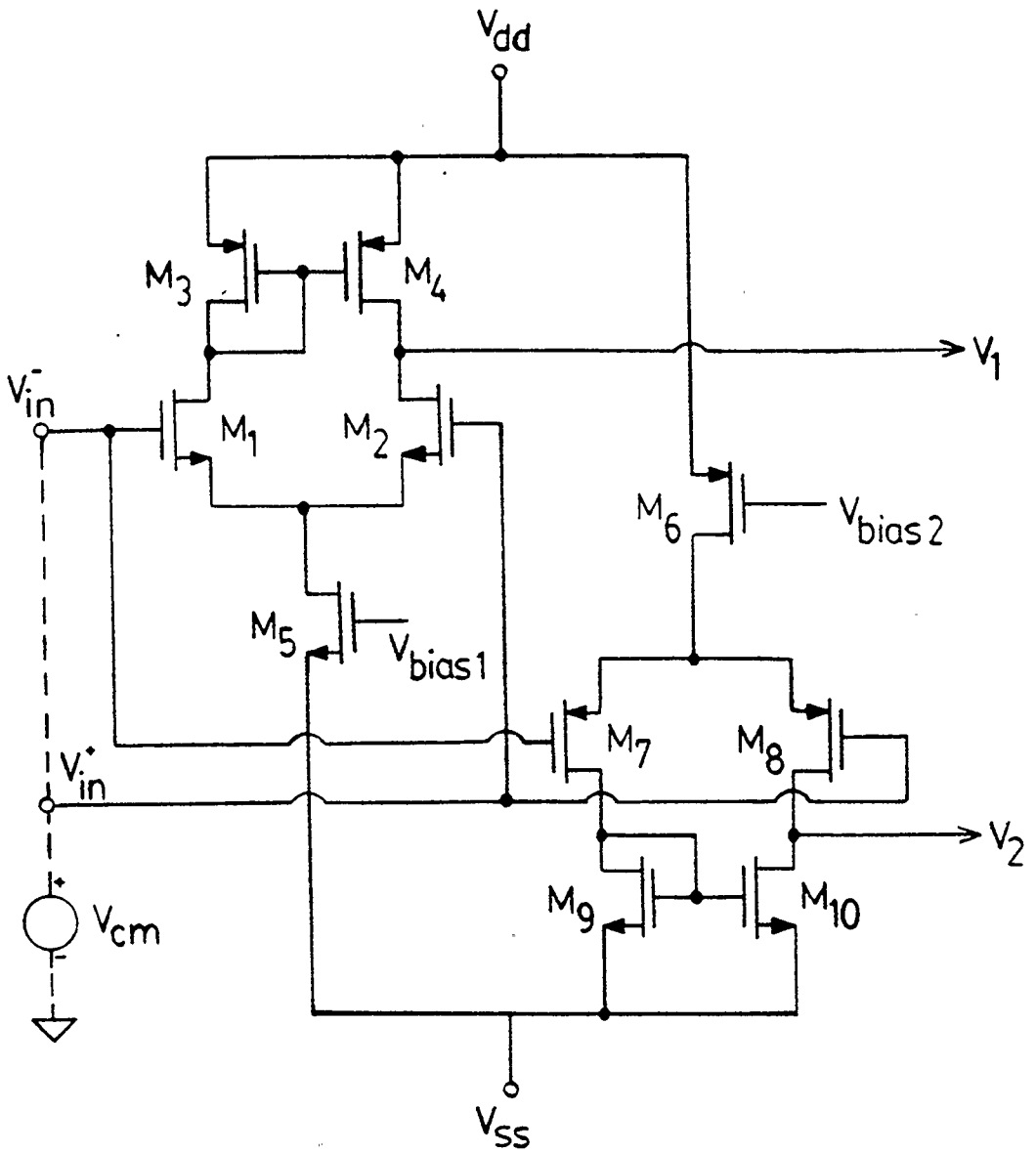


Fig.6.3 The Complementary Input Stages

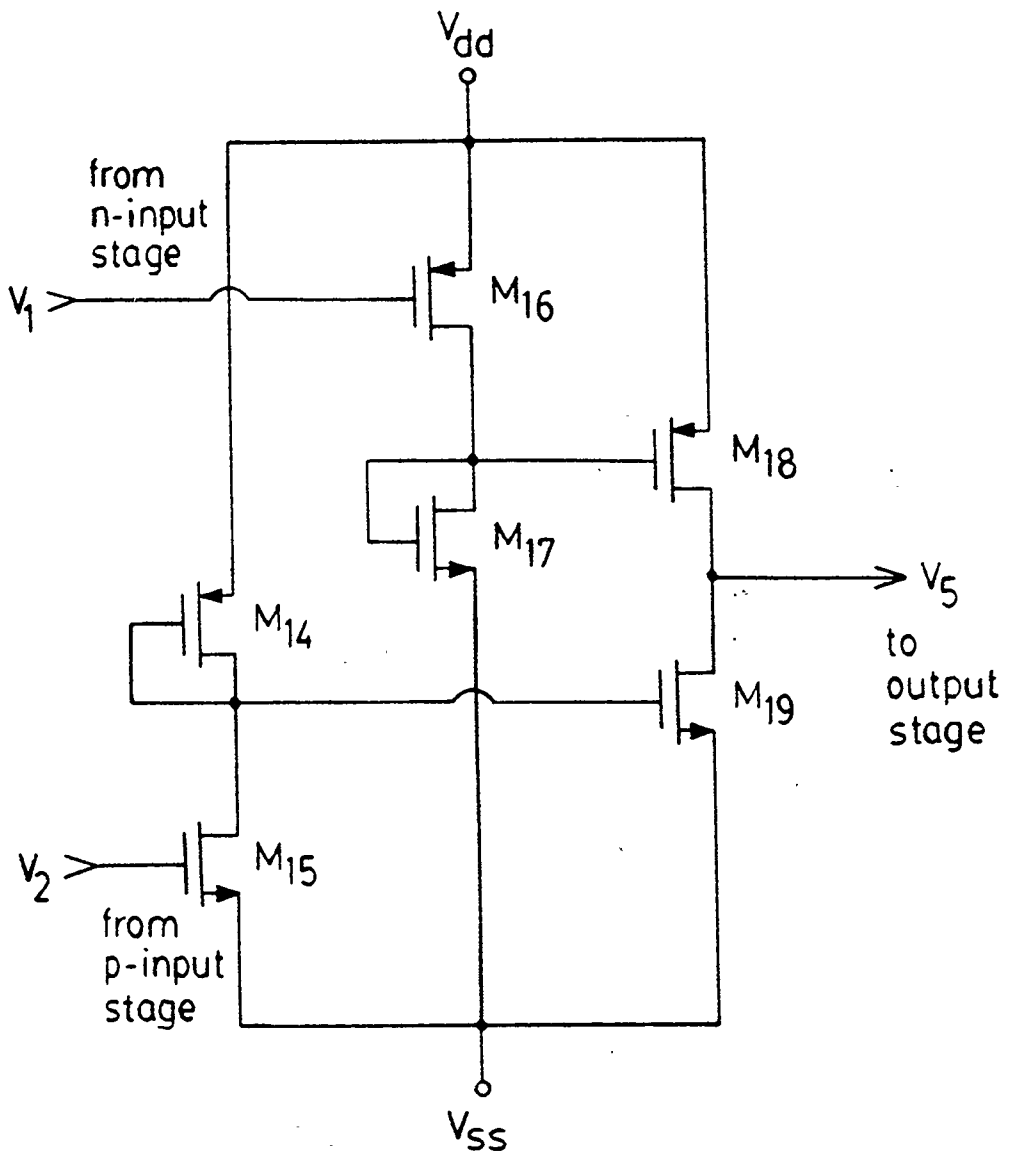


Fig.6.4 The Level-Shifting Stage

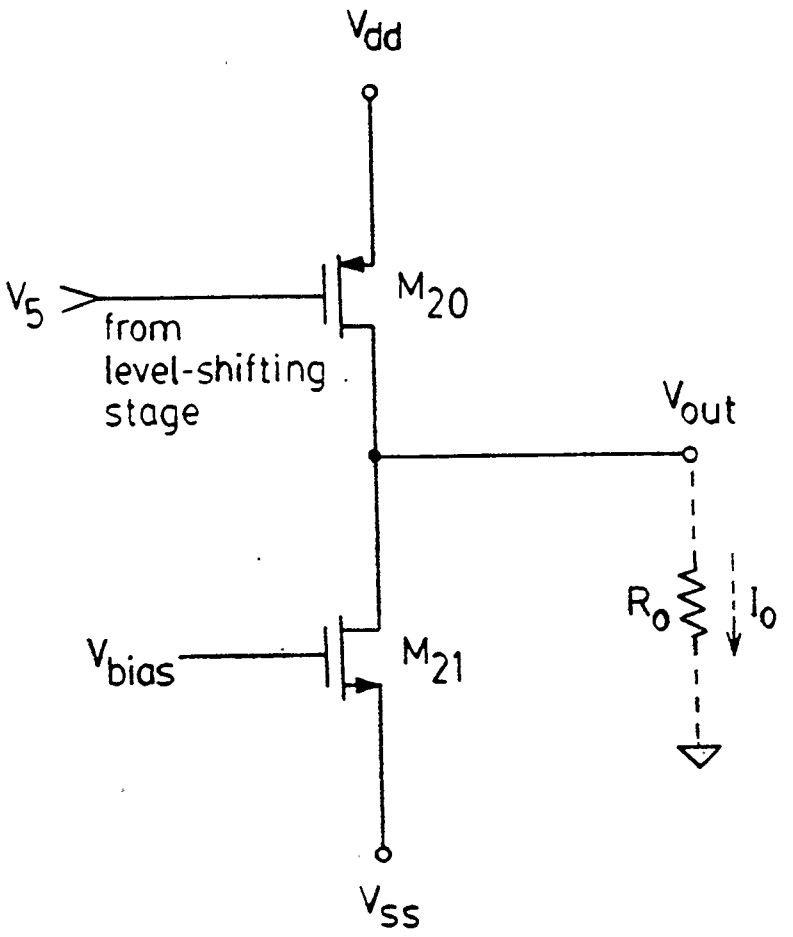


Fig.6.5 The Output Stage

maximum source current as well as the bias current drawn by M_{21}.

The Compensation Network

Frequency compensation in a conventional two-stage operational amplifier is normally done by connecting a pole-splitting capacitor between the two high-impedance nodes of the two stages [17,19]. A similar idea can be used for this three-stage amplifier. The compensation network is shown in Fig.6.6 together with the complete op-amp circuit diagram. In this circuit, capacitor C_1 serves as the pole-splitting capacitor between the n-input stage and the output stage; C_2 provides phase compensation for the p-input stage; C_3 gives the extra pole that compensates the zero appearing near the unity-gain frequency; and finally, R_z avoids any high-frequency feed-through between the input and the output stages.

The Complete Circuit

A complete circuit diagram for the amplifier is shown in Fig.6.6. Transistors M_1 to M_{10} constitute the complementary input stages, M_{11} to M_{13} form a simple bias chain, M_{14} to M_{19} perform the level-shifting function, M_{20} and M_{21} form a class A output stage, and the capacitors and resistor make up the compensation network.

This circuit was analyzed by level-two SPICE with Northern Telecom CMOS-1B (5 micron) process parameters [23]. The simulated characteristics are listed in Table I and are compared with the specified characteristics of the *ICL*7612 amplifier [21] which also has a relatively wide common-mode input range. The simulated open-loop frequency response is also shown in Fig.6.7.

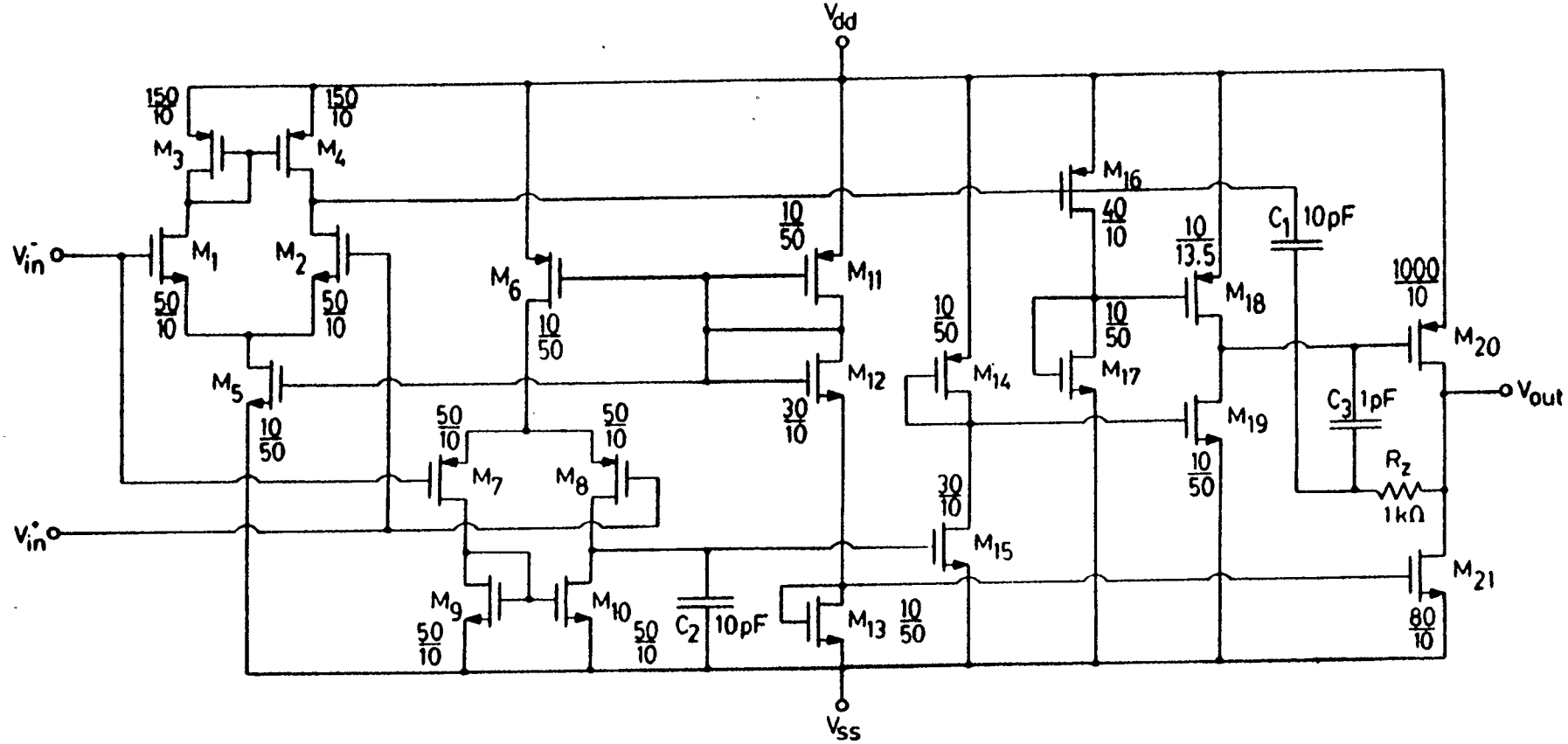


Fig.6.6 The Complete Circuit with Compensation

Table I Comparison of Performances between the Integrated Op Amp and the ICL7612 Op Amp

ELECTRICAL CHARACTERISTICS (Vsupp=±5.0V, Temp.=25°C)

PARAMETER	SPICE-SIMULATED	ICL7612	UNIT
Common-Mode Input Range	± 5.0	- 5.1 + 5.3	V
Output Swing	- 4.85 + 4.99	± 4.8	V
Offset Voltage	0.008	5	mV
Supply Current	0.58	0.1	mA
DC Gain	80	80	dB
Unity-Gain Bandwidth	2	0.48	MHz
Phase Margin	35	60	deg.
Slew Rate	3.5	0.16	V/uS
Common-Mode Rejection Ratio	87	91	dB
Power-Supply Rejection Ratio	74	86	dB

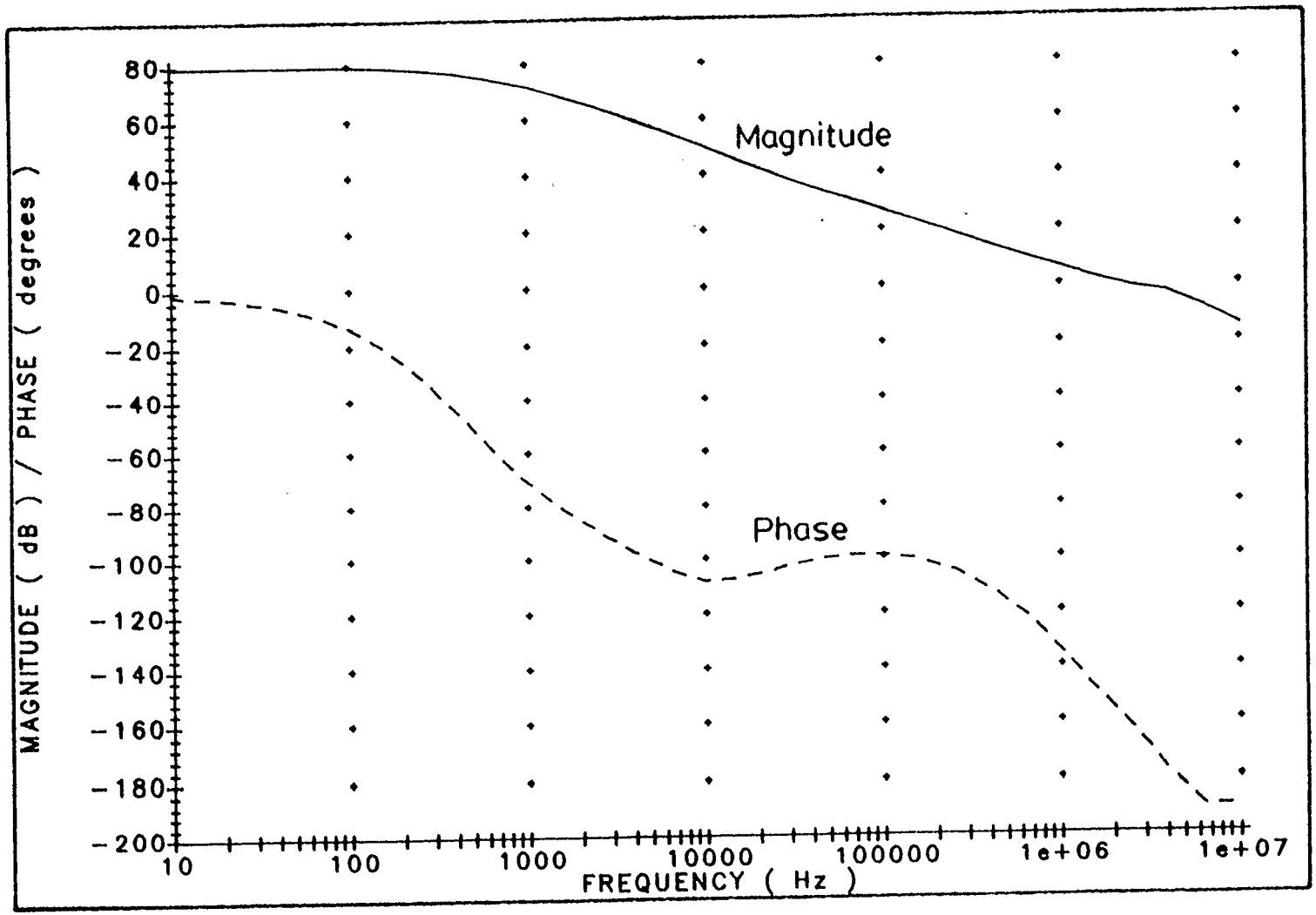


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Fig.6.7 Simulated Open-loop Frequency Response

6.4 Test Results

The experimental wide-input-range amplifier together with the basic and improved RC-controlled VFC were fabricated through the Canadian Micro-electronics Corporation with the Northern Telecom CMOS-1B process. The integrated circuits were then tested and the results for the amplifier are shown in Table II in comparison with the simulated values. Since the amplifier is the most critical component in both the basic and the improved VFC structures, these VFCs are tested only functionally and their performance characteristics are directly related to the op-amp performance.

Some measured parameters agree with simulated results but some do not. As shown in Table II, a common-mode input range up to both supply rails is indeed achieved. Moreover, the output swing, supply current, dc gain, slew rate, and unity-gain bandwidth all agree with simulated values. On the other hand, the measured input offset voltage, CMRR, and PSRR are much worse than their simulated values. These discrepancies are due to either transistor mismatching during fabrication or inaccurate process parameter values used during simulation or because of both reasons. In order for this amplifier to be useful in the VFC circuits, the offset and CMRR must be improved. (The technique for improving these parameters will be discussed in the next section.)

Finally, the frequency response with a gain of ten is shown in Fig.6.8. It can been seen that the phase margin is about zero degrees, which will cause the amplifier to oscillate in the open-loop configuration. This instability, however, can be overcome easily when the amplifier is used in the VFC circuits: a stabilizing capacitor can be

Table II Comparison of Simulated and Measured Characteristics for the Integrated Op Amp

ELECTRICAL CHARACTERISTICS (Vsupp=±5.0V, Temp.=25°C)

PARAMETER	SPICE-SIMULATED	MEASURED	UNIT
Common-Mode Input Range	± 5.0	± 5.0	V
Output Swing	- 4.85 + 4.99	- 4.90 + 4.92	V
Offset Voltage	0.008	4	mV
Supply Current	0.58	0.6	mA
DC Gain	80	80	dB
Unity-Gain Bandwidth	2	2	MHz
Phase Margin	35	0	deg.
Slew Rate	3.5	2.5	V/uS
Common-Mode Rejection Ratio	87	68	dB
Power-Supply Rejection Ratio	74	64	dB

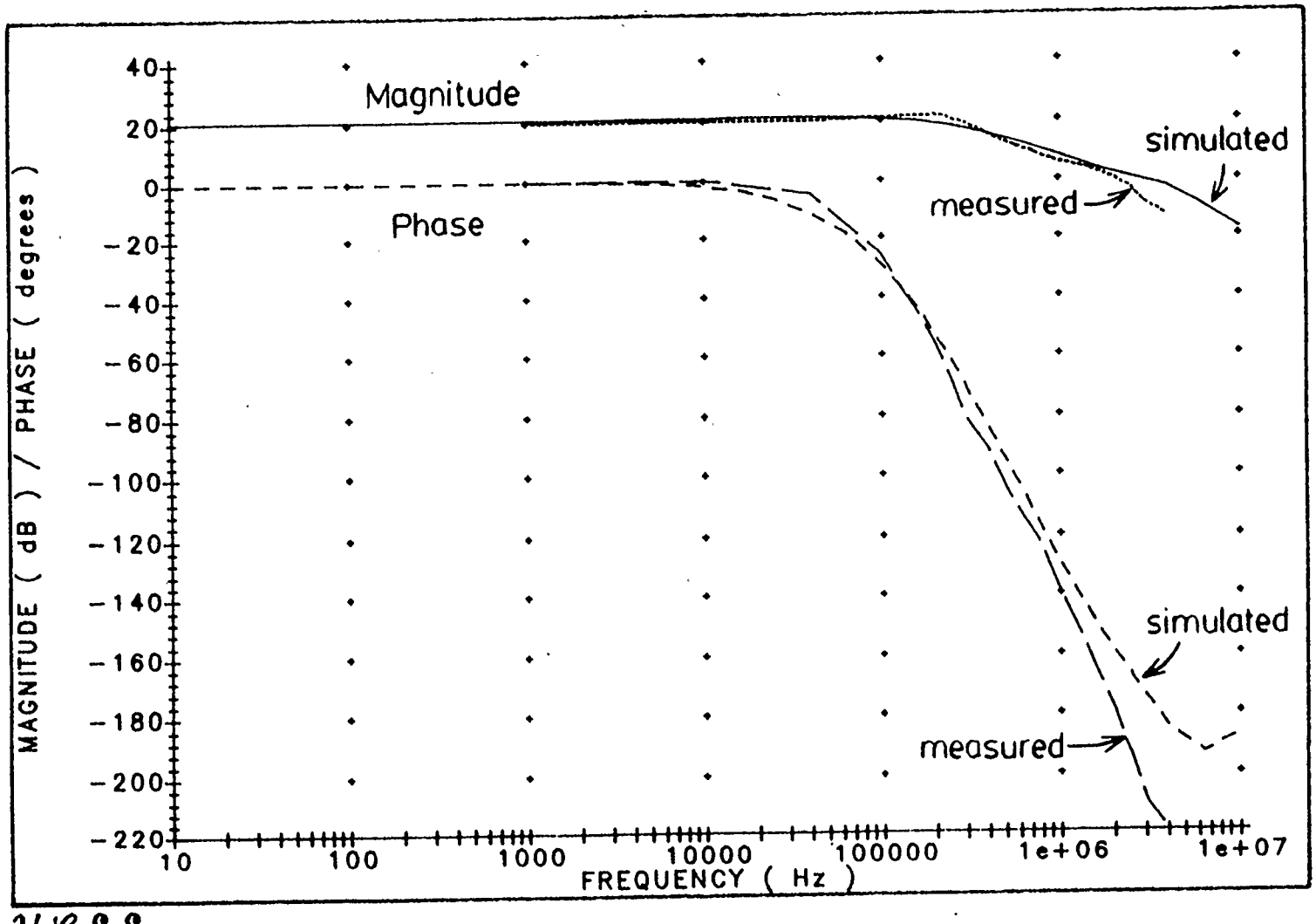

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Fig.6.8 Frequency Responses with Gain of 10

connected to the inverting terminal of the amplifier without affecting the circuit operation.

6.5 A Recommended Integrated VFC System

A useful op-amp design to be used for integrating the VFCs has been proposed in this chapter. It is apparent that in order to successfully integrate a high-performance VFC system, there is a need to reduce the offset and increase the CMRR and PSRR of the proposed amplifier. The easiest way to achieve this is to use the *Commutating Auto-Zeroing* (CAZ) scheme [21,22].

In a CAZ scheme, two amplifiers are switched between two operating modes by a two-phase non-overlapping clock, as shown in Fig.6.9. When *op-amp* 1 is in *mode A*, *op-amp* 2 is in *mode B* and vice versa. When either amplifier is in *mode A*, the input offset of the amplifier is stored in the capacitor and this offset value is subtracted from the non-inverting terminal when the amplifier is switched to *mode B*. Thus, normal op-amp operation is maintained since the amplifiers are switched into the normal operating mode alternately.

Two limitations of the CAZ scheme will become critical when it is applied to the VFCs:

(1) If the normal output V_{out} of the op-amp system is different from the zero-reference V_z, each amplifier has to slew between V_{out} and V_z when it switches from *mode A* to *mode B*. Hence, due to the finite slew rate of the amplifiers, transient voltage spikes that go between V_{out} and V_z will appear at the output of

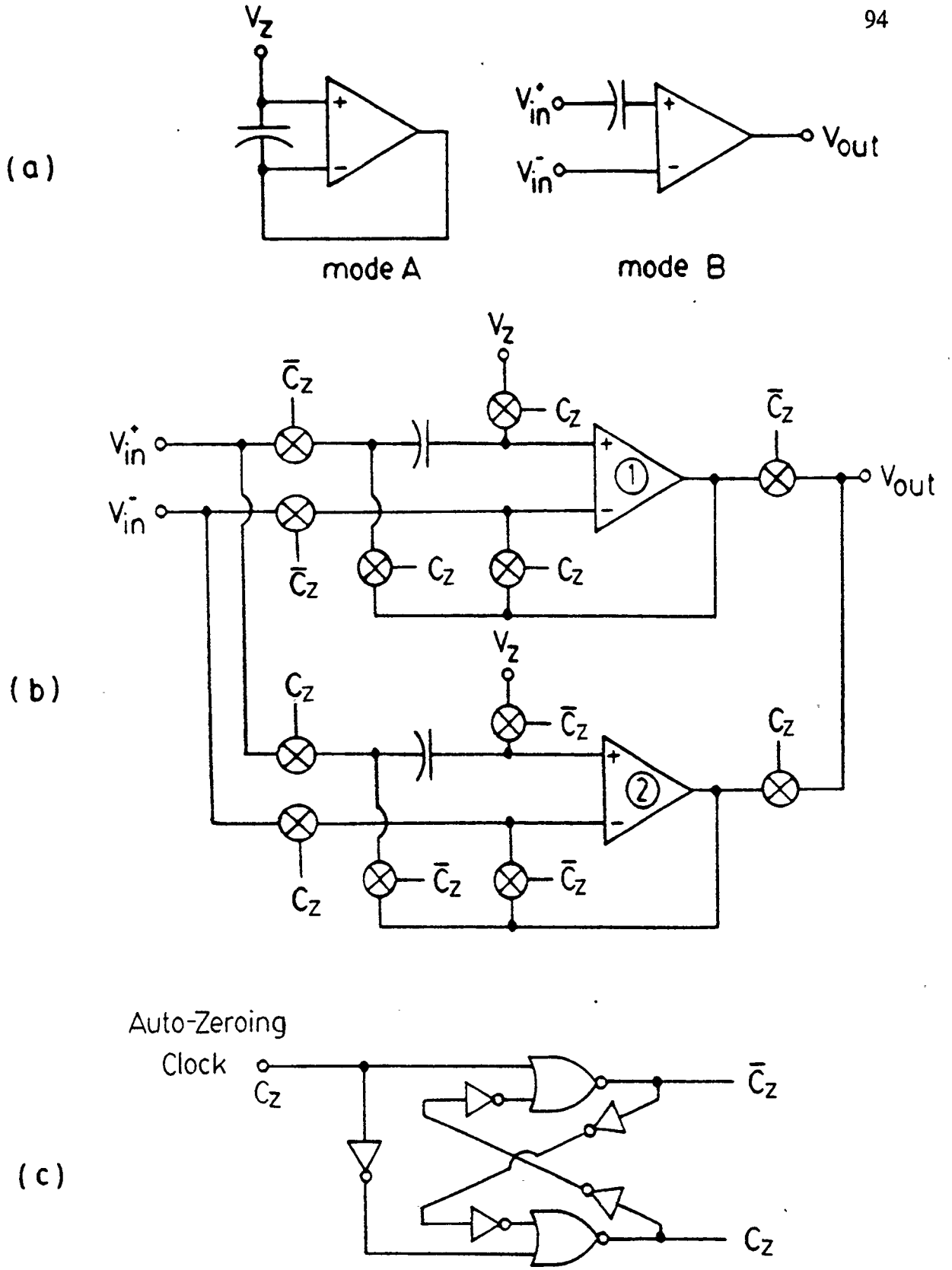


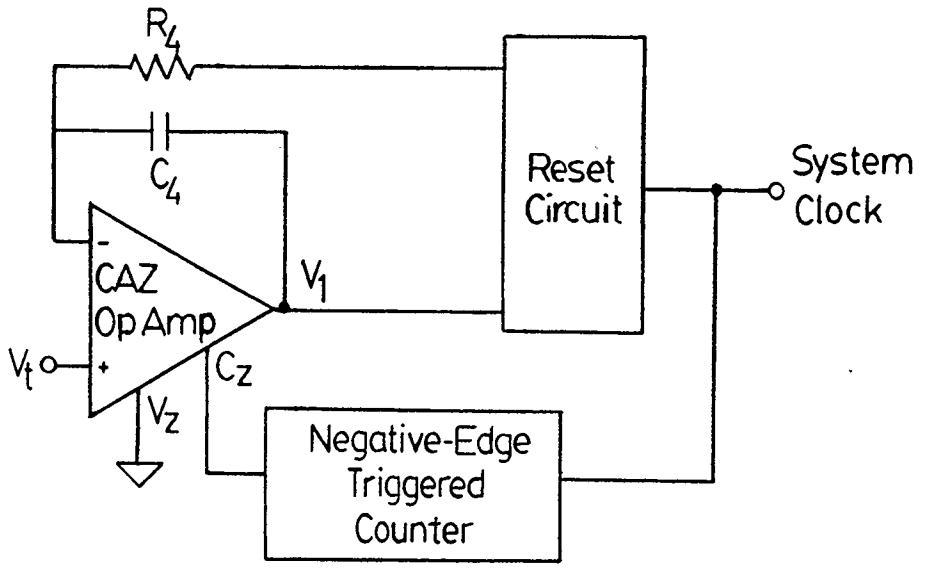
Fig.6.9 Commutating Auto-Zeroing Scheme: (a) The Two Modes, (b) Circuit Diagram, and (c) Generation of the Two-phase Non-overlapping Clock

the system [21,22]. V_z is normally set to V_{in}^+ in the CAZ scheme. However, in order to avoid accidental switching caused by a transient spike; V_z must be set to a level below the threshold of a CMOS NOR-gate in the VFC circuits. As a result, transient noise at the op-amp output is inevitable and its effect must be avoided by proper circuit design.

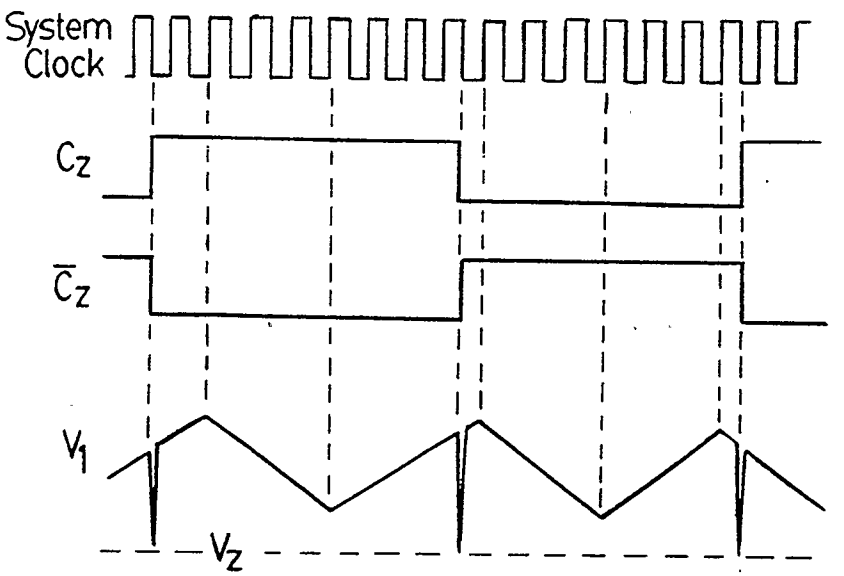
(2) Since the op-amp inputs (V_{in}^+ and V_{in}^-) are connected by switches, a *charge-pumping* current similar to that observed for the *ICL*7650 in Chapter 5 will flow between the two terminals. This current, however, can be reduced to a negligible level by decreasing the auto-zeroing frequency, for example, to 10Hz.

A system that can take care of both problems mentioned above can be constructed as shown in Fig.6.10. The first problem is avoided by using a negative-edge triggered counting circuit (similar to that of the *MC* 14040) to obtain an auto-zeroing clock which is synchronized with the falling edges of the system clock. In this way, transient voltage spikes due to auto-zeroing will never occur at the critical circuit switching points, as illustrated in Fig.6.10(b). The second problem of charge-pumping can be minimized by using a large number of frequency divisions to obtain the auto-zeroing clock from the system clock. As long as a few auto-zeroing cycles are maintained within the conversion period, the CAZ scheme will provide the necessary offset reduction without giving rise to significant bias-current problems.

Consequently, a high-performance integrated VFC system can be realized by the proposed wide-range amplifier with the CAZ scheme and the circuit configuration of Fig.6.10. This integrated VFC system will provide high resolution, high accuracy, and



(a)



(b)

Fig.6.10 An Integrated VFC Constructed with CAZ Op Amp:
(a) Circuit Arrangement
(b) Voltage Waveforms

in particular a useful full-scale input range which has never been achieved by other commercial models.

CHAPTER 7

CONCLUSIONS AND FUTURE CONSIDERATIONS

In this thesis, a number of charge-balance voltage-to-frequency converters were designed and four basic members in this VFC family were discussed in details. They are summarized as follows:

(1) *The basic RC-controlled VFC* produces an output pulse train which width-to-period ratio is proportional to the input voltage and independent of circuit component values. It can also be modified to provide voltage gain, linearization, and dual-supply operations.

(2) *The Improved RC-controlled VFC* has all the useful characteristics of the basic RC-controlled VFC. In addition, it provides instantaneous frequency conversion with less than 0.05% of full scale error.

(3) *The synchronized VFC* is the clock-synchronized version of the basic RC-controlled VFC. Besides all the functions of the RC-controlled VFC, this synchronized version can be applied for inverse-counting analog-to-digital conversion with resolution in the order of 0.1 ppm of full scale and maximum nonlinearity of 2 ppm of full scale.

(4) *The clock-controlled VFC* can provide all the functions and high performance of the synchronized VFC with the additional features of single-counter inverse counting, instantaneous frequency conversion, and frequency-to-voltage

conversion.

The synchronized and clock-controlled VFCs have been implemented with discrete components and tested. A/D conversion with 22-bit resolution, 19-bit linearity, and 0.1 ppm/^oC temperature coefficient was successfully achieved using these VFCs with proper choices of circuit parameters.

In complement with the VFCs constructed with discrete components, an integrated VFC system based on the clock-controlled VFC structure was proposed. A useful building block for analog CMOS integrated circuits - the integrated amplifier with wide common-mode input range - was also presented. Test results for the integrated amplifier proved to be encouraging. With the use of offset reduction schemes such as the commutating auto-zeroing scheme, the wide-range amplifier is suitable for integrated VFC applications.

Possible future research in this area includes the followings:

(1) Since the circuits are useful in temperature and pressure sensing, they are likely to be used in high temperature environment such as oil and gas reservoirs. Thus, the operating temperature range may be wider than the commercial range of 0^oC to 70^oC already tested. More complete temperature analysis and testing should be carried out before using these circuits in any high-temperature work.

(2) When the VFCs are applied in A/D conversion, high resolution is achieved by the inverse counting technique. It is then necessary to either perform a numerical division of two output readings or to take the reciprocal of an output reading. These numerical manipulations can be easily handled by a low cost microcon-

troller which also provides synchronization for the system and any necessary calibration [14,15]. Interfacing the VFCs with microcontrollers is therefore an important step in implementing a complete data acquisition system.

(3) A fully integrated VFC with synchronized digital outputs ready for processing was recommended in Chapter 6. It appears that, in order to realize the recommended VFC system, more effort will have to be spent on improving the stability of the amplifier and perfecting the offset reduction scheme. The work presented by Wong [22] on integrated amplifier design and offset reduction schemes serves as a good source of reference for any further research in this area.

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