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Millimeter-Wave and Sub-Terahertz Parametric Harmonic Generation

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by

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Abstract

The theory of parametric harmonic generation is described in this thesis. It is shown that for Nth-order harmonic generation the time-varying parameter (P), such as elastance (S), capacitance (C), conductance (G), or resistance (R), exhibits $N-1$ periods of a sine wave under one sinusoidal pumping cycle, which is named sinusoidal representation of pumped parameters. The maximum conversion efficiency of reactive frequency multipliers is $1/N$. The related P-V curves are described by the Chebyshev polynomials. Impulse representation of pumped parameters is also developed to represent a transient train of pulses to describe the resistive multipliers.

Several circuits are designed to demonstrate the validity of the theory and explore the parametric circuits in millimeter-wave and sub-THz bands. A frequency tripler is designed in the 28-GHz 5G band, using the topology of symmetric antiparallel pair of series varactors to achieve about 24-dB conversion loss (CL), -8-dBm maximum output power (P_{OUT}), and 18% relative bandwidth (BW). Two reconfigurable frequency multipliers (RFMs) are designed based on antiparallel nMOS-varactor pairs (APNVP) and switched-capacitor varactor (SCV) pairs. The SCV can obtain the ratio of maximum-to-minimum capacitance as high as 20, almost 10 times better than that of MOS varactors. The SCV-based RFM demonstrates much better performance than the APNVP-based RFM. A resistive tripler based on an antiparallel diode-connected nMOS transistor pair is also designed and measured in the D-band, with wide 28% BW and -16 dBm P_{OUT}. The CL can be improved by increasing the nonlinearity of the resistance by tuning the back-gate control voltage. A voltage-controlled inductor is proposed based on a transistor-controlled capacitor and demonstrated in a D-band injection-locked oscillator with a $\geq$16% tunable operating frequency range, dc power as low as 5.6 mW, and a compact 0.018-mm^2 core size.

Preface

This thesis is original, unpublished, independent work by the author, Nan Zhang.

Acknowledgements

Foremost, I would like to express my sincere gratitude and appreciations to my supervisor Dr. Leonid Belostotski, and my co-supervisor Dr. James W. Haslett. Dr. Belostotski leads me to understand the beauty of CMOS analog and RF circuit design, and helps me solve confusions in studies and researches patiently. He is always kindly supportive to me with generous help whenever I need. The talks and discussions in his offices and group meetings inspire me to explore unknowns in the electronic world. I will always benefit from his teaching and guidance in my life. Dr. Haslett has been an Academic Staff Member for 50 years. I not only respect his encyclopedic knowledge and great achievements in academia but also have been influenced by his meticulous scholarship and noble personality. His suggestions are always kind and helpful.

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For my wife Yan and my parents

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List of Abbreviations

Acronym	Definition
5G	Fifth-generation wireless
AC	Alternating current
AMOSV	Accumulation-mode MOS varactor
APDNP	Antiparallel diode-connected nMOS transistor pair
APDP	Antiparallel-diode pair
APNVP	Antiparallel nMOS varactor pair
APVP	Antiparallel varactor pair
AS-VAR	Anti-series MOS varactor
Bias T	Bias tee
BiCMOS	Bipolar CMOS
BPF	Band-pass filter
BW	Bandwidth
C	Capacitance
CAPDP	Complementary antiparallel diode pair
CCAT	Cerro Chajnantor Atacama Telescope
CL	Conversion loss
CMOS	Complementary metal oxide semiconductor
C-SCVP	Complementary SCV pair
DC	Direct current
DUT	Device under test
FET	Field-effect transistor
EM	Electromagnetic
FinFET	Fin field-effect transistor
FM	Frequency multiplier
FYST	Fred Young Submillimeter Telescope
G	Conductance
GaAs	Gallium arsenide
GaN	Gallium nitride
GSG	Ground-signal-ground
HBV	Heterostructure barrier varactor
HEB	Hot electron bolometric
HEMT	High-electron-mobility transistor
HPF	High-pass filter

Acronym	Definition
HRR	Harmonic rejection ratio
IF	Intermediate frequency
IL	Injection-locked
ILFM	Injection-locked frequency multiplier
ILO	Injection-locked oscillator
InP	Indium phosphide
IPN	Integrated phase noise
IRPP	Impulse representation of pumped parameter
LC	Inductor-capacitor
LO	Local oscillator
LPF	Low-pass filter
MEMS	Microelectromechanical systems
MIM	metal-insulator-metal
Mm-wave	Millimeter-wave
MOM	metal-oxide-metal
MOS	Metal oxide semiconductor
N	Multiplication factor
nMOS	n-channel MOS
NR	New Radio
n-VAR	n-type MOS varactor
P	Parameter
PA	Power amplifier
PAE	Power-added efficiency
PLL	Phase-locked loop
pMOS	p-channel MOS
PN	Phase noise
PPF	Polyphase filter
Q	Quality factor
QILO	Quadrature ILO
QVCO	Quadrature VCO
R	Resistance
RF	Radio frequency
RFM	Reconfigurable frequency multiplier
S	Elastance
SAPSV	Symmetric antiparallel pair of series varactors

Acronym	Definition
SB-CAPDP	Self-biased CAPDP
SBD	Schottky barrier diode
SCV	Switched-capacitor varactor
SCVP	SCV pair
SiGe	Silicon germanium
SIS	Superconducting-insulating-superconducting
SOI	Silicon on insulator
S-QBV	Symmetrical quantum-barrier varactor
SRPP	Sinusoidal representation of pumped parameter
SW	Switch
TCC	Transistor-controlled capacitor
THz	Terahertz
TL	Transmission line
TR	Tuning range
VCI	Voltage-controlled inductor
VCO	Voltage-controlled oscillator
VDD	Supply voltage
WR	Rectangular waveguide

Chapter 1

Introduction

People have observed parametric phenomena for a long time in history. For example, a child playing on a swing is a typical pumped mechanical parametric system [1]. In the natural world, all systems can be categorized into four kinds ideally: linear time-invariant, nonlinear time-invariant, linear time-variant, and nonlinear time-variant, of which the circuits called "parametric circuits" are theoretically linear and time-varying [2]. However, since the time-varying property is usually realized by the nonlinear properties of the circuit components, the terminology nonlinear is quite often used in the field of parametric circuits, e.g., the nonlinear capacitance. In the electronic field, a number of essential properties of nonlinear energy-storing systems such as the "negative-resistance effect" for parametric amplifiers were described by early pioneers such as Faraday in 1831 and Lord Rayleigh in 1883, respectively, and an electro-mechanical nonlinear capacitance was described by Hartley in 1936, which was similar to the modern varying-capacitance parametric circuits [3]. With more and more research interests in parametric circuits during and after World War II, Manley and Rowe published the lossless theory of the power-frequency distribution of a reactive system, which was known as Manley-Rowe relations [4]. Manley-Rowe relations are the fundamental theory representing the conservation of energy behind the parametric phenomena in our natural world, not only including the electronic field, but also nonlinear mechanics, dynamics, radiophysics, and optics [2]. As an example in the optical field, an optical parametric amplifier using silicon nanophotonic waveguides is demonstrated to have a 25.4-dB gain for signals around the pump wavelength of 2200 nm [about 136 terahertz (THz)] [5].

1.1 Motivations

1.1.1 Motivations to Fill the THz Gap

The THz band is usually defined from 0.3 to 3 THz, or from 100 μm to 1 mm in terms of the wavelength, and is known as the submillimeter-wave band. The THz frequency range has occupied a technological gap, for which neither room-temperature photonics nor conventional electronics is well suited [6]. The photonic devices, which use population inversion, are difficult to operate in this band due to the thermal energy kT_{A}, where k is Boltzmann's constant and T_{A} is the absolute temperature, being equal to the 6-THz photon energy [6]. Therefore, conventional photonic devices to be implemented at a lower frequency within the THz band need cryogenic cooling, e.g., a quantum-cascade laser can emit at 3.22 THz at 200 Kelvins (K) [7]. Conventional transistor-based electronic devices operate well at tens of gigahertz (GHz), but it becomes more and more difficult for such devices to provide a sufficient gain even in the lower portion of the THz band below 1 THz. GaN high-electron-mobility transistors (HEMTs) are reported with a power-gain cutoff frequency (f_{max}) at 444 GHz in [8], whereas the f_{max} of a 22-nm fully-depleted silicon-on-insulator (SOI) complementary metal-oxide-semiconductor (CMOS) process is limited to 320 GHz as reported recently in [9].

Although these difficulties exist in processing signals in the THz band, this band has drawn great efforts to improve the detection, generation, and processing of THz signals for a variety of applications. The THz imaging of concealed subjects and opaque materials is of enormous interests, for security screening and medical scanning due to the finer spatial resolution compared with the millimeter-wave (mm-wave) imaging, and safer non-ionizing nature compared with X-rays [10]. Another major interest is in the fields of geophysics and astronomy for the detection of terrestrial and extraterrestrial signals in the THz band, e.g., through the new generation of telescopes for submillimeter astronomical observations, such as the Fred Young Submillimeter Telescope (FYST), previously known as the Cerro

Chajnantor Atacama Telescope (CCAT). Although absorption in the THz band from gases, especially water vapor attenuation, is present, there are windows left in the spectrum to allow the observations of the submillimeter signals, which carry crucial and unique information from the distant outer space, to help astrophysicists explore the secrets of the universe, such as the origins and formations of the planets, the stars, the interstellar materials, and the galaxies [11].

To fill the THz gap and push the frontier of electronics to higher and higher frequencies, a lot of work has been done in the THz electronic field. The detection methods of THz signals can be categorized into two major kinds: incoherent detection and coherent detection. The incoherent detection directly detects the amplitude of the input signal and converts the ac signal to a dc voltage or a low-frequency varying signal through a device, typically a diode in CMOS, of which the cutoff frequency can reach 1 to 2 THz [12]. Active THz imaging has been proved at 860 GHz with Schottky barrier diodes (SBDs) in CMOS [10]. The incoherent detection does not need a local oscillator (LO), but the phase information cannot be preserved in the process, and the noise performance is limited [12].

For coherent detection, a heterodyne receiver with a local oscillator (LO) is expected to have an improved sensitivity with both the amplitude and phase of the input signal detected [12]. Antiparallel-diode pairs (APDPs) have been used in the lower edge of the THz band, such as a 210-to-305-GHz receiver with diode-connected MOS field-effect transistors (FETs) for a 20-GHz intermediate frequency (IF) output with a $\times 2$ sub-harmonic LO [13], and a 301-to-314-GHz APDP mixer with Fermi-level managed barrier diodes and a $\times 2$ sub-harmonic LO in [14]. [14] has the largest conversion gain of -23dB with a 30-μW LO, whereas [13] provides a 2-to-7-dB conversion gain together with the IF amplifier, though the dc power consumption and the conversion gain of the mixing stage were not reported. For coherent detection at a higher frequency beyond 1 THz, Schottky diodes, superconducting hot electron bolometric (HEB) devices, and superconducting-insulating-superconducting (SIS) junctions are considered as candidates for the mixer; however, the

Schottky diode mixers need a high LO power and suffer from a low noise performance, and HEB and SIS mixers need cooling systems for a cryogenic operation and are expensive to fabricate [15]. Therefore, new devices and topologies are needed for the rapid developing THz electronics.

FYST (the former CCAT), which operates in the spectrum between 200 to 1600 μm (0.2 to 1.5 THz) as described in [11], has broken ground near the summit of Cerro Chajnantor, Chile, in November 2020. The research project described in this thesis was originally inspired by the requirement of the CCAT as a potential alternative to the cryogenic receiver circuits, but it is not an official part of the CCAT [16]. With the research of the LO generation for the mm-wave and sub-THz parametric circuits, this work focuses on the theory and the demonstration of new types of parametric frequency multipliers, as well as the new components of varactors and variable inductors for high-frequency applications in CMOS.

As demonstrated in the varactor-pair-based 0.7-THz parametric quintupler in [17] and the 1.4-THz parametric multiplier chain in [18], the parametric circuits with varactors and varistors are seen as a candidate full of potential for the LO generation of the future THz directly and sub-harmonically pumped heterodyne receivers at room temperature, for the THz coherent detection and spectroscopy. The theory and the methods of the analysis of the mm-wave and sub-THz parametric circuits presented in this thesis possess the potential to be used in the developments of the new parametric amplifiers and frequency converters in the THz band. With the goals of building the theoretical foundations of high-frequency parametric multipliers, and demonstrating the potential of mm-wave and sub-THz parametric circuits and components, this research on parametric harmonic generation provides an attempt to explore the frontier of THz electronics and fill the THz gap in this exciting frequency regime.

1.1.2 Background of Parametric Electronics

Along with the publication of Manley-Rowe relations in 1956, parametric circuits drew tremendous interests in the 1950s and 1960s, as parametric amplifiers, frequency converters, frequency multipliers (FMs), and dividers [19]. Although the terminology "parametric" was historically used for varying reactive parameters (*P*s), i.e. inductance (L) and capacitance (C), resistive parameters, i.e. varying resistance (R) or conductance (G), can be also utilized for the passive time-varying circuits, thereby they can be considered as a special kind of lossy parametric circuits [20]. While the passive parametric circuits do not consume dc power for themselves, they can provide gain in parametric amplifiers and conversion gain in frequency converters. Varactors and varistors in parametric circuits have high cutoff frequencies, which are able to operate at millimeter-wave (mm-wave) and higher frequencies, such as the sub-THz and THz bands. The developments of diode varactors enabled the implementations of practical parametric circuits with varying capacitance in the 1950s [19]. The advantages of parametric circuits showed potential as a passive solution to wireless transceivers at high frequencies. However, the parametric circuits were replaced by active circuits in the 1970s, and the research of reactive parametric circuits was almost silent for 30 years, except for some work in the fields of some nonlinear passive circuits such as passive multipliers [21].

Although the parametric circuits seemingly vanished in the era of integrated circuits, the trend was reversed in the 2000s dramatically. The parametric circuits experienced a revival with research interests increasing rapidly since then. A number of integrated parametric circuits emerged in the CMOS technology, operating in the radio frequency (RF) and mm-wave bands, such as frequency downconverters [22, 23], frequency upconverters [24], parametric oscillators [25], filters [26], and amplifiers [27, 28]. Resistive and reactive parametric multipliers are utilized in frequency bands up to sub-THz and THz [17, 18, 29–36]. Microwave parametric amplifiers with Josephson junctions are also developed based on the parametric effect of nonlinear inductance for coherent detection of photons and readout of

superconducting quantum bits [37, 38].

The following questions would be naturally raised: Why were parametric circuits almost totally replaced by active circuits in the 1970s? Why did the revival happen with the developments of RF and mm-wave circuits in CMOS? The answers are from the very special natures of the parametric circuits.

First, the operation of parametric circuits depends on a strong driving force (voltage or current) called "pumping". Although the parametric circuits themselves consume no dc power, the pumping needs to be generated at a high frequency with a strong RF power, which consumes a considerable amount of dc power. The parametric "gain" is a result of the redistribution of ac power at different frequencies based on Manley-Rowe relations; as such it does not violate the law of energy conservation, but is achieved at a price of high pumping power and the associated dc power consumption. With strong pumping and a limited output power, the conversion loss (CL) is usually large for on-chip passive frequency multipliers. The optimization of CL under a high-power pumping as well as to obtain a high output power are major targets of a parametric multiplier design. And, the strong pumping may cause strong fundamental leakage at the output port, and as a result, adequate filtering is necessary or a must.

Second, to have a high efficiency of the parametric circuits, special circuit terminations, called "idler" circuits, are necessary for many parametric circuits. While the idlers are non-input or non-output signals in the parametric circuits, they play an important role in the operation of parametric circuits by tuning the circuits to have signal gain or loss [19]. Idler circuits add costs in terms of design complexity and chip area. Since the circuit performance is sensitive to the idlers, the idlers need to be tunable in a wide range of frequency and impedance, or the circuit performance would be much limited and degraded.

Third, reactive parametric circuits are based on the nonlinearity of the reactive device, e.g., the varactors. The modern varactors in CMOS technologies are MOS varactors, which have a monotonic C-V curve with limited ratio of maximum to minimum capacitance. The

small ratio represents a limited nonlinearity of the device, and therefore limits the high-frequency performance significantly. Due to the nonlinear property, the gain or CL is also very sensitive to the input power level. For example, in the operating range, CL of the passive FM can change by 10 dB when the input level is increased by 10 dB such as in [32].

Fourth, since the impedance of the varying capacitance is directly dependent on the frequency, and the operation of parametric circuits depends on the filtering of unnecessary frequency harmonics, the bandwidths (BWs) of the reactive parametric circuits are usually narrow, and the center frequencies and gains are sensitive to process variations.

Therefore, at relatively low operating frequencies, the parametric circuits are much less competitive than active circuits, especially since they need bulky filtering and matching networks at the low frequency. However, in a high-frequency range up to THz, the advantages of parametric circuits become more and more attractive. With the improvements of topology and the performance of the varactor device in CMOS, the cutoff frequencies of the varactors are beyond one THz [17, 39], which makes the parametric circuits in the THz band possible. Whereas the conventional CMOS active circuits are still struggling to provide a sufficient active gain in the sub-THz band, the parametric circuits have the potential to be used as different kinds of transceiver circuits, such as demonstrated in the 1.4-THz multiplier chain in [18]. Although the parametric circuits still need to face the needs of the strong pumping, the frequency converters can be still implemented without a gain, thereby the difficulty can be alleviated, and this issue can be potentially solved by using active voltage-controlled oscillators (VCOs) with a parametric multiplier to generate an LO signal as the high-frequency pumping. As estimated in [29], a zero-dc-power multiplier with an on-chip power amplifier (PA) at a much lower input frequency can consume less dc power than that of an active multiplier operating at the required harmonic frequency.

When the nonlinearity of the core component is increased, in a general case, power at all harmonics will increase, whereas the FMs only require one output harmonic enhanced. To increase the efficiency of the required Nth harmonic, and suppress all other harmonics,

the relation between the specific nonlinearity, the related time-varying parameters, and the generation of the *N*th harmonic, is studied in this thesis theoretically, and is verified in measurements of the demonstration circuits.

Although idlers are necessary for many parametric circuits, such as conventional single-varactor FMs with multiplication factor (N) larger than two as [40], idlers are not desired in the parametric circuits if possible. Since the idler circuits are short or low-impedance terminations at different harmonics other than the required *N*th harmonic and the fundamental input frequency, they may tamper the output of the tunable *N*th frequency multiplications. Therefore, the relation between the time-varying parameters based on certain nonlinearity and the *N*th harmonic generation is wanted to be idler-less.

Once the idler-less relation of certain nonlinearity and *N*th harmonic is obtained, it is expected that not only the efficiency of frequency conversion and harmonic suppression can be effectively understood and improved theoretically, but also FMs with tunable N can be realized based on the tunable nonlinearity with a simplified one-stage circuit topology. Furthermore, with the tunable nonlinearity of the core device, e.g. in some resistive FMs, the CL dependence on the input power level can be reduced to get a flatter CL curve to avoid the dramatic CL change caused by the input level, and improve the total CL and the maximum output power. With an improved device performance and optimized matching networks, the broad BWs of both reactive and resistive multipliers are also one of the major goals for parametric circuits.

As a conclusion, the advantages of the parametric circuits bring the revival of parametric circuits to this century and make them very hopeful candidates for operations in the THz band. As the optical parametric devices already demonstrated in the optical field beyond the range of a hundred THz [5], the parametric circuits have potential to play a critical role in filling the gap between the electronic and the optical fields. However, there are a number of challenges, which need to be solved for the future applications of parametric circuits in the sub-THz and THz bands. Before introducing the work in this thesis to provide some

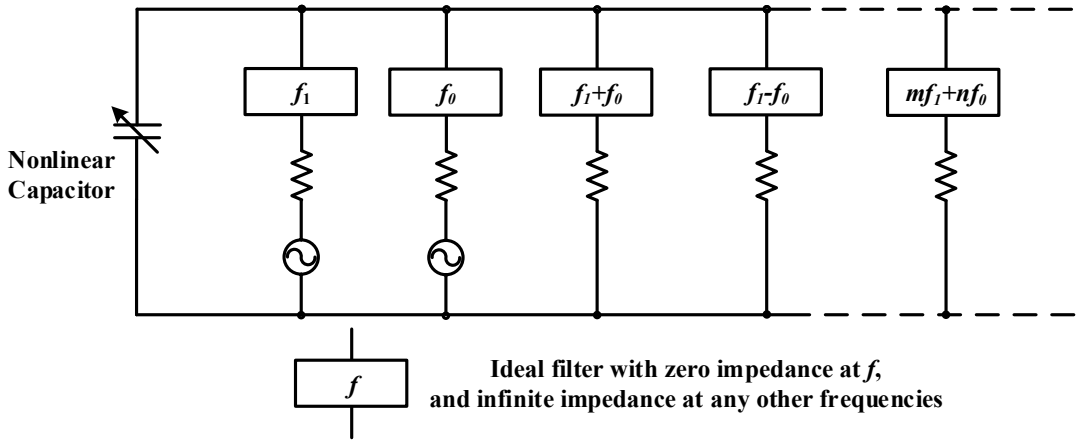


Figure 1.1: Circuit with a nonlinear capacitor to illustrate Manley-Rowe relations.

solutions to these challenges, some basic concepts about the background of the parametric electronics are introduced first.

1.2 Manley-Rowe Relations

Manley-Rowe relations reflect the basic law of energy conservation in the parametric system [2]. To give a picture of the Manley-Rowe relations, a lossless varactor (nonlinear capacitor) is used as shown in Fig. 1.1. Although nonlinear inductance can be also used to build parametric circuits, the research in this thesis focuses on the nonlinear capacitance, due to the practical varactors in silicon processes. An attempt to build a passive nonlinear inductor in CMOS is given in Chapter 6. The input frequencies are at f_0 and f_1. Ideal band-pass filters are used in each paths of the frequency components with resistive terminations. The ideal filter has zero impedance at the pass-band frequency point, and infinite impedance at other frequencies. The powers at each frequencies fulfill the relations as

$$\sum_{m,n} \frac{mP_{mn}}{m\omega_1 + n\omega_0} = 0 \tag{1.1}$$

$$\sum_{m,n} \frac{nP_{mn}}{m\omega_1 + n\omega_0} = 0 \tag{1.2}$$

where m, n are the coefficients of f_1 and f_0, P_{mn} is the power at the frequency equal to $mf_1 + nf_0$, and ω is the angular frequency equal to $2\pi f$. For a frequency multiplier, the input signal is the only signal source, i.e. $m = 0$. The terms in the left side of (1.1) become zero, and (1.2) becomes

$$\sum_n P_n = 0 \tag{1.3}$$

where P_n is the power at the Nth harmonic. Therefore, when only the input fundamental signal and the Nth harmonic output signal exist, ideally the conversion efficiency is 100% due to the lossless varactor, such as

$$P_1 = -P_N \tag{1.4}$$

where the negative sign means the power flowing out of the circuit.

For a varying-resistance circuit, since the circuit is lossy, the maximum conversion efficiency is much lower than for reactive parametric circuits. As the theoretical analysis in [20] indicates, under a condition that the varying resistor has characteristic $\partial i/\partial v \geq 0$, the conversion efficiency is limited by

$$\frac{P_{out}}{P_{in}} \leq \frac{1}{m^2 + n^2} \tag{1.5}$$

where P_{out} is the output power at $mf_1 + nf_0$, and P_{in} is the sum of P_1 and P_0. Again, for FMs, if $m = 0$, the conversion gain of Nth harmonic is limited by

$$\frac{P_{out}}{P_{in}} \leq \frac{1}{N^2}. \tag{1.6}$$

For example, a conventional varistor doubler has a maximum efficiency calculated as 25% due to the lossy resistance, whereas an ideal varactor doubler can have a calculated maximum 100% efficiency. Although it seems that the reactive multipliers may have a much better efficiency than the resistive multipliers, the 100% efficiency is difficult, or sometimes

not even possible to achieve in both theory and real circuits. In contrast, if the nonlinearity of the component can be manipulated so that $\partial i/\partial v < 0$, the efficiency can be higher than the limit from (1.6) as shown in [41], which serves as a good starting point to be exploited to increase the efficiency of the resistive multipliers in this thesis.

1.3 Nonlinear Devices and Parametric Circuits

1.3.1 Nonlinear Devices for Parametric Circuits

The core device of parametric circuits is a nonlinear device with a variable parameter, such as a varactor with variable capacitance (or its inverse, i.e. the elastance) and varistor with variable resistance (or its inverse, i.e. the conductance), with parasitic series R_s or parallel C_p, as in the simplified models shown in Fig. 1.2(a) and (b), respectively. The representations of elastance and conductance are used for the convenience of the analysis, which will be introduced in the following Chapter 2. When the parasitic R_s and C_p are small, and therefore can be neglected, there is no need to distinguish the series and parallel topologies, since only the variable parameter is preserved, such as the S and G in the models.

In CMOS technologies, the varactors are typically accumulation-mode MOS varactors (AMOSVs), whereas varistors are usually realized by Schottky barrier diodes (SBDs) [32]. Since the resistance and capacitance of Schottky diodes can both vary with voltages, the diodes can operate in either varactor mode or varistor mode. In addition, the SBD can operate in a hybrid of varactor and varistor modes, i.e., both the resistance and capacitance are variable such as in [42, 43], which may cause the theoretical analysis of the harmonic generation to become complex and lack the straightforward and intuitive expressions of efficiencies of multipliers. Therefore, in the analysis of the parametric harmonic generation in this thesis, only one parameter of the core nonlinear device is assumed to be variable, i.e., for a varactor, only the capacitance is variable and the series resistance R_s is constant, and for a varistor, only the resistance is variable and the parallel capacitance C_p is constant. Furthermore, to focus on the analysis of the variable parameters, the constant parasitic

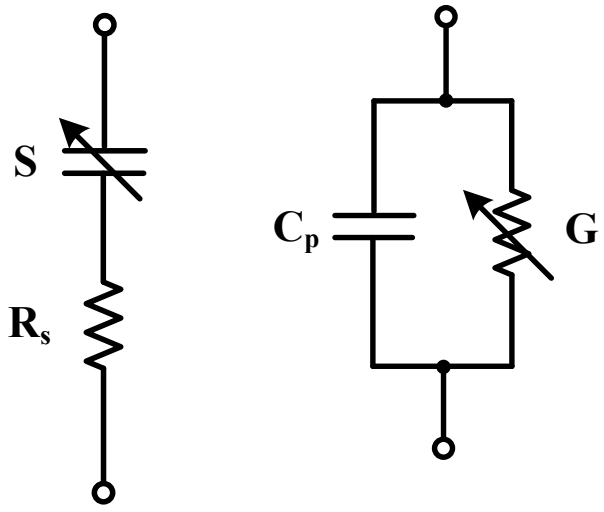


Figure 1.2: The simplified models of (a) a varactor and (b) a varistor.

parameters are assumed small, unless noted otherwise. C_p of varistors is ignored in the theoretical analysis of the resistive multipliers presented in the next chapter about the parametric theory. For similar reasons, to simplify the analysis of reactive parametric circuits, R_s of varactors is also ignored as an approach to the Manley-Rowe lossless condition for reactive multipliers, when doing a part of the calculations in the next chapter. However, the influence of R_s and C_p may become significant in some cases, e.g., when the operation is close to or beyond the cutoff frequency of the varactor, or when the phase difference of pump voltage and current of resistive multipliers exists, R_s and C_p should be taken into the consideration, which will be discussed in the next chapter.

To evaluate both the nonlinear capacitance and the impact of R_s on a parametric circuit, a figure of merit, called dynamic cutoff frequency (f_{cd}), is defined as

$$f_{cd} = \frac{S_{max} - S_{min}}{2\pi R_s} = \frac{r_c - 1}{2\pi R_s} S_{min}, \tag{1.7}$$

where

$$r_c = \frac{C_{max}}{C_{min}} = \frac{S_{max}}{S_{min}} \tag{1.8}$$

is the ratio of the maximum to minimum capacitance or elastance, and elastance S_{max} and S_{min} are the inverse of minimum and maximum capacitance (C_{min} and C_{max}), respectively. Generally speaking, r_c represents the nonlinearity of the capacitance, e.g., r_c=1 means the capacitor is constant and is not a nonlinear capacitor. When r_c is larger, f_{cd} is also larger based on (1.7) when compared at the same level of capacitance. The conventional MOS varactors in mm-wave and THz parametric circuits have limited r_c, such as 2.1 in [30] and 1.6 in [17], which becomes the bottleneck for the high-performance parametric circuits.

The time-varying resistance, on the other hand, can be also used for multipliers and mixers, i.e. the various resistive diode based circuits [31–33]. Based on the nature of the variable resistance, they usually have higher CL than the reactive counterparts; however, since the variable resistance is less frequency dependent, the resistive multipliers can have wider bandwidth such as about 60% relative BW in [44], whereas reactive multipliers usually have a limited BW, such as 12% in [30]. The nonlinear ratio of maximum to minimum resistance (r_r) can be also tuned for resistive multipliers by tuning the current-voltage (I-V) curves, which is called self-dynamic biasing and static biasing in [33]. However, self-dynamic biasing is dependent on the input level, and static biasing in [33] is used for a low input power level. Both of them can only tune one side of the I-V curves around the off zone, and need extra dc-block capacitors in the biasing circuits.

This thesis proposes the following new devices to improve the performance of parametric circuits:

- a new switched-capacitor varactor (SCV) topology is proposed and implemented, which obtains an r_c as high as 20 and a 1.5-THz f_{cd}. The SCV advances the performance of varactors well into the THz band using a 22-nm CMOS SOI technology;

- a new type of varactors is also used to tune the inductance of a mm-wave on-chip inductor-capacitor (LC) tank to realize a voltage-controlled inductor, which is used to build a D-band (defined as 110 to 170 GHz) injection-locked oscillator (ILO) in this thesis, which can serve as a signal source for the future THz applications;

- a topology using back-gate control voltage (V_{BG}) is proposed and used in a resistive multiplier to provide input-level independent R-V control with good symmetry around zero voltage, and does not need extra biasing circuit components based on the CMOS SOI technology.

When the circuits in 22-nm CMOS SOI were designed and fabricated, the design kits were still immature and under development by the foundry.

1.3.2 Four-Frequency Mode of Operation

Although the Manley-Rowe relations indicate that the parametric process involves infinite number of harmonic combinations of the input frequencies, i.e. f_0 and f_1 (in practice f_1 is not multiple or sub-harmonic of f_0, known as "in-commensurate" [19]), in practical analysis of parametric circuits, a typical process called "four-frequency mode of operation" is often used [45]. In the four-frequency mode, a small RF signal is added to and subtracted from a strong pump signal, thereby in total four signals are involved at f_0+f_1, f_0-f_1, f_0, and f_1 frequencies. Pumping at f_0 is typically strong, which can decide the time-varying parameter of the circuit, whereas the RF input at f_1 is small, causing the linear system response to the RF signal, and the linear analysis methods, such as based on impedance Z-matrix or admittance Y-matrix, can be used to analyze the system. As a result, the total system is time-varying but linear [2].

From this point of view, the parametric frequency multipliers can be considered as the most basic parametric circuits, since the RF input and fundamental pumping are exactly the same in the parametric multipliers. Only the fundamental input f_0 and its harmonics Nf_0 exist in the multiplication process, so that the theoretical analysis can be much simplified. Parametric dividers are more complex than multipliers, since sub-harmonics are generated in the dividing process. Notice that since pumping is generally necessary for any parametric circuits, the analysis of FMs offers the foundation of theories that can be expanded for all externally pumped parametric circuits.

The generation of high-frequency harmonics without using idlers can not only be directly used as the pumping of parametric amplifiers or frequency converters but also can be combined into the other parametric circuits to save the number of components and reduce the loss between different circuit stages. For example, to build a parametric amplifier or frequency downconverter around 200 GHz, the pumping is necessary to be at or above 200 GHz, however, assuming that the strong pumping signal is only available up to 40 GHz due to instrument limitations, then the FM is needed with $N \geq 5$. Since the same varactor can be used both for the parametric multiplier and the parametric amplifier or frequency converter, the topology called "harmonic pumping" can be utilized to reduce the number of the circuit stages and combine the multiplier and other parametric circuit together [19]. The input sub-harmonic pumping frequency can be much lower than the required pumping frequency, e.g., in the previous example, the pumping is at 40 GHz, which is internally multiplied to 200 GHz, and is used as the pumping of the high-frequency amplifiers or frequency converters.

Since harmonic pumping parametric circuits are combinations of multipliers and other parametric circuits, the theory for the idler-less harmonic generation is not only key for parametric FMs but also paves a road to realize other future sub-THz and THz parametric circuits with harmonic pumping. For example, a frequency-domain analyzing method is utilized for a frequency upconverter in [46], which can be further developed with the harmonic pumping with a sub-harmonic LO. Sub-harmonic $\times 2$ LOs are used for the THz frequency downconverters in [13] and [14] with APDPs, whereas based on this harmonic generation theory, the conversion efficiency can be potentially improved if the APDPs are used for odd-order harmonic pumping instead of the even-order.

1.3.3 Idlers

The idlers are signals generated or used in the parametric process, but not a part of inputs or outputs [19]. For a frequency multiplier, the input frequency is the fundamental frequency

at f_0, and the output is at Nf_0 for the N^{th} FM, whereas the idler frequency can be at $2f_0$ to $(N-1)f_0$. One or more idlers are considered necessary for one-varactor parametric multipliers with $N > 2$ [40]. For example, for a tripler the idler is at $2f_0$, so that the output is at $3f_0 = 2f_0 + f_0$. For a quadrupler, the idler is also at $2f_0$. For a quintupler, at least two idlers are necessary, either at $2f_0$ and $3f_0$, or $2f_0$ and $4f_0$. With larger and larger N, more and more idlers are necessary [19].

The idlers circuits in the parametric circuits are realized as terminals with certain impedance or short circuit conventionally. These idler circuits not only increase the complexity and loss, increase the cost of the circuits in terms of more circuit components, but also tamper the tunability of N of the multiplier. For example, in a quintupler, a short-circuit idler is at $4f_0$, which shorts the output as a quadrupler. This demonstrates that other topologies should be considered to deal with the idlers of the quintuplers, if a multiplier with tunable N is wanted.

Others have long learned that in a parametric tripler, the second harmonic idler can be removed by the mirror symmetry of the C-V curve [21]. The varactor triplers are implemented based on one "peak" or "valley" C-V curves such as in [29,30]. C-V with one valley is also used in the parametric quintupler at 0.7 THz in [17]; however, since the "1-valley" C-V curve is conventionally used for the third harmonic generation, when applied in the quintupler, either the strong third harmonic needs to be filtered out, or the third harmonic should be used as an idler. Therefore, one important motivation of this research is to investigate how to realize any-order parametric multipliers without using idlers. The symmetry of the parameter-voltage (P-V) curve is proved to be critical for the idler-less harmonic generation, and as the theoretical analysis in this work shows, the required symmetry of the P-V is much more complex than a simple mirror symmetry or monotonic asymmetry of conventional passive multipliers.

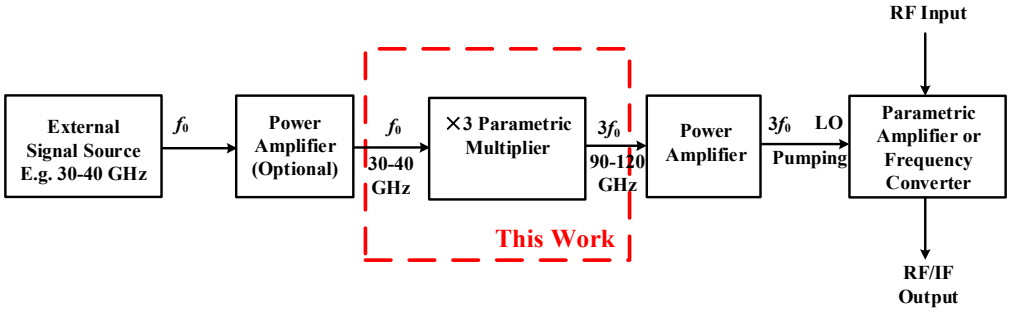
The symmetric R-V curve can be also used for the odd-order generation of harmonics based on diodes [31–33]. The nonlinear R-V curves with multiple peaks or valleys have

been found useful in the high-order harmonic generation without fulfilling the condition limited by $\partial i/\partial v > 0$ [41]. However, the relation between certain nonlinear R-V, the time-varying resistance, and the Nth harmonic was not well explained, and the third harmonic idler was used for the $\times 5$ resistive multiplier in [41]. In this research, the general relation between time-varying parameters and harmonic generation is developed in terms of not only reactive parameters C and S, but also resistive parameters R and G, so that the theory can provide a full vision for both reactive and resistive parametric multipliers.

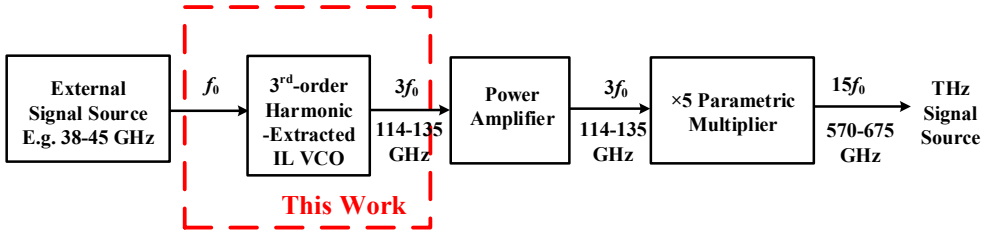
1.4 Examples of Applications of Parametric Circuits in Wireless Transceivers

To illustrate the applications of the parametric circuits and the injection-locked oscillator (ILO) designed in this thesis, the diagrams of potential applications are shown in the Fig. 1.3. As a direct application, the input mm-wave signal can be used to pump the parametric multiplier as this work, and generate the output signal in the lower D-band, which can be amplified by a PA and further used as the input of LO (pumping) signal of the next stage of parametric amplifiers or frequency converters with an RF output signal for an amplifier or IF for a downconverter, respectively, as shown in Fig. 1.3(a).

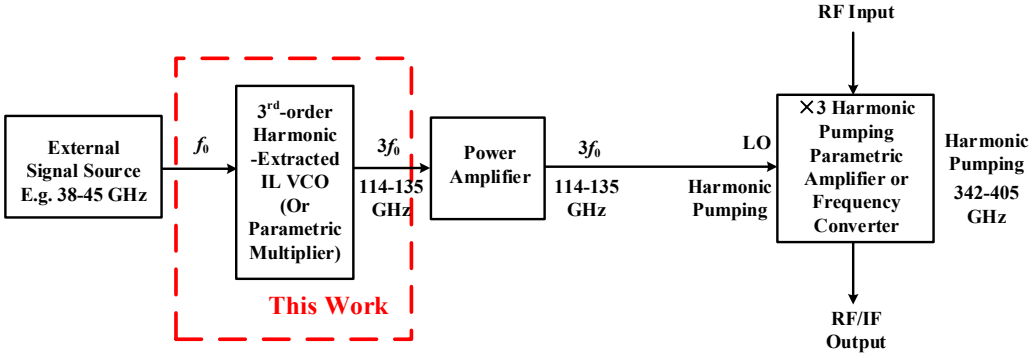
As an alternate choice, the ILO designed in this work is injection locked by a low-frequency input signal from an external source, and a third-order harmonic is generated at the D-band. The ILO operates similarly as a multiplier, and the output can also be used as the input of the next multiplier stage, to generate a higher-frequency harmonic in the THz band, as shown in Fig. 1.3(b). The voltage-controlled ILO (IL VCO) does not need an input PA since it does not need a very high input power, such as 10 dBm in a typical case. An additional D-band PA may be needed after the harmonic oscillator or the frequency multiplier, to enhance the input power of the next stage, such as a THz multiplier chain. The D-band PA is not part of this thesis, but it has been demonstrated in 16-nm FinFET CMOS technology with a 26-dB gain and 15-dBm output power around 115 to 135 GHz consuming 207-mW dc power in [47]. The THz multipliers can be designed



(a)



(b)



(c)

Figure 1.3: Potential applications of this work: (a) parametric multiplier for a D-band parametric amplifier or frequency converter; (b) harmonic-extracted IL VCO for a THz signal source; (c) IL VCO or parametric multiplier for harmonic pumping of THz parametric circuits.

in the same way as the D-band multipliers, e.g., a quintupler with a "two-peak" C-V curve based on the parametric theory demonstrated in this thesis. The mm-wave and potential THz parametric multipliers can operate based on the same theory, and the simulated f_{cd} of

the varactor device in this thesis can be beyond one THz, although due to the limitation of the measurement conditions, the passive multipliers are only designed to the upper limit of the D-band in this work.

As a future development, the multiplier and the other functional parametric stage such as a parametric amplifier or a frequency converter in the THz band can be combined together as the harmonic pumping topology, which is shown in Fig. 1.3(c). In this circuit: a separate THz multiplier is avoided, the number of circuit components is reduced, the topology of filtering and matching networks is simplified, and the total loss of the circuit chain can be decreased. For the applications in the sub-THz and THz bands, some important specifications of parametric multipliers, such as CL, BW, output power, and harmonic suppression need to improve based on new theories and topologies, which will be addressed in the later chapters.

1.5 Outlines of the Thesis

As per the discussions in this chapter, there are several challenges for parametric circuits to be used in the mm-wave, sub-THz, and THz applications.

First, the theory of parametric harmonic generation and time-varying parameters obtained by certain device nonlinearity is necessary but has not been studied in depth in the past, especially for $N > 3$. The key question is how to enhance the required harmonic while suppressing all other harmonics. This goal cannot be simply realized by increasing the ratio of maximum to minimum capacitance r_c or resistance r_r, since simply increasing the ratio may increase power at all harmonics. For example, the second, third, and fourth harmonics are not wanted when building a quintupler, i.e. the harmonic suppression will be much worsened if all the harmonics are enhanced simultaneously. The idlers are not wanted in this relationship. The theory of the parametric generation and the required time-varying parameters with a specific nonlinearity is given in Chapter 2. The calculated conversion efficiency of reactive and resistive circuits are also given.

On the other hand, with a proper theory of harmonic generation for a certain harmonic, increasing the ratio r_c is still welcomed for varactors, since f_{cd} can be increased with higher r_c. In the conventional CMOS process, the r_c of varactors is limited, and the performances of parametric circuits with these varactors are also limited when operating at high frequencies, such as in the sub-THz or THz band. To increase r_c, an SCV topology is proposed and verified in a D-band parametric multiplier together with the tunable C-V curves to realize a reconfigurable parametric multiplication. A topology to tune the resistance ratio r_r is used to adjust the R-V curve to reduce the CL at a high input power with a back-gate control voltage.

A varactor tripler operating in the 28-GHz 5G New Radio (NR) band is described in Chapter 3 to demonstrate that the parametric circuits can be used in the mm-wave band as one candidate in the surging 5G tidal wave. The 27.1 to 32.4 GHz frequency tripler is implemented in a 45-nm SOI CMOS, with a maximum −8-dBm output power and minimum 24.3-dB CL. The harmonic suppression achieves 13.6 dBc for the fundamental and 20.1 dBc for the second harmonic, respectively.

In Chapter 4, to demonstrate the theory of the relation between the time-varying capacitance, the corresponding shapes of nonlinear C-V curve with peaks and valleys, and the N^{th} harmonic generation while suppressing all other harmonics, two passive third-, fourth, and fifth-order reconfigurable D-band frequency multipliers (RFMs) are designed and measured. To demonstrate the advantages of the SCV, the multiplier circuits are implemented both with SCVs and conventional MOS varactors in a 22-nm SOI CMOS process. Significant improvements in CL and relative BW are achieved in both simulations and measurements with the SCV multiplier.

In Chapter 5, a resistive tripler is also designed in the D-band with diode-connected MOS FETs in the 22-nm SOI CMOS technology to demonstrate the tunability of the back-gate voltage and the nonlinear R-V curve to reduce CL and enhance output power. The output power and CL are improved by 1.7 dB when V_{BG} is reduced from 0 to −2 V.

A D-band injection-locked Colpitts oscillator, which can be used as the signal source of the sub-THz parametric applications, is demonstrated in Chapter 6. With a very large tuning range of the variable capacitance, the control voltage of the transistor-controlled capacitor (TCC) can be used to tune a mm-wave variable inductance, so that the injection-locked oscillator can be controlled by a voltage-controlled inductor (VCI). The voltage-controlled ILO with the third-order harmonic extracted in the D-band operates between 112.5 to 135 GHz.

The conclusion is summarized in Chapter 7. The future work is also concluded in this chapter. The extension of the parametric harmonic generation theory to parametric frequency dividers is included in the Appendix.

1.6 Thesis Contributions

The 28-GHz varactor frequency tripler, the D-band resistive tripler and the ILO with VCI were published in the IEEE Microwave and Wireless Components Letters in [29], [31], and [48], respectively.

The D-band RFMs were presented and published in the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2020 [39].

A paper discussing the relations of time-varying circuit parameters and idler-less parametric harmonic generation has been submitted for review to IEEE Transactions on Microwave Theory and Techniques in November, 2020.

Chapter 2

Relations of Time-Varying Circuit Parameters and Idler-less Parametric Harmonic Generation

In this chapter, the theory of relations of time-varying parameters (P) [i.e. capacitance (C), elastance (S), resistance (R), or conductance (G)], the corresponding P-V curves [i.e., C-V, S-V, R-V or G-V curves], and the generation of specific harmonics of the fundamental input are discussed. First the basic concepts and frequency-domain analysis methods are introduced. Then a sinusoidal representation of time-varying parameters is introduced for both reactive and resistive multipliers, which is the key for the proposed relations between the time-varying parameter and the required any-order harmonic generation. After that, since the sinusoidal representation of resistive parameters has some limitations in the resistive multipliers, an impulse representation of time-varying parameters is also proposed to further analyze the operation of resistive multipliers. The efficiency calculated as a conversion gain (actually conversion loss for the passive multipliers) is given, which is simply $1/N$ for the Nth-order reactive parametric multipliers.

Inspired by prior works on varactor triplers and quintuplers with one-peak or one-valley symmetric C-V curves such as in [17, 21, 49], the idler-less Nth-order harmonic generation with sinusoidally and impulse pumped parameters and the related theoretical relations are first proposed in this work.

2.1 Basic Concepts and Equations

Conventionally, single-varactor parametric multipliers are analyzed in frequency domain [19], whereas parametric triplers with symmetric C-V curves are analyzed based on the transient equations [21]. Transient methods need complex transient calculations and cannot be easily used for general any-order FMs but limited to special cases, e.g., idler-less triplers. It is also difficult to apply the transient analysis to the even-order harmonic generation

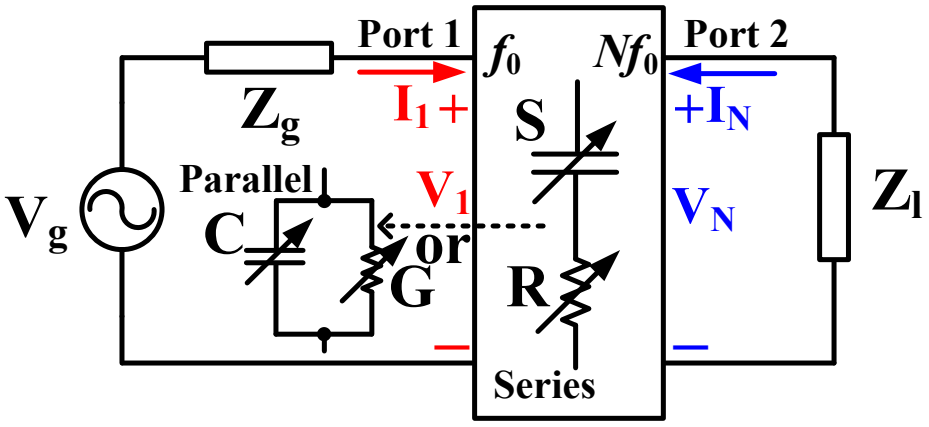


Figure 2.1: Two-port network for the analysis of parametric multipliers.

with a high order ($N > 3$). The state-of-the-art passive one-stage quadruplers still use a monotonic C-V or I-V curve for the fourth-order harmonic generation, which unavoidably generate the second-order harmonic that is used as an idler [43].

To obtain the general relation of the parametric harmonic generation with specific nonlinearity, the analysis in this thesis begins with the conventional frequency-domain analyzing methods based on the impedance- (Z-) and admittance- (Y-) matrix methods [19].

A two-port network with a nonlinear varactor or varistor is shown in Fig. 2.1. For convenience of the analysis of multipliers, the varactors are typically connected in series, and the varistors are typically connected in parallel. The source V_g is utilized to provide the fundamental input signal V_1 at f_0, and the output signal V_N is at Nf_0. The current I_1 and I_N at the fundamental and N^{th} harmonic are indicated by the directions of the currents in Fig. 2.1, respectively. The source impedance is Z_g and load impedance is Z_ℓ. The ideal filters are also used (not shown in the figure) in the FM, to ensure that only the signals at f_0 and Nf_0 can pass through port 1 and 2, respectively.

The input pump voltage and current are periodic in time, and so are the time-varying Ps driven by the periodic input signals. When the series topology is used, the transient voltage-current (V-I) relation of the nonlinear device is based on the variable impedance

$Z = R + S/(j\omega)$, which is given as

$$v(t) = \int S(t)\, i(t)\, \mathrm{d}t + R(t)\, i(t) \tag{2.1}$$

where $v(t)$ and $i(t)$ are voltage and current flowing through the nonlinear device, respectively, $S(t)$ is the time-varying elastance [inverse of the time-varying capacitance $C(t)$], and $R(t)$ is the time-varying resistance representing an in-phase (i.e., resistive) ratio of $v(t)$ and $i(t)$. Unlike the constant capacitance, the variable capacitance of a nonlinear capacitor is a kind of incremental capacitance [19], of which the total charge Q_c cannot be simply expressed by $Q_c = CV$ because it needs an integration over the voltage range with the changing C.

To get the frequency-domain expressions of the V-I relations, V, I, and Z are represented with Fourier series as

$$S(t) = \sum_{k=-\infty}^{\infty} S_k e^{jk\omega_0 t} \tag{2.2}$$

$$R(t) = \sum_{k=-\infty}^{\infty} R_k e^{jk\omega_0 t} \tag{2.3}$$

$$v(t) = \sum_{k=-\infty}^{\infty} V_k e^{jk\omega_0 t} \tag{2.4}$$

$$i(t) = \sum_{k=-\infty}^{\infty} I_k e^{jk\omega_0 t} \tag{2.5}$$

where k is the number of each harmonic of the Fourier coefficients of elastance (S_k), resistance (R_k), voltage (V_k), and current (I_k), and ω_0 is angular frequency equal to $2\pi f_0$. These Fourier coefficients are found from

$$P_k = \frac{1}{2\pi} \int_0^{2\pi} P(t)\, e^{-jk\omega_0 t}\, \mathrm{d}(\omega_0 t) \tag{2.6}$$

where $P(t)$ represents a time-varying parameter [i.e. either $S(t)$ or $R(t)$ or as discussed

next either $G(t)$ or $C(t)$] of which the Fourier coefficients are of interest as well as $v(t)$ and $i(t)$. Since $S(t)$, $R(t)$, $v(t)$, and $i(t)$ are all real, the complex conjugations of the Fourier coefficients fulfill $S_k^* = S_{-k}$, $R_k^* = R_{-k}$, $V_k^* = V_{-k}$, and $I_k^* = I_{-k}$.

The basic V-I relations of the parametric multipliers then can be derived for kth-order of voltage in terms of mth-order of current ($m \in \mathbb{Z}$), by applying (2.2)–(2.5) in (2.1) when $k, m \neq 0$,

$$V_k = \sum_{m=-\infty}^{\infty} I_m \left(R_{k-m} + \frac{1}{jk\omega_0} S_{k-m} \right). \tag{2.7}$$

Therefore, each harmonic voltage is the sum of multiples of an infinite number of harmonic currents.

Specifically, as an example, the complete equations for the first three terms (useful for reactive doublers and triplers) are given as

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = Z_{\text{react}} \times \begin{bmatrix} I_3^* \\ I_2^* \\ I_1^* \\ I_1 \\ I_2 \\ I_3 \end{bmatrix} \tag{2.8}$$

where

$$Z_{\text{react}} = \begin{bmatrix} \frac{S_4}{j\omega_0} & \frac{S_3}{j\omega_0} & \frac{S_2}{j\omega_0} & R_s + \frac{S_0}{j\omega_0} & \frac{S_1^*}{j\omega_0} & \frac{S_2^*}{j\omega_0} \\ \frac{S_5}{j2\omega_0} & \frac{S_4}{j2\omega_0} & \frac{S_3}{j2\omega_0} & \frac{S_1}{j2\omega_0} & R_s + \frac{S_0}{j2\omega_0} & \frac{S_1^*}{j2\omega_0} \\ \frac{S_6}{j3\omega_0} & \frac{S_5}{j3\omega_0} & \frac{S_4}{j3\omega_0} & \frac{S_2}{j3\omega_0} & \frac{S_1}{j3\omega_0} & R_s + \frac{S_0}{j3\omega_0} \end{bmatrix} \tag{2.9}$$

with R_0 replaced by R_s and all high-order coefficients of R are neglected.

When the parallel topology is used, variable admittance $Y = G + j\omega C$ can be used to analyze I-V relations in the same way but with

$$i(t) = C(t) \frac{\mathrm{d}v(t)}{\mathrm{d}t} + G(t)\, v(t) \tag{2.10}$$

where $C(t)$ is the time-varying capacitance, and $G(t)$ is the time-varying conductance. By using Fourier series,

$$G(t) = \sum_{k=-\infty}^{\infty} G_k e^{jk\omega_0 t} \tag{2.11}$$

$$C(t) = \sum_{k=-\infty}^{\infty} C_k e^{jk\omega_0 t}, \tag{2.12}$$

where Fourier coefficients G_k and C_k are found from (2.6), and $G_k^* = G_{-k}$ and $C_k^* = C_{-k}$. Again, by replacing Fourier coefficients in (2.10),

$$I_k = \sum_{m=-\infty}^{\infty} V_m \left(G_{k-m} + jk\omega_0 C_{k-m}\right). \tag{2.13}$$

When the order is limited to three, the frequency conversion Y-matrix for a resistive multiplier is

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = Y_{\text{resis}} \times \begin{bmatrix} V_3^* \\ V_2^* \\ V_1^* \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{2.14}$$

where

$$Y_{\text{resis}} = \begin{bmatrix} G_4 & G_3 & G_2 & G_0 + j\omega_0 C_p & G_1^* & G_2^* \\ G_5 & G_4 & G_3 & G_1 & G_0 + j2\omega_0 C_p & G_1^* \\ G_6 & G_5 & G_4 & G_2 & G_1 & G_0 + j3\omega_0 C_p \end{bmatrix} \tag{2.15}$$

with C_0 replaced by C_p and all high-order coefficients of C are neglected.

Noticing that ideal filters are put in the input and output ports, the input impedance at the fundamental frequency f_0 and the output impedance at the output frequency Nf_0 can

be found from (2.7) or (2.13). The input impedance at f_0 is found by

$$Z_{in} = \frac{V_1}{I_1} = \sum_{m=-\infty}^{\infty} \frac{I_m}{I_1} \left(R_{1-m} + \frac{1}{j\omega_0} S_{1-m} \right) \tag{2.16}$$

and the output impedance at the Nf_0 is found by

$$Z_{out} = \frac{V_N}{I_N} = \sum_{m=-\infty}^{\infty} \frac{I_m}{I_N} \left(R_{N-m} + \frac{1}{jN\omega_0} S_{N-m} \right). \tag{2.17}$$

At the terminations, the circuit signal-source impedance Z_g and source voltage V_g establish

$$V_g = V_1 + Z_g I_1 \tag{2.18}$$

and the circuit load Z_ℓ results in

$$V_N = -Z_\ell I_N. \tag{2.19}$$

With these termination conditions and together with (2.7) or (2.13), the conversion efficiencies of the parametric multipliers can be derived. These efficiencies are defined in the similar way of power gains, but the number is always negative in decibels (dB), since the parametric multipliers are passive and consume no dc power. The conversion "gain" is actually "loss" when discussed in the thesis.

Similar as the transducer gain of amplifiers, the frequency conversion transducer gain $G_{T,N}$ is defined as the power delivered to the load at the Nth harmonic over the available power from the source at the fundamental frequency, which is calculated from

$$G_{T,N} = \frac{|I_N|^2 \Re\{Z_\ell\}}{|I_1|^2 \Re\{Z_g\}}. \tag{2.20}$$

The frequency conversion power gain $G_{P,N}$ is defined as the ratio of the power delivered to

the load to the power delivered into the circuit, which is calculated from

$$G_{P,N} = \frac{|I_N|^2 \Re\{Z_\ell\}}{|I_1|^2 \Re\{Z_{in}\}}. \tag{2.21}$$

From the definitions of various conversion gains, $G_{P,N}$ represents the ability of the multiplier to provide the frequency conversion, and indicates the maximum efficiency under the condition of power match at the output port, whereas $G_{T,N}$ is the power gain that can be actually measured in real multipliers, and may be different from $G_{P,N}$, unless a conjugate match condition is fulfilled at the input port. Again, these "conjugate power matching" conditions are only applied to the fundamental and Nth-order harmonic at the source and load, respectively, which will be explained in details in Section 2.4.1.

Before deriving the specific expressions of efficiencies of reactive and resistive multipliers, first the pumping and pumped parameters are introduced in the next subchapter.

2.2 Pumping and Pumped Parameters

As introduced in Chapter 1, pumping is one of the most important features of the parametric circuits to vary the specific variable parameter of the circuits. The pump signal is a large signal, which can decide the time-varying state of the parametric circuits, and is generated by an LO or an external input signal. Since in parametric multipliers, pumping is the only input signal, the pumped parameters, which are represented by P in this thesis (when P represents power, subscripts are used to distinguish them), dominate the performance of the parametric circuits. Therefore, the key for the investigation of the parametric harmonic generation is to research the pumped parameters under certain pumping conditions.

In real circuits, the pumped $P(t)$ is dependent on the input power level, e.g., with a monotonic parameter-voltage (P-V) curve, the ratio of maximum to minimum P is increased with the increasing input voltage range. To simplify the problem, the pump voltage range is normalized to -1 to 1 V in this research, as well as the voltage range in the P-V

curves, which means a full pumping defined in this voltage range. In the series topology, the small parametric resistance of the varactor is ignored, thereby the voltage is fully applied to the variable capacitance. The transient waveforms can have various forms; however, the most common form is the sinusoidal voltage

$$V(t) = \cos(\omega_0 t) \tag{2.22}$$

where the amplitude is normalized to 1, and the initial phase of the pump voltage is arbitrarily set to zero for convenience. Since there is only one input signal in the FMs, the initial phase should not have an influence to the process of the harmonic generation, if the starting time instance of the analysis is arbitrarily selected, assuming the pumped circuit is not sensitive to the initial phase, e.g. P-V curve is an equation of polynomials dependent on the voltage.

The current can also be used as the pumping force instead of the voltage. For resistive or reactive components, the periodic pumped parameters under periodic voltage pumping are approximately equivalent to the parameters under periodic current pumping, i.e. there is no essential difference of the harmonic generation when the input is either a fundamental current or a voltage. As explained in [19], in the series topology the variable capacitance and resistance are in series thereby current pumping is preferred, whereas in the parallel topology the voltage pumping is preferred. To simplify the analysis, in the following discussions, the small parasitic R_s or C_p is neglected, and only V-I relations based on Z-matrix and pump voltage are used, unless noted otherwise.

When a polynomial expression for modeling P-V curves is used, it may be natural to assume that the pumped parameters may be in the form of sine waves. However, the question is what the pumped parameter is like, and what kind of nonlinear P-V curves can be utilized to get the required time-varying parameter, which is related to the specific harmonic generation. In the conventional theory, the calculated Fourier coefficients of P are

all non-zero, whereas the key idea of the theory in this work is to only keep the necessary coefficients non-zero in order to generate the Nth-order harmonic while suppressing all other harmonics, i.e., only the required output harmonic is generated and all the other harmonics are not produced. The required non-zero Fourier coefficients are obtained by a sinusoidal pumping, and the corresponding transient pumped parameter is in the simplest form, which are introduced in the next subchapter.

2.3 Sinusoidal Representation of Pumped $P(t)$ (SRPP)

When the polynomials for modeling P-V are used, based on the expression of $V(t)$ as (2.22), the expression of $P(t)$ for the harmonic generation can be expected to be composed of terms of $\cos(n\omega_0 t)$, where n is a non-negative integer. The initial phase is set to zero since the pump voltage has a zero initial phase, and the amplitude is normalized to unity. The only coefficient left is n, whose expression is desired to be as simple as possible.

For the targeted idler-less Nth-order harmonic frequency multiplication, only the fundamental and the Nth harmonic exist at the input and output ports, respectively. By applying filters to the two ports, all other harmonics, which are not of interest, are removed from the V-I equations of Z-matrix in (2.7) or Y-matrix in (2.13), therefore there are ideally $V_k|_{k\neq\pm N,1} = 0$ and $I_k|_{k\neq\pm N,1} = 0$ to avoid generation of other harmonics and to remove idlers. To simplify the analysis, only V_1, V_N, I_1, I_1^*, I_N, and I_N^* are kept in the analysis of the Z-matrix in (2.7) , whereas expressions of V_1^*, V_N^* can be obtained by the symmetry of the matrix straightforwardly.

By observing (2.7) and knowing that only the fundamental and Nth harmonic are taken into consideration, the coefficients are set at $k = N$, and $m = 1$, then the harmonic output voltage V_N is related to the fundamental input I_1 with a variable parameter P_{N-1}, whereas V_N is related to I_N with P_0 by setting $k = N$, and $m = N$. P_0 is a dc coefficient, which is always larger than zero, for a practical positive capacitance or resistance.

Since $V_N \equiv V_k|_{k=N}$ is calculated by adding multiples of I_1, I_1^*, I_N, and I_N^* by the Fourier

coefficients of P, it seems that the terms of I_1^* and I_N^* should also be taken into consideration in (2.7) or (2.13). However, when setting $k = N$, and $m = -1$ or $-N$, the resultant coefficients P_{N+1} and P_{2N} are assumed to be small because of the larger order, thereby they can be neglected. Therefore, only Fourier coefficients P_0, P_{N-1}, and P_{N-1}^* of a variable circuit parameter $P(t)$ (representing S, C, G, or R) are necessarily non-zero for the Nth-order idler-less frequency multiplication (harmonic generation).

The Euler's formula $\cos(x) = \frac{1}{2}e^{jx} + \frac{1}{2}e^{-jx}$ can be applied to get the non-zero P_{N-1} and P_{N-1}^* such as

$$\cos\left((N-1)\,\omega_0 t\right) = \frac{1}{2}e^{j(N-1)\omega_0 t} + \frac{1}{2}e^{-j(N-1)\omega_0 t}. \tag{2.23}$$

Compared with (2.2), the transient sinusoid $\cos\left((N-1)\,\omega_0 t\right)$ is directly related to P_{N-1} and P_{N-1}^*. Therefore, when the time-varying parameter $P(t)$ has the form of $\cos\left((N-1)\,\omega_0 t\right)$ under pumping of $\cos\left(\omega_0 t\right)$, i.e. the pump voltage $V(t)$, the Nth-order idler-less parametric harmonic generation is obtained. This condition means that in one pumping period, the pumped parameter should have $N-1$ periods. Chebyshev polynomials of the first kind provide such a relationship [50]:

$$\cos\left((N-1)\,\omega_0 t\right) = T_{N-1}\left(\cos\left(\omega_0 t\right)\right) \tag{2.24}$$

where $N \in \mathbb{Z}^+$. The expression of T_{N-1} is

$$T_{N-1}(V) = \sum_{r=0}^{[(N-1)/2]} \frac{(-1)^r\,(N-1)!\left(1-V^2\right)^r V^{N-1-2r}}{(2r)!\,(N-1-2r)!}. \tag{2.25}$$

The first six expressions of $\cos\left((N-1)\,\omega_0 t\right)$ are given as

$$T_0 = 1 \tag{2.26}$$

$$\cos\left(\omega_0 t\right) = T_1 = V(t) \tag{2.27}$$

$$\cos(2\omega_0 t) = T_2 = 2V(t)^2 - 1 \tag{2.28}$$

$$\cos(3\omega_0 t) = T_3 = 4V(t)^3 - 3V(t) \tag{2.29}$$

$$\cos(4\omega_0 t) = T_4 = V(t)^4 - 8V(t)^2 + 1 \tag{2.30}$$

$$\cos(5\omega_0 t) = T_5 = 16V(t)^5 - 20V(t)^3 + 5V(t). \tag{2.31}$$

To avoid negative transient pumped parameters and generate practical $P(t)$ based on the pump voltage from (2.22), each expression from T_0 to T_5 is increased by one (in reality, any number larger than 1 is applicable to make sure the pumped parameter larger than zero) resulting in the following P_{N-1} (normalized such that $P \in [0,2]$) dependence on $V \in [-1,1]$:

$$P_0(V) = 2 \tag{2.32}$$

$$P_1(V) = V + 1 \tag{2.33}$$

$$P_2(V) = 2V^2 \tag{2.34}$$

$$P_3(V) = 4V^3 - 3V + 1 \tag{2.35}$$

$$P_4(V) = 8V^4 - 8V^2 + 2 \tag{2.36}$$

$$P_5(V) = 16V^5 - 20V^3 + 5V + 1. \tag{2.37}$$

The normalized P-V curves for the harmonic generation with $N \leq 6$ are plotted in Fig. 2.2. A constant P_0 is related to a fixed capacitor or resistor, and does not perform any frequency conversion. P_1 has a monotonic and asymmetric (around the zero-vertical axis) dependence on V, which generates a $P(t)$ in the form of $\cos(\omega_0 t)$ under pumping of $V = \cos(\omega_0 t)$, and is useful for doublers. P_2 is a symmetric parabola curve (termed "1-valley curve"), which exhibits $P(t)$ in the form of $\cos(2\omega_0 t)$, and is used for triplers. P_3, P_4, and P_5 can be described as "1-peak and 1-valley", "2-valley", and "2-peak and 2-valley"

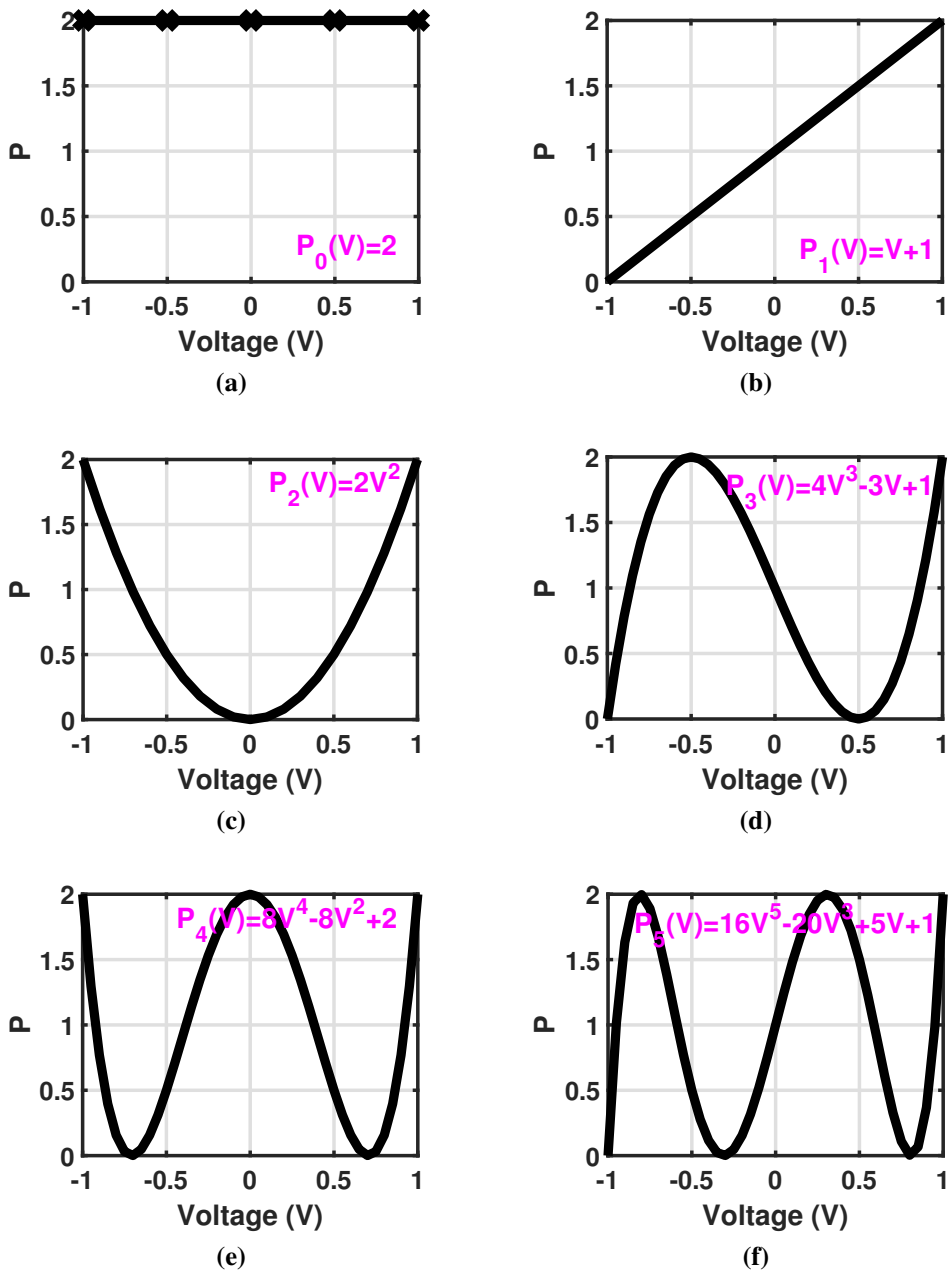


Figure 2.2: Normalized P-V curves for (a) fundamental, (b) second-order, (c) third-order, (d) fourth-order, (e) fifth-order, and (f) sixth-order harmonic generation, respectively.

curves, which are used for the generation of the fourth-, fifth-, and sixth-order harmonics, respectively. The P-V dependence of harmonic generations for higher N can be generalized in the same way based on (2.25). From the analytical expressions and the plotted P-V curves, the symmetry of the P-V curves to generate the required harmonics efficiently can

be concluded. To generate Nth odd-order harmonic, $P(V)$ is an even function, and the P-V curve should be mirror symmetric, i.e., the P-V curve is reflected by the vertical axis at zero voltage. To generate Nth even-order harmonic, $P(V)$ is an odd function, and the P-V curve should be asymmetric, i.e. the P-V curve is rotationally symmetric around the origin. As the normalized P-V curve illustrated in Fig. 2.2, the curves in (a), (c) and (e) are mirror symmetric for the odd-order harmonic generation, whereas the curves in (b), (d) and (f) are rotationally symmetric for the even-order harmonic generation.

2.4 Examples of SRPP

2.4.1 Pumped Elastance with SRPP

The reactive multipliers have time-varying parameters as elastance S or capacitance C. The analysis begins with S but it can be also used for C, since the transient C can be seen as an out-of-phase approach of the transient sine wave of S. The frequency doubling from pumped elastance is based on the S-V relation(2.33), i.e., $S(V) = V + 1$. The resistance R_s is assumed a small constant value, so that the resistive high-order Fourier coefficients are zero in (2.7). Then, $S(t)$ is

$$S(t) = \cos(\omega_0 t) + 1. \tag{2.38}$$

Applying Euler's formula $\cos(x) = \frac{1}{2}e^{jx} + \frac{1}{2}e^{-jx}$, (2.38) becomes

$$S(t) = 1 + \frac{1}{2}e^{j\omega_0 t} + \frac{1}{2}e^{-j\omega_0 t}. \tag{2.39}$$

Compared with (2.2), the time-varying elastance can be written as

$$S(t) = S_0 + S_1 e^{j\omega_0 t} + S_1^* e^{-j\omega_0 t} \tag{2.40}$$

where $S_0 = 1$, $S_1 = \frac{1}{2}$, $S_1^* = \frac{1}{2}$, and all other coefficients are zero.

By applying (2.38) and the resultant Fourier coefficients S_0, S_1, and S_1^* in equation (2.7),

the two-port Z-matrix for a reactive doubler is expressed as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} R_s + \frac{S_0}{j\omega_0} & \frac{S_1^*}{j\omega_0} \\ \frac{S_1}{j2\omega_0} & R_s + \frac{S_0}{j2\omega_0} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \tag{2.41}$$

which has the input at the fundamental, i.e. V_1 and I_1, and only generates the output at the second harmonic, i.e. V_2 and I_2. The equation (2.41) of the two-port network yields the transducer conversion gain $G_{T,2}^{\text{react}}$ [1], such as

$$G_{T,2}^{\text{react}} = \frac{\frac{1}{2}|I_2|^2 \Re\{Z_\ell\}}{\frac{1}{8}|V_g|^2 \Re\{Z_g\}}. \tag{2.42}$$

With the source and load conditions (2.18) and (2.19), $G_{T,2}^{\text{react}}$ is calculated as

$$G_{T,2}^{\text{react}} = \frac{4R_g R_\ell |Z_{21}|^2}{|(Z_{11}+Z_g)(Z_{22}+Z_\ell) - Z_{12}Z_{21}|^2} \tag{2.43}$$

where $R_g = \Re\{Z_g\}$, and $R_\ell = \Re\{Z_\ell\}$. With the Z-parameters in (2.41), and assuming that the imaginary parts of Z_g and Z_ℓ cancel imaginary parts of Z_{11} and Z_{22} conjugately, i.e., $\Im\{Z_g\} = -\frac{S_0}{j\omega_0}$ and $\Im\{Z_\ell\} = -\frac{S_0}{j2\omega_0}$, $G_{T,2}^{\text{react}}$can be simplified as

$$G_{T,2}^{\text{react}} = \frac{4R_g R_\ell \frac{|S_1|^2}{2\omega_0^2}}{2|R_g R_\ell + \frac{|S_1|^2}{2\omega_0^2}|^2}. \tag{2.44}$$

When $R_g R_\ell = |S_1|^2 / (2\omega_0^2)$, the maximum efficiency of reactive doublers is estimated by $1/2$.

For reactive parametric triplers, the same procedure can be performed though it is more complex than for doublers, since the term of I_1^* is also involved in the V-I relations, which harms the symmetry of the Z-matrix. First the elastance from (2.34) is considered as

$$S(t) = 2\cos^2(\omega_0 t) = \cos(2\omega_0 t) + 1. \tag{2.45}$$

The Fourier series coefficients of this elastance are calculated $S_0 = 1$, $S_2 = \frac{1}{2}$, and $S_2^* = \frac{1}{2}$, and all other terms are zero. From (2.7), the Z-matrix of triplers is described as

$$\begin{bmatrix} V_1 \\ V_3 \end{bmatrix} = \begin{bmatrix} \frac{S_2}{j\omega_0} & R_s + \frac{S_0}{j\omega_0} & \frac{S_2^*}{j\omega_0} \\ 0 & \frac{S_2}{j3\omega_0} & R_s + \frac{S_0}{j3\omega_0} \end{bmatrix} \begin{bmatrix} I_1^* \\ I_1 \\ I_3 \end{bmatrix}. \tag{2.46}$$

Noticing that since only terms of fundamental and Nth harmonic are present, the idlers, such as V_2 and I_2, do not appear in (2.46). To solve for the conversion gain, the relation between I_1^* and I_1 needs to be obtained.

As a general case, the initial phase θ is added to the normalized

$$V(t) = \cos(\omega_0 t + \theta), \tag{2.47}$$

This way $S(t)$ becomes

$$S(t) = \cos(2\omega_0 t + 2\theta) + 1. \tag{2.48}$$

From Euler's formula, the same derivation gives

$$S_0 = 1 \tag{2.49}$$

$$S_2 = \frac{1}{2} e^{j2\theta} \tag{2.50}$$

$$S_2^* = \frac{1}{2} e^{-j2\theta}. \tag{2.51}$$

Therefore, the initial phase only has an influence on the phase (i.e. argument) of the complex S_2 and S_2^*. To simplify the analysis, the transient capacitance is used instead of elastance. Noticing that since the normalized capacitance ($C(t) \in [0,2]$) is the inverse of the

elastance, it can be approximately expressed as

$$C(t) = 1 - \cos(2\omega_0 t + 2\theta). \tag{2.52}$$

If R_s is ignored in (2.1), the voltage of varactor can be calculated as

$$v(t) = \int \frac{i(t)}{C(t)}\,\mathrm{d}t. \tag{2.53}$$

Therefore, the varactor current is calculated as

$$i(t) = C(t)\frac{\mathrm{d}\,v(t)}{\mathrm{d}t}. \tag{2.54}$$

By applying both (2.52) and (2.47), the total transient current can be solved as

$$i(t) = C(t)\,\omega_0 \sin(\omega_0 t + \theta) \tag{2.55}$$

$$i(t) = (1 - \cos(2\omega_0 t + 2\theta))\,\omega_0 \sin(\omega_0 t + \theta) \tag{2.56}$$

$$i(t) = -\frac{1}{2}\omega_0 \sin(3\omega_0 t + 3\theta) + \frac{3}{2}\omega_0 \sin(\omega_0 t + \theta). \tag{2.57}$$

With the interest on I_1 and I_1^*, the terms of $\sin(\omega_0 t + \theta)$ is investigated by using $\sin(x) = \frac{1}{2j}e^{jx} - \frac{1}{2j}e^{-jx}$, to get

$$I_1 = \frac{3}{4j}\omega_0 e^{j\theta} \tag{2.58}$$

$$I_1^* = -\frac{3}{4j}\omega_0 e^{-j\theta}. \tag{2.59}$$

With the termination condition

$$V_3 = -Z_\ell I_3 \tag{2.60}$$

and (2.46),

$$I_3 = \frac{-\frac{S_2}{j3\omega_0}}{R_s + Z_\ell + \frac{S_0}{j3\omega_0}} I_1, \tag{2.61}$$

the input impedance is calculated as

$$\Re\{Z_{in}\} = \Re\left\{\frac{V_1}{I_1}\right\} = \Re\left\{R_s + \frac{S_0}{j\omega_0}\right\} + \Re\left\{\frac{S_2}{j\omega_0}\frac{I_1^*}{I_1}\right\}$$

$$+ \Re\left\{\frac{|S_2|^2}{3\omega_0^2\left(R_s + Z_\ell + \frac{S_0}{j3\omega_0}\right)}\right\}. \tag{2.62}$$

Noticing that the only term with I_1^* is in the form of I_1^*/I_1,

$$\frac{I_1^*}{I_1} = -e^{-2j\theta} \tag{2.63}$$

and from (2.50),

$$\Re\left\{\frac{S_2}{j\omega_0}\frac{I_1^*}{I_1}\right\} = 0. \tag{2.64}$$

Therefore, in the calculation of the power gain of the tripler, I_1^* does not have an influence no matter the initial phase θ. Again, if R_s is neglected and Z_ℓ is impedance match via $\Im\{Z_\ell\} = -S_0/(j3\omega_0)$ in (2.61), the input impedance is calculated as

$$\Re\{Z_{in}\} = \frac{|S_2|^2}{3\omega_0^2 R_\ell}. \tag{2.65}$$

Then, the power gain of the tripler is expressed by

$$G_{P,3}^{\text{react}} = \frac{\frac{1}{2}|I_3|^2 R_\ell}{\frac{1}{2}|I_1|^2 \Re\{Z_{in}\}} = \frac{|I_3|^2 R_\ell}{|I_1|^2 \frac{|S_2|^2}{3\omega_0^2 R_\ell}} = \frac{1}{3}. \tag{2.66}$$

When the conjugate match is used at the input port, i.e., $R_g = \Re\{Z_{in}\} = |S_2|^2/\left(3\omega_0^2 R_\ell\right)$ with a cancellation of imaginary parts, the maximum transducer gain of the reactive triplers

is $G_{T,3}^{\text{react}} = G_{P,3}^{\text{react}} = 1/3$.

Note that (2.57) not only gives I_1 and I_1^*, but also I_3 and I_3^*, thereby it seemingly can be used to directly derive the relation for the harmonic generation. However, since the output is terminated by a load impedance, I_3 and I_3^* should be calculated by (2.7) with termination conditions. Since the ideal filters are used at both input and output ports in this configuration, the fundamental currents are almost not influenced by the load, and (2.57) can be used to determine the relations of I_1 and I_1^*.

Since the maximum theoretical efficiency is 1/2 and 1/3 for doublers and triplers, respectively, it can be expected that for any-order reactive parametric multipliers the maximum possible gain is $1/N$. The general expressions of frequency conversion power gain and transducer gain are derived next for any $N > 3$. By using the nonlinearity from (2.25), the time-varying elastance is written as

$$S(t) = \cos\left((N-1)\omega_0 t\right) + 1. \tag{2.67}$$

Only S_0, S_{N-1} and S_{N-1}^* are non-zero. Therefore the Z-matrix from (2.7) is

$$\begin{bmatrix} V_1 \\ V_N \end{bmatrix} = \begin{bmatrix} R_s + \frac{S_0}{j\omega_0} & \frac{S_{N-1}^*}{j\omega_0} \\ \frac{S_{N-1}}{jN\omega_0} & R_s + \frac{S_0}{jN\omega_0} \end{bmatrix} \begin{bmatrix} I_1 \\ I_N \end{bmatrix}. \tag{2.68}$$

The equation (2.68) can be applied to any order with $N > 3$ and $N = 2$. Only the triplers are special, since I_1^* is involved with the term of S_2, which is only non-zero when $N = 3$. With two-port network method with termination conditions, the general transducer gain can be written directly as

$$G_{T,N}^{\text{react}} = \frac{4R_g R_\ell \frac{|S_{N-1}|^2}{N\omega_0^2}}{N\left|R_g R_\ell + \frac{|S_{N-1}|^2}{N\omega_0^2}\right|^2}. \tag{2.69}$$

When $R_g = \Re\{Z_{in}\} = |S_{N-1}|^2 / \left(N\omega_0^2 R_\ell\right)$, the maximum $G_{T,N}^{\text{react}} = G_{P,N}^{\text{react}} = 1/N$.

To illustrate how to obtain $G_{P,N}^{\text{react}}$ in a general case, the steps are given in the following

derivation. From the expression of $G_{P,N}^{\text{react}}$ in (2.21) and Z_{in} in (2.16),

$$G_{P,N} = \frac{|I_N|^2 \Re\{Z_\ell\}}{|I_1|^2 \Re\{Z_{in}\}} = \frac{|I_N|^2 R_\ell}{|I_1|^2 \Re\left\{\sum_{m=-\infty}^{\infty} \frac{I_m}{I_1}\left(R_{1-m} + \frac{1}{j\omega_0} S_{1-m}\right)\right\}}. \tag{2.70}$$

Since it is an Nth-order multiplier, only I_1, I_1^*, I_N and I_N^* are preserved giving

$$G_{P,N} = \frac{|I_N|^2 R_\ell}{|I_1|^2 \Re\left\{R_0 + \frac{1}{j\omega_0} S_0 + \frac{I_1^*}{I_1}\left(R_2 + \frac{1}{j\omega_0} S_2\right) + \frac{I_N}{I_1}\left(R_{1-N} + \frac{1}{j\omega_0} S_{1-N}\right) + \frac{I_N^*}{I_1}\left(R_{N+1} + \frac{1}{j\omega_0} S_{N+1}\right)\right\}}. \tag{2.71}$$

For a reactive multiplier, resistance terms other than R_0 (i.e. R_s of the varactor) as well as the elastance term no less than Nth order are neglected,

$$G_{P,N}^{\text{react}} = \frac{|I_N|^2 R_\ell}{|I_1|^2 \Re\left\{R_s + \frac{1}{j\omega_0} S_0 + \frac{I_N}{I_1} \frac{1}{j\omega_0} S_{1-N}\right\}} \tag{2.72}$$

excluding the case when $N = 3$. Based on (2.68) and using the load termination condition,

$$V_N = \frac{1}{jN\omega_0} S_{N-1} I_1 + \left(\frac{1}{jN\omega_0} S_0 + R_s\right) I_N = -Z_\ell I_N, \tag{2.73}$$

with output matching condition

$$\Im\{Z_\ell\} = -\frac{S_0}{jN\omega_0}, \tag{2.74}$$

and neglecting the small R_s, the current relation can be obtained as

$$\frac{I_N}{I_1} = -\frac{S_{N-1}}{jN\omega_0 R_\ell}, \tag{2.75}$$

which is applied to (2.72) to get

$$G_{P,N}^{\text{react}} = \frac{|I_N|^2 R_\ell}{|I_1|^2 \Re\left\{-\frac{S_{N-1}}{jN\omega_0 R_\ell}\frac{1}{j\omega_0}S_{1-N}\right\}} = \frac{|I_N|^2 R_\ell}{|I_1|^2 \frac{|S_{N-1}|^2}{N\omega_0^2 R_\ell}} = \frac{1}{N} \tag{2.76}$$

knowing S_0 is real as a dc term.

Since in the process of the generation of the Nth harmonic only S_0, S_{N-1}, and S_{N-1}^* are non-zero, there is a straightforward relationship between S_{N-1} and Nth harmonic, which means that it is a natural result for SRPP to have the suppression of any other harmonics. The generation of other harmonics needs other order elastance to be efficiently generated, however, any S with an order other than $N-1$ and 0 are zero with SRPP. This feature is welcomed since it can reduce the requirements of filtering harmonics and improve the harmonic rejection significantly.

2.4.2 Pumped Capacitance with SRPP

The SRPP of capacitance follows the same rule as the pumped elastance, since the transient sine wave of the pumped capacitance is approximately an out-of-phase approach of the elastance in the time domain. Exactly speaking, in the previous subchapter, $S(t)$ is normalized to [0, 2], which means the actual inverse belongs to [0.5, ∞] and is difficult to handle in practice. Therefore, to simplify the analysis, the range of $C(t)$ is also normalized to [0, 2] without changing the basic characteristics of the parametric generation process, i.e. in one period of pumping the time-varying capacitance experiences $N-1$ periods. Under this pumping condition, the total efficiency can be calculated in the same way as the elastance with non-zero S_0, S_{N-1}, and S_{N-1}^*. Although the pumped capacitance can generate other non-ideal coefficients of elastance under sinusoidal pumping voltage, these three terms are dominant, and others are insignificant in this pumped capacitance approach. Therefore the sinusoidal pumped capacitance should have a similar performance when operating in parametric multipliers.

For example, considering (2.33) as the simple case of variable capacitance for the frequency doubling,

$$C(t) = \cos(\omega_0 t) + 1, \tag{2.77}$$

which is driven by the pump voltage in (2.22) with R_s neglected. By applying Euler's formula $\cos(x) = \frac{1}{2}e^{jx} + \frac{1}{2}e^{-jx}$, (2.77) can be rewritten as $C(t) = 1 + \frac{1}{2}e^{j\omega_0 t} + \frac{1}{2}e^{-j\omega_0 t}$ to obtain $C_0 = 1$, $C_1 = 1/2$, $C_1^* = 1/2$, and all other Fourier coefficients of C are zero. The same method can be used to do the analysis for the reactive multipliers with the pumped capacitance with SRPP as for the pumped elastance. Under the pump voltage of (2.22), and neglecting parallel resistance G_p, the Y-matrix from (2.13) can be used for the parametric doublers with (2.77).

To create a $\cos(2\omega_0 t)$ term in $C(t)$ of the reactive triplers, (2.34) is employed as

$$C(t) = 2\cos^2(\omega_0 t) = \cos(2\omega_0 t) + 1. \tag{2.78}$$

As shown in (2.57) of the pumped elastance, $C(t)$ in the form of $\cos(2\omega_0 t)$ can generate the third harmonic, as required for the idler-less frequency tripler.

For a frequency multiplier with $N > 3$, the normalized transient capacitance is assumed to have the form of

$$C(t) = 1 + 2|C_{N-1}|\cos((N-1)\omega_0 t) \tag{2.79}$$

where $C_0 = 1$, and $|C_{N-1}| \approx \frac{1}{4}(C_{max} - C_{min})$ as [19].

As the nonlinear P-V curves reported in Fig. 2.2, in one period of the pumping, e.g. the pump voltage in the form of $\cos(\omega_0 t)$ transits from 1 to −1 V, and then back to 1 V, the time-varying capacitance has total $N-1$ periods for the Nth-order harmonic generation, which is shown in Fig. 2.3 for the harmonic generation with an order from the fundamental to the sixth, showing the capacitance dependence on the phase of the pump voltage $\cos(\omega_0 t)$ in one period (a total phase of 2π).

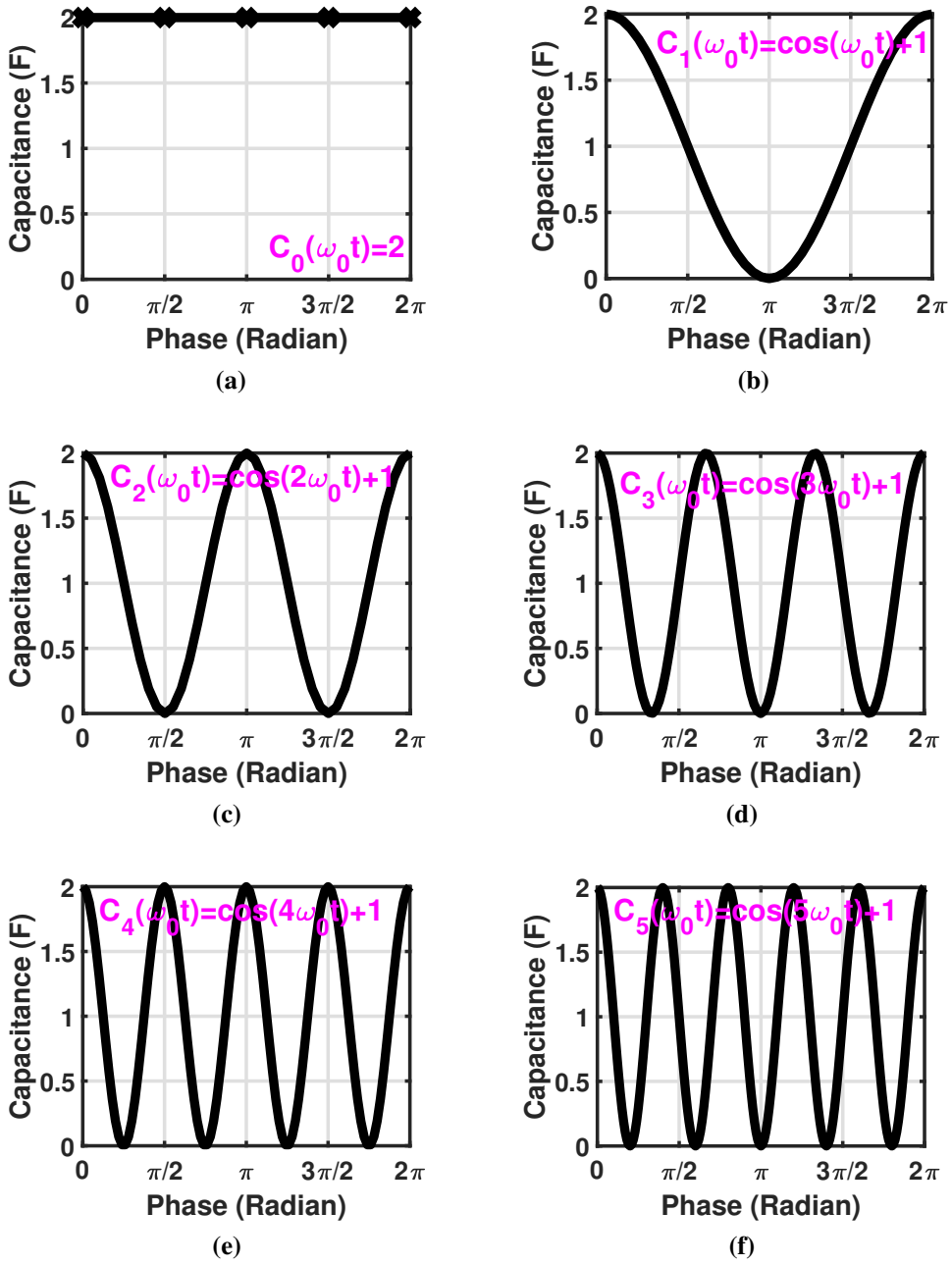


Figure 2.3: Periodic transient capacitance of the varactors with normalized C-V curves versus the phase of the pump voltage for (a) fundamental, (b) second-order, (c) third-order, (d) fourth-order, (e) fifth-order, and (f) sixth-order harmonic generation.

2.4.3 Pumped Conductance with SRPP

Pumped conductance with SRPP can be utilized in the similar way as the pumped elastance or capacitance, i.e., the frequency multiplication can be realized by using a nonlinear device

with time-varying conductance or resistance. In practice, the resistive multipliers are built with Schottky barrier diodes. The model of a varactor is usually in series topology, such as a variable capacitor in series with an R_s, whereas Schottky diodes are modeled in parallel, such as in [43], therefore the pumped conductance and Y-matrix from (2.13) can be used for the analysis of the resistive multipliers. As discussed in Section 1.3.1, to simplify the analysis of resistive multipliers and avoid the hybrid operation, the parallel parasitic capacitance C_p is assumed to be constant, so that the only time-varying parameter is the variable conductance $G(t)$. The analysis and calculation of gains of SRPP of conductance is identified in a similar fashion as was described for the SRPP of elastance or capacitance. In one pump period, $G(t)$ experiences $N-1$ periods to have non-zero G_0, G_{N-1}, and G_{N-1}^*, for the Nth-order harmonic generation. To avoid repetitive derivation procedures, the derivation of the gain expressions of the resistive multipliers are given with the pumped resistance with SRPP in Section 2.4.4, assuming the parasitic C_p is small and can be neglected.

Since the variable conductance or resistance are utilized, the resistive multipliers are always lossy, but they can operate in the wide bandwidth since the variable parameters do not change with the frequency ideally.

2.4.4 Pumped Resistance with SRPP

In the analysis of the reactive multipliers, it can be seen that it is more convenient to use the pumped capacitance over the pumped elastance, since capacitance is more commonly used in the modeling, and the value of capacitance is tiny in modern technologies, whereas the elastance is extremely large in size. The similar situation also happens in the pumped resistance of SRPP, and the Z-matrix from (2.7) is used together with (2.25) to get the required time-varying resistance for the harmonic generation, which is expressed as

$$R(t) = 1 + 2\,|R_{N-1}| \cos\left((N-1)\,\omega_0 t\right). \tag{2.80}$$

Again, only R_0, R_{N-1}, and R_{N-1}^* are non-zero as derived from (2.80). With only keeping the variable resistance terms, the Z-matrix from (2.7) becomes

$$\begin{bmatrix} V_1 \\ V_N \end{bmatrix} = \begin{bmatrix} R_0 & R_{N-1}^* \\ R_{N-1} & R_0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_N \end{bmatrix} \tag{2.81}$$

for $N > 3$ and $N = 2$. For $N = 3$, I_1^* is involved and it is discussed separately. With the two-port network and the termination conditions, the frequency conversion transducer gain can be directly derived as

$$G_{T,N}^{\text{resist}} = \frac{4R_g R_\ell \left|R_{N-1}\right|^2}{\left(\left(R_0+R_g\right)\left(R_0+R_\ell\right) - \left|R_{N-1}\right|^2\right)^2}. \tag{2.82}$$

To derive the conversion power gain, (2.70) is used with ignoring the elastance terms as

$$G_{P,N}^{\text{resist}} = \frac{\left|I_N\right|^2 R_\ell}{\left|I_1\right|^2 \Re\left\{R_0 + \frac{I_1^*}{I_1}R_2 + \frac{I_N}{I_1}R_{1-N}\right\}} \tag{2.83}$$

where

$$Z_{in}^{\text{resist}} = R_0 + \frac{I_1^*}{I_1}R_2 + \frac{I_N}{I_1}R_{1-N}. \tag{2.84}$$

For $N \neq 3$, $R_2 = 0$,

$$G_{T,N}^{\text{resist}} = \frac{\left|I_N\right|^2 R_\ell}{\left|I_1\right|^2 \Re\left\{R_0 + \frac{I_N}{I_1}R_{1-N}\right\}}. \tag{2.85}$$

From (2.81) with the load termination condition

$$V_N = R_{N-1}I_1 + R_0 I_N = -Z_\ell I_N. \tag{2.86}$$

With $Z_\ell = R_\ell$,

$$\frac{I_N}{I_1} = -\frac{R_{N-1}}{R_\ell + R_0} \tag{2.87}$$

can be applied to (2.85) to get

$$G_{P,N}^{\text{resist}} = \frac{|I_N|^2 R_\ell}{|I_1|^2 \Re\left\{R_0 - \frac{|R_{N-1}|^2}{R_\ell + R_0}\right\}} \tag{2.88}$$

$$G_{P,N}^{\text{resist}} = \frac{|R_{N-1}|^2 R_\ell}{(R_\ell + R_0)\left((R_\ell + R_0)R_0 - |R_{N-1}|^2\right)}. \tag{2.89}$$

When the input match fulfills

$$R_g = R_0 - \frac{|R_{N-1}|^2}{R_\ell + R_0}, \tag{2.90}$$

the $G_{T,N}^{\text{resist}}$ can be equal to $G_{P,N}^{\text{resist}}$.

For $N = 3$, like for the reactive case discussed previously, using $V(t) = \cos(\omega_0 t + \theta)$, the time-varying

$$R(t) = 2\cos^2(\omega_0 t + \theta) = \cos(2\omega_0 t + 2\theta) + 1 \tag{2.91}$$

has the general expression of R_2 as

$$R_2 = |R_2| e^{j2\theta}. \tag{2.92}$$

For the convenience of calculation of the current, normalized $G(t)$ is assumed to have the form approximately, as

$$G(t) = 1 - \cos(2\omega_0 t + 2\theta). \tag{2.93}$$

The transient current can be calculated as

$$i(t) = G(t)V(t) = -\cos(2\omega_0 t + 2\theta)\cos(\omega_0 t + \theta) + \cos(\omega_0 t + \theta) \tag{2.94}$$

$$i(t) = -\frac{1}{2}\cos(3\omega_0 t + 3\theta) + \frac{1}{2}\cos(\omega_0 t + \theta). \tag{2.95}$$

Therefore

$$I_1 = |I_1|e^{j\theta} \tag{2.96}$$

$$I_1^* = |I_1|e^{-j\theta} \tag{2.97}$$

then

$$\frac{I_1^*}{I_1}R_2 = |R_2|. \tag{2.98}$$

The conversion power gain of resistive triplers can be derived from (2.83), as

$$G_{P,3}^{\text{resist}} = \frac{|R_2|^2 R_\ell}{(R_\ell + R_0)\left((R_\ell + R_0)(R_0 + |R_2|) - |R_2|^2\right)} \tag{2.99}$$

and the conversion transducer gain of the resistive triplers is derived as

$$G_{T,3}^{\text{resist}} = \frac{4R_g R_\ell |R_2|^2}{\left((R_0 + |R_2| + R_g)(R_0 + R_\ell) - |R_2|^2\right)^2}. \tag{2.100}$$

2.5 Impulse Representation of Pumped $P(t)$ (IRPP)

2.5.1 Pumped Resistance with IRPP

For varactors in reactive multipliers, the ratio of maximum to minimum capacitance is usually limited, such as 2 to 3 from a conventional MOS varactor, which is used for SRPP. However, for the varistors in the resistive multipliers, since the varying resistance behaves like a switch, i.e., when the diode is turned on, it has a low on resistance R_{ON} (about several or tens Ω), whereas it has a very high impedance (larger than MΩ) or a nearly open circuit when it is turn off. On and off states of diodes are only controlled by the voltage across

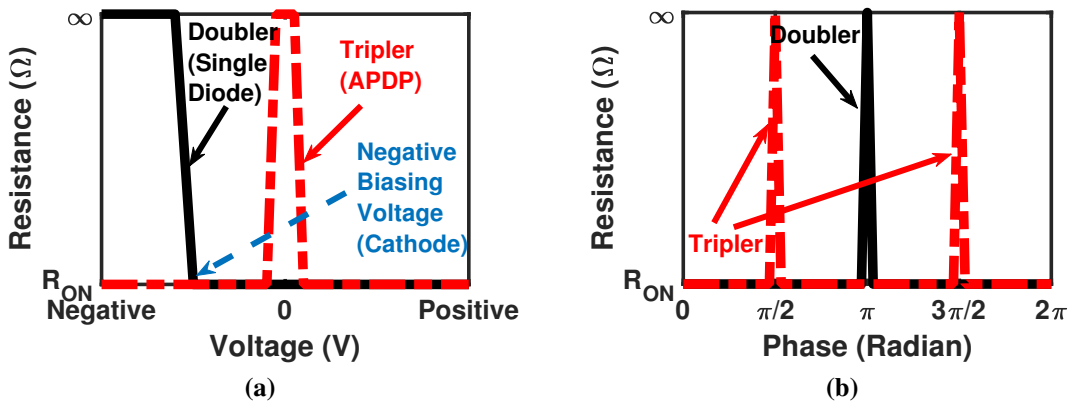


Figure 2.4: Illustrations of IRPP (a) R-V curves of the piecewise approach and (b) periodic transient impulse resistance of a single diode (forward biased with a dc voltage) for doublers, and an APDP for triplers. The curves are not to scale.

their two terminals, which is just the input pump voltage $V(t)$. With a simple piecewise approach of asymptotes, it can be modeled that the time-varying resistance varies from R_{ON} to infinity, which is very different from the SRPP, which has a limited ratio of variable parameters, and does not become infinity.

The next step is to investigate the R-V curves of the diodes for resistive FMs. The resistive doubler is realized with a single diode, which has a monotonic R-V curve [34]. Only when the forward biasing voltage of the diode is larger than the turn on voltage (V_{ON}), the diode is on with low R_{ON} as per the piecewise model. For a tripler, an antiparallel-diode pair (APDP) with symmetric "one-peak" R-V curve is used [32, 33]. Similarly, when the voltage (absolute value) is less than V_{ON}, the APDP is off with infinite resistance ideally, otherwise it is on with small R_{ON}. The two typical R-V curves are shown in the Fig. 2.4(a), which are not to the scale.

Before diving into the analysis of the impulse-like variable parameters, it is noted that since infinity is involved in the process of the harmonic generation, a mathematics approach for analyzing such circuits is required. To avoid infinite numbers in the calculation of Fourier coefficients, the width of the peak is assumed be very narrow thereby approximating pulses. This is reasonable when the pumping is strong, which is true for parametric

circuits. The total pump voltage is much larger than V_{ON}, making the "duty cycle" of the pulses very small, which results in an impulse representation of pumped $P(t)$ (IRPP). Since the width of the impulse is narrow, in such situations, rather than using sinusoids for the analysis, a train of Dirac delta functions $\delta(t)$ can be employed, which is shown in Fig. 2.4(b) for doubler with a single diode and triplers with the APDP. Since the width of the infinite-height pulse is narrow, the integration of one $\delta(t)$ is unity, which is solvable for the Fourier coefficients of IRPP.

The transient representation of the impulse-like resistance is a periodic superposition of the delta functions at the instance τ_i, which is expressed as

$$R_i(t) = A_i \sum_{n=-\infty}^{\infty} \delta(t - nT - \tau_i) \tag{2.101}$$

where T is the period of the pump signal, A_i is an amplitude coefficient of the delta function, and i represents impulse, not a number of coefficients. The total transient resistance is then modeled as

$$R(t) = R_i(t) + R_{\mathrm{ON}}. \tag{2.102}$$

For a doubler with a forward-biased diode (i.e. a negative dc voltage is biased at the cathode of the diode) as shown in Fig. 2.4(a), the large resistance when the diode is off is repeated at $1T/2$, $3T/2$, $5T/2$, etc., under pumping of $\cos(\omega_0 t)$. As such, there is only one peak in one period of pumping, and the spacing of the peaks is 2π, i.e., the period of the pump voltage. The transient $R(t)$ can be written in terms of phase as

$$R(t) = A_i \sum_{n=-\infty}^{\infty} \delta(\omega_0 t - 2n\pi - \pi) + R_{\mathrm{ON}}. \tag{2.103}$$

The dc Fourier coefficient R_0 from the impulse can be calculated via

$$R_0 = \frac{A_i}{2\pi} \int_0^{2\pi} R_i(t)\, \mathrm{d}(\omega_0 t) + R_{ON} = \frac{A_i}{2\pi} + R_{\mathrm{ON}}. \tag{2.104}$$

The non-dc even- and odd-order Fourier coefficients of $R(t)$ are calculated as

$$R_{\text{even}} = \frac{A_i}{2\pi}, \tag{2.105}$$

$$R_{\text{odd}} = -\frac{A_i}{2\pi}, \tag{2.106}$$

respectively.

The impulse of resistance of the resistive triplers with APDP occurs at $1T/4$, $3T/4$, $5T/4$, $7T/4$, etc., i.e. in each pump period of $\cos(\omega_0 t)$ there are two peaks, and the time intervals between the peaks are equal to $T/2$. In terms of phase, the impulse of APDP under pumping occurs at $\pi/2$, $3\pi/2$, $5\pi/2$, $7\pi/2$, etc., and the phase intervals are π. The transient resistance of APDP can be written as

$$R(t) = A_i \sum_{n=-\infty}^{\infty} \delta\left(\omega_0 t - n\pi - \frac{\pi}{2}\right) + R_{\text{ON}}. \tag{2.107}$$

For triplers,

$$R_0 = \frac{A_i}{\pi} + R_{\text{ON}}, \tag{2.108}$$

$$R_{4,8,12\ldots} = \frac{A_i}{\pi}, \tag{2.109}$$

$$R_{2,6,10\ldots} = -\frac{A_i}{\pi}. \tag{2.110}$$

All other terms are zero.

Comparing doublers and triplers, it can be concluded that in each pumping period, the number of peaks is $N-1$, and the peaks are equally spaced in time or phase, resulting in $2\pi/(N-1)$ spacing. As a general rule, to generate the Nth harmonic with resistive multipliers, it is necessary to have $N-1$ pulses of transient resistance or conductance under one period of pumping, with equal time or phase interval. The resultant Fourier coefficients

are calculated and summarized as

$$R_0 = \frac{(N-1)A_i}{2\pi} + R_{\mathrm{ON}} \tag{2.111}$$

and

$$R_{(2u+1)(N-1)} = -\frac{(N-1)A_i}{2\pi} \tag{2.112}$$

$$R_{(2u+2)(N-1)} = \frac{(N-1)A_i}{2\pi} \tag{2.113}$$

where $u \in \mathbb{Z}$ is introduced for representing Fourier coefficients in multiples of $N-1$ under pumping of $\cos(\omega_0 t)$. All other coefficients of R are zero. It can be observed that the non-zero coefficients are spaced with more and more zeros (equal to $N-2$) when N becomes larger. By applying different u, all non-zero coefficients of R are found, among them the most important one is the R_{N-1} when $u = 0$, and its conjugate R^*_{N-1}.

The biasing of the diodes or APDP has an important influence to the resistive multiplication with IRPP. For a forward-biased single diode, if the biasing is zero voltage, and V_{ON} is small, then the resistance in half of the period is infinity and in the other half is low, which violates the assumption of IRPP. To make sure that the impulse is narrow, a negative voltage can be connected to the cathode of the diode to realize the R-V curve for the doubler shown in Fig. 2.4(a). If the pump voltage is too large in the negative direction, it can make the width of the pulse too wide and the integration of infinity difficult; therefore, the full pumping condition should be carefully chosen to make sure that the narrow impulse occurs. In this case, the reactive component, i.e. the parasitic capacitance can be neglected. During most period of the pumping cycle, i.e., the pumping voltage traverses from positive to negative, and then back to positive, the R_{ON} is low or even close to short circuit, except at the negative point where the impedance significantly changes to infinity. At these impulse points, the transient voltage change does not change the current, since $V(t)$ is in the form of $\cos(\omega_0 t)$, and $I(t) = C\,\mathrm{d}V/\mathrm{d}t = -C\omega_0 \sin(\omega_0 t)$, which is exactly zero at π, 3π, 5π, etc.,

which are the locations of the pulses in Fig. 2.4(b) for doublers. Therefore the influence of the parallel capacitance does not matter, i.e., the current and voltage are always in phase since the capacitive terms are ignored, and the circuit is purely resistive.

This feature is seemingly not so important for resistive doublers, but is critical for the triplers, since the pulses happen at $\pi/2$, $3\pi/2$, $5\pi/2$, etc., which means $\mathrm{d}V/\mathrm{d}t$ is not zero, and there is some phase difference from 0 to 90 degrees between the current and voltage. The phase difference between current and voltage makes it complex for the analysis, and as discussed in the previous chapter, in this work about the parametric generation theory, the hybrid process of both varying reactance and resistance is not discussed. Therefore, the parallel capacitance of APDP is also neglected in the analysis, making the current and voltage always in-phase in the analysis. The influence of the small reactive terms in APDP triplers on the analysis of the efficiency with IRPP is insignificant since only a constant reactive term is added as in (2.14), which is ignored in this analysis of the resistive harmonic generation. An equivalent replacement for the APDP tripler can be described to have two peaks at the negative and positive boundaries of the pumping as shown in Fig. 2.5(a), to replace the one peak at zero voltage in R-V. With this modification to the R-V curve, the pulses now occur at 0, π, 2π, 3π, etc., instead of $\pi/2$, $3\pi/2$, $5\pi/2$, $7\pi/2$, etc., under the same pumping $\cos(\omega_0 t)$, to make sure that the current calculated by $\mathrm{d}V/\mathrm{d}t$ in the form of $\sin(\omega_0 t)$ is always zero at these time instances, as shown in Fig. 2.5(b). Notice that the presence of pulses at 0, π, 2π, 3π, etc. instead of $\pi/2$, $3\pi/2$, $5\pi/2$, $7\pi/2$, etc., is not a simple phase shift of the initial phase of the pumping. If only the initial phase is changed, $V(t)$ is changed from $\cos(\omega_0 t)$ to $\sin(\omega_0 t)$ changing the form of dV/dt from $\sin(\omega_0 t)$ to $\cos(\omega_0 t)$, and at 0, π, 2π, 3π, etc., $\mathrm{d}V/\mathrm{d}t$ is non-zero, which still causes the phase shift between currents and voltages, and is not desired for the pumping analysis.

The transient resistance of the equivalent APDP can be written as

$$R(t) = A_i \sum_{n=-\infty}^{\infty} \delta(\omega_0 t - n\pi) + R_{\mathrm{ON}}. \tag{2.114}$$

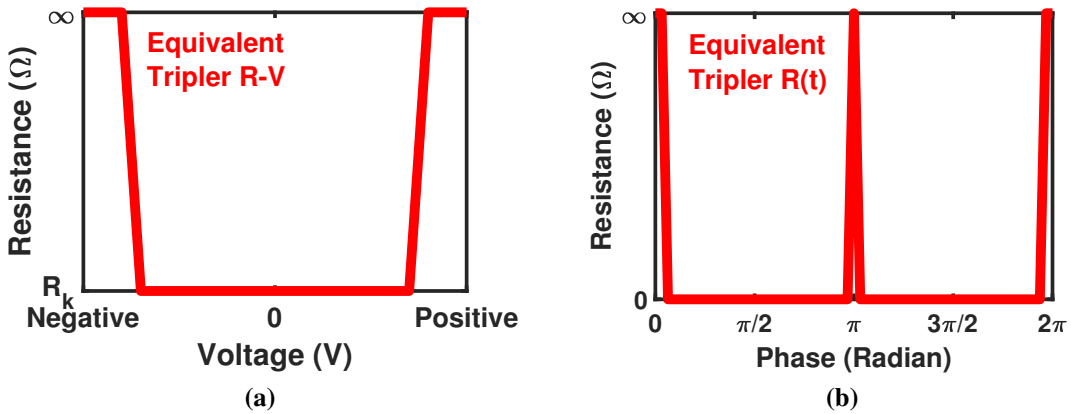


Figure 2.5: Illustrations of equivalent APDP tripler with IRPP under pumping of $\cos(\omega_0 t)$ (a) equivalent R-V curve of the piecewise approach and (b) periodic transient impulse resistance of the equivalent APDP. The curves are not to scale.

For the equivalent APDP ,

$$R_0 = \frac{A_i}{\pi} + R_{\text{ON}}, \tag{2.115}$$

$$R_{\text{even}} = \frac{A_i}{\pi}, \tag{2.116}$$

and all other terms are zero.

Whereas the SRPP represents a time-varying parameter with limited ratio approaching sine waves, the IRPP represents a switched time-varying parameter changing between on and off. From this point of view, SRPP is like an "analog" representation with sinusoidal waveform, whereas IRPP is like a "digital" representation with only two switched states. However, they have the similarity in the parametric harmonic generation. For SRPP to generate the Nth harmonic, the pumped parameters should exhibit $N-1$ periods within one pump period, whereas for IRPP to generate the Nth harmonic, the number of delta functions are $N-1$ within one period of the pump signal, and their locations in the transient waveform plot are equally spaced. The specific calculation process for the derivation of the efficiencies of the resistive multipliers are given in Section 2.5.2.

2.5.2 Calculated Efficiencies of IRPP

The calculation of resistive multipliers with IRPP is similar to the derivation with SRPP, but with more non-zero Fourier coefficients. With the Z-matrix from (2.7), the doubler can be represented by

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_3 & R_2 & R_0 & R_1^* \\ R_4 & R_3 & R_1 & R_0 \end{bmatrix} \begin{bmatrix} I_2^* \\ I_1^* \\ I_1 \\ I_2 \end{bmatrix}. \tag{2.117}$$

By applying (2.104) to (2.106), the doubler equation becomes

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} -\frac{A_i}{2\pi} & \frac{A_i}{2\pi} & \frac{A_i}{2\pi} + R_{\mathrm{ON}} & -\frac{A_i}{2\pi} \\ \frac{A_i}{2\pi} & -\frac{A_i}{2\pi} & -\frac{A_i}{2\pi} & \frac{A_i}{2\pi} + R_{\mathrm{ON}} \end{bmatrix} \begin{bmatrix} I_2^* \\ I_1^* \\ I_1 \\ I_2 \end{bmatrix}. \tag{2.118}$$

Since all reactive terms are neglected, all the elements in the Z-matrix are real. Given that $V(t)$ is in the form of $\cos(\omega_0 t)$, it is acceptable to assume that all terms of V and I are all real under the termination condition

$$V_2 = -R_\ell I_2. \tag{2.119}$$

Therefore, with $I_1 = I_1^*$, and $I_2 = I_2^*$, the Z-matrix (2.118) becomes

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{A_i}{\pi} + R_{\mathrm{ON}} & -\frac{A_i}{\pi} \\ -\frac{A_i}{\pi} & \frac{A_i}{\pi} + R_{\mathrm{ON}} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{2.120}$$

For the triplers, the similar process can be performed with the equivalent models of the

APDP. From (2.7), the tripler has a Z-matrix as

$$\begin{bmatrix} V_1 \\ V_3 \end{bmatrix} = \begin{bmatrix} R_4 & R_2 & R_0 & R_2^* \\ R_6 & R_4 & R_2 & R_0 \end{bmatrix} \begin{bmatrix} I_3^* \\ I_1^* \\ I_1 \\ I_3 \end{bmatrix}. \tag{2.121}$$

With the calculated coefficients of R from (2.115) and (2.116), the Z-matrix can be written as

$$\begin{bmatrix} V_1 \\ V_3 \end{bmatrix} = \begin{bmatrix} \frac{A_i}{\pi} & \frac{A_i}{\pi} & \frac{A_i}{\pi} + R_{\mathrm{ON}} & \frac{A_i}{\pi} \\ \frac{A_i}{\pi} & \frac{A_i}{\pi} & \frac{A_i}{\pi} & \frac{A_i}{\pi} + R_{\mathrm{ON}} \end{bmatrix} \begin{bmatrix} I_3^* \\ I_1^* \\ I_1 \\ I_3 \end{bmatrix}. \tag{2.122}$$

Again, with the load termination condition and $V(t)$ in the form of $\cos(\omega_0 t)$, all terms of V and I are assumed to be real, and therefore

$$\begin{bmatrix} V_1 \\ V_3 \end{bmatrix} = \begin{bmatrix} \frac{2A_i}{\pi} + R_{\mathrm{ON}} & \frac{2A_i}{\pi} \\ \frac{2A_i}{\pi} & \frac{2A_i}{\pi} + R_{\mathrm{ON}} \end{bmatrix} \begin{bmatrix} I_1 \\ I_3 \end{bmatrix}. \tag{2.123}$$

From (2.7) it is known that the conjugates of current terms are involved in the calculation of the efficiency of the Nth harmonic generation when Fourier coefficients with orders of 2, $N+1$, and $2N$ are non-zero. The Fourier coefficients of IRPP are more complex than those of the SRPP since only 0 and $(N-1)$th orders of Fourier coefficients are non-zero for the SRPP but all orders at multiples of $N-1$ are non-zero for the IRPP from (2.112) and (2.113). For any $N > 3$, 2 and $N+1$ cannot be multiples of $N-1$. Since N and $N-1$ are relatively prime, $2N$ cannot be multiples of $N-1$, when $N > 3$. Therefore, for the Nth harmonic generation, the Z-matrix of IRPP is

$$\begin{bmatrix} V_1 \\ V_N \end{bmatrix} = \begin{bmatrix} \frac{(N-1)A_i}{2\pi} + R_{\mathrm{ON}} & -\frac{(N-1)A_i}{2\pi} \\ -\frac{(N-1)A_i}{2\pi} & \frac{(N-1)A_i}{2\pi} + R_{\mathrm{ON}} \end{bmatrix} \begin{bmatrix} I_1 \\ I_N \end{bmatrix}. \tag{2.124}$$

The general expression of the frequency conversion gain of the multiplier with IRPP $G_{Ti,N}^{\mathrm{resist}}$ can be written as

$$G_{Ti,N}^{\mathrm{resist}} = \frac{4R_g R_\ell D^2}{\left(\left(D + R_{\mathrm{ON}} + R_g\right)\left(D + R_{\mathrm{ON}} + R_\ell\right) - D^2\right)^2} \tag{2.125}$$

where $D = \frac{A_i}{\pi}$ for $N = 2$, $D = \frac{2A_i}{\pi}$ for $N = 3$, and $D = \frac{(N-1)A_i}{2\pi}$ for $N > 3$. The power gains can be derived in exactly the same way as for the SRPP and is not repeated here.

One interesting observation may be made for the infinite, equal in the absolute value, and non-zero Fourier coefficients of R with the IRPP. SRPP only has dc and P_{N-1} non-zero terms, whereas IRPP, such as shown in (2.112) and (2.113), has an infinite number of Fourier coefficients of R with the order of multiples of $N-1$. For example, in a doubler with a single diode, any-order R_k is non-zero. As such, seemingly with ideal filters, it can be used to generate any-order harmonic, just based on the single diode doubler. Furthermore, since any high-order R_ks are equal in the absolute value as (2.105) and (2.106), it can be used to build any-order idler-less resistive multipliers with the same efficiency. The same phenomenon also occurs for the resistive triplers to generate any odd-order harmonics. However, it is not practical to generate any high-order harmonic with sufficient output power with only one diode or APDP. A single nonlinear device can generate an infinite order of harmonics, such as a diode, but when the order becomes high, the high-order Fourier coefficients of R_ks are decreased accordingly. The calculated $|R_k|$s are equal only due to the impulse delta function used in the model. Only when the $R(t)$ of IRPP is ideally in the form of impulse described by the delta function, the single diode can generate the infinite number of equal $|R_k|$s. Therefore a more realistic square-wave approximation of $R(t)$ should be used to replace the delta function, with finite height and width of the pulses,

to simulate the switched on and off states of the varying resistance. The analysis with the square wave shows that the $|R_k|$ is reduced as N increased, and when the width of the square wave is reduced to a small value, it is equivalent to the IRPP.

2.6 Discussions on Efficiencies of Parametric Multipliers

2.6.1 Reactive Multipliers

For passive multipliers, the power gains are less than unity, and can be viewed as the circuit efficiency. As theoretically predicted by Manley-Rowe relations [4], the maximum conversion efficiency (i.e., the frequency conversion power gain when all the harmonic power is delivered to the load) of a lossless reactive multiplier can reach 100% ideally, for $N = 2$ without idlers and $N > 2$ with one or more idlers [19]. However, this 100% efficiency only exists in the calculation of the reactive multipliers, not in simulations or measurements. One key limitation is the series resistance R_s of the varactor, which both limits the dynamic cutoff frequency and makes the lossless assumption less valid.

One interesting problem is that the SRPP can always provide a maximum power gain of $1/N$, even if with the zero R_s under the proposed idler-less pumping condition, which is much less than the ideal 100%. It is instructive to discuss how the conventional pumping provides ideally calculated (though not in real circuits or simulation) 100% efficiency, and the difference between the conventional pumped parameters and the SRPP of the reactive parametric multipliers. As shown in Section 2.3, in the SRPP only P_0, P_{N-1}, and P^*_{N-1} coefficients of the time-varying $P(t)$ are non-zero under pumping, which makes a straightforward way to generate the required harmonic while suppressing all other harmonics. In conventional pumping with diode varactors as shown in [19], higher order of pumped parameters exist in the parametric process. For example, in a reactive doubler, the SRPP only requires that S_0, S_1, and S^*_1 are non-zero, whereas in a conventional parametric theory, S_2 is also non-zero. In the theory of this work, S_2 is related to the third harmonic and is not used; however, in conventional diode-varactor doublers, having non-zero S_2 permits current term

$\frac{S_2}{j\omega_0} I_1^*$ to contribute to the output voltage and increase $G_{P,2}^{\text{react}}$ from 1/2 to 1. Although more non-zero Fourier coefficients may possibly increase the efficiency, it introduces more harmonics or idlers, and may not be practical or easily realizable for modern MOS varactors. The mm-wave diode doublers demonstrate a much less than 100% efficiency experimentally, such as less than 30% in [51, 52], 33% with conventional diode varactor in [53]. An interesting cryogenic doubler shows 48% efficiency at room temperature, whereas the efficiency increases to 61% at 14 Kelvins in [54], which indicates that the series parasitic R_s should be a critical limiting factor in obtaining the high efficiency of the multipliers.

To evaluate the influence of the R_s and the ratio of the capacitance, the dynamic cutoff frequency f_{cd} is commonly used for varactors in parametric circuits. It is shown that the nearly 100% efficiency only occurs at a very low relative frequency, i.e. less than 0.1% of f_{cd}. When the input frequency f_0 increases from 0.1% to 10% of f_{cd}, the maximum calculated efficiency drops from 98% to 20% [19]. Since nowadays parametric circuits are commonly used in the high-frequency range, the performance with frequency less than 0.1% f_{cd} is not of interest.

For a parametric tripler, the maximum calculated efficiency is also about 100%, if a second-harmonic idler circuit is used, and the tripler operates below 0.1% f_{cd} [19, Fig. 8.17, p. 350]. This 100% efficiency, however, is not attainable in the real parametric triplers. So far, the experimentally verified high-frequency parametric multipliers are reported to be limited to ~5% of a sub-THz heterostructure-barrier-varactor (HBV) tripler [55] and < 1% of an HBV THz quintupler [56]. The ideal calculated efficiency of the single-varactor tripler with an idler is compared with the calculated and simulated curves based on the SRPP, and a calculated reference curve from a symmetrical quantum-barrier varactor (S-QBV) tripler [21], as shown in Fig. 2.6. The S-QBV has a symmetric C-V curve and can operate at 1% f_{cd} to have a near ~100% calculated efficiency. Base on the comparison shown in Fig. 2.6, the calculated efficiency of the tripler with a symmetric C-V curve in [21] is actually better than a conventional single-varactor tripler when the relative

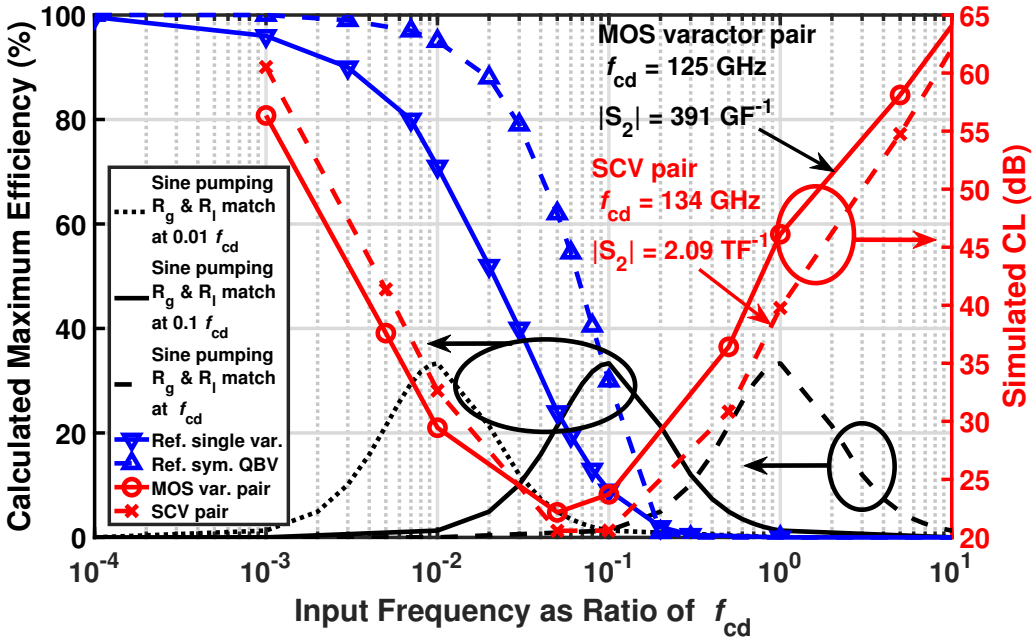


Figure 2.6: The calculated maximum efficiencies of SRPP under sinusoidal pumping with impedance matching conditions at $f_0 = 0.01 f_{cd}$, $0.1 f_{cd}$, and $1 f_{cd}$, respectively, as well as the reference maximum efficiencies, which are calculated by using conventional methods in [19] for a single-varactor tripler with a second-harmonic idler circuit, and in [21] for an S-QBV tripler. Simulated CL for triplers employing MOS varactor and SCV pairs are also shown.

frequency becomes high. In the case of the SRPP, the maximum calculated efficiency is 1/3, or about 33% at about 10% f_{cd}, which is almost the same as the calculated value from [21], which shows that for triplers the idler-less efficiency is not worse than the efficiency calculated by the conventional transient method in [21], and much better than the efficiency based on a conventional single-varactor with idlers in [19] in a high relative frequency range. The calculation of the efficiency with the SRPP is based on the input matching $\Re\{Z_{in}\} = R_g = |S_2|^2 / \left(3\omega_0^2 R_\ell\right)$ as in Section 2.4.1, at frequencies of $\omega_0/2\pi = 0.01 f_{cd}$, $0.1 f_{cd}$, and $1 f_{cd}$, respectively. Since the matching is obtained at frequency ω_0, the efficiency is frequency dependent. In summary, increasing r_c from a small value can improve the conversion efficiency with larger $|S_{N-1}|$ as well as push the matching frequency to a higher value; however, f_{cd} should be taken into consideration with R_s when the matching frequency becomes high and close to f_{cd} , thereby the relationship between efficiency,

matching, r_c, and f_{cd} is not straightforward.

Although it appears that the calculated curve when matched at f_{cd}, could show much better efficiency than the conventionally calculated efficiency, it should be treated as an artificial result. Although f_{cd} is not present in the equations of efficiencies of the reactive multipliers, such as in (2.69), f_{cd} is still a limiting factor for the efficiency of the parametric multipliers even with the SRPP. Since f_{cd} is related to R_s and $S_{max} - S_{min} \approx 4|S_{N-1}|$, the calculated matching R_g and R_ℓ may not be much larger than R_s when the frequency reaches f_{cd} . In this case the assumption of $R_s \approx 0$ made to derive (2.69) may not be valid any more. The simulations based on the MOS varactors and the SCV pairs are also added the Fig. 2.6 to illustrate that the ratio of capacitance can also influence the efficiencies. Optional ideal filters are used in the simulations without source and load matching. For example, the SCV can provide about 5 times better $|S_2|$ for the tripler than the MOS varactor, which provides a smaller conversion loss at higher relative frequencies as shown in Fig. 2.6.

2.6.2 Resistive Multipliers

Resistive multipliers are always lossy and cannot exhibit a 100% efficiency theoretically expected from the reactive multipliers. The maximum efficiency is calculated as $1/N^2$, e.g. 25% for varistor doublers [20]. The measured efficiency of a varistor doubler in [35] is reported as about 8%, which is much less than the 25% theoretical limit.

To calculate the conversion efficiency for the SRPP with pumped resistance, (2.82) is used. It can be seen that increasing $|R_{N-1}|$ can improve the conversion efficiency, which relates to increasing the ratio of maximum to minimum resistance r_r. To ensure positive resistance, $R_0 \geq 2|R_{N-1}|$ should be fulfilled otherwise the minimum $R(t)$ is less than zero, when the dc term in (2.80) is R_0. With the minimum $R_0 = 2|R_{N-1}|$, and $R_g = R_\ell$, from (2.82) the maximum conversion efficiency is calculated as $G_{P,N}^{\text{resist}} \approx G_{T,N}^{\text{resist}} \approx 0.07$ (i.e. 7% efficiency) when $R_g = R_\ell = \sqrt{3}|R_{N-1}|$ for $N = 2$ and $N > 3$. For $N = 3$, (2.100) can be used to calculate the efficiency in the same way. This number is close but slightly lower

than experimentally verified 8% in [35]. This result can be examined in two ways. As one possible reason, in the diode multipliers, both the variable resistance and capacitance exist, even though the connection is resistively biased without using dc block capacitors. This hybrid operation may increase the efficiency higher than the case with only variable resistance, since reactive multipliers can provide higher efficiency than the resistive multiplier, e.g, maximum 100% versus 25% for doublers. However, since the connection topology of the diode is resistive, i.e. the biasing voltage is not connected through dc block capacitors, the reactive multiplication may not play a very important role in the parametric operation. The other reason is that the diodes possibly do not work as accurately as the SRPP. As explained previously, the switching-like time-varying R can be represented by IRPP with on and off states. Then, the conversion efficiency can be estimated by (2.125) instead of (2.82). With the impulse approach, there is no need to assume $R_0 \geq 2|R_{N-1}|$ such as in the SRPP. Without using sinusoidal waveform, $R_{\rm ON}$ can be a very small value. Assuming $R_{\rm ON} \approx 0$, the calculated maximum $G_{Ti,N}^{\rm resist}$ can be even higher than what is expected from the conventional theoretical limit of $1/N^2$ [20]. For example, when $R_g = R_\ell = D$ in (2.125), $G_{Ti,2}^{\rm resist} = 4/9$, which is larger than 1/4 predicted by the conventional theory. It is also interesting to note that $G_{Ti,2}^{\rm resist} = 1/4$ when $R_g = R_\ell = 2D$ and $R_{ON} = 0$, which is the same as predicted by the conventional theory.

For resistive multipliers with higher N, either with SRPP or IRPP, it can be noticed that the efficiency does not decrease fast with increasing N such as the case in the reactive multiplier. The efficiency based on (2.82) does not depend on N, whereas the efficiency expression of reactive multipliers directly depends on N in (2.69). This predicts that when N becomes large, the high-order resistive multipliers have the potential to provide much larger efficiency than the limit identified by the conventional theory. For example, from (2.82) for $N = 5$, the maximum efficiency calculated with SRPP of R is the same as for the doubler case, which is 7% instead of $1/25 = 4\%$ calculated from the conventional theory. When N is larger, this difference becomes more significant. As discussed in [57],

the theoretical limit of $1/N^2$ described by [20] is from the assumption $\partial i/\partial v > 0$, which not only requires a positive resistance but also a positive I-V derivative, which is valid for a single diode with monotonic R-V curve, but does not apply for a time-varying resistance with an arbitrary R-V curve with peaks and valleys.

2.7 Summary

In this chapter, the theory of the idler-less reactive and resistive parametric harmonic generation is described and elaborated with pumped parameter examples. The Z-matrix or Y-matrix methods are used to give the voltage and current relations of parametric multipliers in the frequency domain. The expressions of efficiencies in terms of frequency-conversion power gains and transducer gains are derived for the parametric multipliers.

Two representations of transient parameters P (S, C, R, or G) are utilized to describe the pumped parameters in the idler-less parametric multipliers. The first one is the SRPP, which generates the Nth-order harmonic by exhibiting $N-1$ periods of $P(t)$ in one pumping period, or an equivalent condition when only dc and $(N-1)$th Fourier coefficients of Ps exist. The other method is the IRPP, which generates the Nth-order harmonic by exhibiting $N-1$ pulses in one pumping period. The IRPP is developed to illustrate the switch-like transient resistance of diodes to generate harmonics. As such it realizes a very high parameter ratio and a very narrow width of pulses with on and off states.

The general relations of the time-varying parameters (S, C, R, or G) with the SRPP, the related symmetries of P-V curves, and the corresponding harmonic generation under sinusoidal pumping are listed in Table 2.1. It is worth to point out that it is possible to generate the sub-harmonics in the same way with sub-harmonically pumped parameters in the form of $\cos(\omega_0 t/N)$, which is briefly discussed in the Appendix.

Table 2.1: Summary of harmonic generation based on time-varying parameters with SRPP under sinusoidal pumping.

N	Transient $P(C/S/R/G)$	P-V(C-/S-/R-/G-V) Normalized to [0, 2]	P-V(C-/S-/R-/G-V) Symmetry
1	Constant	$P_0(V) = 2$	Symmetric (constant)
2	$\cos(\omega_0 t)$	$P_1(V) = V + 1$	Asymmetric (monotonic)
3	$\cos(2\omega_0 t)$	$P_2(V) = 2V^2$	Symmetric (1-peak or 1-valley)
4	$\cos(3\omega_0 t)$	$P_3(V) = 4V^3 - 3V + 1$	Asymmetric (1-peak and 1-valley)
5	$\cos(4\omega_0 t)$	$P_4(V) = 8V^4 - 8V^2 + 2$	Symmetric (2-peak or 2-valley)
6	$\cos(5\omega_0 t)$	$P_5(V) = 16V^5 - 20V^3 + 5V + 1$	Asymmetric (2-peak and 2-valley)
N (odd)	$\cos((N-1)\omega_0 t)$	$P_{N-1}(V) = T_{N-1}(V) + 1$	Symmetric with $(N-1)/2$ peaks or valleys
N (even)	$\cos((N-1)\omega_0 t)$	$P_{N-1}(V) = T_{N-1}(V) + 1$	Asymmetric with $(N-2)/2$ peaks and $(N-2)/2$ valleys

Chapter 3

Parametric Frequency Tripler With n-Type Varactors at 28 GHz

A passive varactor tripler was designed in the 28-GHz 5G NR band. The parametric frequency tripler with the improved varactor pair topology was verified with a 45-nm silicon-on-insulator (SOI) CMOS technology. SOI technology reduces the unnecessary parasitics, and naturally avoids latch-up problems. The n-type MOS varactors are used in a symmetric antiparallel pair of series varactor (SAPSV) topology proposed in this work to reduce the conversion loss (CL), and are verified with excellent performance as a parametric tripler, such as 24.3-dB CL, −8-dBm maximum output power (P_{OUT}^{max}), 17.8% relative bandwidth, which are better in the comparison with prior reported resistive and reactive CMOS parametric triplers. The on-chip LC networks are compact for filtering and matching, and a 9.66-dB integrated phase noise (IPN) is also measured from 1 to 100 kHz at 28.95 GHz.

3.1 Background

To achieve ultra low jitter of IPN in 5G systems, the phase noise (PN) of the LO should be minimized while operating over a wide bandwidth and consuming as low as possible dc power (P_{DC}). The direct generation of LO with VCOs and phase-locked loops (PLLs) in the 5G mm-wave band suffers from the power-hungry blocks such as frequency dividers, and limited PN performance. Therefore, FMs following low frequency PLLs play an important role in LO signal generation in the mm-wave 5G bands such as the multipliers used in [58] and [59].

Conventionally, passive FMs integrated with CMOS technology are used at frequencies higher than 100 GHz [30, 32, 33] or up to the THz band [18]. Passive FMs themselves consume no dc power, though a PA may be necessary to get the required pump power. The PN of the passive FM is low since there are neither active devices nor dc current in a parametric FM. The applications of passive FMs in the 5G band are limited by various factors, such as

the high pump power, high CL, poor harmonic rejection, and bulky filtering and matching networks. The D-band resistive tripler in [33] has a 32-dB CL, whereas the reactive tripler in [30] at ~100 GHz has a 28-dB CL. To have a high output power, the high CL further requires higher input power (P_{IN}) to pump the circuit. And, this high P_{IN} results in a large fundamental leakage. Odd-order FMs can utilize symmetry of the nonlinearity to suppress the even-order harmonics; however, such harmonic rejection ratio (HRR) was only reported around 10 dBc in [32] and [30], which would be poor if used for 5G applications. The fundamental leakage of [32] and [30] was not reported unfortunately. Another disadvantage of the prior reported passive FMs is the CL varies with P_{IN} significantly, e.g., CL varies by 10 dB in [32] and 5 dB in [33], when P_{IN} is in a 10-dB operating range. HBV triplers and GaAs-diode triplers were reported with CL of 14 dB in [60], and 13 dB in [61], respectively, showing the potential of non-CMOS passive triplers to reduce the CL. However, the non-CMOS passive triplers use expensive processes with bulky off-chip waveguides and microstrips, which increase the costs and add difficulties in the integration.

On the other hand, active triplers can provide much smaller CL or even a conversion gain in the mm-wave band, such as 1.3 dB in [62], though active triplers consume some amount of dc power. As an example, a sixth-order active FM for a quadrature-LO generation of a 28-GHz 5G NR transceiver was reported in [63] and is shown in Fig. 3.1(a). The quadrature VCOs (QVCOs) and injection-locked (IL) FMs in [58,59] are replaced by a $\times 6$ single-ended output FM. As the block diagram shows in Fig. 3.1(a), the input and output baluns are required before and after the active FM, to feed the polyphase filter (PPF) to generate the required quadrature LO for the 5G system.

To employ the passive FMs with benefits such as low phase noise and full passive (zero dc power in the multipliers stage), and to address the problems such as high CL and large chip area of matching and filtering networks, a symmetric antiparallel pair of series varactors named SAPSV topology is proposed to achieve an improved ratio of capacitance r_c and simple dc biasing circuits, as the core device of the 28-GHz frequency tripler in a

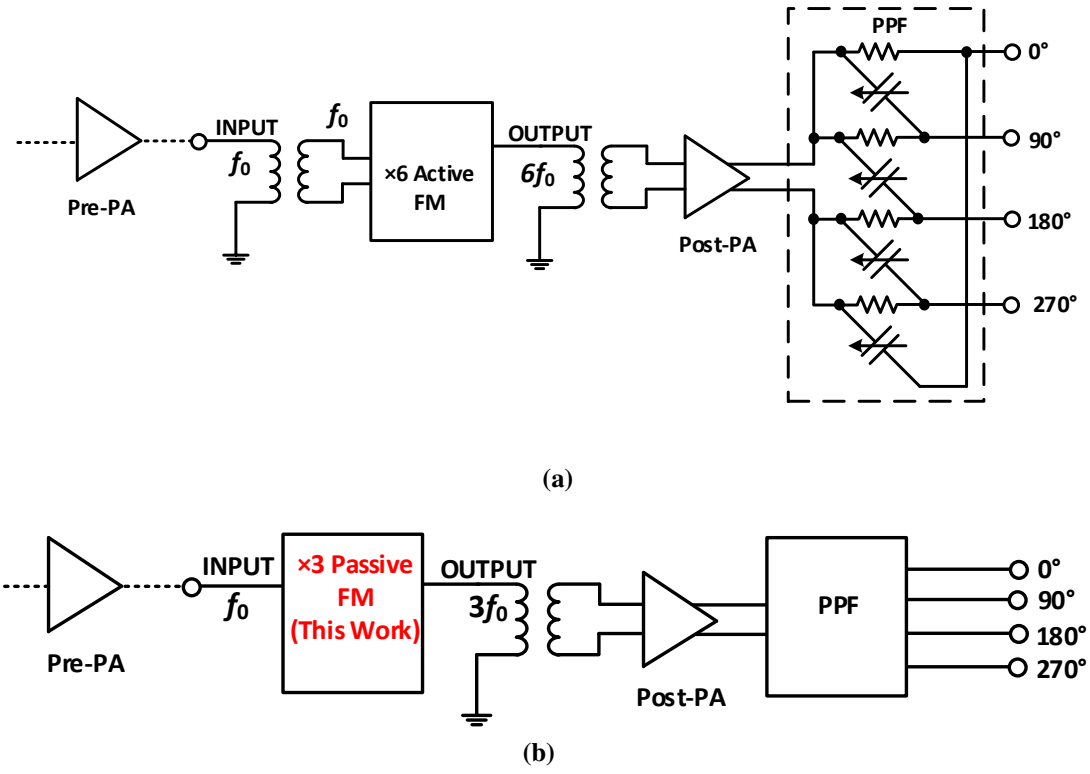


Figure 3.1: Block diagrams of the implementations of FMs for LO generation in 5G transceivers. (a) 28-GHz 5G NR transceiver in [63]. (b) This work.

45-nm SOI-CMOS process. Compact inductor–capacitor (LC) filters and the symmetric varactor topology are utilized to improve the CL and the harmonic suppression. Long transmission lines (TLs), which are used in THz FMs [18], are avoided in this design since they are too big at 28 GHz. Compared with Fig. 3.1(a), the application with the proposed tripler removes the input balun, and benefits from the passive tripler with low added PN and high even-order HRR, if used in the 5G NR systems as shown in Fig. 3.1(b). Noticing that pre-PAs and post-PAs are used in both cases, the active FM needs a significant amount of dc power to have a conversion gain (otherwise active FMs also have CL), whereas a passive FM stage consumes no dc power, resulting in an estimated lower total dc power budget compared with the active counterpart.

3.2 Nonlinear Reactive Device Topology

As discussed in Chapter 2, the reactive FMs have lower CL compared with the resistive FMs. Since the 5G applications of FMs require CL as low as possible to compete with active FMs, a passive tripler discussed in this chapter is based on MOS varactors. Although the varactor FMs exhibit a narrower BW compared with the varistor FMs, for a certain 5G band, such as the 28-GHz band, it is not a drawback, since carefully designed LC networks with the improved device topology can provide a wide BW to cover this frequency range. Only when the design specifications require a multi-band coverage of 5G, resistive FMs may show advantages in the broadband operation, although the prior diode-based FMs in CMOS did not exhibit very wide relative BWs, such as 10% in [32] and 15% in [33].

The proposed SAPSV topology is compared with prior resistive and reactive nonlinear device topologies in passive triplers, with a varying input voltage (V_{IN}) in Fig. 3.2. A complementary antiparallel diode pair (CAPDP) is shown in Fig. 3.2(a), which has n-type and p-type Schottky barrier diodes (n- and p-SBDs) connected in antiparallel. This simple antiparallel diode topology results in poor CL and harmonic suppression, as well as a dramatic change in CL up to about 10 dB when P_{IN} varies from -2 to 8 dBm [32]. Self-dynamic and static biasing is added to the n-SBD side to improve the CAPDP in Fig. 3.2(b), which is called "self-biased" CAPDP (SB-CAPDP) in [33]. One side (i.e. n-SBD side) of the I-V curve is tuned by self or static biasing, thereby the nonlinearity is tunable partially; however, the tuning is not performed for the p-SBD side thereby limiting the tuning capacity and symmetry of this topology, which is a drawback for efficient odd-order harmonic generation and even-order harmonic suppression. SB-CAPDP also needs a number of extra components, such as dc-block capacitors in the dc biasing circuits.

A symmetric MOS varactor topology is shown in Fig. 3.2(c), which is known as anti-series MOS varactor (AS-VAR) tripler in [30]. The anti-series topology with identical AMOSVs ideally has a symmetric C-V curve; however, their series resistance R_ss are added

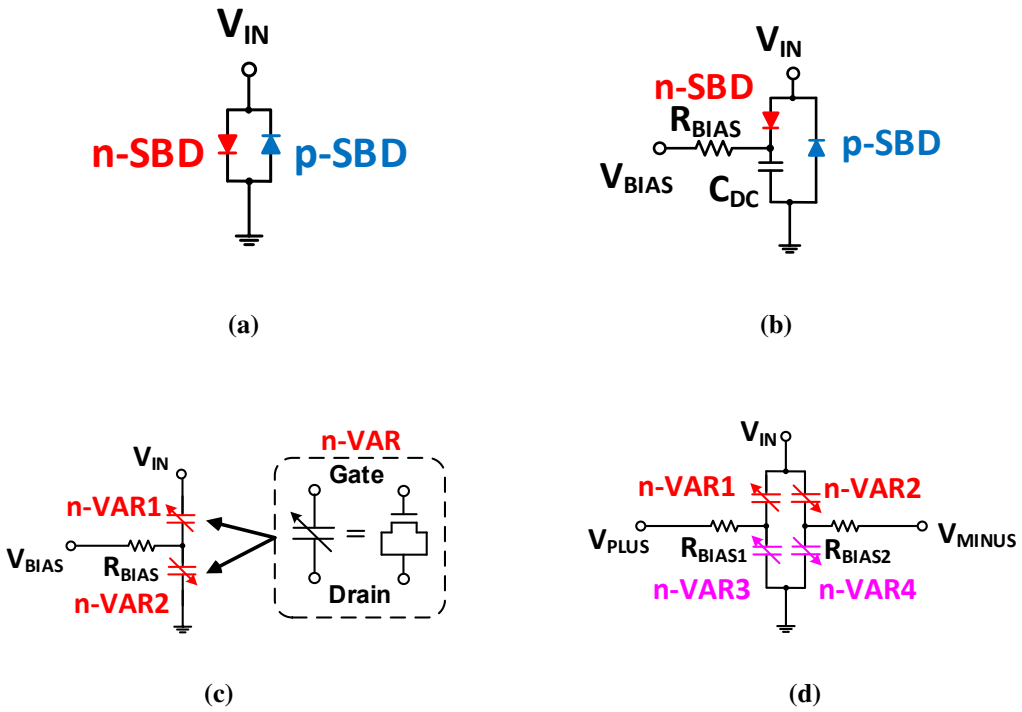


Figure 3.2: Topologies of symmetric nonlinear devices for triplers (a) CAPDP. (b) SB-CAPDP. (c) AS-VAR. (d) SAPSV.

in series, causing the cutoff frequency f_{cd} limited by the doubled R_s, whereas in antiparallel topology R_s is halved, though it does not mean the antiparallel topology must have a better f_{cd} since the capacitance is also added in parallel. In comparison of f_{cd}s , both R_s and r_c of C_{max} to C_{min} should be considered. The application of AS-VAR is also limited by the conventional CMOS technology, since the drain (source) terminal of the AMOSV is connected to n-well in the p-substrate directly, which must keep a non-negative biasing voltage (V_{BIAS}). Also, since the other one terminal of a MOS varactor is gate, the parasitics seen from the gate to drain and drain to gate may be different in conventional CMOS technology, thereby the anti-series topology in conventional CMOS may not be able to provide the perfect symmetry in C-V.

Fig. 3.2(d) shows the proposed SAPSV topology in SOI CMOS. All four varactor components are n-type MOS varactors (n-VARs), thus minimizing the mismatch between

these devices. Unlike the topologies in Fig. 3.2(a) and (b), SAPSV does not need to model p-type devices. By eliminating the dc-block capacitors (C_{DC}) as shown in Fig. 3.2(b) and needed in other parts of the layout (not shown), SAPSV benefits from simpler dc biasing topology, less parasitics from metal connections, and a smaller chip area.

Thanks to the SOI CMOS technology, any positive and negative static biasing voltages (V_{PLUS} and V_{MINUS}), within the range to avoid gate oxide breakdown, can be used to bias the MOS varactors free of latch-up concern. V_{PLUS} and V_{MINUS} are connected to the common nodes of the series varactors through 5-kΩ resistors (R_{BIAS}s) as shown in Fig. 3.2(d). The simulated C-V curves are plotted in Fig. 3.3, when all $V_{\mathrm{PLUS}} = -V_{\mathrm{MINUS}} = V_{\mathrm{BIAS}}$. Whenever V_{BIAS} changes, the C-V curves always keep near-perfect symmetry for the generation of the third harmonic and the suppression of the even-order harmonics. As shown in Fig. 3.3, when V_{PLUS} is positive, the C-V curve has a valley with a larger ratio of capacitance r_c than the ratio of a peak when V_{PLUS} is negative. Therefore, V_{PLUS} and V_{MINUS} are selected as positive and negative biasing voltages, respectively, to obtain higher f_{cd} from (1.7).

Compared with the series topology in Fig. 3.2(c), the SAPSV topology can improve both r_c and R_s to increase f_{cd} of the varactor pairs. Although the four n-VARs can be the same size in a tripler, the symmetry only needs that the left side (n-VAR1, 3) matches the right side (n-VAR2, 4). The simulation shows that CL is improved when the bottom two n-type MOS varactors are larger than the top two in size. When the ratio of varactor sizes (i.e., width ratio of n-VAR3, 4 over n-VAR1, 2) is increased, total r_c and R_s are both improved. For a simple series topology, since the top and bottom varactor must be the same to keep the C-V symmetry, two equal R_s of the varactor are added, as such the total $R_s = 2R_{s,var}$ where $R_{s,var}$ is a parasitic resistance of a single varactor, whereas in SAPSV with larger bottom varactor sizes, the resistance of the varactor pair is much reduced to $R_{s,var}/2$ if the resistance of the bottom two varactors is low enough. By using optimized gate-finger ratio of top to bottom varactors as 9/36, the maximum simulated r_c reaches 2.8 as shown in Fig.

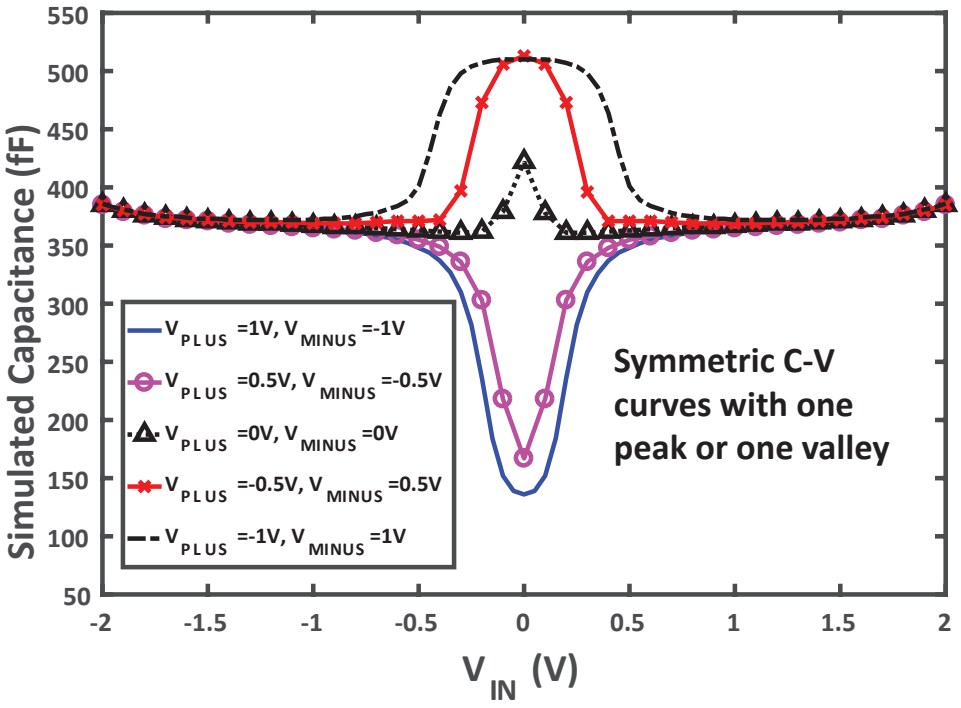


Figure 3.3: Simulated C-V curves of SAPSV with different biasing voltages.

3.3, whereas it is only 2.1 of the AS-VAR in [30]. Since both r_c and R_s are improved for a higher f_{cd}, the CL of the tripler is also reduced based on the discussion in Section 2.6.1.

3.3 Frequency Tripler Design

Figure 3.4 shows the schematic of the proposed SAPSV-based parametric frequency tripler. The input LC tank and the low-pass filter (LPF) select the range of the input frequency f_0, and stop the harmonics flowing back to the input port. The generated third harmonic signal at $3f_0$ passes through the LC high-pass filter (HPF) to a common-source buffer stage for output. The fundamental and second harmonic ($2f_0$) are suppressed by the on-chip HPF and the output LC tank. Resonant frequencies of the input and output parallel LC tanks are tuned to 9.3 and 28 GHz, respectively. Gate-to-source capacitance (C_{gs}) of the buffer MOS FET and the parasitic capacitance from the pad (C_{PAD}) are absorbed into the shunt capacitors in the LC tanks. The performance of the on-chip RF inductors on the high

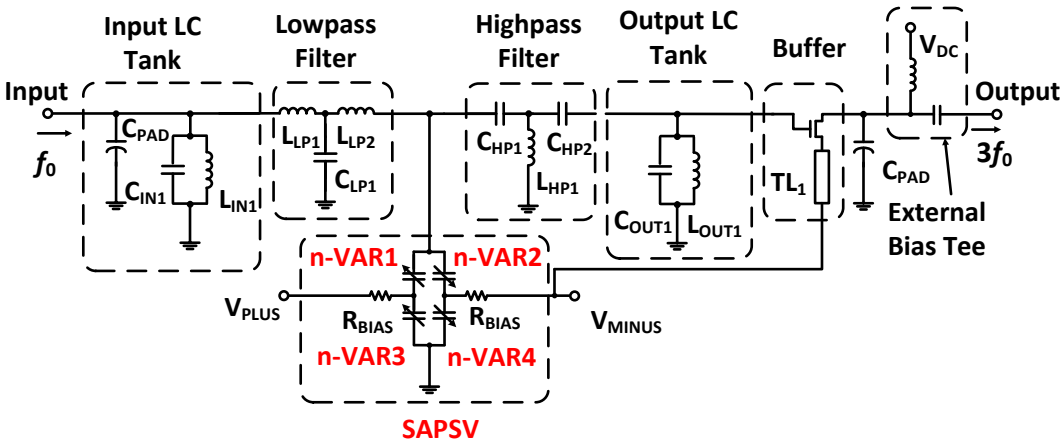


Figure 3.4: Schematic of the passive frequency tripler with SAPSV.

impedance substrate is verified by the electromagnetic (EM) simulation. The value of the high quality factor (Q) metal-insulator-metal (MIM) capacitors, the on-chip inductors, and the finger sizes of the n-type MOS varactors are optimized together to achieve the minimum CL over the desired 28-GHz 5G bandwidth.

The output buffer stage is added for measurement purpose, to imitate the small capacitance-like load of the FM. It also isolates the output and reduces the effect from the load to the circuit. To focus on the performance of the passive tripler, the buffer does not provide any power gain. The measured CL is only slightly increased by a simulated 1.5-dB loss associated with the buffer. The active buffer can be simply modified to have gain instead of loss to further improve the CL performance, by removing (i.e. short circuiting) the source degeneration TL1 in Fig. 3.4.

3.4 Measurement Results

The fabricated chip of the tripler was measured by wafer probing. The RF input and output signals were fed through high-frequency ground-signal-ground (GSG) probes. A 50-GHz bias tee (bias T) was used for a 0.3-V drain voltage as the dc supply (V_{DC}) for the buffer stage. A 40-GHz spectrum analyzer was used for the output power spectrum and PN mea-

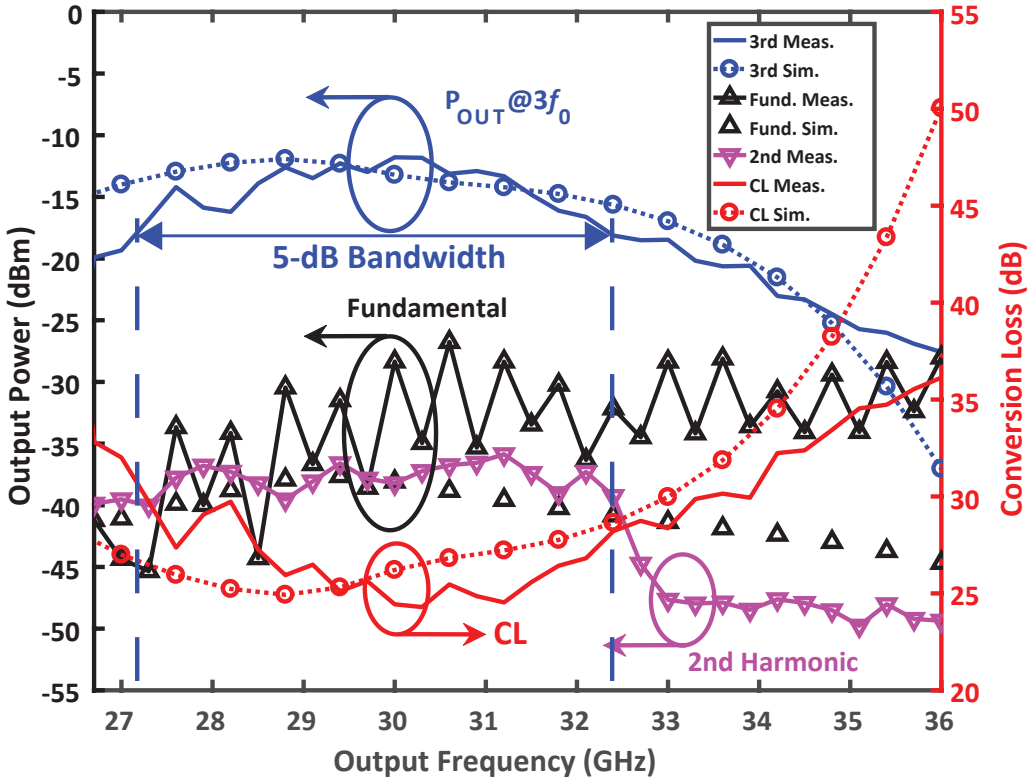


Figure 3.5: Measured and simulated P_{OUT}, CL, and fundamental and second-harmonic output power versus output frequency $3f_0$ at $P_{\mathrm{IN}} = 13$ dBm. Fundamental and second harmonic are measured at f_0 and $2f_0$, respectively.

surement.

Figure 3.5 shows the simulated and measured P_{OUT}, CL, and harmonics versus output frequency $3f_0$ with a 13-dBm P_{IN} and 0.9-V V_{PLUS}, where the minimum CL of 24.3 dB occurs at 30.3 GHz. The measured results of the third-harmonic P_{OUT} and the CL well match the simulation as shown in Fig. 3.5. HRR measured at the output port is kept above 13.6 dBc for the fundamental, and 20.1 dBc for the second harmonic, below the desired third-harmonic output through the whole 5-dB bandwidth. Since the simulated second harmonic is about 60 dB lower than P_{OUT}, it is not shown in the figure. The ripples of the measured fundamental leakage as shown in Fig. 3.5 are possibly due to the high mismatch (attenuation) of the filter network to suppress the high-power fundamental input P_{IN}.

The measured and simulated P_{OUT}, CL and harmonics versus P_{IN} are shown in Fig. 3.6.

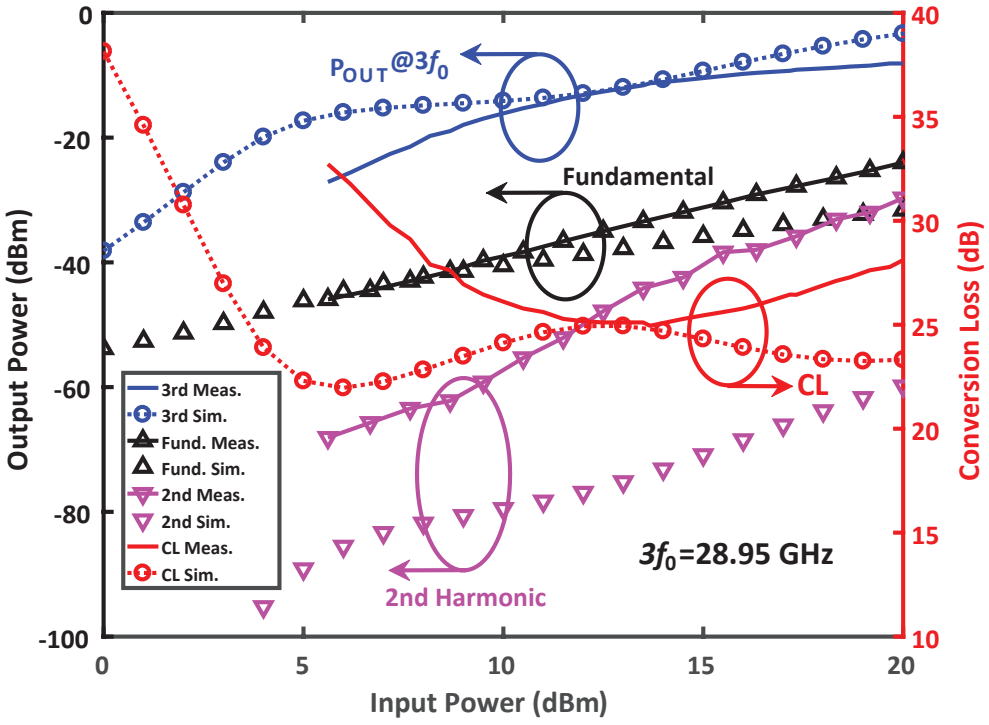


Figure 3.6: Measured and simulated P_{OUT}, CL and harmonics versus P_{IN}.

When P_{IN} varies from 8 to 20 dBm, CL only varies within 3 dB. The measured maximum P_{OUT} (P_{OUT}^{max}) reaches -8 dBm at about 29 GHz. The dependence of P_{OUT} and harmonics on V_{PLUS} ($V_{\mathrm{MINUS}} = -V_{\mathrm{PLUS}}$) is shown in Fig. 3.7. In both Figs. 3.6 and 3.7, the measured second harmonic is much lower than the third harmonic output power level, though is higher than the simulated second harmonic, due to the process mismatch and variations as well as the non-symmetric parasitics which make the C-V curves not perfectly symmetric.

The measured added phase noise performance is shown in Fig. 3.8. The calculated IPN with an integrated frequency range from 1 kHz to 10 MHz is -35.7 dBc at 28.95 GHz. The added IPN (i.e. the difference between IPN of the tripler output and the signal source) is only 9.66 dB, which is very close to the theoretical prediction calculated by $20\log(N) = 9.54$ dB when $N = 3$ [64].

As shown in Table 3.1, this work is compared with other passive triplers, as well as active multipliers for LO generation in 28-GHz 5G NR systems in CMOS. This SAPSV

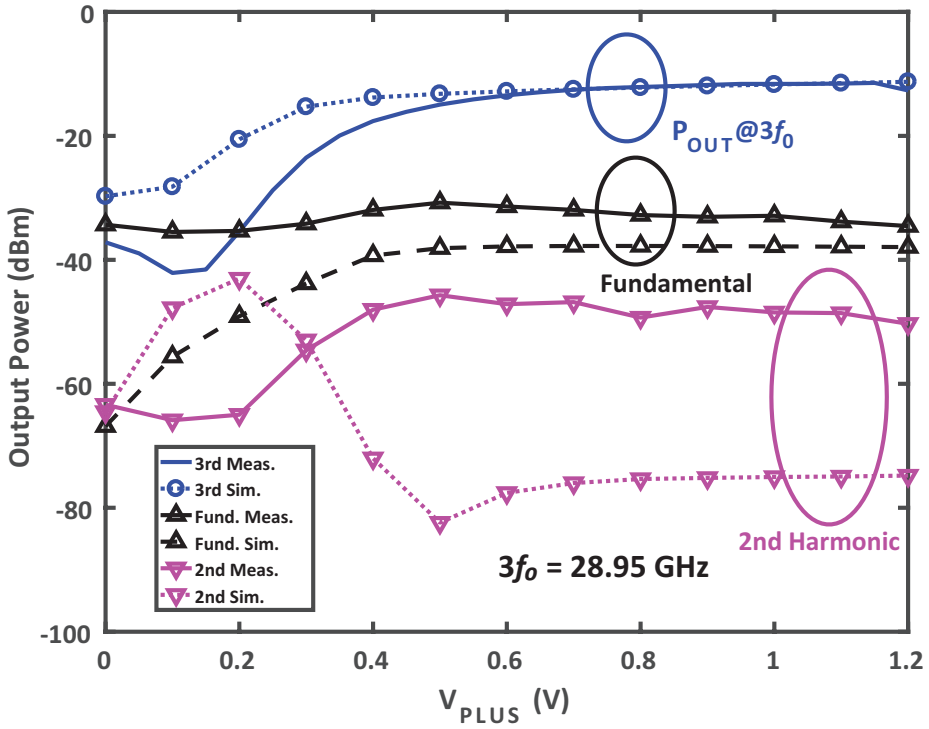


Figure 3.7: Measured and simulated P_{OUT} and harmonics versus V_{PLUS}.

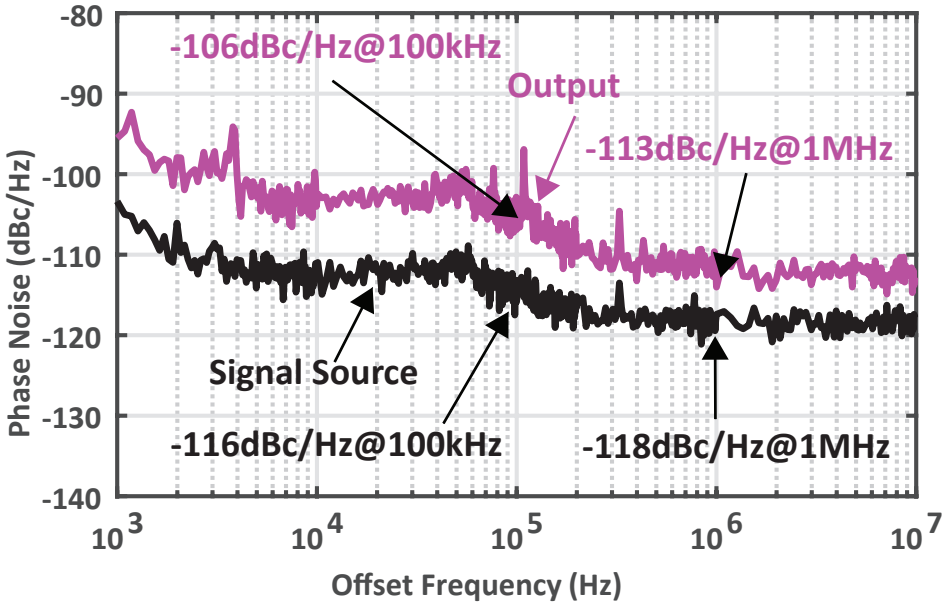


Figure 3.8: Measured phase noise of the tripler output and the input signal.

tripler has smaller CL, higher P_{OUT}^{max}, and wider relative BW, compared with other reactive and resistive triplers in CMOS. The fundamental and second harmonic rejections are characterized over the whole operating BW, input power levels, and biasing voltages, which are not fully available in prior publications of CMOS passive triplers. The measured added IPN is very close to the theoretical prediction $20\log(3)$ dB. The dc power of the passive $\times 3$ stage is zero, and the dc power of the output buffer is 35 mW. Reducing it to 25 mW results in only a 0.2-dB CL increase in measurements. As discussed previously, this source degenerated buffer does not provide any power gain, and its added loss should be subtracted to get the actual CL of the passive tripler.

To get a full and adequate estimation of the dc power of the multiplier, the state-of-the-art CMOS PAs are investigated for the pre-/post-PAs as shown in the application diagram of Fig.3.1 (b). A pre-PA to enhance the pump signal at f_0 (about 8 to 10 GHz) with assumed 35% power-added efficiency (PAE) and 10-dBm P_{OUT}, consumes 26-mW dc power, whereas a post-PA is estimated to consume 10 mW for a 0-dBm P_{OUT} in the 28-GHz band based on [65] and [66]. As a result, the total dc power from the amplifiers is estimated as 26 to 36 mW, whereas the tripler does not consume any dc power. This dc power is comparable with the active FMs in Table 3.1, and less than the total dc power of [63,67,68]

The die micrograph is shown in Fig. 3.9. The total die size is 0.48 mm^2, whereas the core size including all passive filters and LC tanks with the buffer is 0.26 mm^2.

3.5 Conclusions

The proposed SAPSV topology for passive reactive triplers improves the symmetry of the nonlinearity of the varactors in CMOS, provides a higher r_c and an improved f_{cd} to reduce the CL to 24.3 dB, and realizes a 17.8% BW with a maximum -8 dBm P_{OUT} in the 28-GHz 5G NR band. The dc biasing circuits are also simplified. Compact LC networks are used to achieve 13.6-dBc fundamental and 20.1-dBc second-harmonic rejection over the measured 27.1-to-32.4-GHz BW and the full input power range. About -35.7-dBc IPN and 9.66 dB

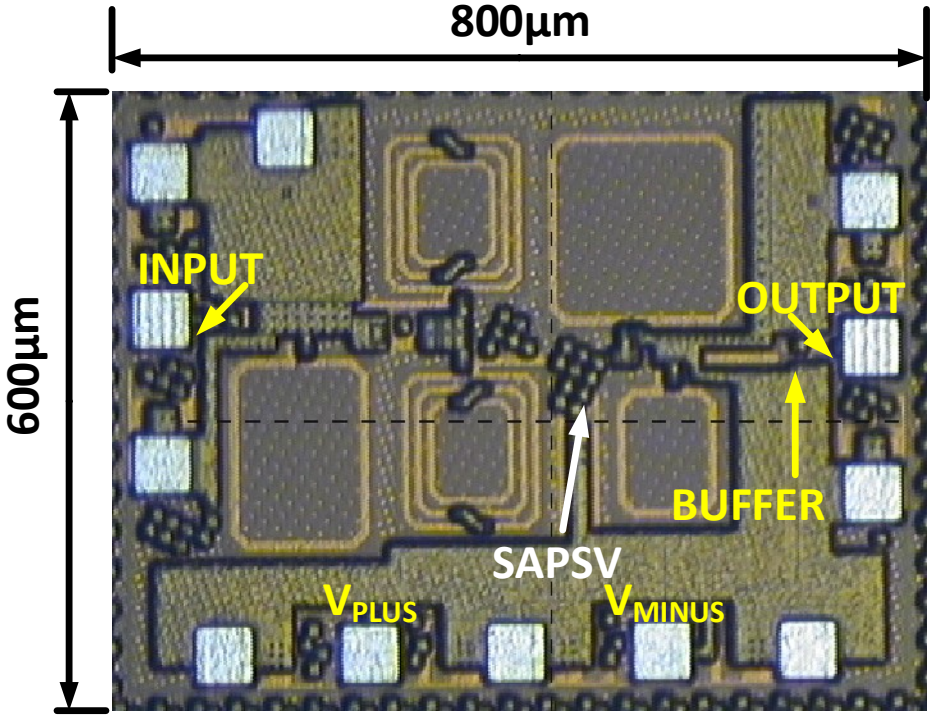


Figure 3.9: Die micrograph.

added IPN of the passive tripler are obtained in measurements.

Table 3.1: Comparison with passive and active multipliers in CMOS

Ref.	**This Work**	[33]	[30]	[67]	[63]	[68]
Appr.	**SAPSV**	SB-CAPDP	AS-VAR	Active QVCO+ QILO	Active $\times3\times2$	Active PLL+ ILFM
Tech.	**45-nm CMOS SOI**	0.13-μm CMOS	0.13-μm CMOS	0.13-μm CMOS	65-nm CMOS	65-nm CMOS
N	$\times$**3**	$\times3$	$\times3$	$\times3$	$\times6$	$\times7.5$
Freq. (GHz)	**27.1 to 32.4**[a]	146 to 170[a]	96 to 108[b]	26.5 to 29.7[b]	23.4 to 24.6[b]	28 to 31[b]
BW (%)	**17.8**	15.2	11.8	11.4	5	10.2
Min. CL (dB)	**22.8 24.3**[c] $P_{IN}=13$	32	27.5	NA	NA	NA
P_{OUT}^{max} (dBm)	**–8** $P_{IN}=20$	-18.6 $P_{IN}=13.4$	-20 $P_{IN}=7.5$	-22[de]	-3	-16[de]
Fund. HRR (dBc)[f]	**>13.6**	NA	NA	NA	NA	NA
2nd HRR (dBc)[f]	**>20.1**	30[g]	10[g]	NA	NA	NA
Added IPN (dBc)	**9.66**	NA	NA	10.5[d]	NA	17.5[d]
P_{DC} (mW)	**0 (Tripler) 25 to 35 (Buffer)**	0	0	20.8 (QILO) 49.7 (Total)	37.1 (FM) 44.4 (Buffer)	22.7 (ILFM) 41.8 (Total)
Chip Area (mm^2)	**0.48 (With pads) 0.26 (Core)**	0.22	3	1 (Total)	0.3	0.32[h] 1.4 (Total)

[a] 5-dB BW. [b] Not specified or not defined by dB. [c] Including 1.5dB loss from the buffer. [d]Extracted from figures. [e]Typical value. [f]Through the whole BW with reference to the desired harmonic. [g]Not specified for the whole BW. [h]Active area.

Chapter 4

Passive Third-, Fourth-, and Fifth-Order Reconfigurable D-Band Frequency Multipliers Based on Switched-Capacitor Varactors

To realize reconfigurable frequency multipliers (RFMs) based on the time-varying SRPP of capacitance, two RFMs were designed and implemented in a 22-nm CMOS SOI technology, operating in a broad bandwidth of D-band for third, fourth, and fifth harmonic generation. One RFM is based on conventional MOS varactors connected as antiparallel varactor pairs (APVP) but implemented with the back-gate voltage (V_{BG}) to tune the C-V curves, together with dc biasing voltages V_{PLUS} and V_{MINUS} to obtain the $\times 3$, $\times 4$, and $\times 5$ modes of the RFM. The conventional MOS varactor has a limited ratio of capacitance r_c, thereby the total performance of the parametric multipliers is limited with these varactors, such as a high CL and a narrow BW. To improve the r_c as well as to achieve a high f_{cd}, a new varactor device topology named shunt switched-capacitor varactor (SCV) is proposed to replace the conventional MOS varactors in mm-wave RFMs. The SCVs are shown to exhibit an r_c as high as 20 in the simulation, which corresponds to about 10 times improvement relative to the conventional mm-wave or THz MOS varactors. The SCVs are connected in complementary SCV pairs (C-SCVPs) to achieve the required C-V shapes for the $\times 3$, $\times 4$, and $\times 5$ RFM. Compared with the MOS-varactor-based RFM, the SCV-based RFM achieves improvements of 11.4, 6.6, and 7.9 dB in minimum CL, and 3.3%, 90%, and 400% in relative BW for the three FM modes, respectively, which demonstrates the potential of SCVs to significantly improve the performance of the mm-wave and THz parametric circuits.

4.1 Background

Conventionally, reactive varactor-based FMs have a fixed multiplication factor (N), such as $\times 2$ [69], $\times 3$ [30], and $\times 5$ [17]. As introduced in Section 1.3.3, the idlers used in the

parametric FMs can also restrict the tunable N of the parametric FMs. Although active multipliers show tunable N by waveform shaping [70], the active RFM consumes dc power and exhibits limited harmonic suppression, and the waveform shaping is still not applicable for passive RFMs. As the SRPP method discussed in Section 2.3, the Nth-order harmonic generation can be realized by using nonlinear C-V curves with corresponding peaks and valleys, to obtain a time-varying $N-1$ periods of capacitance or elastance in one period of pumping excited by a sinusoidal input signal. The nonlinear C-V curves of varactor pairs can be manipulated into "1-valley", "2-valley" asymmetric, and "2-valley" symmetric C-V curves by tuning the biasing voltages , for the third, fourth, and fifth harmonic generation, respectively. The lossy idlers are avoided in all of the $\times 3$, $\times 4$, and $\times 5$ FM modes.

The MOS varactor pairs have been traditionally used for the establishment of symmetric C-V curves to generate an odd-order harmonic, such as AS-VAR in the tripler [30], complementary MOS varactor pairs in the quintupler [17], and the SAPSV in the tripler described in Chapter 3. Presently, only "1-peak" or "1-valley" C-V curve is used for the odd-order harmonic generation, not only for triplers but also for quintuplers [17, 71]. However, this RFM design is the first demonstration of the tunable C-V curves with multiple peaks and/or valleys for tunable harmonic generation with $N \geq 3$.

SAPSV shows that in SOI CMOS technologies, antiparallel nMOS varactors can be connected to realize the symmetric C-V curve, avoiding the necessity of using pMOS varactors in parallel MOS varactor pairs in [17]. The same concept is used to develop the reconfigurable antiparallel nMOS varactor pairs (APNVPs) for the RFM. Although APNVP RFM can be used for the $\times 3$, $\times 4$, and $\times 5$ RFM, the performances, such as CL and P_{OUT}^{max}, are limited by the low ratio of maximum to minimum capacitance r_c of the on-chip MOS varactors. Such ratio is directly related to the maximum attainable $|S_{N-1}|$ of the pumped elastance and is the key factor for the high-frequency performance of the parametric multipliers. As discussed in Section 2.6.1, two varactors with a similar f_{cd} but different r_c can also have different performance in reactive multipliers. The one with much higher

r_c can exhibit a lower minimum CL achieved at a higher frequency. Some non-CMOS process, such as the HBV, can reach r_c as high as 4, whereas the typical r_c of MOS varactors in mm-wave and THz applications is in the order of 2 [17,30], or about 3 in this 22-nm CMOS SOI process, resulting in a low dynamic cutoff frequency f_{cd}, which significantly limits the applicable frequency range and the performance of mm-wave and THz parametric circuits, with the MOS varactor as a bottleneck.

A new type of shunt switched-capacitor varactor topology named SCV is proposed in this work to increase the r_c to above 20 in the 22-nm CMOS SOI process, with the purpose to be used for sub-THz and THz parametric circuits. This increase is about 10 times higher than in conventional bulk CMOS processes. The nMOS SCV exhibits an f_{cd} at 937 GHz when $r_c = 20$. With even smaller transistor size and C_{min}, higher f_{cd} can be achieved, as high as 1.5 THz in the simulation. As a reference, the f_{cd} of AS-VAR of a 100-GHz tripler in [30] is from 200 to 450 GHz with a 1.3 to 2.1 r_c, and f_{cd} of a symmetric varactor pair in a 0.7-THz quintupler in [17] reaches 1.8 THz but with a limited r_c of 1.6. To be used in the D-band RFM, both nMOS and pMOS SCVs are combined together to form a complementary SCV pair (SCVP) named C-SCVP, which is utilized for the establishment of the required tunable shapes of C-V curves. Both SCVP RFM and APNVP RFM are fabricated and measured to demonstrate the validity of the theory of the reconfigurable harmonic generation. Although both of the designs can perform the $\times 3$, $\times 4$, and $\times 5$ frequency multiplications, the SCVP RFM exhibits significant improvements in almost all specifications, including CL, P_{OUT}^{max} , relative BW, and harmonic suppression, demonstrating the potential of the SCV topology for high performance sub-THz and THz parametric circuits.

4.2 Varactor Device Topologies

4.2.1 SCV Configuration

The initial concept of the SCV is from switched-capacitor banks, which are commonly used in various kinds of circuits, such as the VCO in [72]. An example of the shunt switched-capacitor bank is shown in Fig. 4.1(a). In this topology, C1 is in series with an ideal switch (SW), and the total capacitance of the circuit is controlled by the SW. Given the capacitor C1 is much larger than C2, the switched bank seems promising for increasing the r_c since the ratio equals to C1+C2 over C2. However, although it can be used for some VCOs controlled by a dc voltage, it does not fulfill the desired characteristics for the parametric circuits. When the capacitance in the parametric circuits is varied by an SW, such as the degenerate parametric amplifier described in Chapter 1 of [1], the charge Q_c equal to CV is kept constant in the process, so that the variation of capacitance can cause voltage change. It is not the case in the simple switched-capacitor bank, since the voltage V_{IN} between the input terminal and ground is always constant, when the SW is turned from on to off. There is no voltage change at the top terminal caused by the capacitance change, thereby it is not a kind of useful high-frequency varactors for parametric circuits.

To solve the problem in the switched-capacitor bank, the SCV topology is proposed to preserve the constant charge within the circle as shown in Fig. 4.1(b). When the SW is turned on, C2 is shorted, and the total capacitance is C1. When the SW is turned off, the C1 is in series with C2. Given that C2 is much smaller than C1, C_{max} is C1 when the SW is on, and C_{min} is about C2 when the SW is off, assuming the SW is ideal, i.e. the on resistance is zero and the off resistance is infinity. The SW can be replaced by a real nMOS SW or pMOS SW to build the basic SCV circuits.

The control voltage of the SW is connected to the gate of the MOS FET, therefore nMOS SW and pMOS SW have the opposite polarity versus the control voltage. By utilizing this feature, the gate control voltage can be directly connected to the input terminal

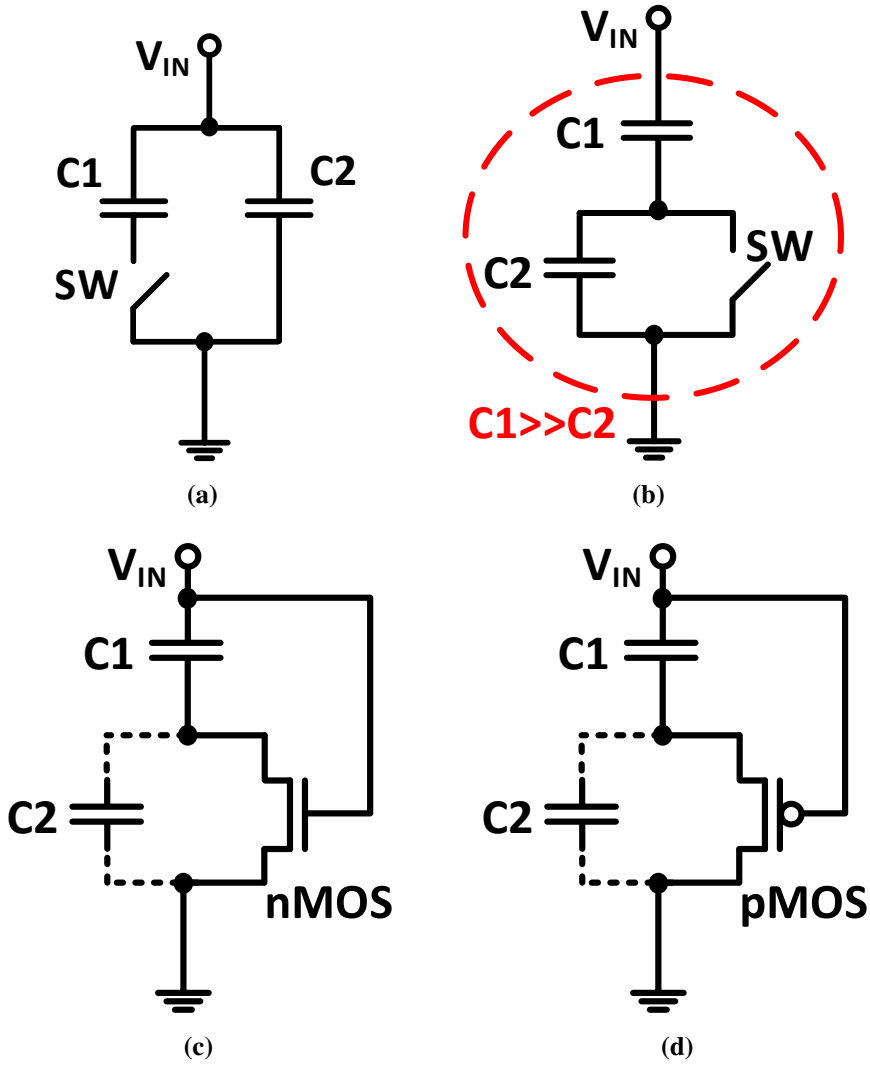


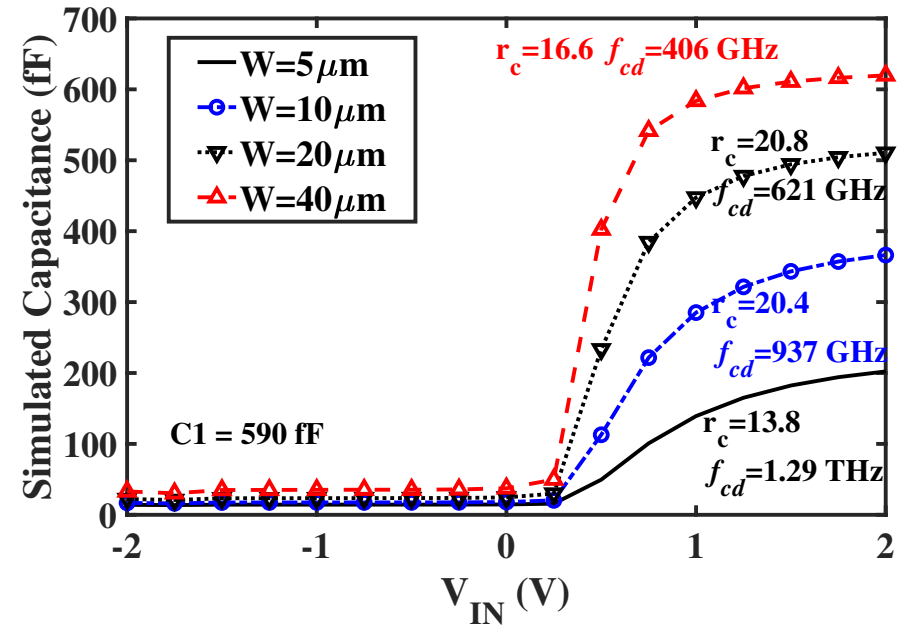
Figure 4.1: Topologies of shunt varactors. (a) Switched-capacitor bank. (b) SCV with an ideal SW. (c) SCV with an nMOS SW. (d) SCV with a pMOS SW.

V_{IN}, to realize the asymmetric increasing and decreasing C-V curves with the nMOS and pMOS SWs, as shown in Figs. 4.1(c) and (d), respectively. To maximize r_c, the minimum capacitance C_{min} should be minimized, therefore the stand-alone C2 is removed, and C2 in Fig. 4.1(c) or (d) is absorbed into the drain-to-source parasitic capacitance of the MOS SW. A narrow width (W) of the MOS FET is also preferred since the small gate- and drain-to-source capacitance is wanted to minimize C_{min}. The resultant C-V curves with different Ws of the nMOS and pMOS SWs are shown in Figs. 4.2(a) and (b), respectively. To maximize C_{max}, a large C1 is chosen as 590 fF. It can be seen from the figures that when the

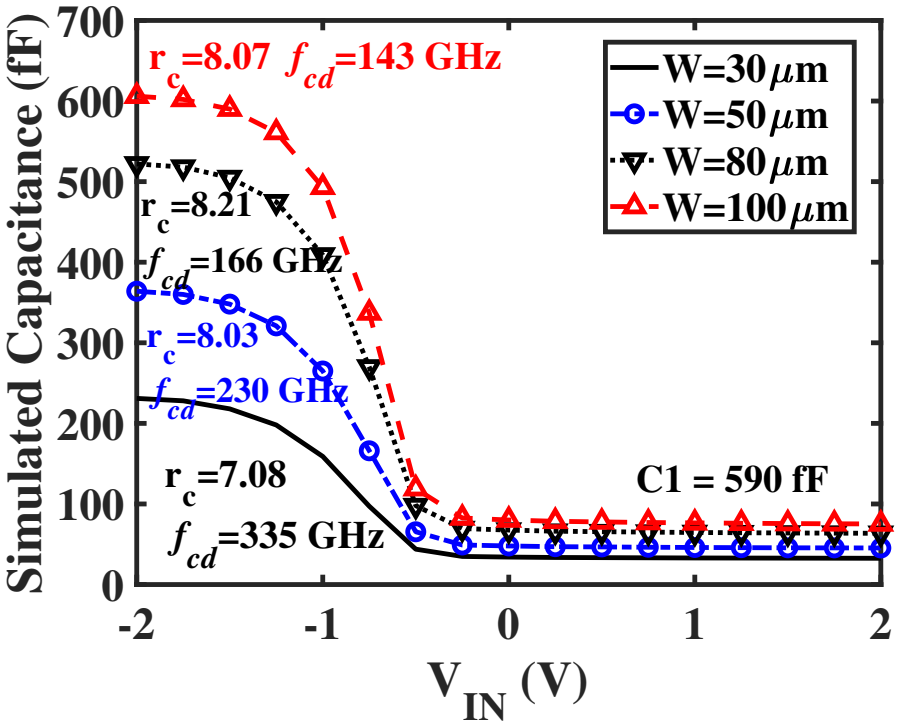
SW size is very small, C_{max} cannot reach the sum of C1 and the parasitic capacitance of the SW, because of the high parasitic resistance of SW, which limits the total equivalent capacitance. Therefore, there is an optimized value of W to balance C_{min} and C_{max}. As shown in Fig. 4.2, the maximum r_c reaches above 20 for nMOS SCV and 8 for pMOS SCV, which are much larger than r_c of conventional MOS varactors, which is only in the order of 2 to 3. The f_{cd} of the nMOS SCV reaches 937 GHz when $r_c = 20.4$. When W is reduced to 2.4 μm, the nMOS SCV exhibits an f_{cd} as high as 1.5 THz with $r_c = 6.6$. The pMOS SCV has a worse performance in terms of lower r_c and f_{cd} compared with the nMOS SCV, due to the larger channel resistance of a pMOS compared to an nMOS FET. By reducing the W of the pMOS SW, 640-GHz f_{cd} and $r_c = 3.8$ can be obtained with a 10-μm W of the pMOS FET. As shown in Fig. 2.6, with a same level of f_{cd} , the SCV pair has a $|S_2| \approx (S_{max} - S_{min})/4$ [19] as high as 5 times as that of the $|S_2|$ of the MOS varactor pairs. As demonstrated in Fig. 2.6, for a condition with $R_g = R_\ell = 50\,\Omega$, a tripler using SCV can achieve a lower CL at higher relative frequencies than using conventional MOS varactors theoretically even with the same level of f_{cd} , and the improvement will be more significant if much higher f_{cd} is exploited.

The shunt topology is convenient for the proposed nMOS and pMOS SCVs, whereas series topology is also possible, if the ground terminals in Figs. 4.1(c) and (d) are RF ground with bypass capacitors, and the dc biasing can be realized through biasing resistors. However, this series topology makes the dc biasing complex for the multiplier design and is not used in this design.

A potential drawback of the SCV is that the imperfect SW with parasitic resistance can lower the total quality factor (Q), when the SW is on, and especially during the transition between on and off states (i.e., between C_{max} and C_{min}). The transition Q can be very low since the equivalent resistance of the SW is some value between very low and high. The Q dependence on voltage and frequency of a transistor-controlled variable capacitor will be discussed with details in Chapter 6. In contrast, the total resistance of the MOS varactors



(a)



(b)

Figure 4.2: Simulated C-V curves of SCV with (a) nMOS SW; (b) pMOS SW.

does not change significantly during the voltage changing range, and thus the Q of MOS varactors does not experience a significant change. However, the measurement results of SCVP RFM and APNVP RFM do not show observable performance degradation due to the low Q in the transition voltage range in the SCV-based RFM relative to the MOS-varactor-based RFM, which suggests the low Q of the SCV transition region may not be an insurmountable hurdle for the parametric circuits.

4.2.2 C-SCVP and APNVP Configuration

The increasing or decreasing C-V curves in Figs. 4.2(a) and (b) can be used to build frequency doublers. However, for N no less than 3, the required C-V curves need peaks and/or valleys as in the harmonic generation theory in Section 2.3. The nMOS varactor can be connected in antiparallel to form a MOS varactor pair as the APNVP topology to obtain the "1-peak" or "1-valley" symmetric C-V curve for triplers, as required in Fig. 2.2(c). In this SOI CMOS technology, back-gate voltage V_{BG} is useful to fine tune the shape of the C-V curve for better symmetry, as shown in Fig. 4.3(a). For the shunt SCV topology, the "1-peak" or "1-valley" C-V curve can be obtained by employing the nMOS SCV and pMOS together to form the C-SCVP, which can provide the symmetric C-V curves for triplers, as shown in Fig. 4.3(b).

To get more peaks or valleys in the C-V curves for $N > 3$, multiple varactor pairs can be placed in parallel, and biased with biasing voltages V_{BIAS} at different voltage potentials. For $\times 4$ and $\times 5$ multiplications, as shown in Figs. 2.2(d) and (e), "1-peak and 1-valley" asymmetric and "2-valley" symmetric C-V curves are required by the harmonic generation theory, respectively, which can be realized by a dual-varactor-pair topology as shown in Fig. 4.4. In the dual-varactor-pair topology, two varactor pairs are connected in parallel, and biased with a positive voltage V_{PLUS} and a negative voltage V_{MINUS}. The varactor pair can be either C-SCVP or APNVP, and the total resultant C-V curves are the sum of the individual C-V curves of each pair (i.e. the ones shown in Fig. 4.3), and the positions of

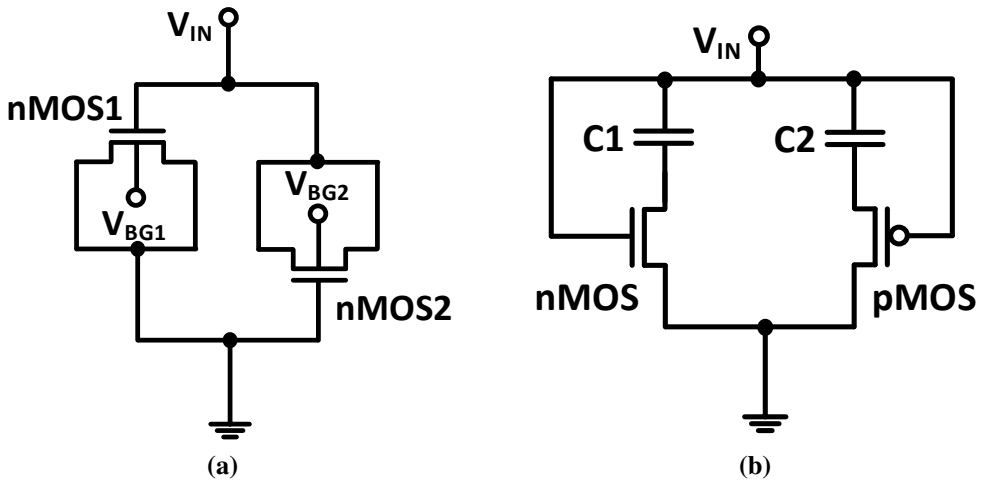


Figure 4.3: Topologies of varactor pairs: (a) APNVP. (b) C-SCVP.

the valleys of the C-V curves can be adjusted by the biasing voltages V_{BIAS}s (i.e. V_{PLUS} and V_{MINUS}).

The reactive tripler only needs one valley in the C-V curve as shown in Fig. 2.2(c), which can be obtained by setting both V_{PLUS} and V_{MINUS} of the dual varactor pair to zero ($V_{\text{PLUS}} = V_{\text{MINUS}} = 0$). For a $\times 5$ quintupler, two valleys are needed for the symmetric C-V curve as shown in Fig. 2.2(e), so that the absolute value of the biasing voltages V_{BIAS} can be defined as $V_{\text{BIAS}} = V_{\text{PLUS}} = -V_{\text{MINUS}}$. The value of V_{BIAS} should be large enough to ensure the two valleys are far apart. The "1-peak and 1-valley" C-V curve for a $\times 4$ quadrupler as shown in Fig. 2.2(d) resembles a part of the "2-valley" C-V curve for quintuplers in Fig. 2.2(e), by shifting the pump voltage range for a small step relative to 0 V. Therefore, the "1-peak and 1-valley" C-V curve for quadruplers can be realized by a "2-valley" asymmetric C-V curve, which is shifted from a "2-valley" symmetric C-V curve for quintuplers, based on symmetrically biased V_{BIAS} and $-V_{\text{BIAS}}$ plus a small shift voltage V_{SHIFT} as the new V_{PLUS} and V_{MINUS}, respectively. The steps to get the required C-V curves for quintuplers and quadruplers are visualized in Fig. 4.5. The full pumping for quintuplers is the full range covering two valleys in the C-V curve, whereas the full pumping range for the quadrupler is only the red part of C-V curve as shown in Fig. 4.5.

The final resultant C-V curves of the dual varactor pairs with C-SCVPs and APNVPs

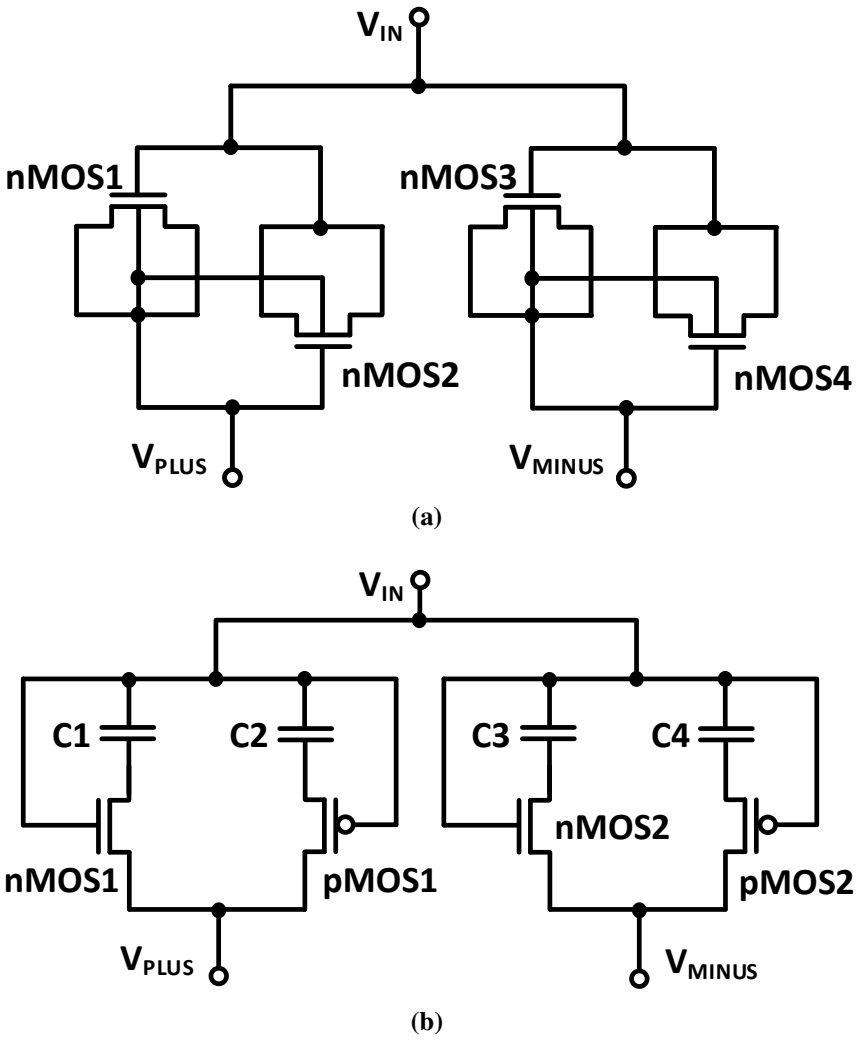


Figure 4.4: Topologies of dual varactor pairs: (a) Dual APNVP. (b) Dual C-SCVP.

are shown in Fig. 4.6. When V_{PLUS} and V_{MINUS} are both zero, the C-V curve is "1-valley" symmetric for triplers. When $V_{\mathrm{BIAS}} = V_{\mathrm{PLUS}} = -V_{\mathrm{MINUS}} = 0.8$ V, i.e.V_{PLUS} and V_{MINUS} are ± 0.8 V, the C-V curve is "2-valley" symmetric for quintuplers. When a $V_{\mathrm{SHIFT}} = 0.4$ V is added to both V_{PLUS} and V_{MINUS}, i.e. $V_{\mathrm{PLUS}} = 1.2$ V and $V_{\mathrm{MINUS}} = -0.4$ V, the C-V curve is "2-valley" asymmetric for quadruplers, of which the effective part is "1-peak and 1-valley" C-V curve. It can be seen from the Fig. 4.6 that the dual C-SCVP device exhibits a much higher r_c than that of the dual APNVP device. However, the C-V curve of the dual C-SCVP device is slightly less symmetric than that of the dual APNVP device composed of all nMOS FETs, due to the difference between nMOS and pMOS FETs. The "1-valley"

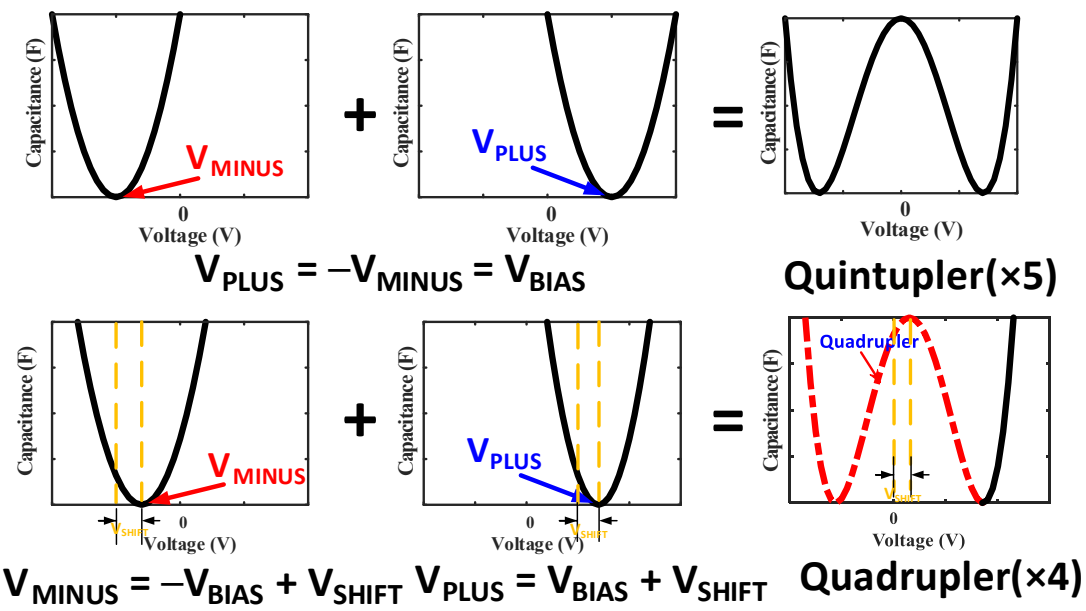


Figure 4.5: Steps to get the sum of C-V curves of varactors to obtain "2-valley" symmetric C-V for quintuplers, and "1-peak and 1-valley" C-V for quadruplers.

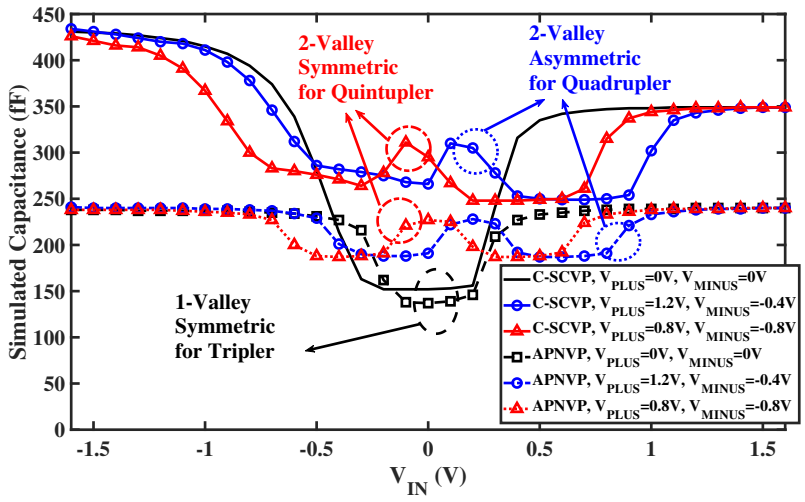


Figure 4.6: Simulated C-V curves of dual C-SCVP and dual APNVP.

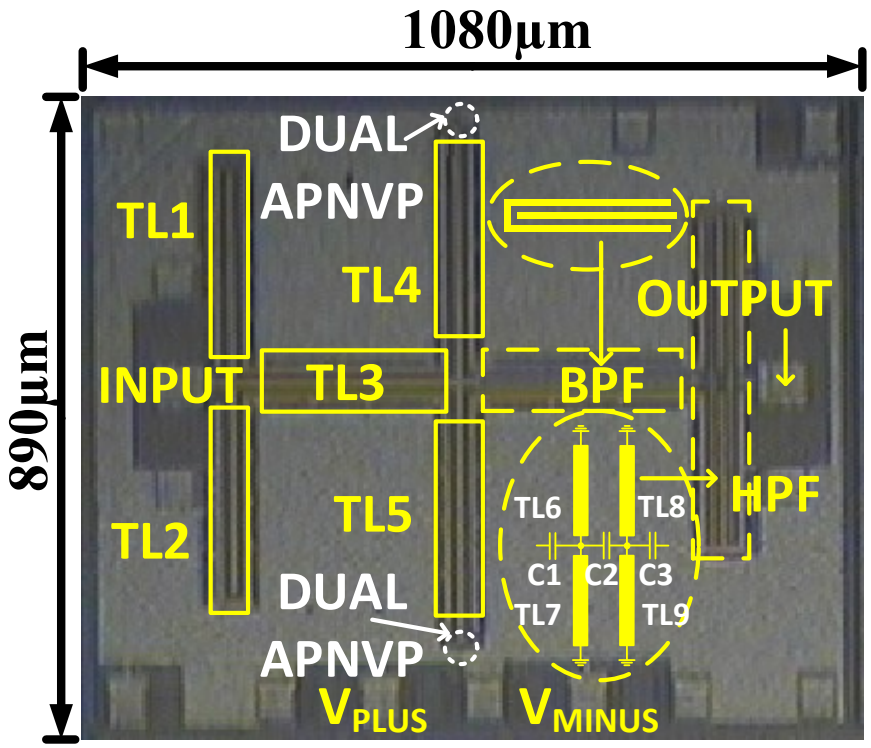
C-V curve combining nMOS and pMOS SCVs reaches an r_c of maximum to minimum capacitance of about 2.8, and the resultant f_{cd} reaches about 860 GHz for the D-band applications, whereas the "2-valley" C-V curve has a 1.7 r_c , and a 210-GHz f_{cd}, which are lower than those of the "1-valley" C-V due to the much higher minimum capacitance when the two valleys in C-V are separated away.

For comparison purpose in the Fig. 4.6, in the real layout two dual APNVPs are used for the APNVP RFM, whereas C-V of only one dual APNVP is shown in Fig. 4.6. In SCVP RFM, one C-SCVP is placed in the top and the other one is placed in the bottom, as the die micrograph shows in Fig. 4.7(b), as such two C-SCVPs compose one dual C-SCVP in the RFM, of which the C-V curve is shown in Fig. 4.6.

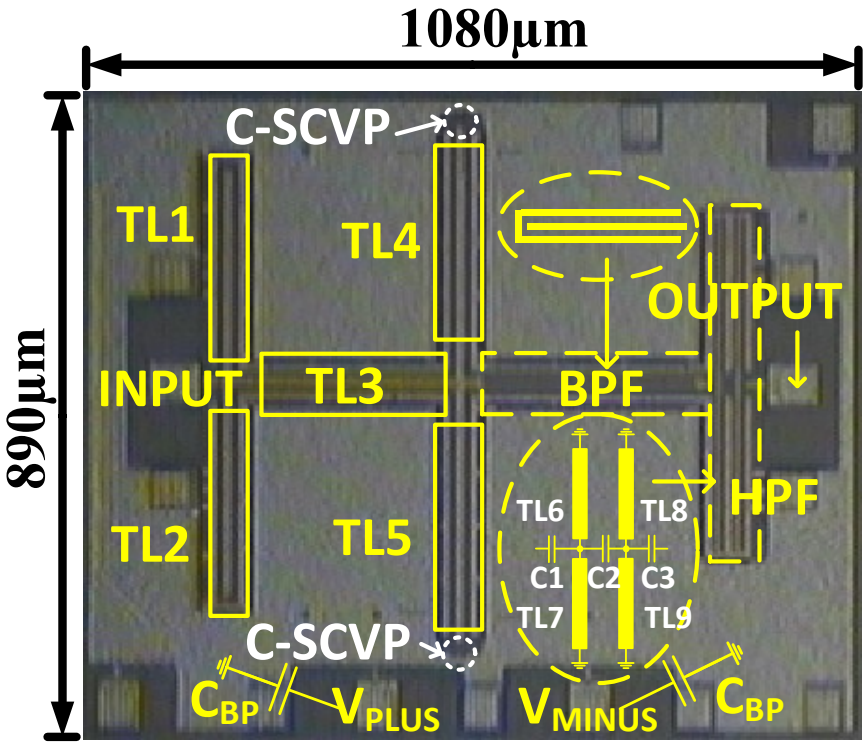
4.3 RFM Circuit Design

The schematic superposed on the die micrograph is shown in Figs. 4.7(a) and (b), for APNVP RFM and SCVP RFM, respectively. The layout has a balanced topology to keep the total layout symmetric geometrically. The input filtering network is composed of quarter-wave transmission lines TL1 to TL3. TL1 and TL2 are open stubs, which can provide an open circuit for the generated harmonics and stop them from going back to the input terminal, with a center target frequency band at 110 to 120 GHz, due to the design considerations and measurement limitations in the lab. TL4 and TL5 are used to improve the matching of the core device to the rest of the network and optimized to improve CL and P_{OUT}.

The output band-pass filter (BPF) is built by open stubs [32], which increases the CL no more than 5 dB in the frequency band targeted for the RFM output from 85 to 163 GHz in simulations. The length, width and spacing of the BPF are 190, 3, and 4 μm, respectively. An optional high-pass filter (HPF) is implemented as a high-pass LC filter. The inductors in the HPF are implemented by short stubs TL5 to TL9 due to the small size at the D-band frequency. The capacitors C1 to C3 are mm-wave metal-oxide-metal (MOM) capacitors. The cutoff frequency of the HPF is about 86 GHz, which adds about 3 to 4 dB loss in the desired frequency band. The HPF can improve the fundamental and second-order harmonic suppression, since these two harmonics are the strongest leaking harmonics possibly presented at the output terminal, and the BPF cannot suppress them significantly. As per simulations, the second harmonic rejection can be improved by 10 to 15 dB with the HPF. The sizes of the nMOS and pMOS SWs as well as the sizes of the



(a)



(b)

Figure 4.7: The die micrograph with the schematic of the RFM. (a) APNVP RFM. (b) SCVP RFM.

fixed capacitors in the SCV are optimized for the lowest CL, whereas the shape of the C-V curve is preserved and unchanged in the optimization (i.e. only the absolute capacitance value as shown in Fig. 4.6 is changed). C1 and C3 are 48 fF, whereas C2 and C4 are 85 fF confirmed by the optimization.

The passive filtering and matching networks are the same for the APNVP and SCVP designs. The only difference of the total layout except the core device is that some additional bypass capacitors (C_{BP}s) are added in the layout of the SCVP RFM in Fig. 4.7(b). C_{BP}s are connected between V_{PLUS} or V_{MINUS} terminals and the ground, for better RF ground of the passive device. In simulations, adding C_{BP}s can improve the CL by 3.4, 1.2 and 2.6 dB for the $\times 3$, $\times 4$, and $\times 5$ SCVP RFM, and extend the relative BW to 38.8% and 35.4% from 27.9% and 24.3% for the $\times 3$ and $\times 4$ SCVP RFM, respectively. Simulations show that the APNVP RFM can benefit from the same extra C_{BP}s in a similar way. However, since the APNVP RFM was the first tapeout for the RFM, the improvement with C_{BP}s was added for the second round of tapeout with SCVP RFM but not realized at the time when the APNVP RFM was fabricated.

4.4 Measurement Results

The measurement setup of the D-band RFMs is shown in Fig. 4.8. The RF input signal is generated by a 40-GHz signal generator, and is amplified by an external RF PA to pump the device under test (DUT). Two PAs are used to cover the frequency range of the RFM measurement. The low-frequency PA operates up to about 27 GHz, whereas the high-frequency PA operates typically between 30 to 40 GHz, but it can operate slightly lower than 30 GHz to narrow the frequency gap between the operating BWs of the two PAs. The RF power fed to the RFM is calibrated carefully within the frequency and power ranges of the measurement to the end of the cable connected to the GSG input probe. The D-band output signal is detected by a waveguide GSG probe and is passed to a D-band frequency extender through an S-bend waveguide. Then the output signal is downconverted to the IF

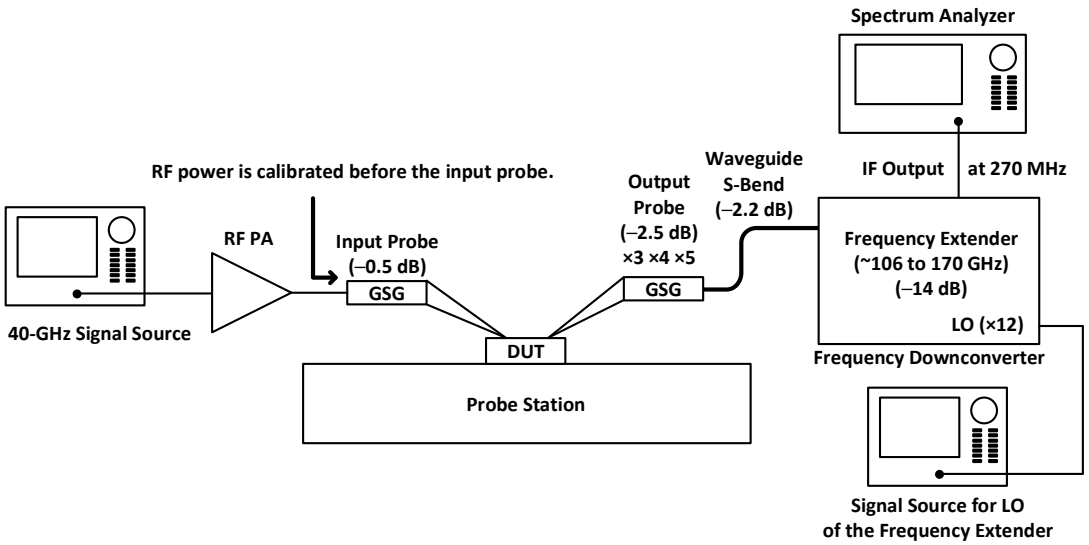


Figure 4.8: Measurement setup.

frequency band at about 270 MHz by the frequency extender, and then is measured by the spectrum analyzer. The frequency extender has an internal $\times 12$ FM for the D-band LO, which is fed by a 20-GHz signal generator in the measurement. The available measurement frequency range is limited by the PAs and the frequency extender, which has a lower limit at about 106 GHz. The typical losses and CL of the frequency extender are also shown in Fig. 4.8. The actual losses and CL are dependent on the frequency, and they are calibrated for each steps of frequency and power levels, by lookup tables of data from the calibration.

The simulated and measured P_{OUT} versus P_{IN} and output frequency (f_{OUT}), as well as the measured harmonics of the SCVP RFM are shown in Fig. 4.9. Some parts of the frequency range are limited by the instruments of the measurement setup. For the $\times 3$ FM mode, both V_{PLUS} and V_{MINUS} are set to zero, thus the third-order harmonic P_{OUT} is not tunable by V_{BIAS}. The simulated and measured P_{OUT} of the required harmonics, and other unwanted adjacent harmonics versus the biasing voltages are shown in Figs. 4.10(a) and (b), for the $\times 4$ and $\times 5$ FM modes, respectively. Since the third harmonic is out of the measurable frequency range in these measurements, simulated curves are given. For the fifth-order harmonic generation of quintuplers, the C-V curves should always be symmetric. Therefore, the biasing voltages are set as $V_{\mathrm{BIAS}} = V_{\mathrm{PLUS}} = -V_{\mathrm{MINUS}}$, as shown in Fig.

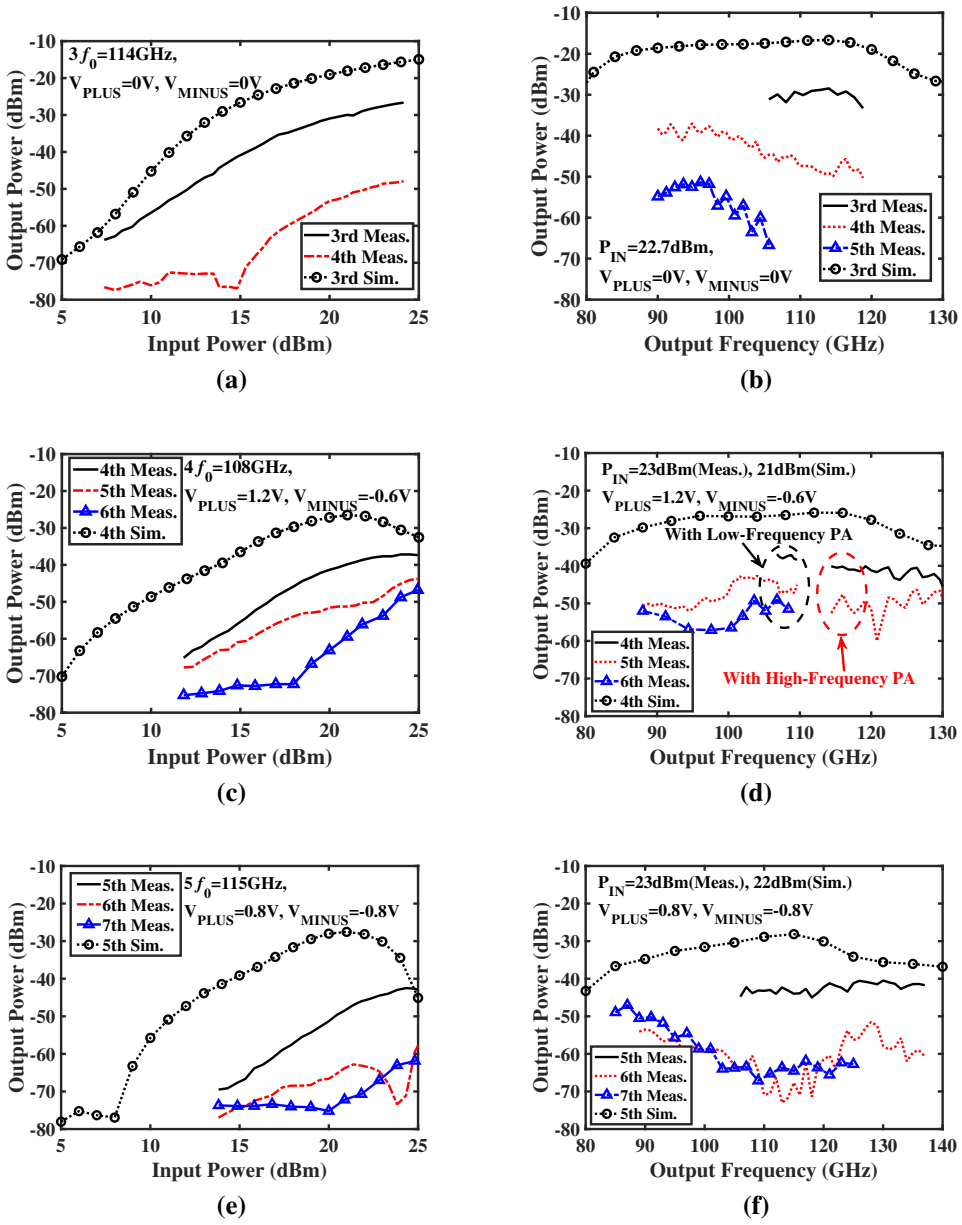


Figure 4.9: Dependence of simulated and measured P_{OUT}, and measured harmonics corresponding to the same fundamental input on P_{IN} and f_{OUT} for SCVP RFM: (a) and (b) $\times 3$; (c) and (d) $\times 4$; (e) and (f) $\times 5$.

4.10(b). When the V_{BIAS} is at 0 V, the C-V curve only has one valley, and the RFM can generate odd-order harmonics, with both strong third and fifth harmonics, as the simulation in Fig. 4.10(b) shows, noticing that the third harmonic is partially suppressed by the filters. However, when the V_{BIAS} is increased to about 0.8 to 1 V, the symmetric C-V curve is

changed to have two valleys, as shown in Fig. 4.6. In this V_{BIAS} range with the "2-valley" symmetric C-V curve, the fifth-order harmonic generation is enhanced, and becomes the strongest at 0.8 V in the measurement and at 1 V in the simulation, whereas the third-order harmonic is suppressed by about 20 dB. Prior works only realized that symmetric C-V curves can suppress even-order harmonics, whereas enhance odd-order harmonics. Here, it is proved in theory and measurements that symmetric C-V curves can also suppress the odd-order harmonics (here, it is the third harmonic). Not only the symmetric or asymmetric C-V curves can be used to enhance or suppress odd or even harmonics, the number and shape of the valleys and peaks are also important for the harmonics generation, which is elaborated in the theory of the SRPP in Section 2.3. In the range of "2-valley" symmetric C-V, the measured fifth harmonic also has a peak >20 dB higher than the sixth and seventh harmonics.

For the fourth-order harmonic generation of quadruplers, the C-V curves should be "2-valley" asymmetric based on the tunable C-V of the dual varactor pair, therefore V_{PLUS} is kept constant at 1.2 V, and the V_{MINUS} is swept from 0 V to -1.2 V. The generated harmonics versus V_{MINUS} are shown in Fig. 4.10(a). When the V_{MINUS} is around -0.6 to -0.4 V, the C-V curve, which is illustrated in Fig. 4.6, is "2-valley" asymmetric, and the required fourth harmonic is enhanced both in simulation and measurement, whereas all odd-order harmonics are suppressed in this voltage range. Although sixth harmonic is also enhanced in this voltage range with the asymmetric C-V, the peak of the sixth harmonic is well below the fourth by more than 10 dB. When the V_{MINUS} is reduced to -1.2 V, both the third and fifth harmonic are enhanced since the C-V curve becomes symmetric, whereas the even-order harmonics are suppressed. From Figs. 4.10(a) and (b), it can be seen that the third harmonics are suppressed with "2-valley" symmetric C-V at $V_{\mathrm{PLUS}} = 0.8$ V and $V_{\mathrm{MINUS}} = -0.8$ V, as well as "2-valley" asymmetric C-V at $V_{\mathrm{PLUS}} = 1.2$ V and $V_{\mathrm{MINUS}} = -0.6$ V; however, the third harmonic is enhanced when $V_{\mathrm{PLUS}} = 1.2$ V and $V_{\mathrm{MINUS}} = -1.2$ V, which corresponds to an approximately "2-valley" symmetric C-V. When V_{PLUS} and

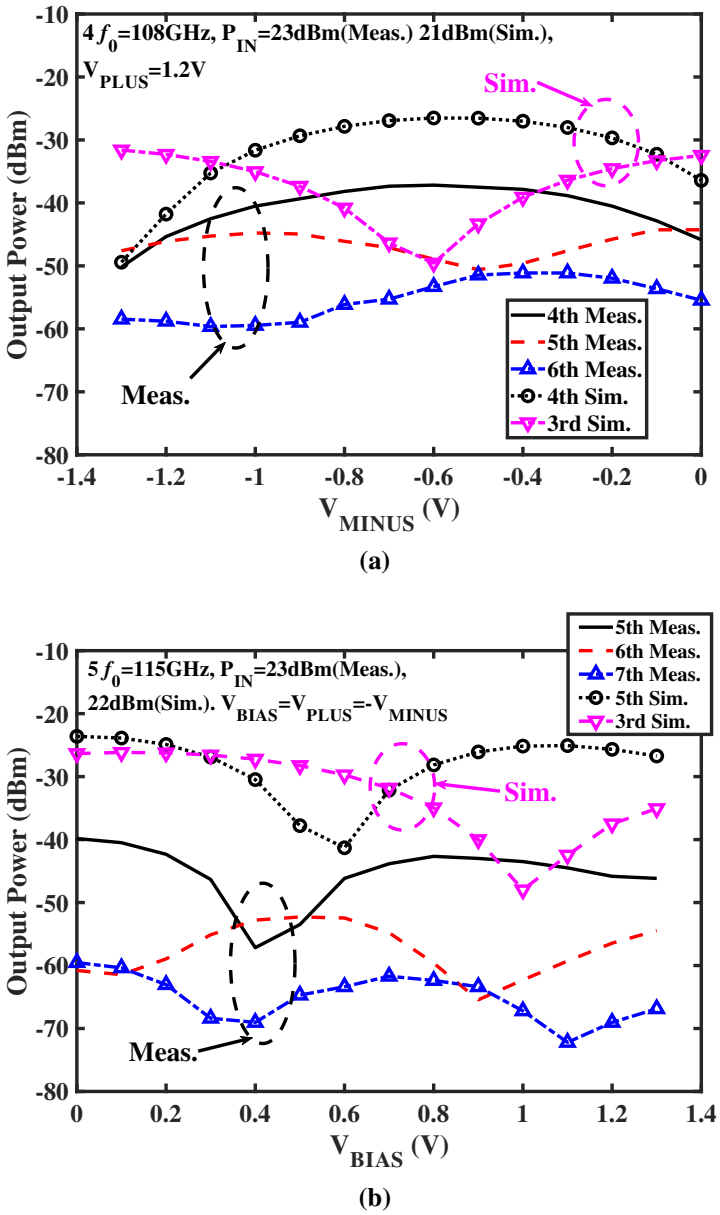


Figure 4.10: Dependence of P_{OUT} and harmonics on (a) V_{MINUS} with a constant V_{PLUS} for $\times$4 SCVP RFM; (b) V_{BIAS} for $\times$5 SCVP RFM.

V_{MINUS} are $\pm$1.2 V, the two valleys are far away from each other. Thus, under a given input power, the pumping cannot fully cover the total voltage range of two valleys resulting in the actual C-V curve within the pumping range to exhibit one peak, which generates the third harmonic.

The CLs of the SCVP RFM and APNVP RFM are compared in Fig. 4.11, with de-

pendence on P_{IN} and f_{OUT}. Some of the measurements are limited by the BW of the instruments as explained previously. For all key performance specifications, such as minimum CL, P_{OUT}^{max}, BW and harmonic rejection ratio, the SCVP RFM has a much better performance than the APNVP RFM. They are compared in the Table 4.1, which demonstrate the advantages of the SCV over the conventional MOS varactor. Since C_{BP}s are added in the layout of the SCVP RFM but do not exist in the layout of the APNVP RFM, for a fair comparison, SCVP RFM without these extra C_{BP}s is simulated to show the improvements compared with the APNVP RFM. The minimum CLs are improved by 11.4, 6.6, and 7.9 dB, and the relative BWs are improved by 3.3%, 90%, and 400%, defined as $100\%(\mathrm{BW}_{\mathrm{SCVP}}-\mathrm{BW}_{\mathrm{APNVP}})/(\mathrm{BW}_{\mathrm{APNVP}})$, for the $\times 3$, $\times 4$, and $\times 5$ multiplications, respectively, without the added C_{BP}s in the layout.

Although most of the trends in the measured curves match the simulation, there are discrepancies in the CL as well as P_{OUT} in values between the measurements and the simulations. The reason for the discrepancies is possibly due to the parasitics parameters not included in the post layout extractions and the EM simulation of the total layout. As explained in Section 4.3, adding C_{BP}s improves the total performance such as CL and BW, which means that good RF ground of the varactor pair device is critical for the RFM performance. The APNVP and C-SCVP topologies directly use V_{PLUS} and V_{MINUS} as RF ground. This is an important difference from the SAPSV, which only uses V_{PLUS} and V_{MINUS} for dc biasing. Therefore, it is suggested that making use of the biasing technologies in SAPSV may improve the performance of SCV-based parametric circuits.

The performance of the SCVP RFM is also compared with the only other RFM found in [70], which is an active RFM using waveform shaping and operating around 200 GHz, for $\times 4$, $\times 6$, and $\times 8$ multiplications. Although the active RFM can provide a maximum conversion gain up to 7 to 10 dB, as well as a higher P_{OUT}^{max} , it needs an on-chip multiple-stage PA, and the active multiplier with the PA consumes 63 mW of dc power in a SiGe bipolar CMOS (BiCMOS) process, whereas passive multipliers consume no dc power,

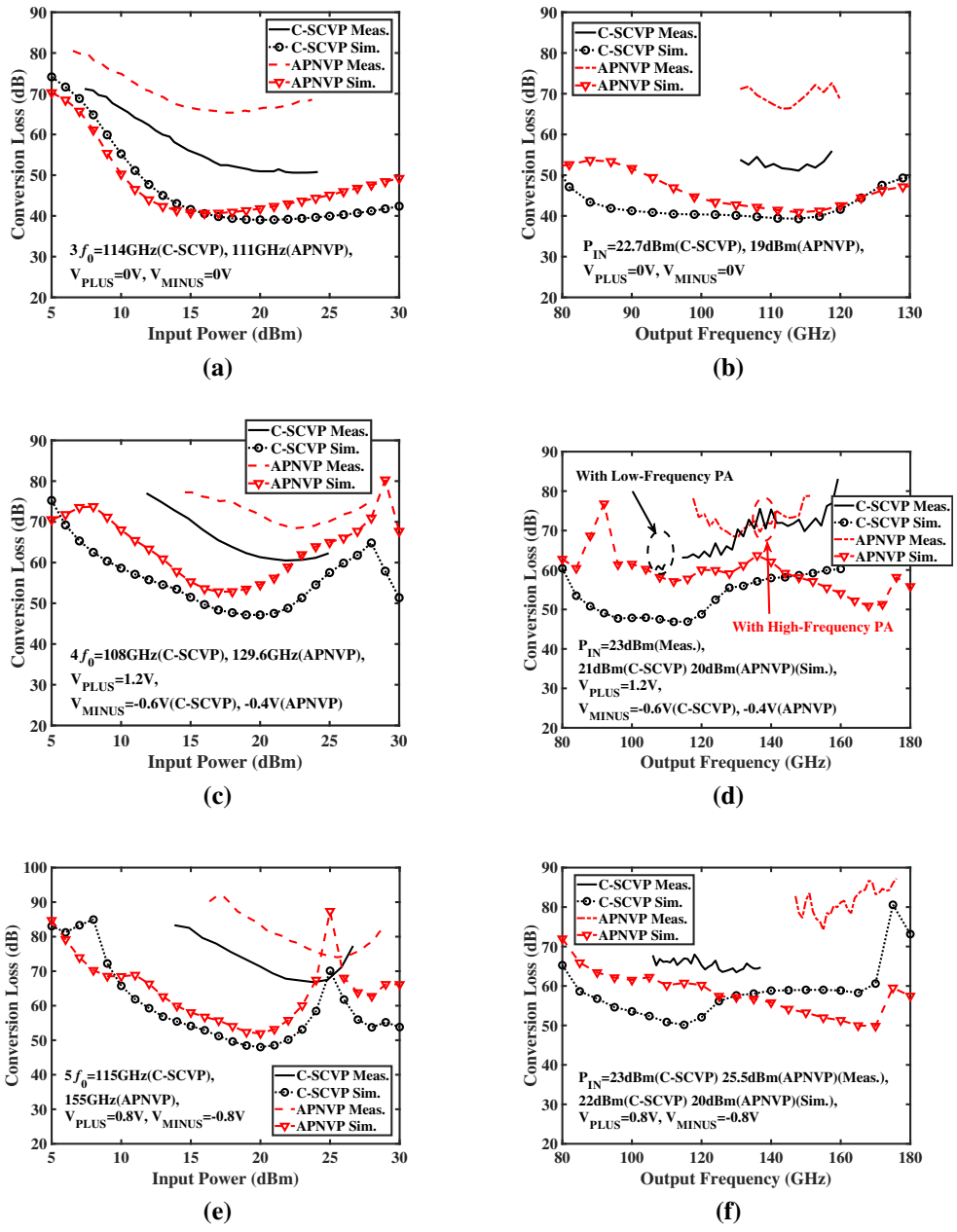


Figure 4.11: Dependence of simulated and measured CL on P_{IN} and f_{OUT} for SCVP RFM and APNVP RFM: (a) and (b) $\times 3$; (c) and (d) $\times 4$; (e) and (f) $\times 5$.

though passive RFM cannot amplify the output signal. The active RFM not only has a limited relative BW (defined by 5-dB for both works), but also has a limited harmonic rejection ratio as low as about 5 dBc when the N becomes high, showing that the active RFM generates much stronger unwanted harmonics with a large N. For both SCVP RFM and ac-

Table 4.1: Performance summary and comparison of the SCVP RFM and APNVP RFM

Appr.	**C-SCVP**			APNVP		
N	**×3**	**×4**	**×5**	×3	×4	×5
Output Freq. (GHz)	**83 to 123**[a]	**86 to 123**[a]	**106 to 137**[b]	96 to 126[a]	124 to 141	152 to 160
BW[c] (%)	**38.8**[a]	**35.4**[a]	**25.5**[b]	27[a]	12.8	5.1
Min. CL (dB)	**50.6**	**59.9**	**63.5**	65.4	67.7	75
P_{OUT}^{max} (dBm)	**−26.6**	**−37.2**	**−40.5**	−44.8	−45	−48
HRR (dBc)[d]	**>13 (4th) >26 (5th)**	**>7 (5th) >12 (6th)**	**>10 (6th) >17 (7th)**	>4 (4th) >11 (5th)	>6 (5th)	NA

[a] Measured frequency range between about 106 to 120 GHz is limited by the lowest frequency of the frequency extenders for ×3 and ×4, and the maximum frequency of the PA for ×3. [b] The measured frequency range is limited by the instruments. [c] 5-dB BW. [d]In the measured 5-dB BW with the given P_{IN}.

tive RFM, the performances become worse when N becomes high; however, for the SCVP RFM this is due to the tunable varactor pairs with limited r_c when the C-V is converted from a high-r_c valley to two low-r_c valleys. If the high N FM is designed independently, f_{cd} of the varactor pairs can be further improved for better performance, whereas waveform shaping topology is based on the clipping of the waveform, which may meet difficulties to improve the performance with very high N as the trend shows in [70]. Although the SCVP RFM has a slightly larger chip size compared with the active RFM, it is due to some layout choices of filtering and matching networks for the broadband operation, and the size can be further reduced with folded TLs, and by removing the optional HPF at the price of less suppression to some lower frequency harmonics.

4.5 Conclusion

A shunt SCV is proposed to replace the conventional MOS varactors in mm-wave and THz parametric circuits with nearly 10 times higher ratio of maximum to minimum capac-

Table 4.2: Performance summary and comparison of the SCVP RFM and the active RFM

Ref.	**C-SCVP (This work)**			TMTT'19 [70][a]		
Tech.	**22-nm SOI CMOS**			0.13-μM SiGe BiCMOS		
Appr.	**C-SCVP**			Waveform Shaping		
N	$\times$**3**	$\times$**4**	$\times$**5**	$\times$4	$\times$6	$\times$8
Output Freq. (GHz)	**83 to 123**	**86 to 123**	**106 to 137**	168 to 208	168 to 216	176 to 216
BW (%)	**38.8**	**35.4**	**25.5**	21.3	25.0	20.4
Min. CL (dB)	**50.6**	**59.9**	**63.5**	-7	-10	-8
P_{OUT}^{max} (dBm)	$-$**26.6**	$-$**37.2**	$-$**40.5**	-9	-6	-8
HRR (dBc)[b]	**>13 (4th) >26 (5th)**	**>7 (5th) >12 (6th)**	**>10 (6th) >17 (7th)**	>26 (3rd) >17 (5th)	>18 (5th) >25 (7th)	>5 (6th) >23 (7th)
P_{DC} (mW)	**0**			63		
Chip Area (mm^2)	**0.96**			0.78		

[a] Performance of [70] is extracted from figures. [b] In the measured 5-dB BW with the given P_{IN}.

itance as well as a high f_{cd}, which results in a significant improvement of the performance of the parametric multipliers. Based on the harmonic generation theory with SRPP, the third-, fourth-, and fifth-order broadband reconfigurable frequency multipliers are designed and fabricated based on C-SCVPs and APNVPs in the D-band. Better performance in terms of lower minimum CL, higher P_{OUT}^{max}, wider relative BW, and better HRR of adjacent unwanted harmonics are achieved by the SCVP RFM compared with the APNVP RFM, demonstrating the potential of the SCVs to replace MOS varactors in future mm-wave and THz parametric circuits.

Chapter 5

D-Band Broadband Passive Frequency Tripler Using Antiparallel Diode-Connected nMOS Transistor Pair

An antiparallel diode-connected nMOS transistor pair (APDNP) based passive tripler was designed for the D-band. This resistive tripler is capable of operating over a wide 27.8% 5-dB bandwidth from 93 to 123 GHz with a maximum -16 dBm output power. The back-gate voltage (V_{BG}) can be used to control nonlinearity of a variable resistance to optimize P_{OUT} and CL of the tripler, for a range of input power levels, especially when the P_{IN} is high. About 2-dB improvement in the P_{OUT} and CL is achieved by only tuning V_{BG}. The tripler is implemented in a 22-nm CMOS SOI process, and avoids the use of Schottky diodes in conventional resistive triplers.

5.1 Background

Schottky barrier diodes (SBDs) have long been used not only in resistive multipliers, but also as candidates for emerging CMOS THz transceivers, such as an 860-GHz imager for incoherent detection [10], and future potential THz mixers for coherent detection [12]. As discussed in Chapter 2, the symmetric R-V curves based on symmetric I-V curves of antiparallel-diode pairs (APDP) are widely used for passive frequency triplers [32, 33, 44, 61], with a suppression of even harmonics. Compared with reactive passive multipliers with MOS varactors or varactor-mode diodes, the operating BW can be made larger, though the CL is typically higher due to the lossy nature of the varying resistance. For example, a 60-to-110 GHz broadband tripler is reported in [44], and a tripler with 4-dBm P_{OUT} in [61], which were both developed based on antiparallel GaAs diodes with microstrip-line and waveguide matching networks. However, passive triplers in CMOS, including the varistor triplers, still exhibit a limited BW and low P_{OUT}^{max}, such as $P_{\mathrm{OUT}}^{max} = -25$ dBm and BW = 10% in [32], and $P_{\mathrm{OUT}}^{max} = -19$ dBm and BW = 15% in [33]. The limited BWs of CMOS

varistor FMs are possibly due to the parasitic capacitance of the SBD and limited BW of the filtering and matching networks. Active multipliers have also been reported in D-band [73] and [74]; however, the odd-order active FMs in [73] and [74] consume high P_{DC} and large chip area, whereas compact passive triplers only consume zero P_{DC}. The efficiencies of the active FMs also drop very fast at even higher frequencies, where passive circuits and components still dominate.

Although SBDs can be integrated with modern CMOS technologies, they incur extra fabrication costs of device layers on silicon substrates [32,33], or non-silicon [42,44,61,75]. [75] and [42] present diode multipliers operating in varactor mode (i.e., the diode is biased in the variable capacitance mode). MOS varactor triplers, such as in [30], do not need extra process modifications. As in the CMOS SAPSV tripler described in Chapter 3, the capacitance ratio and total f_{cd} are improved to achieve a 24-dB CL and −8-dBm P_{OUT}^{max} in the 28-GHz band. The total BW of the SAPSV tripler is limited to 18%, which is larger than in [32] and [33], but an even larger BW may be expected for varistor FMs. Other varactor FMs, such as AMOSV in [30] and HBV in [76], are reported with limited BWs of 12%, which are harder to impedance match over wide frequency ranges than varistor multipliers, e.g. as wide as about 60% relative BW of [44]. Noting that the diode-connected nMOS transistors have been demonstrated with THz operating capability, as in the 0.3-THz CMOS receiver in [13], the antiparallel diode-connected nMOS transistor pairs, named APDNPs, are seen as potential replacements for the APDPs in the mm-wave and sub-THz frequency multipliers.

There are some barriers for using diode-connected MOS FETs in the CMOS D-band passive triplers, including large parasitics and a high non-flexible forward voltage drop due to the structure of the conventional MOS FETs. A floating-body biasing topology in [13] is used to mitigate the undesired asymmetry of body effect of MOS FETs, to obtain higher rejection of the second harmonic, as shown in [12]. However, the floating-body topology cannot remove all the parasitics, such as the body-to-well capacitance, whether the body is

floating or not. An SOI technology naturally removes parasitics from drain and source to body or well by insulating the transistor from the substrate. The well under the insulator serves as a back gate, instead of a body terminal of the FET in the conventional CMOS process. The back-gate voltage (V_{BG}) can tune the threshold voltage of the transistor and, therefore, can enlarge the cutoff region (also known as "off zone" in [33]) of the diode pairs, and modify the nonlinearity of the APDNPs to improve the CL.

For passive APDP FMs, CL exhibits a large variation when P_{IN} varies in the operating range, such as 10 dB variation of CL with a P_{IN} from -2 to 8 dBm in [32]. Due to the low barrier of SBDs, the minimum CL of an SBD tripler is typically obtained at a low P_{IN}. When P_{IN} is further increased, the CL could worsen and increase, resulting in a nonlinear behavior of CL and a limited P_{OUT}^{max}. Although the CL of this passive tripler is slightly larger due to the loss of the broadband passive networks composed of filters, this D-band frequency tripler benefits from the higher threshold voltage of the diode-connected MOS FETs tuned by the V_{BG}, achieving a higher P_{OUT}^{max} to -16 dBm measured at 111 GHz, and about 2 to 3 times better relative BW than the SBD and varactor triplers in CMOS [30, 32, 33].

5.2 Circuit Description

The SB-CAPDP topology in [33] is an improvement of the simple APDP as shown in Fig. 5.1(a). SB-CAPDP uses a bias capacitor C_{BIAS} at the cathode of the n-SBD and a bias resistor (R_{BIAS}) to apply a biasing voltage (V_{BIAS}) to tune the I-V curve of the n-SBD. As in the discussion in Section 3.2, though SB-CAPDP can tune the nonlinearity by using V_{BIAS} or self-biasing, it has two major drawbacks. First, only the n-SBD side is tuned to modify the I-V curve, thereby the nonlinearity is non-symmetric around the zero bias point. Second, since the V_{IN} node is used for self biasing, all metal traces connected to the V_{IN} node should also have bypass capacitors when they are connected to mm-wave shunt stubs to ground, which adds an extra cost for dc biasing. These extra bypass capacitors are not

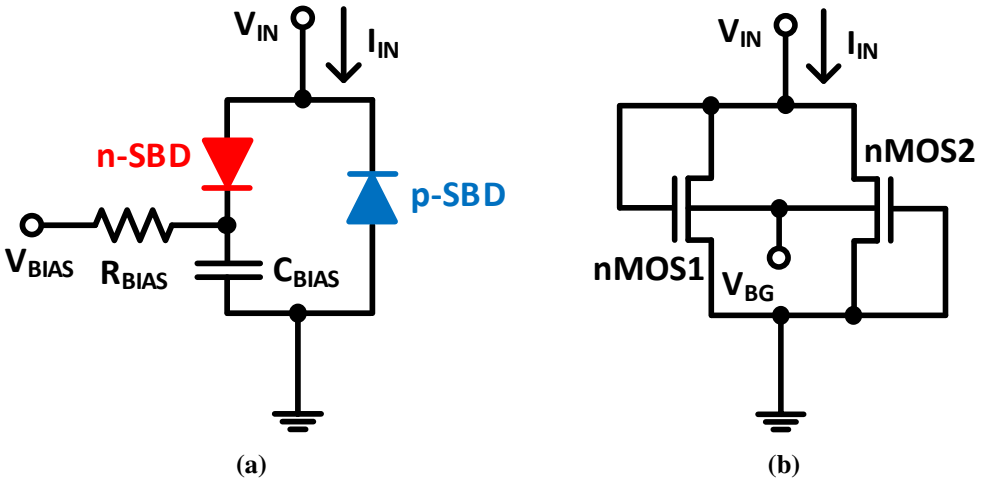
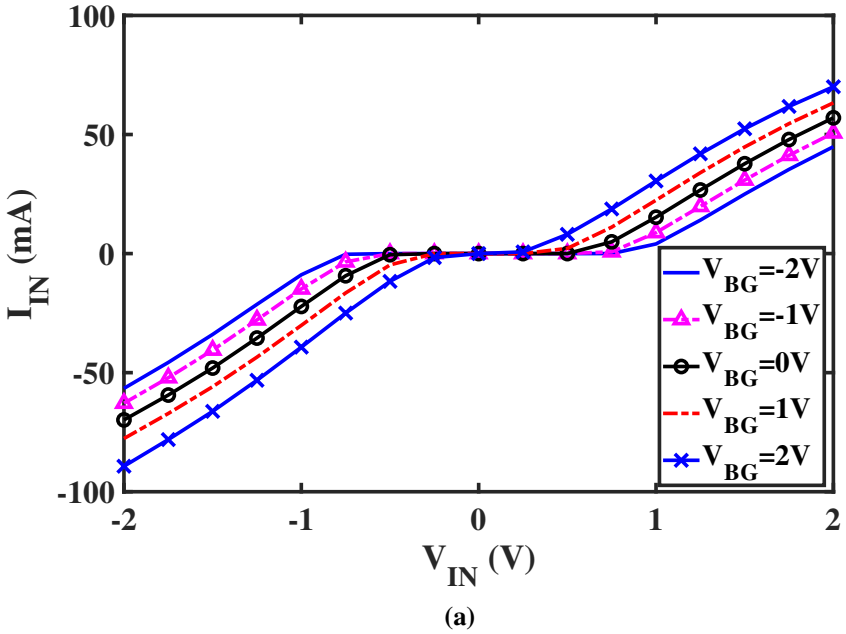


Figure 5.1: Topologies of diode pairs. (a) SB-CAPDP. (b) APDNP.

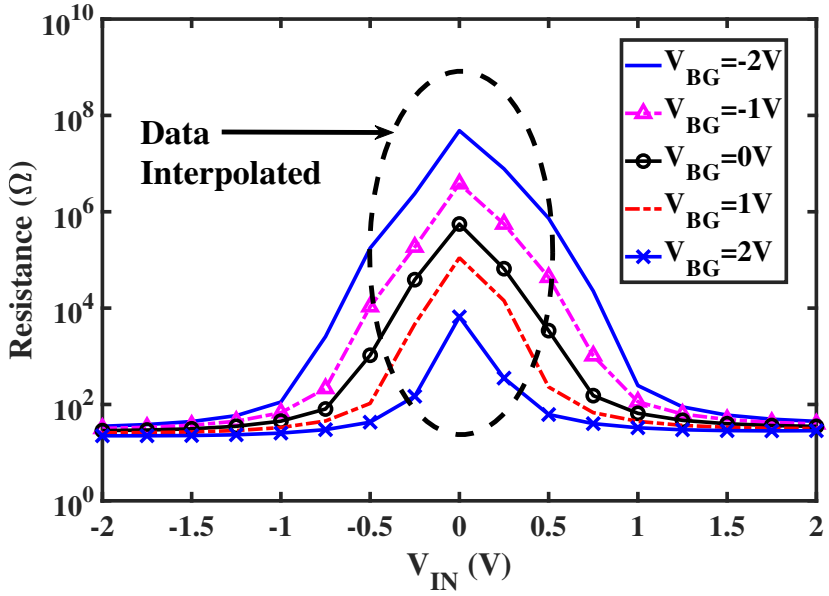
shown in Fig. 5.1(a).

Alternatively, the APDNP topology in Fig. 5.1(b) requires no extra bypass capacitors or resistors implemented in the CMOS SOI process, since the back-gate node is connected to the p-well under the insulator, which is naturally isolated from the transistors. Although SOI technology is free of device latch-up problems, it requires back-gate voltage V_{BG} connected to the p-well to be negative, e.g. -2 to 0 V, to avoid forward biasing p-n junctions in the substrate. However, if the n-well enclosing the p-well from all directions is connected to the highest supply voltage (VDD), V_{BG} can be positive to lower the threshold voltage of the MOS FETs. Since this design is fully passive, VDD is only connected to the n-wells for better p-n isolation purpose, not to the transistors.

To illustrate the advantages of the APDNP in Fig. 5.1(b), the circuit dc I-V curves are measured from the input terminal to the ground through the diode-connected transistors, as shown in Fig. 5.2(a), where the current direction is indicated by I_{IN} in Fig. 5.1(b). When V_{BG} is decreased, the cutoff region of the transistors is enlarged due to the increase of the threshold voltage. It means V_{BG} can be used to tune the nonlinearity of the device efficiently and symmetrically due to the simultaneous change of I-V curves of both sides, instead of one side from SB-CAPDP in Fig. 5.1(a). The measured R-V curves are shown



(a)



(b)

Figure 5.2: Measured characteristics of the total two APDNPs of the tripler depending on V_{BG}. (a) I-V curves. (b) R-V curves.

in Fig. 5.2(b), which are nearly symmetric for triplers, and can be tuned by V_{BG}. Since the current near $V_{IN} = 0$ is too small and out of the range that the instrument can measure, the R-V curves near zero V_{IN} are interpolated from the measured curves. From Fig. 5.2(b),

the ratio between maximum and minimum resistance (r_r) is dramatically increased, when the cutoff region is enlarged. Since the APDNPs used for triplers are varistors pumped by V_{IN}, the cutoff frequency can be calculated using the method from [77], which reaches 420 GHz for this design, and is high enough for the D-band applications. Provided P_{IN} is high enough to fully pump the varistors, with higher r_r by reducing V_{BG} (i.e., the threshold voltage is increased), the CL and P_{OUT} can be both improved, under a given high P_{IN}. Noticing that further increasing P_{IN} after a "saturation" can worsen CL and result in a decrease of the power level of the generated harmonic, tuning capacity from V_{BG} improves the FM performance at even higher P_{IN}, and both better minimum CL and P_{OUT}^{nax} can be achieved. On the other hand, with increasing V_{BG} and lowering the threshold voltage, the input signal with low P_{IN} can still traverse beyond the shrunk cutoff region, thus the achievable r_r is increased for the signal and CL can be improved. The benefit of lowering voltage drop of SBDs at low P_{IN} was observed previously in SB-CAPDP triplers in [33]. Since SBDs are a hybrid of variable resistance and capacitance, even if the diode pairs are connected in a varistor mode instead of a varactor mode, their variable capacitance can still influence the total FM performance. For MOS FETs, instead of a MOS-varactor connection topology described in Chapter 3, i.e. the source and drain terminals of the nMOS FETs are connected, the diode connection topology only connects gate and drain terminals of nMOS FETs. In this SOI CMOS process, the diode-connected MOS FETs only have an about 1.3 ratio of capacitance change simulated from the Y-parameters at 40 GHz. Therefore, the influence of the varying capacitance is small, and the varying resistance dominates, whereas a MOS FET connected in varactor mode exhibits a capacitance ratio as about 3 typically in this technology.

The schematic of the resistive tripler is superposed on the chip micrograph shown in Fig. 5.3. Totally two APDNPs are placed in the top and bottom of the layout, respectively. The D-band passive tripler has the same passive filtering and matching parts of the layout as the RFM design described in Chapter 4. The only major difference is that the two dc

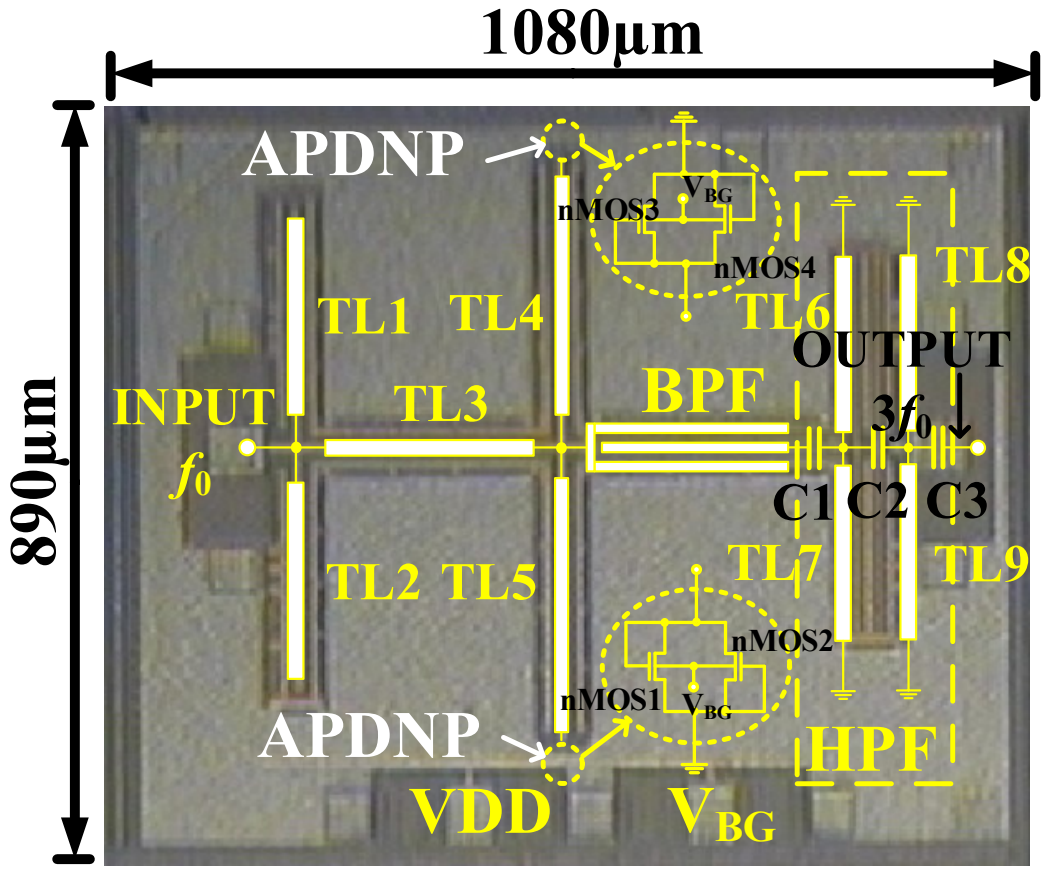


Figure 5.3: Die micrograph and the total schematic of the APDNP tripler.

signals used for probing in measurements are VDD and V_{BG}, instead of V_{PLUS} and V_{MINUS} in the D-band RFM. Since V_{BG} is not used for the passive SCVP RFM, VDD connection is optional for the RFM.

To avoid repetitive discussion in the passive layout design of the passive FM, which has been discussed in Section 4.3, it is neglected in this chapter. One important aspect is that the BPF and HPF each add about 3 to 4 dB loss to the total CL in this desired frequency band. Although both filters operate together to get the flat frequency response in the D-band, the HPF with an about 86-GHz cutoff frequency can be removed to reduce the total CL. However, without HPF the suppression to the fundamental and second harmonic would be worsened, and the total pass band would be extended and moved to a much lower frequency, due to the nature of the broadband resistive FMs. Per simulations, the second-harmonic rejection would degrade by 10 to 15 dB without the HPF. Since the D-band

tripler operates at a very high frequency, the other harmonics are far away from the required frequency band. Also the D-band rectangular waveguides (WR), used for conducting the high-frequency output signals, can naturally suppress other harmonics out of the designated frequency band, thereby the price is considered to be acceptable when operating in the D-band with a second harmonic in the range of about 60 to 80 GHz.

5.3 Measurement Results

The fabricated chip of the passive tripler was measured by wafer probing, which is shown in Fig. 5.4. The input signal at f_0 is fed from a 40-GHz signal generator and amplified by a 40-GHz PA. These instruments in the input side limit the upper output frequency range up to 120 GHz. A D-band WR6.5 frequency extender limits the measurable lower frequency to about 106 GHz. The 0.8-V VDD, which is applied for isolation purpose, as well as the tunable V_{BG} are provided by an external dc supply. As there is no dc current drawn through VDD, the passive tripler consumes zero dc power. The output signal is downconverted by the frequency extender to about 270-MHz IF, and then measured by a spectrum analyzer, calibrated based on the CL from the down-conversion. The calibration steps are the same as those introduced in Section 4.4.

The measured and simulated P_{OUT} and CL versus output frequency ($3f_0$) are shown in Fig. 5.5. The measured 5-dB BW is limited by the BW of the instruments to about 106 to 120 GHz, whereas the tripler is designed and simulated to have a broad BW from 93 to 123 GHz. In the measured frequency range, the minimum CL of 38 dB and the maximum P_{OUT} well match the simulation under $P_{\mathrm{IN}} = 20$ dBm as shown in Fig. 5.5. The measured fourth and fifth harmonics with dependence on $3f_0$ corresponding to the same fundamental input are also shown in the figure. The harmonic rejection ratios reach 46 and 16 dBc in the available measured frequency range for the fourth and fifth harmonics, respectively.

The measured and simulated P_{OUT} and CL versus P_{IN} at 111 GHz as well as the measured fourth harmonic are shown in Fig. 5.6. Other harmonics are out of the measurable

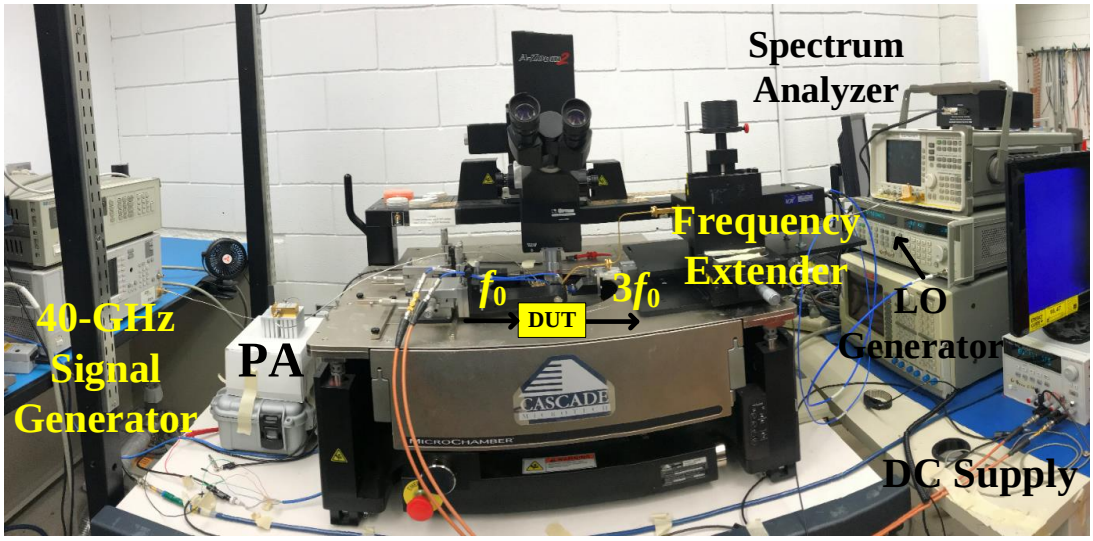


Figure 5.4: Measurement setup.

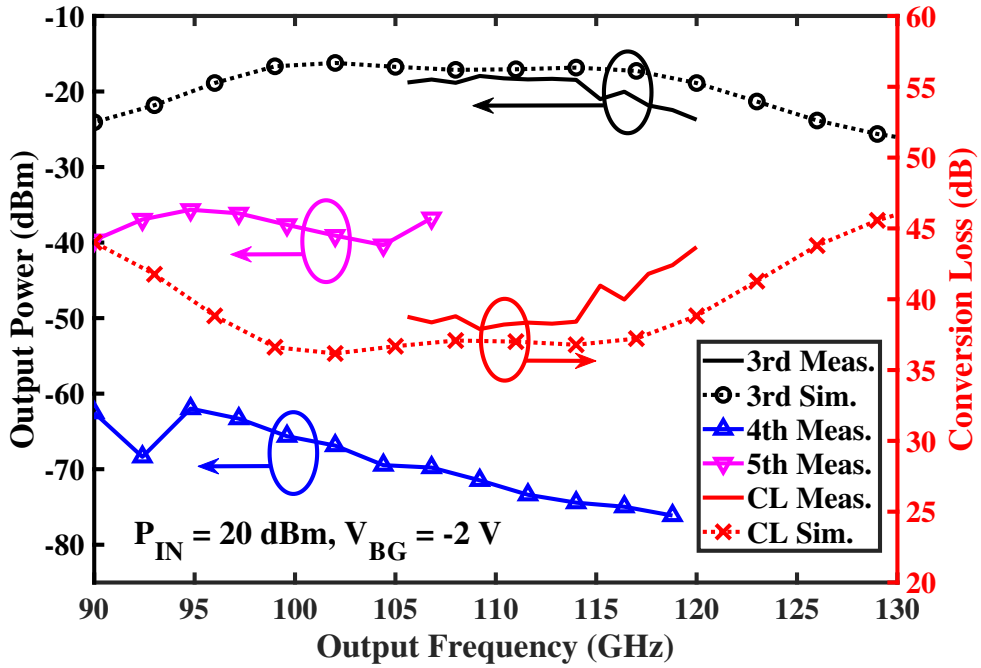


Figure 5.5: Measured and simulated P_{OUT} and CL versus $3f_0$ at a 20-dBm P_{IN} and measured fourth and fifth harmonics versus $3f_0$ relative to the fundamental input.

frequency range. The measured P_{OUT}^{max} reaches -16 dBm at 24-dBm P_{IN}. The variation in CL is less than 5 dB when the P_{IN} is in the range from 14 to 24 dBm, where the measured fourth harmonic stays 46 dB below the desired third harmonic. The diode-connected MOS FETs in APDNP can handle a P_{IN} as high as 24 dBm without any observable damage or

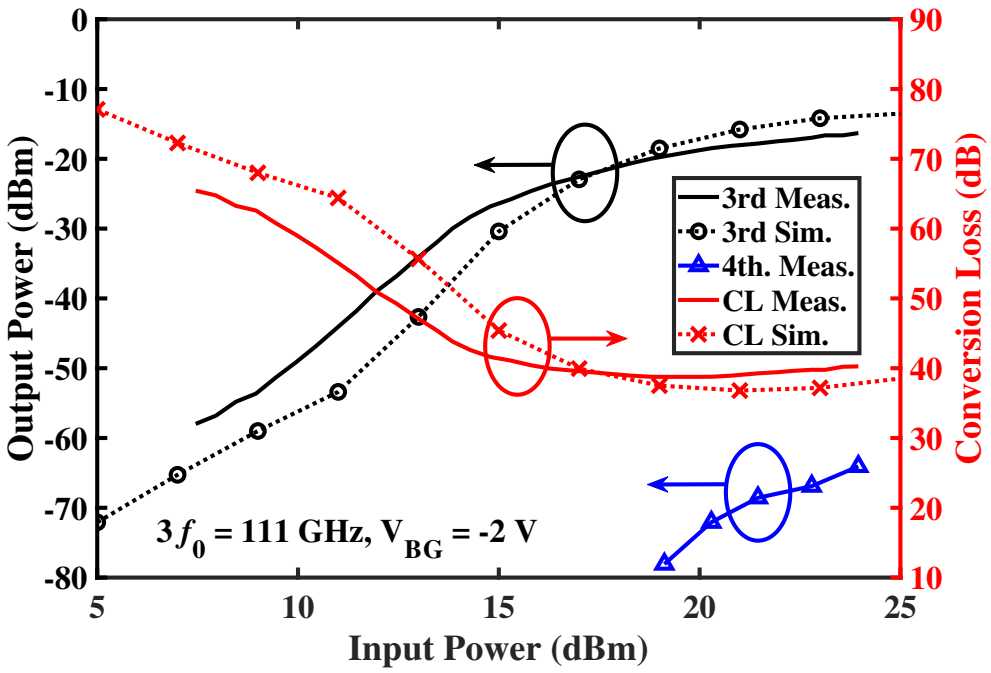


Figure 5.6: Measured and simulated P_{OUT} and CL versus P_{IN} at 111 GHz, and the measured fourth harmonic relative to the same fundamental input.

failure of the devices in the measurement, which guarantees the high power operation for mm-wave applications.

The P_{OUT} tuned by the back-gate control, under given 20-dBm P_{IN} at 111GHz, is shown in Fig. 5.7. The P_{OUT} is improved by 1.7 dB when V_{BG} is tuned from 0 to -2 V. Since P_{IN} is held constant in the process, the CL is also improved by 1.7 dB, without any extra cost. The tuned power performance is measured with a 0.1-V step and a 1/6-dB resolution achievable by the spectrum analyzer. As expected from the harmonic generation theory, the simulations, and the measurements, reducing V_{BG} improves both third-order P_{OUT} and CL at high P_{IN} level with increased ratio of the nonlinear resistance.

The comparison with other passive and active triplers higher than 100 GHz is given in the Table 5.1. Within the measurement window of 106 to 120 GHz, there is a close agreement between measured results and the simulations, which suggests that the simulation results are sufficiently accurate. For comparison purpose, one active tripler in InP technology [73] is also given, exhibiting a conversion gain and a high output power at 14

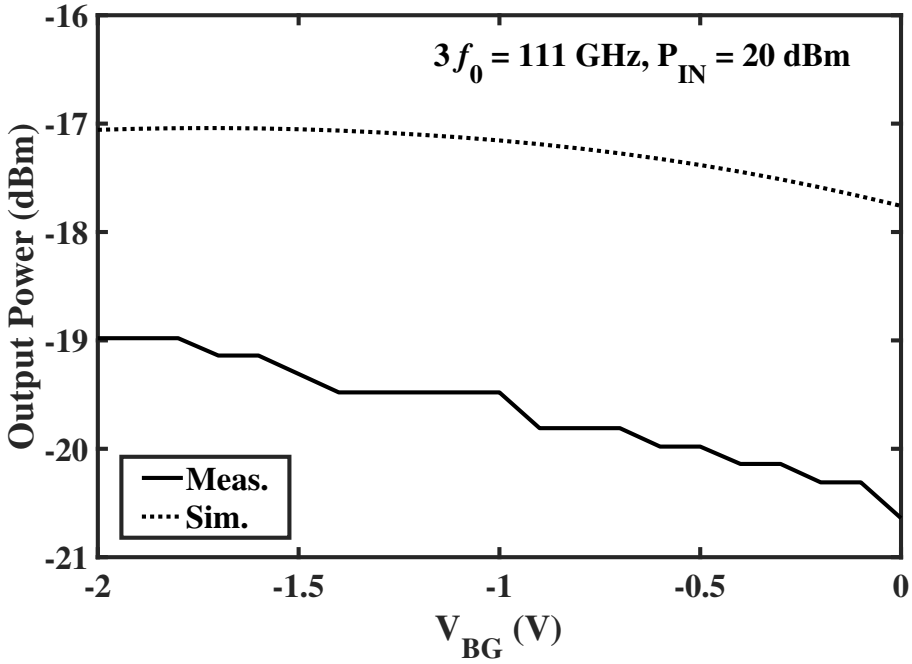


Figure 5.7: Measured and simulated P_{OUT} versus V_{BG} tuned for higher P_{OUT} at 111 GHz and 20-dBm P_{IN}.

dBm; however, the active InP tripler consumes 156-mW P_{DC}. The passive GaAs tripler in [44] can provide an about 60% BW and -3-dBm P_{OUT}, but it is not integrated in CMOS and needs bulky TL matching networks, whereas this APDNP tripler shows a dramatically smaller chip size in a commonly used and less expensive process. The 27.8% BW and -16 dBm P_{OUT}^{max} are best in the reported CMOS passive D-band FMs among [30, 32, 33]. Although the tripler is implemented with larger size than some other prior designs, it is solely due to its fully balanced structure and layout choices rather than inherent circuit requirements, given the passive part of the layout was the same as the broadband reconfigurable SCV FM in Chapter 4. The CL of this APDNP tripler is larger than other passive FMs in the table; however, this is due to the trade-off between P_{OUT}^{max}, BW, harmonic suppression, and CL, e.g. 2 to 3 times relative BW is achieved with only several dB increase in CL compared with other SBD-based resistive FMs in [32] and [33]. If the HPF following the BPF was removed from the design, which was not used in [32], [33] and [30], the circuit would obtain the same level of CL in the resistive FMs [32] and [33], with a much higher P_{OUT}^{max}

Table 5.1: Comparison with state-of-the-art 100-GHz frequency triplers

Ref.	**This Work**	[33]	[32]	[30]	[44]	[73]
Appr.	**APDNP**	SB-CAPDP	CAPDP	AS-VAR	APDP	Active
Tech.	**22-nm CMOS SOI**	0.13-μm CMOS	0.13-μm CMOS	0.13-μm CMOS	GaAs	250-nm InP
N	**×3**	×3	×3	×3	×3	×3
Freq. (GHz)	**93 to 123**[a]	146 to 170	144 to 159	96 to 108	60 to 110	90 to 141
BW[c] (%)	**27.8**[a]	15.2	9.9	11.8	58.8	44.2[e]
Min. CL (dB)	**38 (34 to 35)**[g]	32	34	27.5	19[b, d]	−13
P_{OUT}^{max} (dBm)	**−16** $P_{\mathrm{IN}} = 24$ **(−12 to 13)**[g]	−18.6 $P_{\mathrm{IN}} =$ 13.4	−25 $P_{\mathrm{IN}} = 11$	−20 $P_{\mathrm{IN}} = 7.5$	−3[b, d] $P_{\mathrm{IN}} = 16$	14.2 $P_{\mathrm{IN}} = 2$
4th HRR (dBc)	**≥46**	NA	NA	NA	≥15	NA
5th HRR (dBc)	**≥16**	NA	NA	NA	≥10	NA
Chip Area (μm^2)	**1080 ×890**	540×410	740×470	2000 ×1500	6000 ×900[f]	1900 ×960

[a] Measured 106 to 120 GHz range is limited by the instruments. [b] Estimated from figures. [c] 5-dB BW. [d]In the range from 100 to 110 GHz. [e]3-dB BW. [f]Al_2O_3 substrate. [g]Estimated without the optional HPF.

and much larger relative BW (the lower limit of the frequency range would be expanded to a much lower frequency) than the original design, although as such the FM would operate mainly out of the D-band and the measurable range of the setup.

5.4 Conclusion

An mm-wave APDNP topology based on diode-connected MOS FETs for frequency multiplication was implemented in a broadband passive tripler with a −16 dBm P_{OUT}^{max} and 93-to-123-GHz operating BW in the 22-nm CMOS SOI technology. The balanced topology with

broadband TL-based filtering and matching networks is designed to operate over a 27.8% relative BW, and is verified in the available measurement range from 106 to 120 GHz. The close agreement between simulations and measurements supports the validity of the simulation results. Back-gate voltage is used to tune the I-V and the resulting R-V nonlinearity of the diode-connected transistors, which shows a 1.7-dB improvement in the P_{OUT} and CL under a given constant 20-dBm P_{IN}. The APDNP of this design can reliably handle an input power as high as 24 dBm, and the fourth- and fifth- harmonic rejection ratios in the measured frequency range reach 46 and 16 dBc, respectively. The APDNP topology is demonstrated in this work to be a cost-efficient alternative to the SBD APDP topology with high P_{OUT}^{max} and wide BW in future mm-wave and sub-THz frequency multipliers.

Chapter 6

Voltage-Controlled Inductor in a D-Band Colpitts Third-Harmonic-Extracted Injection-Locked Oscillator

D-band oscillators can be built as the signal source of the THz LO multiplier chains, as well as the harmonic pump signal of the THz parametric circuits. In Chapter 4, an SCV topology is used to significantly improve the capacitance ratio r_c of the varactor operating in the mm-wave frequency band, and the similar concept can be used to tune the equivalent inductance of a tunable LC tank in the mm-wave band, by using a variable capacitance device, named transistor-controlled capacitor (TCC).

In this chapter, an mm-wave voltage-controlled inductor (VCI) based on the series LC tank is presented and achieves a large ratio of maximum to minimum inductance (r_L) with a quality factor Q about 5 to 12 at 40 GHz. For demonstration of the mm-wave VCI, a D-band Colpitts third-order-harmonic-extracted injection-locked oscillator (ILO) is designed in the 22-nm CMOS SOI technology, without using any MOS varactors. The third-harmonic voltage-controlled ILO (IL VCO) operates from 112.5 to 135 GHz, tuned through a VCI with $r_L = 4$. The dc power consumption of the ILO is 13 mW with a 1.2-V supply, but is reduced to 5.6 mW with a 0.8-V supply when a 2-V back-gate voltage (V_{BG}) is used. Thanks to the small size of the VCI and the removal of MOS varactors, the core chip area of the ILO excluding the output filter is only 0.018 mm^2. The total tunable operating frequency range is no less than 16%, and the added phase noise (PN) is about 10 dB, which is close to the theoretical prediction of $20\log(3) = 9.54$ dB.

6.1 Background

High-frequency on-chip variable inductors have wide applications to tune the operating frequency ranges of devices and circuits, such as VCOs, FMs, and filters. Non-electrical methods have been used to develop integrated variable inductors with microelectromechan-

ical systems (MEMS) , such as electrothermal-actuated variable inductors, out-of-plane variable inductors, and magnetic flux-tuned inductors with movable metal plates [78].

To avoid the expensive MEMS, the electrical methods are developed as a cost-efficient approach of the variable inductors on chip. One electrical approach utilizes the inductor arrays with switches (SWs) to tune the sum of the total inductance of sectional inductors [79]. Although this approach can obtain a relatively large ratio of the inductance, it requires a large chip area to connect the inductors in series, and it needs a number of SWs reducing the total Q of the tank and adding parasitics. As a result, the inductor arrays are better for achieving high total inductance, such as 140 to 300 pH in [79], but are likely not very suitable for very small inductance, which limits its potential applications at a very high frequency.

The other approach utilizes transformers, wherein the load impedance of a secondary coil has an influence at the primary. When the load is tuned by a voltage or current, by using transistors, varistors, or varactors, the inductance seen from the primary coil is variable [80]. When the tuning parameter is a voltage, a VCI is realized, such as the one in [80]. The performance of the transformer-based VCI is limited by the coupling efficiency of coils, e.g., the ratio r_L of maximum inductance (L_{max}) to minimum inductance (L_{min}) is only limited to 1.2 (tuned from -1 to 1 V) in [80], and 1.7 (tuned from 0 to 8 V) in [81].

To achieve a large r_L and a high Q in the mm-wave band, a VCI composed of LC tanks with a large tuning range (TR) and compact size is proposed and demonstrated in the D-band third-order-harmonic-extracted ILO, without using conventional varactors of which the r_c is limited in the mm-wave band.

6.2 VCI Design

The VCI benefits from the development of SCV in Chapter 4, though different design considerations are taken for VCI. The concept of this VCI is based on the shunt series LC tank as shown in Fig. 6.1(a). When the capacitance is variable, the effective inductance

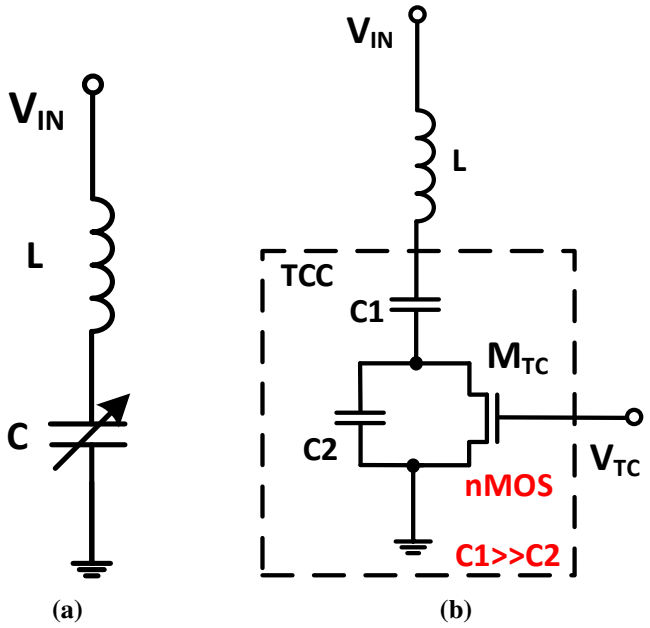


Figure 6.1: Topologies of VCI. (a) Ideal model. (b) VCI with TCC.

seen from the input V_{IN} to the ground is simply varied by the value of the series capacitance as

$$L_{\text{eff}} = L - \frac{1}{\omega^2 C}. \tag{6.1}$$

When the variable capacitance is varied by the voltage (i.e. a varactor), the VCI is realized in a certain frequency range. From (6.1), it is straightforward that L_{eff} can be as large as L when C is large, and L_{eff} can be near zero or even negative (i.e., becoming capacitive) when C is reduced to a small value. Similar with the shunt SCV topology in Section 4.2.1, the shunt VCI can also be used in a series topology, though with extra C_{BP}s and R_{BIAS}s.

To realize the VCI based on the series LC tank with a large TR, a major challenge is that the tuning ratio r_c of MOS varactors is only limited to about 2 to 3 in the mm-wave and THz bands [17, 30]. As per the discussions in Section 4.2.1, the SCV can reach a maximum r_c higher than 20 with a 937-GHz f_{cd}; therefore, the switched-capacitor varactor topology seems as a promising candidate for this mm-wave VCI. However, the requirements of high-frequency passive FMs and active VCOs are different, and the SCV needs

some modifications to be used for VCIs. As shown in Fig. 6.1(b), the shunt variable capacitor is realized by a transistor-controlled capacitor, named TCC, with an nMOS transistor M_{TC} tuned by a tuning control voltage (V_{TC}). M_{TC} is in parallel with a small C2, and in series with a large C1, which is similar to the concept of the SCV, but the TCC and the SCV are different in several aspects.

For varactor FMs, the SCV needs to maximize r_c, and as such the size of the transistor SW (similar as the M_{TC} in Fig. 6.1(b)) is small, and the capacitor C2 is absorbed into the parasitic capacitance from the transistor to minimize C_{min}. The SCV is actually a capacitor C1 in series with the transistor SW, whereas the TCC needs to minimize the on resistance of the transistor to keep a high Q. Therefore, the width (W) of the M_{TC} can reach 200 to 400 μm in the VCI design, and the C2 is preserved in the TCC since the minimum capacitance C_{min} of the TCC cannot be too small to avoid the negative inductance.

When $V_{\mathrm{TC}} \leq$0 V, the capacitance of the TCC is C2 plus some parasitic capacitance from M_{TC}. When $V_{\mathrm{TC}} \geq$0.8 V, the capacitance of the TCC is about C1 assuming the on resistance of the M_{TC} is small. The simulated r_c of the TCC can reach as high as about 17, and Q of the TCC varies from 1 to 14 in simulations at 30 GHz. Although it is possible to tune the L_{min} to be near zero to have a very large TR of inductance, the Q of the inductor would be very low when the inductance is too small, and the value of L_{min} would be very sensitive to the process variation of C2 plus the parasitic capacitance of M_{TC}, which makes the design not practical. A trade-off is made between the Q of the VCI, the process variation, and the TR of the VCI, which directly has an influence of the frequency tuning range of the ILO. L_{min} is chosen at 20 pH for this ILO design, which also ensures the ILO oscillation with the small inductance. In this case, M_{TC} has a large W for lowering the on resistance, and the parasitic capacitance of the M_{TC} can be absorbed into C2 to get the required L_{min} , i.e. the size of M_{TC} can be enlarged, whereas deducting the part of capacitance from the C2. The resultant r_L is about 4, resulting in a VCI TR of 300% calculated by $100\%(L_{max}-L_{min})/L_{min}$ [78].

There is another challenge that this VCI is only inductive in the designed mm-wave

band, but appears as an open circuit at dc, thus the VCI cannot be used to conduct any dc current or for dc biasing.

6.3 ILO Design with VCI

An inductively tunable third-harmonic ILO was designed for the demonstration of the proposed VCI, as shown in Fig. 6.2. The Colpitts oscillators are widely used above 100 GHz, due to the low phase noise and large TR [81, 82]. The VCI is used to replace the resonator inductor as indicated in the red circle in Fig. 6.2, in the conventional common-drain/collector Colpitts oscillator used in [83]. One advantage to select the common-drain Colpitts oscillator is that the VCI as L1 in the oscillator does not need to be the path to carry any dc current, whereas other type of oscillators such as common-gate Colpitts oscillators or cross-coupled oscillators may need the resonator inductors for dc paths [84]. The inductor L2 is added to the common-drain Colpitts topology and optimized to enhance the output power though limiting the TR of the oscillator [85].

At the input side, there are several ways to inject the fundamental signal at f_0 to the circuit, e.g., with a transformer coupled to the input inductor [83], or with a current mirror connected to the source of the transistor M1 [86]. To minimize the chip area and reduce the total dc power from the transformers or the tail transistor networks, the injected signal is directly coupled to the voltage supply VDD node. Although the direct injection may require more input power (noted as P_{IN}), due to the reflection at the input port and the loss from the on-chip VDD decoupling capacitors (not shown in Fig. 6.2) , it is demonstrated as an efficient way to inject power to the ILO, as indicated by both simulated and measured results, compared with a 120-GHz ILO in [87].

At the output side, to avoid output transformers, such as used in [86], as well as active output buffers in the D-band, a passive high-pass filter (HPF) is designed as a high impedance at the injected frequency f_0, and passes the third-order harmonic output at $f_{\mathrm{OUT}} = 3f_0$. The core area of the resultant Colpitts ILO only occupies a compact 0.018

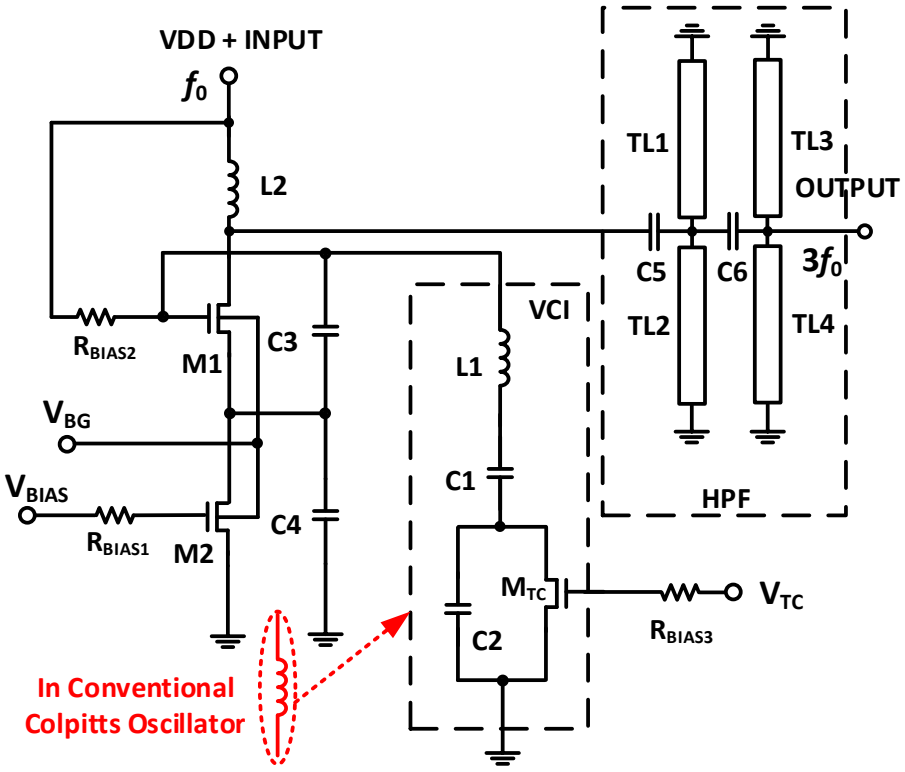


Figure 6.2: Schematic of the Colpitts ILO with VCI.

mm^2, including all the active components, VCI, and L2. A passive HPF composed of TLs and capacitors is exploited to extract the f_{OUT}, which only occupies 0.015 mm^2, as shown in Fig. 6.3.

The inductance of the VCI, the capacitance of the TCC, and the capacitance of a reference MOS varactor from the same 22-nm SOI CMOS are simulated and compared in Fig. 6.4(a). The quality factors (Qs) of these three devices are shown in Fig. 6.4(b). The varying range of V_{TC} is from -2 to 2 V in the simulation. The fixed inductor in the VCI is 89 pH. The TCC used in the VCI has a maximum to minimum capacitance ratio r_c at about 7, which is much larger than the r_c of the conventional CMOS varactor. Together with the high r_c, the Q of the TCC is much higher than the Q of the MOS varactor reaching as high as about 20, when compared at the same capacitance (e.g. at 0V). When the voltage is not larger than 0 V, the Q of the TCC is significantly better than the Q of the MOS varactor, as shown in Fig. 6.4(b). When the V_{TC} becomes high, it appears that the Q of the MOS

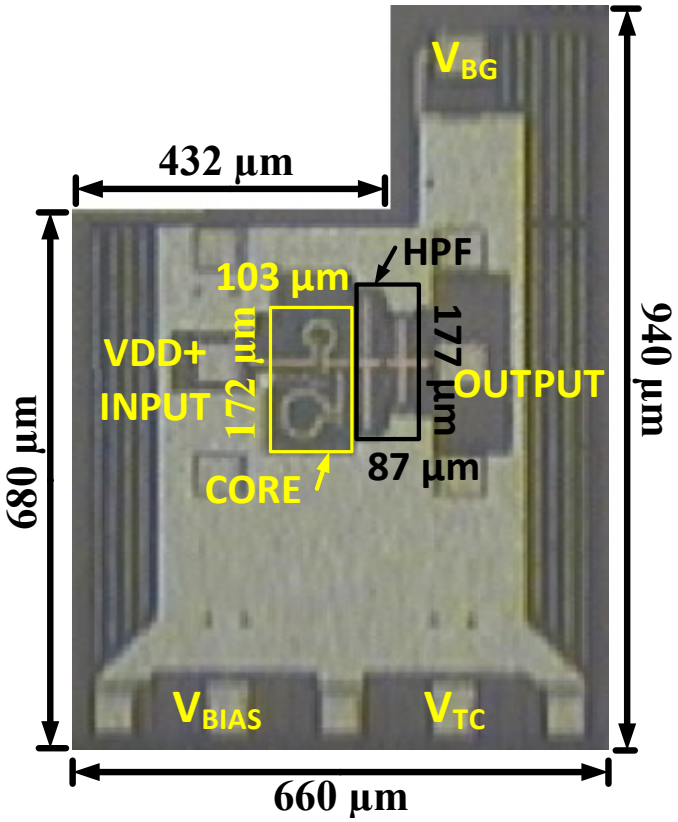


Figure 6.3: Die micrograph.

varactor is higher; however, that is due to the limited TR and C_{max} of the MOS varactor. Based on the conventional definition of quality factor (Q_{CON}), which is calculated by

$$Q_{\mathrm{CON}} = \left| \frac{\mathrm{Im}(y_{11})}{\mathrm{Re}(y_{11})} \right| \tag{6.2}$$

from [80], the Q of a variable capacitor varies with the value of the capacitance accordingly assuming R is constant. For a fair comparison of Q, the two varactors should be compared with the same levels of capacitance. On the other hand, the capacitance of the TCC is more than three times that of the MOS varactor, whereas the Q is much higher than one third of the Q of the MOS varactor (except for a small voltage region during the transition explained in Section 4.2.1 for the SCV), which demonstrates the TCC has a better performance than the MOS varactor.

With the series TCC with an $r_c \approx 7$, the VCI has a smoothly varying inductance from

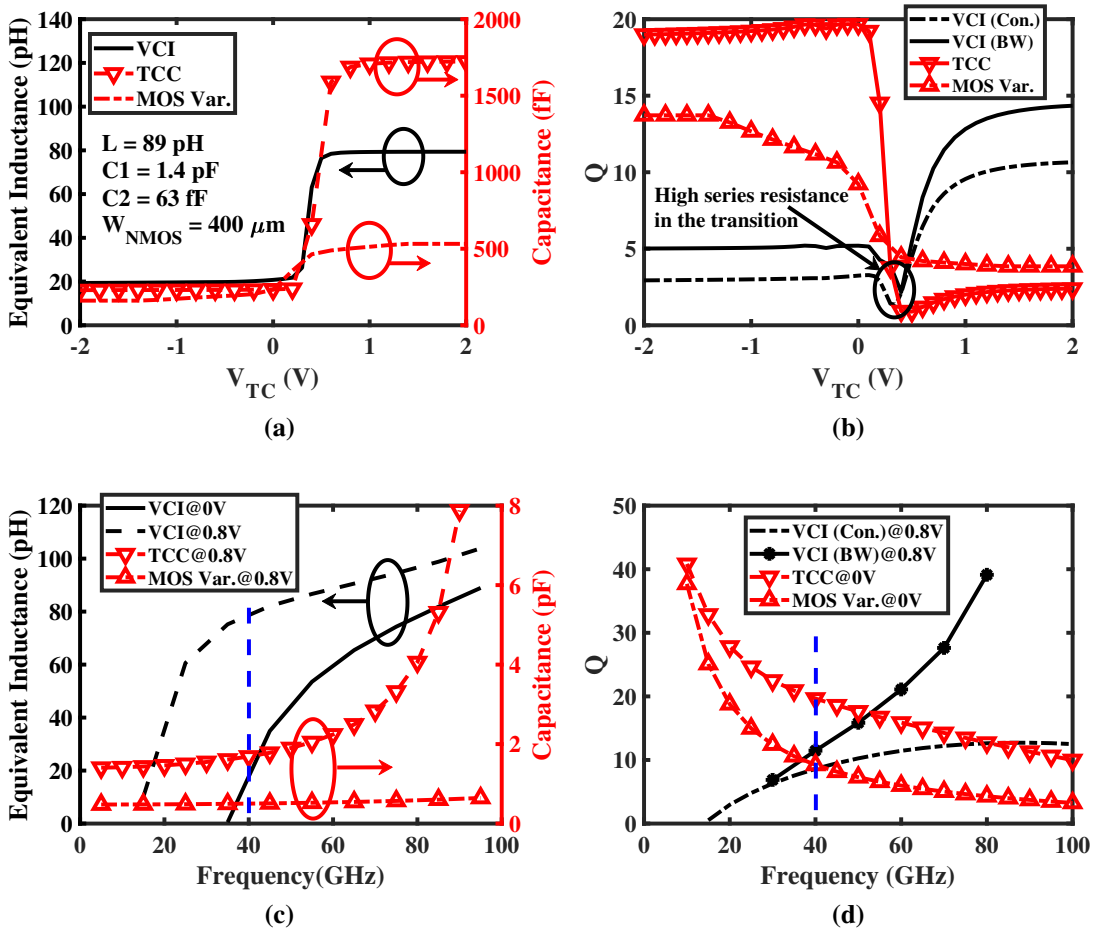


Figure 6.4: L_{eff} of the VCI, C of the TCC and the reference MOS varactor, as well as Q versus V_{TC} simulated at 40 GHz in (a) and (b), and versus frequency in (c) and (d).

20 to 80 pH between the transition V_{TC} range from 0.2 to 0.6 V. The inductance ratio r_L reaches 4. Although in Fig. 6.1(b) the V_{TC} is directly connected to the gate of the M_{TC}, in device simulations and the ILO design, a 2-kΩ biasing resistor is used to reduce the parasitics and the leakage from the drain-to-gate capacitance of the M_{TC}, since the size of the M_{TC} is very large (W = 400 μm) for the TCC.

For the high-frequency on-chip inductors, the conventionally defined Q_{CON} may deviate from the physically meaningful definition of quality factor in terms of energy storage and dissipation, due to the large shunt capacitance to the substrate [88]. Therefore, a definition

of Q_{BW} by the 3-dB BW is given as

$$Q_{\mathrm{BW}} = \frac{\omega_{\mathrm{res}}}{\mathrm{BW}_{\mathrm{3dB}}} \tag{6.3}$$

in [88], where ω_{res} is the resonant frequency of the inductor when resonating with a capacitor, and $\mathrm{BW}_{\mathrm{3dB}}$ is the 3-dB BW of the resonating circuit. Both Q_{CON} and Q_{BW} are shown in Figs. 6.4(b) and (d), where Q_{BW} is considered as more physically meaningful than Q_{CON}. The maximum Q_{BW} of the VCI is higher than 10 in the varying voltage range, whereas, in the transition region with V_{TC} between 0.2 to 0.6 V, Q_{BW} is as low as 2.2 due to the high equivalent series resistance from the TCC in the transition region.

These key parameters including L_{eff} , C, and Q simulated versus frequency up to 100 GHz are shown in Figs. 6.4(c) and (d). Although the ratio of r_L reaches 4 at 40 GHz, the r_L is reduced when the frequency becomes much higher than 40 GHz. The phenomenon can be predicted by (6.1) and indicates that the VCI should have smaller varying capacitance for the applications at higher frequencies. As shown in Fig. 6.4(d), the Q_{BW} becomes much higher than Q_{CON} when the frequency becomes higher in a frequency range, which can be also observed from prior on-chip variable inductors in [88] and [80].

The simulated self-oscillating frequency of the ILO in response to V_{TC} is shown in Fig. 6.5, when biased as an oscillator without the injection. The autonomous oscillator circuit has a fundamental oscillation in the mm-wave band around 40 GHz, and the third harmonic is extracted as the output. In the simulation, the Colpitts oscillator has a much larger TR with the proposed VCI than the same circuit but tuned by a 30-to-90 fF MOS varactor, which replaces the 51-fF C3 in the schematic, with a fixed inductor having an L_{eff} at 20 or 80 pH obtained by constantly biasing the VCI. Based on the simulation, it can be expected that the VCI topology can be further improved with larger TR of the ILO by combing the tunable VCI and the MOS varactor together. The ILO design is optimized for the extraction of the third harmonic of the fundamental injection, with trade-off among phase noise (PN),

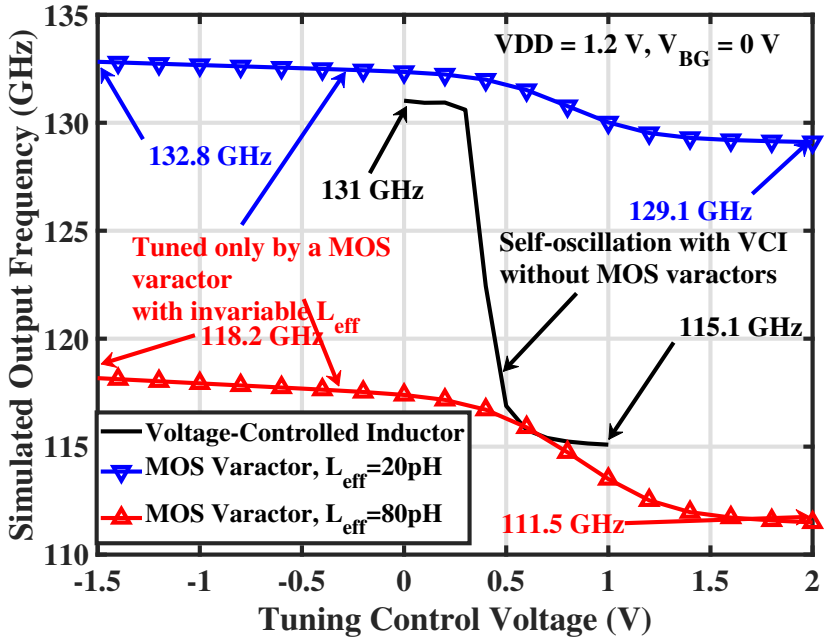


Figure 6.5: Simulated self-oscillating output frequency $3f_0$ versus V_{TC} for the ILO with VCI, and for ILO with fixed-value L_{eff} of the VCI at 20 and 80 pH, and a MOS varactor replacing C3 tuned by a separate V_{TC}.

P_{OUT} and TR.

6.4 Measurement Results

The injected signal is provided by a 50-GHz network analyzer, and is amplified by a 60-GHz PA. The path to generate the 10.6-dBm P_{IN} is shown in Fig. 6.6, with the typical gains or losses of the instruments and devices noted. The output D-band signal at $3f_0$ is downconverted by the frequency extender, and is measured by a spectrum analyzer, which is similar as the setup for other D-band chips in this thesis, and, therefore, is ignored in this figure. The injection signal at f_0 is combined with the dc supply VDD in a bias T and fed to the ILO together with a GSG probe. The on-chip decoupling capacitor for VDD is also shown in the figure, which is discussed in Section 6.3. Although it may increase leakage of P_{IN}, this effect is mitigated in layout by trying to lead the leakage from the decoupling capacitor back to the source of M2. As shown in the measured results, the required P_{IN} to

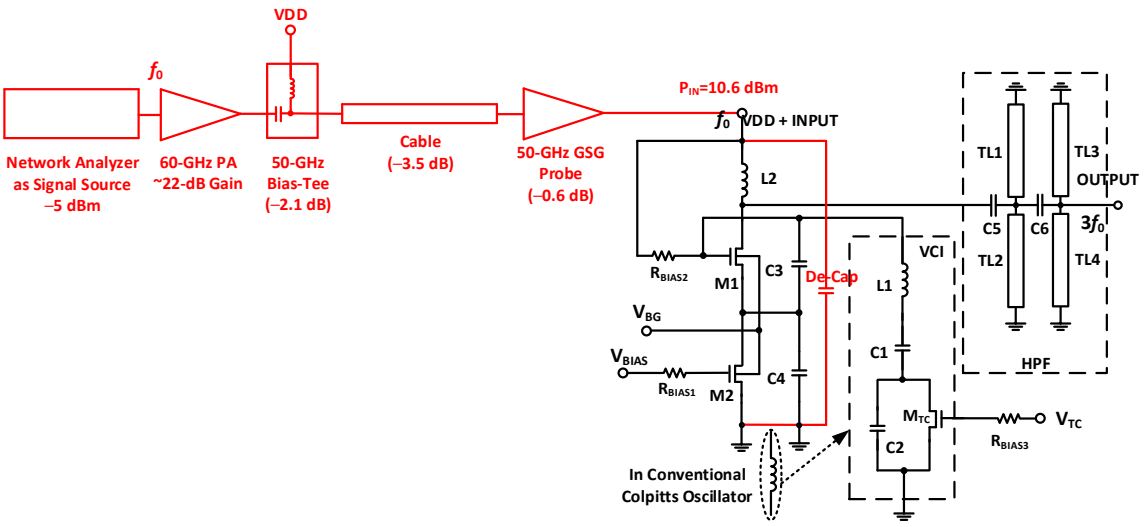


Figure 6.6: The block diagram to generate the required injection locking signal, with the decoupling capacitor for VDD.

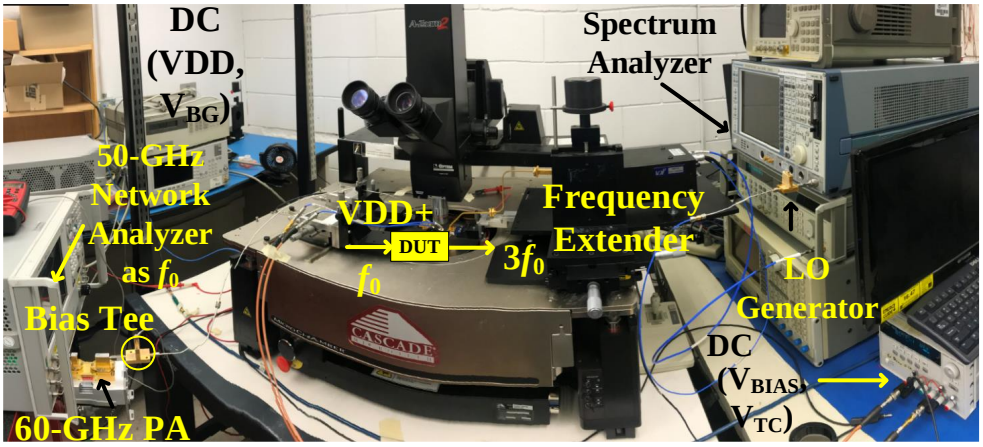


Figure 6.7: Measurement setup of the ILO.

lock the oscillator is not much larger than in other D-band ILOs, such as 10-dBm P_{IN} at 40-GHz for a third-harmonic 120-GHz ILO in [87]. The photograph of the total measurement setup is shown in Fig. 6.7.

The dc power (P_{DC}) of the circuit is measured by monitoring the dc current from the VDD through the bias T. The measured P_{OUT} at $3f_0$ and P_{DC} versus the biasing voltage (V_{BIAS}) to the gate of M2 are shown in Fig. 6.8 at 1.2-V VDD. As shown in the figure, the optimized operation condition with highest P_{OUT} is at 0.6-V V_{BIAS}, which is around half of the VDD. When the back-gate tuning voltage (V_{BG}) of the SOI CMOS transistor is used, the

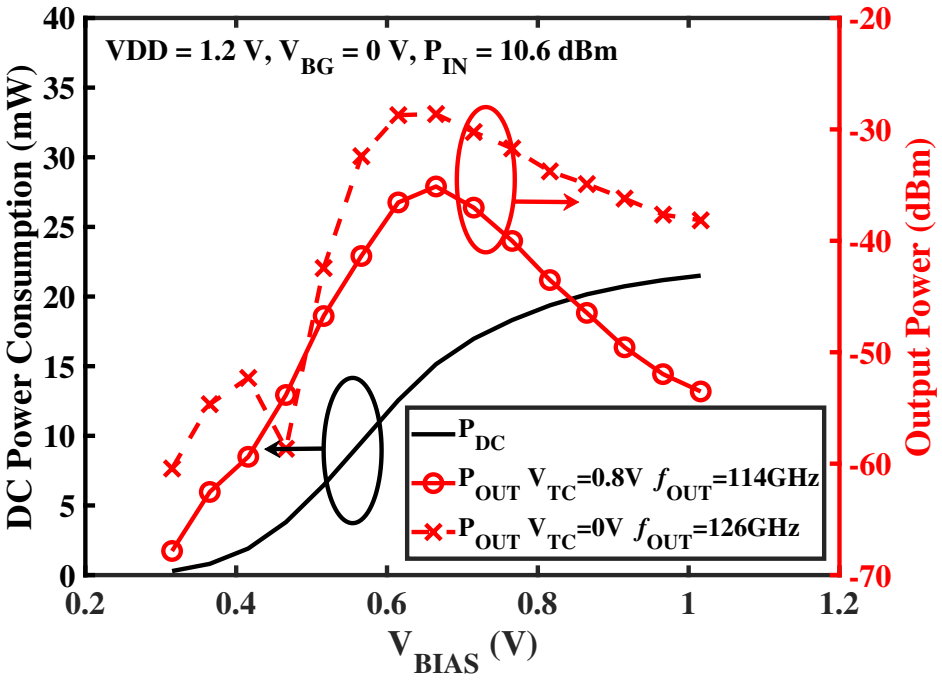


Figure 6.8: Measured P_{OUT} and P_{DC} versus V_{BIAS} at 1.2-V VDD.

VDD can be lower to reduce the total P_{DC} significantly, by decreasing the threshold voltage of the transistors. When the V_{BG} is increased from 0 to 2 V, the VDD can be reduced to 0.8 V, and the P_{DC} is decreased to only 5.6 mW with a 0.4-V V_{BIAS}. The measured P_{OUT}^{max} is -29 dBm, when $f_{\mathrm{OUT}} = 126$ GHz and $V_{\mathrm{TC}} = 0$ V as shown in Fig. 6.8.

The measured P_{OUT} versus the tunable frequency range under different V_{TC}s and VDDs are shown in Fig. 6.9. When the V_{TC} is tuned from 0 to 0.8 V, the tunable output frequency range continuously covers 112.5 to 132 GHz for 1.2-V VDD and 114 to 135 GHz for 0.8-V VDD. Although the P_{OUT} with 0.8-V VDD is lower than that of 1.2-V VDD, biasing with 0.8-V VDD effectively reduces P_{DC}.

The P_{OUT} versus the injected P_{IN} is plotted in Fig. 6.10, for V_{TC} at 0 and 0.8 V, respectively. The ILO loses lock when P_{IN} is less than -4 dBm at 114 GHz, though the ILO needs 5-dBm P_{IN} to get locked at 126 GHz. After the startup of the injection-locked oscillation, it was possible to disconnect the injected signal and observe the free-running oscillation between 116 and 126 GHz, which are tuned by 0.8- and 0-V V_{TC}, respectively. However,

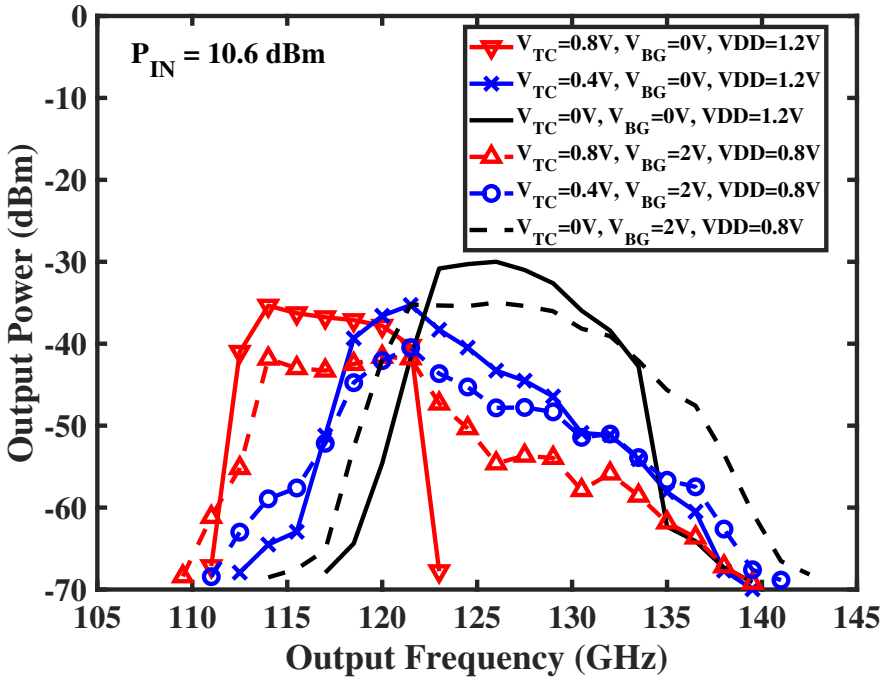


Figure 6.9: Measured P_{OUT} versus f_{OUT} with 0.8- and 1.2-V VDDs.

the measured P_{OUT} at $3f_0$ is very low without the injection. As in simulations, although the free-running oscillation at f_0 around 40 GHz is always strong with or without the injection, the extraction of the third harmonic in the D-band depends on the injection, which shows the same trend as the measurement.

The PN of the injected and the output signals are shown in Fig. 6.11, at $V_{\mathrm{TC}} = 0$, 0.4, and 0.8 V, respectively. The PN of the the third-order harmonic and the fundamental input differ by the theoretical 20log(3) $\approx$ 10 dB. It can be seen from the figure that the measured PN is slightly higher with a 0-V V_{TC} than with V_{TC} at 0.4 and 0.8 V. It is possibly due to the higher measured frequency with V_{TC} at 0 V, since the three curves are all compared with the same injected signal at 40 GHz, which is limited by the frequency range of the spectrum analyzer in the measurement setup. The sensitivity of the measurement instruments limits the PN measurements in the offset frequency range above 1 MHz. Since the PN of the third harmonic of the ILO follows in the fundamental input [89], the injected-signal PN, rather the quality factor of the VCI, dominates the PN contribution of the ILO .

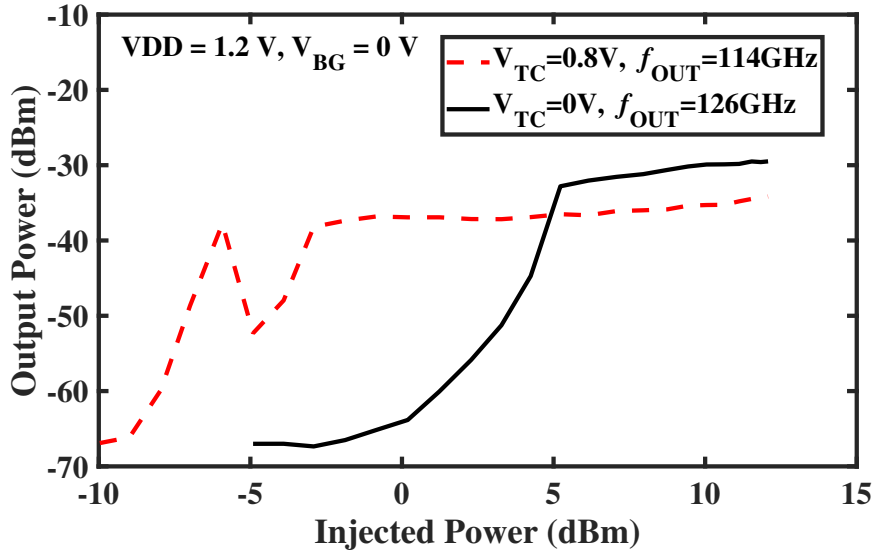


Figure 6.10: Measured P_{OUT} versus P_{IN} with 1.2-V VDD.

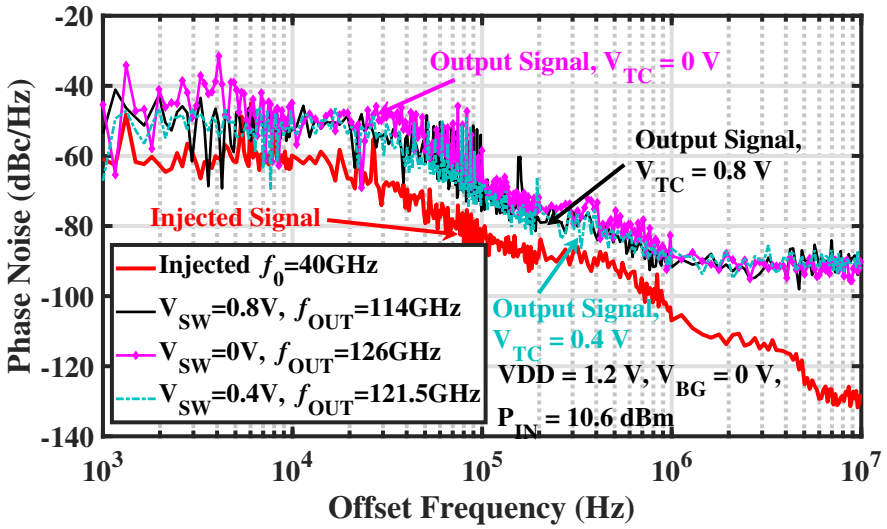


Figure 6.11: Measured PN of the injected and output signals.

This VCI is compared with other prior on-chip mm-wave variable inductors in Table 6.1. The proposed VCI with the TCC has a higher TR than all other variable inductors in the table, especially compared with the transformer-based variable inductors. Though the inductor array such as in [79] can provide a larger TR than transformer-based variable inductors, it suffers from a much lower operating frequency and limited Qs even at the lower frequencies. The lower Q of the VCI at L_{min} is partially due to the lowest L_{min}

Table 6.1: Summary of VCI and other variable inductors

Ref.	**This work**	[90]	[80]	[81]	[91]	[79]
Freq. (GHz)	**40**	60	77	84[b]	100	23 to 36
Variable Inductor Topo.	**Series LC Tank + TCC**	Transf. + Var. Resistor	Transf. + Varactor	Transf. + Varactor	Transf. + Transis-tor	Inductor Arrays[c]
L_{max} (pH)	**79.1 @0.8V**	30.5	61.9 @1V	87.2 @0V	34.1 @2mA	300
L_{min} (pH)	**19.7 @−0.8V**	20.4	55.7 @−1V	52.4 @8V	31.6 @12mA	140
Q[a]	**11.5 @0.8V 2.4 @−0.8V**	5.3 3.8	13@1V 20@−1V	2@0V 14@8V	6@2mA 16 @12mA	7[d] 8.9[d]
TR %	**302**	49.5	55.7	66.4	7.9	114

[a] Q at L_{max} and L_{min}. [b] Estimated from the second harmonic. [c] Differential inductor. [d] Only copper layer is used.

achieved by the VCI with the TCC. Notice the VCI with the TCC can get any small value of inductance, and the Q varies with L accordingly assuming the equivalent loss resistance is not dramatically changed. Other topologies of variable inductors, however, may have different relationship between Q and L, e.g., the lowest Q is obtained at the higher L, such as in [80] and [81].

The performance of the third-harmonic-extracted ILO is summarized and compared with other 100-to-250-GHz ILOs and VCOs in Table 6.2, including VCOs in [81] and [91] using variable inductors in Table 6.1. The IL VCO with VCI in this work has a $\geq 16\%$ tunable operating frequency range, which is only tuned by the high-TR inductor with the V_{TC}. The 0.018-mm^2 core chip area is the smallest by avoiding the use of inductor arrays and the transformers. The 5.6-mW P_{DC} is also the smallest in the comparison table, by using the V_{BG} to tune the SOI MOS FETs to operate with a 0.8-V VDD. Although other oscillators may have higher P_{OUT}, they employ SiGe with a much higher P_{DC} such as [82], [81], and [91], or have a limited TR and a larger chip size such as [92].

Table 6.2: Summary of 100-to-250-GHz ILOs and VCOs

Ref.	**This work**		[82]	[92]	[81]	[91]
Techn.	**22-nm SOI CMOS**		55-nm SiGe	90-nm CMOS	0.13-μm SiGe	0.13-μm SiGe
Appr.	**IL VCO with VCI**		Varactor	Quad. SILO	Varactor + Var. Inductor	Variable Inductor
$\times N$	$\times$**3**		$\times$2 (VCO)	$\times$3	$\times$2 (VCO)	$\times$2 (VCO)
Supply (V)	**1.2**	**0.8**	2.5	1.2	5	NA
Output Freq. (GHz)	**112.5 to 132**[a]	**114 to 135**[a]	188.5 to 250.6	99.9 to 110.7	148 to 188[c]	198 to 205
Range (%)	**16**[a] **8.3**[b]	**16.9**[a]	28.3	10.3	23.8[c]	3.5
P_{OUT}^{max} (dBm)	**−29**	**−35**	−3.7	−22	NA	−7.2
P_{DC} (mW)	**13**	**5.6**	82.1	8.5	108	57
Chip Area (mm^2)	**0.018 (Core)**[d]		0.31	0.3 (Core) 0.88	0.079 (Core) 0.53	0.073 (Core)

[a] 10-dB frequency range. [b] Tuning range with free-running .[c] Tuned by both varactor and variable inductor. [d] 0.033 mm^2 with core and HPF including all components of the ILO as shown in the schematic.

6.5 Conclusion

A high-TR VCI is proposed with TCC in this work, which is demonstrated in a D-band ILO with the extraction of the third-order harmonic. With the VCI tuned by a tuning voltage, the IL VCO tunable output-frequency range is achieved from 112.5 to 135 GHz ($\geq$16%). The dc power is 13 mW under 1.2-V, but can be reduced to 5.6 mW under 0.8-V VDD using the back-gate voltage to lower the threshold voltage. The measured additional phase noise of the third harmonic to the injection signal is close to the theoretical prediction. The compact core size of 0.018 mm^2 is obtained by using the VCI and the simplified injection topology. The third-harmonic-extraction ILO demonstrates the potential of the VCI with

the TCC in mm-wave and D-band applications with low power consumption, compact size, and wide tuning range.

Chapter 7

Conclusions and Future Work

The operations of parametric reactive and resistive frequency multipliers are analyzed in the frequency domain with Fourier series based on Z-matrices or Y-matrices. Idlers, required by the conventional single-varactor parametric circuits, are avoided in this thesis. The pumped parameters, i.e. capacitance, elastance, resistance and conductance, are represented in the form of an SRPP for the idler-less parametric harmonic generation. The SRPP describes the process of harmonic generation whereby the pumped parameter exhibits $N-1$ periods under one period of the sinusoidal pump signal in the time domain for the Nth-order harmonic generation. The relation between the required parameter and voltage is described by Chebyshev polynomials of the first kind to generate the Nth harmonic. The maximum conversion efficiency of the Nth harmonic is $1/N$ for reactive frequency multipliers. An IRPP is developed as another pumping mechanism for the resistive multipliers with impulse-like pumped parameters. In one period of sinusoidal pumping, $N-1$ pulses are used to generate the Nth harmonic for resistive multipliers. The relations between nonlinearity in terms of the ratio of maximum to minimum parameters, such as r_c and r_r, and the conversion efficiency are analyzed. The relations between the operating frequency range, dynamic cutoff frequency f_{cd}, and the conversion efficiency of a reactive multiplier are also discussed.

To demonstrate the validity of the parametric harmonic generation and apply the proposed theory in parametric circuits operating in the mm-wave band, sub-THz band, and future THz band, a variety of parametric circuits, operating from the 28-GHz 5G band to D-band up to 160 GHz, are designed and measured.

A frequency tripler with an improved symmetric C-V curve is implemented in a 45-nm SOI CMOS process. The SAPSV topology composed of all nMOS varactors provides better r_c and f_{cd} with a simplified biasing topologies, compared with conventional AS-

VAR topology with nMOS varactors. The measured CL is 24.3 dB with a 17.8% BW. The maximum P_{OUT} reaches -8 dBm in the 28-GHz band. The added phase noise is also measured and is close to the theoretical prediction.

Two reconfigurable frequency multipliers are designed in the D-band and fabricated in a 22-nm SOI CMOS process. The varactor pairs with C-SCVP and APNVP realize tunable C-V curves with "1-valley", "2-valley" asymmetry, and "2-valley" symmetry for the third, fourth, and fifth harmonic generation, respectively. The measurement results demonstrate the validity of the theory of the harmonic generation by tuning the shapes of C-V curves to enhance and suppress the corresponding specific harmonic. The SCV is proposed with an almost 10 times better r_c and a higher f_{cd} for parametric circuits, and is implemented in the SCVP RFM. The measured results show that SCVP RFM has significant improvements compared with APNVP RFM in almost all aspects of the performance.

A resistive tripler with APDNP is also implemented in the D-band to demonstrate the tunability of r_r to improve the total CL, especially with a high P_{IN}, as well as a wide 27.8% BW in the D-band, in 22-nm SOI CMOS. The back-gate voltage can enlarge the cutoff region of the APDNP and, therefore, increase the total r_r under a high P_{IN} to improve the CL by 1.7 dB, when the V_{BG} is applied. A maximum P_{OUT} is measured as -16 dBm in the available measured frequency range.

Finally, a TCC is used to build a VCI as a tunable series LC tank. The VCI is demonstrated in a D-band third-harmonic-extracted IL VCO in 22-nm SOI CMOS. The ILO achieves a tunable operating frequency range $\geq$16% only tuned by the VCI. The dc power consumption is only 5.6 mW when V_{BG} is used to lower the threshold voltages of the transistors. The core chip size is as compact as 0.018 mm^2, and the measured added phase noise is close to the theoretical prediction.

The parametric harmonic generation theory proposed and demonstrated in this thesis opens a new path to the field of future parametric circuits, not limited to mm-wave and THz parametric multipliers, but also applicable for parametric amplifiers and frequency

converters in wireless transceivers. Harmonic pumping is a potential method to combine the harmonic generation and other parametric circuits together, which can save the cost of circuit components and stages, as well as reduce the total loss in the passive circuits. The methodology and theory in terms of the SRPP and IRPP have the potential to be used to explore the new frontiers of the parametric circuits, to fill the THz gap between conventional electronic and optic fields. Some future research directions are discussed in the following.

Based on the classic Manley-Rowe relations, the varying reactance is not limited to capacitance but also can be inductance. The VCI can be potentially used as a kind of time-varying inductance. Therefore, the VCI with the TCC not only can be applied in the future high-frequency VCOs and ILOs, but also has the potential in future mm-wave and THz parametric circuits with variable inductance.

Based on the derivations of the conversion gains, it is noticed that mathematically the resistance, capacitance, or inductance is not required to be always positive. In fact negative parameters sometimes can make the denominators of the conversion gain expressions even smaller, such as for resistive multipliers, which means a higher conversion gain can be obtained, though it might not be practical for current nonlinear resistance devices in parametric circuits to be negative. The VCI with the TCC is a straightforward way to generate a negative inductance in a certain frequency range, i.e., the device would change between inductive and capacitive under pumping, which may be of interests for future parametric circuits.

The SCV is demonstrated to have a very high ratio of capacitance with an f_{cd} as high as 1.5 THz in this technology, which will have potentials in many future parametric circuits, not limited in the frequency multipliers, potentially replacing the conventional MOS varactors in the THz band.

The series R_s is a key limitation for the f_{cd} as well as the performance of the parametric circuits. As shown in [54], cryogenic environment helps increase the efficiency of parametric multipliers, due to the reduction of the resistance. Since parametric circuits are passive,

they are not influenced significantly by the cryogenic behavior of the active device. As such, cryogenic parametric circuits will be another research direction of interests for very high-performance passive circuits at extremely low temperatures.

The theory of the parametric harmonic generation can be expanded to the sub-harmonic generation, with parameters in terms of $\cos(\omega_0 t/N)$, under one pumping cycle, which is similar to the SRPP. Since the parametric dividers do not consume dc power, the research and development of a parametric divider based on the parametric sub-harmonic generation have a potential to save dc power for mm-wave and THz applications, which need dividers, such as in possible THz phase-locked loops. Some initial derivation of the parametric sub-harmonic generation is given in the Appendix.

Although parametric circuits have been developed for more than half a century, and have been almost forgotten for several decades, with research on the new theories and components related to the parametric circuits, it is expected to have more and more exciting discoveries and creations in the parametric field in the mm-wave and THz bands or at even higher frequencies.

Bibliography

[1] K.-H. Löcherer and C.-D. Brandt, *Parametric Electronics An Introduction*. Springer-Verlag Berlin Heidelberg New York, 1982. *(Cited on pages 1, 35 and 81.)*

[2] V. Damgov, *Nonlinear and parametric phenomena theory and applications in radiophysical and mechanical systems*. New Jersey ; London: World Scientific, 2004. *(Cited on pages 1, 9 and 14.)*

[3] L. A. Blackwell, *Semiconductor-diode parametric amplifiers*. Prentice-Hall international series in engineering, Englewood Cliffs, N.J.: Prentice-Hall, 1961. *(Cited on page 1.)*

[4] J. M. Manley and H. E. Rowe, "Some general properties of nonlinear elements-Part I. General energy relations," *Proc. of the IRE*, vol. 44, no. 7, pp. 904–913, 1956. *(Cited on pages 1 and 57.)*

[5] X. Liu, R. M. Osgood, Y. A. Vlasov, and W. M. J. Green, "Mid-infrared optical parametric amplifier using silicon nanophotonic waveguides," *Nature Photonics*, vol. 4, pp. 557–560, 2010. *(Cited on pages 1 and 8.)*

[6] T. H. Lee, "Terahertz electronics: The last frontier," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, pp. 30–34, 2014. *(Cited on page 2.)*

[7] N. Horiuchi, "Chasing room temperature," *Nature Photonics*, vol. 6, p. 213, 2012. *(Cited on page 2.)*

[8] Y. Tang *et al.*, "Ultrahigh-speed GaN high-electron-mobility transistors with $f_T/f_{\max}$ of 454/444 GHz," *IEEE Electron Device Lett.*, vol. 36, no. 6, pp. 549–551, 2015. *(Cited on page 2.)*

[9] L. Gao, Q. Ma, and G. M. Rebeiz, "A 20–44-GHz image-rejection receiver with >75-dB image-rejection ratio in 22-nm CMOS FD-SOI for 5G applications," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2823–2832, 2020. *(Cited on page 2.)*

[10] R. Han *et al.*, "Active terahertz imaging using Schottky diodes in CMOS: Array and 860-GHz pixel," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2296–2308, 2013. *(Cited on pages 2, 3 and 100.)*

[11] W. Wild, R. Gusten, W. S. Holland, R. J. Ivison, and G. J. Stacey, "Large antennas for ground-based astronomy above 1 THz," in *Proc. IEEE Antennas and Propagation Society Int. Symp.*, pp. 2391–2394, 2006. *(Cited on pages 3 and 4.)*

[12] Q. Zhong *et al.*, "CMOS terahertz receivers," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, pp. 1–8, 2018. *(Cited on pages 3, 100 and 101.)*

[13] Q. Zhong *et al.*, "A 210-to-305GHz CMOS receiver for rotational spectroscopy," in *IEEE ISSCC Dig. Tech. Papers*, pp. 426–427, Jan. 2016. *(Cited on pages 3, 15 and 101.)*

[14] H. Ito and T. Ishibashi, "Low-local-oscillator-power sub-harmonic mixing in 300-GHz band by Fermi-level managed barrier diode," *Electron. Lett.*, vol. 56, no. 24, pp. 1326–1328, 2020. *(Cited on pages 3 and 15.)*

[15] F. Rodriguez-Morales *et al.*, "Development of integrated HEB/MMIC receivers for near-range terahertz imaging," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 6, pp. 2301–2311, 2006. *(Cited on page 4.)*

[16] E. Zailer, H. Xie, N. Zhang, R. Plume, L. Belostotski, and M. Okoniewski, "University of Calgary participation in CCAT CHAI development," in *Proc. IEEE Int. Symp. Antennas Propag. URSI Nat. Radio Sci. Meeting*, pp. 1378–1379, 2015. *(Cited on page 4.)*

[17] Z. Ahmad and K. K. O, "0.65–0.73THz quintupler with an on-chip antenna in 65-nm CMOS," in *Proc. Symp. on VLSI Circ.*, pp. C310–C311, June 2015. *(Cited on pages 4, 5, 7, 13, 16, 22, 78, 79, 80 and 115.)*

[18] Z. Ahmad, M. Lee, and K. K. O, "1.4THz, −13dBm-EIRP frequency multiplier chain using symmetric- and asymmetric-CV varactors in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 350–351, 2016. *(Cited on pages 4, 5, 7, 64 and 66.)*

[19] J. Paul Penfield and R. P. Rafuse, *Varactor Applications*. M.I.T. Press, 1962. *(Cited on pages x, 5, 6, 14, 15, 16, 22, 23, 24, 29, 42, 57, 58, 59 and 83.)*

[20] R. H. Pantell, "General power relationships for positive and negative nonlinear resistive elements," *Proc. of the IRE*, vol. 46, no. 12, pp. 1910–1913, 1958. *(Cited on pages 5, 10, 60, 61 and 62.)*

[21] K. Krishnamurthi and R. G. Harrison, "Analysis of symmetric-varactor frequency triplers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 2, pp. 649–652, 1993. *(Cited on pages x, 5, 16, 22, 58 and 59.)*

[22] Z. Zhao *et al.*, "Coherent parametric RF downconversion in CMOS," in *Proc. IEEE Radio Freq. Integr. Circ. Symp. (RFIC)*, pp. 377–380, May 2010. *(Cited on page 5.)*

[23] Z. Zhao *et al.*, "Gain-configurable lower sideband parametric downconverter," in *Proc. European Microwave Integrated Circuits Conf. (EuMIC)*, pp. 113–116, Oct. 2017. *(Cited on page 5.)*

[24] Z. Zhao *et al.*, "35.5 GHz parametric CMOS upconverter," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, pp. 477–479, Sep. 2012. *(Cited on page 5.)*

[25] W. Qian and C. Qian, "Frequency modulated parametric oscillation for antenna powered wireless transmission of voltage sensing signals," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1783–1791, 2019. *(Cited on page 5.)*

[26] L. K. Yeung, X. Zou, and Y. E. Wang, "BPFs with parametrically compensated passband insertion loss and selectivity," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 803–806, 2020. *(Cited on page 5.)*

[27] M. Mehrpoo, F. Sebastiano, E. Charbon, and M. Babaie, "A cryogenic CMOS parametric amplifier," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 5–8, 2020. *(Cited on page 5.)*

[28] K. Badiyari and N. Nallam, "A switched-capacitor RF receiver exploiting MOS parametric amplification to reduce NF," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 160–163, 2019. *(Cited on page 5.)*

[29] N. Zhang, L. Belostotski, and J. W. Haslett, "28-GHz passive frequency tripler with n-type varactors in 45-nm SOI CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 3, pp. 292–295, 2020. *(Cited on pages 5, 7, 16 and 21.)*

[30] S. Kabir *et al.*, "A direct 100 GHz parametric CMOS tripler," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, pp. 557–559, Oct. 2013. *(Cited on pages 5, 13, 16, 64, 65, 67, 70, 77, 78, 79, 80, 101, 102, 110, 111 and 115.)*

[31] N. Zhang, L. Belostotski, and J. W. Haslett, "*D*-band broadband passive frequency tripler using antiparallel diode-connected nMOS transistor pair in 22-nm CMOS SOI," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 7, pp. 689–692, 2020. *(Cited on pages 5, 13, 16 and 21.)*

[32] D. Shim, C. Mao, S. Sankaran, and K. K. O, "150 GHz complementary anti-parallel diode frequency tripler in 130 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, pp. 43–45, Jan. 2011. *(Cited on pages 5, 7, 11, 13, 16, 48, 64, 65, 67, 89, 100, 101, 102, 110 and 111.)*

[33] D. Shim *et al.*, "Self-dynamic and static biasing for output power and efficiency enhancement of complementary antiparallel diode pair frequency tripler," *IEEE Microw.*

Wireless Compon. Lett., vol. 27, pp. 1110–1112, Dec. 2017. *(Cited on pages 5, 13, 16, 48, 64, 65, 67, 77, 100, 101, 102, 105, 110 and 111.)*

[34] C. Mao, S. Sankaran, E. Seok, C. S. Nallani, and K. K. O, "Millimeter wave varistor mode Schottky diode frequency doubler in CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 3, pp. 173–175, 2009. *(Cited on pages 5 and 48.)*

[35] M. Hrobak, M. Sterns, M. Schramm, W. Stein, and L. Schmidt, "Design and fabrication of broadband hybrid GaAs Schottky diode frequency multipliers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4442–4460, 2013. *(Cited on pages 5, 60 and 61.)*

[36] A. Suarez and R. Melville, "Simulation-assisted design and analysis of varactor-based frequency multipliers and dividers," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 3, pp. 1166–1179, 2006. *(Cited on page 5.)*

[37] S. Chaudhuri, J. Gao, and K. Irwin, "Simulation and analysis of superconducting traveling-wave parametric amplifiers," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, pp. 1–5, 2015. *(Cited on page 6.)*

[38] M. Haider, J. A. Russer, J. Abundis Patino, C. Jirauschek, and P. Russer, "A Josephson traveling wave parametric amplifier for quantum coherent signal processing," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 956–958, 2019. *(Cited on page 6.)*

[39] N. Zhang, L. Belostotski, and J. W. Haslett, "Passive third-, fourth-, and fifth-order reconfigurable D-band frequency multipliers based on switched-capacitor varactors," in *Proc. 63rd IEEE Int. Midwest Symp. Circuits & Syst. (MWSCAS)*, Aug. 2020. *(Cited on pages 7 and 21.)*

[40] H. A. Watson, *Microwave Semiconductor Devices and Their Circuit Applications*. McGRAW-HILL, 1969. *(Cited on pages 8 and 16.)*

[41] P. D. Batelaan, T. J. Tolmunen, and M. A. Frerking, "Quantum-well diode frequency multipliers: varistor case," *IEEE Microw. Guid. Wave Lett.*, vol. 2, no. 7, pp. 289–291, 1992. *(Cited on pages 11 and 17.)*

[42] G. Chattopadhyay, "Technology, capabilities, and performance of low power terahertz sources," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 33–53, 2011. *(Cited on pages 11 and 101.)*

[43] J. Jun, L. Bin, M. Li, H. Yue, S. Xiangyang, T. Yaoling, H. Hailong, C. Fengjun, D. Xianjin, and Z. Jian, "Single-stage frequency quadrupler with SBD and four-octave LPF at 335 GHz," *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 4, pp. 446–454, 2017. *(Cited on pages 11, 23 and 44.)*

[44] M. Hrobak, M. Sterns, M. Schramm, W. Stein, and L. Schmidt, "Planar varistor mode Schottky diode frequency tripler covering 60 GHz to 110 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1–4, 2013. *(Cited on pages 13, 100, 101, 110 and 111.)*

[45] E. W. Matthews, J. A. Luksch, and G. A. VerWys, "Design and operation of four-frequency parametric up-converters," *IRE Trans. Microw. Theory Techn.*, vol. 9, no. 1, pp. 44–52, 1961. *(Cited on page 14.)*

[46] Z. Zhao, S. Magierowski, and L. Belostotski, "Linearity analysis of CMOS parametric upconverters," *IEEE Access*, vol. 8, pp. 190906–190921, 2020. *(Cited on page 15.)*

[47] B. Philippe and P. Reynaert, "A 15dBm 12.8%-PAE compact D-band power amplifier with two-way power combining in 16nm FinFET CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 374–376, 2020. *(Cited on page 17.)*

[48] N. Zhang and L. Belostotski, "A demonstration of a voltage-controlled inductor in a D-Band Colpitts third-harmonic-extracted injection-locked oscillator," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 10, pp. 969–972, 2020. *(Cited on page 21.)*

[49] J. M. Duchamp, P. Ferrari, J. W. Tao, and D. Lippens, "Some rules for the choice of the C(V) characteristic for the design of frequency triplers with symmetrical varactors," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 1, pp. 359–362 vol.1, 2002. *(Cited on page 22.)*

[50] S. S. Bayin, *Mathematical Methods in Science and Engineering*. John Wiley & Sons, 2018. *(Cited on page 31.)*

[51] J. V. Siles, E. Schlecht, R. Lin, C. Lee, and I. Mehdi, "High-efficiency planar Schottky diode based submillimeter-wave frequency multipliers optimized for high-power operation," in *Proc. 40th Int. Conf. Infr. Millim. THz Waves (IRMMW-THz)*, pp. 1–1, 2015. *(Cited on page 58.)*

[52] S. Liang, X. Song, L. Zhang, Y. Lv, Y. Wang, B. Wei, Y. Guo, G. Gu, B. Wang, S. Cai, and Z. Feng, "A 177–183 GHz high-power GaN-based frequency doubler with over 200 mW output power," *IEEE Electron Device Lett.*, vol. 41, no. 5, pp. 669–672, 2020. *(Cited on page 58.)*

[53] D. H. Steinbrecher, M. E. Goff, and A. H. Solomon, "Iterative synthesis of varactor-multiplier microwave networks and a doubler with 0.17 Watt output at 47 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 157–160, 1967. *(Cited on page 58.)*

[54] D. W. Porterfield, T. W. Crowe, R. F. Bradley, and N. R. Erickson, "A high-power fixed-tuned millimeter-wave balanced frequency doubler," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 4, pp. 419–425, 1999. *(Cited on pages 58 and 132.)*

[55] R. Dahlbäck, J. Vukusic, R. M. Weikle II, and J. Stake, "A tunable 240–290 GHz waveguide enclosed 2-D grid HBV frequency tripler," *IEEE Trans. Microw. Theory Techn.*, vol. 6, no. 3, pp. 503–509, 2016. *(Cited on page 58.)*

[56] A. Malko, T. Bryllert, J. Vukusic, and J. Stake, "A 474 GHz HBV frequency quintupler integrated on a 20 μm thick silicon substrate," *IEEE Trans. Microw. Theory Techn.*, vol. 5, no. 1, pp. 85–91, 2015. *(Cited on page 58.)*

[57] M. Frerking, "Quantum well multipliers: Triplers and quintuplers," in *Proc. Int. Symp. on Space Terahertz Tech.*, pp. 319–321, 1990. *(Cited on page 61.)*

[58] S. Yoo, S. Choi, J. Kim, H. Yoon, Y. Lee, and J. Choi, "A PVT-robust -39dBc 1kHz-to-100MHz integrated-phase-noise 29GHz injection-locked frequency multiplier with a 600μW frequency-tracking loop using the averages of phase deviations for mm-band 5G transceivers," in *IEEE ISSCC Dig. Tech. Papers*, pp. 324–325, 2017. *(Cited on pages 64 and 65.)*

[59] J. Zhang, H. Liu, C. Zhao, and K. Kang, "A 22.8-to-43.2GHz tuning-less injection-locked frequency tripler using injection-current boosting with 76.4% locking range for multiband 5G applications," in *IEEE ISSCC Dig. Tech. Papers*, pp. 370–372, 2018. *(Cited on pages 64 and 65.)*

[60] R. Dahlbäck, J. Vukusic, R. M. Weikle II, and J. Stake, "A tunable 240–290 GHz waveguide enclosed 2-D grid HBV frequency tripler," *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 3, pp. 503–509, 2016. *(Cited on page 65.)*

[61] C. Guo *et al.*, "A 135–150-GHz frequency tripler with waveguide filter matching," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 10, pp. 4608–4616, 2018. *(Cited on pages 65, 100 and 101.)*

[62] Y. Lee, Y. Hsiao, and H. Wang, "A 57–78 GHz frequency tripler MMIC in 65-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 9, pp. 723–725, 2016. *(Cited on page 65.)*

[63] J. Pang *et al.*, "A 28-GHz CMOS phased-array transceiver based on LO phase-shifting architecture with gain invariant phase tuning for 5G new radio," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1228–1242, 2019. *(Cited on pages x, 65, 66, 75 and 77.)*

[64] S. A. Mass, *Nonlinear Microwave and RF Circuits*. Artech House, 2003. *(Cited on page 73.)*

[65] F. Bohn, B. Abiri, and A. Hajimiri, "Fully integrated CMOS X-band power amplifier quad with current reuse and dynamic digital feedback (DDF) capabilities," in *Proc. IEEE Radio Freq. Integr. Circ. Symp. (RFIC)*, pp. 208–211, 2017. *(Cited on page 75.)*

[66] S. Shakib, M. Elkholy, J. Dunworth, V. Aparin, and K. Entesari, "A wideband 28GHz power amplifier supporting 8×100MHz carrier aggregation for 5G in 40nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 44–45, 2017. *(Cited on page 75.)*

[67] D. Shin, S. Raman, and K. Koh, "A mixed-mode injection frequency-locked loop for self-calibration of injection locking range and phase noise in 0.13μm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 50–51, 2016. *(Cited on pages 75 and 77.)*

[68] J. Kim *et al.*, "A 76fsrms jitter and -40dBc integrated-phase-noise 28-to-31GHz frequency synthesizer based on digital sub-sampling PLL using optimally spaced voltage comparators and background loop-gain optimization," in *IEEE ISSCC Dig. Tech. Papers*, pp. 258–260, 2019. *(Cited on pages 75 and 77.)*

[69] T. A. Vu *et al.*, "300-GHz balanced varactor doubler in silicon CMOS for ultrahigh-speed wireless communications," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, pp. 341–343, April 2018. *(Cited on page 78.)*

[70] V. Rieß, C. Carta, and F. Ellinger, "Frequency multiplication with adjustable waveform shaping demonstrated at 200 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 4, pp. 1544–1555, 2019. *(Cited on pages 79, 96, 98 and 99.)*

[71] T. Bryllert *et al.*, "11% efficiency 100 GHz InP-based heterostructure barrier varactor quintupler," *Electron. Lett.*, vol. 41, pp. 131–132, Feb. 2005. *(Cited on page 79.)*

[72] M. Haghi Kashani, R. Molavi, and S. Mirabbasi, "A 2.3-mW 26.3-GHz g_m-boosted differential Colpitts VCO with 20% tuning range in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 4, pp. 1556–1565, 2019. *(Cited on page 81.)*

[73] S. Carpenter, Z. S. He, V. Vassilev, and H. Zirath, "A +14.2 dBm, 90–140 GHz wideband frequency tripler in 250-nm InP DHBT technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 3, pp. 239–241, 2018. *(Cited on pages 101, 109 and 111.)*

[74] A. A. Farid, A. Simsek, A. S. H. Ahmed, and M. J. W. Rodwell, "A broadband direct conversion transmitter/receiver at D-band using CMOS 22nm FDSOI," in *Proc. IEEE Radio Freq. Integr. Circ. Symp. (RFIC)*, pp. 135–138, 2019. *(Cited on page 101.)*

[75] M. Krach, J. Freyer, and M. Claassen, "Power generation at millimetre-wave frequencies using GaAs/GaAlAs triplers," *Phys. Status Solidi C*, vol. 1, no. 8, pp. 2160–2182, 2004. *(Cited on page 101.)*

[76] A. Malko *et al.*, "Silicon integrated InGaAs/InAlAs/AlAs HBV frequency tripler," *IEEE Electron Device Lett.*, vol. 34, pp. 843–845, July 2013. *(Cited on page 101.)*

[77] A. C. Bunea *et al.*, "Monolithic integrated antenna and Schottky diode multiplier for free space millimeter-wave power generation," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 1, pp. 74–77, 2020. *(Cited on page 105.)*

[78] O. F. Hikmat and M. S. Mohamed Ali, "RF MEMS inductors and their applications—a review," *J. Microelectromech. Syst.*, vol. 26, pp. 17–44, Feb. 2017. *(Cited on pages 114 and 116.)*

[79] J. Zhang *et al.*, "85-to-127 GHz CMOS signal generation using a quadrature VCO with passive coupling and broadband harmonic combining for rotational spec-

troscopy," *IEEE J. Solid-State Circuits*, vol. 50, pp. 1361–1371, June 2015. *(Cited on pages 114, 126 and 127.)*

[80] Y. Yun *et al.*, "Variable inductors in CMOS for millimeter-wave applications," *IEEE Electron Device Lett.*, vol. 33, pp. 1081–1083, July 2012. *(Cited on pages 114, 119, 121 and 127.)*

[81] J. Al-Eryani *et al.*, "Wideband 148–188 GHz push-push VCO using variable inductance and capacitance," in *Proc. European Microwave Integrated Circuits Conf. (EuMIC)*, pp. 313–316, Oct. 2016. *(Cited on pages 114, 117, 127 and 128.)*

[82] A. Mostajeran and E. Afshari, "An ultra-wideband harmonic radiator with a tuning range of 62 GHz (28.3%) at 220 GHz," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, pp. 164–167, June 2017. *(Cited on pages 117, 127 and 128.)*

[83] H. Ghaleb *et al.*, "A 160-GHz switched injection-locked oscillator for phase and amplitude regenerative sampling," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, pp. 821–823, Sep. 2017. *(Cited on page 117.)*

[84] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2001. *(Cited on page 117.)*

[85] Y. Chen, K. Mouthaan, and F. Lin, "Design of X-band and Ka-band Colpitts oscillators using a parasitic cancellation technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1817–1828, 2010. *(Cited on page 117.)*

[86] A. Vishnipolsky and E. Socher, "F-band injection locked tripler based on Colpitts oscillator," in *Proc. IEEE 12th Topical Meeting on Silicon Monolithic Integr. Circuits in RF Syst.*, pp. 13–16, Jan. 2012. *(Cited on page 117.)*

[87] C. J. Lee *et al.*, "A 120 GHz I/Q transmitter front-end in a 40 nm CMOS for wireless chip to chip communication," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, pp. 192–195, 2018. *(Cited on pages 117 and 123.)*

[88] K. O, "Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies," *IEEE J. Solid-State Circuits*, vol. 33, no. 8, pp. 1249–1252, 1998. *(Cited on pages 120 and 121.)*

[89] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, 2004. *(Cited on page 125.)*

[90] X. Liu, Z. Huang, J. Yin, and H. C. Luong, "Magnetic-tuning millimeter-wave CMOS oscillators," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, pp. 1–8, 2019. *(Cited on page 127.)*

[91] P. Chiang, O. Momeni, and P. Heydari, "A 200-GHz inductively tuned VCO with -7-dBm output power in 130-nm SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 61, pp. 3666–3673, Oct. 2013. *(Cited on pages 127 and 128.)*

[92] W. Chen *et al.*, "An 100-to-110 GHz low-dc-power sub-harmonically injection-locked quadrature oscillator using stacked boosting technique in 90-nm CMOS process," in *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 381–384, June 2019. *(Cited on pages 127 and 128.)*

Appendix: Parametric Sub-Harmonic Generation

To have a full picture of the pumping theory with time-varying parameters that is not limited to the frequency multipliers, a divider-by-2 is analyzed with transient periodic capacitance in the form of $\cos(\omega_0 t/2)$ by replacing $2\omega_0$ in (2.41) with ω_0. With only non-zero S_0, $S_{\frac{1}{2}}$ and $S^*_{\frac{1}{2}}$ calculated by (2.7), and only keeping half and fundamental terms, the V-I relation becomes

$$\begin{bmatrix} V_{\frac{1}{2}} \\ V_1 \end{bmatrix} = \begin{bmatrix} R_s + \frac{S_0}{j\frac{1}{2}\omega_0} & \frac{S^*_{\frac{1}{2}}}{j\frac{1}{2}\omega_0} \\ \frac{S_{\frac{1}{2}}}{j\omega_0} & R_s + \frac{S_0}{j\omega_0} \end{bmatrix} \begin{bmatrix} I_{\frac{1}{2}} \\ I_1 \end{bmatrix}, \tag{1}$$

which can be analyzed in the same way as frequency multipliers, noticing that by replacing $2\omega_0$ with ω_0 the integral range for Fourier coefficients becomes 4π instead of 2π.

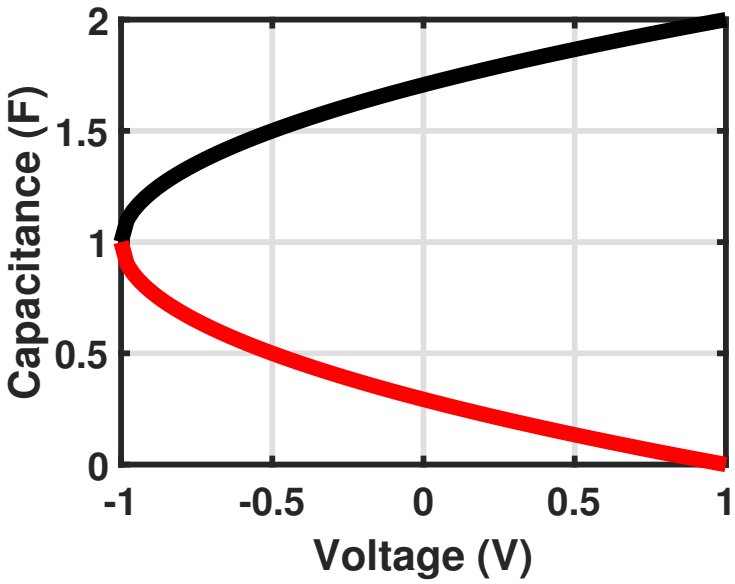
By using the half angle formula, the C-V curve for generation of capacitance in the form of $\cos(\omega_0 t/2)$ can be built as a function normalized to [0, 2]

$$C = \pm\sqrt{\frac{V+1}{2}} + 1. \tag{2}$$

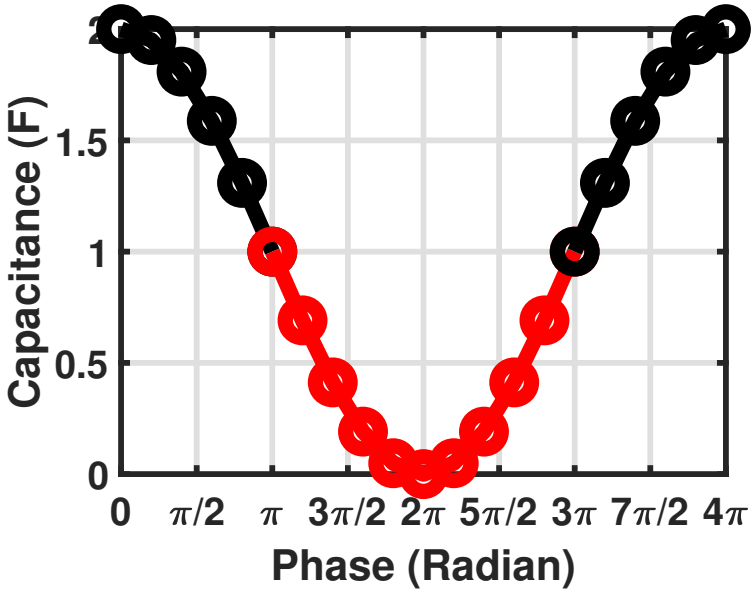
Again, to avoid negative capacitance, the normalized C-V equation is increased by one, so that the resultant C-V curve is positive for the divider as shown in Fig. A.1(a). The corresponding transient capacitance is shown in Fig. A.1(b).

If the elastance other than S_0, $S_{\frac{1}{2}}$, and $S^*_{\frac{1}{2}}$ are all zero, the idler at $3\omega_0 t/2$ can play an important role in the frequency conversion as confirmed by the analysis with the Z-matrix containing S_0, $S_{\frac{1}{2}}$ and $S^*_{\frac{1}{2}}$. By using (2.10), when the capacitance is in the form of $\cos(\omega_0 t/2)$ and the voltage of $\cos(\omega_0 t)$, current components at $\omega_0 t/2$ and $3\omega_0 t/2$ are generated simultaneously. With the idler at $3\omega_0 t/2$, (1) should be modified accordingly.

$1/N$ dividers with $N>2$ are not discussed in this thesis, since there is lack of simple analytical expressions even for the one-third harmonic generation. The functions of the solutions of $\cos(\omega_0 t/N)$ in the form of $\cos(\omega_0 t)$ are piecewise functions with sub-functions defined over overlapping voltage ranges. Therefore, circuits generating the required C-V



(a)



(b)

Figure A.1: (a) C-V curve for a divider-by-2; (b) Transient capacitance for the divider-by-2 under $\cos(\omega_0 t)$ pumping.

curve are expected to exhibit a memory mechanism to generate the transient $\cos(\omega_0 t/N)$ capacitance. The idlers are also possibly needed for the effective high-order sub-harmonic generation.