THE UNIVERSITY OF CALGARY

A Two-Stage Gate Drive Scheme for Snubberless Operation of Power MOSFETs and IGBTs

by

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A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE DEGREE OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL AND COMPUTER

ENGINEERING

CALGARY, ALBERTA

AUGUST, 2001

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ABSTRACT

A central issue in reducing the size and cost of power converters is the control of transistor voltage and current transients during the switching process. Load side snubbers and clamps are bulky and expensive. Increasing the gate resistors values is inexpensive and simple but switching times as well as power losses are increased. A gate drive scheme is investigated which realizes low-noise, snubberless operation of power MOSFETs and IGBTs without an excessive increase in switching losses or switching times. A novel gate driver is presented which uses only a few extra low-voltage components. Experimental results are presented for both a power MOSFET and an IGBT in a hard-switching application. It is shown that the proposed driver scheme obtains an acceptable compromise between switching speed, power dissipation and electromagnetic interferences (EMI).

ACKNOWLEDGEMENTS

Thanks are due on many levels to Dr. Nowicki, my supervisor, but most of all — for complete freedom in research, friendship, good advice, support and encouragement. Thanks!

Several technicians in the Dept. of Electrical Engineering were of great assistance and their help is deeply appreciated. Thanks to Mr. Ed Evanik for all-round support in the lab work, to Mr. Frank Hickli for help in the machine shop, and to Mr. John Shelly and Mr. Garwin Hancock for help with the equipment.

I also wish to thank Dr. Brent Maundy of the Dept. of Electrical Engineering, and Mr. Stan Zwierchowski and Mr. George Squires of the TR Labs for help with the EMI measurements.

Special thanks to all my friends who helped me in many ways during this endeavor. Thanks to Julian Lee for great support and help at every stage of this work. The help and encouragement of Naga R. Mudigonda and Qazi Mehbubar Rahman is also greatfully acknowledged.

To my patient mother.

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LIST OF SYMBOLS AND NOMENCLATURE

τ	Mean carrier lifetime for the diode.
Γ	Reflection coefficient.
C_d	DC-link capacitor.
C_f	Gate drive filter capacitor.
C_{gs}	Gate-source capacitance.
C_{gd}	Gate-drain capacitance.
C_{ov}	Overvoltage snubber capacitor.
D_f	Freewheeling diode.
D_{ov}	Overvoltage snubber diode.
D_{Ls}	Turn-on snubber diode.
E_{off}	Turn-off switching loss.
E_{on}	Turn-on switching loss.
E_{loss}	Total switching loss.
g_m	Transconductance of the power transistor.
i_C	Instantaneous transistor current (IGBT).
i_D	Instantaneous transistor current (MOSFET).
i_{Df}	Instantaneous freeewheeling diode current.
i_G	Instantaneous gate current.
I_0	Load current.
I_D	Steady state transistor current (MOSFET).
I_C	Steady state transistor current (IGBT).
I_{rr}	Diode reverse recovery current.
L	Load inductance.
L_σ	Equivalent stray inductance.
L_e	Transistor module inductance.

L_s	Turn-on snubber inductance.
Q_{rr}	Diode reverse recovery charge.
$r_{DS(on)}$	On-state resistance of MOSFET.
R_d	Gate drive damping resistor.
R_{Goff}	Gate resistor during turn-off.
R_{Gon}	Gate resistor during turn-on.
R_L	Load resistance.
R_{Ls}	Turn-on snubber resistance.
R_{ov}	Overvoltage snubber resistance.
S	Snappiness factor of diode.
$t_{d(off)}$	Turn-off delay time.
$t_{d(on)}$	Turn-on delay time.
t_{fi}	Current fall time during turn-off.
t_{fv}	Voltage fall time during turn-on.
t_{ri}	Current rise time during turn-on.
t_{rv}	Voltage rise time during turn-off.
t_{rr}	Diode reverse recovery time.
v_{GE}	Instantaneous gate-emitter voltage (IGBT).
v_{GS}	Instantaneous gate-source voltage (MOSFET).
v_{CE}	Instantaneous collector-emitter voltage (IGBT).
v_{DG}	Instantaneous drain-gate voltage (MOSFET).
v_{DS}	Instantaneous drain-source voltage (MOSFET).
v_{Df}	Instantaneous freewheeling diode voltage (cathode to anode).
V_d	Dc-link voltage.
$V_{DS(on)}$	On-state voltage drop of MOSFET.
V_{GG+}	Positive rail gate drive voltage.
V_{GG-}	Negative rail gate drive voltage.

$V_{GS(th)}$	Gate threshold voltage.
V_{GS,I_0}	Gate voltage needed to maintain load current in the active region.
V_N	Neutral voltage in LISN.
V_P	Phase voltage in LISN.
Z_{load}	Surge impedance of a motor.
Z_0	Surge impedance of a cable.

CHAPTER 1

INTRODUCTION

1.1 Developments in modern power semiconductor devices

Most of the electrical power produced today is processed by power electronics to make it suitable for various applications, such as dc and ac regulated power supplies, electrical machine drives, electrochemical processes, heating and lighting control etc. At the heart of modern power electronics lie the power semiconductor devices which provide the muscle for power conversion. The power electronics community has long recognized that progress in reducing system size and weight, and in improving system reliability and efficiency are paced by the availability of improved power devices that can be produced at low cost. The ideal device must be able to support a very large voltage in the off-state, carry high currents in a small area with a low on-state voltage drop, and be able to switch rapidly between on and off states. In addition, it is preferable for the device to be able to regulate the rate of rise of current when it is turned on, and to limit the current in the circuit under faulty operating conditions without the aid of external circuit elements. Although much progress has been made in striving towards these goals, the ideal device continues to elude the power semiconductor designer, thus providing strong motivation for further research and development in this area. A brief review of the modern power semiconductor devices is now presented.

(a) Bipolar Devices

The modern age of power electronics began with the invention of thyristor (or silicon controlled rectifier) by Bell Laboratory in 1956. Since its introduction, the thyristor has found widespread applications in phase-controlled and chopper-fed dc drives, lighting and heating control, high voltage dc (HVDC) conversion, static var

compensation (SVC) and ac machine drives. A thyristor can be triggered into conduction by a short gate current pulse, but once the device is conducting, the gate loses its control to turn off the device. Despite this drawback, the thyristor continues its supremacy in the high power market. This is because, at present, no other device can match the performance of these devices, and their application to very high power systems is expected to continue in the forseeable future.

Following the introduction of the thyristor, many other bipolar devices were introduced with improved electrical characteristics. Among these, the most significant are the Gate Turn-off (GTO) thyristor and the power Bipolar Junction Transistor (BJT). A GTO, as the name suggests, is basically a thyristor-type device which can be turned on by a positive gate current pulse, but in addition, has the capability of being turned off by a negative current pulse. GTOs are the most frequently used gate controlled semiconductor at high voltages ($\geq$3300V) and high power ($\geq$0.5 MVA) in traction and industrial converters today. Several manufacturers offer GTOs up to a rated switch power of 36 MVA (6000 V, 6000 A) [1]. The trade off between conduction, turn-on and turn-off behavior of conventional GTOs leads to typical turn-off gains between 3 and 5. The non-homogeneous turn-off transient caused by the constriction of the turn-off current toward the center of cathode islands limits the turn-off dv/dt to about 500-1000 V/μs requiring bulky and expensive snubber circuits. The rather complex gate drive as well as the relatively high power required to control the GTO are other substantial disadvantages.

A BJT, unlike thyristor-like devices, is a continuously current-controlled bipolar two-junction device. Although very popular in the 1970s and 1980s for medium power applications, power BJTs have nearly disappeared from the market due to the availability of devices with superior characteristics. One of the primary difficulties with the application of the BJT is a degradation in the gain of the device with increasing blocking voltage capability. This results in a need for larger control signals

which must be delivered using expensive discrete cicuits. Further, due to a limited Safe Operating Area (SOA) arising from current filamentation, these devices require snubber circuits which raise system cost in their applications.

The relatively large control currents required for bipolar devices result in gate circuits based on discrete components, which increase system size and weight, and inhibit efficient manufacturing. This, combined with their need for expensive snubber circuits has provided the impetus for development of a new generation of power devices with high input impedances which can be controlled by integrated circuits. The most commercially successful power devices with a high input impedance have been based upon Metal Oxide Semiconductor (MOS)-gate structures and are discussed now.

(b) MOS-gate power devices

The first MOS-gate semiconductor power device that became commercially available was the power MOS Field Effect Transistor (MOSFET), introduced in 1976 by Siliconix Inc. The input terminal, the gate, is isolated from the silicon substrate by a thin layer of silicon dioxide. This isolation results in very high current gains for the MOSFET, and in turn, simplified gate drive requirements. In addition, the current transport in a MOSFET occurs solely via majority carriers (electrons for an n-channel structure). This eliminates the large storage and fall times observed in bipolar devices due to minority carrier transport. The MOSFET devices are, therefore, extremely fast compared to other devices making them ideal for high frequency (>50 kHz) applications. The merits of the MOSFET are offset by the fact that for high voltage devices, on-state resistance increases very rapidly with breakdown voltage ($V^{2.5}$). Consequently, the application of MOSFETs has been restricted to low-voltage circuits ($\leq$200 V). The development of Cool-MOS in 1998 enabled a reduction of the on-state resistance, $r_{DS(on)}$, by a factor of 5 to 10 compared to conventional vertical MOSFETs for the same chip area in a voltage range of 600 to 1000 V [2]. At present, the

silicon power MOSFET is the device of choice for applications below 200 V, and with ongoing developments it is expected to make strong inroads in the medium voltage market. The state-of-the-art devices are available with ratings up to 1000 V, 100 A (SanRex) and 60 V, 1000 A (Semikron).

In order to achieve a high input impedance device for high voltage applications, the Insulated Gate Bipolar Transistor (IGBT) was proposed in the 1980's [3]. In the IGBT, a MOS-gate region is used to control current transport in a wide-base high-voltage bipolar transistor. This results in a device with the attractive characteristics of the high input impedance and fast switching performance of a power MOSFET combined with the superior on-state characteristics of bipolar devices. The switching speed of the IGBT can be adjusted by lifetime control processes making it suitable for a wide variety of medium and high power applications. IGBTs have almost completely replaced BJTs in the medium power applications and with the recent improvements in power ratings they are increasingly replacing GTOs and thyristors in high power industrial and traction applications. Today there are 600 V, 1200 V, 1700 V, 2500 V, and 3300 V IGBTs with currents up to 2400 A on the market. Samples of 4500 V IGBTs have been tested in the laboratories of several manufacturers, and recently Eupec introduced 6500 V IGBTs with currents up to 600 A [4].

Despite the outstanding electrical characteristics of the IGBT, the prospects for obtaining a reduction in power losses are being explored by investigation of MOS-gated thyristor structures. Among the various devices proposed [5, 6], the device that is expected to be a dominant player in the future is the Integrated Gate Commutated Thyristor (IGCT). The IGCT is the result of substantial improvements in the conventional GTO structure, gate drive, packaging and the integrated inverse diode as well as changes in the turn-off process, and is considered as a new component. 4.5 kV and 5.5 kV IGCTs with currents up to 4000 A have been developed [4]. The device is already making a dent in the medium voltage market, as evident by ABB's decision to

base its new motor drive line, ACS 1000 (4.16 kV, 0.3-4.9 MW), on IGCT technology [7]. Efforts are ongoing to extend the voltage and power capabilities of the device, and it is expected that the IGCT will prove to be a serious competitor in the medium and high power markets.

1.2 Protection of power semiconductor switches

A power semiconductor device is indeed the most complex and "fragile" element in a converter and needs to be suitably protected against thermal as well as electrical stresses. Although the cost of power semiconductor devices in typical power electronic equipment may not exceed twenty to thirty percent, the total equipment cost is highly influenced by the performance of the power devices. The two main components of this cost are the heat sinks and auxiliary circuits, called snubbers, to alleviate electrical as well as thermal stresses on the switching power devices. A direct consequence of the advancements in the power semiconductor technology has been a reduction in the system size and weight, and improvement in system reliability and efficiency.

The previous section has outlined some of the problems associated with the conventional bipolar devices. The limited safe operating area (SOA) of these devices necessitates the use of snubbers, which are quite bulky and expensive. In addition, the slow switching operation causes switching losses to be quite high. This results in increased cooling requirements, and limits the maximum frequency at which the converter can be operated. By comparison, modern gate controlled devices are quite rugged with square SOAs, and can be switched on and off quite rapidly. Consequently, the converters employing these devices have reduced heat sink and snubber requirements, and can be operated at higher frequencies which offers further savings due to a reduction in the size of passive components. In addition, the modern gate controlled devices offer the advantage that peak electrical stresses can be limited within the SOA, even under fault-level conditions, by proper gate drive techniques— thus

permitting compact and high performance snubberless system operation.

1.3 Motivation behind thesis

It has already been mentioned that gate control techniques can be applied to limit switching transients of modern gate-controlled devices. Several schemes have been suggested to achieve snubberless operation with power MOSFETs and IGBTs, and are reviewed in Chapter 2. All the proposed schemes aim at optimizing the switching performance by allowing the different portions of a switching transition to proceed at different rates. The most obvious and the most common way of achieving this is to change the driver impedance during the stages corresponding to current and voltage transitions — hence the name two-stage control. This thesis, which further explores the two-stage gate drive scheme, derives its motivation from two sources.

First, despite the various implementations, the performance of the two-stage driver scheme has not been evaluated in a comprehensive manner in the literature. One of the aims of this work has been to characterize the said scheme completely in order to provide the circuit designer with some measure of improvement in system-performance to be expected, and whether that improvement is significant enough to justify the cost due to increased drive complexity.

Second, some of the proposed driver schemes are overly complex, while for some others the method for obtaining the driver control signals remains obscure. It has been the author's intention to investigate an alternative means of generating control signals which is simple and uses only low-voltage components so as to facilitate monolithic integration.

1.4 Thesis outline

This thesis comprises of six chapters. They are organized in the following manner.

Fast switching operation usually generates large voltage and current overshoots. These transients and their possible harmful effects are discussed in Chapter 2. A

review of the conventional as well as modern gate-control techniques for switching trajectory control is also presented. Chapter 3 presents the basic hardware and measurement techniques necessary for characterizing the switching performance of the power transistor in a hard-switching application. In Chapter 4 the implementation of the two-stage driver scheme is discussed. A simple driver circuit is presented that can be used to completely characterize the two-stage drive scheme. Also, a novel two-stage driver based on gate-source voltage detection is described. In Chapter 5 the experimental results are presented and the performance of the two-stage driver is compared to the conventional means of transient reduction. Finally, conclusions and suggestions for future work in this area are presented in Chapter 6.

A note on terminology: The circuit symbols for an n-channel power MOSFET and an n-channel IGBT are shown Fig. 1.

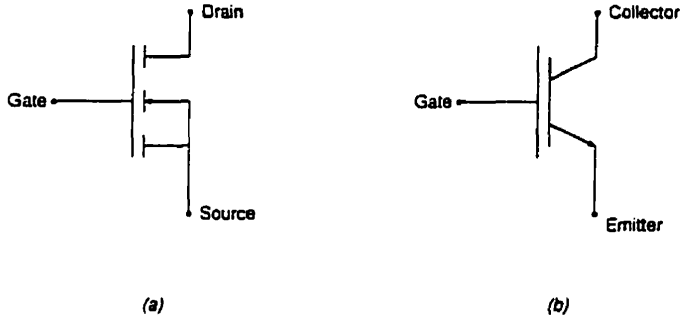

Figure 1.1. Circuit symbols for (a) an n-channel power MOSFET, and (b) an n-channel IGBT.

An IGBT has drive requirements similar to those of a power MOSFET, and the behavior of an IGBT is also quite similar to a MOSFET during most of the switching interval. Due to these reasons and for convenience, most of the discussion in this thesis follows the terminology of one device — the MOSFET, and additional discussion is

provided for the IGBT wherever appropriate. In the following chapters the terms drain and source (i.e. MOSFET related) are used interchangeably with collector and emitter (i.e. IGBT related) respectively.

CHAPTER 2

SWITCHING TRANSIENTS: GENERATION, EFFECTS AND MEANS OF SUPPRESSION

2.1 Introduction

As of now, the most common way of achieving switch-mode power conversion in high-power converters is via *hard switching*, where the transition of the switching devices from one conduction state to the other occurs in the presence of nonzero voltages and currents. The switching characteristics of a power MOSFET and an IGBT for a typical hard switching application and ideal network conditions are discussed in Appendix A. In actual practice, the diodes have a finite recovery time at turn-off and need a negative current, referred to as the reverse recovery current, to sweep away the excess carriers in the drift region. Also, real power circuits have some leakage inductance present due to the interconnect layout of the circuit. The presence of these non-idealities causes voltage and current overshoots during the switching transition, thus placing additional stress on the power devices. These transients and the detrimental effects they may have on the devices and system operation is the subject of discussion of this chapter. Also, the increase in switching speeds over the years has necessarily resulted in higher electrical stresses on the switching devices. A brief review of the various techniques proposed for reducing these stresses is presented in the penultimate section of this chapter.

2.2 Generation of transients

The most common implementation of power MOSFETs and IGBTs is in switching systems where the load inductance is sufficient to maintain a nearly constant current throughout the switching cycle. This is simulated by the use of *clamped inductive load circuit* shown in Fig. 2.1. This simple circuit is valid for almost all power

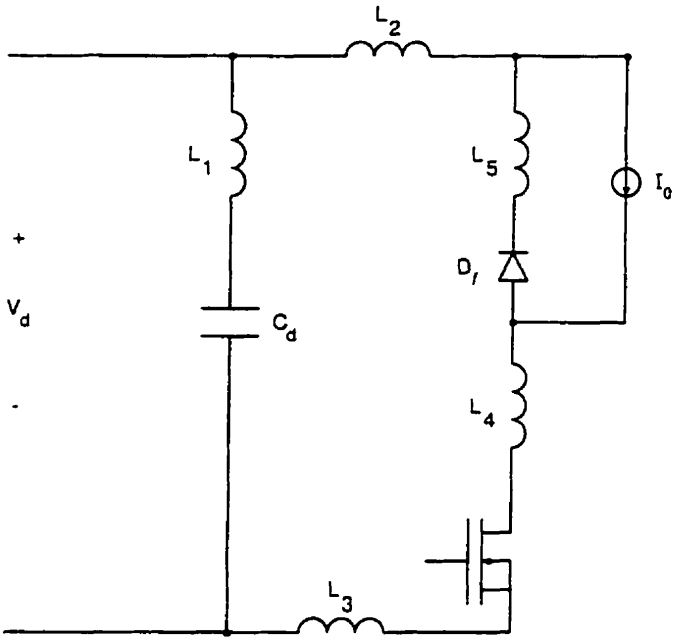

Figure 2.1. Step-down converter with stray inductances shown explicitly.

converter topologies to model the switching operation and is used throughout the rest of this thesis. The stray inductances in the various parts of the circuit are shown explicitly in Fig. 2.1. L_1 is the sum of the capacitor's series inductance and part of the busbar's stray inductance, L_2 and L_3 correspond with the part of the busbar connecting the upper and the lower phase arms, and L_4 and L_5 represent the internal module inductances of the transistor and the diode respectively. This distributed parasitic inductance can be modeled by a lumped inductance L_σ, where L_σ represents the cumulative effect of the various distributed stray inductances.

2.2.1 Turn-off

Fig. 2.2 shows the transistor voltage and current waveforms during the turn-off transient. Prior to $t = t_0$, a gating signal is applied to the power transistor. At $t = t_0$, the transistor voltage begins to rise, but the currents in the various parts of

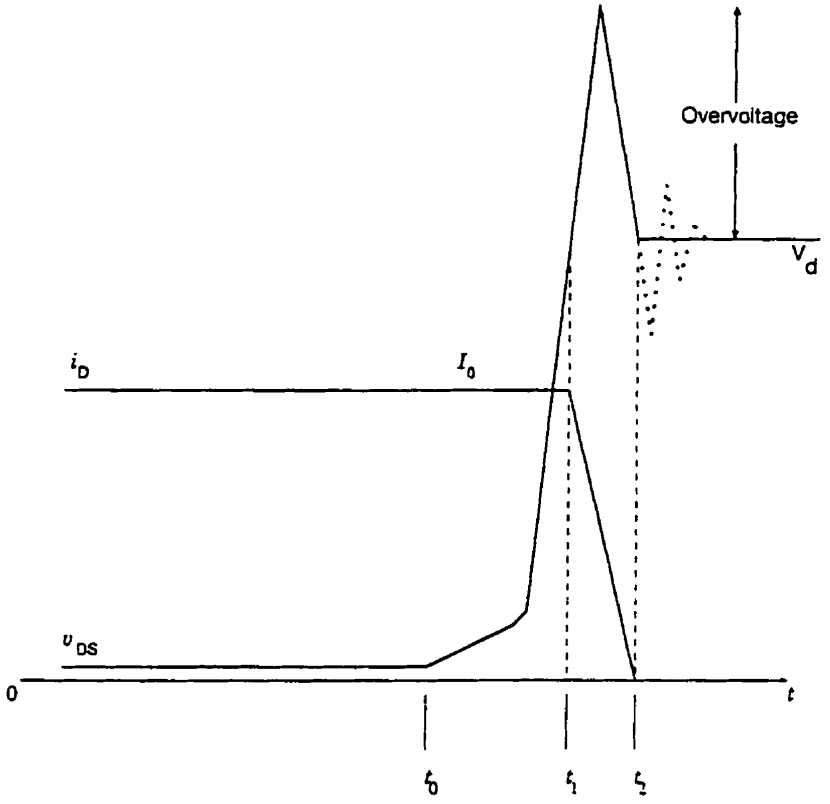

Figure 2.2. Transistor voltage and current waveforms during turn-off.

the circuit remain the same until t_1, when the freewheeling diode begins to conduct. Then the transistor current begins to decrease at a rate dictated by the properties of the transistor and its gate drive. The presence of stray inductance results in an overvoltage across the transistor which is given by:

$$V_{DS,overvoltage} = L_\sigma \cdot (\frac{di}{dt})_{off} \tag{2.1}$$

As seen from Eq. 2.1, the magnitude of voltage overshoot is directly proportional to the rate of current fall. At t_2, the end of current fall time, the voltage approaches the dc link voltage value V_d.

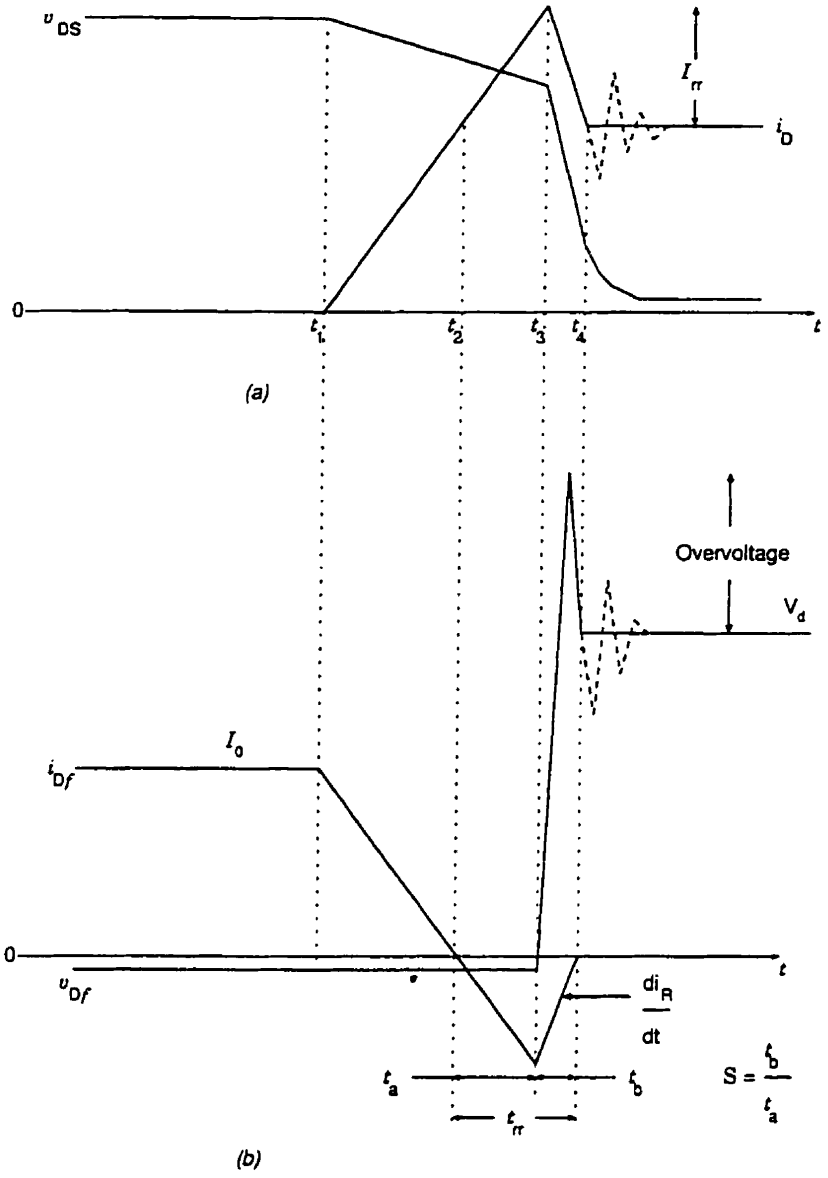

Figure 2.3. Sketch of (a) transistor, and (b) diode switching waveforms during turn-on.

2.2.2 Turn-on

The switching waveforms of the power transistor and the freewheeling diode during the turn-on transient are shown in Fig. 2.3. At some instant prior to $t = t_1$, a gate pulse is applied to the transistor which causes the gate voltage to rise. At t_1, the

load current starts to commutate from the freewheeling diode to the transistor. A positive di/dt combined with the stray inductance, L_σ, causes the transistor voltage to be slightly less than V_d. The current transfer is complete at time t_2 and the diode current has simultaneously reached zero. But the excess carriers stored in the diode's drift region remain, and must be removed before the diode can start to support reverse voltage. The carriers are removed by the combined action of recombination and sweepout by negative diode current. The time associated with the excess charge removal process is the reverse recovery time t_{rr} and the reverse recovery current I_{rr} has a peak value given by

$$I_{rr} = \sqrt{2.\tau.I_0.(\frac{di}{dt})_{on}} \tag{2.2}$$

where τ is the mean carrier lifetime for the diode and I_0 is the load current (assumed constant).

It is evident from the above equation that for a given diode and load current, the value of I_{rr} is determined by the rate of current transfer from the freewheeling diode to the transistor.

As the diode recovers, the decreasing rate of the reverse recovery current, di_R/dt, combined with the stray inductance induces a voltage overshoot across the diode as shown in Fig. 2.3. The di_R/dt is dependent on the rate of current transfer according to the relation

$$\frac{di_R}{dt} = \frac{(di/dt)_{on}}{S} \tag{2.3}$$

where S is the "snappiness" factor of the diode and is defined in Fig. 2.3.

From the above discussion it can be summarized that a large value of $(di/dt)_{on}$ will cause: (1) a high reverse recovery current to flow through the circuit, and (2) a large voltage overshoot across the diode terminals.

It may be added here that regardless of the voltage and current overshoots, switch-

ing from off-state to on-state or vice-versa, itself may be categorized as a transient. And while short switching times are highly desirable for minimizing the power dissipation, fast switching doesn't result in an entirely benign operation. The effects of high speed transitions and of the accompanying transient overshoots are discussed in the following section.

2.3 Effects of switching transients

2.3.1 Circuit internal effects

(a) Voltage overshoots

The most harmful effect of a fast switching transition is the generation of overvoltages – across the transistor during turn-off and across the diode during turn-on. Even a momentary overshoot beyond the rated voltage of the power device will result in junction breakdown and a permanent damage to the device. This condition is most severe under a short-circuit, when the turn-off di/dt may be several times that of under normal operation. It should be noted here that in a bridge configuration the overvoltage appears across the antiparallel device as well (diode in the case of a transistor being turned off, or a transistor in the case of a diode going into conduction), which needs to be suitably protected against the transient overvoltage.

(b) Spurious turn-on of power transistor

In bridge configurations a high dv/dt combined with a large turn-off driver impedance can lead to spurious turn-on of the power transistor. This situation is shown in Fig. 2.4, where the freewheeling diodes D_1 and D_2 are conducting prior to a gate pulse being applied to the transistors T_3 and T_4 at $t = 0$. After the current transfer is complete, the recovery of the outgoing diodes causes a quite high dv/dt (typically 10 V/ns) to be applied across the antiparallel transistors. This applied dv/dt, acting through the drain-gate capacitance (Fig. 2.4(b)) causes the gate voltage to rise mo-

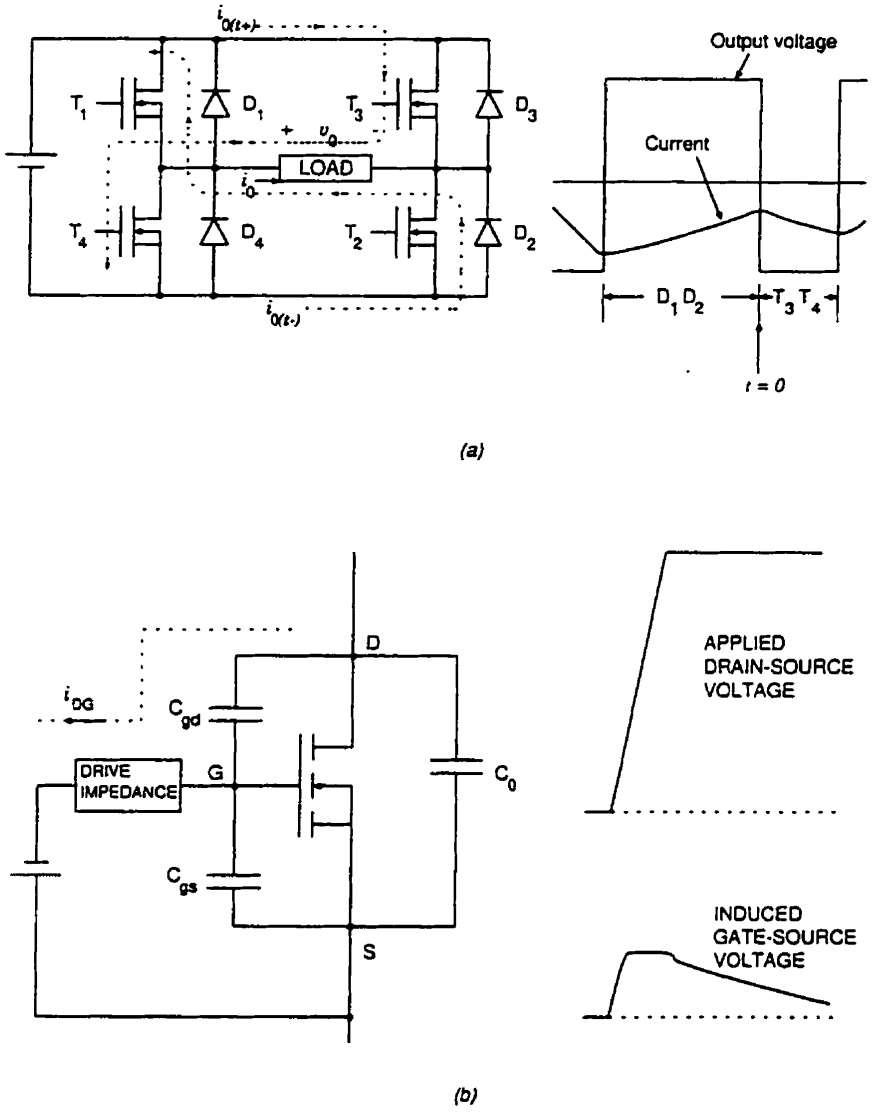

Figure 2.4. dv/dt induced turn-on. (a) Typical circuit where spurious turn-on may occur. (b) Equivalent circuit illustrating the mechanism for conduction due to dv/dt.

mentarily. For a large dv/dt the product of the charging current i_{DG} and the driver impedance may be sufficient to cause the gate voltage to exceed the threshold voltage, causing the transistor to turn-on and leading to additional losses [8].

The dv/dt induced turn-on discussed above in power MOSFETs and IGBTs can be best described as a nuisance, as the phenomenon itself is self-extinguishing and

the power device does not suffer any permanent damage. Under certain conditions, high dv/dt can cause latchup in IGBTs, quite similar to the problem in thyristors [9]. Although a concern for earlier generation devices, this problem has been virtually eliminated in the modern devices by careful optimization of the device geometry [10] and as such, is not discussed here.

2.3.2 External effects

(a) Generation of electromagnetic noise

Rapid voltage and current transitions in a switching power converter result in a spectral content that is rich in high frequency component and can be a source of electromagnetic interference (EMI) to external equipment as well as to sub-systems within the power converter. Fig. 2.5(a) shows a typical switching waveform that is inherent in all switching power converters. Because of short rise and fall times (200 ns typical for medium size variable-speed-drive inverter), this waveform contains significant energy levels at harmonic frequencies in the radio frequency region, several orders above the fundamental frequency. The effect of rise/fall time on spectral content is demonstrated in Fig. 2.5(b) which shows the upper bound on the frequency spectrum of a trapezoidal pulse train with $\tau_r = \tau_f$ [11]. As indicated, the first breakpoint in the spectral bound is related to the pulse width and the second breakpoint is related to the pulse rise/fall time and is $1/\pi\tau_r$. Hence for a given pulse width, the high frequency content of a trapezoidal pulse train is determined primarily by the rise/fall time of the pulse. This point is illustrated in Fig. 2.5(c) which shows the magnitude spectrum for different transition times τ_{r1} and τ_{r2}, where $\tau_{r1} > \tau_{r2}$. Also, a fast switching transition is usually accompanied by high frequency oscillations as indicated in Figs. 2.2 and 2.3. Fourier analysis shows that this ringing has the effect of increasing the emissions in the frequency spectrum near the ringing frequency [11].

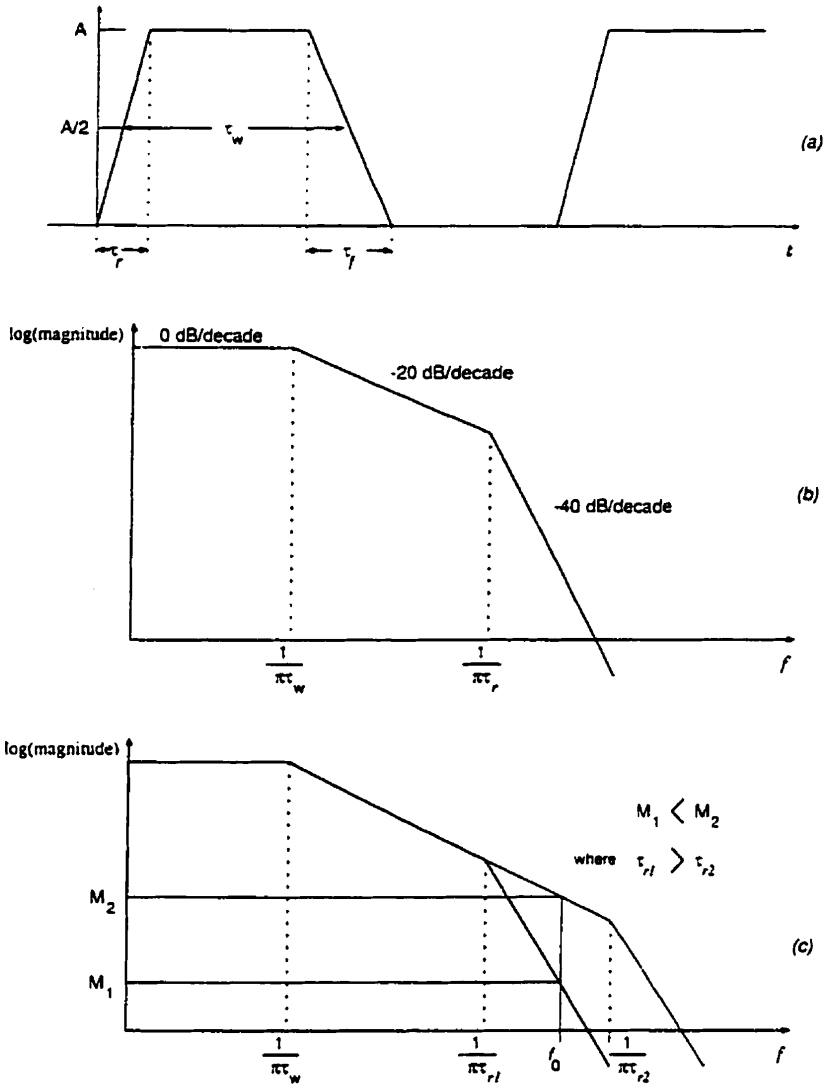

Figure 2.5. Effect of pulse rise/fall time on emission spectrum. (a) Switching waveform that is typical of switching converters. (b) Upper bound on the frequency content of the pulse train in (a). (c) Illustration of increase in high frequency content for short transition times.

In addition, the presence of parasitics contributes significantly to the EMI generated by the system. As discussed in Section 2.2, the presence of stray inductance can cause high voltage transients with wide frequency spectra to appear in the circuit. The parasitic capacitances of heat sinks and transformer windings excited by high

dv/dt cause a noise current to flow through the ground line [12]. Noise problems due to the transient line to ground current are accentuated in motor drives, where the presence of cable line-to-ground capacitance and motor stator winding-to-ground capacitance can cause the capacitive ground current to be significantly high [13]. As the noise current does not have a direct return path to the drive output terminals, it can cause interference with other plant equipment referenced to ground.

(b) Increased motor insulation stress

The migration to IGBTs in medium voltage PWM drives has resulted in increased motor insulation stresses not normally encountered with slower bipolar devices. The output of such drives is a continuous train of steep pulses which are transmitted to the motor terminals via the motor cable. According to transmission line theory the pulses experience a reflection at the motor terminals with the result that the motor terminal voltage is equal to the sum of the incident and the reflected waves [14]. For a motor with the surge impedance Z_{load} and a cable with a surge impedance Z_0, the resulting voltage at the motor terminals is given by

$$V_{receiving\,end} = (1 + \Gamma)\, V_{sending\,end} \tag{2.4}$$

where Γ: Reflection Coefficient $= (Z_{load} - Z_0)/(Z_{load} + Z_0)$.

The above relation gives the maximum voltage possible in case of an infinitely steep voltage pulse. In practice, the pulses have a finite rise/fall time and the cable end voltage is a function of the risetime of drive pulse and the cable length. It is found that a short pulse risetime coupled with a long cable length results in an overvoltage that approaches or even exceeds the value predicted by Eq. 2.4 [15, 16, 17]. Under some conditions the motor terminal voltage can be more than twice the inverter output voltage thus severely stressing the motor insulation system. In addition, a voltage with a high rate of change tends to be distributed along a motor's winding unevenly [15, 16]. This uneven distribution causes a significant stress across the ending turns

which may result in corona or turn-to-turn insulation failure. The damaging effects due to partial discharges accumulate over time thus shortening the machine insulation life. Also, for small drives ($\leq$10 HP) the cable charging current due to high dv/dt may become large enough to cause nuisance overcurrent trips [18].

2.4 Means of transient reduction

2.4.1 Load side solutions (Snubbers)

A snubber is a set of components which reduces the stresses on the power semiconductor switch during the switching interval and transients. A snubber consists of devices such as capacitors and inductors which serve to reduce the switching stress, diodes or other switching devices that will regulate current flow in snubber, and finally some method of discharging the snubber components prior to next switching. Snubber circuits vary in complexity, usually as a result of elaborate methods for discharging the snubber components.

The various snubbers that are available can be broadly classified as dissipative or regenerative snubbers. As the name suggests, for a dissipative snubber the energy stored in the electromagnetic elements is discharged in a resistor as heat. For high power converters these losses may become large enough to limit the maximum operating frequency because of difficulties associated with equipment cooling. A regenerative snubber will store the snubber energy in resonant components (inductors, capacitors, transformers) until it can be discharged into the load or back into the power supply. This improves the system efficiency and reduces the cooling demands. However, the added complexity to the converter has meant very limited use of the energy recovery circuits in practical applications [19].

The literature on snubbers is extensive and it is not possible to list the different snubbers proposed over the years. The operation of two simple switching aid networks used in this project is described here. A circuit for reducing the overvoltage across the

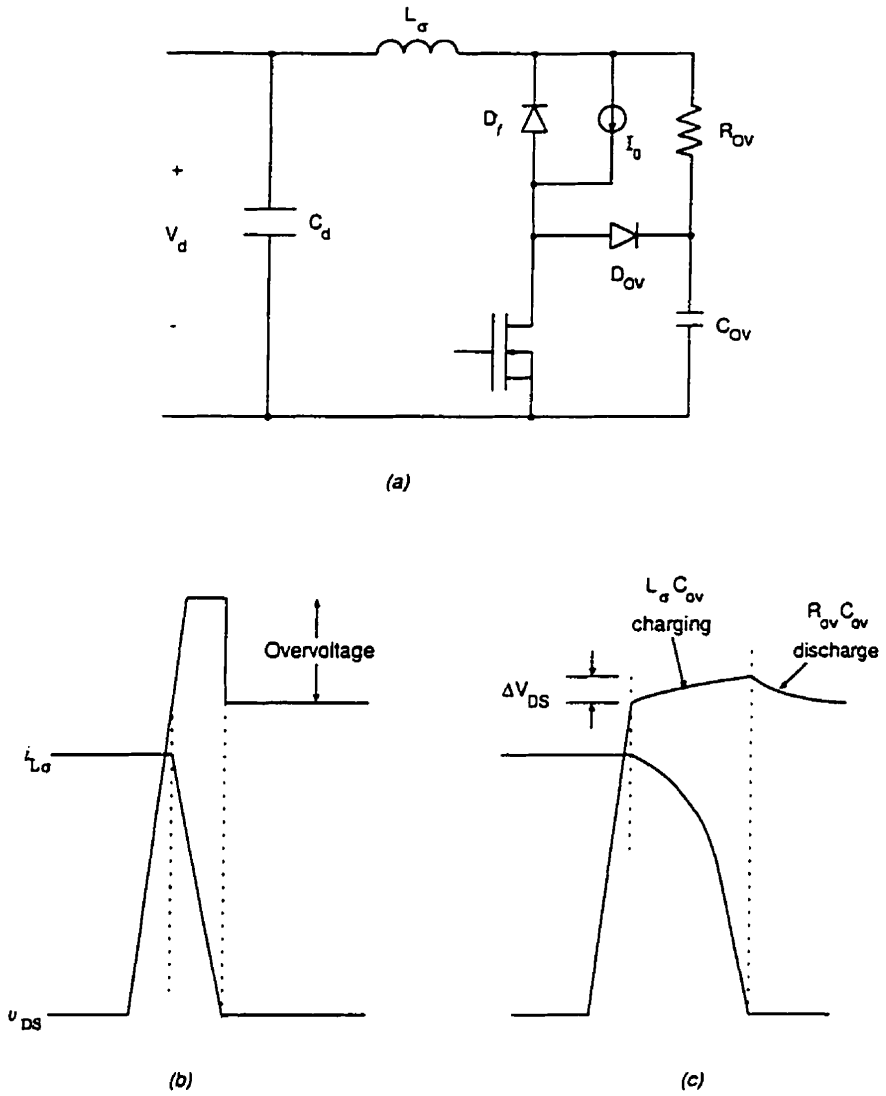

Figure 2.6. Overvoltage snubber. (a) Configuration (b) Sketch of switching waveforms without the overvoltage snubber. (c) Turn-off with an overvoltage snubber.

transistor terminals at turn-off is shown in Fig. 2.6 which also shows the lumped stray inductance L_σ of the circuit. Initially the transistor is conducting and the snubber capacitor C_{ov} is charged to the supply voltage V_d through the resistor R_{ov}. At turn-off the diode D_{ov} provides a path for the energy stored in L_σ to be transferred to the snubber capacitor. Using energy considerations, the overvoltage ΔV_{DS} across the

transistor ($\Delta V_{DS} = \Delta V_{C,ov}$) can be found from the following equation

$$\frac{C_{ov}\Delta V_{DS,max}^2}{2} = \frac{L_\sigma I_0^2}{2} \tag{2.5}$$

Once the current through L_σ has decreased to zero, the overvoltage on the capacitor decreases to V_d through R_{ov}. If the value of stray inductance is known, Eq. 2.5 can be used to estimate the snubber capacitance for obtaining a desired $\Delta V_{DS,max}$. It can be seen that a large value of C_{ov} will minimize the overvoltage. A technique for estimating L_σ is described in Section 3.4.4. The resistance R_{ov} should be chosen so that the capacitor voltage has decreased approximately to V_d prior to the next turn-off of the transistor.

Fig. 2.7 shows the snubber configuration used for reducing the turn-on switching loss and the reverse recovery current. The turn-on snubber reduces the power dissipated in transistor by the virtue of a voltage drop across the snubber inductor L_s during the current growth (similar to L_σ as discussed in Section 2.2). For small values of L_s the rate of current rise is dictated by the transistor and its gate drive circuit and is effectively the same as without the turn-on snubber. In order to reduce the diode peak reverse recovery current, it is necessary to reduce the rate of current rise. This can be achieved by choosing a large value of L_s which causes almost all of V_d to drop across the inductor during current rise time, thus resulting in di/dt given by

$$\frac{di}{dt} = \frac{V_d}{L_s} \tag{2.6}$$

The value of di/dt for a desired value of I_{rr} can be estimated from either Eq. 2.2 or from experimental data. This information then, in turn, can be used to calculate the snubber inductance from Eq. 2.6. During the off-state of the transistor the inductor current I_0 decays towards zero with a time constant L_s/R_{Ls}. The resistor R_{Ls} should be chosen large enough to completely discharge L_s during the minimum off time of the transistor.

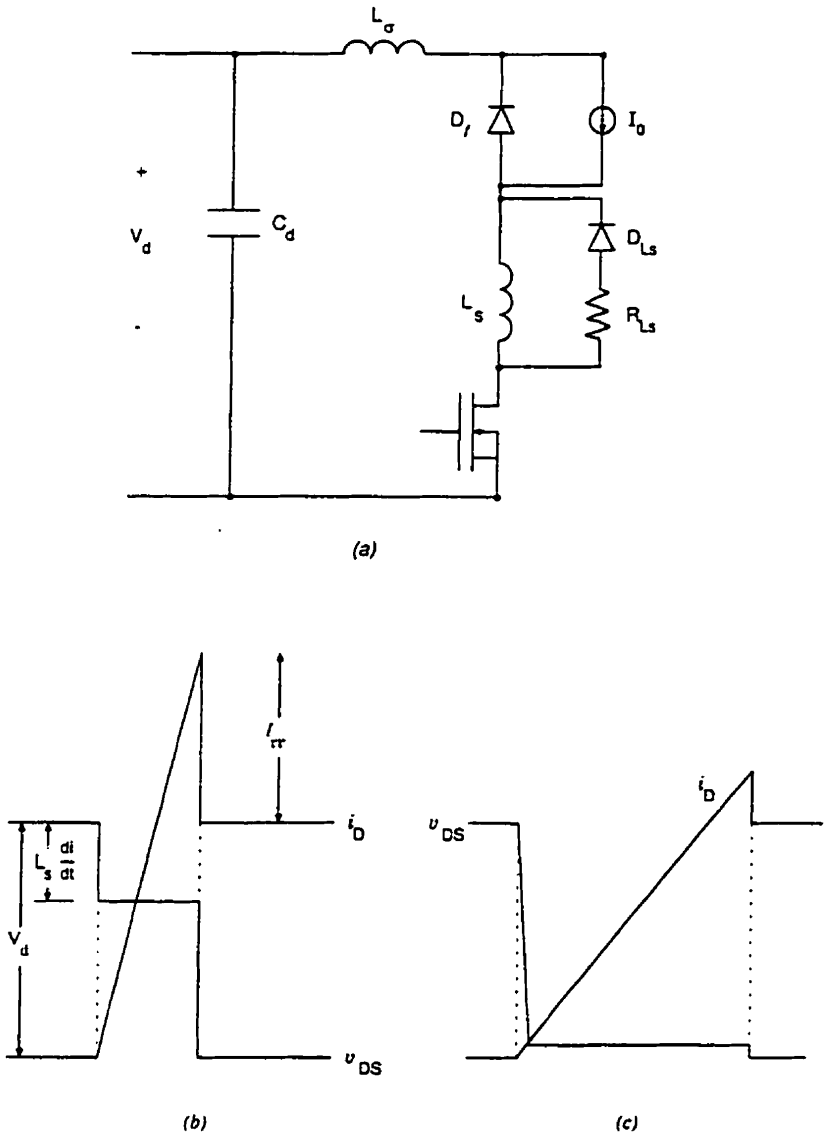

Figure 2.7. Turn-on snubber. (a) Switching waveforms with a small value of L_s or due to the presence of L_σ. (b) Waveforms with a large value of L_s.

Snubbers are, in general, very effective in reducing electrical and thermal stresses in the power switching devices. However, their operation requires extra elements on the load side capable of supporting high voltage, current and power levels. This necessarily results in higher component costs. The design of snubbers itself is a laborious and at times trial and error process as their operation is highly influenced by

presence of parasitics, converter topology and load conditions. In addition, snubbers usually need to be mounted on heat sinks thus increasing space requirements. For devices such as MOSFETs and IGBTs, a reduction in switching stress can be equally obtained by using proper gate driving techniques without the use of snubbers. These techniques are the subject of discussion in the following section.

2.4.2 Gate Control Techniques

Since the introduction of MOS-gate power devices, circuit designers have tried to use the gate-control capability of these devices to reduce overvoltage and overcurrent transients. The simplest way has been to simply slow down the entire switching process by increasing the value of gate resistor R_G (henceforth referred to as the Conventional Gate Drive or CGD). This method was extended to develop asymmetric switching schemes which employ different gate resistors at turn-on and turn-off (Fig. 2.8(a)), and pulse-shaping techniques which allow the rate of rise and fall of gate voltage to be regulated (Fig. 2.8(b)) [20, 21]. The expressions for selecting optimum values of turn-on and turn-off gate resistors for controlling $(di/dt)_{on}$ and $(di/dt)_{off}$ respectively were presented in [22].

Since the slopes of both current and voltage depend upon the value of R_G, increasing the gate resistor to reduce di/dt also causes a reduction in dv/dt. As discussed in Appendix B, this leads to unacceptably high switching losses and delay times. To overcome this problem many techniques have been proposed which allow an independent control of the current and voltage slopes, and are briefly discussed now.

Oljaca [23] proposed adding an extra capacitor between the gate and emitter terminals. The added capacitor provides the designer with an extra variable and allows an independent control of slopes at turn-off. For a given $(di/dt)_{off}$, a careful selection of component values allows the device to be operated at much higher $(dv/dt)_{off}$ thus leading to a reduction in the turn-off switching loss.

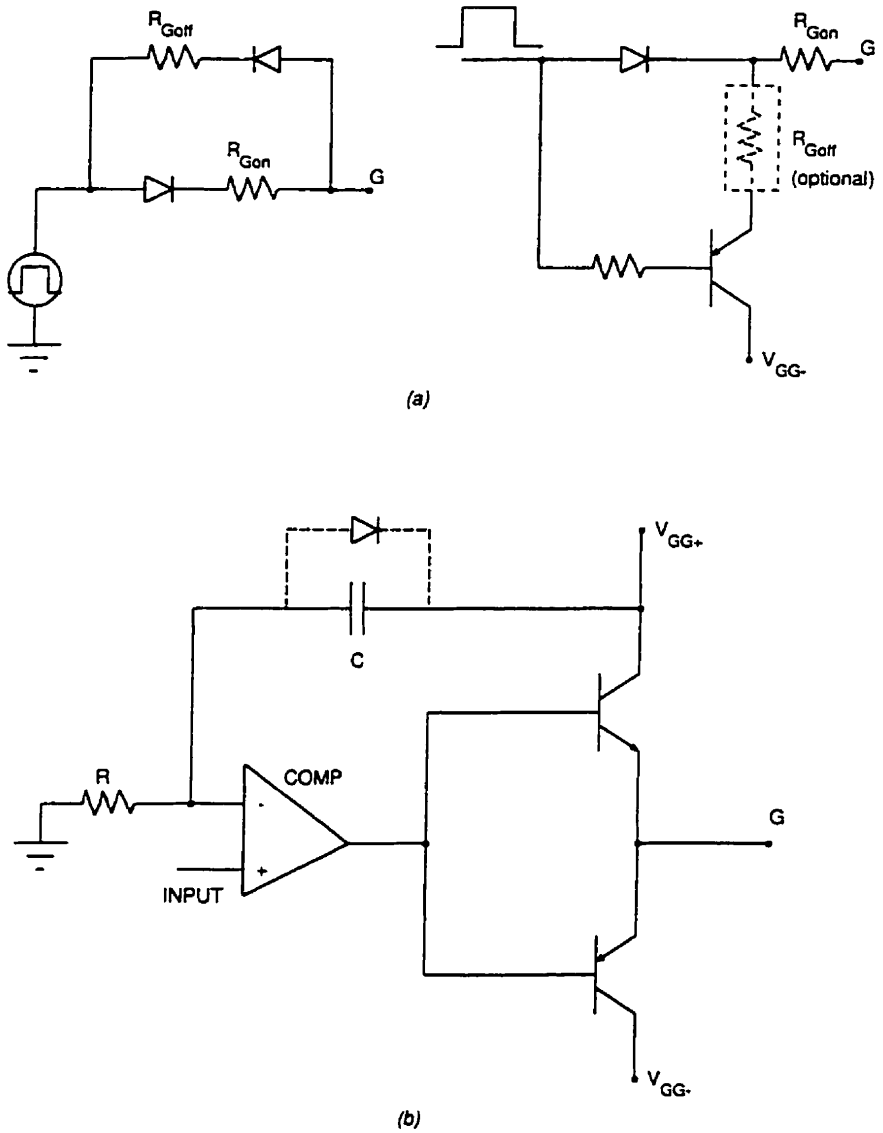

Figure 2.8. Examples of gate drive techniques for asymmetric switching. (a) Schemes employing different gate resistors at turn-on and turn-off. (b) Driver for controlled rise/fall of gate voltage.

The idea of using two gate resistors during the turn-on switching transition was first proposed by Galluzo *et al.* [24]. Fig. 2.9 shows the proposed scheme wherein the $(di/dt)_{on}$ is kept low by selecting a large value of R_1. After a suitable delay Q_2 is turned on after Q_1 and the collector voltage falls rapidly as determined by the small

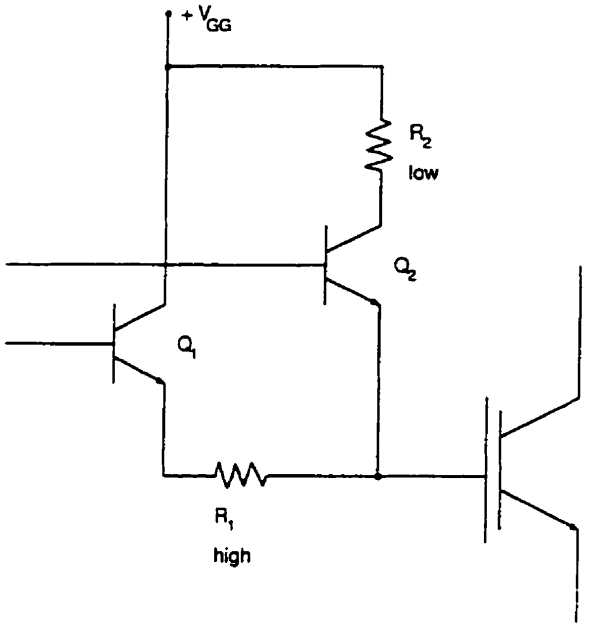

Figure 2.9. Turn-on scheme proposed in [24].

gate resistor R_2.

Using multiple gate resistors during the switching transient also forms the underlying principle of the driver circuit proposed by Weis *et al.* [25] for improved turn-off characteristics. The turn-off process begins with the gate capacitance being rapidly discharged by a low value of gate resistance, thus causing the collector voltage to rise quickly. During the interval of current fall, a switch is made to a high value of gate resistor which results in a low $(di/dt)_{off}$ and consequently low overvoltage. At the end of the turn-off process, the driver resistance is reverted to a small value to avoid parasitic turn-on of the power transistor.

Eckel *et al.* [26] proposed a two-stage gate drive circuit for optimizing the turn-off performance at overcurrent and short-circuit currents. Under this scheme, turn-off speed is kept as high as possible till nominal current levels for minimal turn-off losses. For overcurrent conditions, the overvoltage is kept low by reducing di/dt by switching

over to a high value of turn-off gate resistor.

Igarashi *et al.* [27] presented a driver scheme shown in Fig. 2.10 for low-noise, snubberless operation of IGBTs. This technique uses the voltages induced across the module wiring inductance L_e and a saturation type reactor L_2 for the control of gate charging current during turn-on and turn-off respectively. A low value of I_{rr} is achieved by reducing the magnitude of gate current during the recovery period of the free wheeling diode. During turn-off an extra charge is applied to the gate during the current fall time. This reduces the turn-off di/dt and hence the surge voltage across the transistor terminals. The turn-on scheme as suggested has two serious drawbacks. First, it requires a reactor to be inserted in the power circuit with the primary being capable of supporting the full load current. With a strong trend towards the use of power modules instead of discrete devices, this itself may not always be possible. Second, although the scheme works well for a half-bridge configuration, its implementation for a three phase bridge poses a problem where the current transfer may occur from either of the remaining two phases.

These shortcomings were overcome with a technique employing the module wiring inductance for detection of di/dt at both turn-on and turn-off [28]. The latter scheme reduces the switching speed during the entire turn-on interval. This causes a severe increase in turn-on switching loss thus rendering the scheme useful only at low current levels. The turn-off scheme was also slightly modified to execute di/dt suppression only when collector current is large.

The driver scheme investigated in [29] achieves di/dt reduction at turn-off by applying a positive current pulse to the gate, generated by a RC high pass filter. The magnitude of the current pulse is proportional to the collector current, hence the scheme reduces overvoltages effectively at fault current levels. The turn-on scheme is to decrease the rising rate of collector current by increasing the input capacitance when gate emitter voltage is greater than the threshold voltage. The presence of

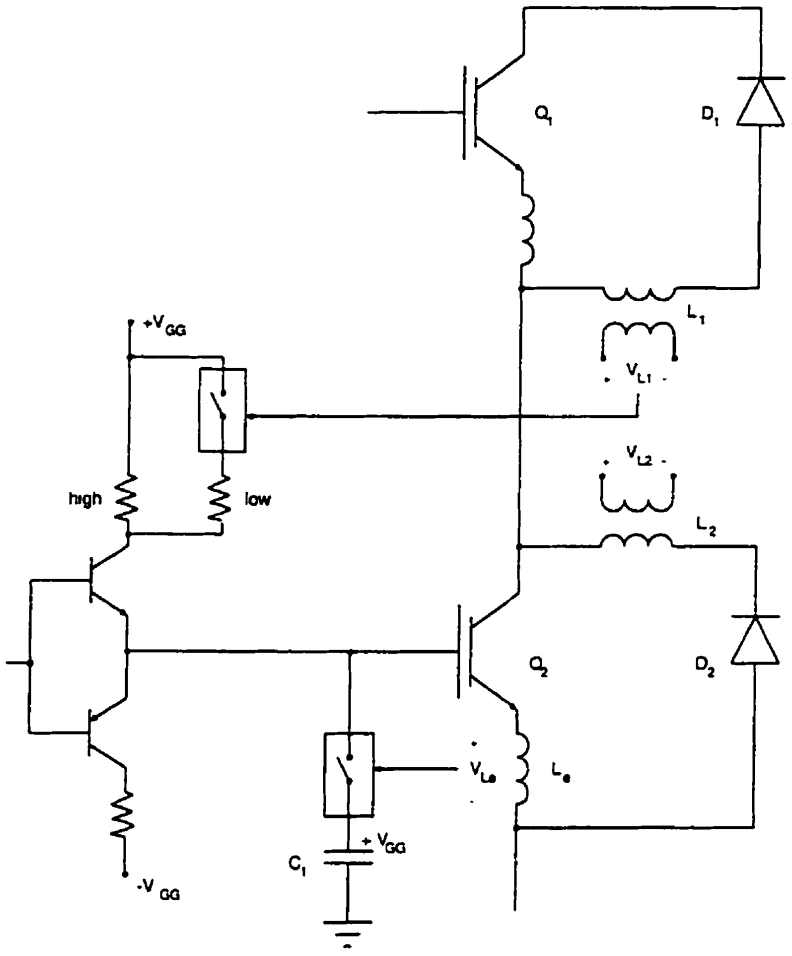

Figure 2.10. Gate drive scheme for snubberless operation proposed in [27].

capacitor during the entire turn-on interval increases voltage fall time and switching loss. Thus, compared to CGD switching this scheme offers only a slight improvement in the form of reduction in turn-on delay time.

John *et al.* [30] investigated a three-stage active gate drive scheme for high power applications. The technique achieves reduction in device switching stress and EMI generated without sacrificing high speed operation. The proposed scheme effectively reduces overvoltages at high current levels and can also dampen oscillations during low current turn-on transient in the IGBT. However, the scheme suffers from the

drawbacks of high control complexity and the fact that the gate drive has to be tuned to operate with the individual device.

Fig. 2.11 shows a technique described in [31] for independent voltage and current gradient control. The circuit controls the gate chargeup/discharge process by providing additional current pulses at suitable instants. The trigger signals for the current generator and current sinker are obtained using a RC high pass filter. A later modification of this approach employs a phase-locked-loop to determine the instant of current injection at turn-on [32], which can lead to poor operation during transient load current conditions. Also, the turn-on delay time is still quite large because a fixed gate resistor is used to limit di/dt during turn-on.

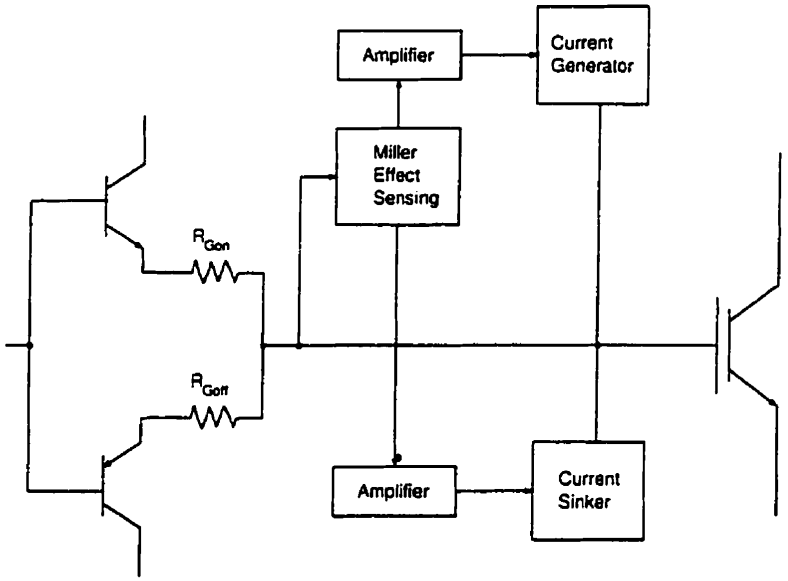

Figure 2.11. Schematic of the circuit proposed in [31].

The IGBT has been used in the active region at turn-off by using a closed loop high speed operational amplifier in the gate driver circuit [33]. In this case, the turn-off dv/dt can be precisely controlled according to the reference voltage command. The

problem with this method is the large switching loss at turn-off, and the fact that the circuit cannot be easily extended to turn-on operation under inductive load switching. The method presented in [34] also uses closed control loops to reduce di/dt at turn-on and dv/dt at turn-off. The technique is claimed to limit the transients even under short circuit conditions. It should be noted here that most of the devices available today are designed to be latch-free [10]. Hence dv/dt reduction is not really necessary for proper device operation. Second, the motor insulation problems due to high dv/dt usually arise only for long cable runs. Choosing application-specific solutions [16, 35] may result in a more efficient and cost-effective operation.

A high performance current source gate drive used in a modular traction converter was reported in [36]. Using a current source drive achieves fast settling of the gate current at different levels and also reduces sensitivity to the variation of internal gate resistors inside the IGBT module. The drive unit uses open loop control to keep di/dt and dv/dt constant and can be programmed to obtain snubberless operation of the inverter.

2.5 Conclusions

Dissipation in a hard switching power converter can be reduced by decreasing the switching times of the power devices. However, fast switching operation is usually accompanied by transient overshoots in voltage and current. The principles underlying the generation of these transients, and their effects on the switching devices and on the electromagnetic environment have been discussed in this chapter. Load side snubbers used to mitigate these effects can be quite bulky and expensive. Non-latching elements such as power MOSFETs and IGBTs allow the transients to be reduced by proper gate control. A critical review of the various gate control techniques aimed at optimizing the switching behavior has been presented in Section 2.4.2. It should be pointed out here that although a very high dv/dt can lead to noise and insula-

tion problems, most gate control schemes tend to maximize dv/dt for reducing the switching loss. This may require external components for some applications but, in general, seems to optimize system cost and operation. This is also the supporting argument for the driver scheme discussed later in this thesis, which switches the power transistor at a high dv/dt level.

CHAPTER 3

BASIC HARDWARE AND MEASUREMENT TECHNIQUES

3.1 Introduction

The study of switching characteristics of a power transistor requires a switching test circuit, a driver to turn the device on and off, and measurement equipment to characterize the performance. These three fundamental issues form the subject of discussion of the present chapter. The chapter begins with a review of the basic requirements for a good gate drive for power MOSFETs and IGBTs. These requirements have been incorporated in the design of a conventional gate drive (CGD) circuit, which is capable of switching the power transistor on and off rapidly. This is followed by a discussion of the practical implementation of the *clamped inductive load circuit* introduced in Chapter 2, which forms the test circuit for observing the switching behavior of transistor under different conditions. The latter part of this chapter documents the measurement techniques employed for characterization of the driver schemes.

3.2 MOSFET/IGBT gate drives

As discussed in Chapter 1, compared to bipolar devices MOSFETs and IGBTs have relatively simple gate drive requirements because of the insulated gate structure. However, these devices require the transfer of charge to and from the gate electrode in order to turn the channel on and off. This transfer must be rapid in order to obtain fast switching speeds, with the result that peak gate currents can be very high.

3.2.1 Gate-Drive Requirements

Switching a MOSFET/IGBT from the non-conducting to conducting state requires that the gate-source voltage be raised above the gate threshold voltage, $V_{GS(th)}$ (typically 2-4 V for MOSFET, 3-5.5 V for IGBT). The minimum gate voltage required for the conduction of the maximum drain current can be determined from the transfer characteristics of the device (5-8 V typical). An overdrive above the minimum value reduces the channel resistance and current rise time; the maximum value being limited by considerations of turn-off delay time and gate-source breakdown voltage ($\pm$20 V).

For turn-off the gate voltage must be lowered below $V_{GS(th)}$. An off-state gate voltage of zero (0 V) usually provides adequate noise immunity. The turn-off speed of a MOSFET can be increased by using a negative gate bias at the expense of increased turn-on delay time, although a negative drive voltage only slightly affects the turn-off time of an IGBT. However, a negative gate bias is commonly used for both MOSFETs and IGBTs in bridge configurations to prevent dv/dt induced turn-on [24].

Furthermore, fast switching times require rapid transfer of charge to and from the gate capacitance. This necessitates a driver with high peak current capability and low output impedance.

3.2.2 Implementation

A simple gate drive circuit incorporating the requirements discussed above was designed and constructed, and is shown in Fig. 3.1. The driver provides a bipolar output of +15/-5 V for rapid turn-on and turn-off of the power transistor. The output stage consisting of discrete transistors in a totem-pole arrangement is capable of sourcing and sinking large gate currents. The output transistors act as emitter followers and offer low output impedance. The gate resistors R_{Gon} and R_{Goff} allow independent control of turn-on and turn-off speeds.

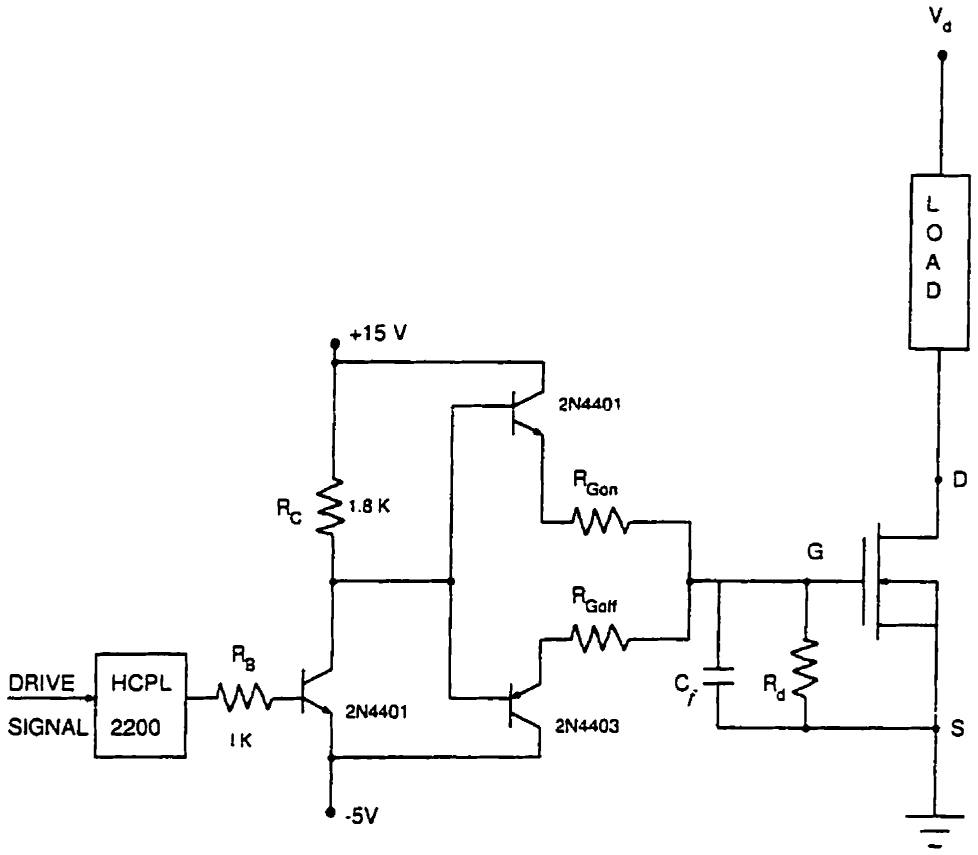

Figure 3.1. Basic driver circuit.

The control signal for the driver is generated using LabWindows/CVI [1] software [37]. An optocoupler at the input stage provides electrical isolation between the drive signal and the rest of the circuitry. The Hewlett-Packard HCPL-2200 devices are employed because of their high speed operation, hysteresis and low input current requirement (1.6 mA).

Special attention is given to minimizing the stray inductance in the drive circuit. In particular, the source inductance is kept as low as possible to avoid switching disturbances due to common impedance coupling [38]. Also, a small filter capacitor C_f and a damping resistor R_d are added across the gate and source terminals to avoid

[1] LabWindows/CVI is a registered trademark of National Instruments Corporation

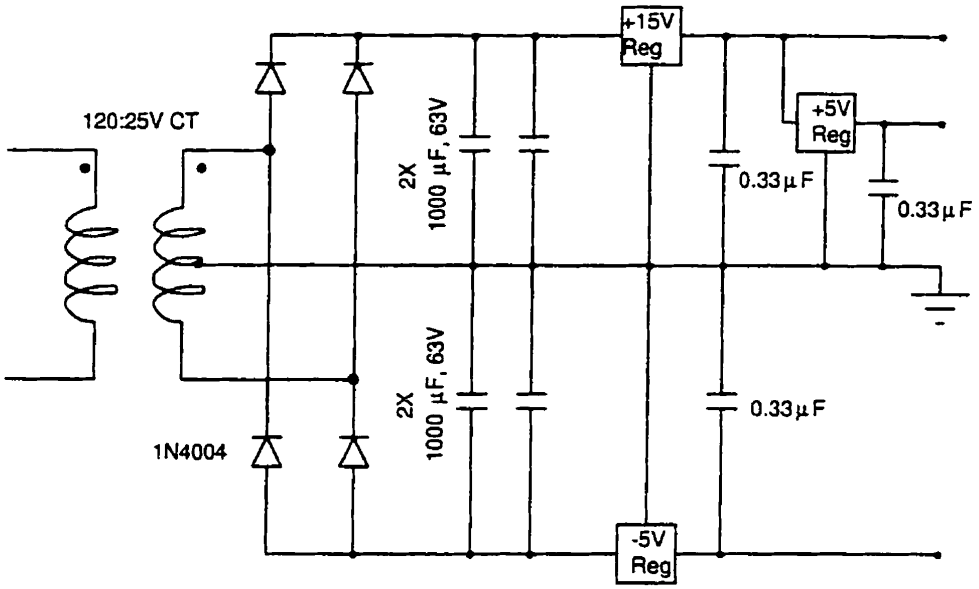

Figure 3.2. Schematic of the gate drive power supply.

oscillations and the problem of retriggering of the device at turn-off [9].

3.2.3 Power Supply

Fig. 3.2 shows the power supply designed for the gate drivers. It consists of a center-tapped, 120/25 V transformer and a full wave rectifier at the output. The rectified voltage is filtered using two 1000 μF electrolytic capacitors connected in parallel. The voltage regulators 7815, 7805 and 7905 give regulated outputs of +15 V, +5 V and -5 V respectively. The 0.33 μF capacitors at the output of regulators improve the transient response and stability.

3.3 Switching test circuit

Fig. 3.3 shows the converter, a DC chopper, used as the test circuit to study the switching characteristics of the power MOSFETs and IGBTs. As discussed in Chapter 2, the switching of the power transistor simulates the operation of a low-side semiconductor switch in an inverter driving an inductive load, such as an induction

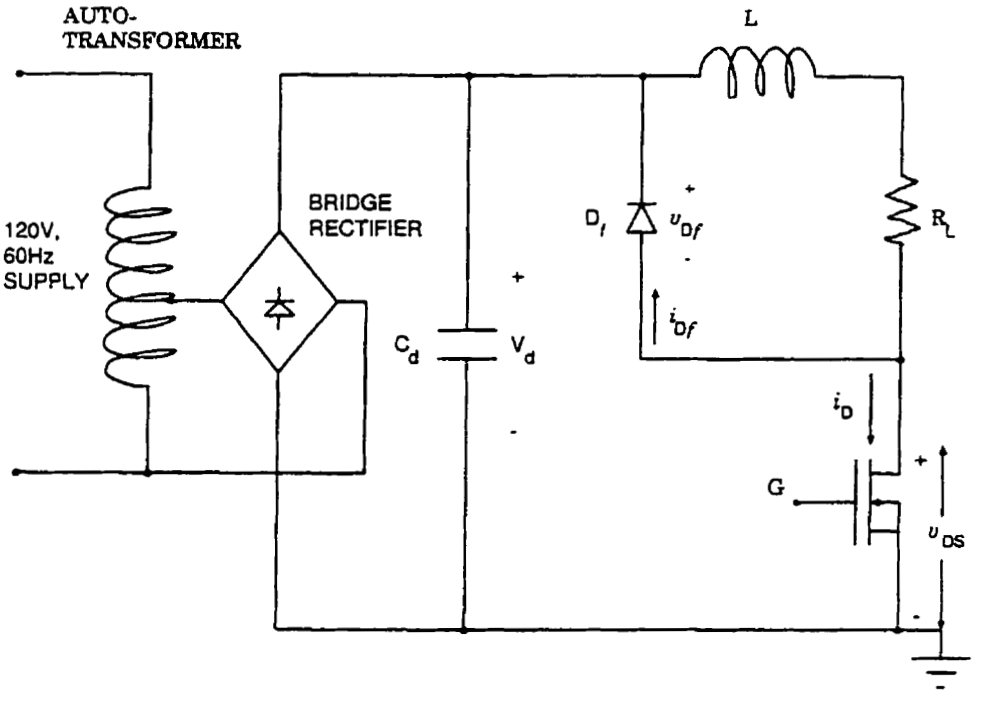

Figure 3.3. Switching test circuit.

motor. In addition, this configuration offers two practical advantages over the conventional DC chopper. First, the source of the transistor is grounded. This permits the use of a single-ended oscilloscope. Second, from the considerations of volts-second balance, a small duty-ratio is required to obtain an almost constant load current. This greatly reduces the conduction losses of the transistor and makes the cooling of the power device much easier.

A test circuit employing MOSFET devices and another with IGBTs was constructed. The power converter is fed from an autotransformer to limit the inrush current. Tables 3.1 and 3.2 give details of the components used and the switching conditions.

As seen from Table 3.1, the load time constant (L/R) is of the order of a few milliseconds, which is much higher than the periodic time of the switching frequency.

Hence the load can be modeled as a constant current source.

The choice of freewheeling diode requires some discussion. Fig. 3.4 shows the turn-on waveforms of a power MOSFET with a fast-recovery rectifier, FR604 (t_{rr}=200 ns), as the freewheeling diode. The transistor exhibits parasitic oscillations of approximately 81 MHz in the active region. These oscillations were thought to be induced due to the snap-recovery characteristics of the diode. A reduction in the amplitude of oscillations by using an RC snubber across the diode confirmed this hypothesis. A better solution is to use a rectifier with soft recovery characteristics. Hence, the HexFred diodes are employed, which are state-of-the-art soft recovery rectifiers with t_{rr} <50 ns.

Table 3.1. Component numbers and ratings of the devices used in the power converter.

COMPONENT	CONVERTER EMPLOYING	
	MOSFET	IGBT
Bridge Rectifier	PB64MS 400 V, 6 A	MB104 400 V, 10 A
DC Link capacitor, C_d	2900 μF, 400 V	2900 μF, 400 V
Freewheeling diode, D_f	HFA08TB60 600 V, 8 A	HFA25TB60 600 V, 25 A
Inductor, L	10 mH	10 mH
Load resistor, R_L	2 Ω	1 Ω
Power transistor	IRF740 400 V, 10 A	IRGBC30U 600 V, 23 A

Table 3.2. Circuit conditions for studying the power transistor switching behavior.

TEST CONDITION	CONVERTER EMPLOYING	
	MOSFET	IGBT
DC link voltage, V_d	100 V	100 V
Load current, I_0	5 A	15 A
Switching frequency, f	8 kHz	8 kHz
Duty ratio of transistor, D	11.7%	20%

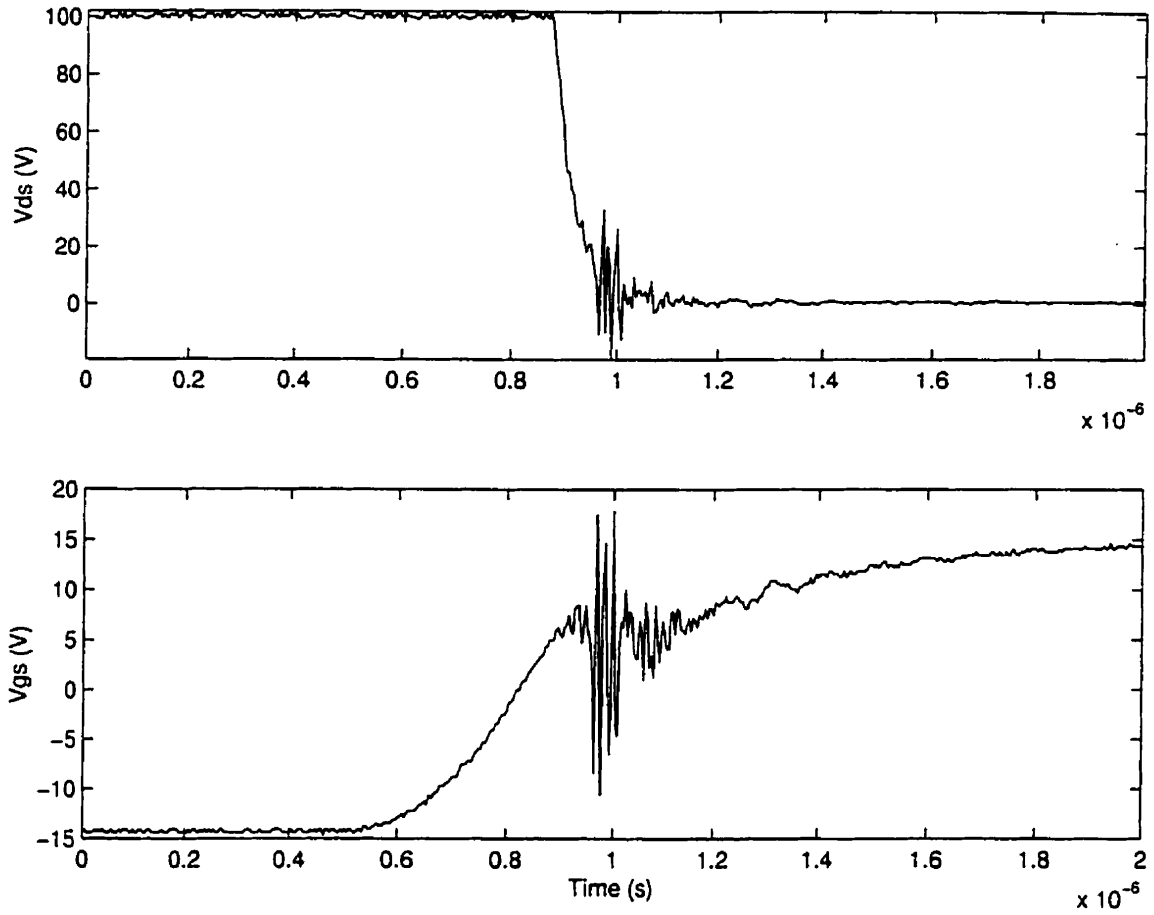

Figure 3.4. Oscillations in MOSFET due to snap-recovery characteristics of the free-wheeling diode.

3.4 Measurement Techniques

3.4.1 Voltage and Current

The transistor voltages are measured using HP54600A oscilloscope and HP x10 probes. Tektronix A6303 current probe with AM603 amplifier is used to measure the current.

3.4.2 Switching Loss

The energy lost in transistor when it switches on or off is

$$E_{loss} = \int_{t_1}^{t_2} v_{DS}(t).i_D(t)\,\mathrm{dt} \tag{3.1}$$

where t_1–t_2 is the switching interval.

An accurate measurement of this energy loss is essential for characterization and comparison of the driver techniques discussed later in this thesis. For this purpose, a simple method has been devised by the author which gives fairly accurate and reliable results. First, the transistor voltage and current waveforms displayed on the oscilloscope are sampled and transferred to computer as data arrays. These arrays are then multiplied and the product is numerically integrated over the switching interval to give switching loss incurred in the transition. The energy figures reported were measured under the following conditions [8]:

Turn-on Switching Loss, E_{on}: The turn-on loss is measured over the time interval during which the current rises from 5% of its on-state amplitude and the drain voltage falls to 5% of its off-state value. E_{on} specified in this manner includes the loss component due to reverse recovery of the freewheeling diode.

Turn-off Switching Loss, E_{off}: This energy is measured over a time that starts when the drain voltage has risen to 5% of its off-state value and goes on for 1 μs. This specification ensures that all turn-off tail energy of IGBT is included in E_{off}.

3.4.3 Conducted Emissions

The bulk of electromagnetic noise generated by power electronic equipment lies between the switching frequency and a few megahertz. Since conduction is the dominant mode of transmission in this frequency range, only conducted EMI is measured.

The purpose of a conducted emission test is to measure the radio frequency noise currents that are placed on the utility power grid due to the operation of equipment under test (EUT). The amplitude of these emissions depends not only on the characteristics of the EMI source but also on the impedance seen looking into the ac power system. The high frequency (HF) mains impedance is not nearly constant; rather, it is highly variable in time, location and frequency [39]. To ensure repeatability and comparability of EMI measurements, a standard load impedance must be created at the measurement point. This condition is met by inserting an interface circuit between the EUT and the mains. The interface circuit is called a *line impedance stabilization network* (LISN), also known as a *power line impedance stabilization network* (PLISN), or *artificial mains network* (AMN). The LISN establishes a standard profile of load impedance (50 Ω) toward the EMI source and also filters out HF noise on the mains that could contaminate the measurement. The topology of a LISN and its component values depend upon the frequency range of the conducted emission test (450 kHz–30 MHz for FCC [2] measurement, 150 kHz–30 MHz for CISPR measurement, and 10 kHz–30 MHz for VDE measurement). The *American National Standards Institute* standard, ANSI C63.4-1992, chosen as reference for the conducted emissions test stipulates the frequency range of measurement as 450 kHz–30 MHz [40]. The LISN specified for use over this frequency range was constructed and is shown in Fig. 3.5.

Table 3.3 gives the impedance of the components employed at the lower and the upper bounds of the frequency range of interest. It can be seen that the capacitors are essentially short circuits and the inductor presents a large impedance. The inductor L (50 μH) and the capacitor C_2 (1 μF) prevent ambient noise in the power lines from being measured. The capacitor C_1 (0.1 μF) and the 50 Ω resistor accomplish the

[2]The legal requirements for conducted and radiated emissions that a commercial product must comply with vary from country to country. The respective regulatory bodies in the US and Germany are *Federal Communications Commission* (FCC) and *Verband Deutscher Elektrotechniker* (VDE). *Comite International Special des Perturbations Radioelectriques* (CISPR) is not a regulatory body but develops standards which may be adopted by specific governments.

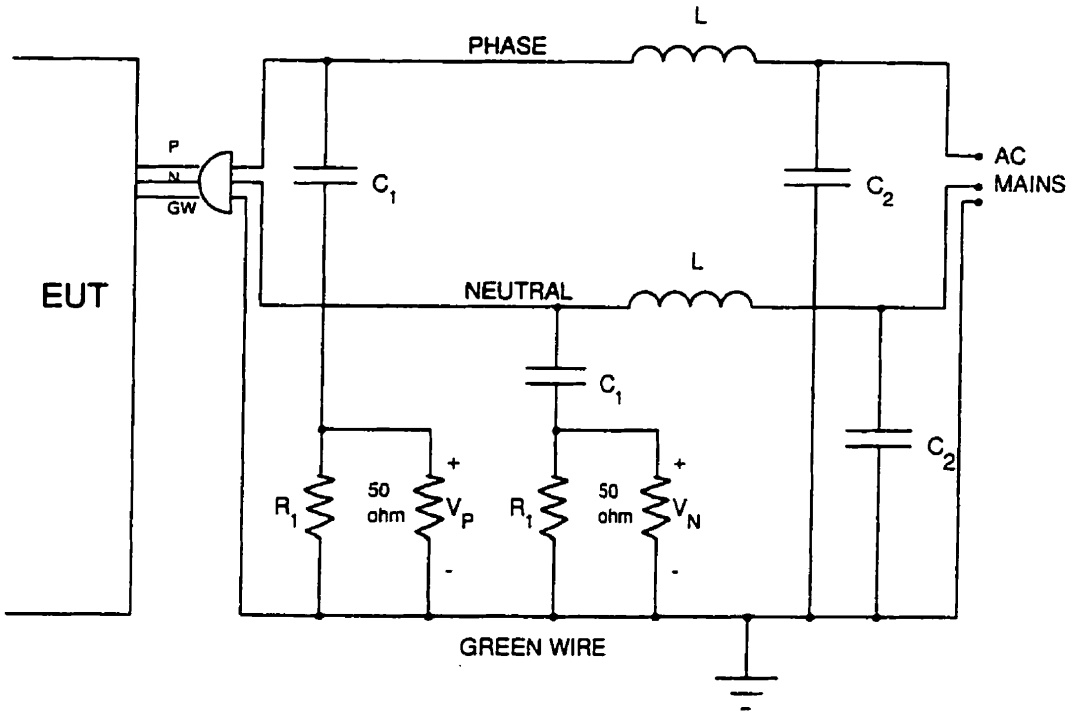

Figure 3.5. Schematic of Line Impedance Stabilization Network.

Table 3.3. Impedance of reactive elements of LISN over the frequency range of measurement.

Element	Z_{450kHz}	Z_{30MHz}
50 μH	141.3Ω	9420Ω
0.1 μF	3.54Ω	0.053Ω
1 μF	0.354Ω	0.0053Ω

task of providing a nearly constant impedance to the EMI source. The capacitor C_1 is included to prevent any dc from overloading the test receiver, and the resistor R_1 (1 kΩ) is used to provide a discharge path for C_1 in the event that the 50 Ω resistor is disconnected. The noise currents exiting the EUT via the phase and the neutral wires cause proportional voltage drops V_P and V_N respectively across the 50 Ω resistors,

which are then measured using a spectrum analyzer.

Data in [41] was used to wind the 50 μH inductors as air-core inductors, so that the peak current drawn by the EUT may not be affected. An HP 4395A spectrum analyzer is used to measure the phase and neutral voltages, V_P and V_N (henceforth referred to as conducted phase and neutral emissions). The voltages V_P and V_N are, in essence, high voltage spikes (sometimes exceeding 400 V) of submicrosecond duration. These signals are attenuated at the input of the spectrum analyzer to protect the receiver stage of the instrument. The resolution bandwidth (RBW) of the instrument is set to 10 kHz which is above the minimum requirement of 9 kHz specified by the ANSI standard.

3.4.4 Stray inductance

An accurate estimate of the stray inductance of the commutation circuit is very helpful in determining the snubber components for overvoltage reduction. Applying Faraday's law of induction results in a simple method of measuring L_σ directly from the switching transients. Although it is a well known fact, it is seldomly used for measurements. However, it proves useful and very accurate as a measuring method.

The idealized switching waveforms of a power MOSFET during the turn-off transient are shown in Fig. 2.2. As discussed in Chapter 2, the presence of stray inductance causes an overvoltage to appear across the transistor terminals. From Eq. 2.1

$$v_{DS} = V_d - L_\sigma \frac{di}{dt}$$

Rearranging yields:

$$L_\sigma = \frac{1}{I_0} \int_{t_1}^{t_2} (V_d - v_{DS}(t))\, \mathrm{dt} \tag{3.2}$$

where t_1–t_2 corresponds to the current fall interval (Please refer to Fig. 2.2).

Thus the time integral of the overvoltage divided by the magnitude of the switched current gives a measure of the stray inductance. For the test circuit employing a MOS-

FET, the integration is performed over the entire current fall time, whereas with an IGBT, where a distinct current tail is present, the time limits are chosen corresponding to the linear fall of collector current. Measurements under different load conditions gave a mean value of L_σ of 556 nH for the 5-A commutation circuit and 575 nH for the 15-A circuit. The overvoltage values obtained with snubbers designed using the aforementioned values of L_σ agree well with the predicted values. This method can be easily extended to paralleled modules in high power bridge configurations as described in [42].

3.5 Conclusions

This chapter has provided a description of the fundamental framework for the experimental work and results to be presented in the following chapters. The CGD presented in Section 3.2.2 also forms the main stage of the two-stage gate driver to be discussed in Chapter 4. This CGD can effectively reduce transients at the expense of increased losses, and its performance is detailed in Appendix B. The switching test circuit discussed in this chapter introduces the external influences present during the inductive-load switching. This circuit has the merits of a low component-count and a single power switch control, making it ideal for the study of switching behavior. The techniques presented for measurement of switching loss and stray inductance are straightforward to implement, yield reliable and accurate results, and eliminate the need for expensive instrumentation (an integrating-type oscilloscope for switching loss) or inexact estimation (for stray inductance).

CHAPTER 4

TWO-STAGE GATE DRIVER: IMPLEMENTATION

4.1 Introduction

As discussed in Appendix B, the main problem with the CGD method of reducing transients is the fact that the slopes of both voltage and current are determined by the gate resistors. An improvement would be a gate driver that provides an independent control of the slopes, and forms the underlying principle of the so-called two-stage gate drive scheme. Over the past decade several gate drivers based on this principle have been proposed and are briefly described in Section 2.4.2.

The various driver schemes proposed differ in their implementation, the derivation of control signals and the portion of the switching transition being controlled. Moreover, for the description of the driver performance, the choice of attributes has neither been consistent nor all-inclusive. In light of this, a simple driver circuit is introduced in this chapter which can be used to characterize the two-stage gate drive scheme. Also, a novel two-stage gate driver is described which effectively reduces the peak transient values and conducted noise without excessively increasing switching losses or switching times.

4.2 Characterization of the two-stage driver scheme

4.2.1 Circuit

Fig. 4.1 shows the schematic of the circuit used for characterizing the two-stage driver scheme. Stage-1 of the driver is basically a CGD as described in Chapter 3. The voltage and current slopes can be controlled independently by triggering Stage-2 of the driver at an appropriate time instant. This effectively results in changing the driver output impedance during the switching transition hence affecting the rate at which the charge is being supplied to or removed from the gate capacitance. The control

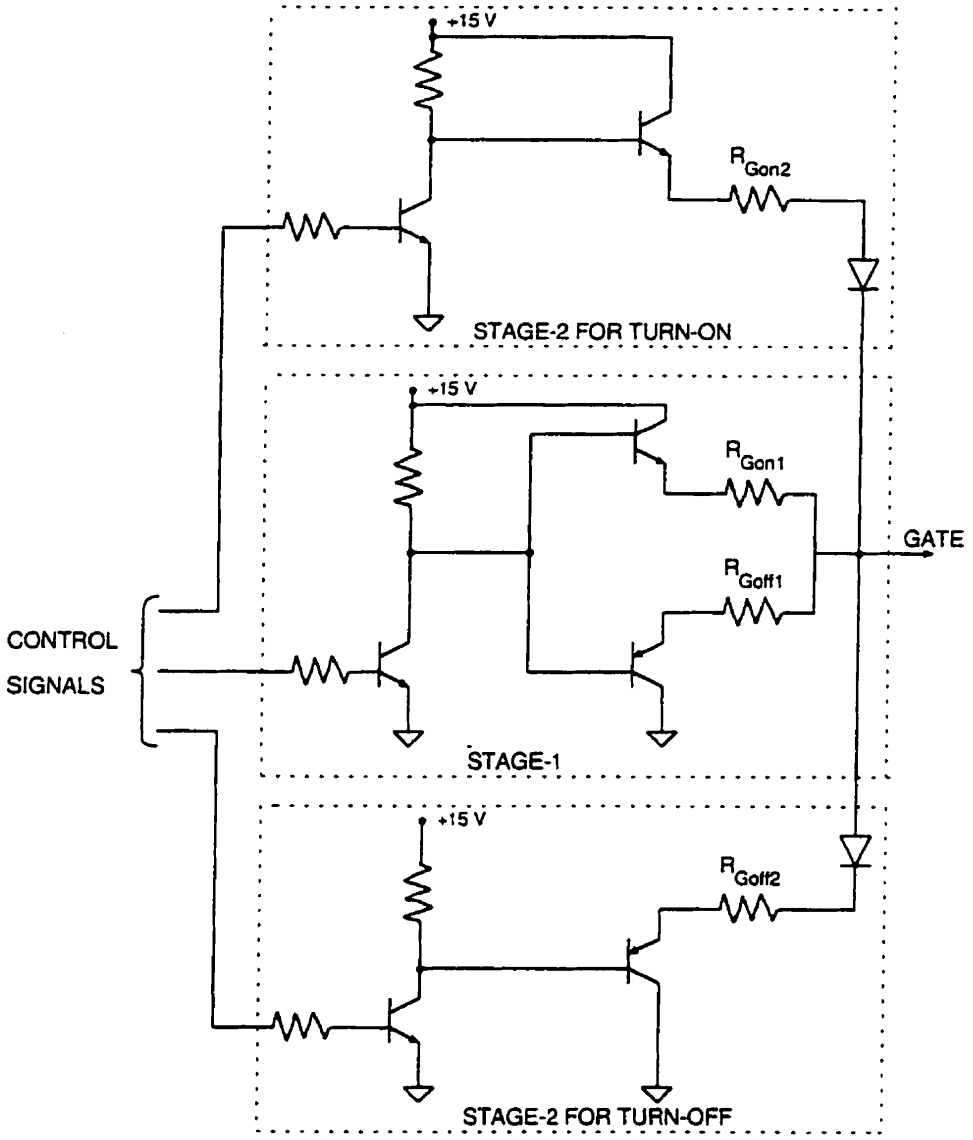

Figure 4.1. Schematic of the circuit used for characterization of the two-stage driver scheme.

signals for this circuit are obtained using LabWindows/CVI. Two PWM signals are generated using software — one driving the main stage of the driver and the other providing control for either turn-on or turn-off. The control signals thus generated have a timing resolution of 50 ns. A finer resolution is obtained by varying the overdrive factor of the driver transistors.

The diodes in Fig. 4.1 protect the output transistors in the Stage-2 of the driver. For instance, as will be shortly discussed, during turn-off the pnp output transistor of Stage-2 needs to be turned off after a short time interval. In absence of the diode this will cause the emitter and base voltages to approach -5 V and +15 V, respectively. This condition requires a signal transistor with a base-emitter breakdown voltage greater than 20 V which is well above the rating of the available devices (7 V for 2N4403). Placing a diode as shown prevents the imminent breakdown of the emitter junction. 11DQ06 Schottky diodes are used for this purpose so that reverse recovery does not have any effect on the operation of the driver.

It should be noted here that the control signals are isolated from the driver by means of optocouplers. Despite this isolation, it is found that at some current levels enough noise is induced on the incoming signal lines to cause improper switching. This problem is solved by placing small filter capacitors at the input of the optocouplers.

4.2.2 Timing Control

4.2.2.1 Turn-on

As explained in Appendix A, the turn-on transition consists of current growth in the power transistor followed by the voltage transfer to the diode. The rate of current growth is kept low by charging the gate capacitance through a large resistor R_{Gon1}. After the freewheeling diode has recovered, a sharp fall in drain voltage is attained by a quick chargeup through the small driver impedance $R_{Gon1} || R_{Gon2}$, where $R_{Gon2} << R_{Gon1}$. The PWM signals and the resulting driver voltages for achieving this control are shown in Fig. 4.2. The drive signal for Stage-2 of the driver is obtained by triggering from the negative edge of the PWM input to the main stage and then inverting the resulting signal. The delay time as well as the switching frequency and the duty ratio can be easily controlled from the *Graphical User Interface* (GUI) created in LabWindows/CVI.

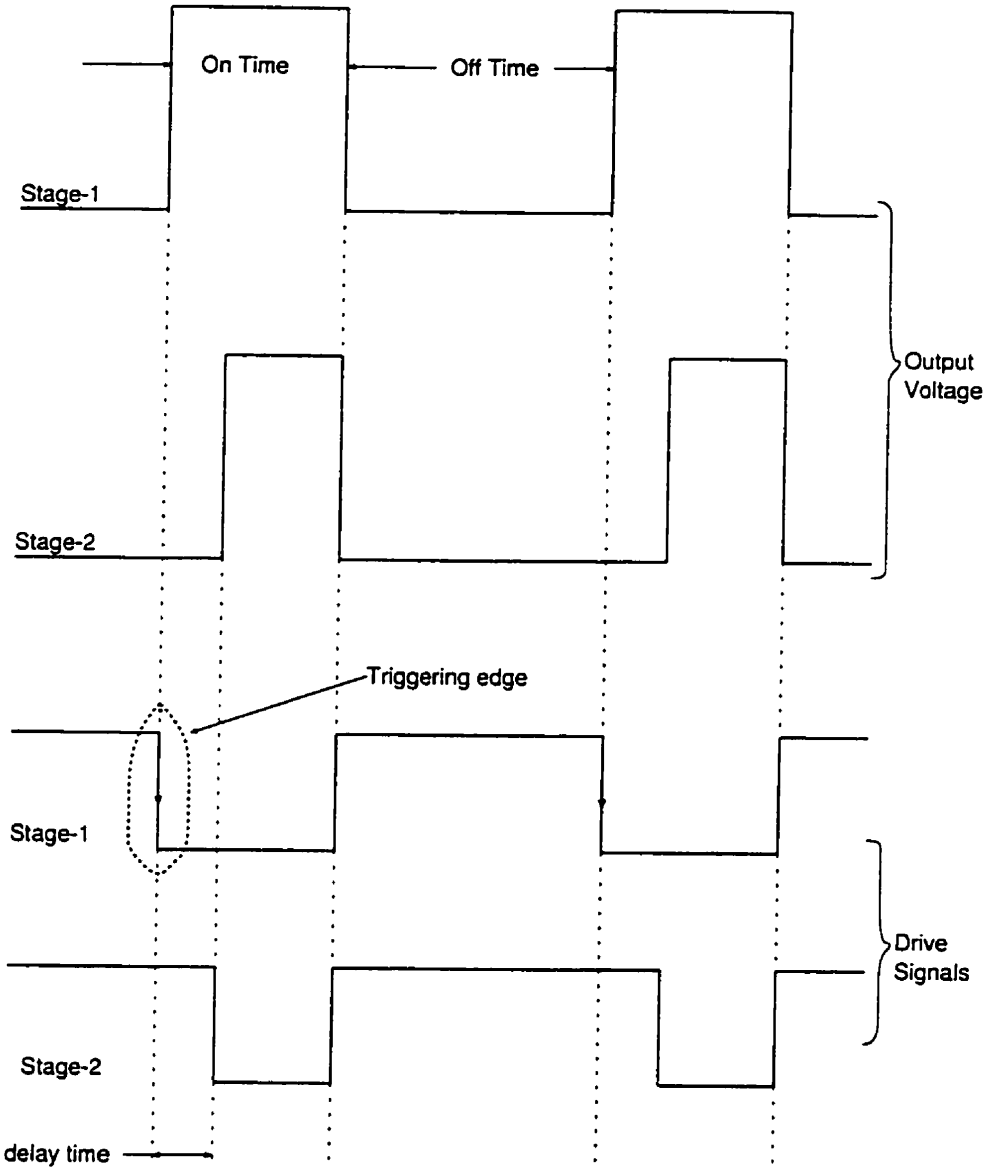

Figure 4.2. Drive signal waveforms for two-stage turn on control.

4.2.2.2 Turn off

During the initial phase of turn-off the gate capacitance needs to be discharged rapidly for short turn-off delay and voltage rise times. This is achieved by turning on both Stage-1 and Stage-2 at the same time thus providing a low impedance path for gate discharge ($R_{Goff1} \| R_{Goff2}$, where $R_{Goff2} << R_{Goff1}$). Stage-2 of the driver is

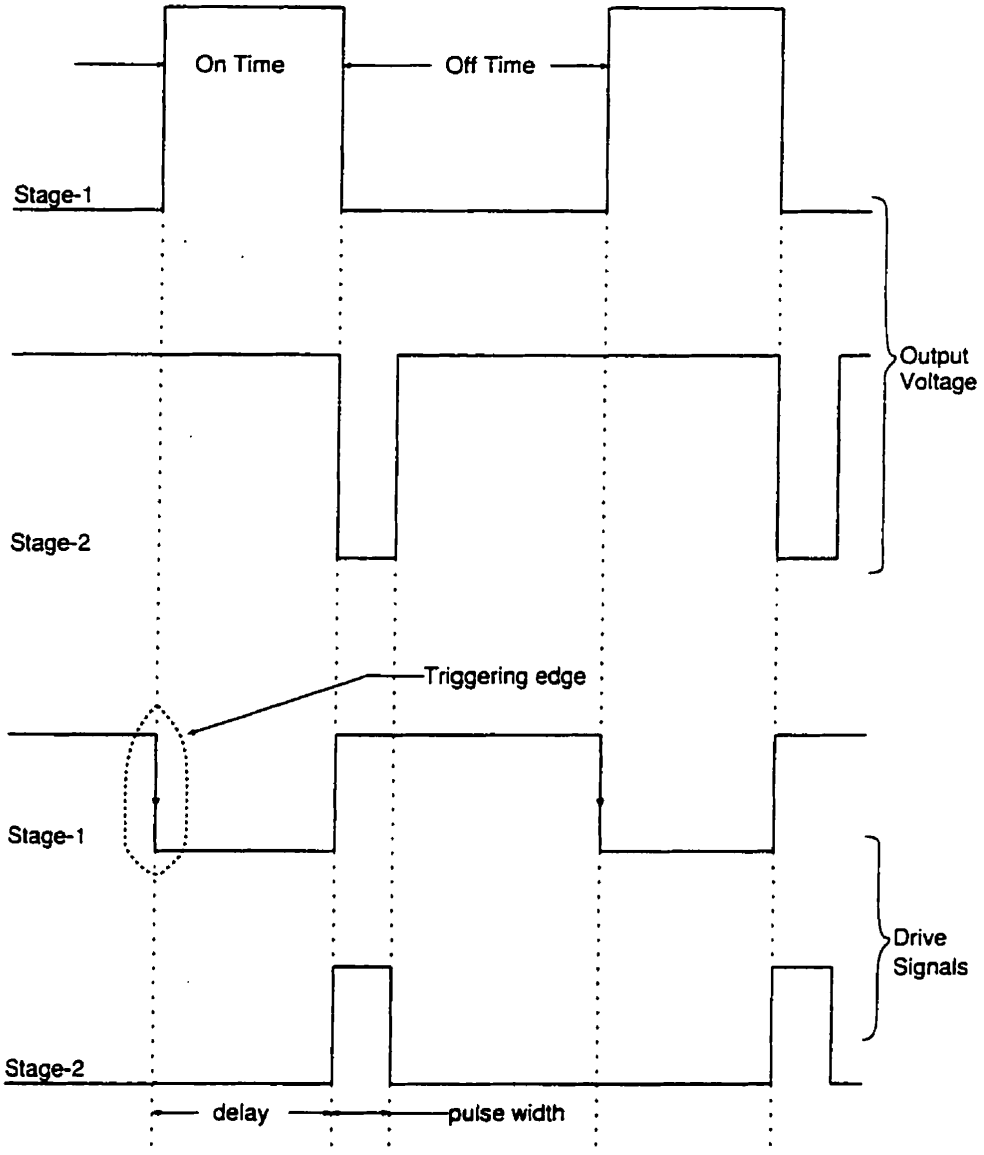

Figure 4.3. Drive signal waveforms for two-stage turn off control.

turned off when the drain voltage has risen to the dc link voltage value. This action increases the driver output impedance to R_{Goff1}, hence reducing the rate of current fall. Fig. 4.3 shows the the drive signal waveforms for the two-stage turn off control. As for turn-on scheme, the control signal for Stage-2 is derived by triggering from the main PWM input and pulse width can be controlled "on-the-fly" from the GUI.

4.3 Novel two-stage driver circuit

A novel scheme for generation of control signals for a two-stage driver is described in this section. This scheme is based on the detection of v_{GS} instead of v_{DS} or dv/dt or di/dt which form the control parameters for most other schemes discussed in Section 2.4.2. The reason for this choice is twofold. First, during a switching transition the first variable to undergo any change is the gate voltage. A technique based on the detection of v_{GS} thus has the advantage of more time being available for the driver components to change state and hence can be used at high switching speeds. Second, the scheme does not require high-voltage components as required for schemes based on v_{DS} or dv/dt detection. Moreover there is no longer a dependence on the module internal inductance L_e (used for di/dt based schemes), which may be poorly specified or be inaccessible for three terminal packages.

The basic idea behind the scheme is to trigger the second stage of the driver when the gate voltage crosses some reference value (found by trial and error). The individual components of the turn-on and turn-off schemes are now briefly discussed.

4.3.1 Turn-on

As discussed in Section 4.2.2.1, the second stage of driver needs to be triggered by some time delay after the main stage for minimizing the switching loss. The control signal for Stage-2 is obtained by using a comparator and an OR gate as shown in Fig. 4.4 which also shows the truth table for the arrangement. The two inputs to the comparator are the gate-source voltage v_{GS} and a reference voltage $V_{REF(on)} > 0$ V. When the turn-on command is applied to the transistor, the gate voltage begins to rise from its negative rail value (say -5 V). As long as $v_{GS} < V_{REF(on)}$, the Stage-2 remains inactive and the drain current rises slowly. When the gate voltage exceeds the reference value, Stage-2 is triggered and the drain voltage falls rapidly. At turn-off the presence of the OR gate prevents the short-circuit of the positive and negative

rails through the power transistor gate.

Fig. 4.5 shows the circuit for Stage-2 of the driver for turn-on control. The driver main stage is the same as in Fig. 4.1. As the initial phase of the turn-on transition needs to be kept relatively slow, a medium speed comparator LM111 (response time $\approx$ 200 ns) proved quite adequate for our purpose. The optocoupler is required to prevent the contamination of the input PWM signal. In the absence of this isolation, the entire circuit "bursts" into oscillations beyond a particular drain current level.

4.3.2 Turn-off

The operation of the turn-off driver discussed here differs from the scheme in Section 4.2.2.2 in one important respect. The second stage of the driver after being turned off for some time is turned on again for the remainder of the off time of the power transistor. This action ensures that the gate is turned off via a small driver impedance and prevents against dv/dt induced turn-on. The basic scheme for turn-off control and the driver signal waveforms are shown in Fig. 4.6. The turn-off transient begins with the simultaneous turn-on of Stage-1 and Stage-2 and a rapid discharge of the gate capacitance. The Stage-2 is turned off for a short time interval at the onset of current fall thus forcing the gate discharge through the high-ohmic Stage-1 gate resistance. This is achieved by detecting the fall of gate voltage below some reference value $V_{REF(off)}$. After the interval set by the monostable, Stage-2 is again turned on to guarantee low-ohmic turned-off status of the transistor.

Fig. 4.7 shows the driver circuit which achieves the above discussed control at turn-off. It may be noted here that the initial time interval for which Stage-2 is on can be fairly small ($\approx$100 ns). This implies that in order for the driver to change states within the aforementioned time, the individual components must be quite fast. Hence a LM710 comparator with 40 ns response time, and a monostable and a XOR gate with propagation delay times of 25 ns and 10 ns, respectively are chosen for

implementing this scheme. A couple of other points are worth mentioning here. The resistor divider network formed by the 3 kΩ and 9.1 kΩ resistors reduces the v_{GS} voltage by a factor of four before being applied to the comparator. This is done so as not to exceed the voltage rating of the LM710 (Input voltage range = ±5 V, Differential input voltage range = ±5 V). The HC logic family has a typical high-level input voltage requirement of $0.7V_{cc}$. The 4-V V_{cc} value was chosen to accomodate the 2.9 V(typical) output of the LM710.

As for the turn-on scheme, an HCPL-2200 optocoupler prevents noise "corruption" of the input signal line.

4.4 Conclusions

A simple method for characterizing the two-stage gate drive scheme has been discussed in this chapter. For the purpose of experimental investigation, this method makes use of the LabWindows/CVI software which offers the advantages of ease of programming and a graphical interface for the control of drive signals. Also, a new gate drive circuit based on gate-source voltage detection has been presented. The circuit achieves control of the switching transitions by modifying the driver impedance at appropriate time instants. The proposed circuit has a part-count less than many schemes presented in the literature and does not require any high-voltage components. The turn-on scheme as implemented has the disadvantage of a rather long delay time. This, however, can be easily rectified by the addition of a monostable as in the turn-off scheme.

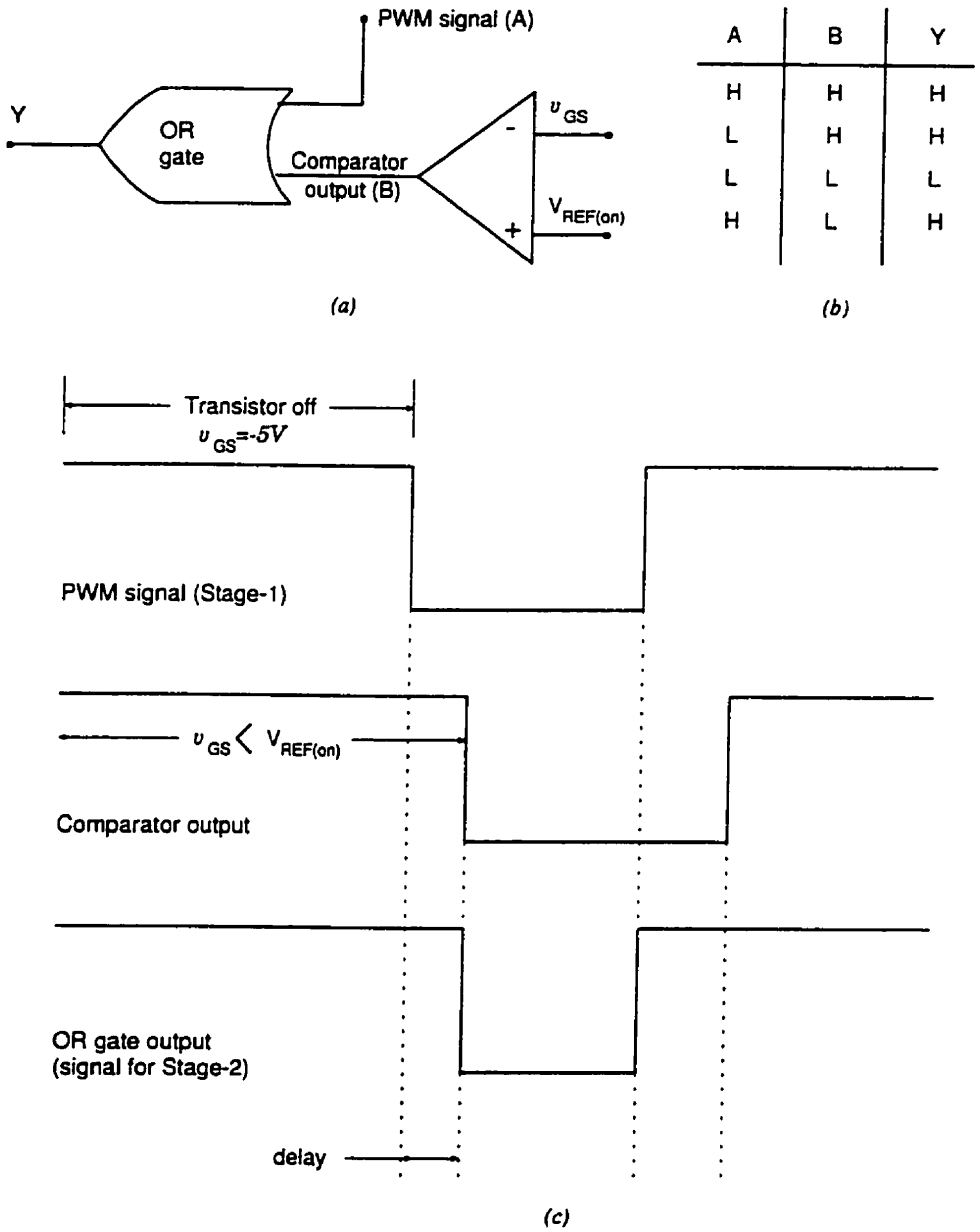

Figure 4.4. Proposed turn-on control scheme. (a) Circuitry for v_{GS} detection and generation of control signals. (b) Truth table for the arrangement shown in (a). (c) Drive signal waveforms at turn-on for the two-stage gate driver.

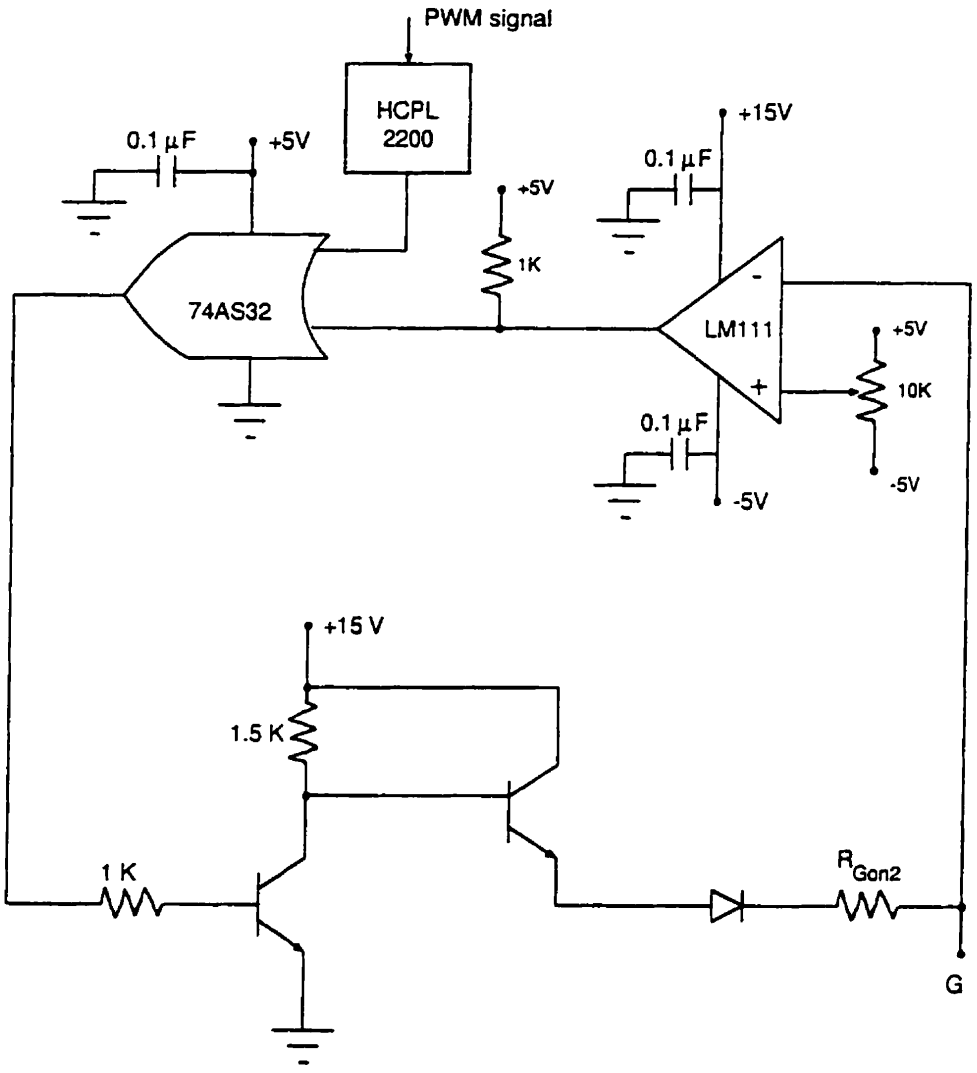

Figure 4.5. Schematic of the proposed second stage of driver for turn-on control.

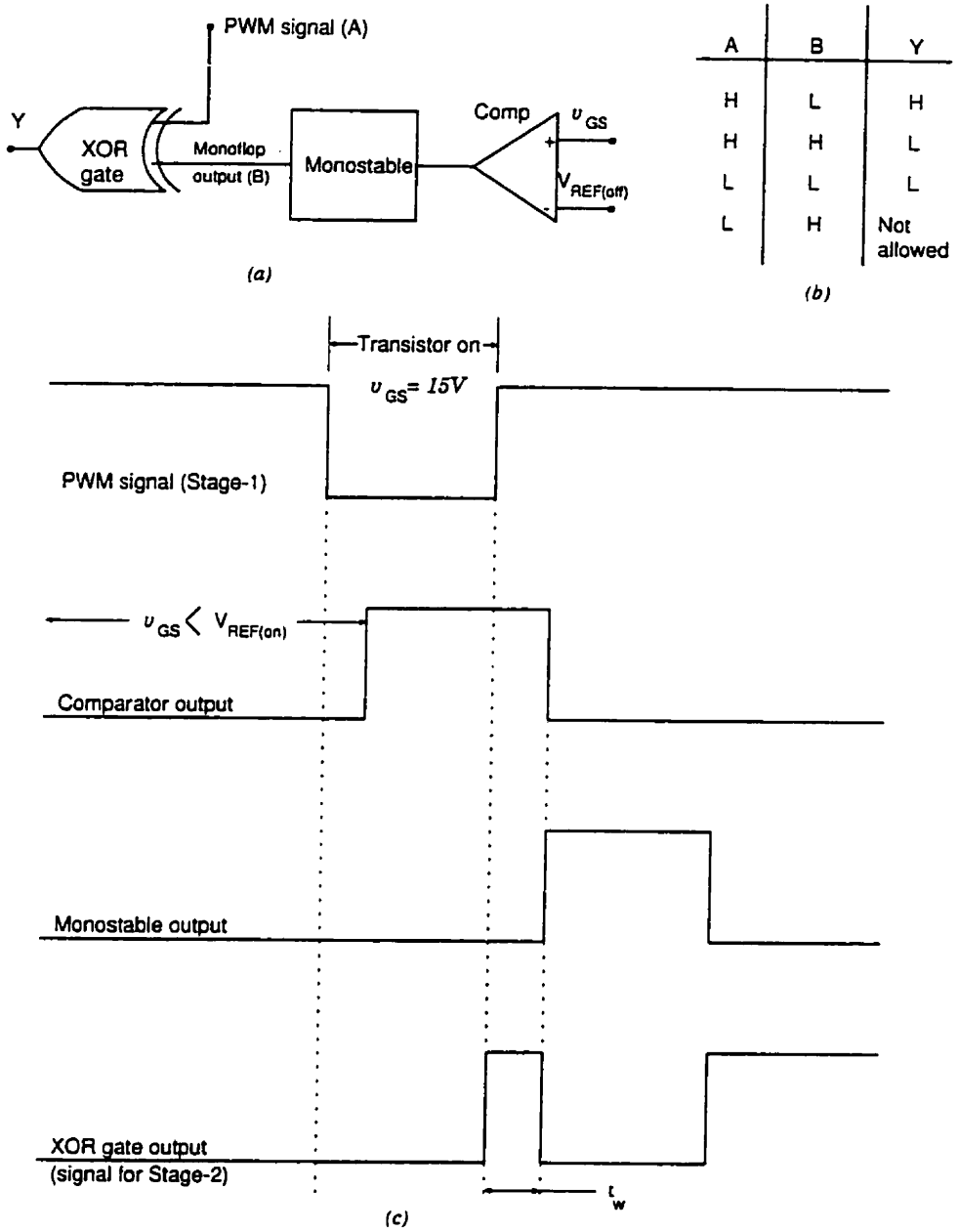

Figure 4.6. Proposed turn-off control scheme. (a) Circuitry for v_{GS} detection and generation of control signals. (b) Truth table for the arrangement shown in (a). (c) Drive signal waveforms at turn-off for the two-stage gate driver.

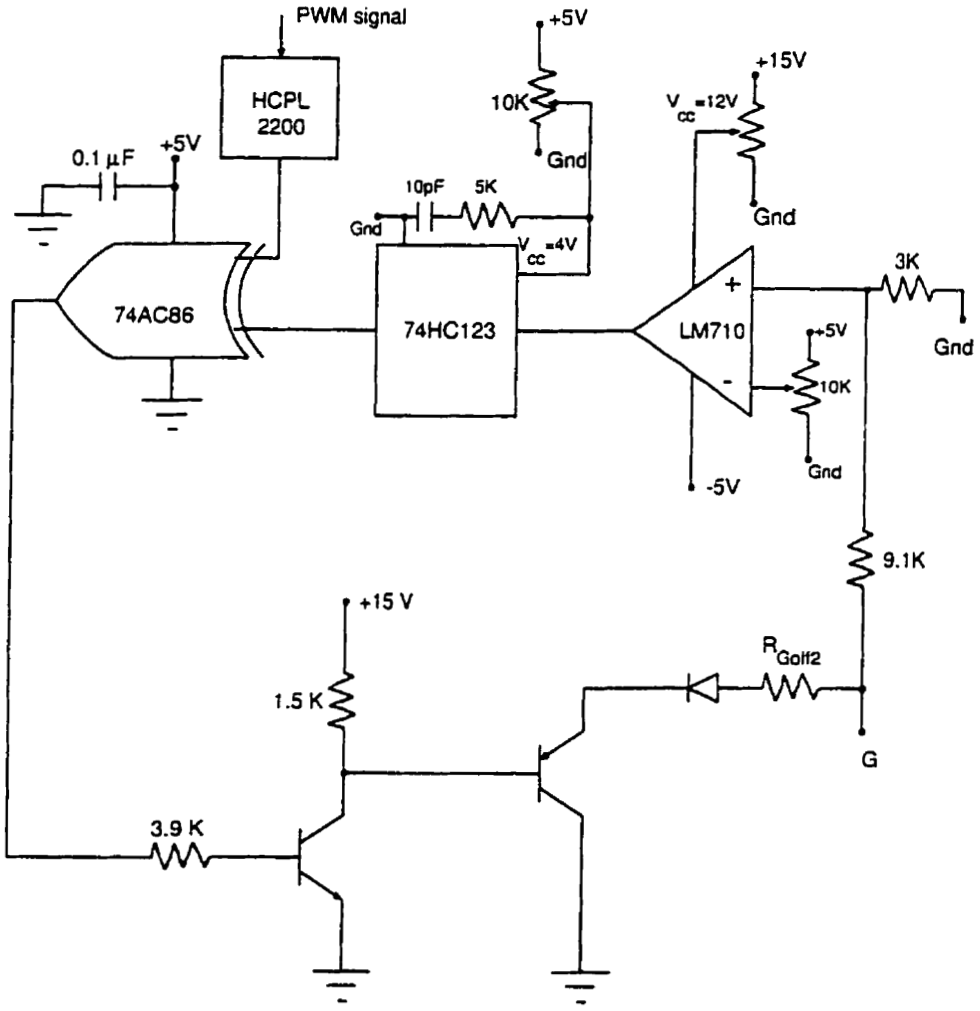

Figure 4.7. Schematic of the proposed second stage of driver for turn-off control.

CHAPTER 5

TWO-STAGE GATE DRIVER: EXPERIMENTAL RESULTS

5.1 Introduction

The performance of the two-stage gate driver scheme is the subject of discussion of this chapter. The characterization technique discussed in the previous chapter is used to study the switching performance of a power MOSFET under different driving conditions. The novel two-stage driver presented in Section 4.3 is tested on an IGBT embedded in a step-down dc-dc converter. For both power MOSFET and IGBT, the driver performance is compared to the conventional means of transient reduction, viz. increasing the gate resistance and the use of snubbers. The characterization is done on the basis of peak values of transients (overvoltage and reverse recovery current), switching losses, delay times and conducted emissions.

5.2 Experimental Results

5.2.1 Switching performance

Figs. 5.1–5.4 show the switching waveforms of the power MOSFET and the IGBT under different switching conditions. It can be readily seen that using low ohmic gate resistors with a CGD results in fast switching times and low switching losses, but also produces high values of reverse recovery current and voltage overshoots. The peak values of transients and the associated electromagnetic noise is reduced by switching with high ohmic gate resistors at the expense of slow switching and high switching loss. Figs. 5.1–5.4 demonstrate that switching with the the two-stage gate driver produces peak values of transients comparable to those obtained with the CGD (slow switching) without excessively increasing the switching loss.

From Figs. 5.1 and 5.3, turn-on with a low driver impedance results in a peak

transient current that is almost twice the value of the load current. A significant amount of ringing is accompanied by the fast switching transition, hence increasing the EMI generated by the power converter. Reducing di/dt with a CGD increases the voltage fall time and also introduces a voltage tail that is quite prominent in the case of the MOSFET. Turn-on with the two-stage gate driver attains a low value of I_{rr} with a low di/dt while optimizing the switching loss by reducing the voltage fall time. The results for switching performance at turn-on are summarized in Tables 5.1 and 5.3. As expected, the switching loss with the two-stage driver is somewhere between the values with CGD-fast and CGD-slow switching. For values of I_{rr} slightly higher than obtained with a CGD (slow switching), the savings in turn-on switching loss are 25% for the power MOSFET and 11.8% for the IGBT. The minimum switching loss is obtained with a turn-on snubber, as almost all of the dc link voltage is dropped across the snubber inductance during the current rise time. As was noted in Chapter 4, the current implementation of the two-stage driver scheme does not offer an improvement in turn-on delay time. Using a small gate resistance at the beginning of the turn-on transition will solve this problem and also offer a further reduction in the turn-on switching loss.

Figs. 5.2 and 5.4 respectively show the turn-off switching waveforms for the MOSFET and the IGBT under different driving conditions. A rapid turn-off of the power transistor with a CGD yields an overvoltage that is roughly 0.9 times the dc link voltage for MOSFET and 1.6 times for IGBT. It is interesting to note here that for identical circuit layout and similar switching speeds, the ringing is significantly lower in the case of the IGBT. Switching with a large value of gate resistance increases the voltage rise time considerably and hence also the switching loss. Turn-off with the two-stage driver reduces the switching speed only during the current fall-time. This results in turn-off delay and voltage rise times essentially of fast switching with a CGD, and a low voltage overshoot at the expense of slightly increased switching loss.

Figs. 5.2 and 5.4 also show the waveforms with an overvoltage snubber, where some ringing is seen to be present due to the resonant circuit formed by the snubber capacitor and parasitic inductance. The switching performance at turn-off is quantitatively represented in Tables 5.2 and 5.4. It can be seen that for a comparable overvoltage reduction, the two-stage driver offers a savings of 29.8% for the MOSFET, and 28.8% for the IGBT in turn-off switching loss compared to the conventional means of increasing the gate resistance. Also significant is the reduction in turn-off delay times compared to a slow CGD.

A note on snubbers: The turn-on and overvoltage snubbers are designed based on the theoretical considerations laid out in Section 2.4.1. Polypropylene capacitors are used for the overvoltage snubbers because of their low dielectric loss, high dv/dt capability and excellent frequency characteristics [43, 44].

The measurement results agree well with the predicted performance except in the case of the turn-on snubber for the 15-A test circuit, where the final value of L_s used (1.4μH) is considerably less than obtained from Eqs. 2.2 and 2.6 (3.0μH). This is because the discussion in Sec. 2.4.1 is based on the assumption of linear rise of current, whereas for large gate resistances the rise of current follows almost a square relationship. As a result, the di/dt near the end of current commutation is significantly higher than the average rate of rise, and a snubber inductance based on the latter value gives I_{rr} lower than the expected value.

Table 5.1. Switching performance of MOSFET under different driving conditions at turn-on.

Switching Condition	Turn-on Switching Loss (μJ)	Reverse Recovery Current (A)	Turn-on Delay Time (ns)
CGD-slow, R_{Gon}=200Ω	76	1.93	194
CGD-fast, R_{Gon}=2Ω	15	5.56	46
Two-Stage Driver $R_{Gon1} = 200\Omega, R_{Gon2} = 2\Omega$	57	2.94	182
Turn-on Snubber $R_{Gon} = 2\Omega$ $R_{Ls} = 5.1\Omega, L_s = 4.1\mu$H	0.35	1.70	62

Table 5.2. Switching performance of MOSFET under different driving conditions at turn-off.

Switching Condition	Turn-off Switching Loss (μJ)	Overvoltage (V)	Turn-off Delay Time (ns)
CGD-slow, R_{Goff}=100Ω	87	24	970
CGD-fast, R_{Goff}=15Ω	28	90	162
Two-Stage Driver $R_{Goff1} = 100\Omega, R_{Goff2} = 15\Omega$	61	28	164
Overvoltage Snubber $R_{Goff} = 15\Omega$ $R_{ov} = 200\Omega, C_{ov} = 22$nF	57	22	164

Table 5.3. Switching performance of IGBT under different driving conditions at turn-on.

Switching Condition	Turn-on Switching Loss (mJ)	Reverse Recovery Current (A)	Turn-on Delay Time (ns)
CGD-slow, R_{Gon}=100Ω	0.289	4.8	616
CGD-fast, R_{Gon}=2Ω	0.041	13.3	68
Two-Stage Driver $R_{Gon1} = 100\Omega, R_{Gon2} = 2\Omega$	0.255	6.5	603
Turn-on Snubber $R_{Gon} = 2\Omega$ $R_{Ls} = 2.7\Omega, L_s = 2\mu$H	0.015	4.4	82

Table 5.4. Switching performance of IGBT under different driving conditions at turn-off.

Switching Condition	Turn-off Switching Loss (mJ)	Overvoltage (V)	Turn-off Delay Time (ns)
CGD-slow, R_{Goff}=270Ω	0.320	50	532
CGD-fast, R_{Goff}=5.1Ω	0.051	163	79
Two-Stage Driver $R_{Goff1} = 270\Omega, R_{Goff2} = 5.1\Omega$	0.228	65	110
Overvoltage Snubber $R_{Goff} = 5.1\Omega$ $R_{ov} = 200\Omega, C_{ov} = 56$nF	0.341	45	70

5.3 Conducted Emissions

The results for conducted emissions are presented in this section with focus on EMI reduction by the two-stage driver compared to fast switching by a CGD. For the 5-A test circuit employing a MOSFET, gate drive signals are generated from LabWindows/CVI which provides two PWM control signals. As a result, the effect of turn-on and turn-off control for the two-stage driver must be studied separately. On the other hand, the novel two-stage driver (tested on the 15-A converter), allows simultaneous control of turn-on and turn-off transitions and, as such, the results are presented for the "combined" two-stage driver.

Although results are shown for both phase and neutral emissions, discussion is provided only for phase emissions as spectra for neutral emissions are almost identical. Also, for the 5-A test circuit employing a MOSFET, most harmonic frequencies display a varying amplitude. Hence for this case the spectrum analyzer is used in the averaging mode and the spectra presented are a result of the average of 50 sweeps.

(a) Test circuit employing MOSFET:

Figs. 5.5 and 5.6 show the conducted emissions for the 5-A converter under different driving conditions at turn-on. For comparison, the turn-off is identical in all the cases with a gate resistor of 100 ohm. Similarly, Figs. 5.7 and 5.8 show emissions under different switching conditions at turn-off with identical turn-on (R_{Gon} = 200 ohm). It can be seen that in both the cases using the two-stage driver reduces conducted noise compared to fast switching operation by the CGD.

For turn-on, the lowest EMI levels are obtained by switching with the turn-on snubber followed by slow turn-on with the CGD. The noise produced by the converter using the two-stage driver is about 5-10 dBμV less than that obtained with a CGD (fast turn-on) over the concerned frequency range.

For turn-off, the highest EMI levels are obtained when the transistor is quickly

turned off with a CGD. The noise levels are, in general, reduced by switching with the two-stage driver. This reduction is most significant in the frequency range of 17-30 MHz, where the noise is reduced by about 3-6 dBμV. Switching with the CGD employing a large gate resistor generates the lowest noise, except at high frequencies (23-30 MHz) where turn-off with the overvoltage snubber gives slightly lower noise.

(b) Test circuit employing IGBT:

The conducted emissions of the 15-A converter with IGBT under different driving conditions are shown in Figs. 5.9–5.16. The gate resistance and snubber component values are as recorded in Tables 5.3 and 5.4. The following observations can be made from a study of the emissions spectra. The highest noise levels over the entire frequency range are obtained for fast switching operation with a CGD. Switching with a large driver impedance generates, in general, the lowest conducted noise, except at some harmonic frequencies where the performance with snubbers is superior. The conducted noise level with the two-stage driver lies between the two extremes of CGD-slow and CGD-fast switching. Switching trajectory control with the proposed driver reduces noise over the entire frequency range of interest (450 kHz-30 MHz) compared to rapid switching with the CGD. Specifically, conducted EMI are reduced by 4-7 dBm over 3-10 MHz, 2-6 dBm over 10-25 MHz and about 1 dBm for frequencies greater than 25 MHz or less than 3 MHz.

5.4 Conclusions

The performance of the two-stage driver scheme has been described in this chapter. The driver technique has been completely characterized for a hard switching application of both power MOSFET and IGBT. It was shown that the driver realizes an effective reduction in reverse recovery current at turn-on and overvoltage at turn-off thus reducing the switching stress and EMI problem. The switching losses and switching times with the two-stage driver are lower than that of a CGD operating at the same peak device stress levels. The scheme inherently generates high dv/dt levels for minimizing the switching loss. For applications where very high dv/dt may be a concern (e.g. motor drives with long cable runs), external means may be employed for attenuating the associated effects.

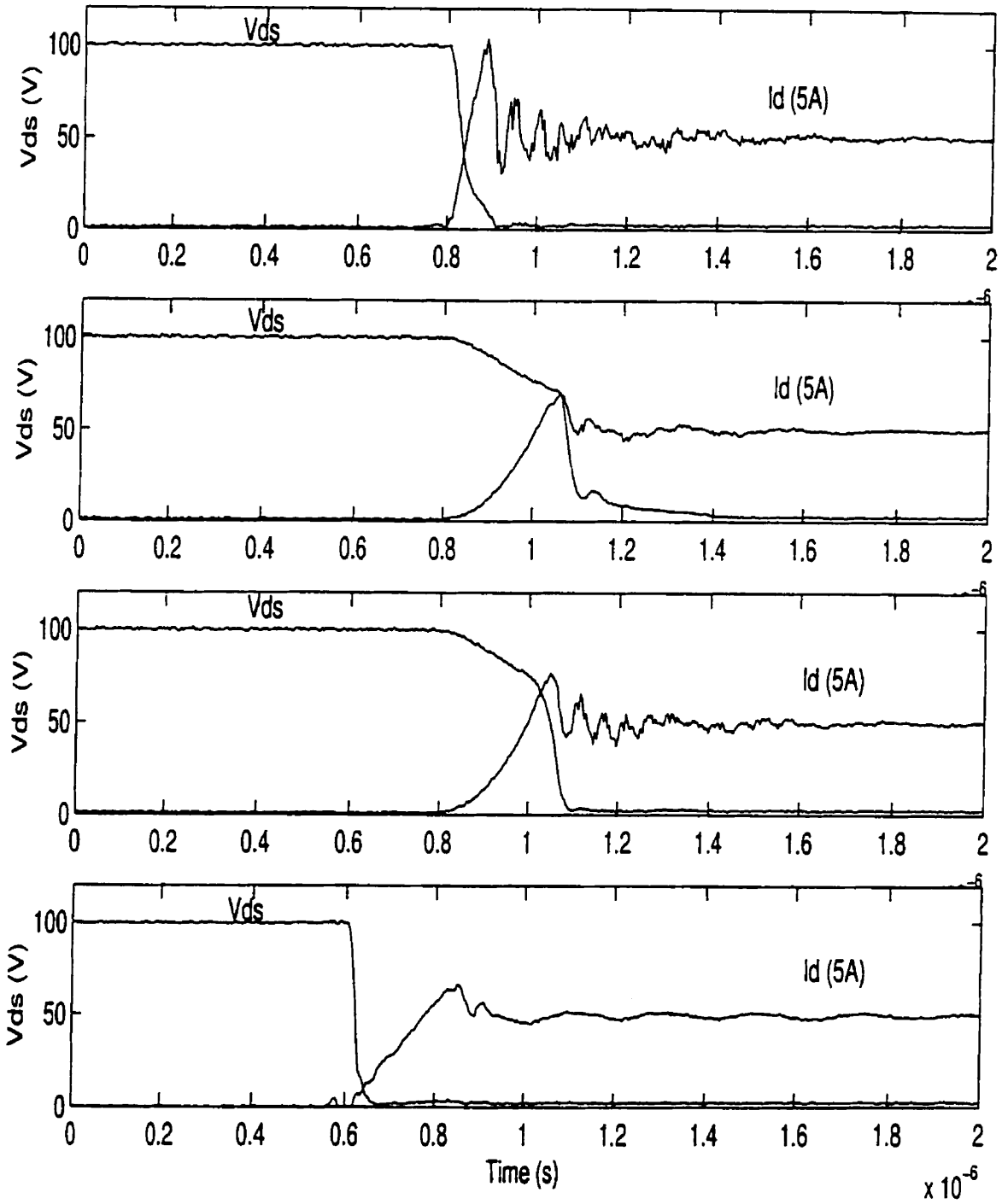

Figure 5.1. MOSFET turn-on waveforms. From top to bottom:(1) CGD turn-on: $R_{Gon} = 2\Omega$ (2) CGD Turn-on: $R_{Gon} = 200\Omega$ (3) Turn-on with two-stage gate driver (4) Turn-on with $R_{Gon} = 2\Omega$ and turn-on snubber

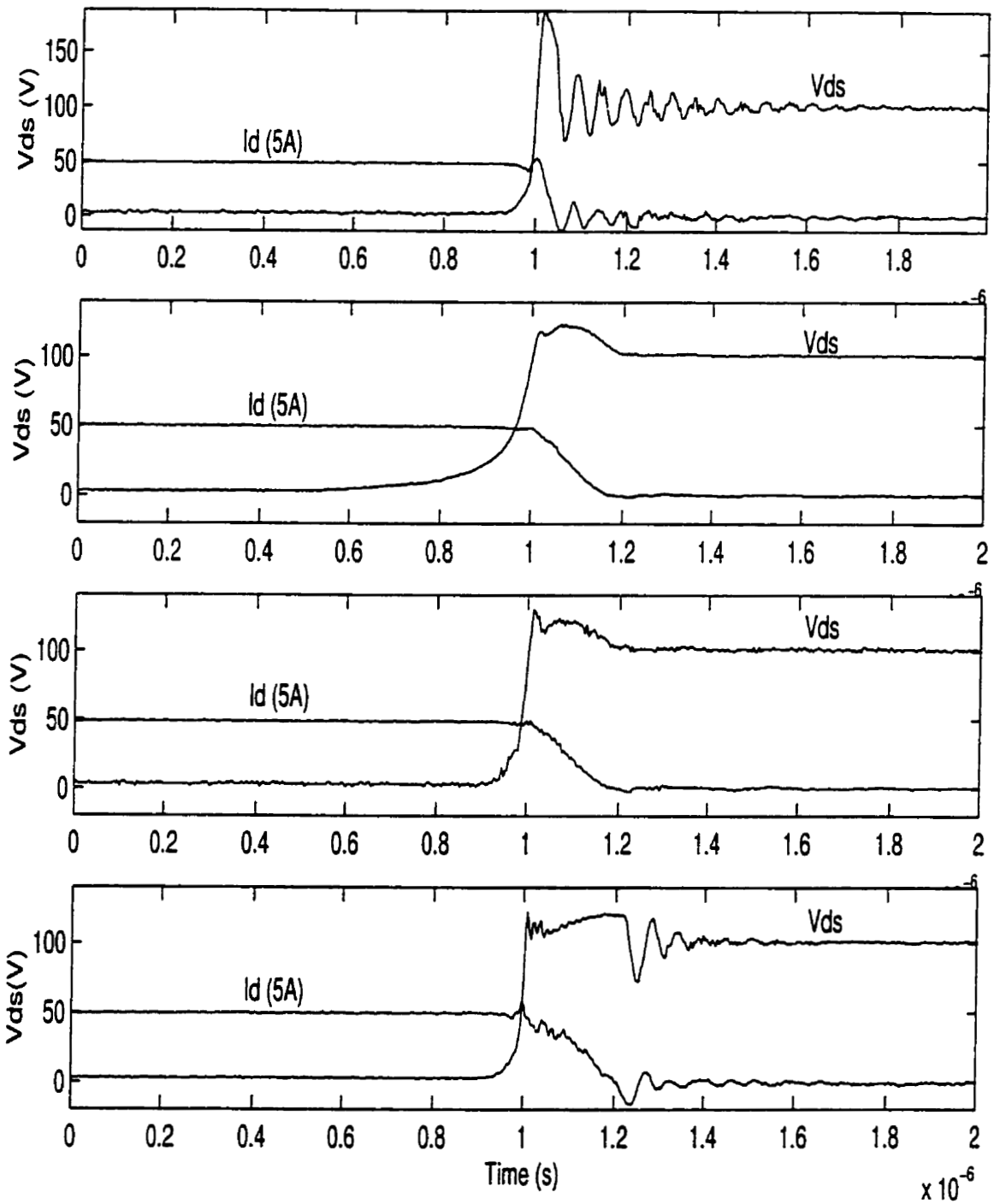

Figure 5.2. MOSFET turn-off waveforms. From top to bottom: (1)CGD turn-off: $R_{Goff} = 15\Omega$ (2) CGD turn-off: $R_{Goff} = 100\Omega$ (3) Turn-off with two-stage driver (4) Turn-off with $R_{Goff} = 15\Omega$ and overvoltage snubber

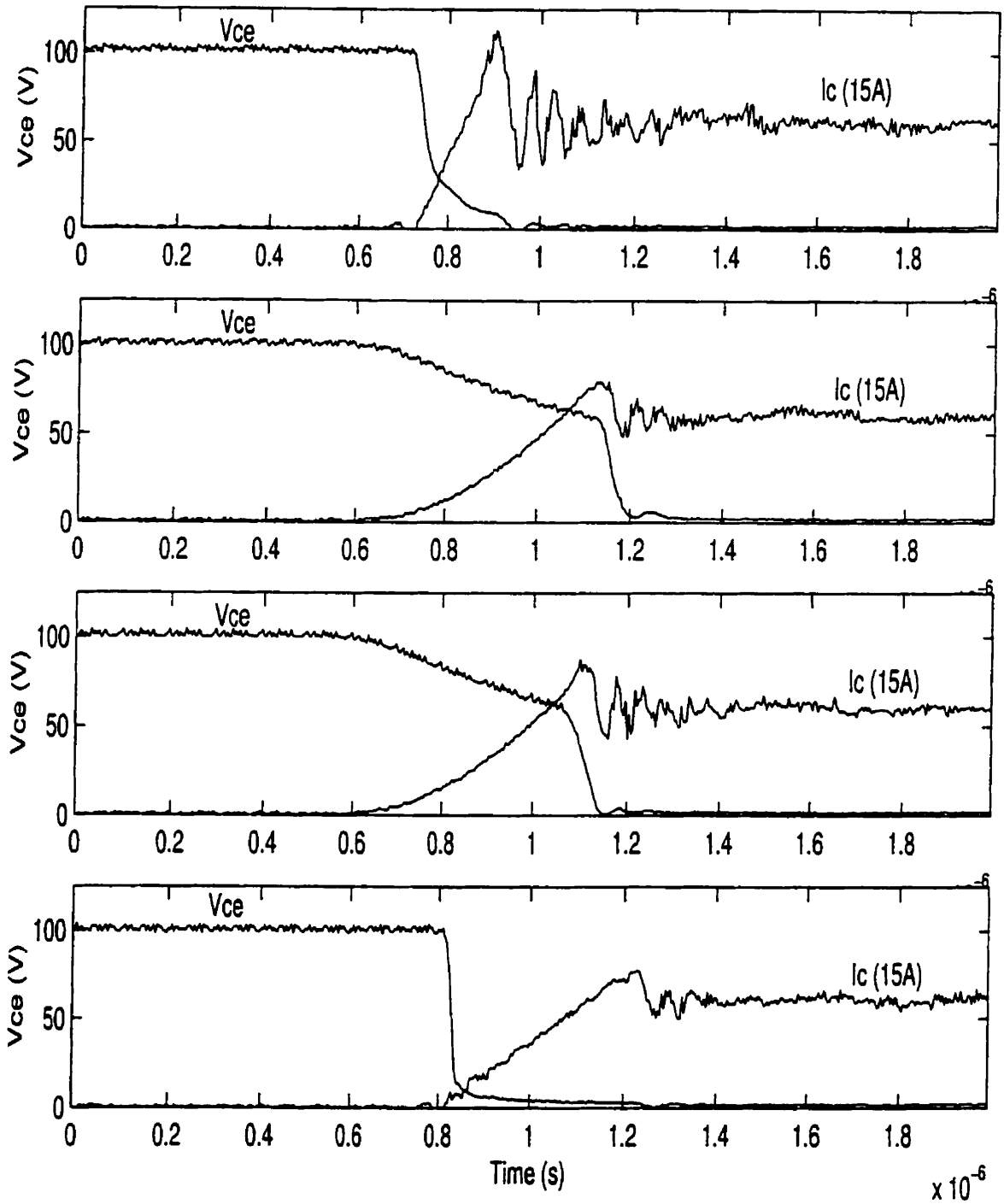

Figure 5.3. IGBT Turn-on waveforms. From top to bottom:(1) CGD turn-on: $R_{Gon} = 2\Omega$ (2) CGD Turn-on: $R_{Gon} = 100\Omega$ (3) Turn-on with the proposed two-stage gate driver (4) Turn-on with $R_{Gon} = 2\Omega$ and turn-on snubber

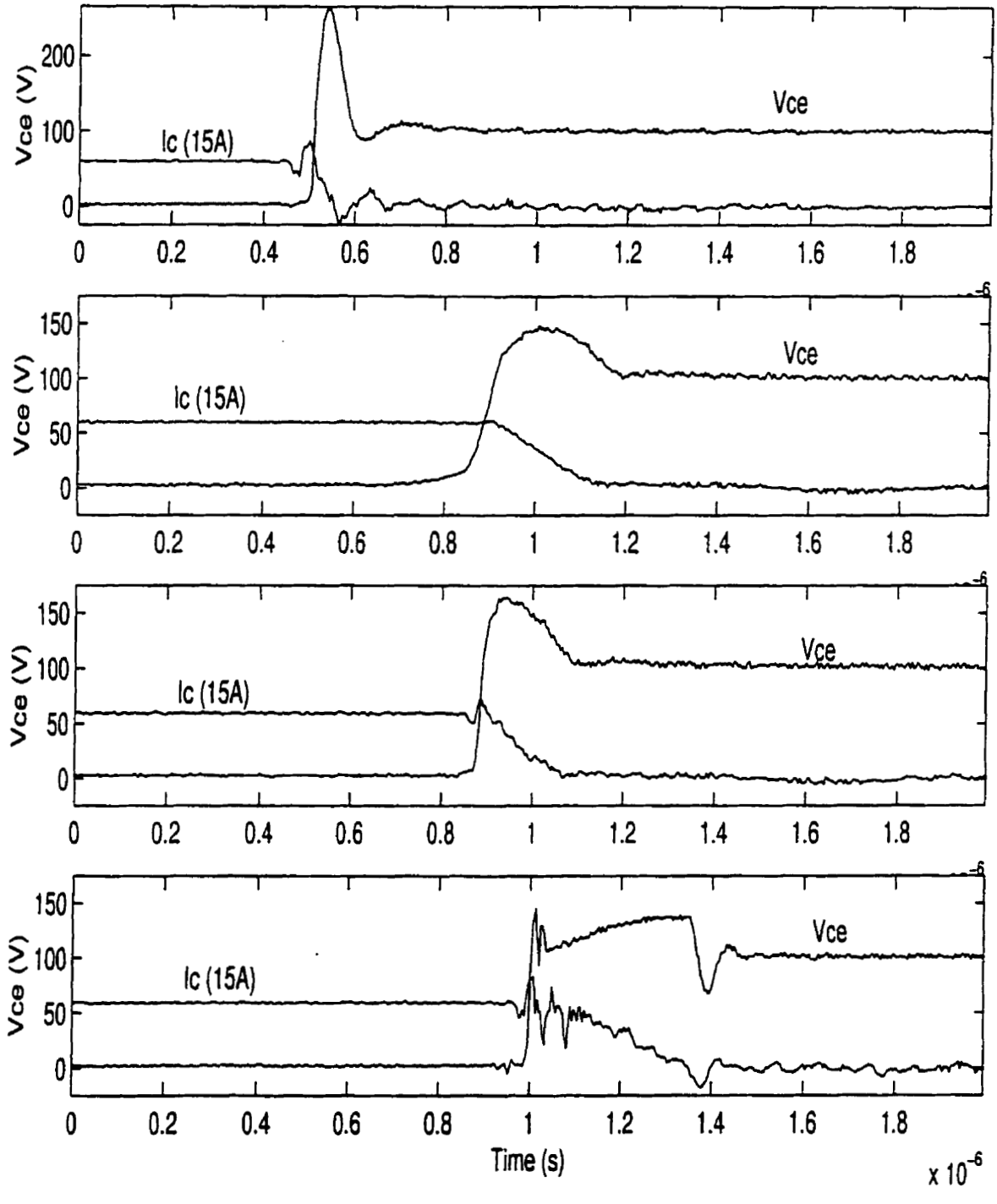

Figure 5.4. IGBT turn-off waveforms. From top to bottom: (1)CGD turn-off: $R_{Goff} = 5.1\Omega$ (2) CGD turn-off: $R_{Goff} = 270\Omega$ (3) Turn-off with the proposed two-stage gate driver (4) Turn-off with $R_{Goff} = 5.1\Omega$ and overvoltage snubber

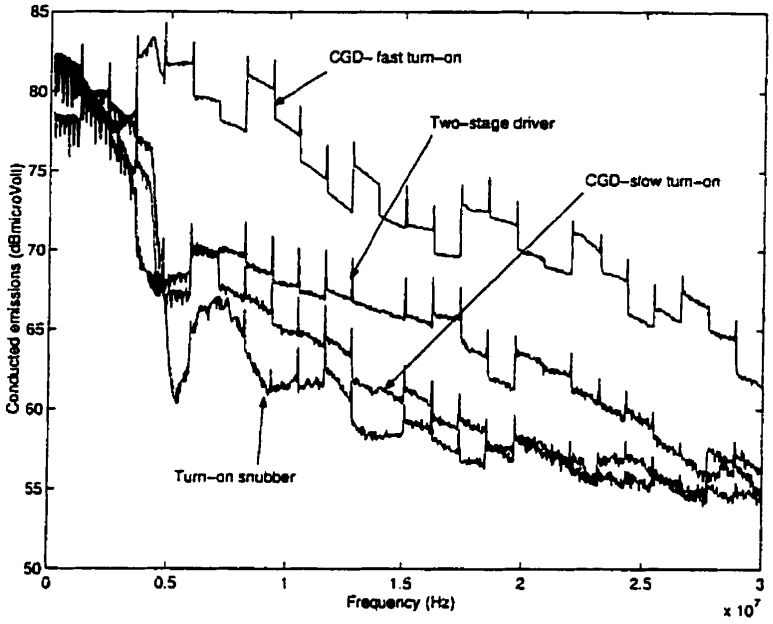

Figure 5.5. Conducted phase emissions of the 5-A converter for different switching conditions at turn-on and identical turn-off.

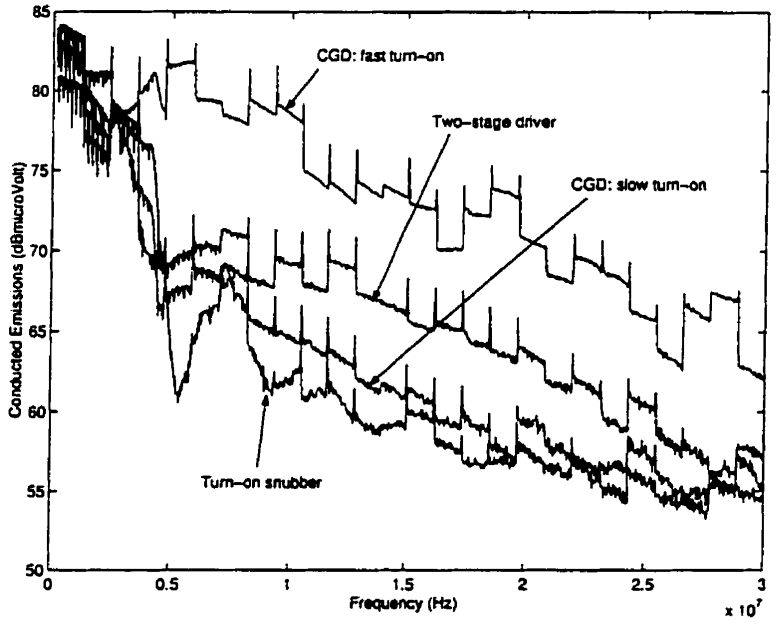

Figure 5.6. Conducted neutral emissions of the 5-A converter for different switching conditions at turn-on and identical turn-off.

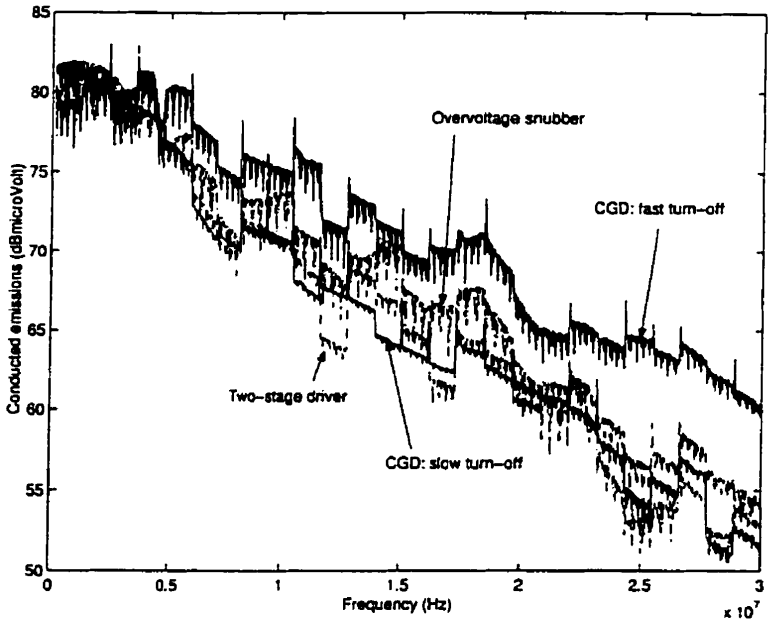

Figure 5.7. Conducted phase emissions of the 5-A converter for different switching conditions at turn-off and identical turn-on.

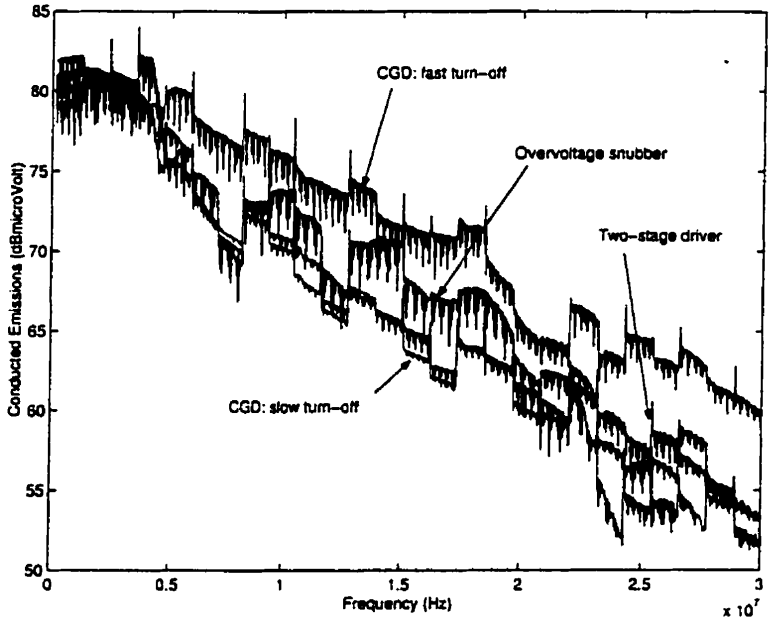

Figure 5.8. Conducted neutral emissions of the 5-A converter for different switching conditions at turn-off and identical turn-on.

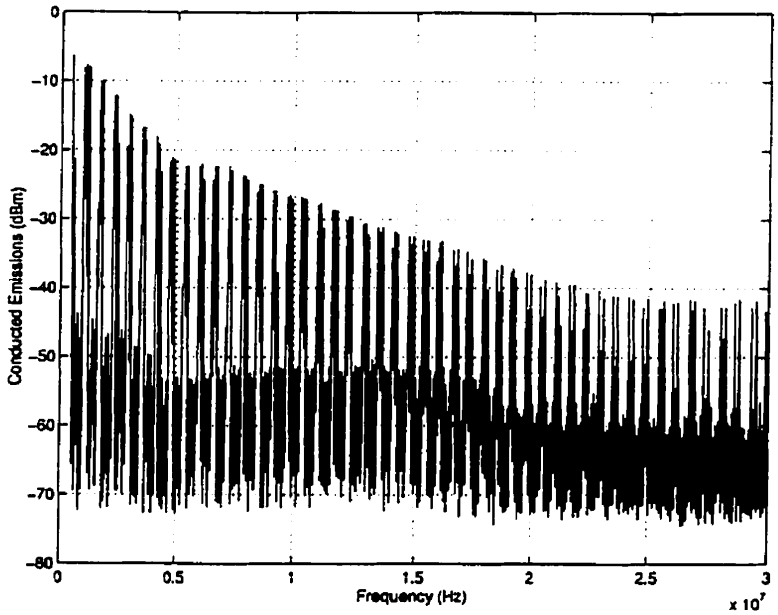

Figure 5.9. Conducted phase emissions of the 15-A converter for slow switching with a CGD ($R_{Gon} = 100\Omega, R_{Goff} = 270\Omega$).

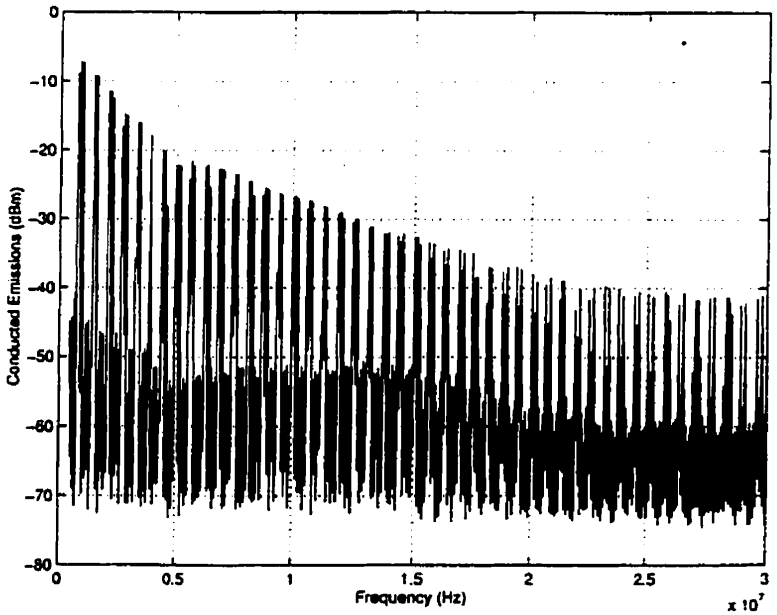

Figure 5.10. Conducted neutral emissions of the 15-A converter for slow switching with a CGD ($R_{Gon} = 100\Omega, R_{Goff} = 270\Omega$).

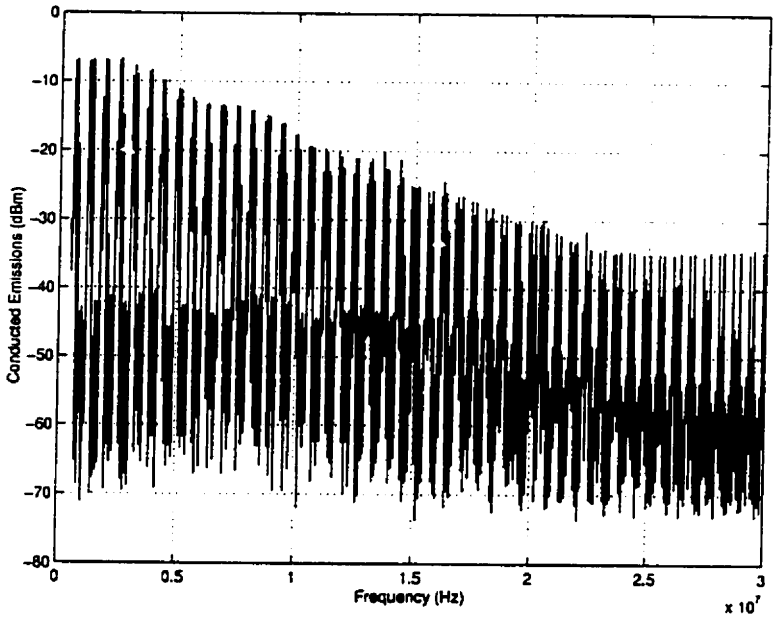

Figure 5.11. Conducted phase emissions of the 15-A converter for high speed switching with a CGD ($R_{Gon} = 2\Omega, R_{Goff} = 5.1\Omega$).

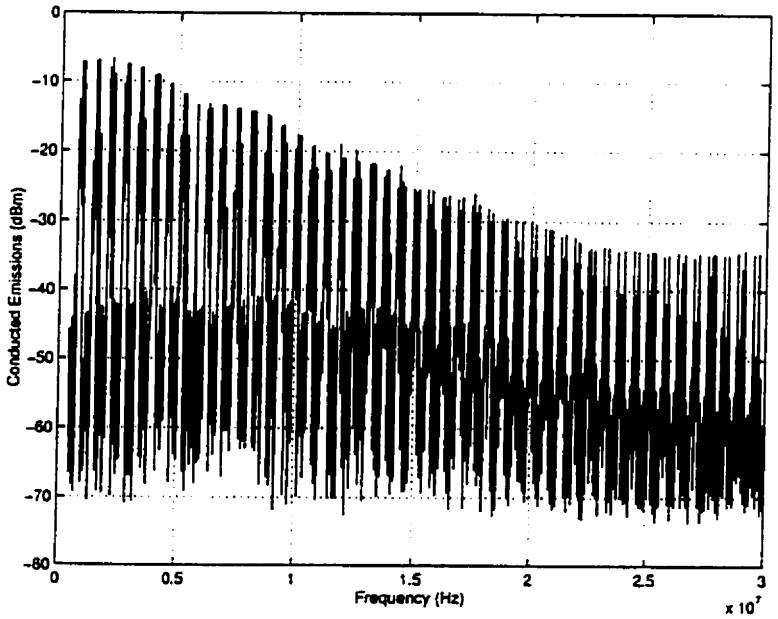

Figure 5.12. Conducted neutral emissions of the 15-A converter for high speed switching with a CGD ($R_{Gon} = 2\Omega, R_{Goff} = 5.1\Omega$).

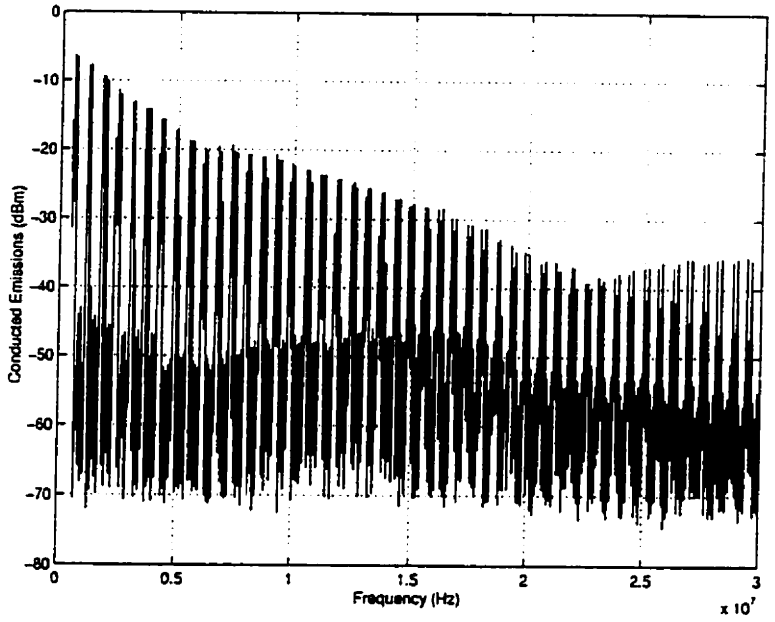

Figure 5.13. Conducted phase emissions of the 15-A converter for switching with the proposed two-stage gate driver.

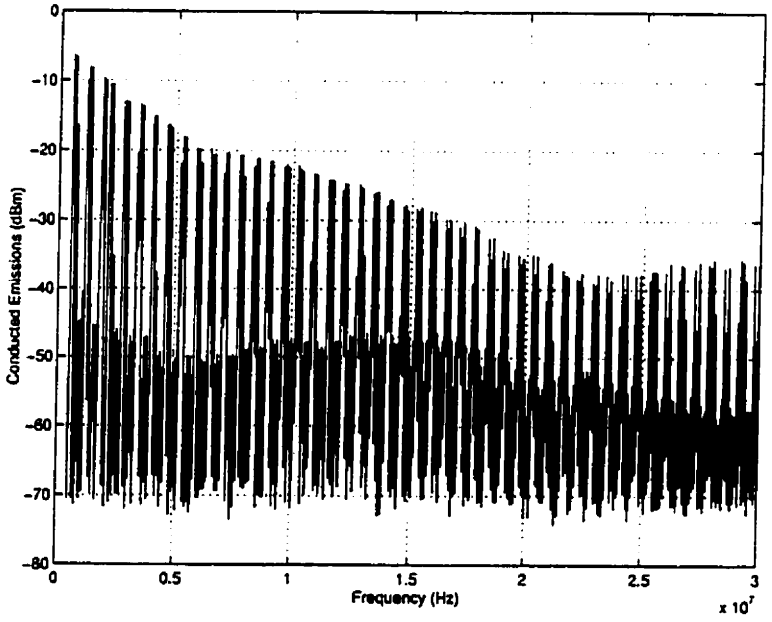

Figure 5.14. Conducted neutral emissions of the 15-A converter for switching with the proposed two-stage gate driver.

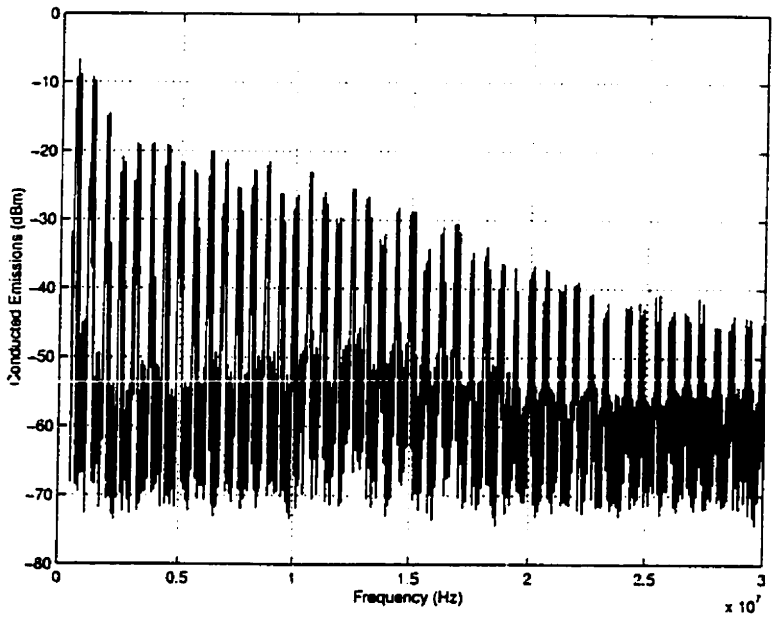

Figure 5.15. Conducted phase emissions of the 15-A converter with turn-on and overvoltage snubbers ($R_{Gon} = 2\Omega, R_{Goff} = 5.1\Omega$).

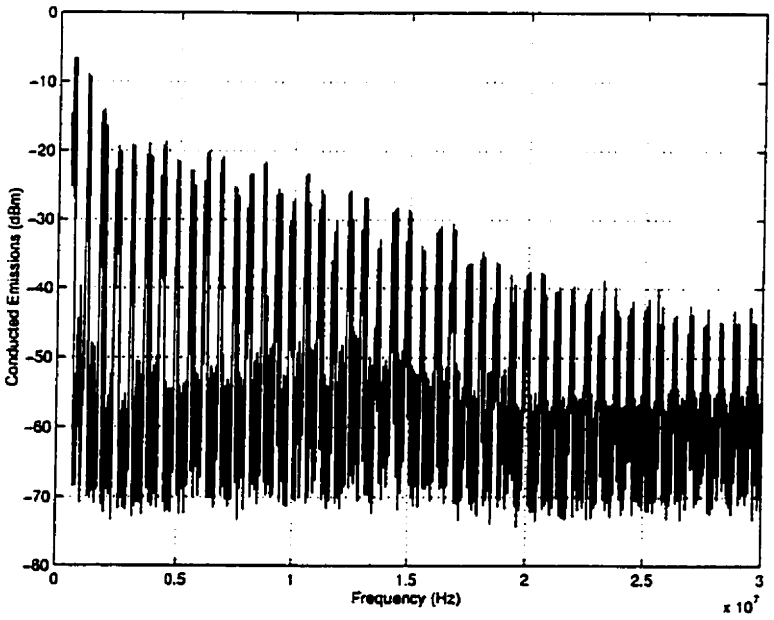

Figure 5.16. Conducted neutral emissions of the 15-A converter with turn-on and overvoltage snubbers ($R_{Gon} = 2\Omega, R_{Goff} = 5.1\Omega$).

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

The two-stage gate drive scheme has been investigated. This scheme can be used to realize low-noise, snubberless operation of high-current gate-controlled devices.

It has been shown that voltage and current overshoots accompanying fast switching operation have a magnitude which is proportional to the rate of current change and is independent of the rate of voltage change with respect to time. This, combined with the fact that for inductive-load switching the voltage and the current do not change simultaneously, form the underlying principle of the two-stage driver technique. Under this scheme, di/dt is kept low to keep the switching transients within acceptable values while dv/dt is kept high to minimize the switching losses and switching times.

In essence, the said scheme aims to optimize the switching behavior. To this end, the control signals need to be generated at precise instants for best performance. Several driver techniques can be envisioned for this purpose. A novel two-stage gate driver has been described which uses gate-source voltage detection for generation of control signals. Also, a simple driver circuit has been presented, which in conjunction with LabWindows/CVI software can be used to characterize the two-stage driver scheme.

The proposed circuits have been tested for a hard-switching application of a power MOSFET and an IGBT, and the experimental results have been presented. It has been shown that the driver scheme combines the slow-drive requirements for low noise and switching stress, and the fast-drive requirements for high speed switching and low switching loss. For the particular application chosen, the two-stage driver scheme offers a total savings in switching loss of 27.6% for the MOSFET and 20.7%

for the IGBT, compared to the conventional means of increasing gate resistance. It may be remarked that the switching performance is, in general, better when snubbers are used. However, this does not take into account the increase in size and cost due to snubbers which may be significant for high power converters.

The driver scheme, as implemented in this thesis, is expected to give optimum results for turn-off switching transients under variable-load conditions. This is because for fixed dc-link voltage applications, such as an inverter, the voltage rise time is more or less independent of the load current. For turn-on, however, the maximum benefits will be attained for current levels close to the nominal design value. For currents below this nominal value, the percentage savings in losses will be slightly reduced.

6.2 Suggestions for future work

Based on the work of this thesis, the following suggestions can be made for future work:

1) As mentioned in the preceding section, the present driver scheme is not optimized for variable-load conditions during turn-on. This is also true for most of the schemes suggested in the literature. Also, most schemes need some sort of extra circuitry for protection of the power transistor during overcurrent and fault conditions. A driver scheme that incorporates adequate transistor protection and optimum switching operation at all load conditions without an excessive increase in part-count would be an interesting and challenging research topic.

Another aspect of the same problem is to make the driver schemes more robust with respect to changes in device parameters, which may vary slightly for the same device type from the same manufacturer (e.g. datasheet for IRGB430U IGBT specifies $V_{GS(th)}$ as ranging from 3.0 V to 5.5 V).

2) It was noted in Chapter 1 that with recent developments, a fair share of the medium and high power markets is expected to belong to IGCTs. Like other power de-

vices, an IGCT has its own characteristic switching behavior and drive requirements. Developing snubberless gate drive techniques, which minimize switching losses, for these devices can result in tremendous savings due to the power levels involved.

REFERENCES

[1] B.K. Bose, "Energy, environment, and advances in power electronics," *IEEE Transactions on Power Electronics*, vol.15, no.4, pp. 688-701, July 2000.

[2] L. Lorenz, G. Deboy, M. Marz, J. Stengl and A. Bachofner, "Drastic reduction of on-resistance with cool MOS," *Power Conversion Intelligent Motion (PCIM)*, no.5, pp. 250-258, 1998.

[3] B.J. Baliga, M.S. Adler, P.V. Gray, R.P. Love and N. Zommer, "The insulated gate transistor," *IEEE Transactions on Electron Devices*, ED-31, pp. 821-828, 1984.

[4] S. Bernet, "Recent developments of high power converters for industry and traction applications," *IEEE Transactions on Power Electronics*, vol.15, no.6, pp. 1102-1117, November 2000.

[5] B.J. Baliga, "Trends in power discrete devices," *Proc. International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, pp. 5-10, 1998.

[6] B.J. Baliga, "The future of power semiconductor device technology," *Proceedings of the IEEE*, vol.89, no.6, pp. 822-832, June 2001.

[7] G. Kaplan, "Industrial electronics," *IEEE Spectrum*, pp. 68-72, January 1999.

[8] J. Catt, R. Chokhawala and B. Pelly, "Introduction to the 600V Add-A-Pak and Int-A-Pak IGBT modules," *Application Note AN-988, International Rectifier Corporation*

[9] N. Mohan, T. M. Undeland and W.P. Robbins, *Power electronics: Converters, Applications and Design*, 2nd Ed., Prentice Hall, New Jersey, 1995.

[10] R. Chokhawala, J. Catt and B. Pelly, "Gate drive considerations for IGBT modules," *IEEE IAS Annual Meeting*, pp. 1186-1195, 1992.

[11] C.R. Paul, *Introduction to electromagnetic compatibility*, John Wiley & Sons, 1992.

[12] L. Tihanyi, *Electromagnetic compatibility in power electronics*, IEEE Press, New York, 1995.

[13] G.L. Skibinski, R.J. Kerkman and D. Sclegel, "EMI emissions in modern PWM ac drives," *IEEE Industry Applications Magazine*, vol.5, no.6, pp. 47-80, November/December 1999.

[14] W.D. Stevenson, *Elements of power system analysis*, McGraw-Hill, 1982.

[15] L.A. Saunders, G.L. Skibinski, S.T. Evon and D.L. Kempkes, "Riding the reflected wave – IGBT drive technology demands new motor and cable considerations," *IAS 43rd Annual Petroleum & Chemical Industry Conference*, Philadelphia, Pennsylvania, pp. 75-84, 1996.

[16] C.J. Melhorn and L. Tang, "Transient effects of PWM drives on induction motors," *IEEE Transactions on Industry Applications*, pp. 1065-1072, vol.33, no.4, July/August 1997.

[17] E. Persson, "Transient effects in application of PWM inverters to induction motors," *IEEE Transactions on Industry Applications*, pp. 1095-1101, vol.28, no.5, September/October 1992.

[18] T. Takahashi, M. Tetmeyer, H. Tsai and T. Lowery, "Motor lead length issues for IGBT PWM drives," *IEEE Pulp and Paper Conference*, pp. 21-27, 1995.

[19] J.D. van Wyk, "Power electronic converters for motion control," *Proceedings of the IEEE*, pp. 1164-1193, vol. 82, no. 8, August 1994.

[20] D.A. Grant and J. Gowar, *Power MOSFETs: theory and applications*, John Wiley & Sons, New York, 1989.

[21] International Rectifier, *HEXFET databook: power MOSFET applications and product data*, 1982.

[22] F. Blaabjerg and J.K. Pedersen, "An optimum drive and clamp circuit design with controlled switching for a snubberless PWM-VSI inverterleg," *IEEE PESC Conf. Rec.*, pp. 289-297, 1992.

[23] M. Oljaca, "Reduction of IGBT switching losses through innovative gate control," *Power Conversion Intelligent Motion*, pp. 83-93, June 1990.

[24] A. Galluzo, R. Letor and M. Melito, "Switching with IGBTs: how to obtain better performance," *Power Conversion Intelligent Motion*, pp. 465-474, June 1991.

[25] B. Weis and M. Bruckmann, "A new gate driver circuit for improved turn-off characteristics of high current IGBT modules," *IEEE IAS Annual Meeting*, pp. 1073-1077, 1998.

[26] H.G. Eckel and L. Sack, "Optimization of the turn-off performance of IGBT at overcurrent and short-circuit current," *EPE Conf. Rec.*, pp. 317-322, 1993.

[27] S. Igarashi, S. Takizawa, M. Tabata, M. Takei and K. Kuroki, "An active control gate drive circuit for IGBTs to realize low-noise and snubberless system," *International Symposium on Power Semiconductor Devices and ICs*, pp. 69-72, 1997.

[28] S. Takizawa, S. Igarashi and K. Kuroki, "A new di/dt control gate drive circuit for IGBTs to reduce EMI noise and switching losses," *IEEE PESC Conf. Rec.*, pp. 1443-1449, 1998.

[29] H. Lee, Y. Lee, B. Suh and D. Hyun, "An improved gate control scheme for snubberless operation of high power IGBTs," *IEEE IAS Annual Meeting*, pp. 975-982, October 1997.

[30] V. John, B. Suh and T.A. Lipo, "High performance active gate drive for high power IGBTs," *IEEE IAS Annual Meeting*, pp. 1519-1529, 1998.

[31] A. Galluzo, M. Melito and G. Belverde, "Switching characteristic improvement of modern gate controlled devices," *EPE Conf Rec*, pp. 374-379, 1993.

[32] S. Musumeci, A. Raciti, A. Testa, A. Galluzo and M. Melito, "A new adaptive driving technique for high current gate controlled devices," *IEEE APEC Conf. Rec.*, pp. 480-486, 1994.

[33] A.N. Githiari, R.J. Leedham and P.R. Palmer, "High performance gate drives for utilizing the IGBT in the active region," *IEEE PESC Conf. Rec.*, pp. 1754-1759, 1996.

[34] C. Gerster and P. Hofer, "Gate controlled dv/dt and di/dt limitation in high power IGBT converters," *EPE Journal*, pp. 11-16, vol. 5, no. 3-4, Jan 1996.

[35] Fluke Corporation Application Note, "Measurement of adjustable speed drives with fluke meters," , 1999

[36] A. Lindberg, W. Belwon and P. Oom, "MACS ICON - IGBT based propulsion systems" *EPE Conf. Rec.*, pp. 3.492-3.497, 1997.

[37] National Instrument, "Multifunction I/O Boards for PCI Bus Computers," *Data Acquisition (DAQ) PCI E series User Manual*, 1997

[38] F. Merienne, J. Roudet and J. L. Schanen, "Switching disturbance due to source inductance for a power MOSFET : analysis and solutions," *IEEE PESC Conf. Rec.*, pp. 1743-1747, 1996.

[39] J. R. Nicholson and J. A. Malack, "RF impedance of power lines and line impedance stabilization networks in conducted interference," *IEEE Transactions on Electromagnetic Compatibility*, pp. 84-86, May 1973.

[40] ANSI C63.4-1992, "American national standard for methods of measurement of radio-noise emissions from low-voltage electrical and electronic equipment in the range of 9kHz to 40GHz ,"

[41] R. E. Tarter, *Principles of solid-state conversion*, Howard W. Sams & Co.(Indianaplois), 1985.

[42] M. Fasching, "Effects of stray inductance on switching transients of an IGBT propulsion inverter and resulting gate control strategies," *IEEE Africon Conf. Rec.*, pp. 467-472, 1996.

[43] R. Anderson, "Select the right plastic film capacitor for your power electronic application," *IEEE IAS Annual Meeting*, pp. 1327-1330, October 1996.

[44] S. Franco, "Polypropylene capacitors for snubber applications," *IEEE IAS Annual Meeting*, pp. 1337-1342, October 1996.

[45] L. Lorenz, "Study of the switching performance of a power MOSFET circuit," *IEEE PESC Conf. Rec.*, pp. 215-224, 1984.

[46] E.S. Oxner, *Power FETs and their applications*, Prentice-Hall Inc., New Jersey, 1982.

[47] Motorola Inc., *Power MOSFET transistor data*, 1988.

APPENDIX A

SWITCHING CHARACTERISTICS OF POWER MOSFETS AND IGBTS

A.1 Switching waveforms

The switching waveforms of a power MOSFET and an IGBT embedded in a step-down dc-dc converter are examined in this section. The switching transients are explained using the circuit model for a power MOSFET and additional discussion is given for an IGBT. The waveforms shown are for the idealized conditions of no dc loop inductance and zero diode reverse recovery current. Also, the L/R time constant of the inductive load is assumed to be large compared to the switching frequency, so that load current may be approximated as a constant current source I_0.

The discussion provided here is mainly extracted from [9, 10, 45] with additional explanations provided by the author.

A.1.1 MOSFET circuit models

The transient performance of the power MOSFET is governed by the oxide and depletion layer capacitances (For a detailed discussion on interelectrode capacitances see [20] or [46]). These capacitances can be modeled by the equivalent ciruit shown in Fig. A.1(a) , which is valid when the MOSFET is in cutoff or in the active region. The drain-source capacitance is not included in the equivalent circuit because it does not materially affect any of the switching characteristics or waveforms.

The capacitances C_{gs} and C_{gd} are not constant but vary with the voltage across them because part of the capacitance is contributed by depletion layers. The change in C_{gd} with $v_{DG}(v_{DS})$, which is diagrammed in Fig. A.1(c), can be as large as a factor of 10 to 100. For approximate calculations of switching waveforms, C_{gd} is approximated by two discrete values C_{gd1} and C_{gd2} shown in Fig. A.1(c) with the

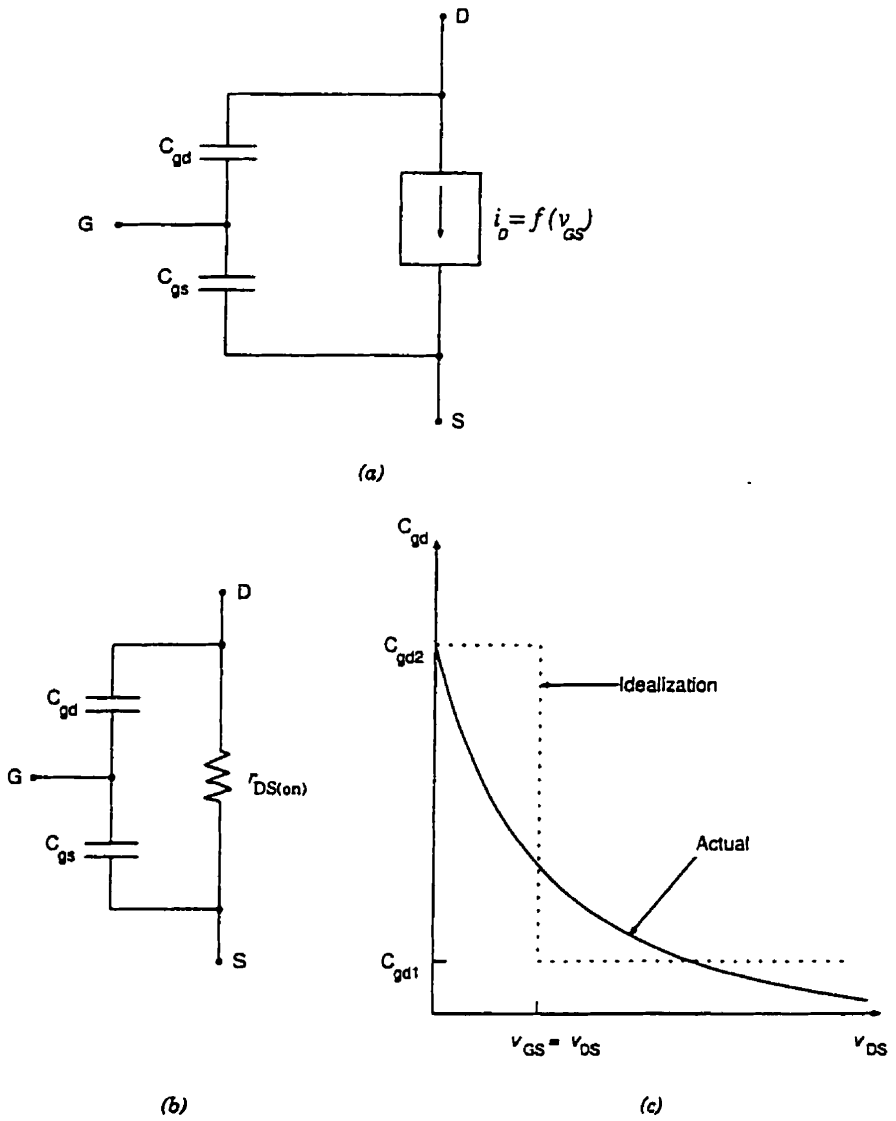

Figure A.1. Circuit models for MOSFETs for transient analysis: (a) MOSFET equivalent circuit in cutoff and active regions; (b) MOSFET equivalent circuit in the ohmic region; (c) variation in gate-drain capacitance with drain-source voltage.

change in value occurring at $v_{DS} = v_{GS}$ where the MOSFET is either entering or leaving the ohmic region. The gate-source capacitance is assumed to be constant.

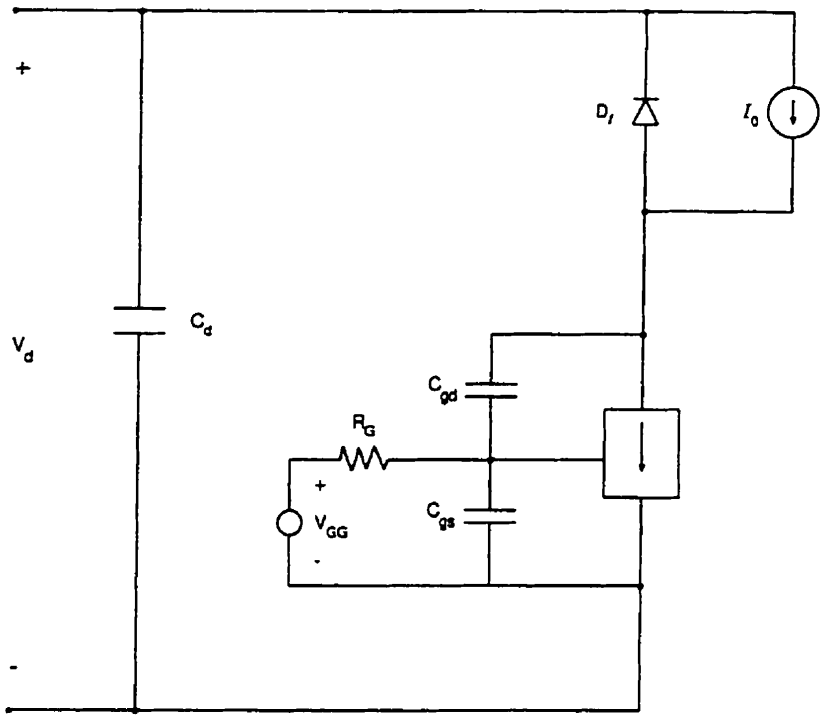

Figure A.2. A MOSFET embedded in a step-down converter.

A.1.2 Turn-on transient

MOSFET turn-on: Fig. A.2 shows a power MOSFET embedded in a step-down converter. It is assumed that the transistor is driven by an ideal voltage source, with gate drive voltage changing in a step manner at $t = 0$ from zero to V_{GG}, which is well above $V_{GS(th)}$. Fig. A.3 shows the turn-on waveforms for the power MOSFET. The turn-on transition occurs in three distinct steps as described below.

Turn-on delay, $t_{d(on)}$ $(0 < t < t_1)$: During the turn-on delay time the gate-source voltage rises from zero to $V_{GS(th)}$ because of the currents flowing through C_{gs} and C_{gd}, as is shown in Fig. A.4(a). The rate of rise of v_{GS} in this region is almost linear, although it is a part of an exponential curve shown dashed in Fig. A.3, which has a time constant $\tau_1 = R_G(C_{gs} + C_{gd1})$. The power MOSFET is still turned-off during this time and therefore v_{DS} and i_D remain constant.

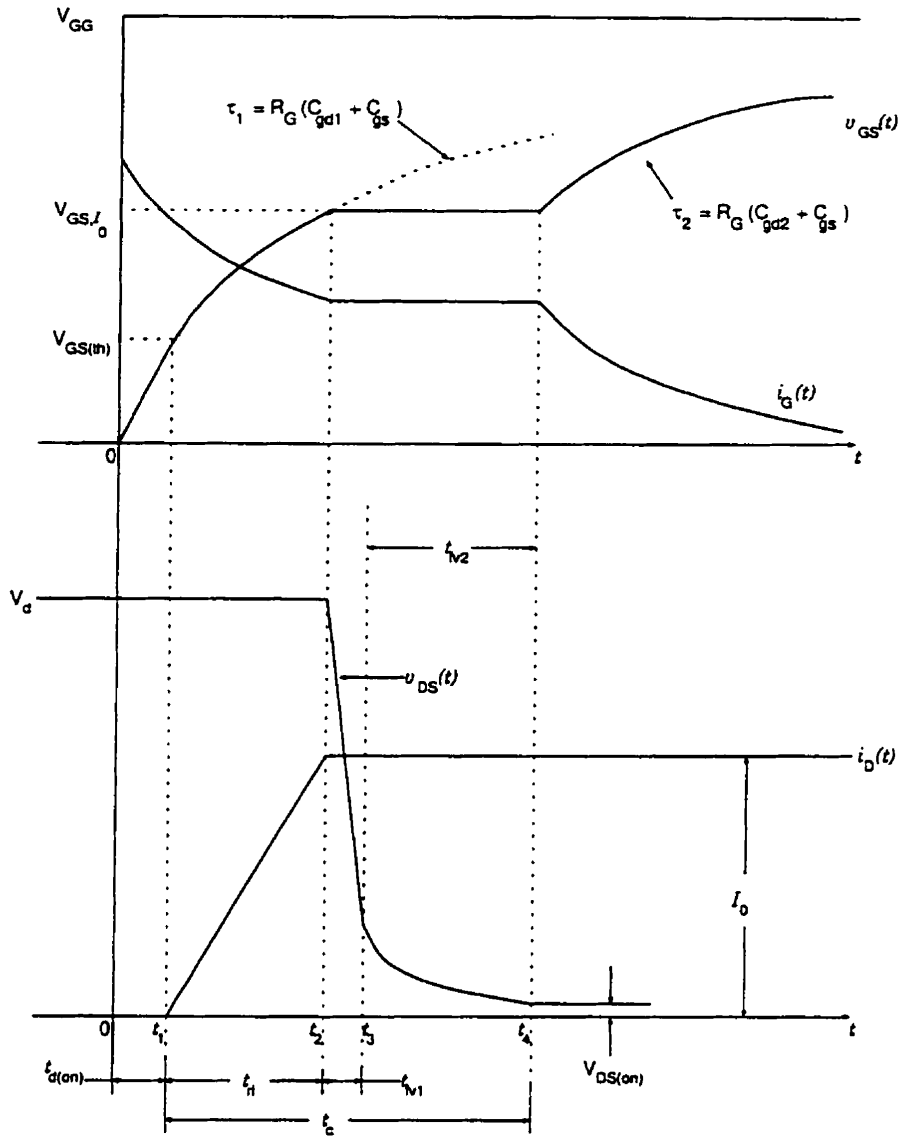

Figure A.3. Sketch of turn-on voltage and current waveforms of the MOSFET for ideal network conditions.

Current rise, t_{ri} $(t_1 < t < t_2)$: When the gate-source voltage reaches the threshold voltage, the drain current begins to flow and the MOSFET current rises in concert with the gate voltage. The current rise is almost linear and is expressed by

$$i_D(t) = g_m(v_{GS}(t) - V_{GS(th)}) \tag{A.1}$$

where g_m is the transconductance of the power transistor.

The equivalent circuit during the period of current growth is shown in Fig. A.4(b). The time required for i_D to build up from zero to I_0 is the current rise time t_{ri}. During the interval t_1–t_2 the diode is still in forward conduction, hence the dc bus voltage V_d essentially appears across the power transistor.

Voltage fall ($t_2 < t < t_4$): After the current transfer is complete at $t = t_2$, the diode— assumed to have no reverse recovery— starts to support the reverse voltage. The gate voltage becomes temporarily clamped at V_{GS,I_0}, which is the gate-source voltage from Eq. A.1 needed to maintain $i_D = I_0$. This apparent exaggeration of input capacitance due to the clamping of gate voltage is usually referred to as the *Miller effect.* The entire gate current i_G, which is given by

$$i_G = \frac{V_{GG} - V_{GS,I_0}}{R_G} \tag{A.2}$$

discharges the C_{gd} capacitance as indicated in Fig. A.4(c). This causes the drain-gate voltage to drop at a rate

$$\frac{dv_{DG}}{dt} = \frac{i_G}{C_{gd}} = \frac{V_{GG} - V_{GS,I_0}}{R_G C_{gd}} \tag{A.3}$$

Since $v_{GS} = V_{GS,I_0}$ during this interval, so $dv_{GS}/dt = 0$. Therefore,

$$\frac{dv_{DS}}{dt} = \frac{dv_{DG}}{dt} = \frac{V_{GG} - V_{GS,I_0}}{R_G C_{gd}} \tag{A.4}$$

The decrease in v_{DS} occurs in two distinct time intervals t_{fv1} and t_{fv2}. The first time interval corresponds to the traverse through the active region where $C_{gd} = C_{gd1}$. The second time interval corresponds to the completion of the transient in the ohmic region where the equivalent circuit shown in Fig. A.4(d) applies and $C_{gd} = C_{gd2}$.

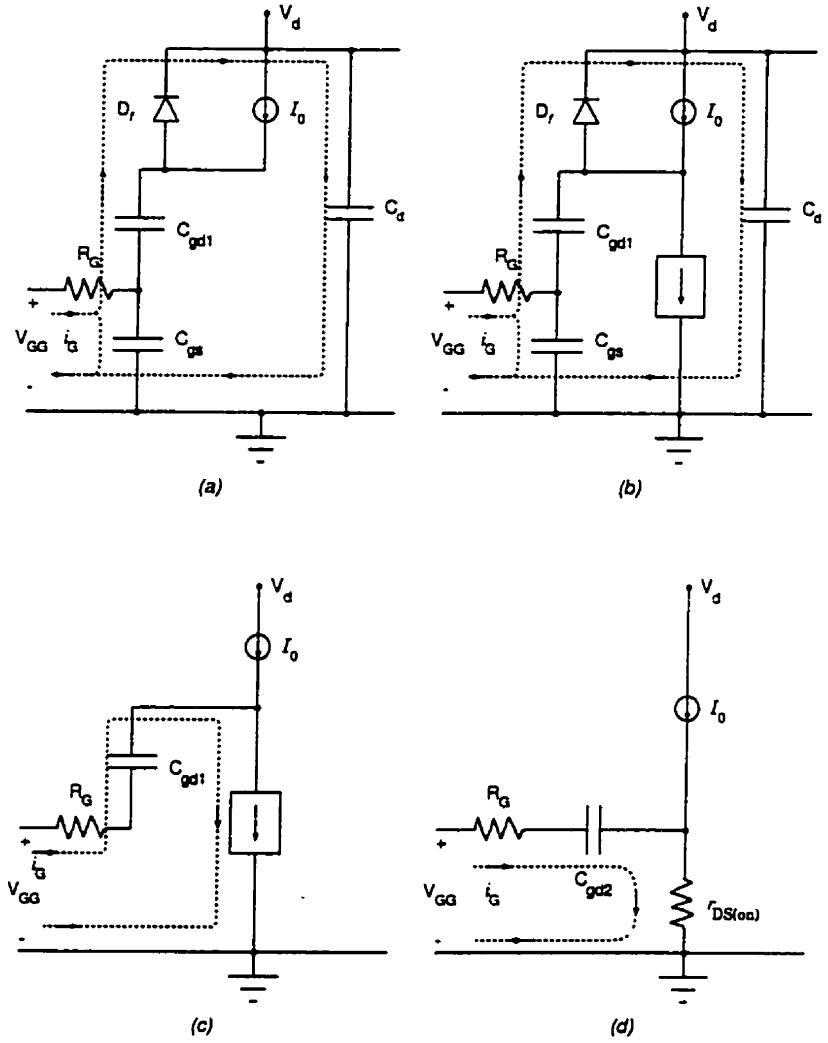

Figure A.4. Equivalent circuits used to estimate the turn-on switching waveforms of the MOSFET: (a) equivalent circuit during $t_{d(on)}$; (b) equivalent circuit during t_{ri}; (c) equivalent circuit during the t_{fv1} interval; (d) equivalent circuit during t_{fv2}.

Once the drain-source voltage has completed its drop to the on-state value of $I_0 r_{DS(on)}$ $(= V_{DS(on)})$, the commutation process is complete. The gate-source voltage becomes unclamped and continues its exponential increase to V_{GG}. This occurs with a time constant $\tau_2 = R_G(C_{gs} + C_{gd2})$, and simultaneously the gate current decays toward zero with the same time constant, as shown in the waveforms of Fig. A.3.

IGBT turn-on: The current and voltage waveforms for the turn-on of an IGBT embedded in a step-down converter are quite similar to those for the MOSFET, shown in Fig. A.3. This is because the IGBT essentially acts as a MOSFET during most of the turn-on interval, and the same equivalent circuits used for discussing the MOSFET turn-on can also be used for calculating the turn-on characteristics of the IGBT.

A.1.3 Turn-off transient

MOSFET turn-off: The turn-off of the MOSFET involves the inverse sequence of events that occur during turn-on. The same basic analytical approach used to find the turn-on switching waveforms can also be applied to determine turn-off characteristics. The turn-off waveforms and associated time intervals are shown in Fig. A.5 for an assumed step change in the gate drive voltage at $t = 0$ from V_{GG} to zero.

IGBT turn-off: The turn-off transient in the IGBT follows the same sequence of events as in a MOSFET till the collector-emitter voltage rises to its blocking state value. Prior to reaching this state, the switching behavior is governed by the MOSFET portion of the IGBT and the equivalent circuits of the power MOSFET are applicable.

The major difference between the IGBT turn-off and the power MOSFET turn-off is observed in the collector current waveform where two distinct time intervals are present. This is shown in Fig. A.6 which also shows the approximate equivalent circuit of the IGBT. The rapid drop that occurs during the t_{fi1} interval corresponds to the turn-off of the MOSFET section of the IGBT. The "tailing" of the collector current during the second interval t_{fi2} is due to the stored charge in the drift region. Since the MOSFET section is off and there is no reverse voltage applied to the IGBT terminals that could generate a negative collector current, there is no possibility for removing the stored charge by carrier sweep-out. The only way that these excess carriers can

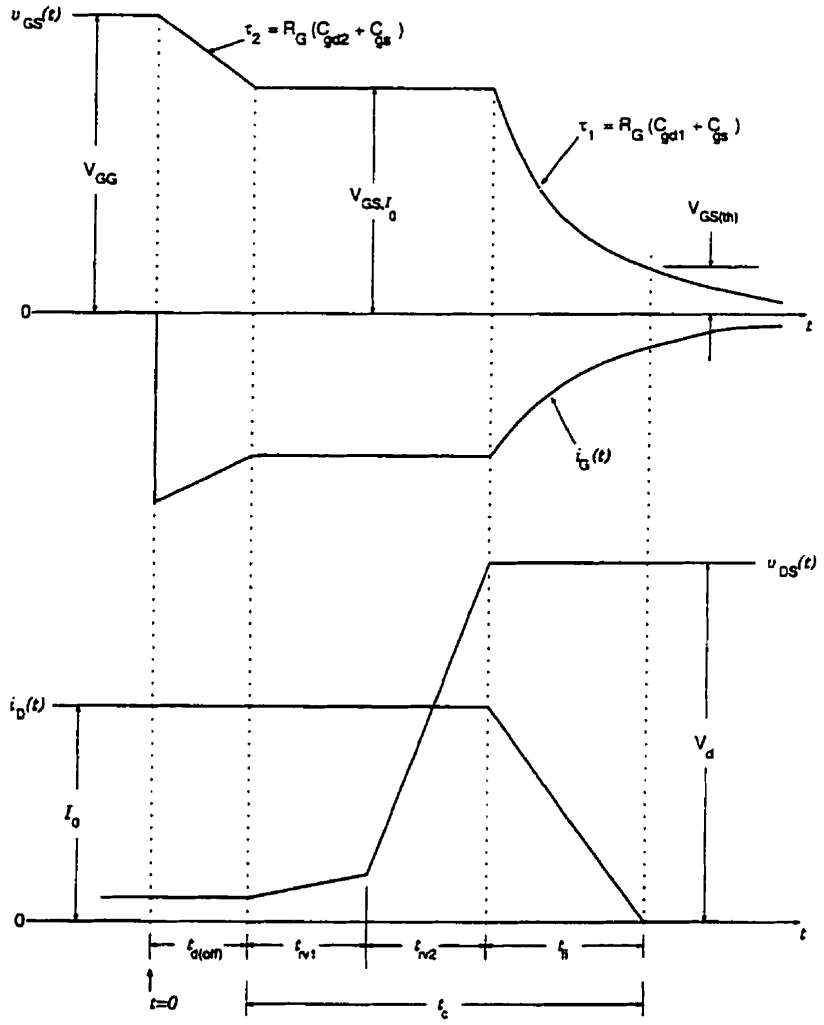

Figure A.5. The MOSFET voltage and current waveforms at turn-off in the diode-clamped inductive load circuit.

be removed is by recombination within the IGBT. The excess-carrier lifetime in the drift region is made large for a low on-state voltage drop. A large carrier lifetime correspondingly results in a long t_{fi2} interval and causes the characteristic "tailing" effect in the IGBTs.

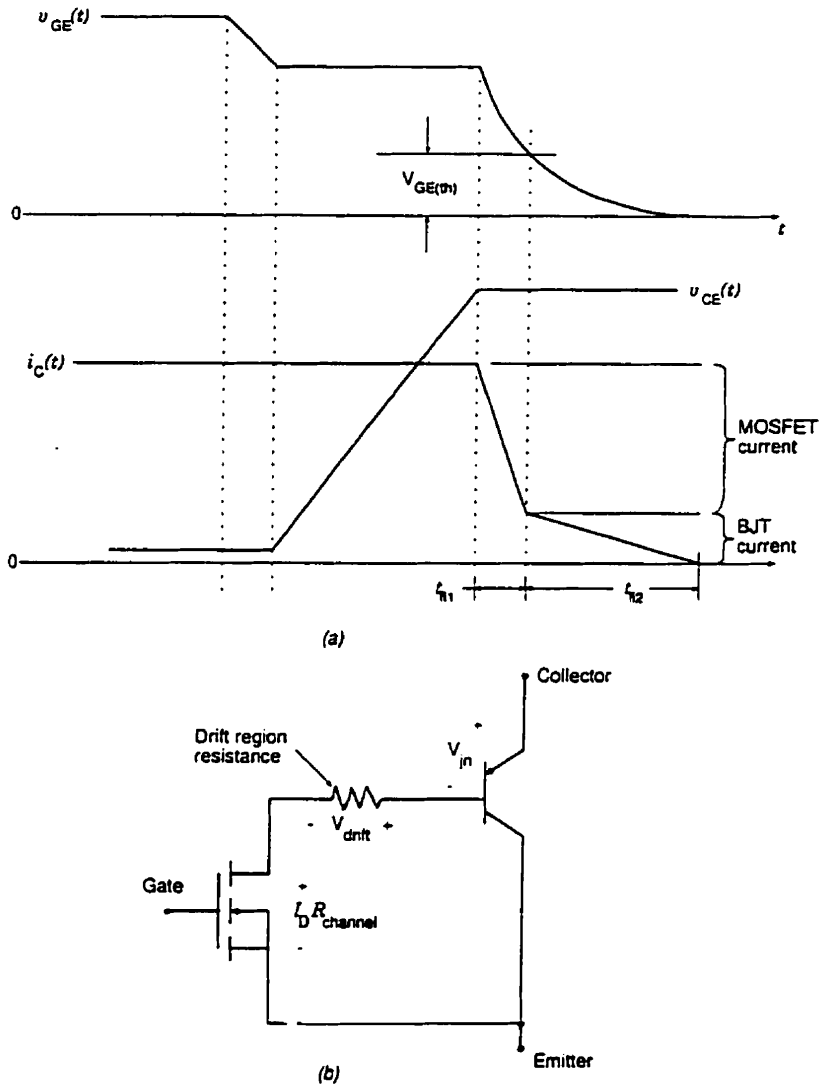

Figure A.6. (a) Sketch of turn-off voltage and current waveforms of an IGBT embedded in a step-down converter. (b) Approximate equivalent circuit of the IGBT.

A.2 Switching times

The preceding discussion has defined switching times for idealized switching waveforms. In practice, the waveforms are not as sharply defined, and this necessitates the switching times to be specified in the following manner [8, 47]:

$t_{d(on)}$— Turn-on delay time: $t_{d(on)}$ is the delay time between the initiation of gate

drive voltage and the start of MOSFET drain current. It is the time measured from the instant at which a positive going gate pulse reaches 10% of its peak amplitude to the instant at which the drain current reaches 10% of its on-state amplitude.

t_{ri}— Current rise time: t_{ri} is the rise time of the current, with a clamped inductive load. It is the time taken by the drain current to rise from 10% to 90% of its on-state value.

t_{fv}— Voltage fall time: t_{fv} is the fall time of the voltage and is the interval during which the drain voltage falls from 90% to 10% of its off-state value.

$t_{d(off)}$— Turn-off delay time: $t_{d(off)}$ is the delay time between the removal of gate drive voltage and the start of the voltage rise across the power transistor. It is the interval during which an input pulse that is switching the transistor to its non-conducting state falls from 90% of its peak amplitude and the drain voltage rises to 10% of its off-state amplitude.

t_{rv}— Voltage rise time: t_{rv} is the rise time of the voltage and is the interval during which the drain voltage rises from 10% to 90% of its off-state value.

t_{fi}— Current fall time: t_{fi} is the fall time of the current, with a clamped inductive load. It is the time taken by the drain current to fall from 90% to 10% of its on-state value.

APPENDIX B

TRANSIENT REDUCTION BY A CONVENTIONAL GATE DRIVE CIRCUIT

As mentioned in Chapter 2, the CGD method usually refers to employing fixed gate resistors during the switching process. A CGD circuit, such as the one shown in Fig. 3.1 and repeated here for convenience, can reduce the magnitude of switching transients by slowing down the switching transition.

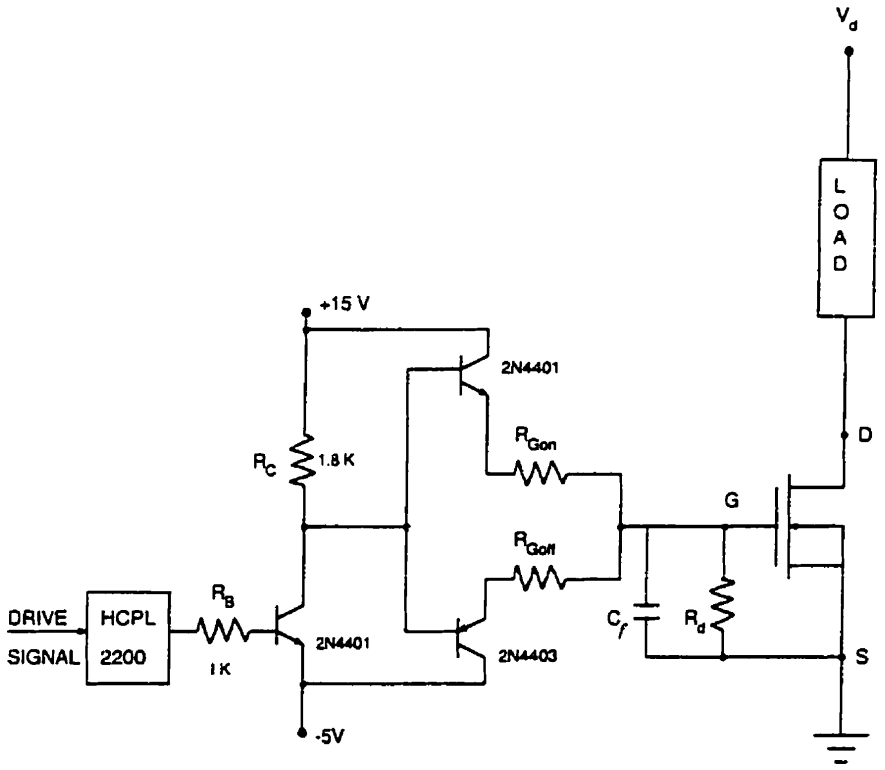

Figure B.1. A conventional gate drive circuit.

From Eqs. 2.1 and 2.2, the diode reverse recovery current at turn-on, and the transistor overvoltage at turn-off can be decreased by reducing $(di/dt)_{on}$ and $(di/dt)_{off}$

respectively. This, in turn, can be achieved by increasing the values of gate resistors R_{Gon} and R_{Goff}. Unfortunately, increasing the gate resistors also leads to long switching delays and a considerable reduction in the voltage slopes at turn-on and turn-off, resulting in increased switching losses. This is demonstrated in Figs. B.2 and B.3 which show the switching waveforms of a power MOSFET and an IGBT respectively for different values of gate resistors. It can be readily seen that increasing the gate resistor reduces the rate of change of current thereby limiting the peak values of reverse recovery current and voltage overshoot. In addition, reducing the current slopes also attenuates/eliminates ringing thus reducing the EMI generated by the converter.

On the other hand, increasing the gate resistance slows down the entire switching process and leads to an increase in switching loss. This is illustrated in Fig. B.4 which shows peak values of voltage and current transients as a function of the switching loss. It can be seen that the gate resistance must be increased significantly (by an order of magnitude) to reduce the transients appreciably. This is accompanied by an enormous increase in the loss incurred during the switching transition. High switching losses severely increase the heat sink requirements leading to increased size and cost of the converter, and/or limiting the switching frequency at which the converter can be operated.

The waveforms in Fig. B.2 and B.3 are aligned by the instant when the gate signal is applied to the transistor. This is done to show the long switching delays that are introduced by the use of large gate resistors. This dependence is characterized in Figs. B.5 and B.6 which also show the increase in voltage and current rise times as the gate resistance is increased. The increased switching times require longer blanking times for PWM converters leading to higher distortion in the output spectrum of the power converter. It is interesting to note from Fig. B.5 that compared to a MOSFET, the IGBT turn-off is not as strongly affected by the value of gate resistor.

The results presented in Figs. B.2 to B.6 clearly indicate that while increasing the gate resistance is a simple and effective means of reducing switching stress and noise levels, the deterioration in overall system performance is quite significant to prevent the use of this method in high performance applications.

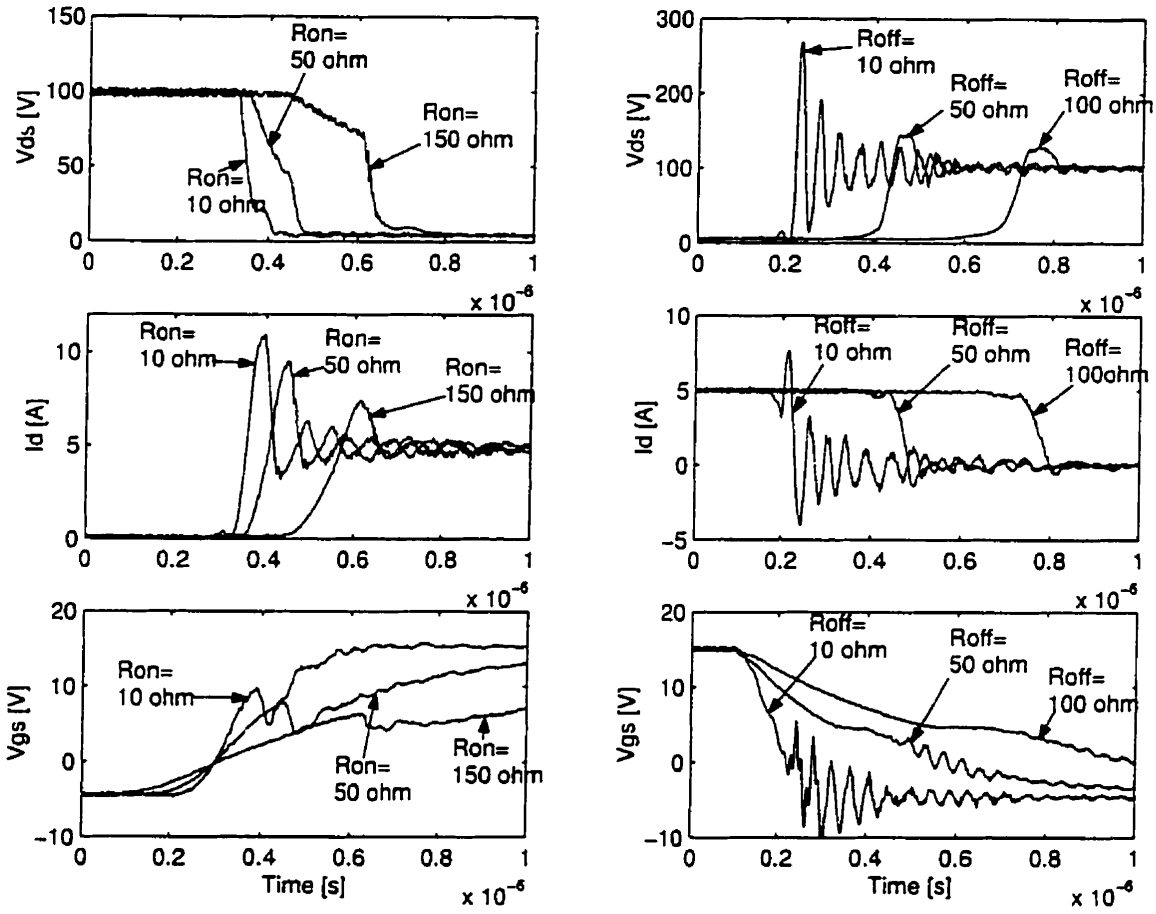

Figure B.2. Switching waveforms of MOSFET with a CGD as the gate resistance is varied. Left: Turn-on waveforms for gate resistor values of 10, 50, 150 Ω. Right: Turn-off waveforms for gate resistor values of 10, 50, 100 Ω. Other conditions are as follows: V_d=100 V, I_0=5 A, V_{GG+}=15 V, V_{GG-}=-5 V.

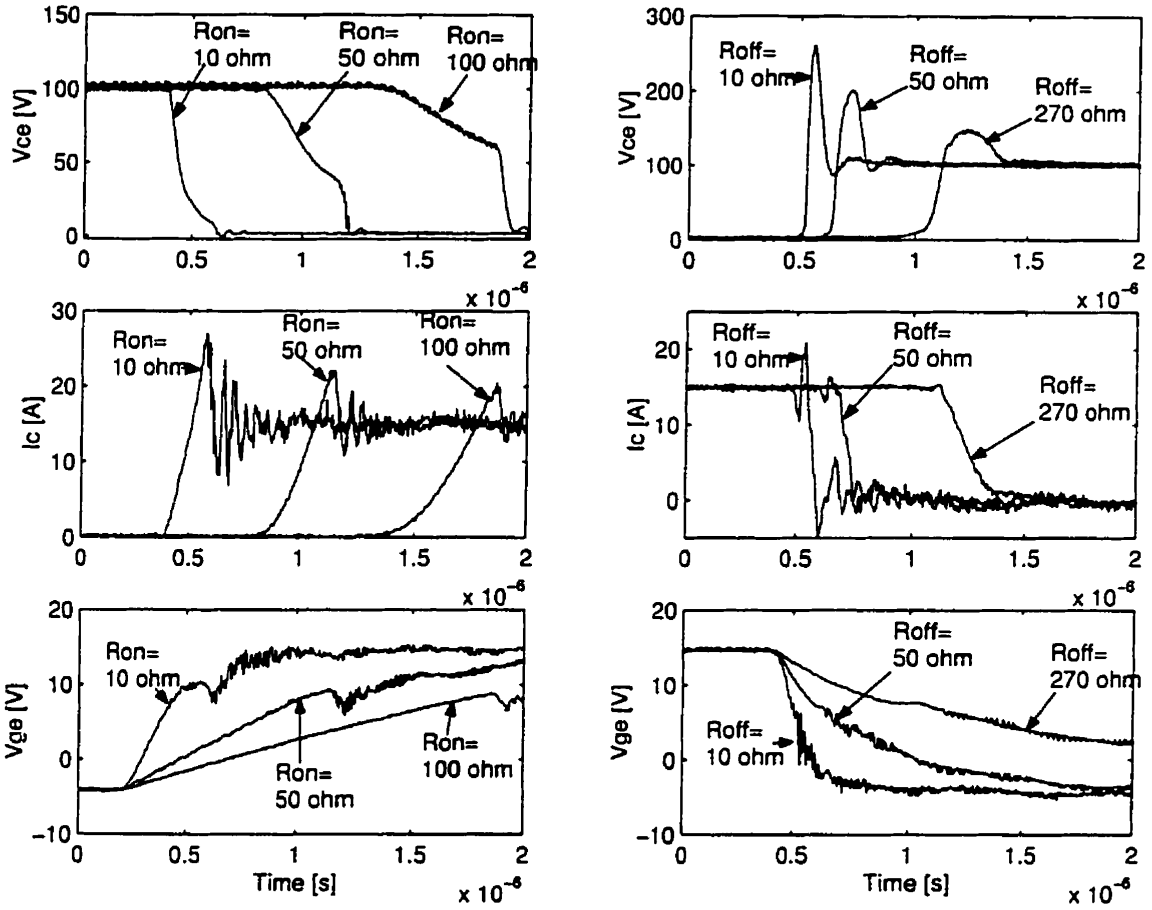

Figure B.3. Switching waveforms of IGBT with a CGD as the gate resistance is varied. Left: Turn-on waveforms for gate resistor values of 10, 50, 100 Ω. Right: Turn-off waveforms for gate resistor values of 10, 50, 270 Ω. Other conditions are as follows: V_d=100 V, I_0=15 A, V_{GG+}=15 V, V_{GG-}=-5 V.

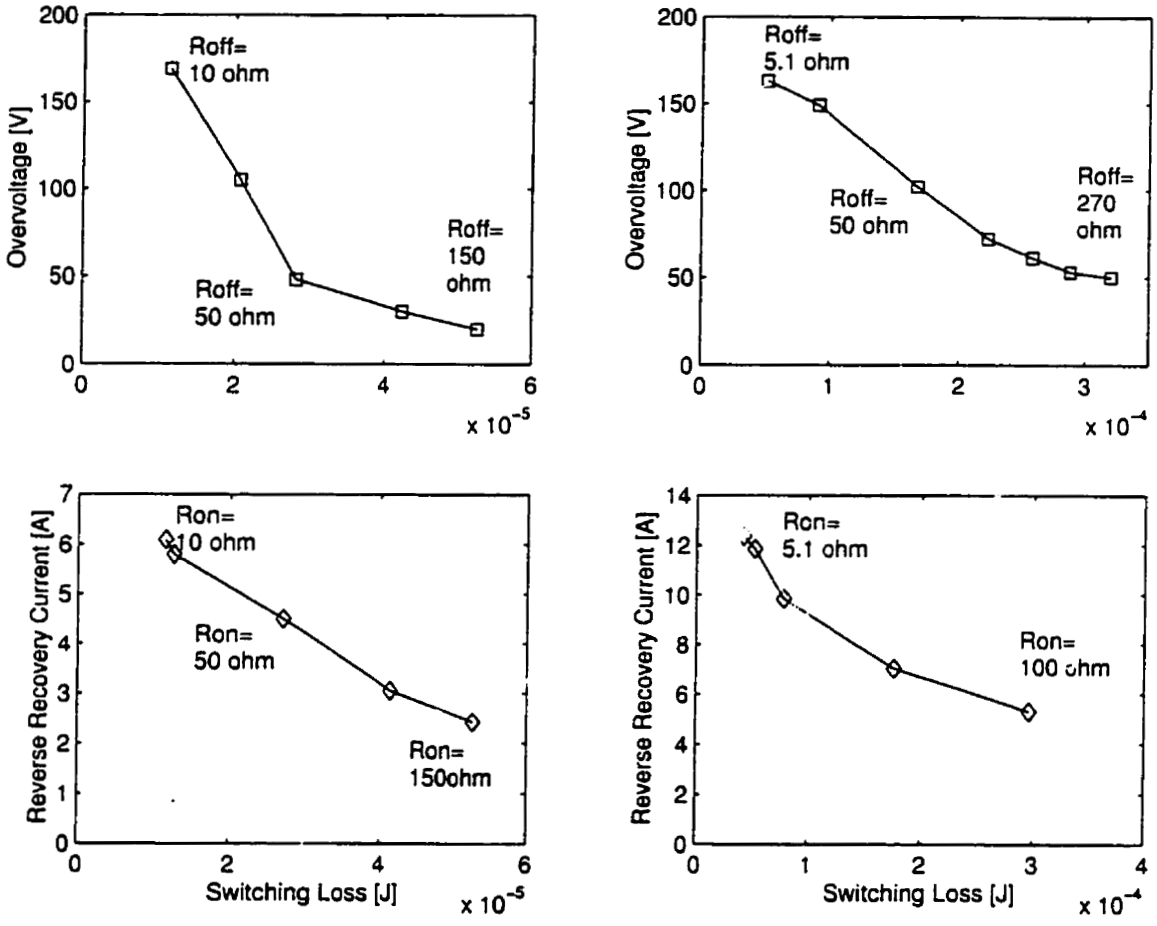

Figure B.4. Plots showing the dependence of switching loss and peak values of transients on the gate resistance. Left: Plots for MOSFET switching at 5 A, 100 V when the gate resistance is varied from 10 Ω to 150 Ω. Right: Plots for IGBT switching at 15 A, 100 V when the gate resistance is varied from 5 Ω to 270 Ω at turn-off, and 5 Ω to 100 Ω at turn-on.

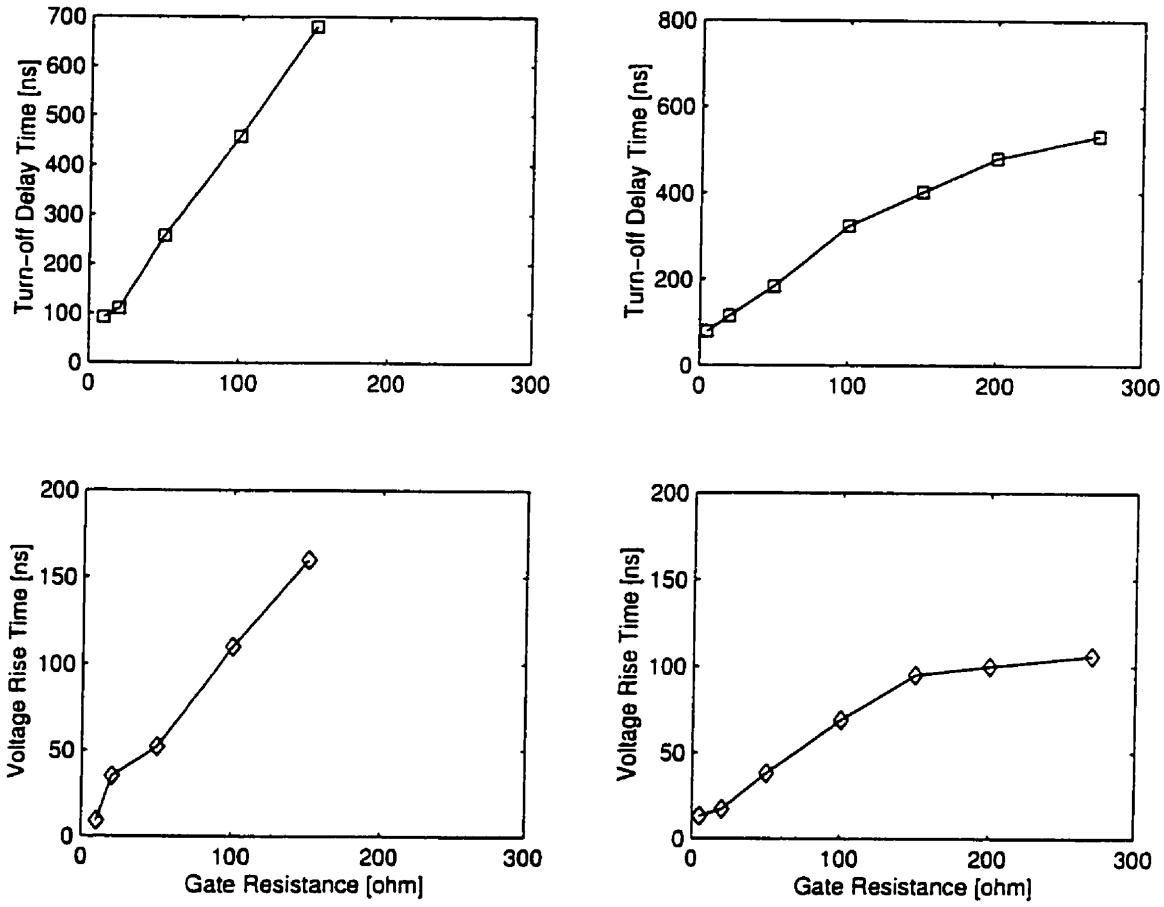

Figure B.5. Turn-off delay times and voltage rise times vs turn-off gate resistance. Left: Plots for MOSFET switching at 5 A, 100 V. Right: Plots for IGBT switching at 15 A, 100 V.

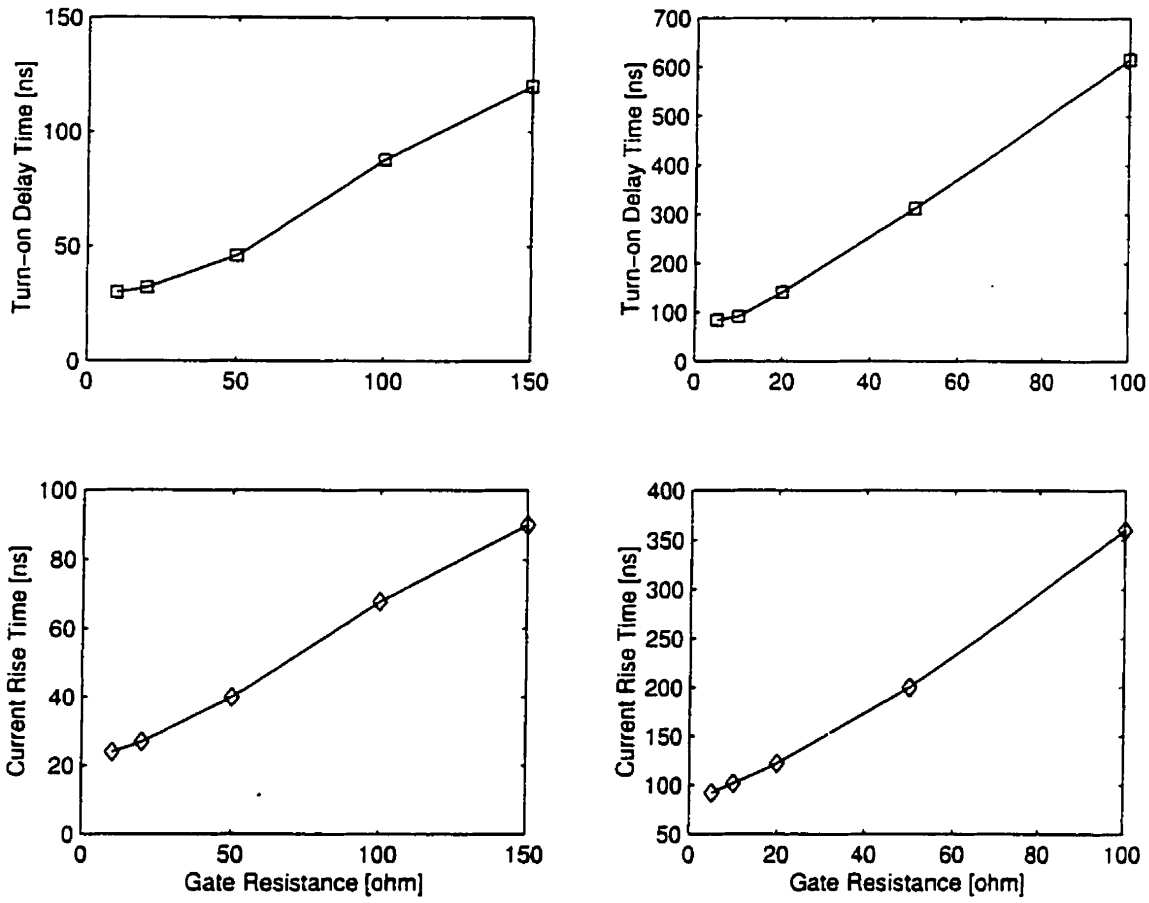

Figure B.6. Turn-on delay times and current rise times vs turn-on gate resistance. Left: Plots for MOSFET switching at 5 A, 100 V. Right: Plots for IGBT switching at 15 A, 100 V.