THE UNIVERSITY OF CALGARY

Improved
Optical Position Sensing

by

Ian C. Williamson

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The undersigned certify that they have read, and recommended to the Faculty of Graduate Studies for acceptance, a thesis entitled, "Improved Optical Position Sensing" submitted by Ian C. Williamson in partial fulfilment of the requirements for the degree of Master of Science.

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Date Aug. 31/92

Abstract

This thesis is presented in three distinct sections each of which relates to the recently developed optical position sensor in a separate way. A solution to the observed reduction in full scale position sensor output with large standard deviation light sources is presented. This solution will ensure that the position sensor static output signal will remain nearly identical regardless of the width of the incident light source.

A fully commercial part version of the position sensor is also presented. This design is ideal for lower cost position sensors in that it requires no custom VLSI components.

The position sensor is also applied to the application of long exposure telescopic astrophotography. This design was created to perform tracking corrections to telescope guidance systems through a feedback arrangement.

It is hoped that this research will further the understanding and use of the optical position sensor.

Acknowledgments

I am greatly indebted to Dr. J.W. Haslett for all his help with both the research contained in and the production of this thesis. He often gave me simple advice which put me back on track when times were tough.

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I would also like to thank Robert Condon of the Department of Physics and Astronomy for help with the telescope tracking system and access to the Astrophysics Department's telescope equipment.

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X_{centre}	Centroid position (arbitrary units)
$M(x)$	Mass function (arbitrary units)
N	Number of detectors in an array
n	Detector number
I_{photo}	Photocurrent (amperes)
P_{opt}	Optical power (watts)
η	Quantum efficiency (unitless)
q	Electronic charge (coulombs)
h	Planck's constant
f	frequency (Hertz)
V_{in}	Input voltage (volts)
V_{out}	Output voltage (volts)
τ	Time constant (seconds)
I_{pmax}	Maximum photocurrent in a gaussian distribution (amperes)
μ	Mean position of a gaussian distribution
σ	Standard deviation
V_{REF}	Position sensor reference voltage (volts)
I_{in}	Input current (amperes)
I_{out}	Output current (amperes)
I_B	Transconductance amplifier bias current (amperes)

I_L	Transconductance amplifier linearization current (amperes)
I_{HE}	Highest end of array current (amperes)
I_{LE}	Lowest end of array current (amperes)
V_{DS}	MOS transistor drain to source voltage (volts)
V_{GS}	MOS transistor gate to source voltage (volts)
V_{SB}	MOS transistor source to bulk voltage (volts)
V_T	MOS transistor threshold voltage (volts)
V_{TO}	Unmodulated MOS threshold voltage (volts)
V_{UPPER}	Upper cascode mirror gate voltage (volts)
V_{LOWER}	Lower cascode mirror gate voltage (volts)
β	MOS transistor transconductance (amperes/volt^2)
L	MOS transistor gate length (meters)
W	MOS transistor gate width (meters)
V_{DD}	Positive power supply voltage (volts)
V_{SS}	Negative power supply voltage (volts)
I_{DO}	MOS transistor "saturation" current (amperes)
γ	MOS transistor body effect factor ($\sqrt{volts}$)
2ϕ	MOS transistor surface inversion potential (volts)
G	Gain factor (unitless)
K	Gain factor (unitless)
V_{array}	Biasing voltage (volts)
λ	Light wavelength (meters)

c	Speed of light (meters/second)
E_{gap}	Semiconductor energy band gap (electron volts)
T_{clk}	Clock period (seconds)
V_{TH}	The thermal voltage kT/q (volts)
k	Boltzmann's constant (electron volts/degree kelvin)
F_{photo}	Optical flux (watts/cm^2)

Chapter 1

The Basic Position Sensor

1.1 Introduction

Perhaps one of the most difficult aspects of electronics is the interfacing of an electronic circuit to some "real world" stimulus while maintaining a certain level of accuracy. The stimulus may be almost anything that can be perceived by the five senses, such as the human voice, temperature, or in our case the movement of a spot of light.

The precise aspect of the spot of light that we are concerned with in this thesis is the instantaneous position of its image. In an ideal system, we would like to remove the effects of all other variables inherent to the spot of light, such as its intensity and size, and produce some measure of the position of the centre of its light profile while maintaining accuracy and circuit simplicity.

The first and most obvious solution to this design problem would be to move as

quickly as possible into the digital domain by using a charge coupled device (CCD) imager as the photoreceptor, an analogue to digital converter (ADC) to perform the domain conversion and a powerful microprocessor to determine the image position. However, this method has its problems. Firstly, the support hardware for CCD imagers including clock generation, power supplies and low noise amplifiers greatly reduces the circuit simplicity. Secondly, accuracy is reduced in the process of conversion of the CCD video signal to digital form. In order to maintain sufficient accuracy, a large number of digital bits must be used, requiring even more support circuitry. Furthermore, the processor handling the calculation of the light position must be able to handle the large amounts of data at a very fast rate in order to maintain approximately continuous position information updates.

Quick calculations using a suitable microprocessor such as the Intel 80C196KB [1] which has its own built in analogue to digital (ADC) and digital to analogue (DAC) converters and simple support circuitry reveal that, even when running at 12 MHz, only 3263 pixels may be processed per second. For a CCD array such as the English-Electric P8600 [2] that contains 576 lines of 385 pixels each, the position information may only be updated every 67 seconds (Using only 10 bits to describe the input video signal)! The update time could probably be reduced and accuracy increased by several orders of magnitude by using a faster, more sophisticated microprocessor with external data conversion circuits, but, again, this will add circuit complexity, and still not achieve continuous operation.

The solution to these problems can be realized by remaining in the analogue

domain. Here, it is possible to achieve continuous output signal updates with relatively simple low power circuitry.

1.2 Mechanical Centroid Definition

A basic analogue optical position sensing system has been developed in recent years [3]. This system borrows from the mechanical engineering concept of the centroid which describes an object's centre of balance as the point at which the sum of all moments is zero.

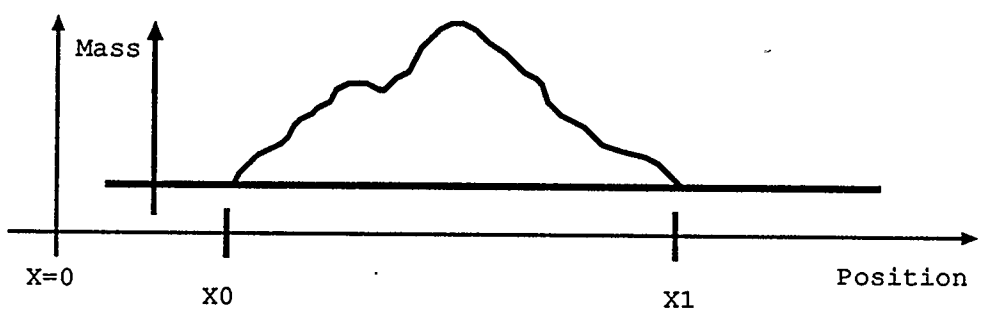

Figure 1.1 - A continuous distribution of mass.

By using Fig. 1.1 as a reference and dealing only in one dimension,

$$\int_{X_0}^{X_1} (X_{centre}-x) \cdot M(x)\ dx = 0 \qquad (1.2.1)$$

where X_{centre} is the position of the centroid, X_0 and X_1 are the limits of the object, and M(x) is the mass at position x, with all distances measured from the same arbitrary origin.

If a complete object is taken to be made up of discrete particles, Eqn. (1.2.1) will become

$$\sum_{n=1}^{N} (X_{centre} - X_n) \cdot M_n = 0 \qquad (1.2.2)$$

where N is the total number of particles, M_n is particle n's mass and X_n is the distance from some arbitrary origin to particle n. If this equation is then solved for X_{centre},

$$X_{centre} = \frac{\sum_{n=1}^{N} X_n \cdot M_n}{\sum_{n=1}^{N} M_n} \qquad (1.2.3)$$

results.

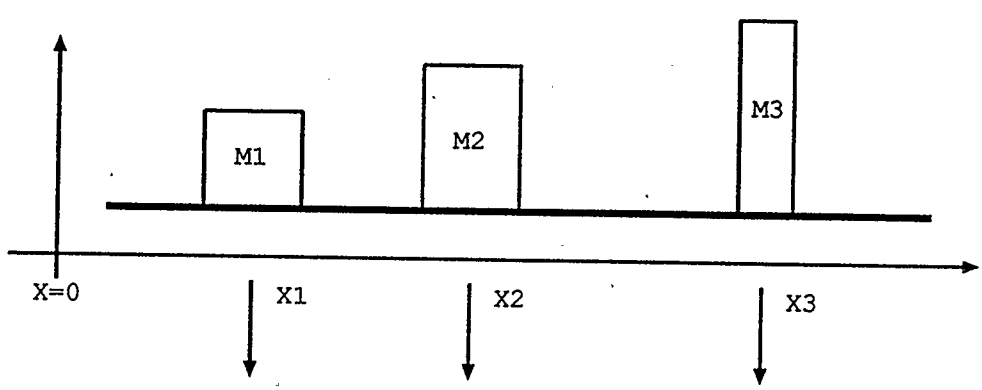

Figure 1.2 - A sample distribution of particle masses.

By way of a simple example, if the system shown in Fig. 1.2 is used as a reference, with the support weight being neglected, the centroid, or centre of balance, for

the complete object can be calculated by using Eqn. (1.2.3) and results in

$$X_{centre} = \frac{X_1M_1 + X_2M_2 + X_3M_3}{M_1 + M_2 + M_3} \tag{1.2.4}$$

which is seen to be simply a weighted average position with N=3.

1.3 Electro-Optical Centroid

The block diagram shown in Fig. 1.3 depicts a one dimensional rendition of the previously mentioned optical position sensor (OPS) created by Gonnasson et al [3]. The simplicity of the circuit, as well as it's ability to reject most non-idealities in the active components are its primary merits.

The operation of the circuit is very straight forward. The magnitude of the photocurrents flowing from each photosensor will be linearly dependent on the light exposure of the photosensor in question. In particular, parasitic phototransistors are used because of their inherent current gain. The photocurrent which results can be expressed as

$$I_{photo(n)} = \frac{G_T A \eta q P_{opt(n)}}{h f} \tag{1.3.1}$$

where G_T is transistor gain, η is the phototransistor's quantum efficiency (typically about 50%), A is the area of the photodetector, q is the electronic charge, $P_{opt(n)}$ is the light flux incident on detector n, h is Planck's constant, and f is the frequency of the incident

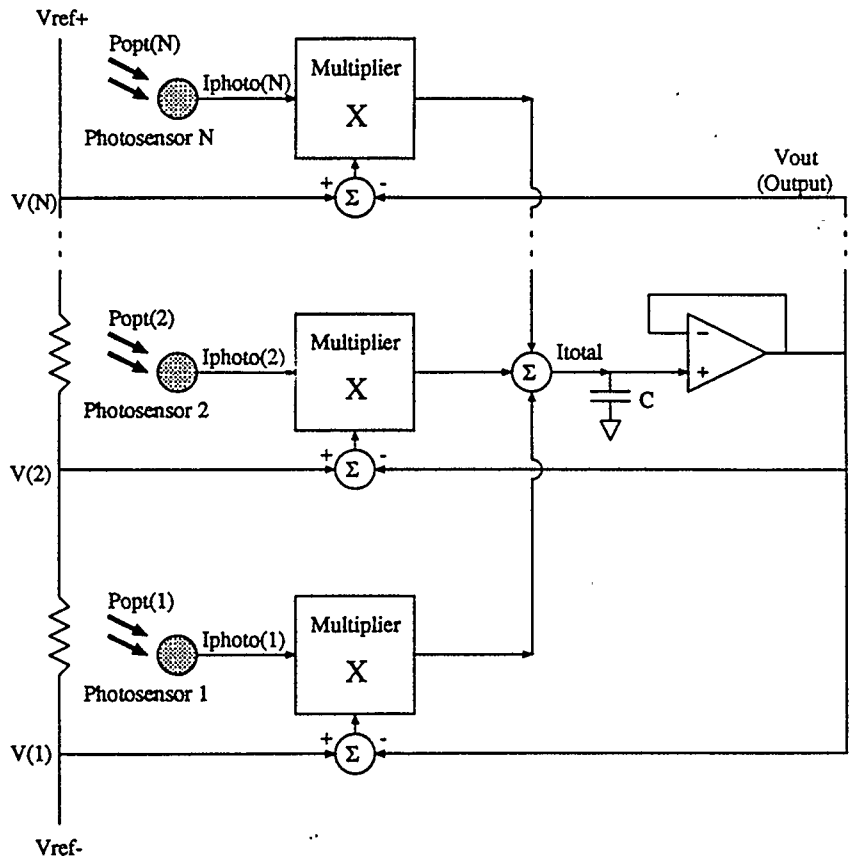

Figure 1.3 - Block diagram of the existing basic position sensor [3].

light. The response of such a phototransistor is typically 2nA/μW/cm^2 for white light for the Northern Telecom CMOS3DLM process with no special processing [3].

The linearly varying reference chain voltages $V_{(1)}$ through $V_{(N)}$ represent the position of the associated photodetectors and the differential voltage between these references and the centroid output voltage provides a weighting for the related photocurrents. The weighted photocurrents are then summed on a capacitor and through negative feedback, the sum of these weighted currents will be reduced to zero.

Ideally, and under these static conditions

$$\sum I = K \cdot \sum_{n=1}^{N} I_{photo(n)} \cdot (V(n) - V_{out}) = 0 \tag{1.3.2}$$

where K is the multiplier gain coefficient (assumed to be equal for all multipliers) and N is the total number of sensors in the system. Solving (1.3.2) for V_{out} results in

$$V_{out} = \frac{\sum_{n=1}^{N} I_{photo(n)} \cdot V(n)}{\sum_{n=1}^{N} I_{photo(n)}} \tag{1.3.3}$$

which can be seen to be analogous to (1.2.3) and thus V_{out} is a measure of the centroid position of the light incident on the photosensors.

To complete the analogy with the mechanical centroid, the photocurrents flowing from the photosensors can be thought of as discrete masses at the position referenced by a particular photosensor's reference voltage. The arbitrary origin from which these reference positions are measured (and hence where the centroid is measured) is entirely controlled by the voltages at the ends of the resistor chain. Typically the voltages at the ends of the reference chain are equal but of opposite sign so that the origin lies at the centre of the array of photosensors.

Since this system is based on negative feedback, it will require some amount of settling time. To get a measure of this settling time, measurements were made of the step response of the circuit [3]. These measurements revealed that the response was

exponential, with a time constant

$$\tau = \frac{C}{K \sum_{n=1}^{N} I_{photo(n)}} \tag{1.3.4}$$

which can be seen to be inversely proportional to the intensity of the incident light source. In practice, the size of the output capacitor, C, may be reduced so that this response is very rapid for most reasonable light intensities.

1.4 Light Sources

It is important to have a model of light sources so that theoretical evaluations can be carried out. The model used throughout this thesis arises from the fact that point light sources are usually not exactly that. They have some distribution which, under sufficient magnification perhaps, will reveal them to be diffused spots, or to have fuzzy edges. It has been found that most of these light sources have intensity profile distributions which may be modeled quite accurately by gaussian curves. In this way, a light source's continuous intensity profile can be described by

$$I_{photo}(X) = I_{pmax} \cdot e^{-\frac{(X - \mu)^2}{2\sigma^2}} \tag{1.4.1}$$

where σ is the standard deviation of the source (normalized to the width of the position sensor's photoarray) and μ is the centre of the distribution or "peak" where I_{photo} is at a

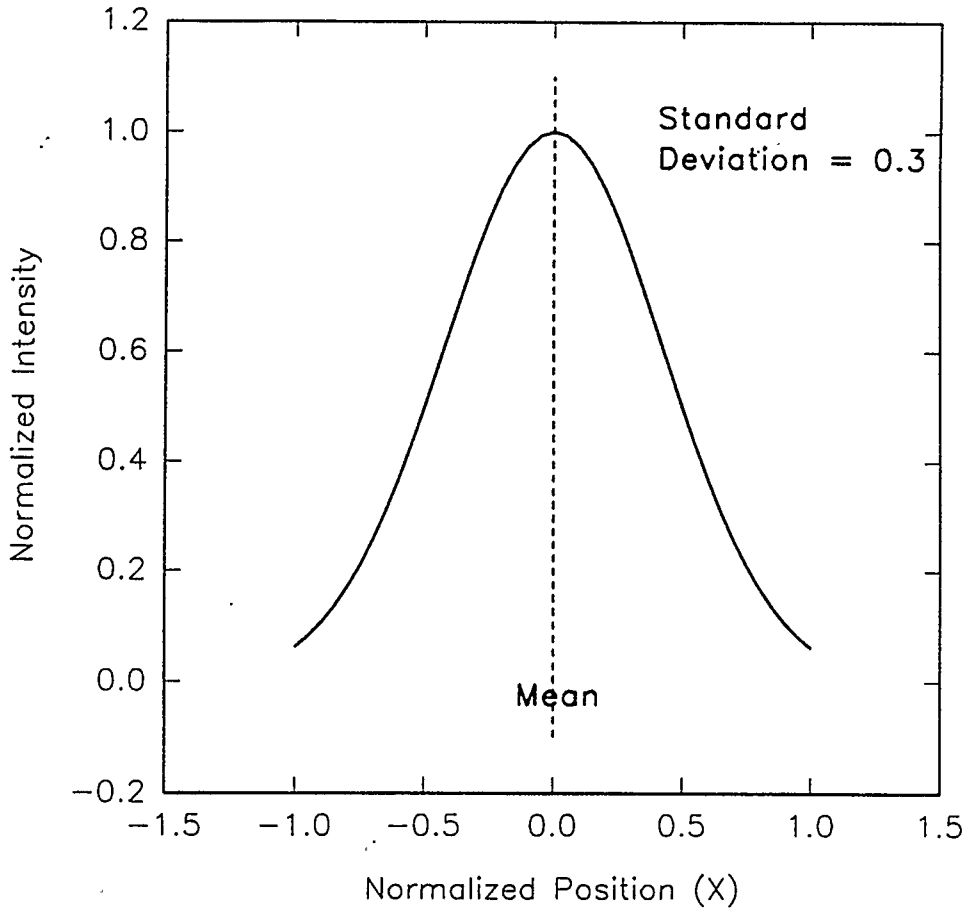

Figure 1.4 - Typical gaussian model of a light source intensity profile.

maximum (I_{pmax}) as shown in Fig. 1.4. Here, Intensity is normalized to I_{pmax} and position is normalized to the width of the detector array in the figure. Note that both μ and X are measured from the same arbitrary origin in the figure.

1.5 Theoretical Response

The voltages along the resistor chain previously shown in Fig. 1.3 can be described by

$$V(n) = \frac{V_{REF} \cdot n}{(N-1)} \tag{1.5.1}$$

where $\pm V_{REF}$ are as shown in the figure; equal but of opposite sign.

When Eqns. (1.3.3), (1.4.1) and (1.5.1) are combined, and if X=0 is taken to be the centre of the array, the equation describing the output voltage takes the form

$$\frac{V_{out}}{V_{REF}} = \frac{\sum_{n=-(N-1)}^{n=(N-1)} e^{-\frac{(n/[2(N-1)] - x)^2}{2\sigma^2}} n/(N-1)}{\sum_{n=-(N-1)}^{n=(N-1)} e^{-\frac{(n/[2(N-1)] - x)^2}{2\sigma^2}}} \tag{1.5.2}$$

where n = -(N-1), -(N-1)+2, -(N-1)+4, ... (N-1) and x is the normalized position of the peak of the gaussian distribution modeled light source relative to the arbitrary origin selected by the resistor chain reference voltages. It is important to note that this transfer function is independent of source intensity, but is still dependent on the standard deviation of the light source. Fig. 1.5 shows the family of curves resulting from various standard deviations of light sources and peak positions.

Eqn. (1.5.2) is dependent upon the standard deviation of the light source because the entire source distribution can not always be present upon the finite sized sensor array. The circuitry will still correctly determine the position of the centroid, but only of the light that is incident upon it. It cannot take measurements of light it cannot see.

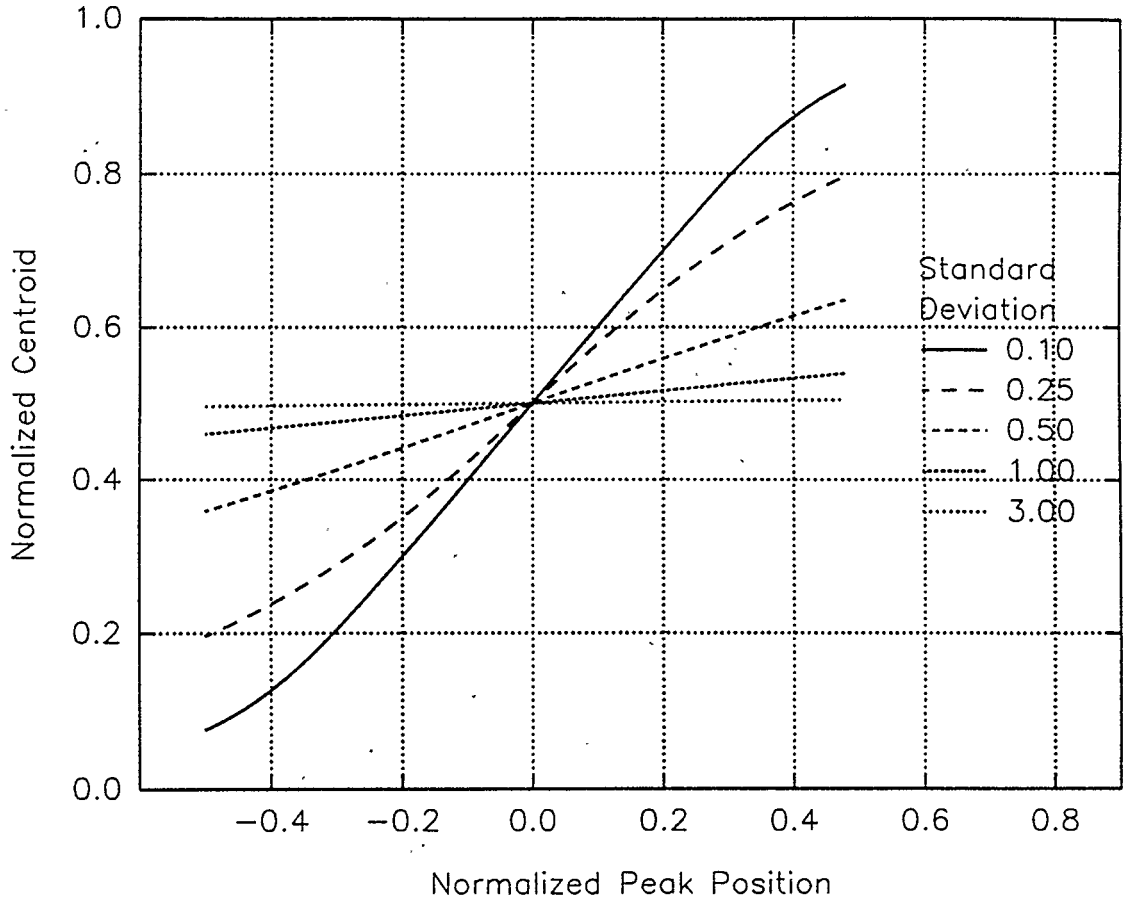

Figure 1.5 - Theoretical centroid position as a function of peak position.

The resulting reduction of output voltage swing with large standard deviation light sources is best described by referring back to the mechanical centroid representation. When larger standard deviation distributions of mass are encountered and the peak of the distribution is moved from one side of the support to the other, the bulk of the mass remains unchanged in position as seen in Fig. 1.6. In the figure, the hatched region represents mass that will always be present for any position of the example distribution. This large, stationary mass swamps the effect of the smaller moving mass on the centroid

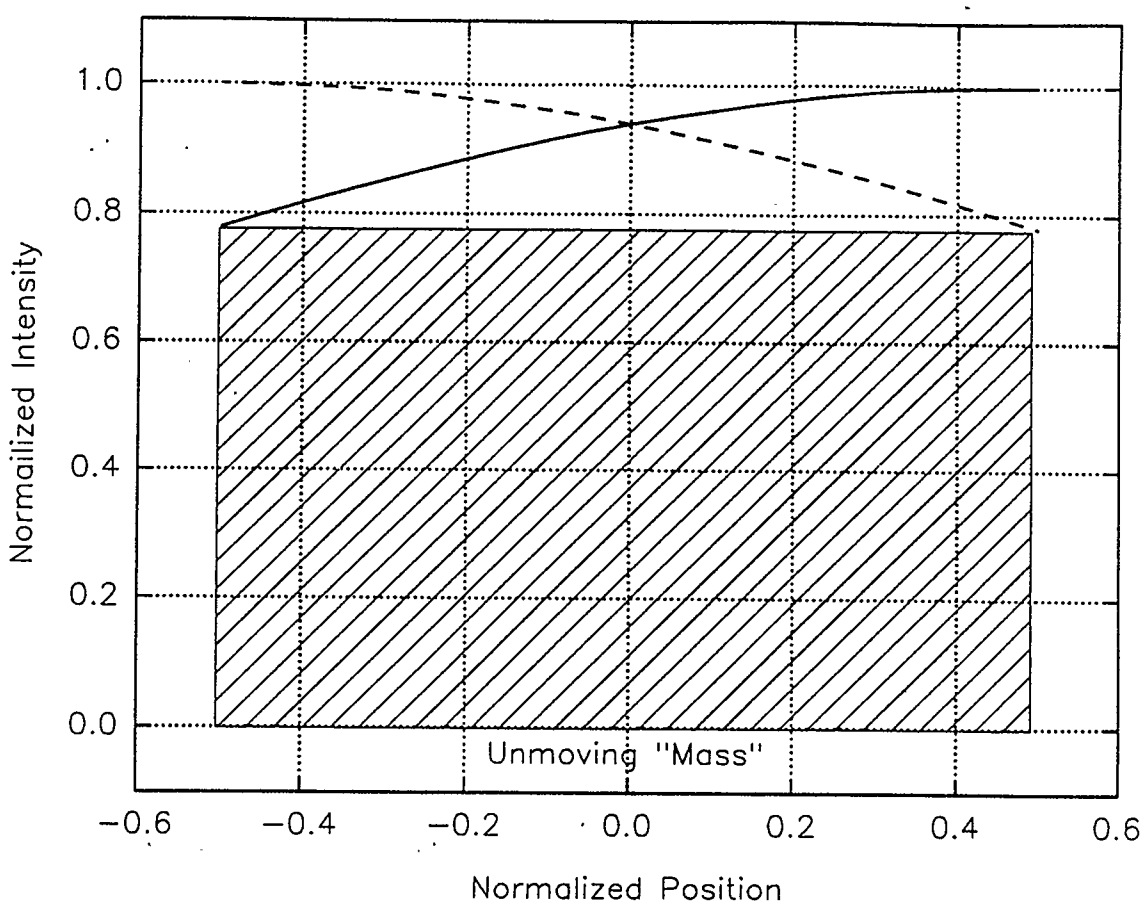

Figure 1.6 - Unchanging portion of light distributions.

position, and as a result the full scale centroid motion (and hence output voltage) is reduced. The larger the distribution's σ, the smaller the moving mass, and the greater the reduction of full scale swing.

1.6 A Practical Realization

The most important part of the position sensing circuitry is the multiplier used for weighting the photocurrents. Poorly designed or overdriven multipliers will have degrading effects upon the overall circuit performance (see Appendix B).

When a discrete component version of the OPS circuit was built, it was decided that RCA CA3280 linearized operational transconductance amplifiers (LOTA) would be used to perform the task of multiplication [3]. This component is very well suited to multiplication of a differential voltage (which may be bipolar), and a positive current (flowing into the LOTA), with the resultant current being both linear and predictable. The practical circuit, equivalent to the block diagram shown in Fig. 1.3, may be seen in Fig. 1.7. To first order (a full analysis of the CA3280 appears in appendix A), the transfer function of the LOTA (consisting of a non-linear OTA that has been linearized by an input section consisting of the diodes and current mirrors of Fig. 1.8) can be shown to act as a two quadrant multiplier and can then be described by

$$I_{out} = K\, I_B\, (V^+ - V^-) \tag{1.6.1}$$

where

$$K = \frac{1}{2\, I_L\, R}\ , \tag{1.6.2}$$

I_B is the differential pair bias current supplied by the photosensors, I_L is the constant linearizing current, and V^+,V^- and R are as given in the figure. Thus K is the multiplier gain coefficient mentioned in Eqn. (1.3.2) and as long as K is the same for all multipliers,

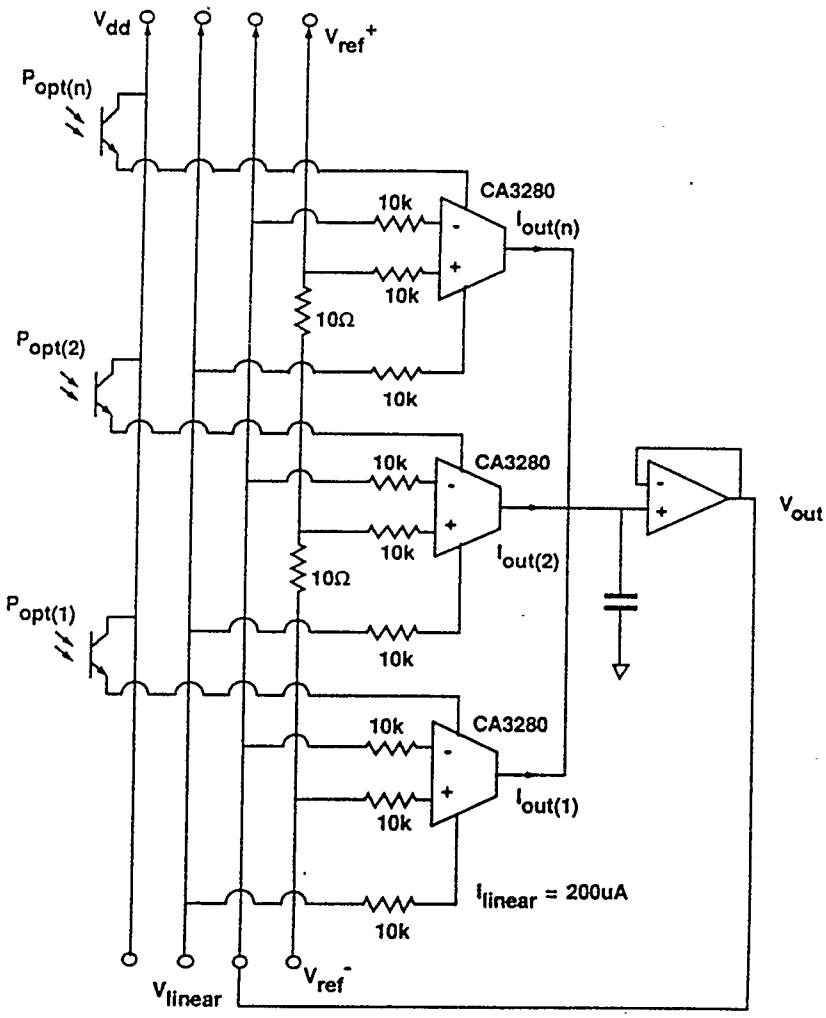

Figure 1.7 - A practical realization of figure 1.3.

it's value, to first order, is irrelevant. (Appendix B describes how K is relevant during circuit design).

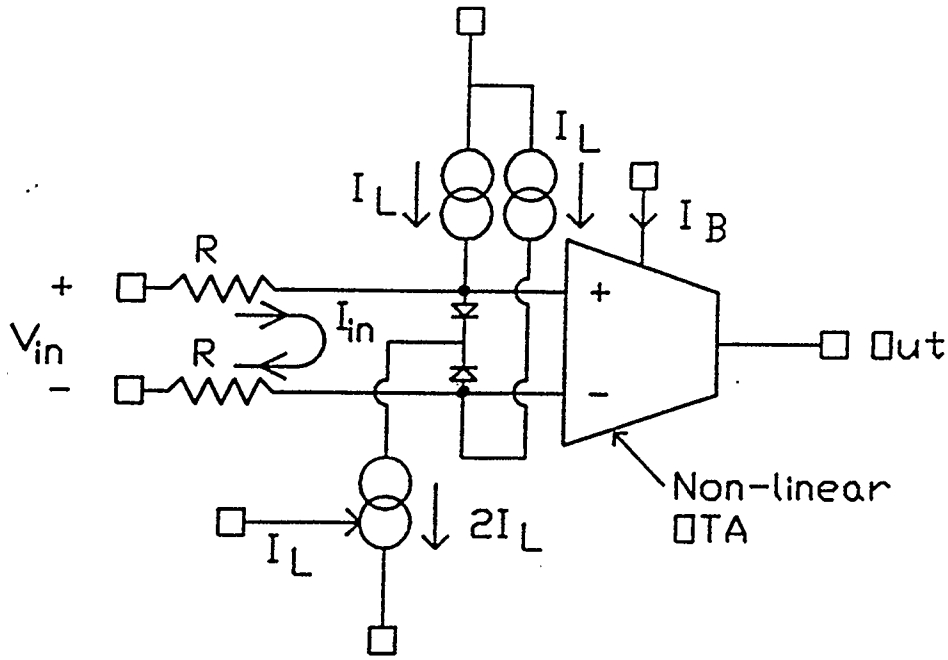

Figure 1.8 - Simplified Linearized Operational Transconductance Amplifier.

1.7 Conclusions

While the basic position sensor has been fully characterized and has been observed to behave in a nearly ideal way [3], it still has some obvious drawbacks. One commonly occurring problem is that while the output signal is, to first order, independent of the light source's intensity, it is still very much dependent upon light source standard deviation. This means that different light sources will stimulate the position sensor to behave in different ways resulting in different output signals for different light sources, which may impair the sensor's use. This thesis describes a method by which this problem may be reduced or, in certain cases completely resolved.

A fully commercial part version of the position sensor is also presented. The purpose of this extension to the basic sensor is twofold. Firstly, it reduces the cost of a complete system by removing all custom VLSI integrated components and relies entirely upon readily available commercial parts, and secondly, it increases the designer's control over some non-ideal second order effects such as the loss of output swing due to low light levels by allowing photocurrent integration.

Finally, a circuit designed to use the optical position sensor for astronomical telescope tracking during long duration astrophotography is presented. Such a use provides information on circuit design using the OPS and reveals some of its shortcomings.

Chapter 2

Source Shape Insensitivity

2.1 Cause of Source Shape Variance

The shape of light sources encountered in any position sensing scheme can vary dramatically. In particular, the amount of spreading (or standard deviation if the source is modeled as a gaussian distribution as in chapter 1) of a point light source may vary by orders of magnitude. This "spreading" of the source has been shown to have a very pronounced effect on the output of the centroid sensing circuitry. The dependence of the ideal output signal (Eqn. (1.5.2)) on the standard deviation of the incident light source results in a reduction of the full scale output at higher standard deviations. This does not mean that there is anything wrong with the centroid circuitry itself. In fact, the true centroid position of the incident light, and hence the output signal, will shift less when a very wide light source is moved across the sensor array than it will with a very narrow

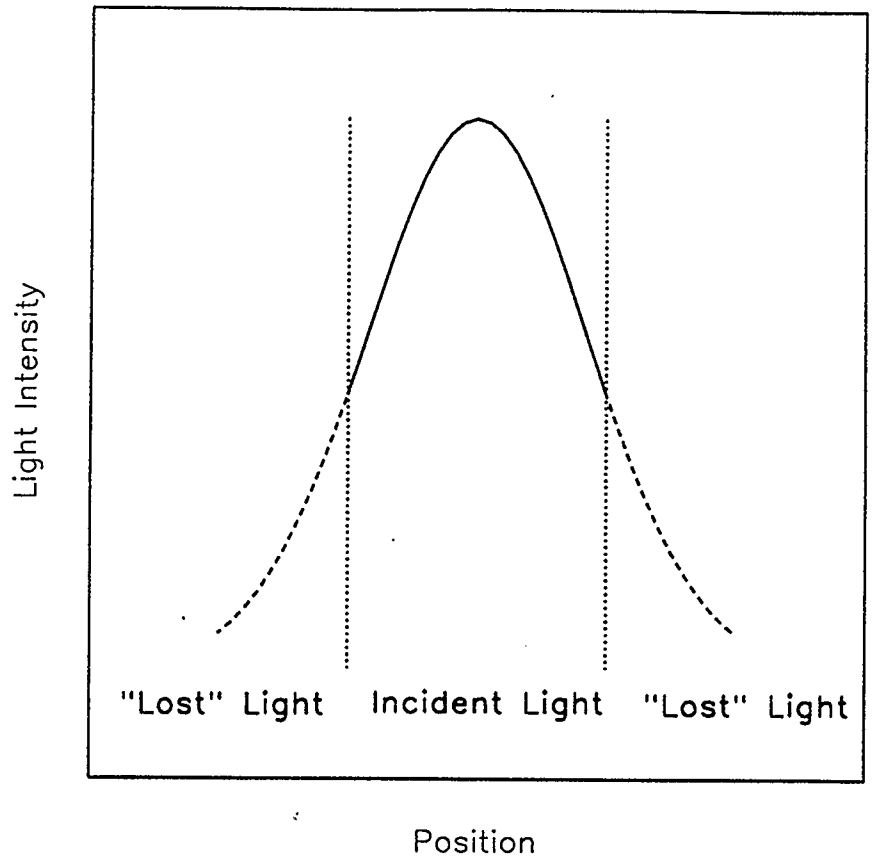

Figure 2.1 - Light being lost off the edges of the array.

source due to the edges of the light distribution being lost off the edges of the photoarray as shown in Fig. 2.1.

Analytically, the output signal may be expressed as in section 1.5 where Eqn. (1.5.2) indicates that the normalized output position, V_{out}/V_{REF}, is to first order independent of the light source intensity, I_{pmax}, but remains dependent upon the light source standard deviation. The theoretical light distributions shown in Fig. 2.2 have been used to demonstrate this dependence by plotting Eqn. (1.5.2) with the peak of

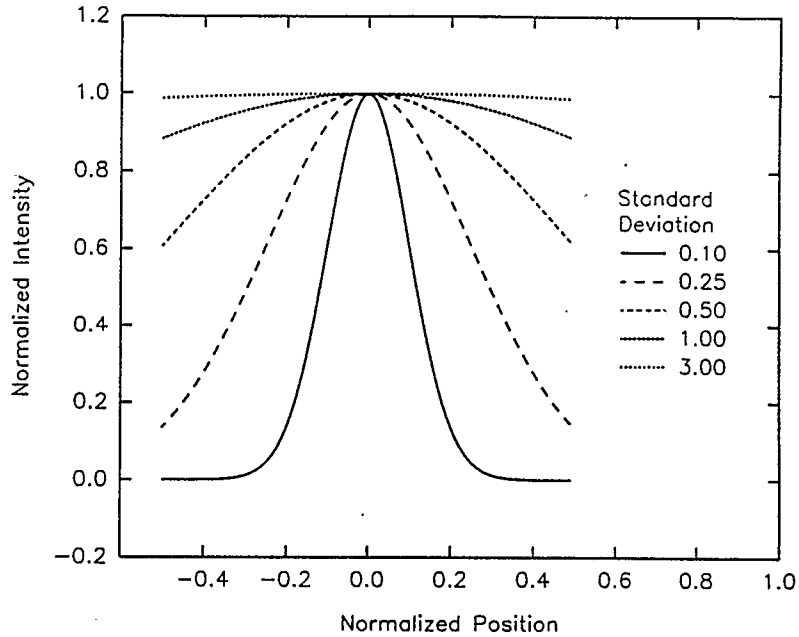

Figure 2.2 - Typical light profiles with varying standard deviations.

the distributions being swept from one end of the photoarray to the other. These plots can be seen in Fig. 1.5.

2.2 Solutions

What is generally desired is peak detection, not centroid detection. The centroid of a light source and its peak will only coincide if the distribution is symmetrical about the peak, as with our light model, and all the light from the source is present upon the finite sized OPS, or at least all light down to a negligible amount. In order to achieve this, correction circuitry can be added between the photosensors and the OPS circuit to

reduce each current flowing from a photosensor by a certain amount (analogous to removing that large, stationary mass described in section 1.5), and by truncating resulting negative currents, if they arise, to zero. The resulting corrected light distribution while no longer gaussian (really a truncated gaussian as shown in Fig. 2.3) fills the

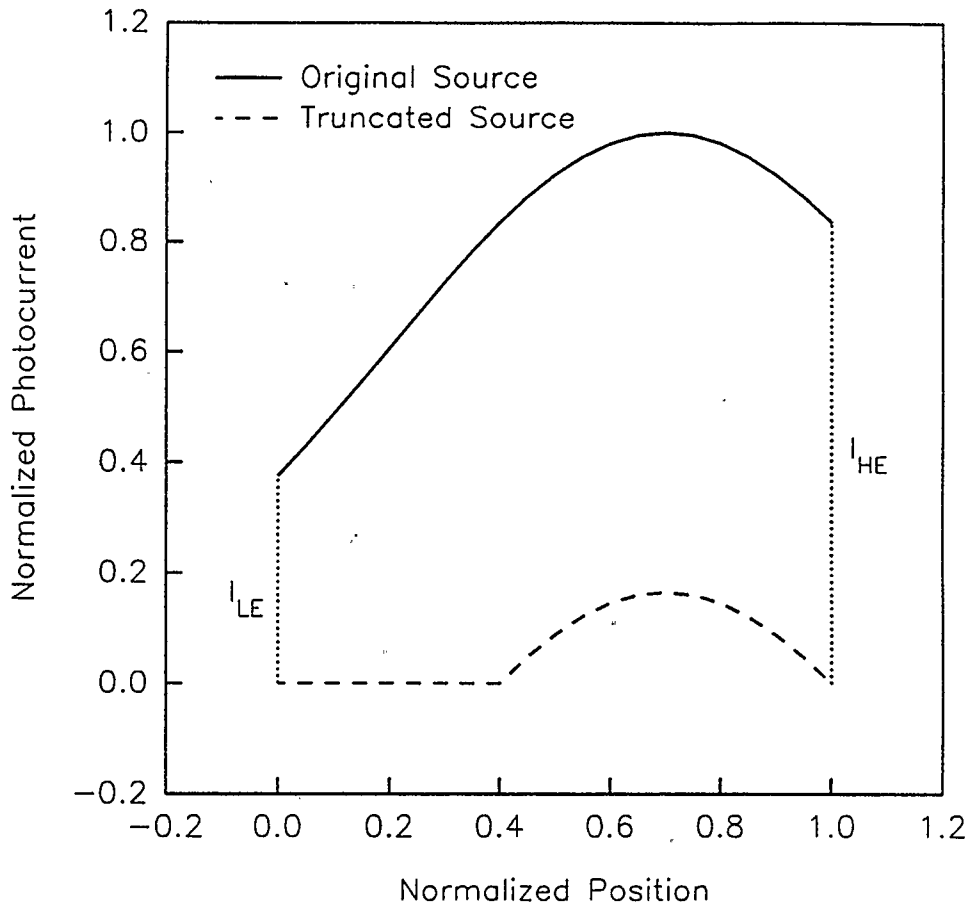

Figure 2.3 - A truncated gaussian distribution.

requirements for peak detection. The proper amount of current to subtract from each photocurrent can be seen to be at least the larger of the two end of array currents. This correction entails comparing the photocurrents at either end of the sensor array, and

subtracting the larger of the two from all photocurrents. Furthermore, because the intensity of the light source doesn't affect the OPS output, subtracting an equivalent correction current from each photocurrent, thereby reducing each photosensor's effective light intensity impacts only the effective standard deviation of the light source and nothing else. However, this technique is not without its drawbacks as will be shown later.

2.3 Theory

With the incident light source profile modeled as a gaussian distribution (Eqn. (1.4.1)), it can be seen that, if the larger of the two photocurrents at either end of the photoarray is removed from all photocurrents, then, as the peak of the light source approaches either end of the array, all photocurrents will be reduced to zero, and the desired peak detection will not result. The array will behave as if in total darkness. For this reason, we will look not only at removing the larger of the two end photocurrents of the array, but will also look at the removal an arbitrary amount of current anywhere between the highest and lowest photocurrents and the removal of the lower of the two end detector photocurrents. As with most things, in theory, removal of either the highest or lowest currents have both merits and drawbacks as will be seen later.

2.3.1 Removal of an Arbitrary Current

The highest end current will always be found at the array edge nearest to the source peak and can therefore always be represented by

$$I_{HE} = I_{pmax}\, e^{-\left(\frac{(0.5 - |x|)^2}{2\sigma^2}\right)} . \tag{2.3.1}$$

Similarly, the lower of the two end of array photocurrents will always be at end of the array that is farthest from the source peak and can be expressed as

$$I_{LE} = I_{pmax}\, e^{-\left(\frac{(0.5 + |x|)^2}{2\sigma^2}\right)} . \tag{2.3.2}$$

An arbitrary amount of current between these two values can therefore expressed as

$$\frac{I_{arb}}{I_{pmax}} = I_{LE} + \alpha\left[I_{HE} - I_{LE}\right] \tag{2.3.3}$$

where α is the coefficient with a range from 0.0 to 1.0 which controls the exact size of I_{arb}. If this current is then subtracted from each photocurrent before entering the OPS the corrected OPS static response can then be shown to be

$$\frac{V_{out}}{V_{REF}} = \frac{\sum_{n=-(N-1)}^{(N-1)} \left(e^{-\frac{(n/[2(N-1)] - x)^2}{2\sigma^2}} - \frac{I_{arb}}{I_{pmax}} \right) \cdot \frac{n}{(N-1)}}{\sum_{n=-(N-1)}^{(N-1)} \left(e^{-\frac{(n/[2(N-1)] - x)^2}{2\sigma^2}} - \frac{I_{arb}}{I_{pmax}} \right)} . \tag{2.3.4}$$

For the case when σ is >> 1, the combination of Eqns. (2.3.3) and (2.3.4) can be

rewritten using a second order Maclaurin series expansion to be

$$\frac{V_{out}}{V_{REF}} \approx \frac{\sum_{n=-(N-1)}^{n=(N-1)} \left[\frac{n^2}{4(N-1)^2} - \frac{1}{4} - |x| \left(2\alpha - 1 + \frac{n}{(N-1)} \right) \right] \frac{n}{(N-1)}}{\sum_{n=-(N-1)}^{n=(N-1)} \left[\frac{N^2}{4(N-1)^2} - \frac{1}{4} - |x| \left(2\alpha - 1 + \frac{n}{(N-1)} \right) \right]} \quad (2.3.5)$$

which is independent of σ as desired. However, it is important to clip the quantities in brackets to zero should they become negative.

2.3.2 Removal of Higher End Current

If we correct the photocurrents by allowing α to be 1.0 in Eqn. (2.3.3) and removing this current ($=I_{HE}$) from all others, the static transfer response of the OPS may now be written

$$\frac{V_{out}}{V_{REF}} = \frac{\sum_{n=-(N-1)}^{(N-1)} \left(e^{-\frac{(n/[2(N-1)] - x)^2}{2\sigma^2}} - e^{-\frac{(0.5 - |x|)^2}{2\sigma^2}} \right) \cdot \frac{n}{(N-1)}}{\sum_{n=-(N-1)}^{(N-1)} \left(e^{-\frac{(n/[2(N-1)] - x)^2}{2\sigma^2}} - e^{-\frac{(0.5 - |x|)^2}{2\sigma^2}} \right)} . \quad (2.3.6)$$

However, this equation does not reflect the effect of clipping the currents such that there are no negative currents. This clipping physically results in reducing the width of the array so that it excludes photodetectors whose currents are less than the I_{HE}. Since the corrected, effective, light source is centred around the peak, x, only detectors that fall into the range

$$(2x - 0.5) \leq n/[2(N-1)] \leq 0.5 \tag{2.3.7}$$

when x ≥ 0, and

$$-0.5 \leq n/[2(N-1)] \leq -(2x - 0.5) \tag{2.3.8}$$

when x < 0 and n increments as in chapter 1, will produce currents greater than or equal to I_{HE} and can thus be used in the centroid calculation. This may be expressed completely for x ≥ 0 as

$$\frac{V_{out}}{V_{REF}} = \frac{\sum_{n=(4x-1)(N-1)}^{(N-1)} \left(e^{-\frac{(n/[2(N-1)] - x)^2}{2\sigma^2}} - e^{-\frac{(0.5 - x)^2}{2\sigma^2}} \right) \cdot \frac{n}{(N-1)}}{\sum_{n=(4x-1)(N-1)}^{(N-1)} \left(e^{-\frac{n/[2(N-1)] - x)^2}{2\sigma^2}} - e^{-\frac{(0.5 - x)^2}{2\sigma^2}} \right)} \tag{2.3.9}$$

where the starting value for n must be rounded up to the next value which fits into the counting scheme described earlier. In this form, Eqn. (2.3.9) gives little feeling for the correction, but by simulation this can be seen to be approximated by the equation

$$\frac{V_{out}}{V_{REF}} = x \tag{2.3.10}$$

with the limitation that the set of x may not include the end points -0.5 and 0.5 and N is large. Eqn. (2.3.10) arises from the fact that when the higher end current is subtracted from all currents the resulting distribution is centred about x, resulting in the centroid being defined as the peak, x. When the peak is at the edge of the array however, all currents are reduced to zero, and V_{out}/V_{REF} will subsequently be undefined. Thus, in

theory, removing the higher end current from all other currents results in peak detection for all light source peak positions in the array excluding distributions centred over the array endpoints.

However, when the source becomes very wide (ie. large standard deviation), the corrected currents that result will become very small, and variations in the photodetectors will play a larger and larger role, as will any other circuit parameter that is not identical for each current path through the position sensor. For this reason, the removal of the higher end is not necessarily the best solution.

2.3.3 Removal of Lower End Current

If we allow α to become zero in Eqn. (2.3.3) and remove this current from all other photocurrents ($=I_{LE}$), the static transfer response can now be represented by

$$\frac{V_{out}}{V_{REF}} = \frac{\sum_{n=-(N-1)}^{(N-1)} \left(e^{-\frac{(n/[2(N-1)] - x)^2}{2\sigma^2}} - e^{-\frac{(0.5 + |x|)^2}{2\sigma^2}} \right) \cdot \frac{n}{(N-1)}}{\sum_{n=-(N-1)}^{(N-1)} \left(e^{-\frac{(n/[2(N-1)] - x)^2}{2\sigma^2}} - e^{-\frac{(0.5 + |x|)^2}{2\sigma^2}} \right)} \qquad (2.3.11)$$

where everything is as in Eqn. (2.3.6). However, since the current that is being subtracted from all other currents is now the lowest anywhere in the array, the clipping that resulted in previous discontinuities does not arise. Eqn. (2.3.11) is continuous and differentiable at all points. By using a second order Maclaurin series expansion on the exponential

terms of Eqn. (2.3.11), the output then takes the form

$$\frac{V_{out}}{V_{REF}} \approx \frac{\sum_{n=-(N-1)}^{n=(N-1)} \left[\left(\frac{nx}{(N-1)} + |x| \right) + \frac{1}{4} \left(1 - \frac{n^2}{(N-1)^2} \right) \right] \frac{n}{(N-1)}}{\sum_{n=-(N-1)}^{n=(N-1)} \left[\left(\frac{nx}{(N-1)} + |x| \right) + \frac{1}{4} \left(1 - \frac{n^2}{(N-1)^2} \right) \right]} \quad . \qquad (2.3.12)$$

Fig. 2.4 shows plots of both Eqn. (2.3.11) and Eqn. (2.3.12) for comparison purposes. It can be seen that the expansion is a good estimate of the full response when x/σ is small. Under these conditions, higher order terms in the Maclaurin series become negligible after the third term. In this way, the response is made independent of the standard deviation of the light source over the range in the centre of the array where x/σ is small. For larger standard deviations, this range encompasses the entire array.

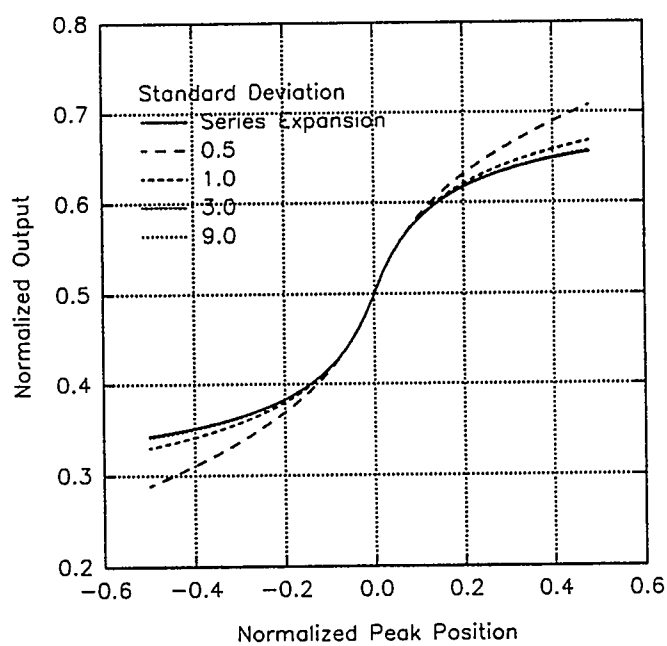

Figure 2.4 - Static transfer response when lower end current is removed.

2.4 Practical Realization

A circuit to perform this current subtraction has been previously built using discrete, bipolar components [4]. However, since the final goal of this line of research is to integrate the photodetectors, standard deviation insensitivity circuitry, and other improvements onto one monolithic integrated circuit, a fully integrated CMOS design and layout was performed. This chip was fabricated using Northern Telecom's 1.2 μm process.

A block diagram of the circuit showing the three basic operational sections capable of handling 14 photocurrent inputs is shown in Fig. 2.5. Each section performs a very simple task. The two input sections, one for either end of array photocurrent, provide the necessary signals to make the comparison of the end of array currents, as well as providing cascode gate voltages to drive slave transistors in each of the fourteen output sections. The switch section uses the comparison information from the input sections to select which end of the array has the higher or lower current (whichever is to be subtracted), and passes the corresponding two control voltages (cascode gate voltages) on to each of the output sections. The current subtraction is performed in the output section, with the resulting current being mirrored to the circuit outputs. Each segment will be discussed in detail.

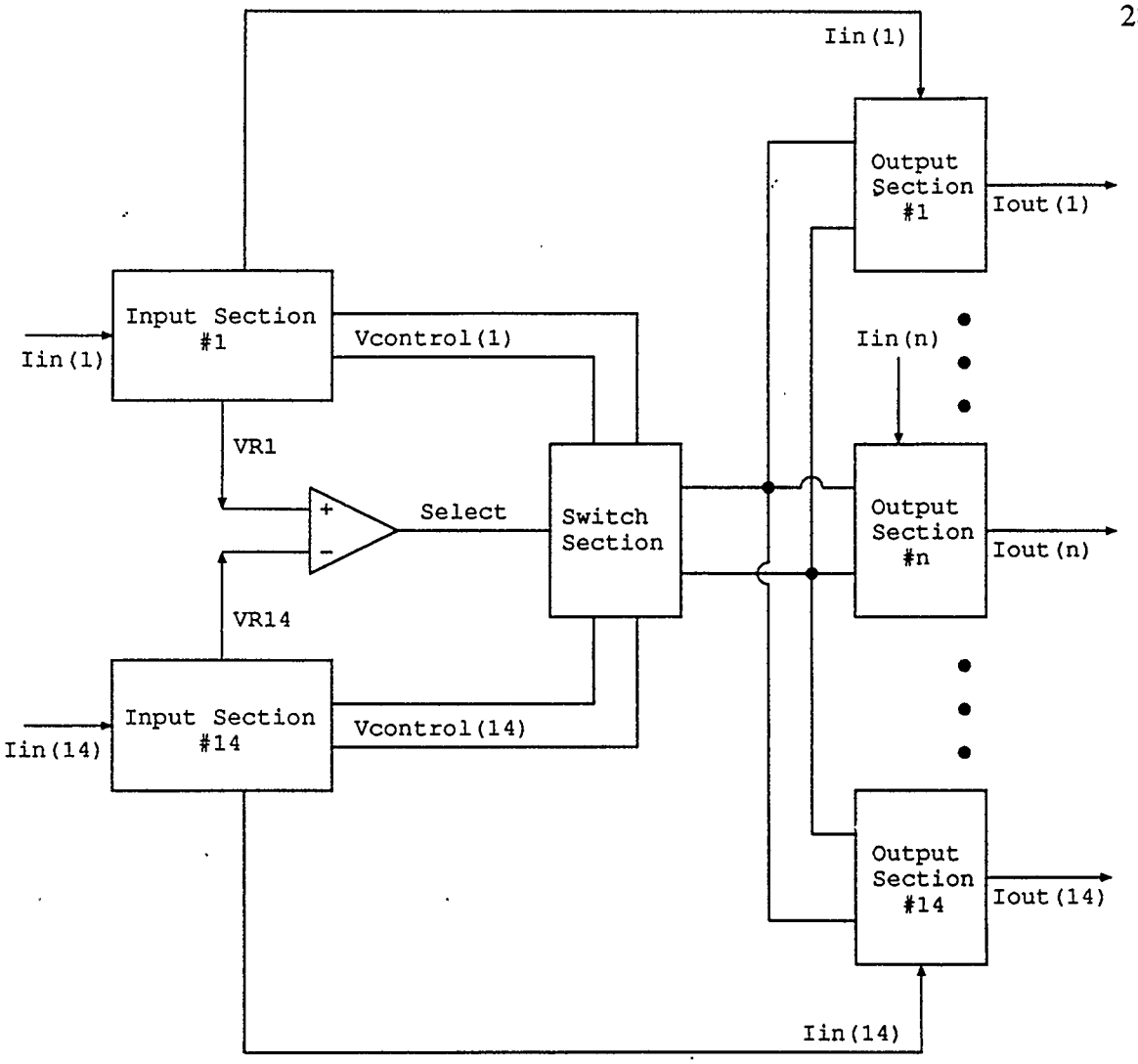

Figure 2.5 - Block diagram of correction circuitry.

2.4.1 The Input Sections

As stated earlier, the function of the input section is threefold:

a) to provide input current information in a form suitable for comparison to other, similar, information;

b) to provide control information for current subtraction; and

c) to mirror the input current so it may be treated along with all other input currents.

A circuit which performs all these tasks is shown in Fig. 2.6. Each end of array input current is first mirrored via two diode connected n-channel enhancement transistors in a cascode formation as shown to create two identical "copies" of the input current. By diode connecting the transistors, and hence maintaining $V_{DS}=V_{GS}$ for both M_{I1} and M_{I2}, it is ensured that, for each input transistor, V_{DS} will always be greater than $V_{GS}-V_T$ and the transistors will remain in saturation. If threshold voltage modulation is ignored for the time being (ie. assuming $V_T=V_{TO}$) and channel length modulation is ignored as well (ie. setting $\lambda=0$), the voltage at the lower transistor's gate (V_{LOWER}) and the voltage of the upper transistor's gate (V_{UPPER}) with respect to ground can be shown to be

$$V_{LOWER} = \sqrt{\frac{2\, I_{in}\, L_2}{\beta\, W_2}} + V_T \tag{2.4.1}$$

and

$$V_{UPPER} = 2\, V_{LOWER} = \sqrt{\frac{8\, I_{in}\, L_2}{\beta\, W_2}} + 2V_T \tag{2.4.2}$$

respectively, provided that both transistors have the same width to length ratio W/L. These voltages, while providing the means for mirroring currents within the input section, also act as control voltages to mirror the input current in the output sections of the circuit.

The first internally mirrored current will be passed through a resistor which is connected to the positive power supply. The voltage at the output of this mirror will be

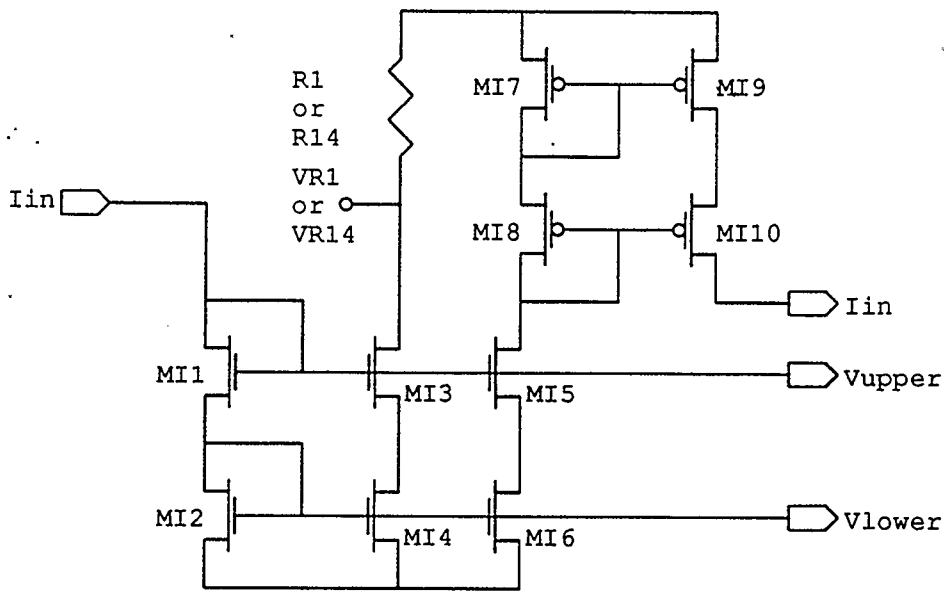

Figure 2.6 - The input section.

linearly related to the input current by the equation

$$V_{R1} = V_{DD} - I_{R1} R_1 \quad . \tag{2.4.3}$$

These voltages, one for either end of the array (V_{R1} and V_{R14}), may then easily be compared by a comparator to decide which of the two end of array currents is either larger or smaller, depending upon which type of correction is desired and the orientation of the comparator. The resulting comparator output, taken as a digital signal, will control which of the two sets of end of array cascode control voltages are passed on to the output stages via the switch section as an indication of the amount of current to be subtracted from each input current.

The second of the internally mirrored currents will simply be mirrored once again

and supplied to the corresponding end of array output stage. By doing so, we are using the end of array input currents to make comparisons, and create other signals without affecting their final use.

Because the n-channel devices in the input sections are to form current mirrors with transistors in the output sections, their sizing depends upon circuit parameters and design criteria in the output sections. For this reason their sizes will be determined and discussed along with the output sections. The p-channel transistors in the input sections, however, were simply sized so that voltages at the inputs of the p-type mirrors would not interfere with the voltages at the outputs of the n-type mirrors (node 1) by forcing the n-channel devices out of saturation. This constraint results in

$$\frac{L_p}{W_p} \leq \beta_p \left(\frac{\frac{V_{DD}}{2} - \frac{V_{TN}}{2} - V_{TP}}{\sqrt{I_{in}^{\max}}} - \sqrt{\frac{L_n}{W_n \beta_n}} \right)^2 \tag{2.4.4}$$

where β_p and β_n are the p and n-channel transconductances, respectively, V_{TP} and V_{TN} are the p and n-channel threshold voltages, respectively, V_{DD} is the upper power supply voltage, W_n/L_n and W_p/L_p are the n and p channel width to length ratios, respectively, and I_{in}^{max} is the maximum expected input current to the input stages.

Input section n-channel devices	40/3
Input section p-channel devices	80/3

Table 2.1 - Input section transistor sizes (W/L in microns).

In this way, the input circuitry provides for each of the three necessary functions by, a) converting the input current to a voltage by passing it through a resistance so that the two end of array currents may be easily compared, b) passing the cascode mirror gate voltages on to the switching section, thus supplying control information to the output stages indicating the amount of current to be subtracted, and c) mirroring the input current in such a way that it can be passed on to the corresponding output stage for later processing.

2.4.2 The Switching Sections

Two of the signals made available by each of the two input stages are used by the switching section. These are the cascode mirror gate voltages as in Eqns. (2.4.1) and (2.4.2), and the comparison voltages V_{R1} and V_{R14}.

For this design, the comparison of voltages V_{R1} and V_{R14} is performed by an external commercial comparator. For the best possible comparison, a low offset voltage operational amplifier should be used. This ensures that the switching of the selection from one end of the array to the other is performed as closely as possible to the centre

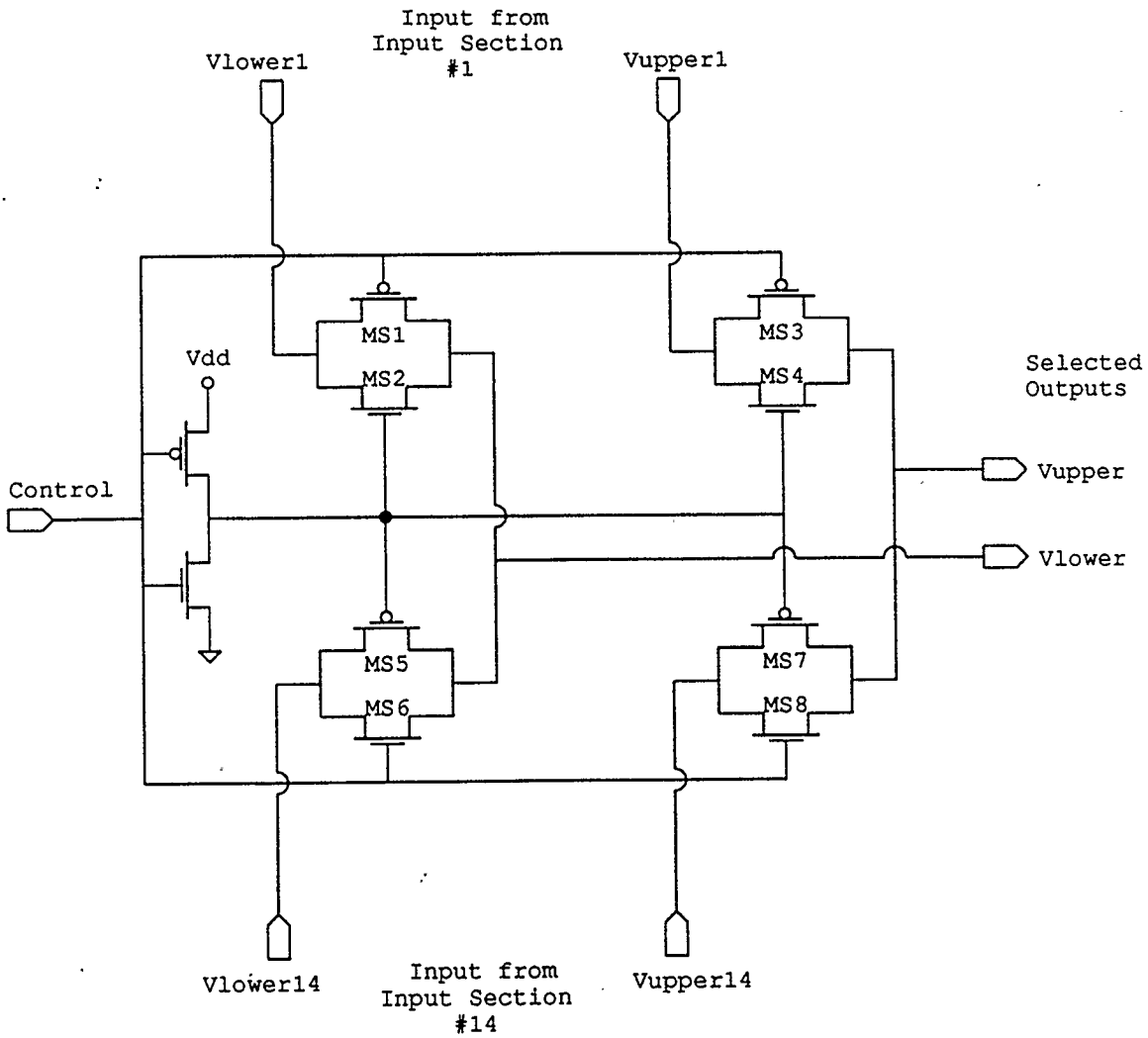

Figure 2.7 - The switching section.

of the array when a symmetrical source is applied to the photoarray.

The comparator's output is, as stated earlier, treated as a digital signal to control four on-board transmission gates as shown in Fig. 2.7, to select which of the two sets of cascode gate voltages should be passed on to the output sections. In the schematic shown when the control signal is high ($=V_{DD}$) the current from Input #14 is selected as the current to be subtracted.

Transmission gates are perhaps the only CMOS analogue circuit elements that can be counted on to perform very nearly ideally. Their performance is independent of most CMOS circuit parameters like threshold voltages and modulation, channel length modulation, and transistor transconductance. Because threshold voltage modulation is not a problem, it is important to connect the substrates for all transmission gate transistors to either the positive or negative supplies for p-type and n-type transistors, respectively. This will ensure that latch-up, the state when a parasitic diode internal to the switching transistors becomes forward biased, is avoided and does not affect circuit operation. In particular, if a p-channel transistor's source and substrate are connected, and the output of the transmission gate remains high due to output capacitances as the input (and the transistor's substrate) falls, the drain substrate pn junction will become forward biased and latch-up occurs. With the n-well substrate connected to the positive supply, this state can never occur.

Because no current is expected to flow through these switches at steady state (very small amounts will flow during switching) they can be made very nearly as small as the technology will allow. These sizes are shown in Table 2.2.

Switching section n-channel device size	3/3
Switching section p-channel device size	3/3

Table 2.2 - Switching section transistor sizes (W/L in microns).

2.4.3 The Output Sections

The heart of the correction circuit is the output section as shown in Fig. 2.8. It is here that the current subtraction is performed, and the resulting corrected currents are mirrored to isolate them from any conditions at the output pins. It is also here where design criteria become most critical in order to perform the best possible subtraction.

Transistors M_{I1} and M_{I2} from the selected input section have gate voltages as described by Eqns. (2.4.1) and (2.4.2) which will be passed through the switching section. These voltages, when applied to the gates of two transistors of similar dimension, will form a cascode mirror and will drive the transistors in the output section to draw the selected input current. There are, however, limitations to this mirroring action. In order for the correct current to be drawn, both of the output stage transistors, M_{O1} and M_{O2} must remain in a saturated state. Fig. 2.9 shows the result of allowing the drain voltage of M_{O1} to drop. A lower limit for this drain voltage (V_1) can be calculated.

Ignoring for the moment the effects of channel length and threshold voltage modulations, for both M_{O1} and M_{O2} to remain saturated, by definition,

$$V_1 \geq V_2 - V_T \tag{2.4.5}$$

must apply for M_{O1} and

$$V_4 \geq V_3 - V_T \tag{2.4.6}$$

for M_{O2}. Hence, if both transistors were saturated to begin with, and V_1 were falling, the transition from the saturation to triode region would occur at

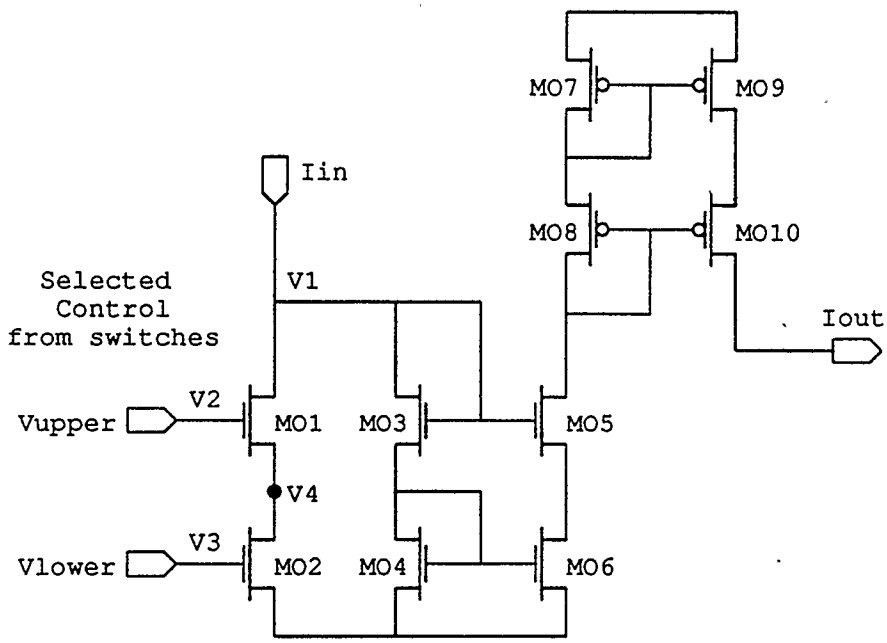

Figure 2.8 - The output section.

$$V_1 = V_2 - V_T \tag{2.4.7}$$

for M_{O1} and

$$V_4 = V_3 - V_T \tag{2.4.8}$$

for M_{O2}. Moreover, since we already have equations for voltages $V_2 = V_{UPPER}$ and $V_3 = V_{LOWER}$ it can be shown that as V_1 drops, M_{O1} will drop out of saturation before M_{O2} and Eqn. (2.4.7) will set a lower limit for V_1, below which M_{O1} will fall out of saturation and the mirroring action will be compromised.

By again referring to Fig. 2.8, it can be seen that the voltage V_1 will be solely controlled by the current flowing through the diode connected transistor pair M_{O3} and

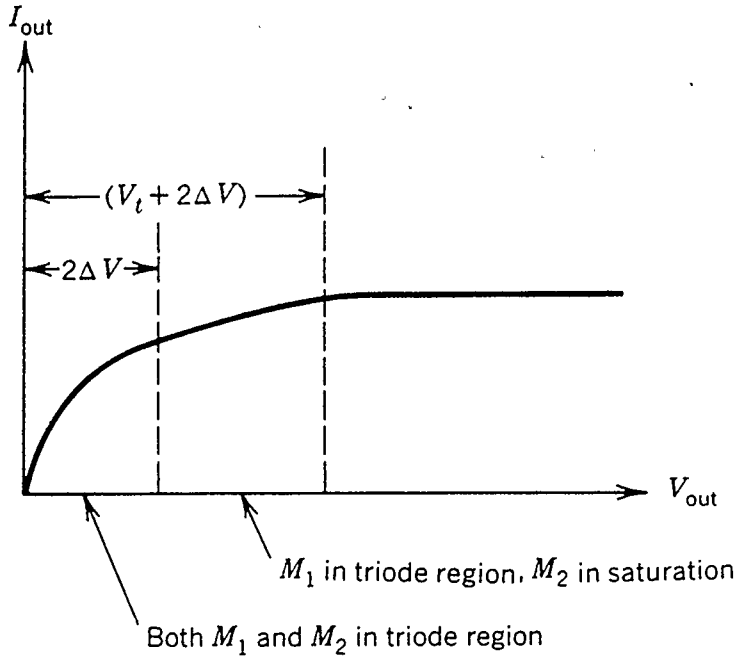

Figure 2.9 - The effect of cascode mirror output voltage on mirror output current. ($\Delta V = V_{LOWER} - V_t$)

M_{O4}. These transistors behave in the same way as M_{I1} and M_{I2}, that is,

$$V_1 = \sqrt{\frac{8\, I_o\, L_3}{W_3\, \beta}} + 2V_T \tag{2.4.9}$$

where I_o is the result of the current subtraction and flows in M_{O3} and M_{O4}.

Here, however, we are only interested in the lower limit of this voltage which, if subthreshold operation is ignored, can be seen to be $V_1 = 2V_T$. Ignoring subthreshold operation is a valid assumption because if any current significantly larger than the transistor "saturation" current I_{DO} (of the order of 10^{-12} amps) is flowing, Eqn. (2.4.9) becomes valid and the size of transistors M_{O1} and M_{O2} can be chosen by using Eqn.

(2.4.7) to find that

$$\frac{W_{12}}{L_{12}} \geq \frac{8\ I_{in}^{max}}{V_T^2\ \beta} \tag{2.4.10}$$

where I_{in}^{max} is the maximum photocurrent expected at any input. For this design the maximum input photocurrent was chosen to 30 μA which, along with the provided fabrication parameters, results in approximately

$$\frac{W_{12}}{L_{12}} \geq 11 \quad . \tag{2.4.11}$$

These sizes, as mentioned earlier, have ramifications in the input circuit. For a current mirror to have unity gain, as desired, all transistors, both driving and slave, must be matched in size. This means that all the n-channel transistors in the input sections must also be sized according to Eqn. (2.4.10).

Output section n-channel transistor size	
M_{O1}, M_{O2}	40/3
M_{O3}, M_{O4}, M_{O5}, M_{O6}	20/3
Output section p-channel transistor sizes	40/3

Table 2.3 - Output section transistor sizes (W/L in microns).

When threshold voltage modulation is taken into account, the lower limit on voltage V_1 is raised to

$$V_1 = 2V_{TO} + \gamma(\sqrt{V_{TO}+2\phi} - \sqrt{2\phi}) \tag{2.4.12}$$

and the voltage V_{UPPER} is raised to

$$V_{UPPER} = \sqrt{\frac{8 I_{in}^{max}}{\beta}\frac{L}{W}} + 2V_{TO} + \gamma(\sqrt{V_{LOWER}+2\phi} - \sqrt{2\phi}) \tag{2.4.13}$$

where V_{TO} is the unmodulated threshold voltage, γ is the body effect factor, 2ϕ is the process surface inversion potential (typically 0.6 volts), and all other parameters are as outlined previously. These equations result in

$$\frac{W}{L} \geq \frac{8\, I_{in}^{max}}{\beta\left[V_{TO}+\gamma\left(\sqrt{V_{TO}+2\phi} - \sqrt{2\phi}\right)\right]^2} \tag{2.4.14}$$

which differs from Eqn. (2.4.10) in that the denominator is slightly larger and accordingly smaller W/L values result. The lower transistors do not suffer from threshold voltage modulation because for these transistors, the source to bulk voltage V_{SB} is always zero.

Actual circuit layouts may be seen in the following Figs. 2.10 through 2.14.

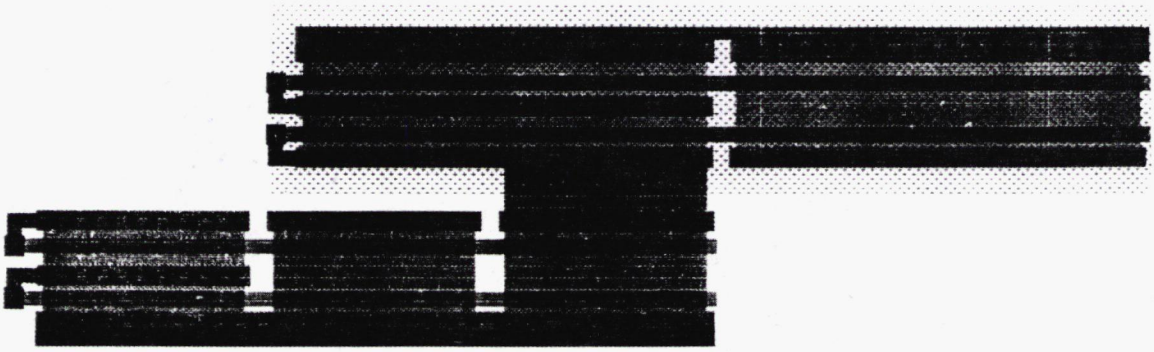

Figure 2.10 - The layout of the input section (1.50 microns/mm).

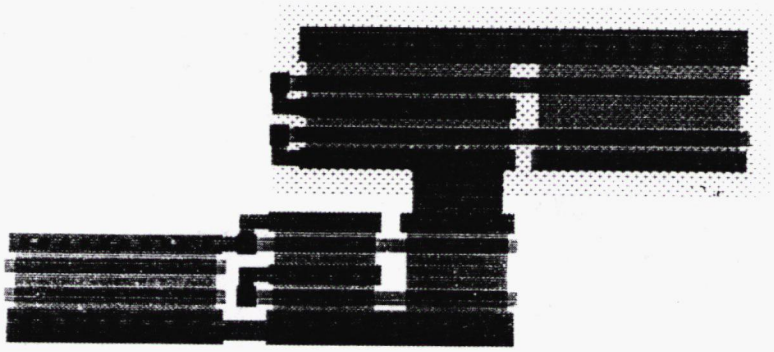

Figure 2.11 - The layout of the output section (1.50 micron/mm).

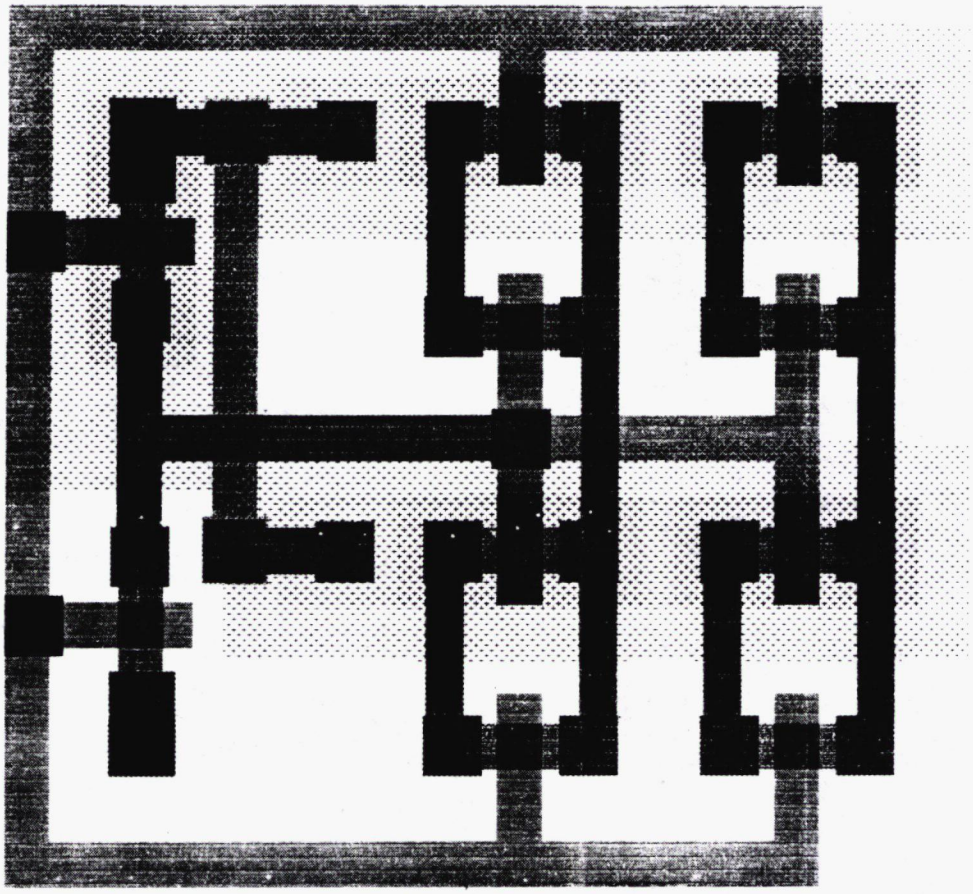

Figure 2.12 - The layout of the switching section (0.5 micron/mm).

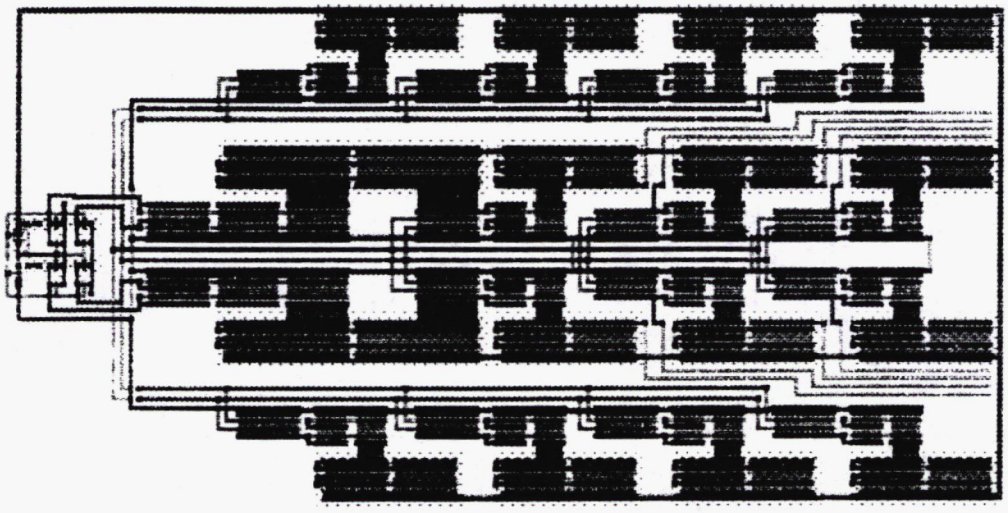

Figure 2.13 - The full circuit (5 micron/mm).

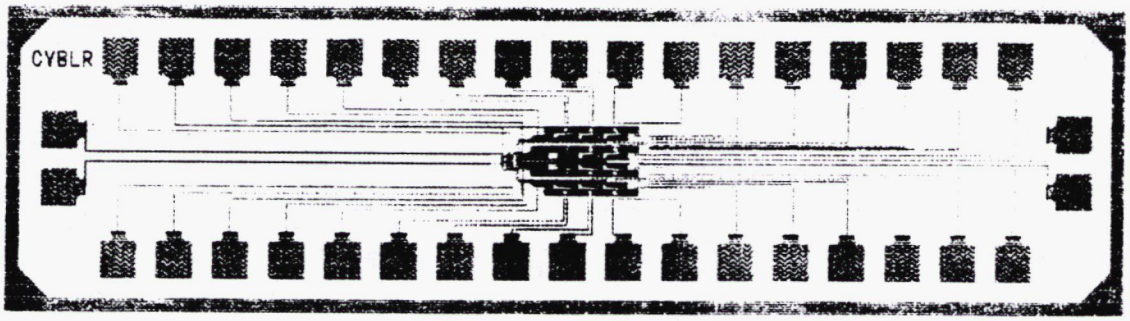

Figure 2.14 - The complete layout (33.3 micron/mm).

2.5 Testing and Results

All testing was done by using an HP semiconductor parameter analyzer to simulate the input currents. While it would have been possible to set up a light source and use the available photoarrays with many more photodetectors than is achievable with the HP, exact control over the standard deviation of the light source would have been very nearly impossible. With the analyzer on the other hand, exact control of all inputs was easily achieved at the cost of a reduced number of photocurrent inputs. The corrected (and uncorrected) photocurrents, were then passed into a discrete component (linear multiplier) centroid sensor built using CA3280 LOTAs as described earlier, to produce the final output. It was observed that the slew rate of the external comparator had no effect on the transient response of the circuit as output capacitor charging times were much larger.

2.5.1 Functionality

The circuit layout was designed in such a way that most of the important internal signals were accessible for measurement. These signals allow for the determination of any flaws in the layout and design that would affect circuit performance.

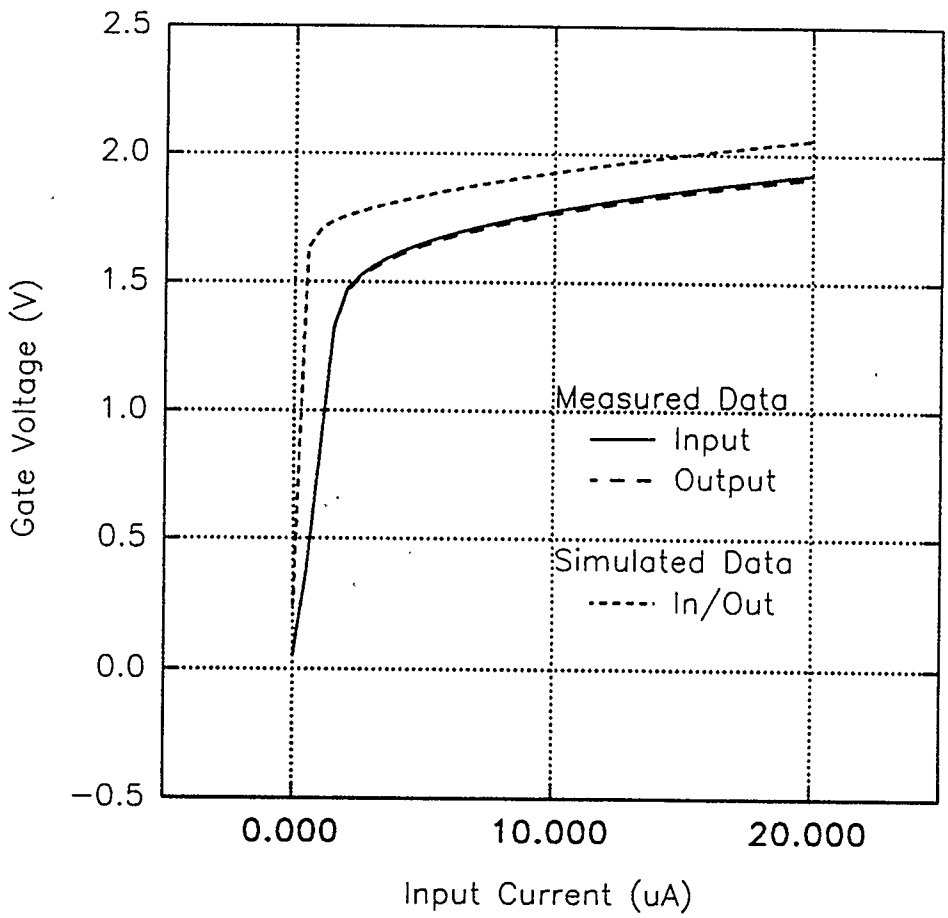

Figure 2.15 - Simulated and measured upper cascode gate voltages.

Fig. 2.15 shows the measured data for V_{UPPER} before entering the transmission gates and after, along with the simulated data for the case when input #1 was the control input. The measured values can be seen to be very nearly identical as would be expected

due to the fact that at steady state, no current will be flowing in the transmission gates, and subsequently there can be no voltage drop across them. The simulated data however differs from the measured data by a significant amount. This can be attributed to using transistor parameter values in the simulations that were not the same as the actual values encountered during testing. The parameters used were those made available by the CMC [5] for level 3 spice simulations. These parameters were stated as being "guidelines only" as "there has not been any calibration of the SPICE models with measured results" and as such it must be accepted that simulated data will differ slightly from measured data.

Fig. 2.16 shows the measured data for V_{LOWER} only at the exit of the transmission gates and the corresponding simulated data. The voltage at the input to the transmission gates was unavailable for measuring but by examining the plots for V_{UPPER} and the relation to the simulated data, the input voltage can be assumed to be identical to the output voltage.

Fig. 2.17 exposes the major problem with this design. The simulated data expresses the desired static response. These plots were made using only two of the current inputs. As the current flowing into input #1 (which was controlling) was increased, the simulated data shows that the resulting current at output #1 should remain at zero. This is the expected response as the current should be subtracted from itself. Any other input current (#14 in this instance), if constant, should slope linearly down as larger currents are subtracted, until, when both the controlling current and the constant current are the same, both outputs should be reduced to zero.

In the figure, input #14 was held at 20 μA, while the controlling input (#1)

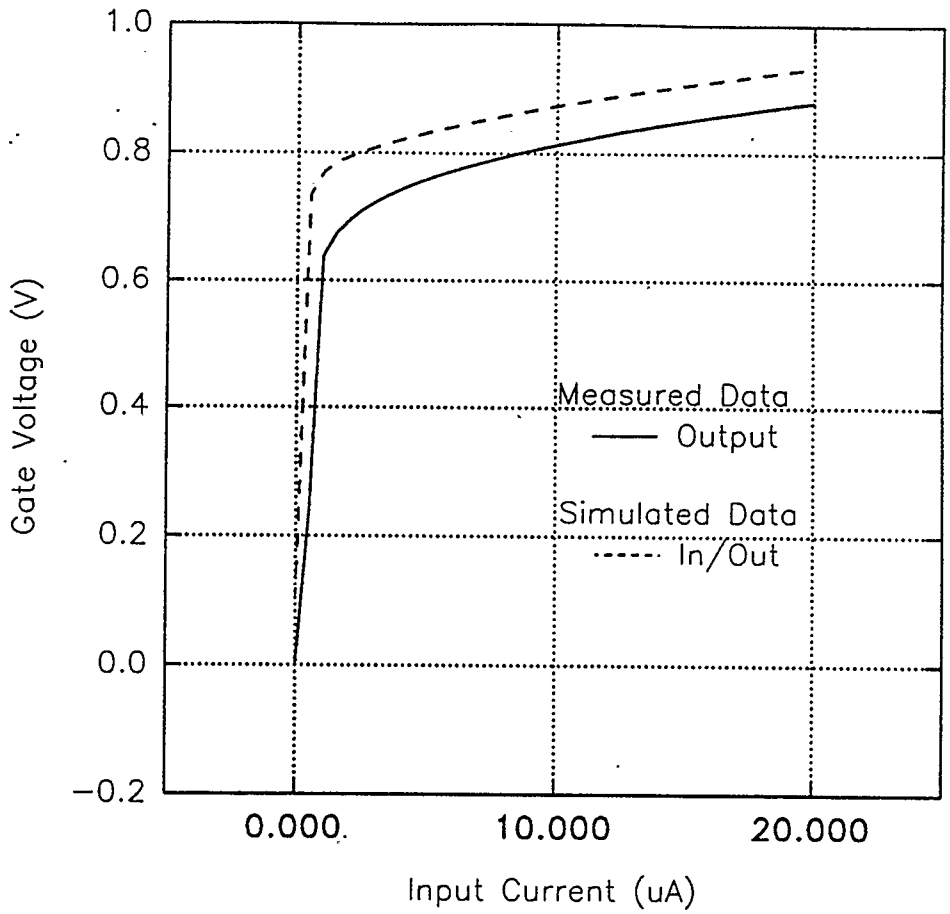

Figure 2.16 - Simulated and measured lower cascode gate voltages.

was raised from 0 to 20 μA. The result shows that, while for the most part the circuit was behaving well, not enough current was being subtracted from either input current. The figure and subsequent tests showed that the amount of leakage or control current lost was of the order of 8% of the control current resulting in

$$I_{o(n)} = I_{in(n)} - G_{IO}\, I_{in(1)} \tag{2.5.1}$$

where the actual current gain, G_{IO}, from the input to the subtraction point in the output was found to be 0.92. Through simple calculations, it can be shown that this size of

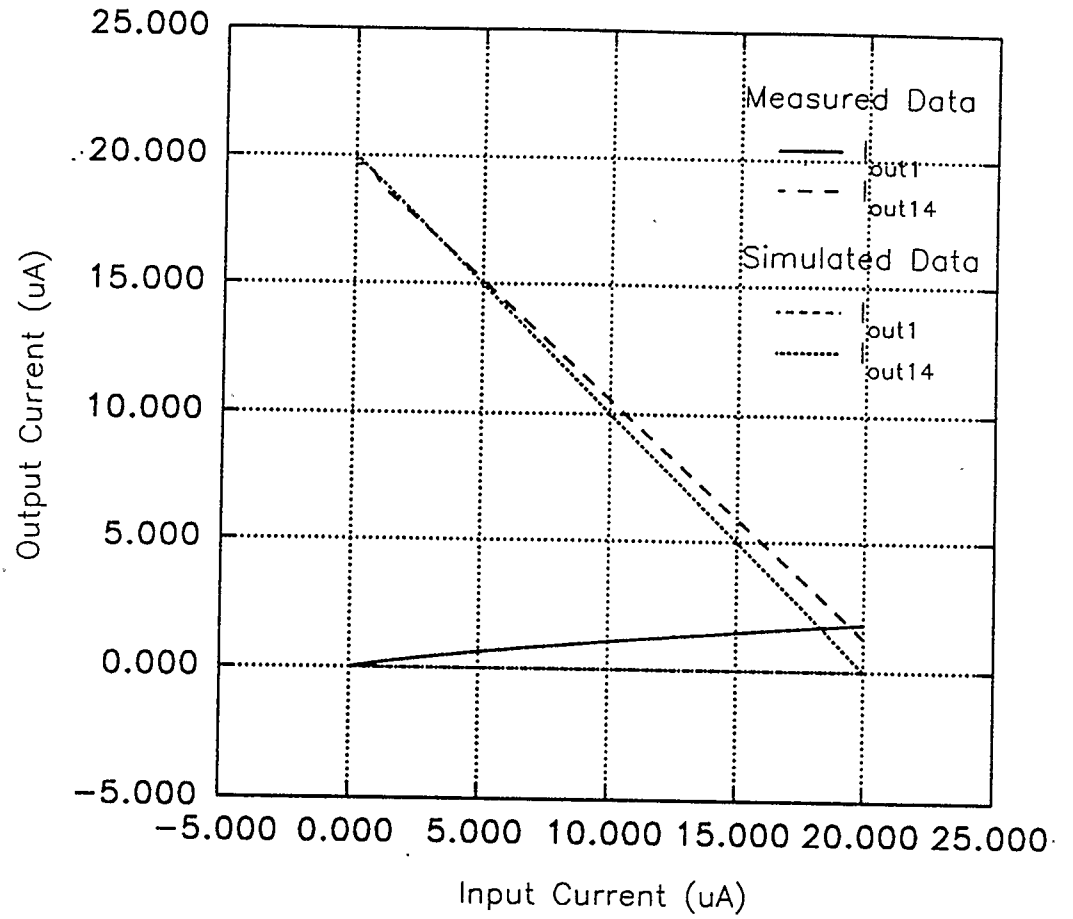

Figure 2.17 - Simulated and measured data for I_{out1} and I_{out14} as a function of I_{in1}.

current gain error could be accounted for by either mismatches in the value of β or a 5-10 mV threshold voltage mismatch in the transistors of the input section and output sections. The exact current gain if only threshold mismatch is accounted for can be found to be

$$G_{IO} = 1 - \frac{2\ \Delta V_T}{(V_{LOWER} - V_T)} \tag{2.5.2}$$

where ΔV_T is the mismatch in transistor threshold voltages.

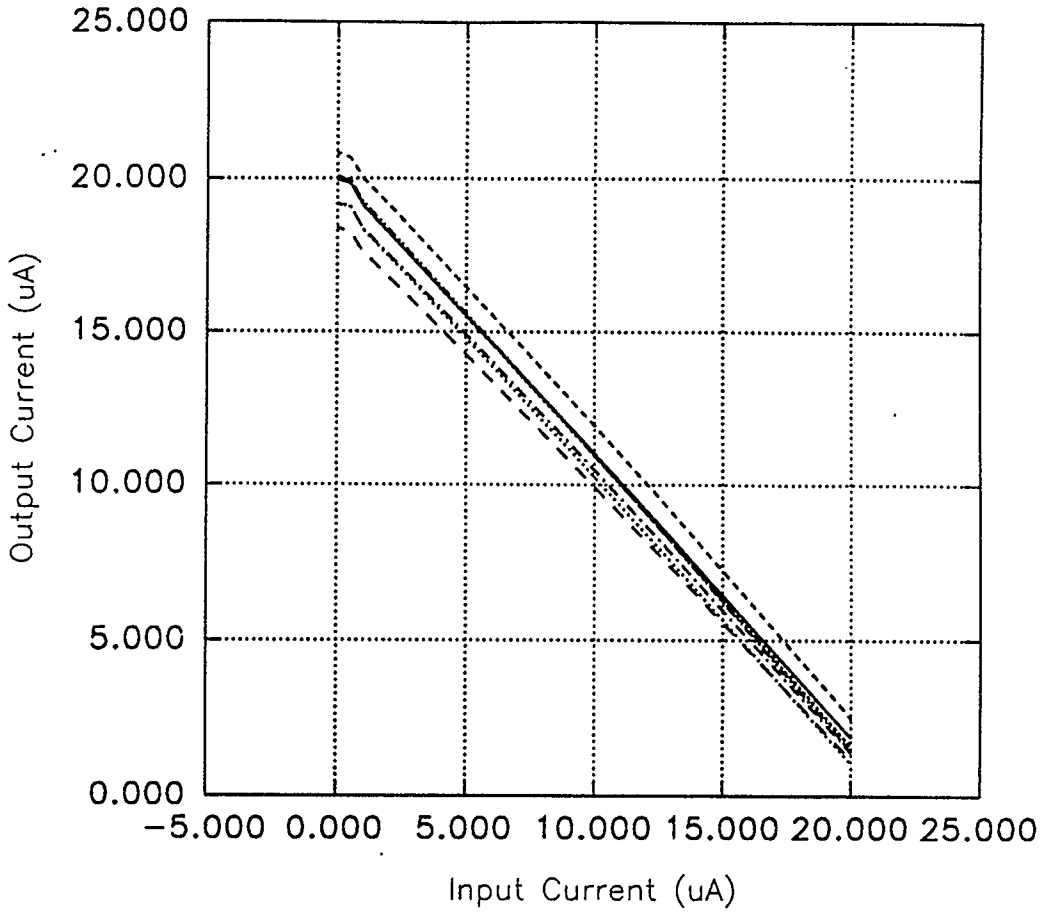

Figure 2.18 - Typical variation in $I_{out(n)}$ as a function of I_{in1}.

2.5.2 Removal of Higher End Current

Fig. 2.19 shows the measured effect of removing the higher of the two end currents from light sources of varying standard deviation. While the curves are generally in the correct position and direction (the ideal response is a rising 45° line through the origin), it was immediately obvious that there was a problem. With the light sources and standard deviations tested, the corrected photocurrents were reduced, with the larger standard deviations, into the range of 100-500 nA. At these current levels, small variations in

detector sensitivity, and processing circuitry had significant effect on the output signal. These problems when coupled with the leakage error mentioned above, resulted in unpredictable results.

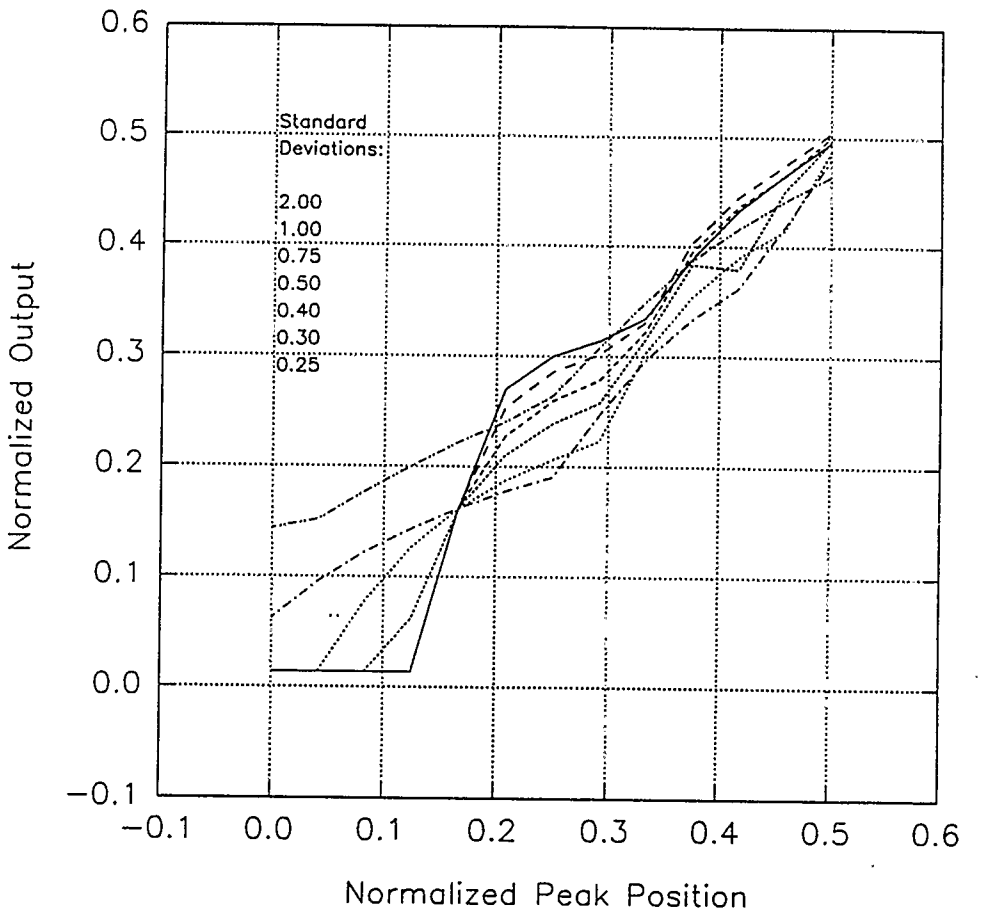

Figure 2.19 - Measured static response when upper current is removed.

2.5.3 Removal of Lower End Current

Removal of the lower of the two end currents lead to much more predictable results. Fig. 2.20 shows the output of the uncorrected OPS. These curves have been shown to

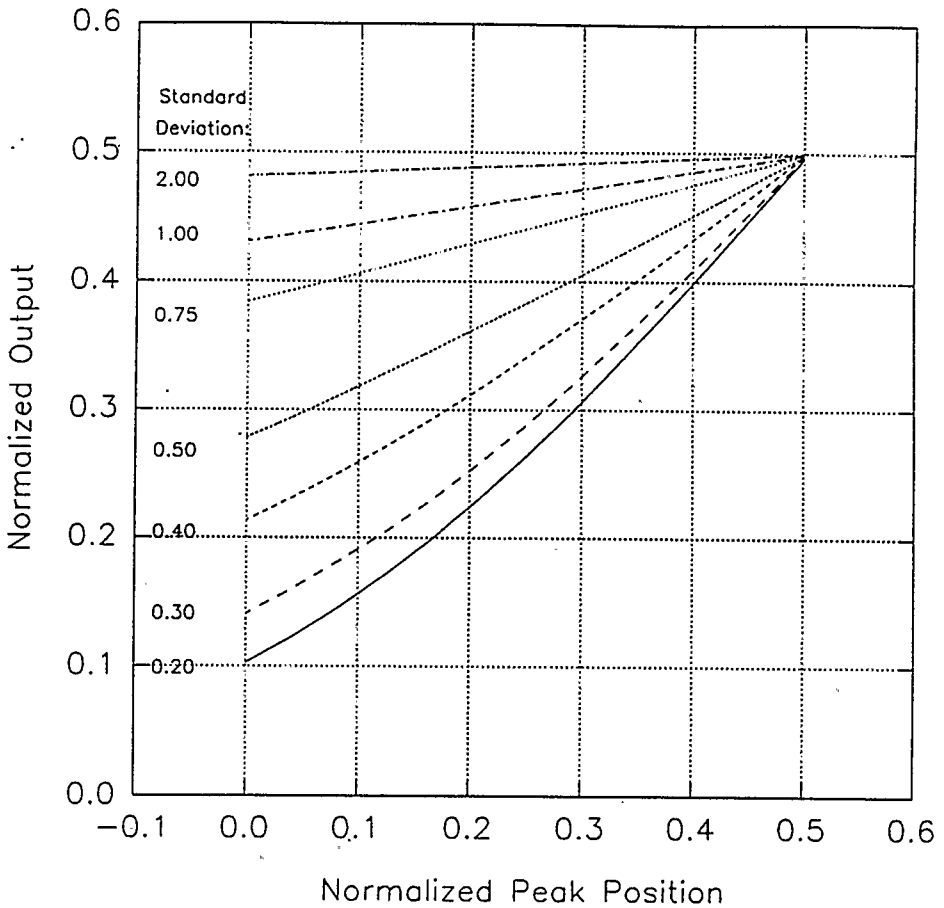

Figure 2.20 - Measured uncorrected position sensor static response.

be well within a maximum error of 1% from the theoretical curves. Fig. 2.21 presents the curves after correction by removal of the lower end current. Some advantage is immediately realized by reduction of the dependence of the output signal on the standard deviation of the light source in the region where x/σ is small, however at higher standard deviations, the source insensitivity, while not completely lost, is greatly reduced.

Figs. 2.22 through 2.28 show both the corrected and uncorrected, measured and theoretical data for each value of σ tested. These verify that the uncorrected circuit

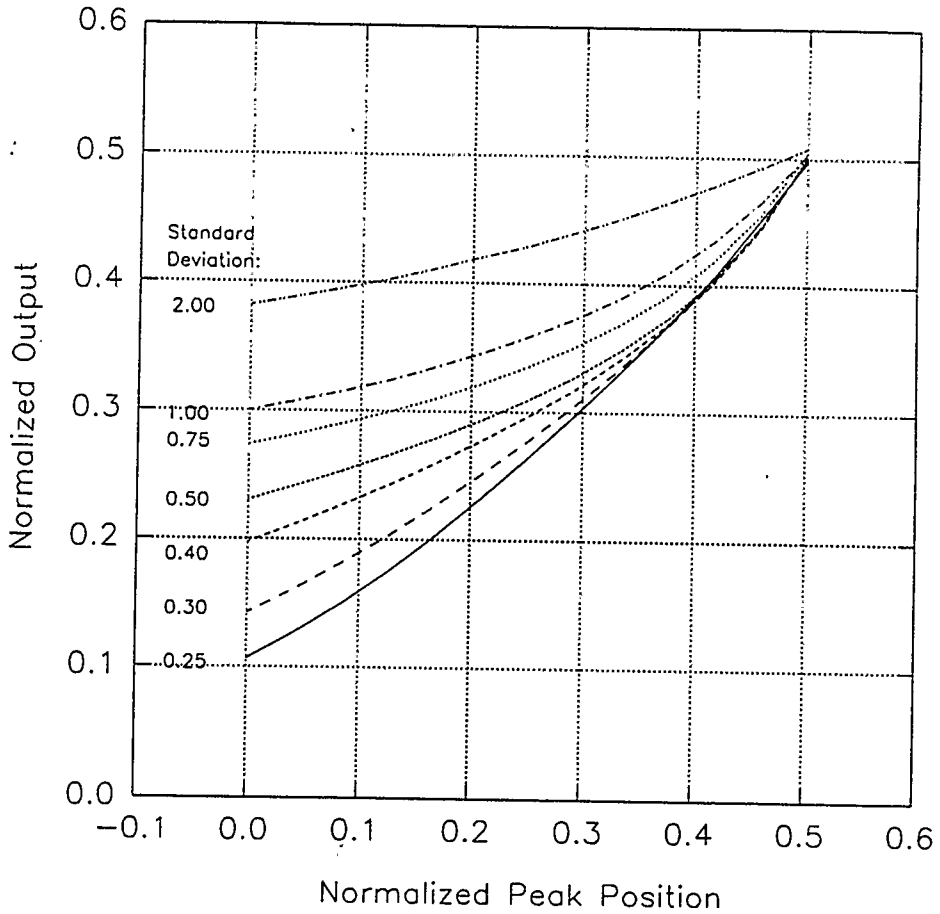

Figure 2.21 - Measured corrected position sensor static response.

output very closely resembles the theory for the uncorrected case, and shows the error in the corrected output.

This error at higher values of σ can be directly attributed to the inaccurate current subtraction mentioned earlier. If this error is taken into account in the simulations, with G_{IO}=0.92, then Figs. 2.29 and 2.30 result, clearly indicating that this is the cause of the error.

Correcting the functional error of non-unity mirror current gains is not easily

solved. The ideal solution lies in creating a current mirror with a gain of precisely unity and with the variability of transistor threshold voltages in modern CMOS processes, the designer can never be assured that the transistors will be matched as well as is necessary for this application.

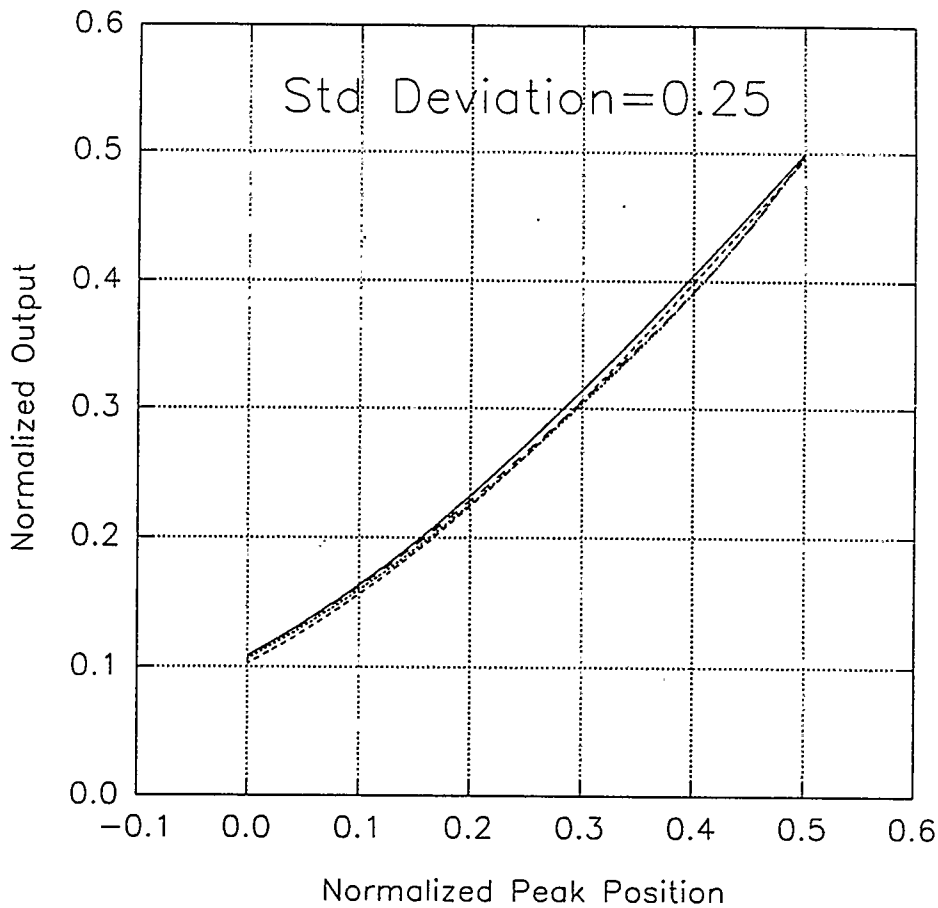

Figure 2.22 - Corrected and uncorrected, measured and theoretical static response (StdDev = 0.25).

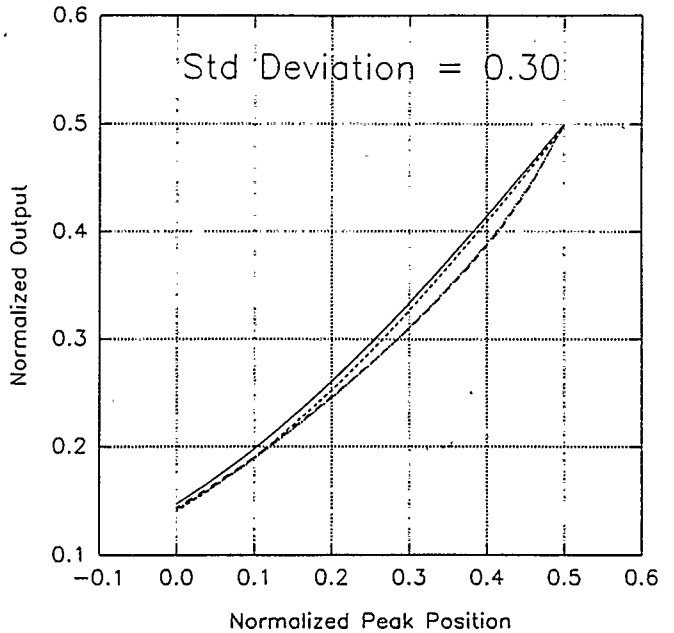

Figure 2.23 - Corrected and uncorrected, measured and theoretical static response (StdDev=0.30).

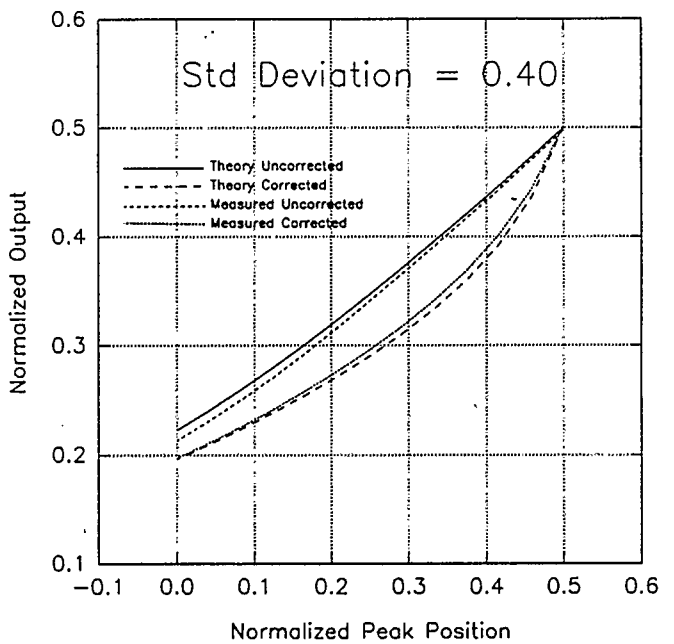

Figure 2.24 - Corrected and uncorrected, measured and theoretical static response (StdDev = 0.40).

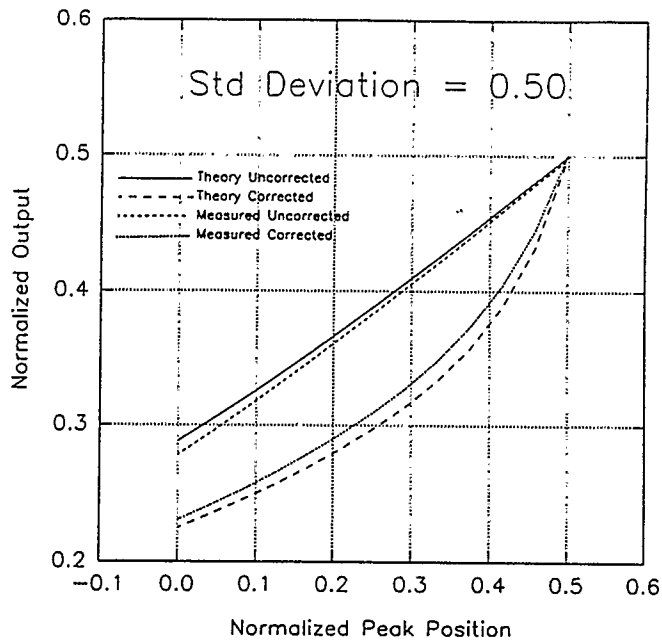

Figure 2.25 - Corrected and uncorrected, measured and theoretical static response (StdDev=0.50).

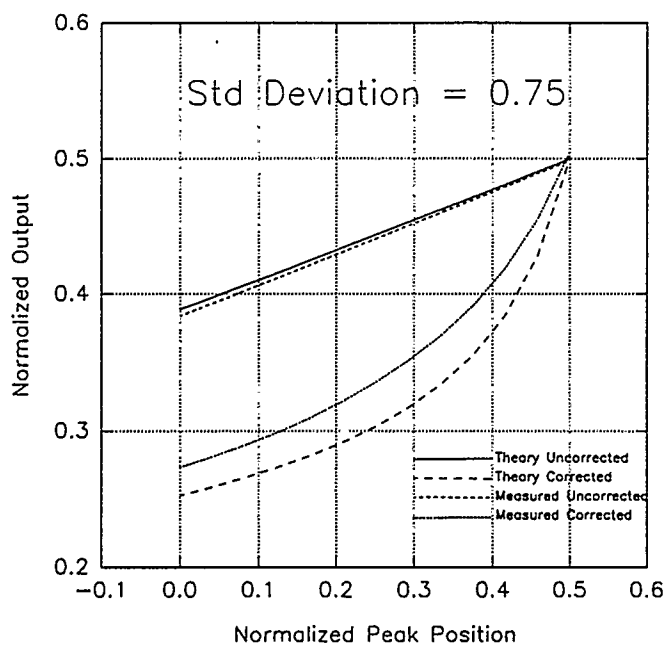

Figure 2.26 - Corrected and uncorrected, measured and theoretical static response (StdDev = 0.75).

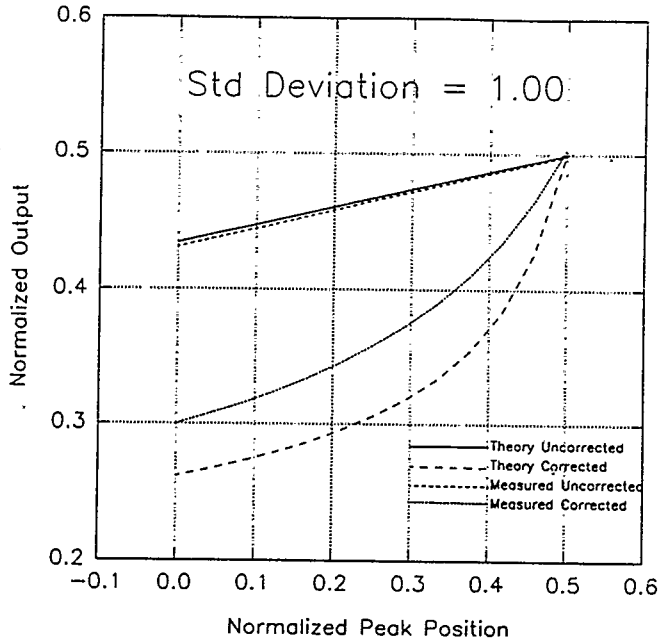

Figure 2.27 - Corrected and uncorrected, measured and theoretical static response (StdDev=1.00).

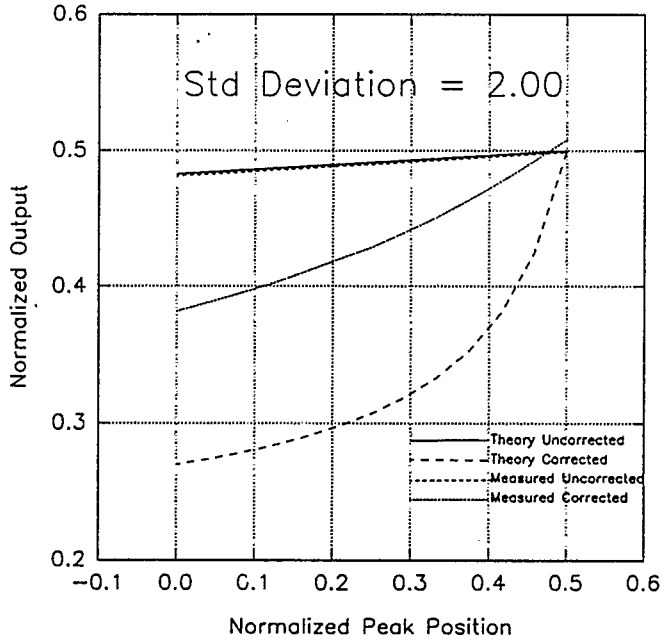

Figure 2.28 - Corrected and uncorrected, measured and theoretical static response (StdDev = 2.00).

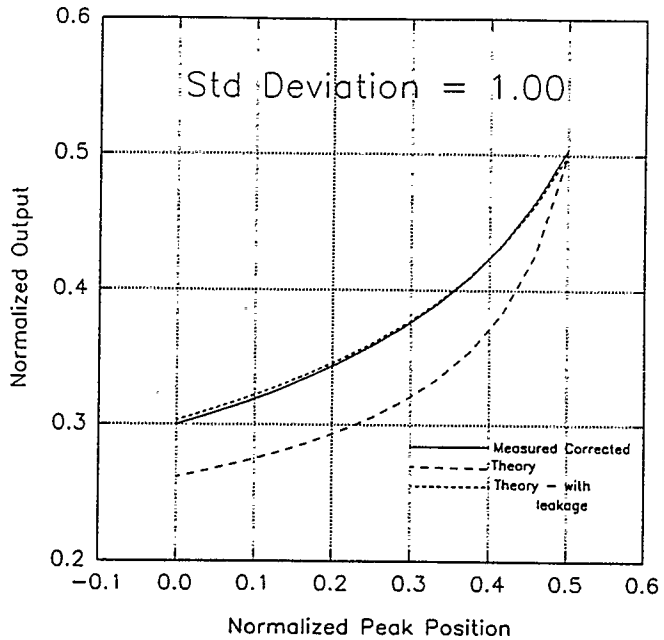

Figure 2.29 - Corrected data with theory incorporating 8% current loss (StdDev=1.00)

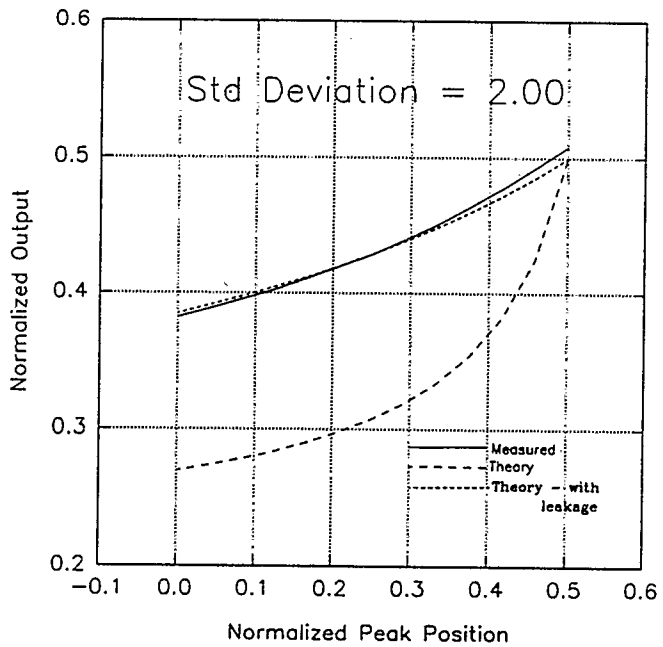

Figure 2.30 - Corrected data with theory incorporating 8% current loss (StdDev=2.00).

2.6 Conclusions and Future Work

The gain errors in the current mirrors between the input sections and the output sections affect the output certainly, but the concept has been shown to be viable. This error in itself however may be correctable in future designs, in various different ways, one of which is by designing the input sections as shown in Fig. 2.31. The cost of this method is that the two end of array currents would not be available for further processing.

This design still relies upon a certain amount of transistor matching. However, it opens the possibility for at least two different threshold voltage values. Transistors M_{I1} and M_{I2} must be matched to the slave transistors in all the output sections, and the remaining transistors in the input section can have a different value of V_T (but must be matched among themselves). The "tank" section of the new input section, consisting of M_{I3} through M_{I6} and M_{I9} through M_{I12} will adjust itself in such a way that I_T will become zero and therefore the transistors M_{I1} and M_{I2} must be drawing exactly I_{IN}. This is achieved through the following process.

Initially, when the current I_{IN} flows, it will flow in transistors M_{I3} and M_{I4}. This current will be mirrored back to itself and to transistors M_{I1} and M_{I2} both of which have different V_T's than M_{I3} and M_{I4}. The result is that the n-channel cascode gate voltages will be raised or lowered in such a way that M_{I1} and M_{I2} will be drawing I_{IN} and I_T will become zero. This will ensure that all cascode slave transistors with the same threshold voltage as M_{I1} and M_{I2} will draw precisely I_{IN} when V_{UPPER} and V_{LOWER} are applied to their gates.

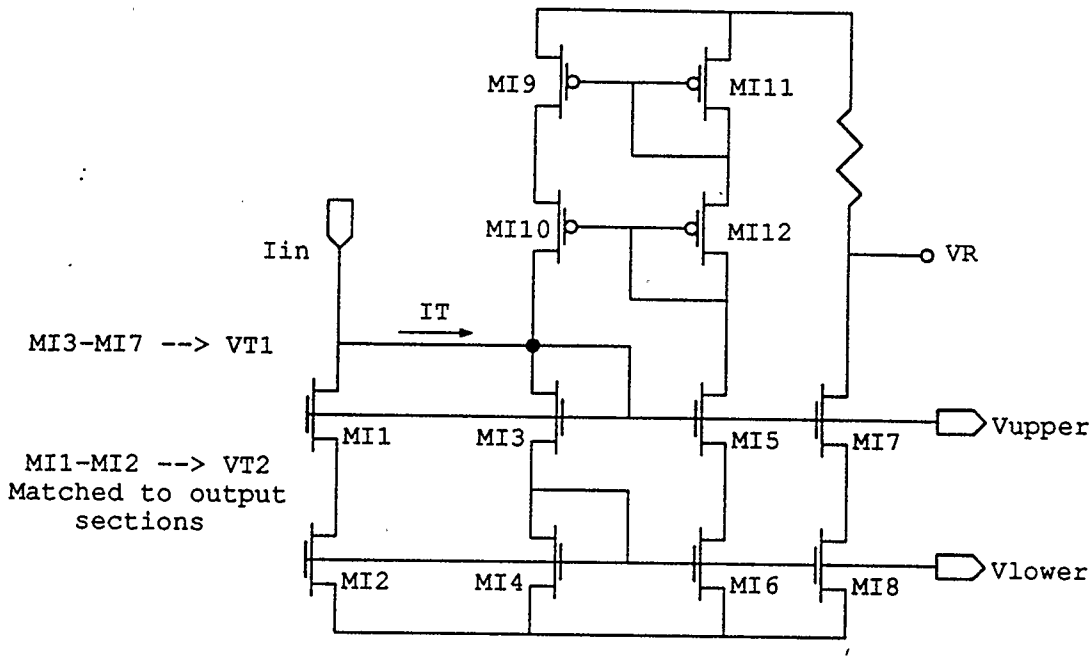

Figure 2.31 - Input circuit to solve V_T matching problems.

Another more complex solution lies in using dynamic current mirrors [6]. These mirrors use the same transistor as both the driver and slave during two separate phases of operation as shown in Fig. 2.32, thus removing the differences in threshold voltage and β. Conceptually, operation is very simple. During phase 0, the capacitor is charged such that

$$V_C = \sqrt{\frac{2\, I_0\, L}{\beta\, W}} + V_T \tag{2.6.1}$$

and during phase 1 of operation, this same voltage is used to drive the transistor. This elegant solution suffers from other shortcomings including charge injection errors due to the switches, and difficulty in producing constant operation, multiple output current

mirrors, but regardless, this solution warrants some future attention.

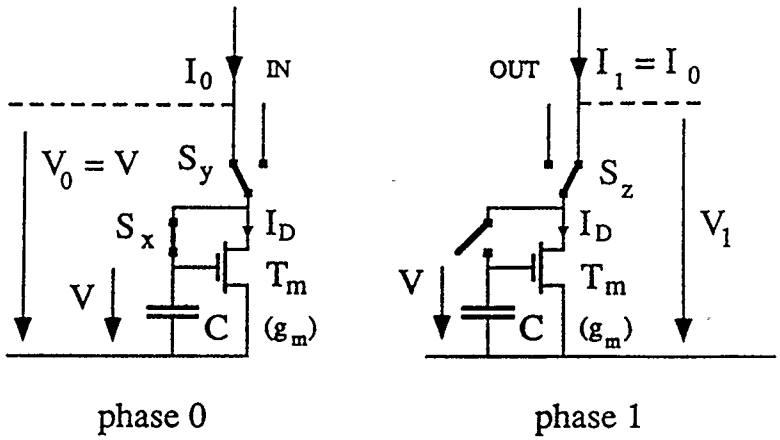

Figure 2.32 - A simple dynamic current mirror.

Chapter 3

A Serial Position Sensor

3.1 Reasons

The basic position sensor, both with and without any additional correction circuitry still has limitations. These include the need for one two-quadrant analogue multiplier per photosensor and a custom VLSI photoarray to provide the tightly spaced photosensors necessary for operation. The first limitation puts a significant limit on the number of multipliers and hence photosensors that can be used due to space limitations, while the second may not be monetarily inhibiting for a large company or university, but the combination of the two reduces the circuit's general usefulness and convenience. Readily available commercial parts cost a fraction of the cost of full custom designs in both time and money and have been pre-tested and are compliant with published specifications.

3.2 The EG&G Reticon RA1662N

The keys to circumventing the above limitations lie in new commercial photodiode arrays such as those made by EG&G Reticon [7]. In particular, the RA1662N "Parallel Output Photodiode Area Array" combines several features which allow for reduced centroid sensor circuitry per photodiode, exposure integration which is important at low light levels and is not achievable with the basic centroid circuitry without much additional hardware, and, by its primary function, provides a non-custom, commercially available, tightly spaced, array of photodiodes.

The array itself consists of a 62 by 16 array of photodiodes with 100 micrometer centre spacing (6.2mm by 1.6mm), each connected to a small amount of MOS circuitry as shown in Fig. 3.1, where V_{array} is a negative voltage. Each of the 62 photocells in a column is connected to one of 16 video output lines with each typically terminated in a resistance. Internal circuitry provides all control signals to consecutively sample each photodiode in a column.

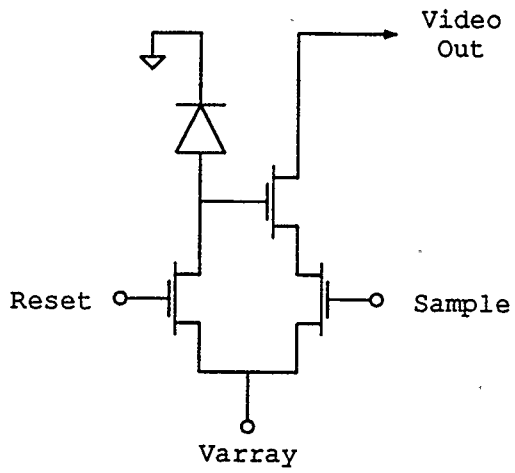

Figure 3.1 - Simple cell circuitry in each EG&G Reticon RA1662N photocell.

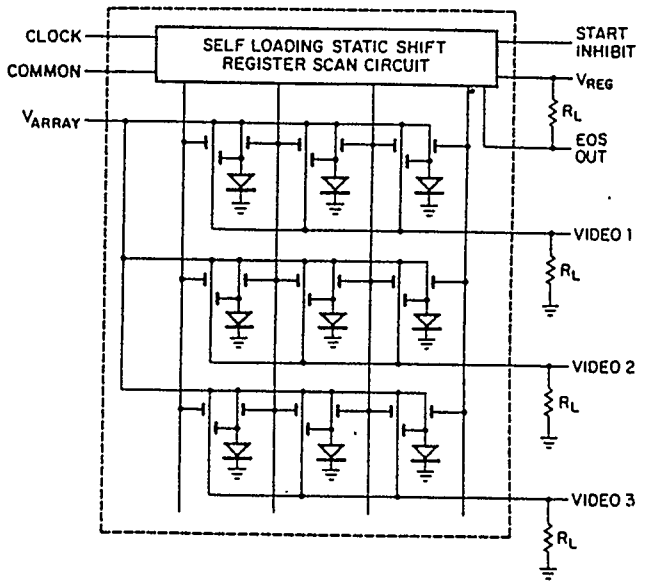

Figure 3.2 - Internal RA1662N connections.

The MOS circuitry in each cell, as in the figure, provides the ability to both sample a cell and reset it. When the RESET signal is pulled high relative to V_{array}, the RESET transistor begins to conduct, and current will attempt to flow against the reverse biased photodiode, in effect charging the diode junction capacitance to V_{array}. The RESET signal is then brought low again and the voltage across the photodiode is allowed to decay for some period of time due to light exposure and generation-recombination effects. Sometime later, when the SAMPLE signal is pulled high relative to V_{array}, the output transistor is allowed to conduct through the sample transistor. Because the voltage at the gate of the output transistor (across the photodiode) will be inversely proportional to the amount that the diode voltage decayed between the time it was reset and sampled, the output current sunk by the output transistor will also be inversely proportional to the intensity of light incident on the photodiode. This cycle moves down each column of

photodiodes in parallel across all 16 columns, at a speed controlled by an input clock, sampling each photodiode while resetting the previously sampled cell.

Fig. 3.3 shows the typical light response of the photodiodes, which is limited on the long wavelength end by

$$\lambda_{max} = \frac{h\ c}{E_{gap}} \tag{3.2.1}$$

where h is Plank's Constant, c is the speed of light, and E_{gap} is the semiconductor's energy band gap. If E_{gap} for silicon is taken to be 1.12 eV, the maximum wavelength that the silicon will convert to charge is 1109 nm. This is well into the infrared band.

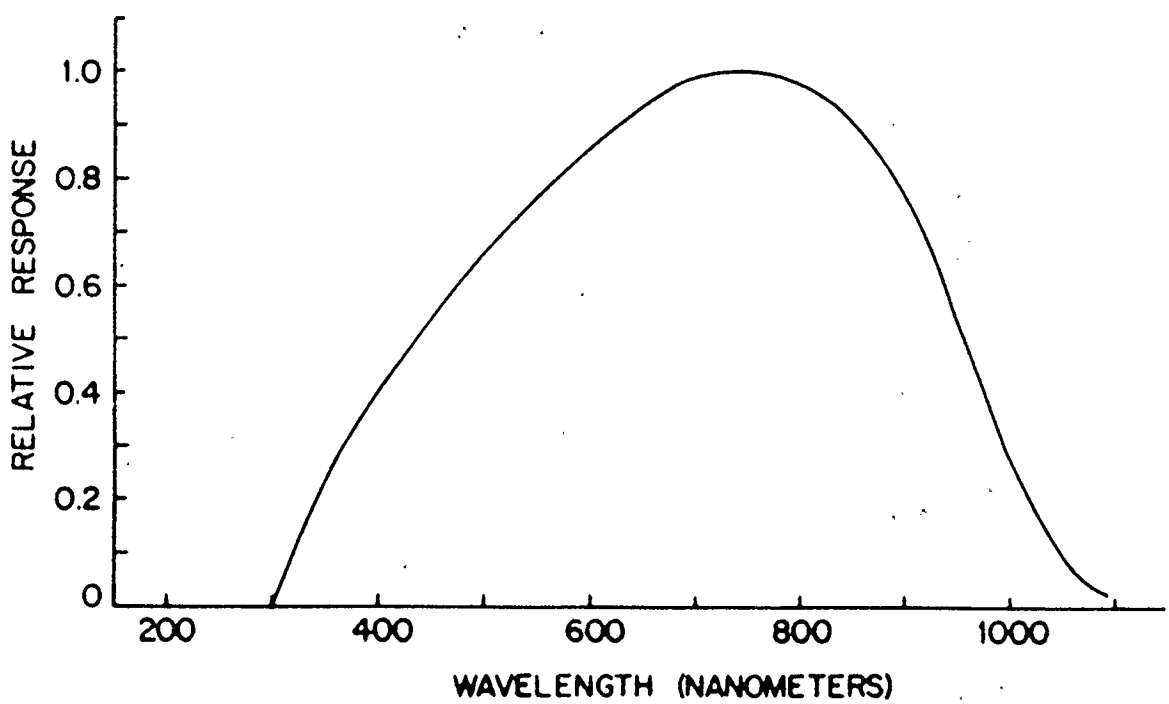

Figure 3.3 - Typical spectral response of the RA1662N photodiode array.

Fig. 3.4 shows the typical output voltage curves for varying levels of exposure, but because very little information on the internal circuit parameters is available to the public, these values have not been checked against simulated data and must therefore be accepted as is. It is sufficient to know that in the dark, currents as high as 200 μA have been observed. The actual size of the output current is dependent upon the size of the output resistor due to non-infinite output resistance effects. Calculations with the given values for V_{ARRAY} and R_L and integration times of 1.6 mS yield light sensitivities of approximately 762nA/μW/cm^2. This is 381.0 times more sensitive than the basic sensor's published sensitivity of 2nA/μW/cm^2.

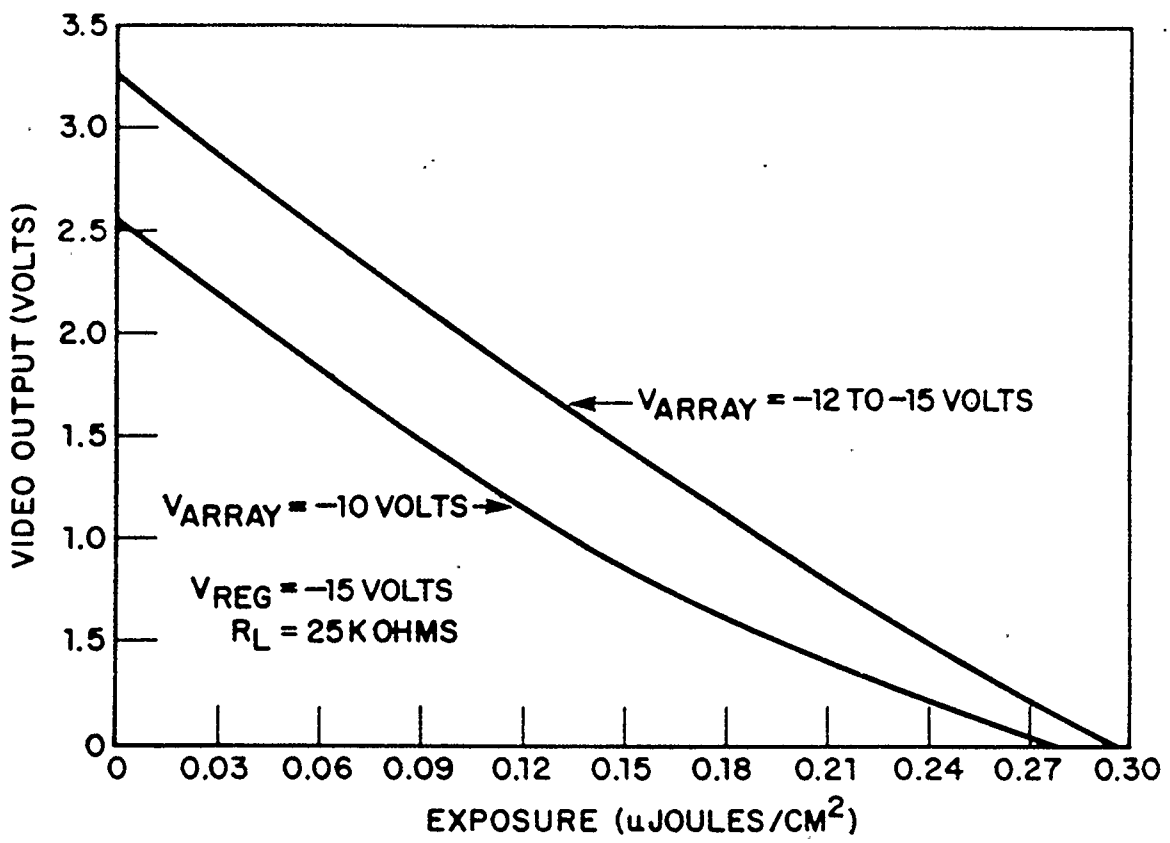

Figure 3.4 - Typical curves of output voltage versus exposure.

Externally, the operation of this chip is very simple. After sampling all 62 photodiodes in the columns, the output currents are returned to zero during a 2 clock cycle retrace. This period of time is marked by the end of scan (EOS) signal being brought high. The exact timing of these signals can be seen in Fig. 3.5.

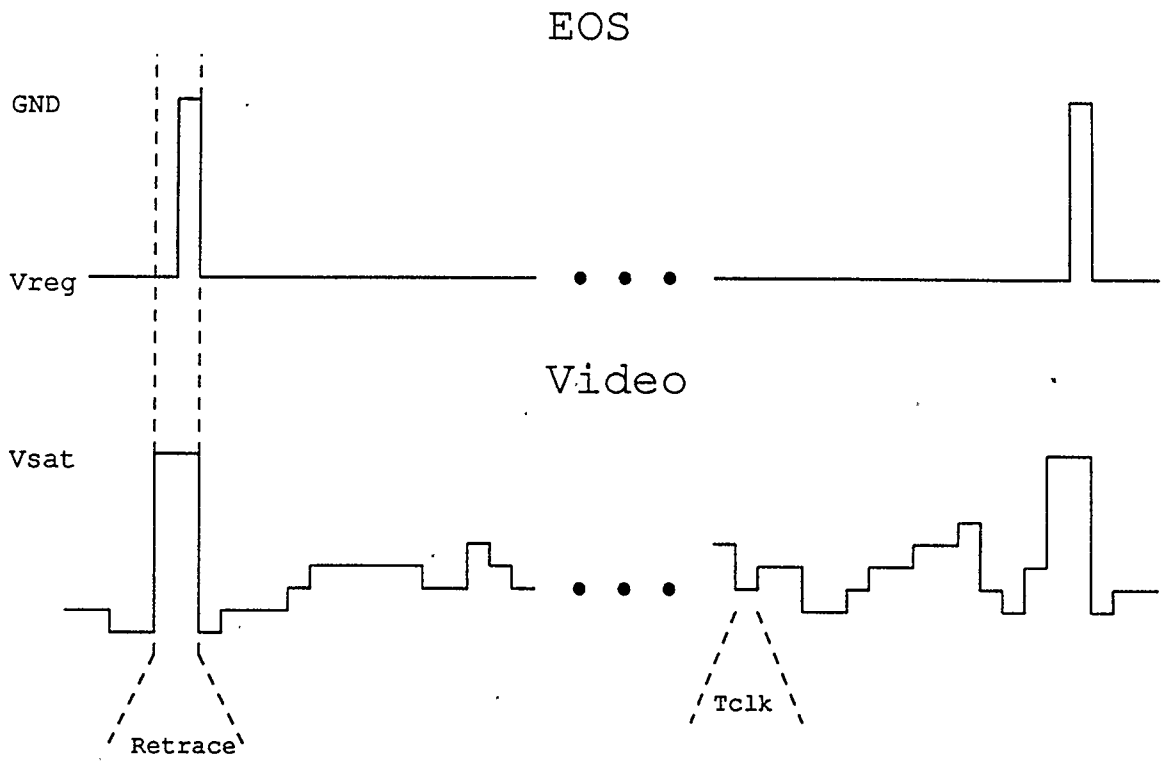

Figure 3.5 - Timing of RA1662N End of Scan and Video signals.

There are only two signals which need be supplied to the chip. These are a clock, which specifies the rate at which the pixels are sampled, and a start inhibit (SI) line. By holding SI high, pixel sampling will continue immediately following the retrace in continuous operation. Sampling will not begin after a retrace until the SI line is brought high.

These controls allow for a two tiered clocking system. One fast clock will determine the rate at which pixels are scanned, and a slow clock signal applied to the SI pin will determine the integration time. This clock should have a very low duty cycle such that

$$t_{high} < 64 \cdot T_{clk} \tag{3.2.2}$$

where t_{high} is the time that the integration clock applied to SI is high, and T_{clk} is the period of the sample clock. This ensures that SI does not remain high for more than one full video scan so that only one complete scan is made for each period of the SI signal. A complete columnar scan of the photodiodes is then made once every period of the SI signal, with a new pixel sampled every period of the CLK signal as seen in Fig. 3.6.

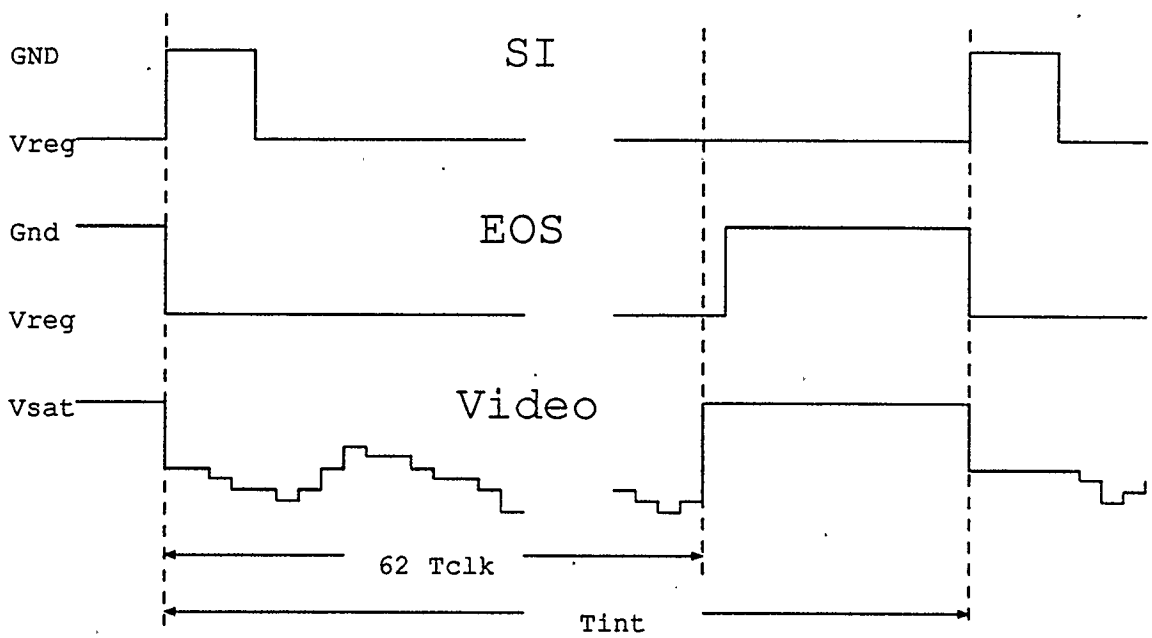

Figure 3.6 - The timing of a two tiered clocking system for the RA1662N.

For the purposes of this thesis, it is assumed that the serial video output current that is sunk by the RA1662N is made up of two signals such that

$$I_{photo(n)} = I_{max} - I_E(n) \tag{3.2.3}$$

where n is the appropriate pixel number, I_{max} is some positive offset current determined by the biasing of the chip and $I_E(n)$ is the current directly proportional to light exposure at pixel n. It is worthwhile noting that this means there is no current sunk if the pixel light exposure makes $I_E(n)=I_{max}$ and I_{max} will be sunk if the chip is operating in darkness.

3.3 Theory

The block diagram of a circuit which can use one of the RA1662N serial video outputs to determine the one dimensional position of the centroid of incident light is shown in Fig. 3.7. This circuit can be broken down into five distinct segments and will be discussed as such. These segments are the input current mirrors, reference voltage generation, multiplication and interpolation, voltage division and output sample/hold.

The two currents emanating from the input mirrors are used to calculate both the numerator and denominator of the centroid equation. The numerator is calculated by multiplying the photocurrent, $I_{o1}(n)$, by a linearly ramping reference voltage, and integrating the resulting current on a capacitor. By the end of one complete scan, the capacitor voltage,

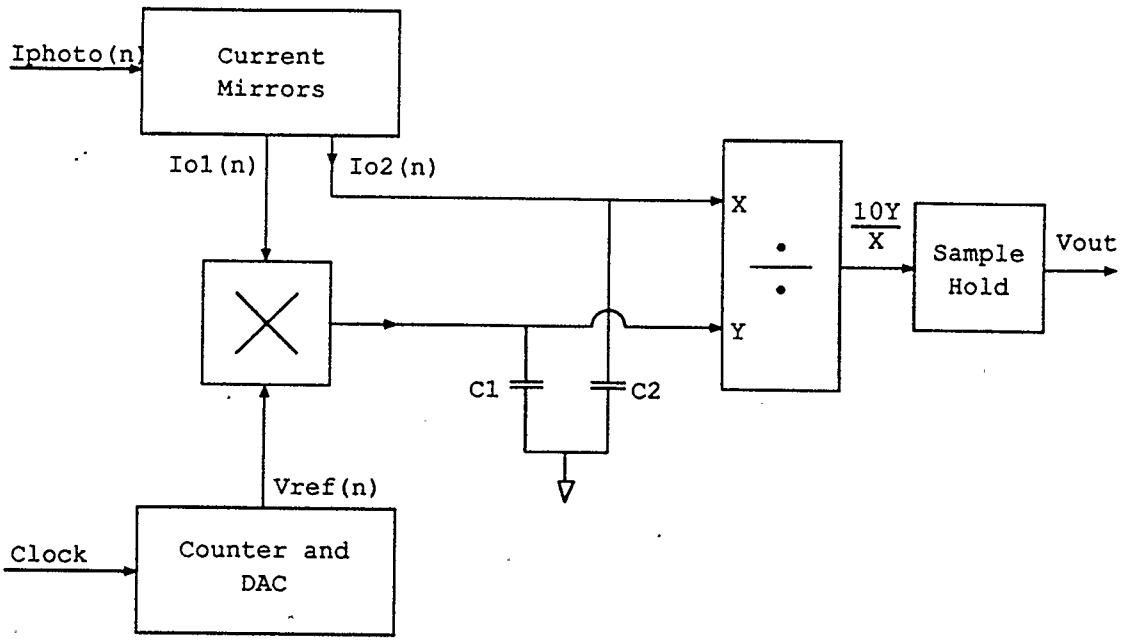

Figure 3.7 - Block diagram of a simple serial position sensor.

$$V_{c1} \propto \sum_{n=0}^{N-1} I_{photo(n)} \, V_{ref}(n) \quad . \tag{3.3.1}$$

The denominator equation value is arrived at by just integrating the photocurrent $I_{o2}(n)$, which is equal to $I_{o1}(n)$ onto a second capacitor, resulting in, at the end of a complete scan,

$$V_{c2} \propto \sum_{n=0}^{N-1} I_{photo(n)} \quad . \tag{3.3.2}$$

V_{c1} may then be numerically divided by V_{c2} and sample/held until the next scan to arrive at an indication of the centroid position.

3.4 A Practical Realization

3.4.1 Input Mirrors

The purpose of the input current mirrors really is twofold when the RA1662N is used. The first is to invert the video current and remove the effects of I_{max} in such a way that higher light exposures will result in higher mirror output currents and the second is to produce two identical "copies" of the resulting current.

A circuit which performs both these tasks is shown in Fig. 3.8. The input to the circuit is one of the photoarray's 16 video outputs. When this signal is terminated across a resistor, R_{p1},

$$V_p(n) = V_{sat} - R_{p1}(I_{\max} - I_E(n)) \tag{3.4.1}$$

where V_{sat} is a constant voltage and everything is as shown in the figure. If all active devices are assumed to be ideal, and assuming $R_{p1}=R_{p2}=R_{p3}=R_p$,

$$I_{o1}(n) = I_{o2}(n) = I_E(n) + \left[\frac{V_{sat} - V_{correct} - R_p I_{\max}}{R_p}\right] \tag{3.4.2}$$

where an easily adjustable $V_{correct}$ can be supplied by a voltage divider since all circuit inputs at this node will be high impedance. $V_{correct}$ can then be adjusted to remove the second term in Eqn. (3.4.2), resulting in

$$I_{o1}(n) = I_{o2}(n) = I_E(n) \quad . \tag{3.4.3}$$

However, if this cancellation is not performed correctly, some constant offset current, I_{off},

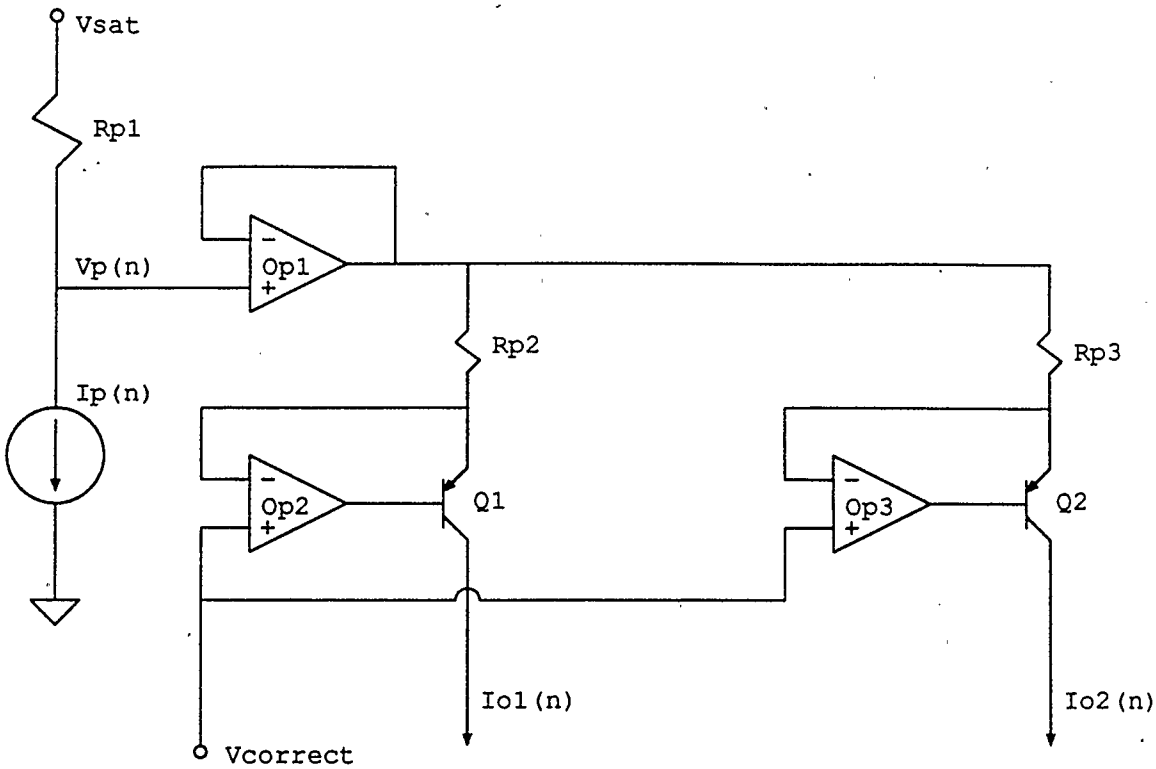

Figure 3.8 - The serial input mirrors.

will also be associated with the mirror output currents. This will have an effect on the centroid calculation, but small values of I_{off} will have little effect as will be seen later.

If nonideal active device parameters are included and resistors are not assumed to be equal, it can be shown that

$$I_{o1}(n) = K_1 I_E(n) + I_{off1} \tag{3.4.4}$$

where

$$K_1 = \frac{\beta_1 R_{p1}}{(\beta_1+1) R_{p2}} \tag{3.4.5}$$

and

$$I_{off1} = \frac{\beta_1}{(\beta_1+1)}\left[\frac{V_{sat}-R_{p1}(I_{\max}-I_{B1}^{+})-R_{p2}I_{B2}^{-}(V_{off1}-V_{off2})-V_{correct}}{R_{p1}}\right] . \quad (3.4.6)$$

$I_{o2}(n)$ may be calculated in a similar way. Again, $V_{correct}$ can be adjusted to cancel the I_{off} terms, but this must be done after the circuit is built for each mirror as a calibration since exact values for the active device errors will not be known.

3.4.2 Reference Voltage Generation

This circuit segment can be seen in Fig. 3.9 and consists of the counter and DAC. $V_{ref}(n)$ must be synchronized with the RA1662N in such a way that when the first pixel video data is being supplied to the input mirrors, the DAC output will be zero, and when the last pixel video data is available, the DAC output should be at V_{REF}. In this way, the DAC will supply a reference voltage to the multiplying OTA that is proportional to the position of the currently sampled pixel. This is analogous in the basic sensor to the voltages down the resistor chain. These voltages will be

$$V_{ref}(n) = \frac{V_{REF}\ n}{N-1} \quad (3.4.7)$$

where N is the total number of pixels in a full output scan.

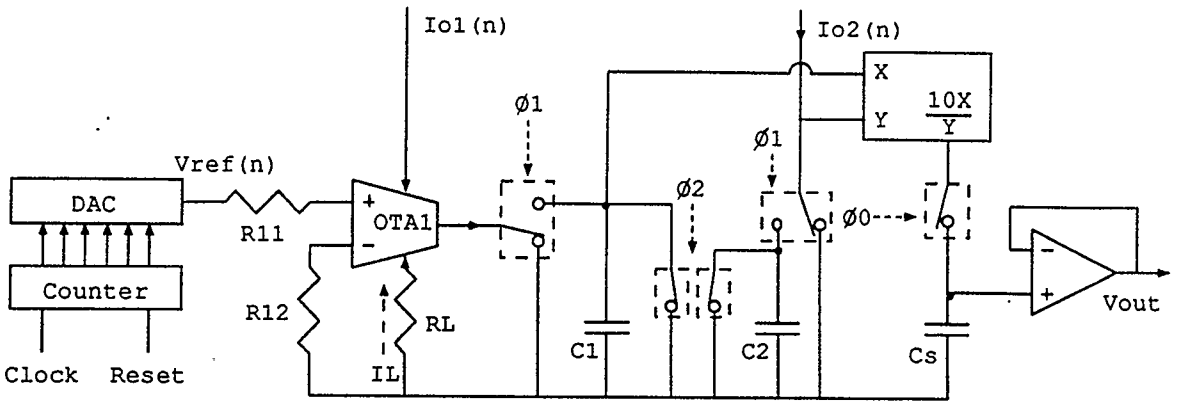

Figure 3.9 - Serial position sensor output processing circuitry.

3.4.3 Multiplication and Integration

This section is composed of the multiplying LOTA (OTA1) and the summing capacitors C_1 and C_2. When $I_{o1}(n)$ and $V_{ref}(n)$ are multiplied together via OTA1, and if the OTA is assumed to be an ideal device,

$$I_{o3}(n) = \frac{I_{o1}(n)\ V_{ref}(n)}{I_L\ (R_{11}+R_{12})} \tag{3.4.8}$$

where everything is as shown in the figure.

Under these conditions, if the voltages on the capacitors C_1 and C_2 are preset to zero before the scan, and

$$V_{ref}(n) = \frac{V_{REF}\, n}{(N-1)} \tag{3.4.9}$$

then by the end of the scan,

$$V_{c1} = \frac{T_{clk}\, V_{REF}}{I_L\, C_1\, (R_{11}+R_{12})} \sum_{n=0}^{N-1} \frac{I_{o1}(n)\, n}{(N-1)} \tag{3.4.10}$$

and

$$V_{c2} = \frac{T_{clk}}{C_2} \sum_{n=0}^{N-1} I_{o2}(n) \tag{3.4.11}$$

which, by referring back to Eqn. (1.3.3), can be seen to be gained versions of the numerator and denominator of the centroid equation (V_{c1} and V_{c2} respectively).

Non-ideal OTA effects result in very complex equations. However, it has been found that one non-ideality in the OTA dominates all others. A small mismatch in the OTA differential pair resulting in only a 1 mV offset voltage produces a significant gain error when linearization is used. As explained in appendix A, the differential voltage applied to the differential pair can be shown to be

$$V_{12} = V_{TH} \ln\left(\frac{I_L + I_{in}}{I_L - I_{in}}\right) \tag{3.4.12}$$

where I_L is the LOTA linearizing current, I_{in} is the input current, and V_{TH} is the thermal voltage kT/q. If some small offset voltage V_{off} is added to this already small value, the output current of the LOTA becomes

$$I_{o3}(n) = I_{o1}(n) \tanh\left(\frac{V_{12}+V_{off}}{2V_{TH}}\right) \tag{3.4.13}$$

and can be approximated due to the very small values of V_{12} and V_{off} to

$$I_{o3}(n) = I_{o1}(n)\left(\frac{V_{12}}{2V_{TH}} + \frac{V_{off}}{2V_{TH}}\right) \tag{3.4.14}$$

in which the second term amounts to a gain error. There is nothing that can be done about this offset, so the design must work around it.

The design of such a multiplier, as with most design problems, involves a trade off between opposing design criteria. Firstly, to void clipping of the multiplier,

$$\frac{V_{REF}}{I_L(R_{11}+R_{12})} \leq 1 \tag{3.4.15}$$

so that the output current does not exceed the photocurrent as the design of the CA3280 LOTAs will not allow for this. Secondly,

$$I_L > I_{in} = \frac{V_{REF}}{(R_{11}+R_{12})} \tag{3.4.16}$$

to ensure that the voltage across the linearization diodes does not become excessive and negates the assumption that $I_{in}=V_{in}/2R$. The second point effectively destroys the OTA gain, and, since V_{12} is kept small, the differential pair mismatch becomes more important. A good balance of these two points arises when the maximum value for I_{in} is limited to 10% of I_L, where if V_{12} is assumed to be small,

$$I_{in}(n) = \frac{V_{ref}(n)}{(R_{11}+R_{12})} \quad . \tag{3.4.17}$$

For the designed circuit, with V_{REF}=10 volts, R_{11} and R_{12} were both chosen to be 500KΩ and I_L set to 100 μA.

The selection of integration capacitors is also subject to various influences. It must be ensured that, as currents are integrated and the capacitor voltage rises, it must never reach a point where the current sources supplying the current fail. For this reason, larger capacitors are necessary at high photocurrent levels. However, these same capacitors must be drained during the retrace time to zero volts across the non-zero resistance (typically about 400 Ω) of the conducting transmission gates. If continuous operation is not being used, and integration time as mentioned earlier is significant, the capacitors will have T_{SI} - 62 T_{CLK} in which to drain across the transmission gates and no problem is likely.

3.4.4 Output Signal Processing

Once a scan is complete, signalled by the counter being at 61, the two integration capacitors C_1 and C_2 will be at voltages proportional to the numerator and denominator of the centroid equation respectively. Several operations involving the analogue transmission gates must now occur. First, integration is stopped by redirecting I_{o2} and I_{o3} to ground, voltages V_{c1} and V_{c2} are divided using a commercial analogue divider and sample/held using a simple transmission gate, capacitor and output follower as shown in Fig. 3.9 and the counter is reset to zero. These three operations can be performed simultaneously. Then the capacitors are discharged by transmission gates connecting them to ground and the cycle can start anew. Figs. 3.10 and 3.11 show the expected effects on the static transfer function of the light source standard deviation and I_{off}.

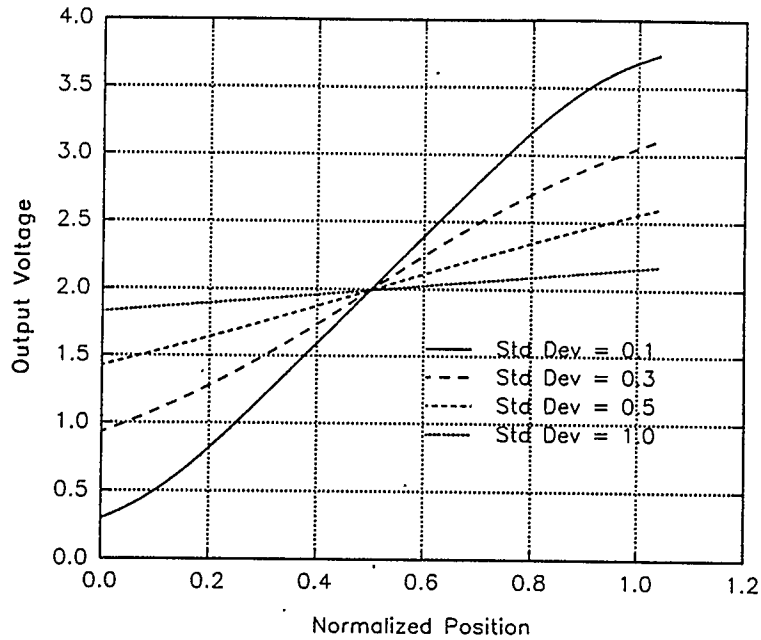

Figure 3.10 - Effect of light source standard deviation on serial position sensor output.

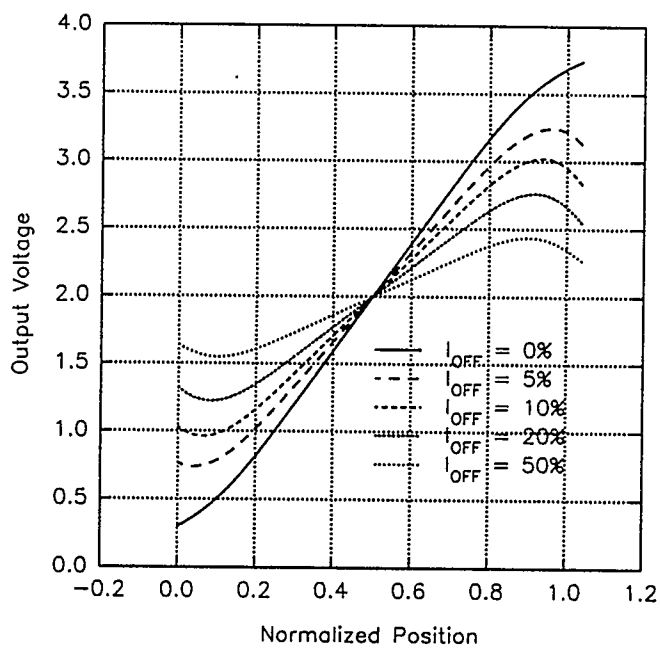

Figure 3.11 - Effect of large offset currents (I_{off}) as percentage of signal peak.

3.5 Testing and Results

Testing proceeded in two stages. First, the input section was tested to ensure that correct current mirroring was accomplished and then the full circuit with the input section and all glue circuitry was tested on several light sources. These light sources were produced by directing a truncated fibre optic cable at the RA1662N. Figs. 3.12 through 3.14 show the inverted (higher currents at higher exposure) and mirrored photocurrents supplied during complete scans of the RA1662N and their best fit gaussian profiles. Any offset current I_{off1} has been removed in the plots prior to curve fitting so that only direct exposure attributable currents ($I_E(n)$) are shown and fitted.

The three light sources were produced by slightly different means. Source A was the first light source, source B was produced by decreasing the light source's intensity to approximately half that of source A, and source C was produced by increasing the sample clock frequency, f_{clk}, from 14.22 kHz to 40.00 kHz, but maintaining approximately the same peak output current by increasing the light source intensity accordingly.

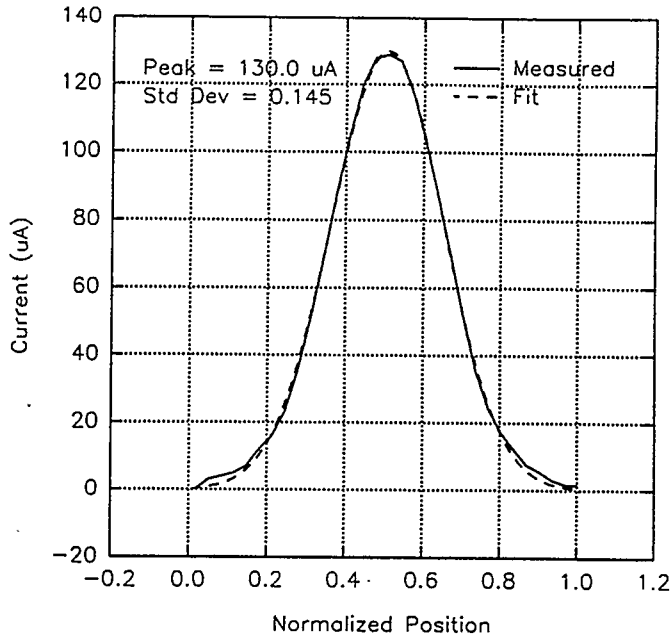

Figure 3.12 - Intensity profile of light source A.

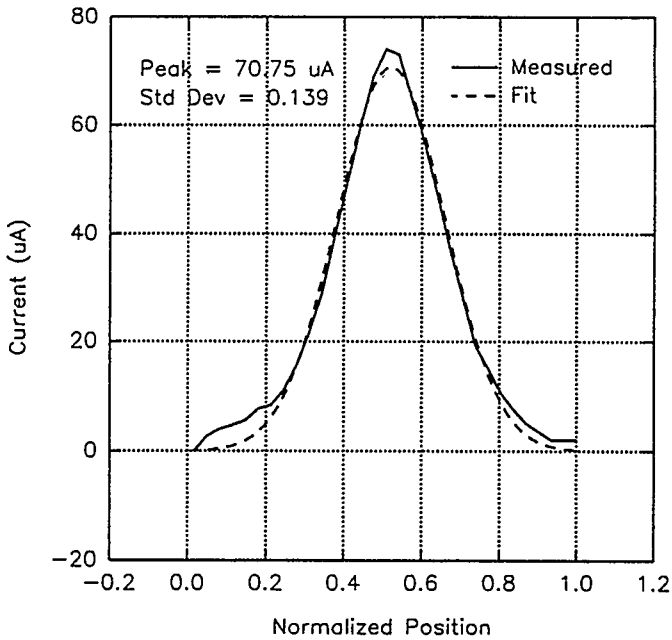

Figure 3.13 - Intensity profile of light source B.

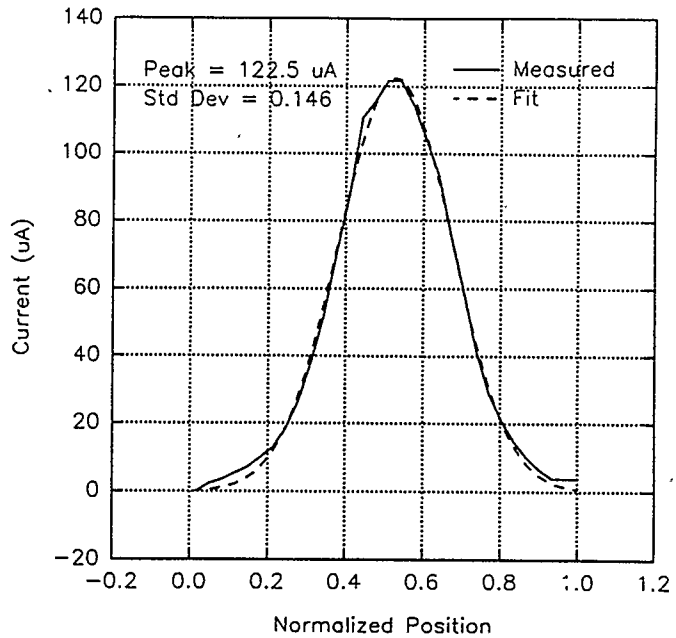

Figure 3.14 - Intensity profile of light source C.

3.5.1 The Input Section

The input current mirrors were tested by applying a current to the input in a fashion similar to the operation of the RA1662N array and measuring the current at the outputs of the current mirrors by terminating them to ground across a nominal 10K resistance. Using measured values for the resistances and transistor β's, current gain values of K_1=1.012 and K_2=1.008 were calculated along with worst case offset current errors of I_{off1}=-1.0969 μA and I_{off2}=-1.0934 μA based on worst case active device tolerances.

Fig. 3.15 shows the accuracy of this type of current mirror. The theoretical curve is simply an ideal, straight line with none of the non-idealities mentioned previously incorporated in it. The I_{o1} and I_{o2} curves show the currents measured across the output

terminating resistances as a function of the input current. The differences between theory and measured data are shown in Fig. 3.16 along with straight lines representing the expected error current due to values of K_1 and K_2 that are greater than unity. The vertical shift between theory and measured curves is the effect of I_{off1} and I_{off2} which can be seen to be much less than half of the worst case values calculated using active device tolerances.

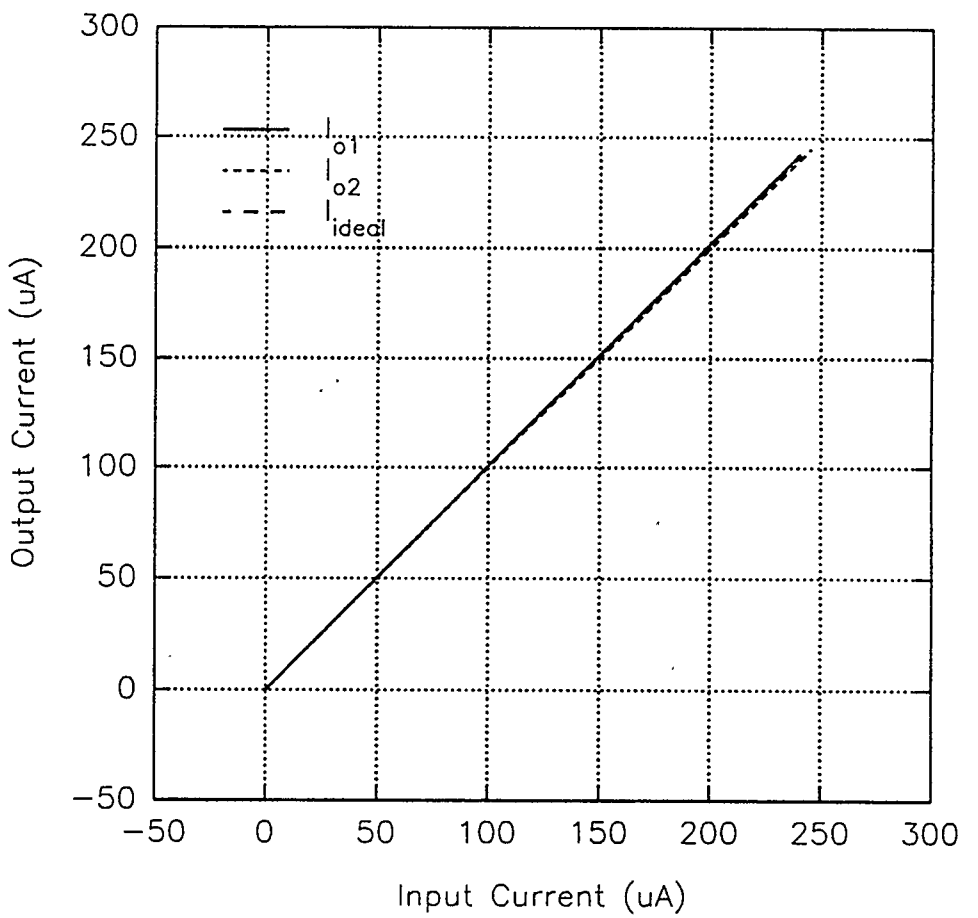

Figure 3.15 - Theoretical and measured input section output currents.

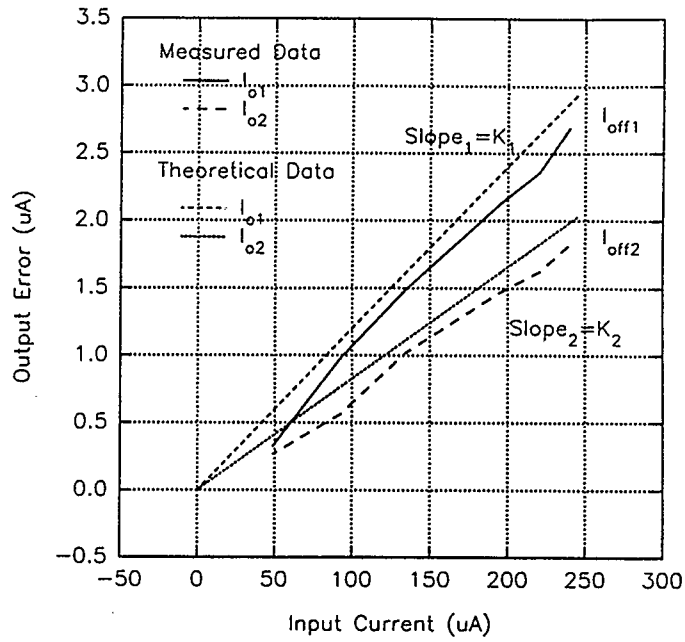

Figure 3.16 - Theoretical and measured input mirror error currents.

3.5.2 Multiplication

The LOTA multiplier was tested in circuit by measuring the output current as the RA1662N and $V_{ref}(n)$ made complete scans of the previous three light sources. To achieve a measure of the error in multiplier output current, plots of the measured output current were made along with plots of the theoretical output current if ideal multiplication were assumed. The difference between these two plots, when plotted against the input photocurrent (I_B) reveals a linear relationship indicating the multiplier gain error

$$\Delta I_{o3}(n) = I_B(n) \cdot \alpha \qquad (3.5.1)$$

where $I_B(n)=I_{o1}(n)$ and $\alpha=16.44\text{x}10^{-3}$. Plots showing that this error current accounts for

the difference between measured data and theoretical data are shown in Figs. 3.19 through 3.20. This gain error is directly attributable to the inherent V_{off} in the LOTA differential pair, as explained earlier and can be accounted for by a value of V_{off} as low as 0.855 mV.

Commercial analogue multipliers were considered and tested in an attempt to remove this multiplier error. However, non-linearities in current-voltage pre and post processing circuits increased circuit complexity and cost, and only marginally better performance, make the use of a commercial analogue multiplier undesirable.

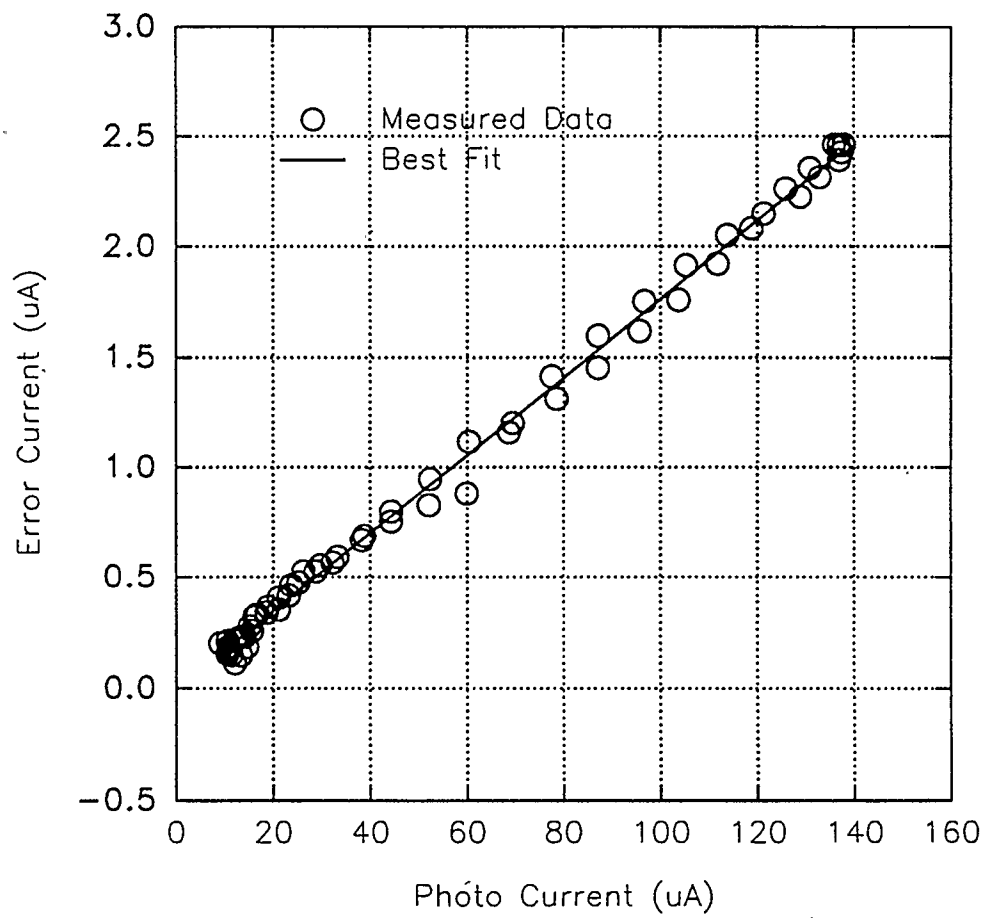

Figure 3.17 - Multiplier output error from source A.

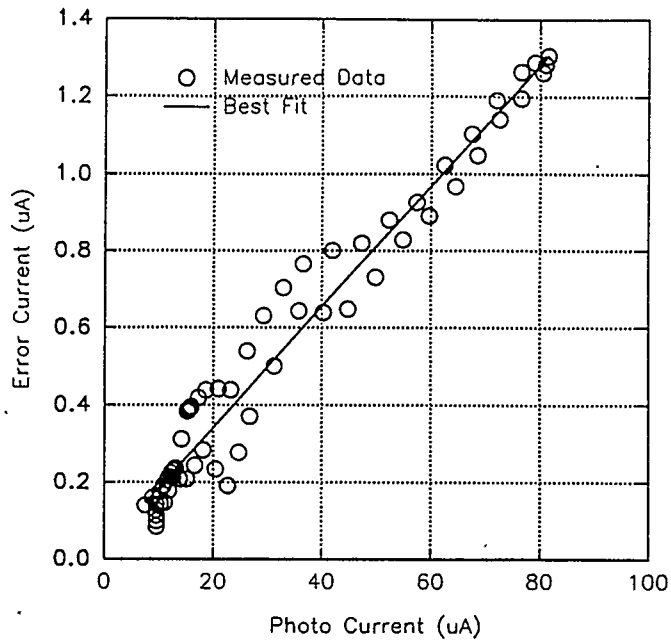

Figure 3.18 - Multiplier output error from source B.

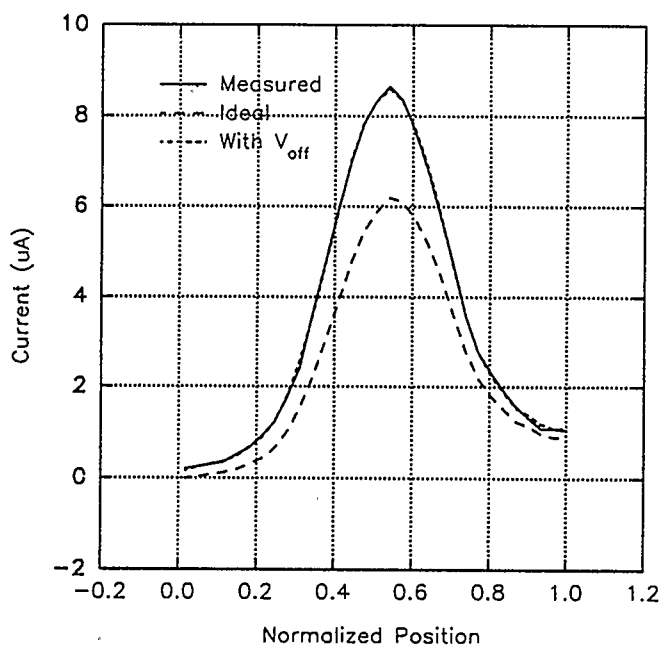

Figure 3.19 - Theoretical and measured multiplier output from source A.

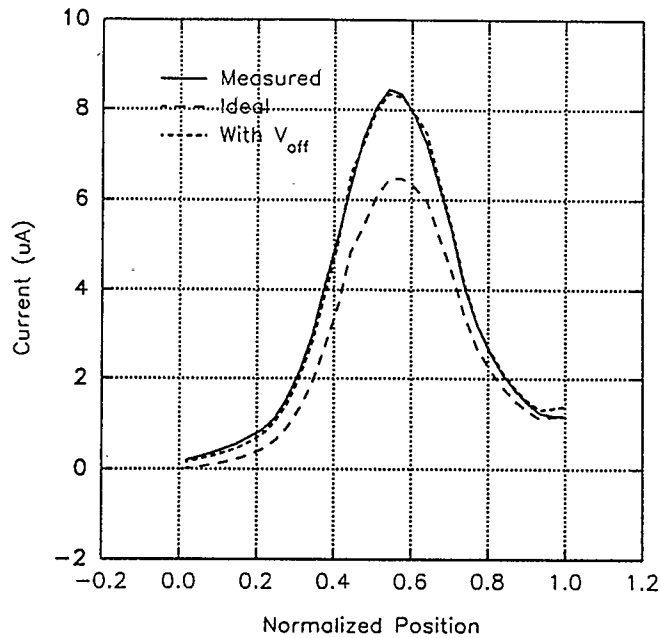

Figure 3.20 - Theoretical and measured multiplier output from source B.

3.5.3 Integration

Fig. 3.21 shows the capacitor voltages V_{c1} and V_{c2} as a function of time normalized to one scan period (and hence normalized to the width of array) when the incident light was bright and uniform across the photoarray. The fact that the light was uniform results in a constant current flowing out of the input section of the circuit. Thus, when this current is directly integrated on a capacitor, the linearly ramping voltage results (V_{c2}). When the constant current is first multiplied by a linearly ramping voltage (resulting in a linearly ramping current) and is then integrated, the second curve results. Fig. 3.22 shows typical integration voltages when the incident light source is a gaussian profile.

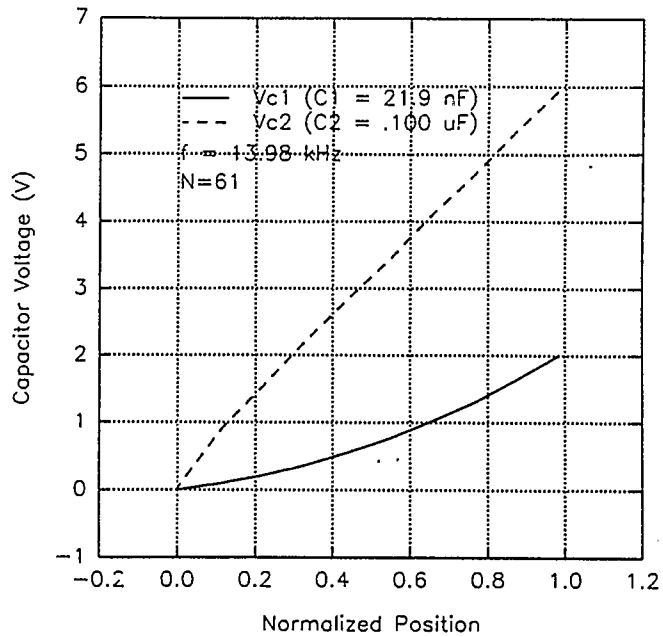

Figure 3.21 - Uniform illumination capacitor charging curves.

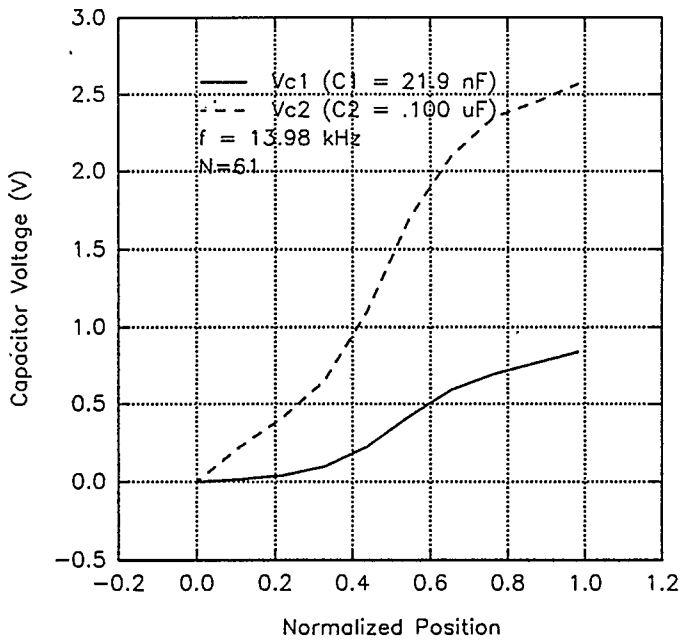

Figure 3.22 - Capacitor charging curves when illumination is a gaussian source.

3.5.4 Signal Output

Figs. 3.23 through 3.25 show the static response of the serial position sensor when each of the three light sources presented earlier are swept across the photoarray. The theoretical data was calculated using the measured component values and three major circuit non-idealities.

The first non-ideality is the offset current added in the input mirrors and whose effect can be seen in Fig. 3.11. The second non-ideality is the effect of multiplier gain error as described earlier. The effect being a shifting of the output voltage curve upwards. Lastly, leakage off the summation capacitors on the order of 300 nA was included. This current is physically the input bias currents on the analogue multiplier amplifiers and has an effect similar to shifting the output curve towards the origin (left).

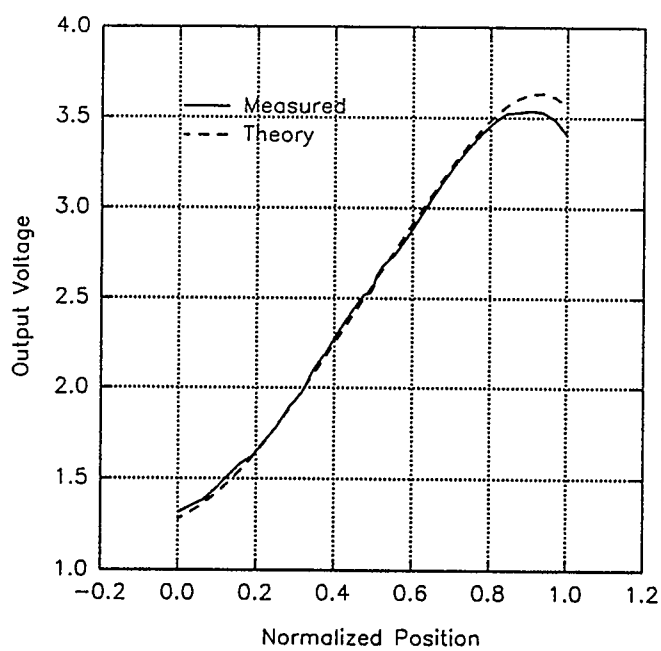

Figure 3.23 - Position sensor static response to source A.

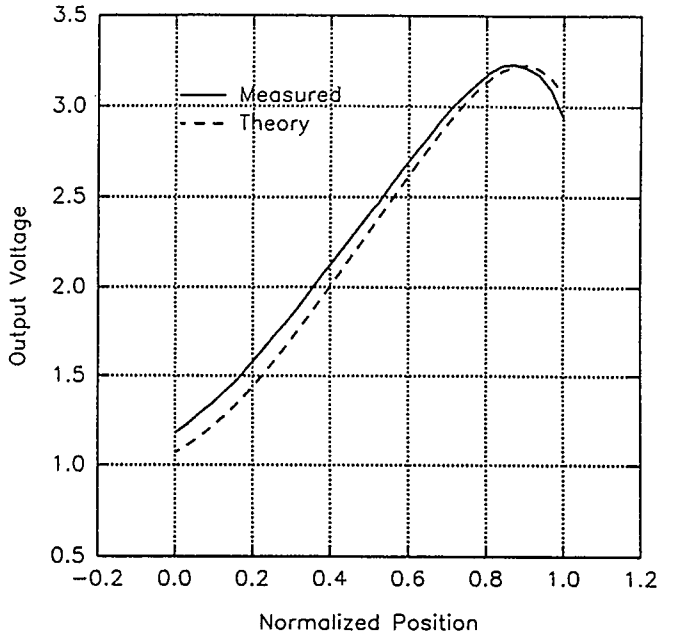

Figure 3.24 - Position sensor static response to source B.

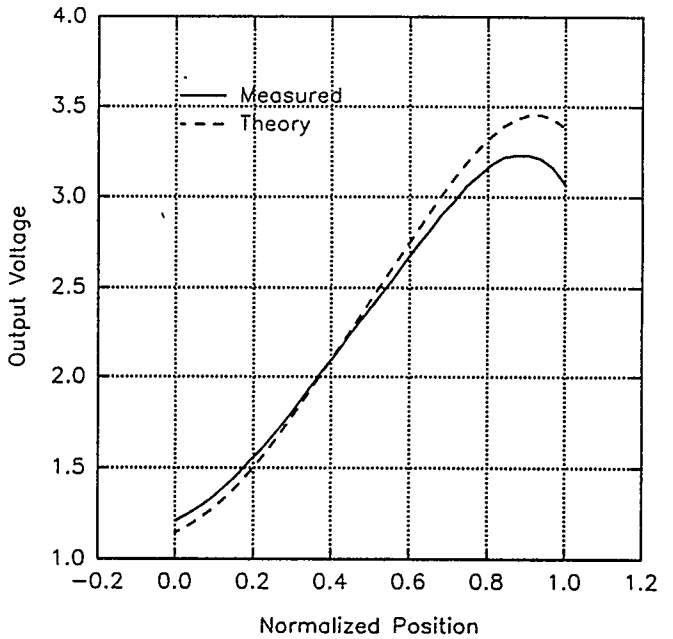

Figure 3.25 - Position sensor static response to source C.

3.6 Conclusions

Further improvements to the shape of the output voltage could be achieved by reducing input mirror offset currents (I_{off}), and buffering the integrating capacitor voltages with low input bias current amplifiers. This would leave the multiplier as the dominant source of error. However, since this is simply a gain error in the output, it can easily be adjusted for by adding or subtracting an offset voltage to the divider output (This feature is usually built into commercial analogue dividers).

The circuit presented in this chapter has been shown to behave in a predictable and desirable manner and as such can be used in control systems requiring low cost, high precision optical position sensing. Greater control over optical integration time also makes this circuit desirable for low light level applications.

Chapter 4

A Telescope Tracking Circuit

The basic (non-serial) position sensor as it currently exists is useful for many applications, one of which is automated telescope tracking for long exposure astronomical photographs [8]. Some deep sky exposures are of the order of 10 hours in length in order to record the very low light levels of distant galaxies. During this exposure time, the stars (and entire sky) will rotate about the polar axis due to the Earth's rotation at approximately 15 degrees per hour, and the telescope must follow this movement with a minimum of error. Typically, the maximum allowable tracking error is of the order of 0.5 arcseconds of angle. Over a 10 hour exposure, even very small errors in drive motor speed and variations in atmospheric refraction will result in tracking errors much larger than those acceptable.

In the past, it was required that an astronomer remain at the telescope to make the necessary tracking corrections every few minutes or seconds depending on the accuracy

of the drive motor. This could be gruelling over the course of a 10 hour exposure.

Currently, at newer observatory installations, CCD systems are used in a feedback arrangement to make the tracking corrections. However, these systems are bulky and costly. The CCD imager must be cooled by liquid nitrogen to reduce CCD dark currents and allow for imaging of the faint stars for tracking, and large computers are necessary to process the incoming CCD data, all resulting in very expensive systems and putting automated tracking out of the price range of the majority of astronomers, the amateurs.

The basic position sensor, however, can be adapted to this cause with very simple control circuitry and therefore at a cost much lower than that for a CCD imaging system. This makes it desirable to develop a telescope tracking system based on the basic OPS system.

The telescope system available for testing was a Celestron 8 inch Schmidt-Cassegrain reflector. The drive motor for this system controls only the right ascension (RA) coordinates, not the declination coordinates, each being a direction in the sky. RA is the direction the earth rotates, and Declination is perpendicular to this direction. The original intent of the motor was to have it plugged into a wall outlet supplying 120 volt RMS 60 Hz electricity with which the synchronous motors drove the telescope in time with the stellar (sidereal) motion. These synchronous motors draw a total of 70 milliamps RMS and dissipate 8 watts. The tracking system will be designed to accommodate these motors.

The tracking system must be capable of using the output voltage from the OPS to correct the speed of the telescope drive motors. In simple terms, if the telescope is

falling behind the rotation of the sky, the control system must be able to increase the speed of the motor and if the telescope runs ahead of the sky, the motor speed must be reduced. There are other considerations that will be broached as they become apparent. Fig. 4.1 shows the block diagram of a simple feedback control system.

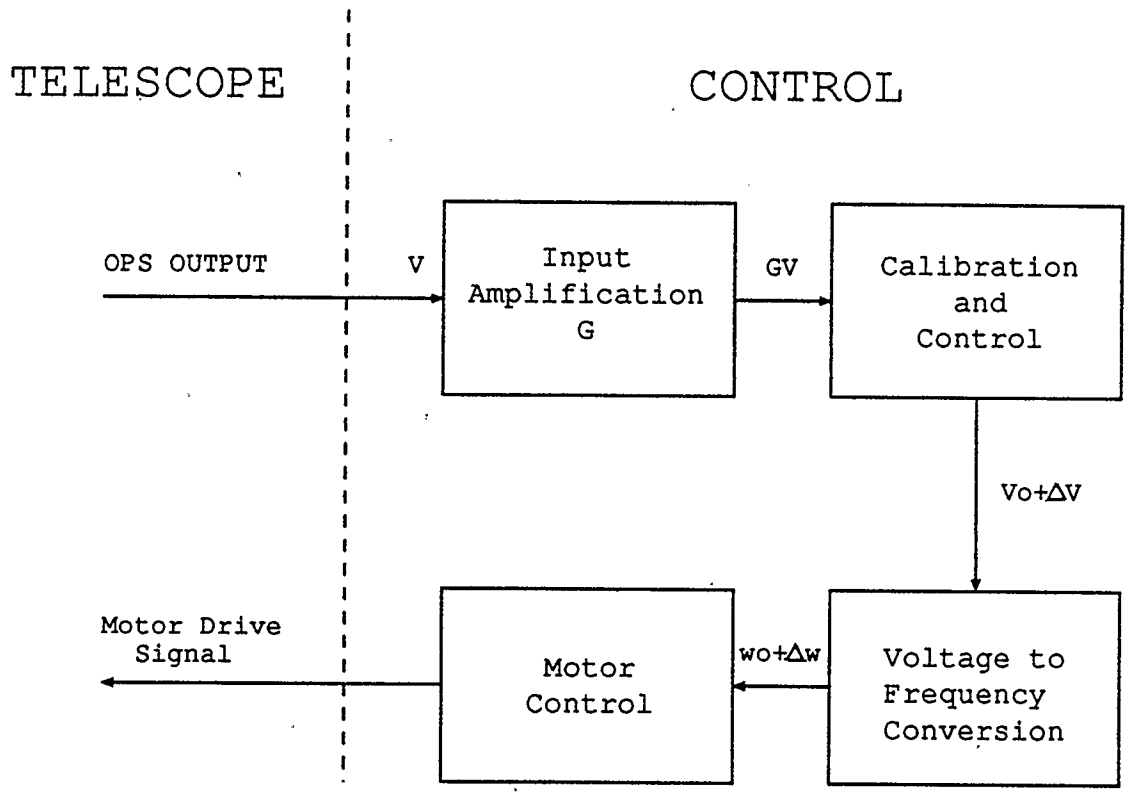

Figure 4.1 - A simple block diagram of a feedback telescope tracking system.

4.1 The Optical System

In order to use the OPS to track, we must first design an optical system to produce two images of the desired starfield. The first image is sent to the camera taking the exposure, and the second must be focused on the OPS array. In order to achieve this, the light cone produced by the main telescope optical system must be passed through a beam splitter, as in Fig. 4.2, or an "off axis" splitter, as in Fig. 4.3, to produce the two focal planes. Each of these methods results in reducing the light flux (watts/cm^2) contained in either of the two resulting images. The beam splitter will produce two images of the starfield each with an flux of

$$F_{camera} = \alpha \, F_{photo} \tag{4.5.2}$$

and

$$F_{OPS} = (1-\alpha) \, F_{photo} \tag{4.5.3}$$

where F_{camera} is the optical flux incident at the camera, F_{OPS} is the optical flux incident on the OPS, F_{photo} is the total optical flux in the light cone, and α is the beam splitter's transmission coefficient which is assumed to be uniform across the entire optical spectrum. Use of the off-axis splitter results in

$$F_{camera} = \left(1 - \frac{A_{offaxis}}{A_{cone}}\right) F_{photo} \tag{4.5.4}$$

and

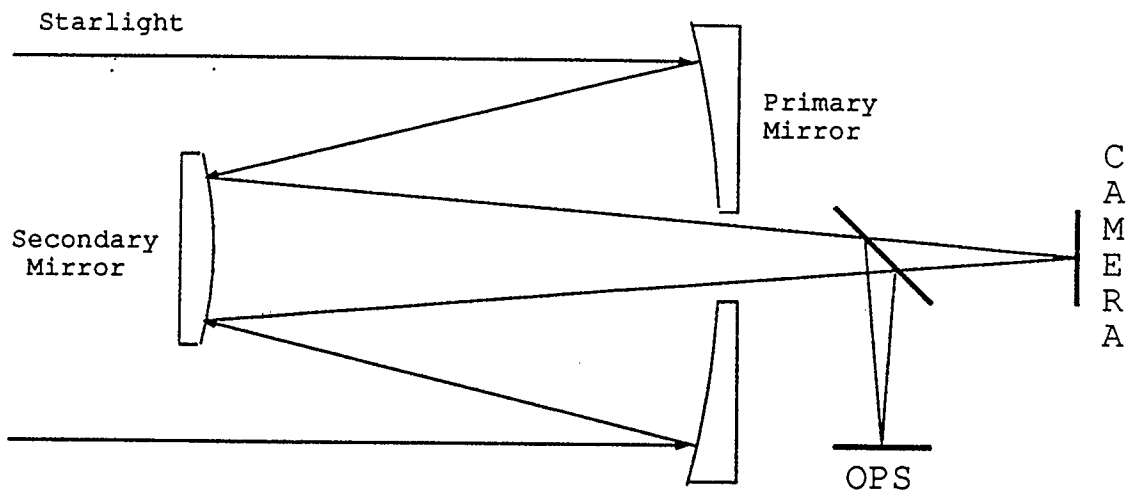

Figure 4.2 - Beam splitter based optical system.

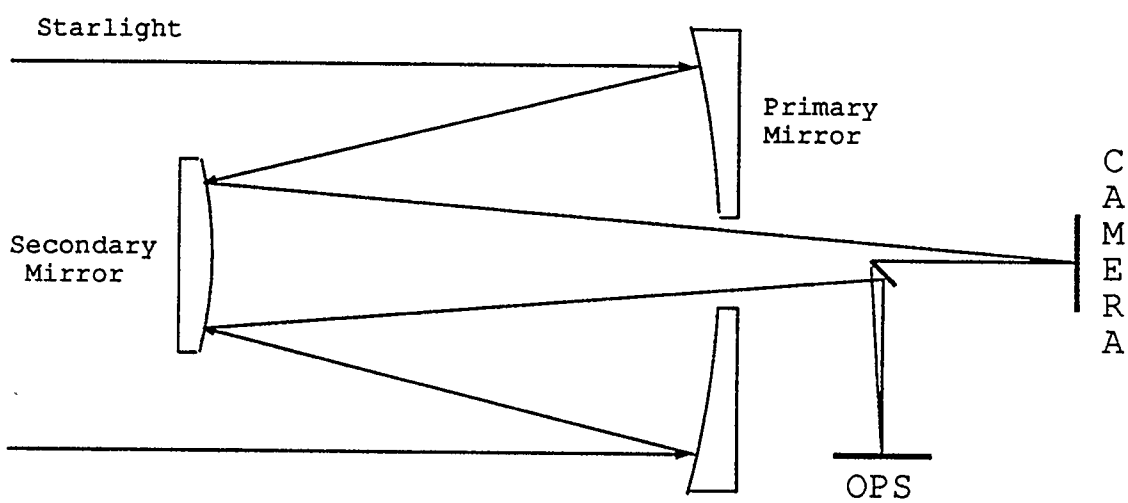

Figure 4.3 - Off axis splitter based optical system.

$$F_{OPS} = \frac{A_{offaxis}}{A_{cone}} F_{photo} \tag{4.5.5}$$

where $A_{offaxis}$ is the area of intersection of the off axis mirror and the light cone, A_{cone} is the area of the light cone at the off axis mirror, and everything else is as above.

Another difference between the two splitting methods is the image at the OPS. If the beam splitting method is used, the image at the OPS will be identical to that at the camera with only a difference in brightness. If the off-axis method is used, the OPS image will only be a part of the edge of the camera image and a small piece off the edge of the camera image will be missing.

After producing these two images, they may be treated separately by any further optics to produce various levels of magnification. For the purposes of this thesis, however, the images were left at prime focus. That is, the images formed by the main optical system were used as is with no further magnification or manipulation.

The power of light incident at the focal plane depends upon many factors, the most important of which is the intensity of the star itself. Stellar brightness is measured in a unitless relative quantity "magnitude" in such a way that

$$M_2 - M_1 = -2.5 \log\left(\frac{F_2}{F_1}\right) \tag{4.5.6}$$

where M_1 and M_2 are the astronomical magnitudes of two stars in some bandwidth and F_1 and F_2 are the star's flux values (watts/cm^2) in the same bandwidth. The best magnitude to compare everything else to is the solar magnitude or constant as it is well

measured and defined. The sun has a magnitude of -26.4 and a flux of 0.137 watts/cm^2 just outside the Earth's atmosphere. The atmosphere however, acts as a filter to light, passing some frequencies and absorbing others as seen in Fig. 4.4 [9]. Thus less light flux than expected will reach the telescope.

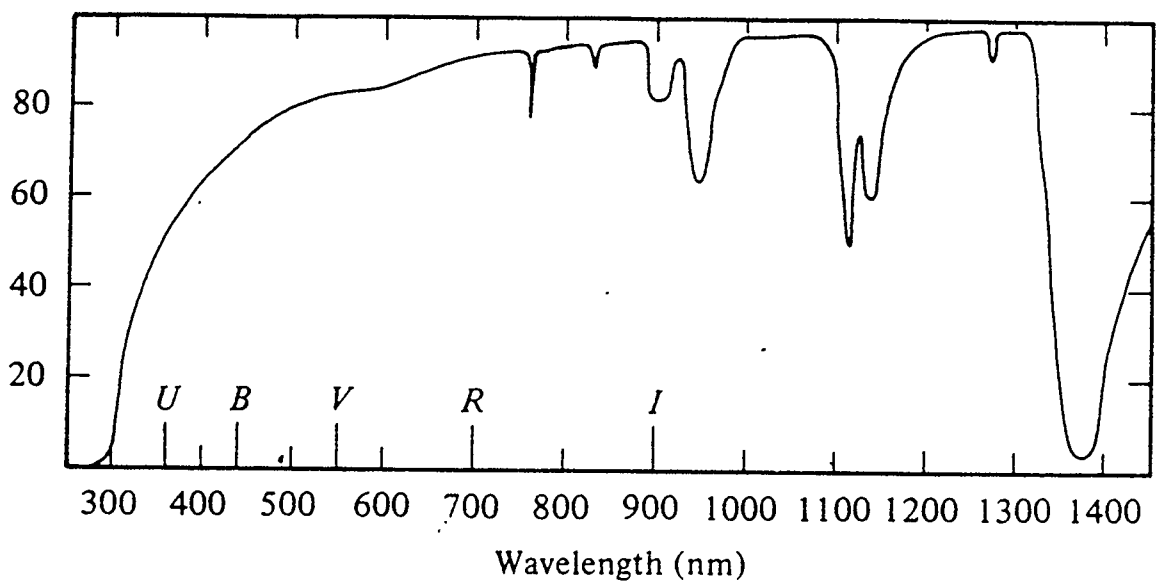

Figure 4.4 - Typical plot of percentage atmospheric transmission.

Physical properties of the telescope itself also affect the amount of light power incident at the focal plane. These include the area of the telescope aperture, the stellar image size, and the reflectance and transmittance of the telescope mirrors and lenses respectively. The area of the telescope's aperture is well known, and the size of the stellar image can be calculated. It will have an angular size limited by the larger of either atmospheric turbulence effects (limiting the angular diameter to approximately $D_T \approx 1.0$ arcsec) or internal telescope diffraction effects,

$$D_I \approx \frac{0.252\ \lambda}{D_T} \tag{4.5.7}$$

where D_I is the angular stellar image size expressed in arcseconds, D_T is the telescope aperture diameter in mm and λ is the light wavelength in nm. The actual stellar image size at the focal plane can then be expressed as

$$A_I \approx \frac{\pi\ D_I\ F_{eff}}{412512\ arcsec} \tag{4.5.8}$$

where A_I is the area of the image, and F_{eff} is the telescope's effective focal length expressed in the same units as A_I [10].

The reflectance and transmittance of the telescope's optics will vary greatly from instrument to instrument and will be largely affected by the materials used to form the optics in the instrument [11]. Typical reflectivities and transmittances may be seen in Fig. 4.5.

A full description of the light flux incident at the stellar image of a reflecting telescope can be written

$$F_I \approx F_A \cdot \tau_{atm} \cdot \frac{A_T}{A_I} \cdot \tau_P \cdot \tau_S \cdot \tau_I \tag{4.5.9}$$

where F_I and F_A are the light fluxes at the image and outside the atmosphere respectively, A_T and A_I are the areas of the telescope aperture and stellar image (from Eqn. (4..5.8)) respectively, τ_{atm} is the spectral atmospheric transmission (approximately 0.7 @ 550 nm), and τ_P, τ_S and τ_I are the spectral transmissions of the primary mirror (approximately 0.8), secondary mirror (approximately 0.8) and focusing lens respectively (approximately 0.9).

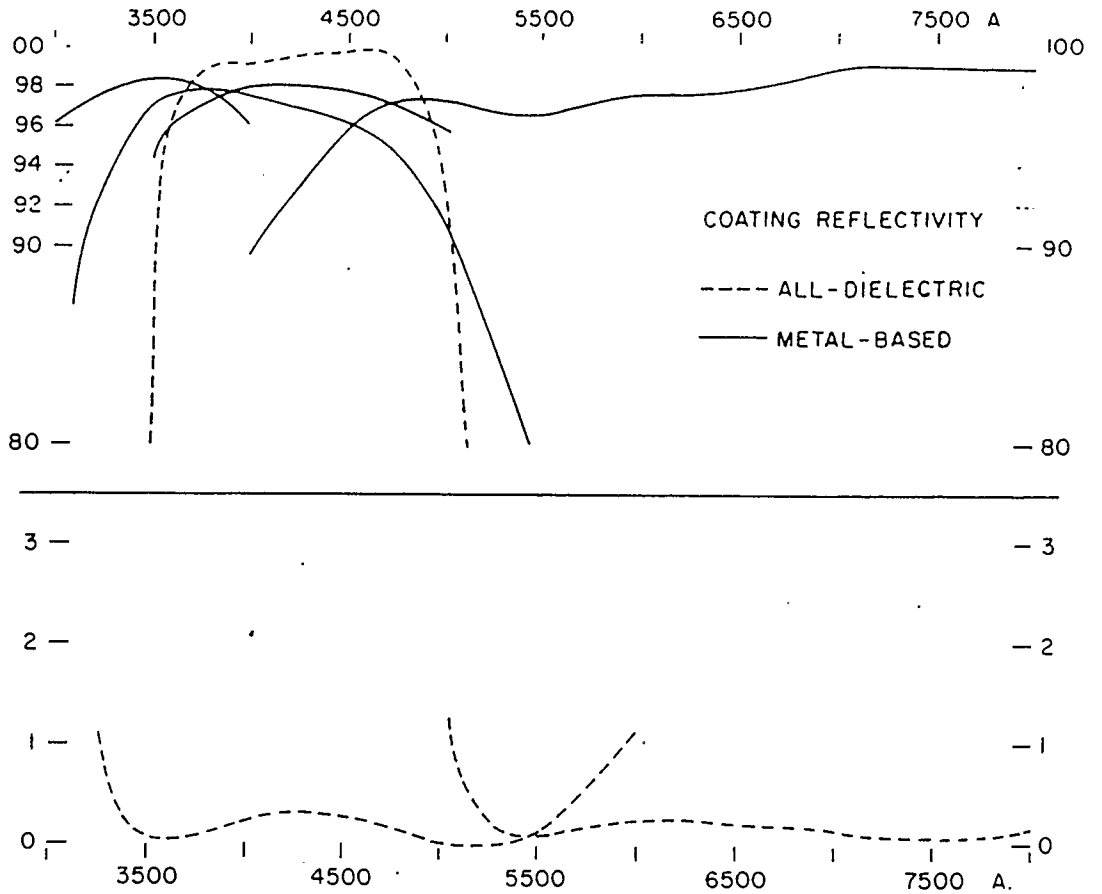

Figure 4.5 - Typical telescope percentage reflectances and transmittances.

It is important to note that the τ_x values are in fact spectra which can not be fully represented by any single number. Using these values and assuming the use of an 8 inch diameter, 10 foot effective focal length telescope at 550 nm, the published value for photosensor sensitivity of 2nA/μwatt/cm^2 and detector size of 84 microns by 90 microns, the following table was produced.

Stellar Magnitude (Unitless)	Image Flux ($\mu W/cm^2$)	Calculated Photocurrent (pA)
0.00	220.00	332.640
1.00	87.65	132.530
2.00	34.89	52.750
3.00	13.89	2.100
4.00	5.530	0.836
5.00	2.200	0.333
6.00	0.877	0.133
7.00	0.349	0.053
8.00	0.139	0.021

Table 4.1 - Stellar magnitude and expected image flux and current values.

4.2 Input Amplification and Calibration

With a star field incident upon the OPS array, it will produce some output voltage dependent upon the centroid of the incident light. The many points of light in the starfield can be assumed to be a single object. Thus, if the starfield image were to shift, the OPS output would also shift providing the control circuitry with a means of determining whether the tracking motor is falling behind or getting ahead of the sky and thereby closing the feedback control loop.

At the low light levels involved in stellar images, second order effects within the OPS reduce the full scale output of the OPS greatly. For this reason, and to reduce the

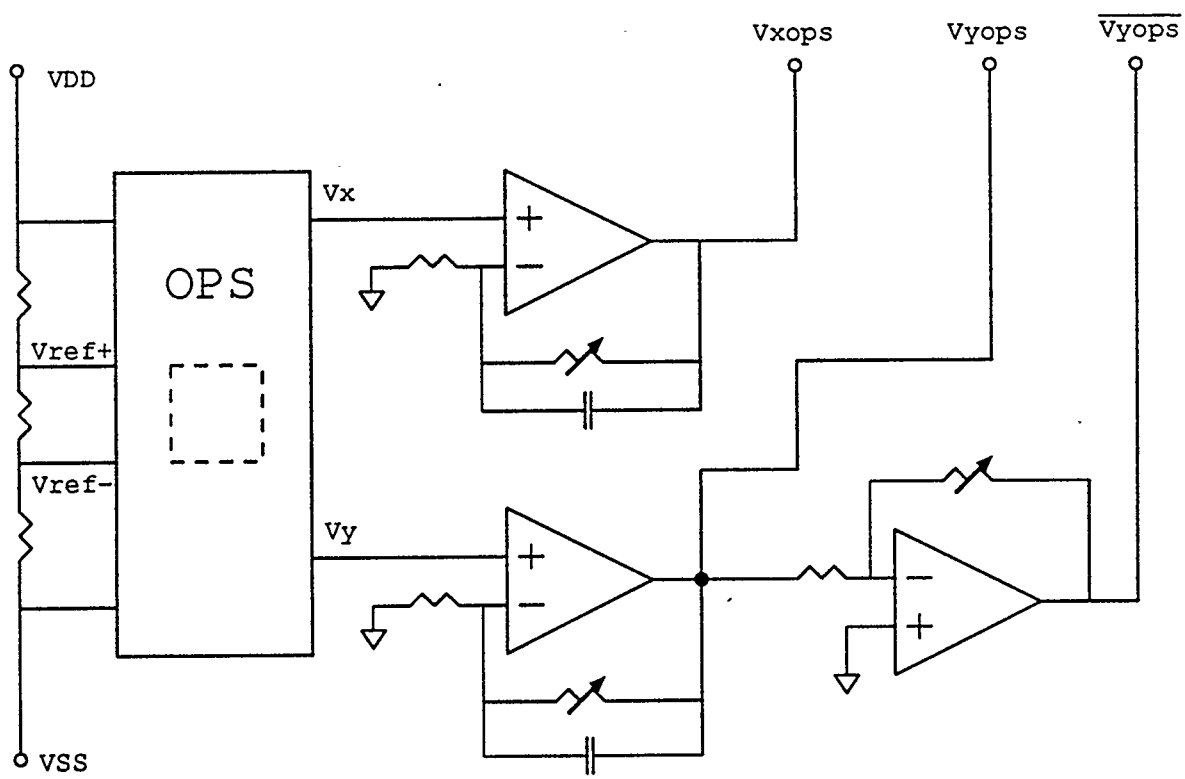

Figure 4.6 - Eyepiece amplification section of the tracking system.

effects of noise pickup problems, the output signal from the OPS must be amplified prior to any further uses. The benefits are twofold; the OPS output signal is buffered, and the noise incurred during signal transmission is reduced. For the circuit designed, the input amplifier gain was made adjustable from 10 to 500 with allowances for lowpass filtering the signal if need be.

The position of the centroid of the starfield may appear anywhere in the array. For tracking purposes, there must be some accommodation for this by permitting the telescope to be positioned, and then "locked on" to the current centroid output position. The control circuitry following the "locking on" or calibration circuitry will always try to maintain the OPS output signal at zero volts. This is considered to be the tracking origin. In order to "lock on" to any output voltage from the OPS, the calibration circuitry must be able to shift the origin of the output signal by either adding or subtracting a constant voltage to the OPS output.

Calibration can be accomplished by sampling/holding the OPS voltage at the press of a button, and then by subtracting this held voltage from the current OPS output. The effect is a shift in the corrected OPS voltage so that the centroid position when the calibration button was pressed becomes the new origin with a corresponding output of zero volts. The sample/held voltage must be maintained for the entire duration that tracking is desired which can be very long periods of time. For this reason, an infinite sample/hold circuit was built and is shown in Fig. 4.7.

Infinite sample/hold operation is straight forward. The output voltage of a counter driven digital to analogue converter (DAC) is first compared to the OPS signal. The

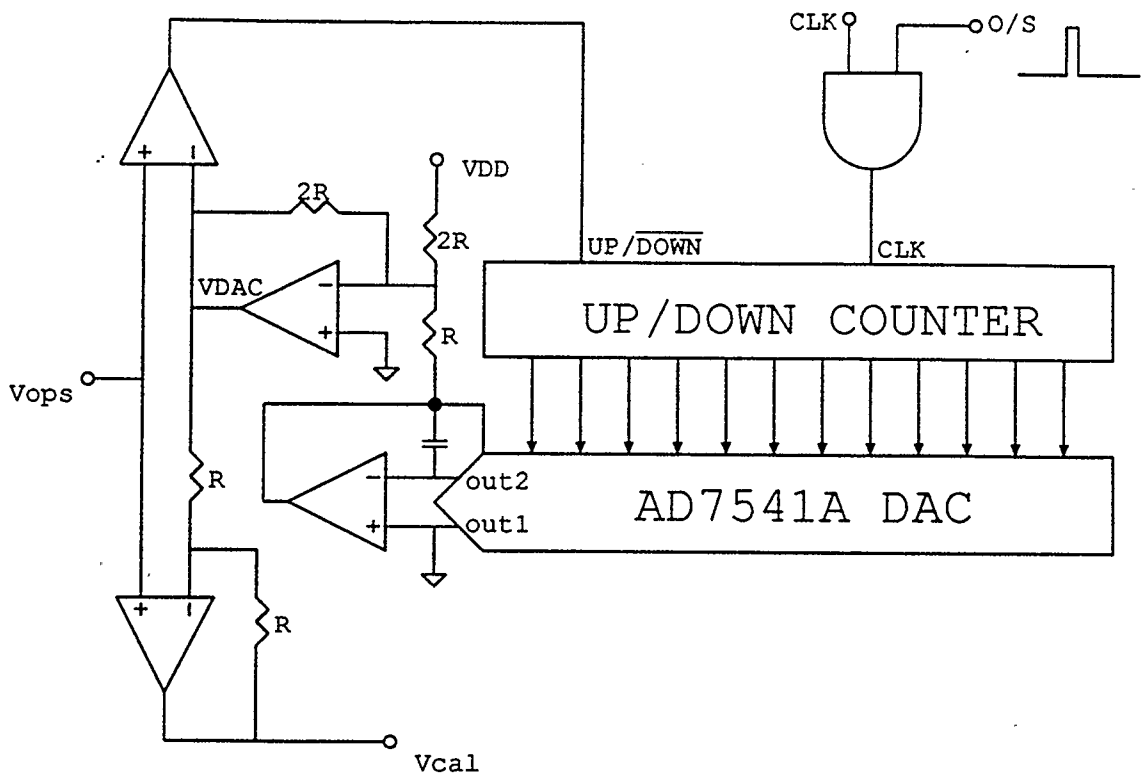

Figure 4.7 - An infinite sample/hold circuit.

resultant comparator output, taken as a digital signal, provides information to the counter as to whether it should count up or down to raise or lower the DAC output voltage. After a maximum period of time determined by

$$\tau = 2^m T_{clk} \tag{4.2.1}$$

where τ is the maximum settling time, m is the number of bits for the counter and DAC's digital connection, and T_{clk} is the period of the counter clock, the voltage at the output of the DAC will be within 1/2 bit resolution to the OPS signal, and counting can stop. This voltage may now be subtracted from the OPS signal to produce a new origin.

In order to control this calibration scheme with a single push button, the button must be connected to a one-shot, the output of which will remain high for a minimum duration of τ. This signal may then be used to gate the clock to the counter.

Through this process, we have generated a bipolar signal (V_{cal}) which can be calibrated with the push of a single button which indicates the relative difference between the current centroid position, and the calibrated centroid position.

4.3 Frequency Control Voltage Production

The image of a star under magnification will always be seen to flicker or move around by a small amount due to atmospheric turbulence between the telescope and the star. This effect is akin to viewing a distant street lamp through rising heat waves on a hot night. For the tracking system to behave properly, it is imperative that the telescope not respond to these rapid position changes, only to the slow tracking errors. For this reason, a damped space circuit was built into the control circuitry.

The typical static response of this type of circuit can be seen in Fig. 4.8. The flattened area at the centre of the distribution reduces the output voltage relative to the input voltage so that changes in input voltage (from the OPS) that do not deviate greatly from the calibrated "locked on" point do not produce large output voltages variations. If, however, the gained and corrected OPS voltage, V_{cal}, deviates from the "locked on" point by a large amount, larger output voltages result. Since this output voltage will be linearly

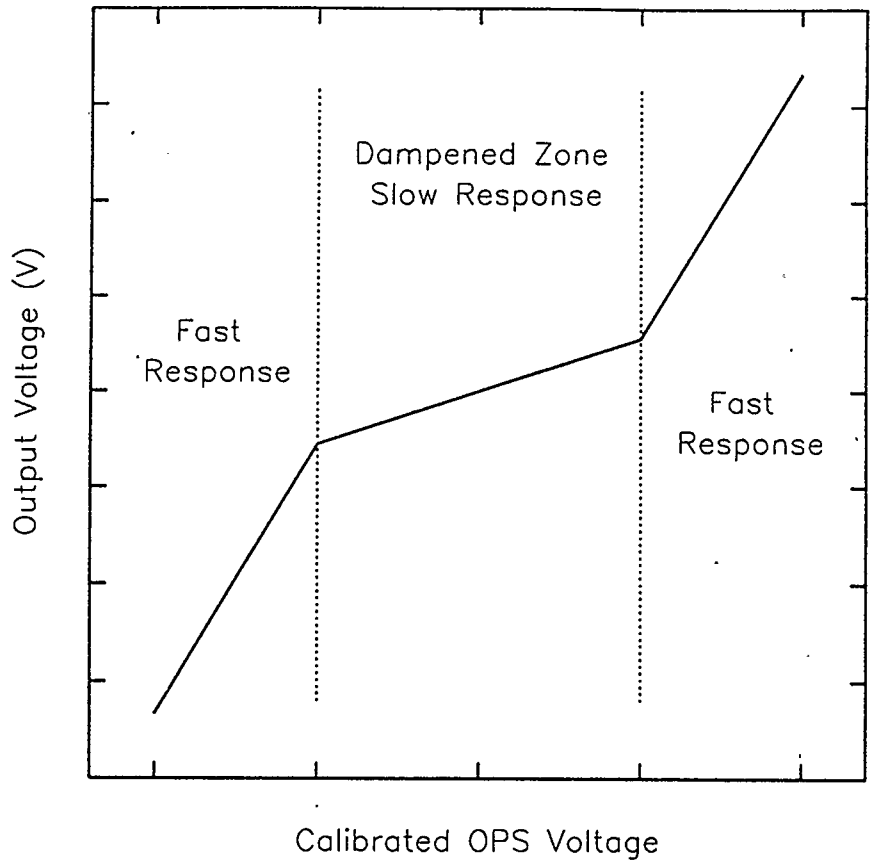

Figure 4.8 - Dampened space circuit typical static response.

related to the motor frequency, the motor speed response of the tracking system to small variations in OPS image position will be slow.

A block diagram of a system to create the desired response is shown in Fig. 4.9 and consists of two precision rectifiers (both negative and positive), an inverting amplifier, a summing amplifier, and an offset adjust amplifier. The schematic of the complete system is shown in Fig. 4.10.

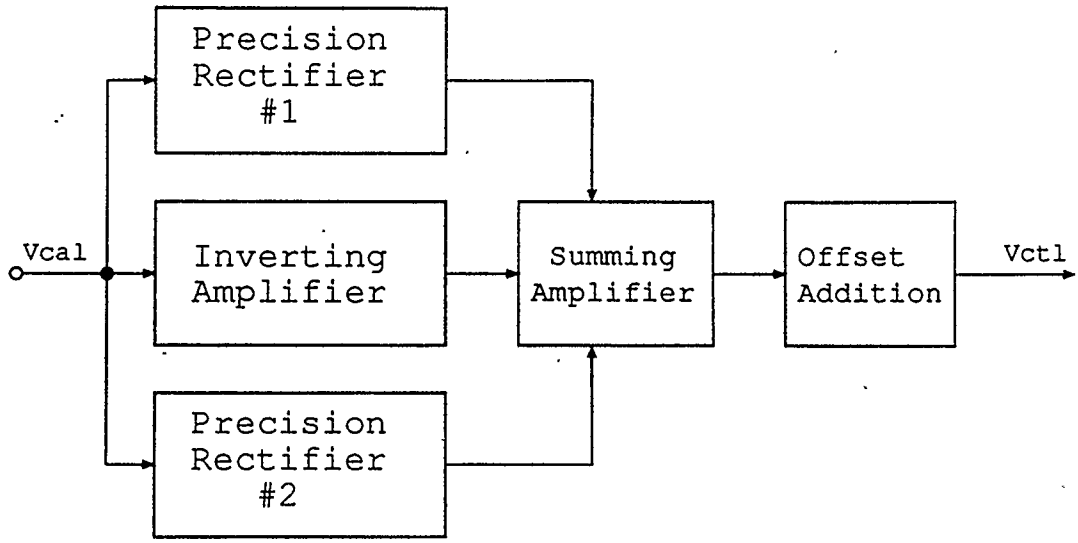

Figure 4.9 - The block diagram of a dampened response circuit.

Each precision rectifier has two states. In one state, the diodes are conducting and the amplifier behaves as a buffer and in the other state, the diodes are reverse biased and the amplifier behaves as an inverting amplifier. Each rectifier has an additional current input (through R1 and R2 respectively) to shift the input voltage at which the change from one state to the other occurs.

Precision rectifier #1 has a response as shown in Fig. 4.11 if the diodes are matched. The change in states occurs when the sum of currents at the inverting pin of the opamp is zero or when

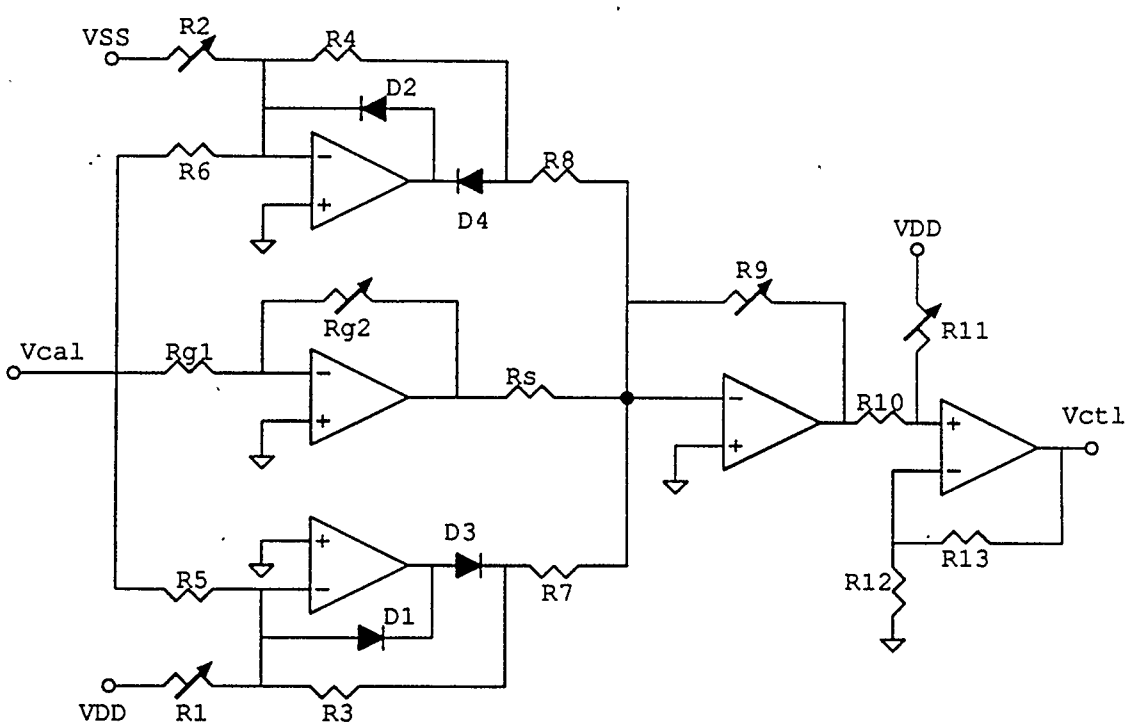

Figure 4.10 - Schematic of a dampened space circuit.

$$V_{in} = -\frac{R_6}{R_2} V_{ss} \tag{4.3.1}$$

where V_{in} is the gained and calibrated OPS output and V_{SS} is the lower supply voltage. Below this value, the output voltage is zero. Above it,

$$V_{ol} = -\frac{R_4}{R_6} V_{in} = G_1 V_{in} \quad . \tag{4.3.2}$$

The same type of response holds for precision rectifier #2 and is shown in Fig. 4.12 with the change in states occurring at

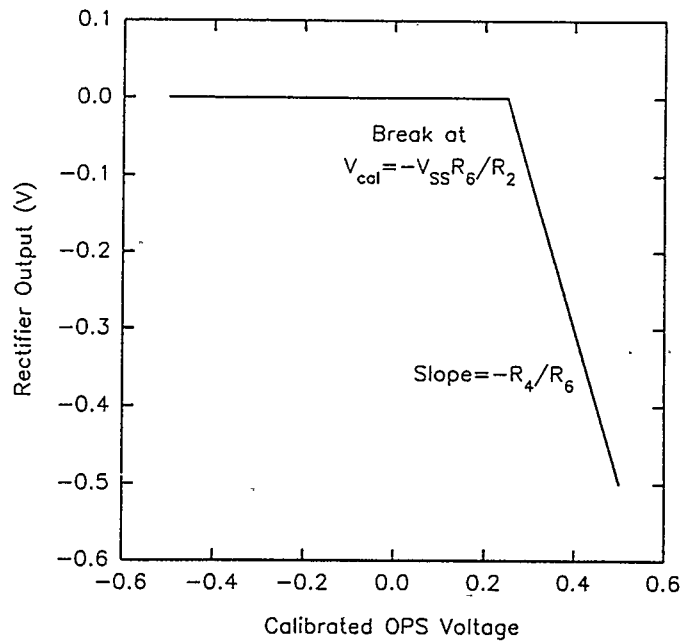

Figure 4.11 - Precision rectifier #1's static response.

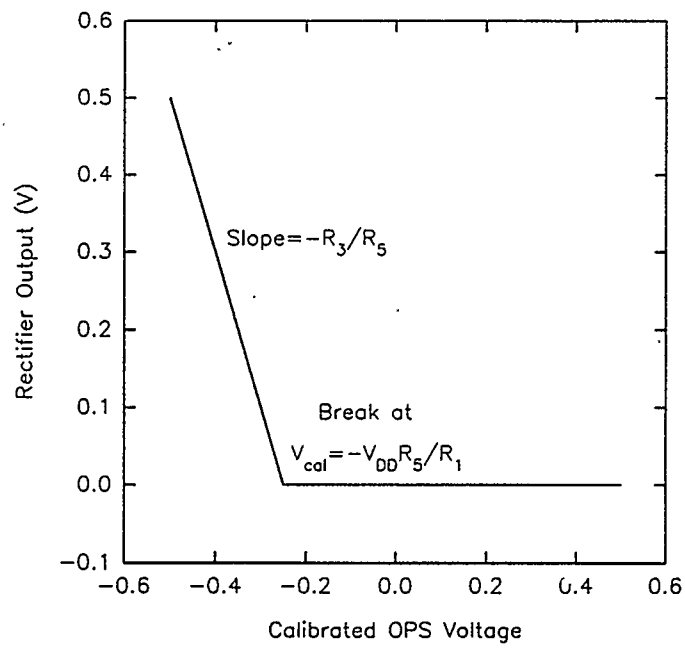

Figure 4.12 - Precision rectifier #2's static response.

$$V_{in} = -\frac{R_5}{R_1} V_{DD} \tag{4.3.3}$$

where V_{DD} is the upper supply voltage and below this value

$$V_{o2} = -\frac{R_3}{R_5} V_{in} = G_2 V_{in} \quad . \tag{4.3.4}$$

When the two outputs of the precision rectifiers are added along with an inverted V_{in},

$$V_S = -\frac{R_{G2}}{R_{G1}} V_{in} = G_3 V_{in} \tag{4.3.5}$$

by a amplifier of gain G_4 (a negative gain), the resulting static response is as shown in Fig. 4.13.

Finally, an offset voltage determined by R_{10} through R_{13} can be added to the response shown in Fig. 4.13 and the signal can be gained again by a factor G_5 creating the complete control voltage for voltage to frequency conversion. This response has all the characteristics we set out to achieve; by allowing R_1 and R_2 to be adjustable the width of the dampened zone may be controlled, all static transfer slopes have been made controllable through variable resistors, and by adding the offset voltage, the free running speed of the system can be set.

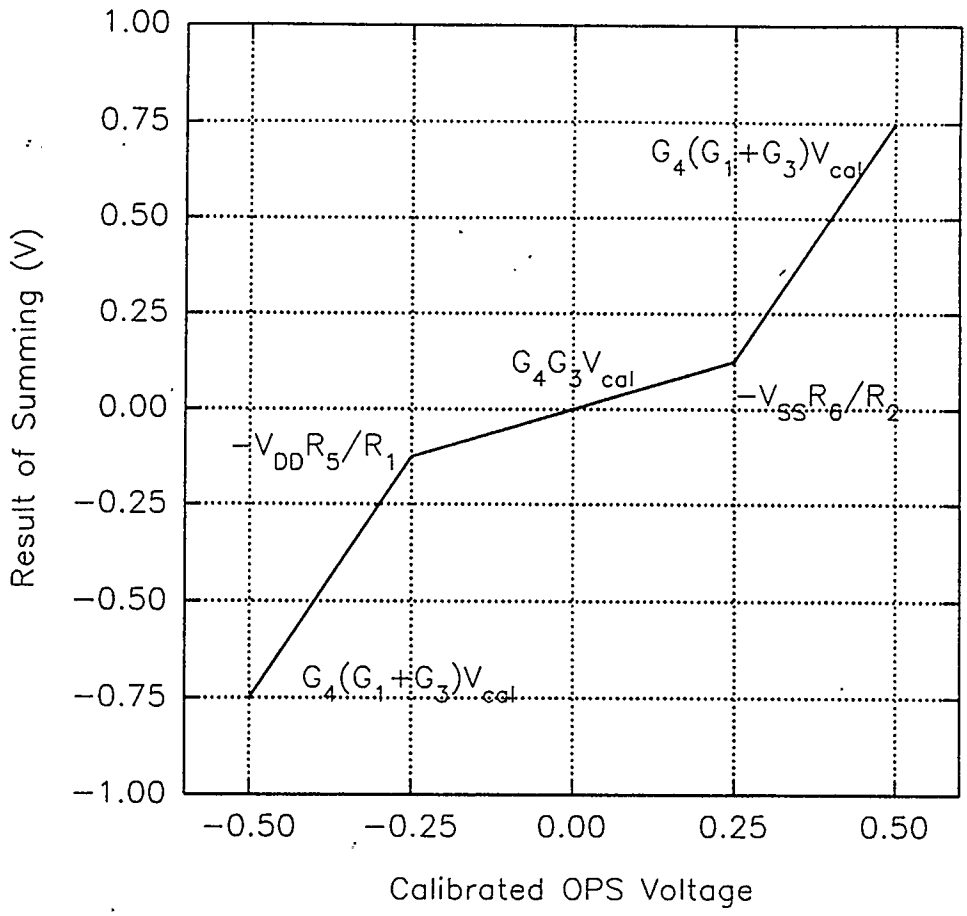

Figure 4.13 - Addition of the precision rectifiers' output and inverted V_{cal}.

4.4 Voltage to Frequency Conversion

Voltage to frequency conversion was performed using the simple 555 timer circuit shown in Fig. 4.15 that had a free running frequency of 120 Hz. This includes a CMOS flip-flop to halve the generated frequency and ensure a square wave, and non-overlapping clock circuitry. For the 555 timer, the output clock will be high during the time

$$T_{high} = (R_1+R_2)C \ln\left(\frac{V_{DD} - \frac{V_{SS} - V_{in}}{2}}{V_{DD}-V_{in}}\right) \tag{4.4.1}$$

and low during the time

$$T_{low} = R_2C \ln(2) \tag{4.4.2}$$

where all parameters are as shown in Fig. 4.15. The resulting frequency, after halving by the flip-flop will be

$$f_{motor} = \frac{1}{2(t_{low} + t_{high})} \quad . \tag{4.4.3}$$

A plot of Eqn. (4.4.3) can be seen in Fig. 4.14. While this response is not perfectly linear, for this control system it serves its function very well.

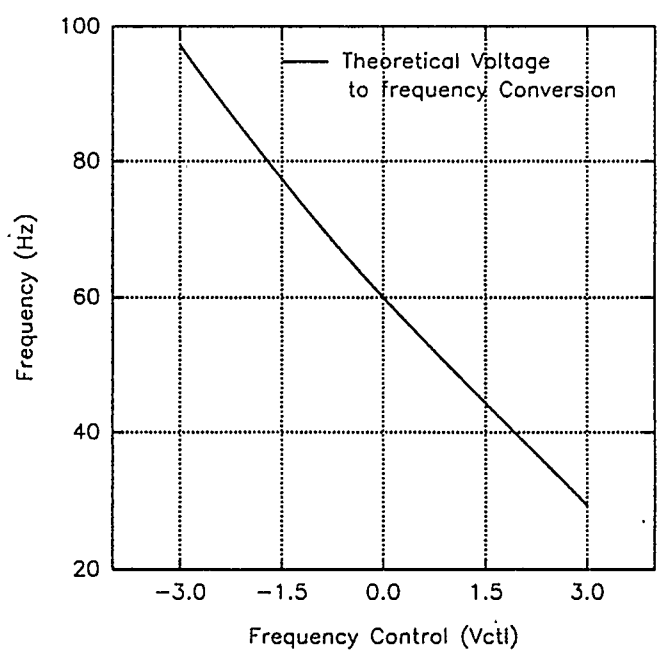

Figure 4.14 - Plot of the theoretical voltage to frequency response.

After production of this CMOS level square wave motor driving signal (CLK), it must be inverted to produce CLKNOT so that both may be supplied to the motor driving circuitry. However, since CLK and CLKNOT are meant to modulate high voltage positive and negative DC voltages it is imperative that CLK and CLKNOT are non-overlapping so that short circuits when both signals are "high" are avoided. To perform this feat, the subcircuit shown in Fig. 4.15 was devised and production of the clocks took the final form shown in Fig. 4.16.

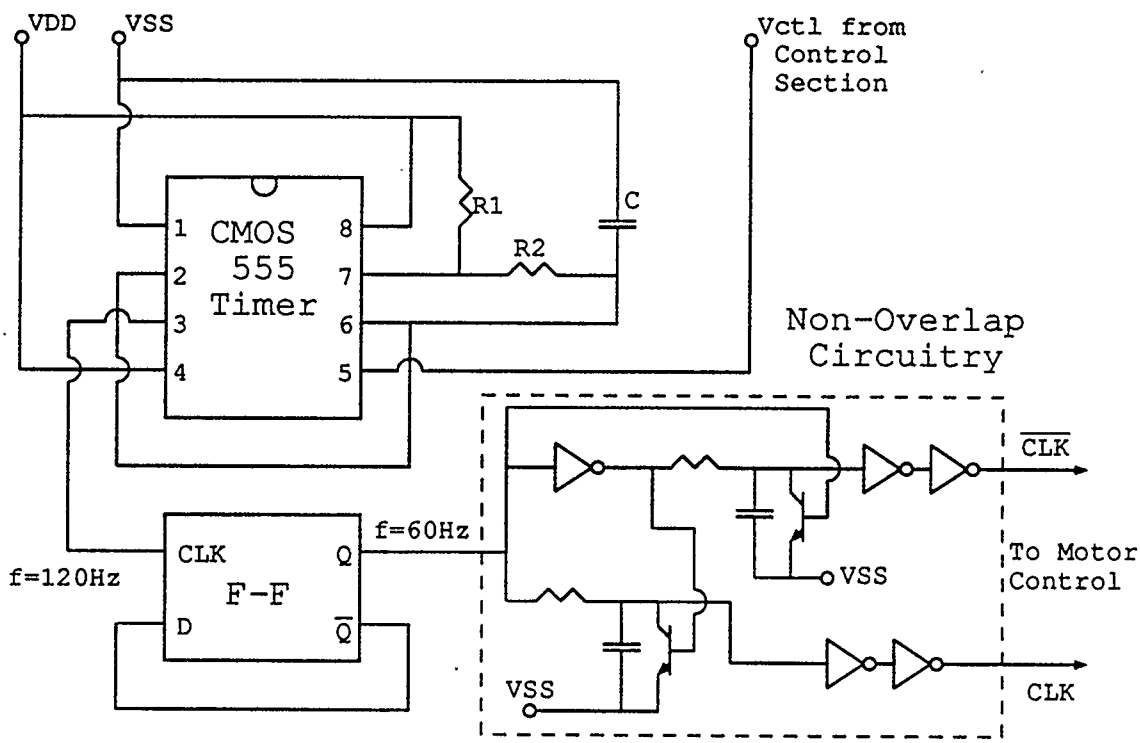

Figure 4.15 - Voltage to frequency convertor.

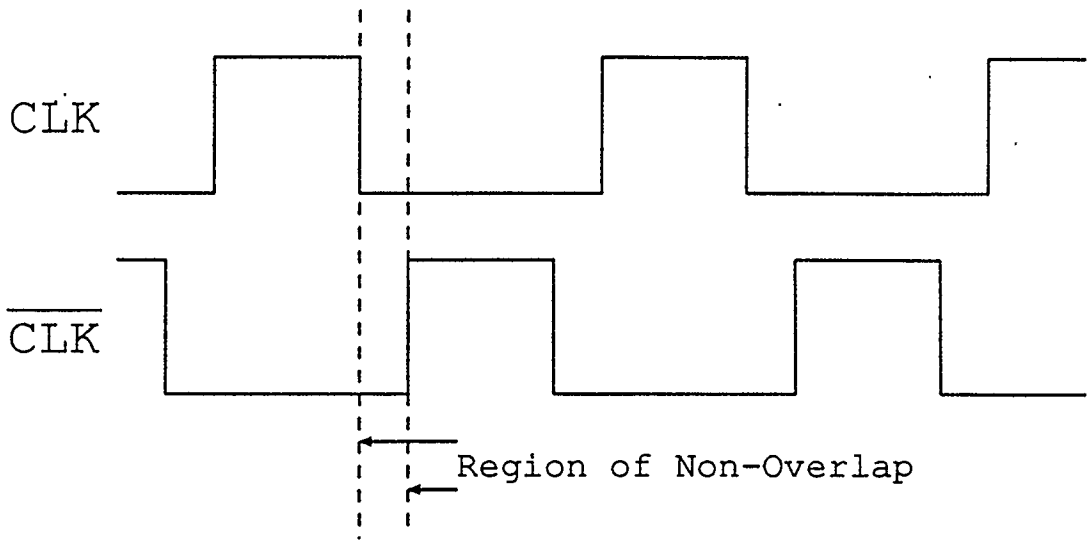

Figure 4.16 - The resulting motor driving signals CLK and CLKNOT.

4.5 Drive Motor Control

The above generated clock, CLK, along with its non-overlapping inverse, CLKNOT, may now be used in the circuit shown in Fig. 4.17 to modulate both +100 and -100 VDC signals respectively to drive the telescope motor. The conversion of the CMOS level signals to the high voltage motor signal was performed by the use of high voltage opto-isolators as shown in Fig. 4.17. These opto-isolators could not supply the 70 mA necessary to drive the telescope motors, so the resulting signal was used to drive a simple class B amplifier consisting of power transistors Q_1 and Q_2. The signal subsequently supplied to the telescope motor appears in Fig. 4.18.

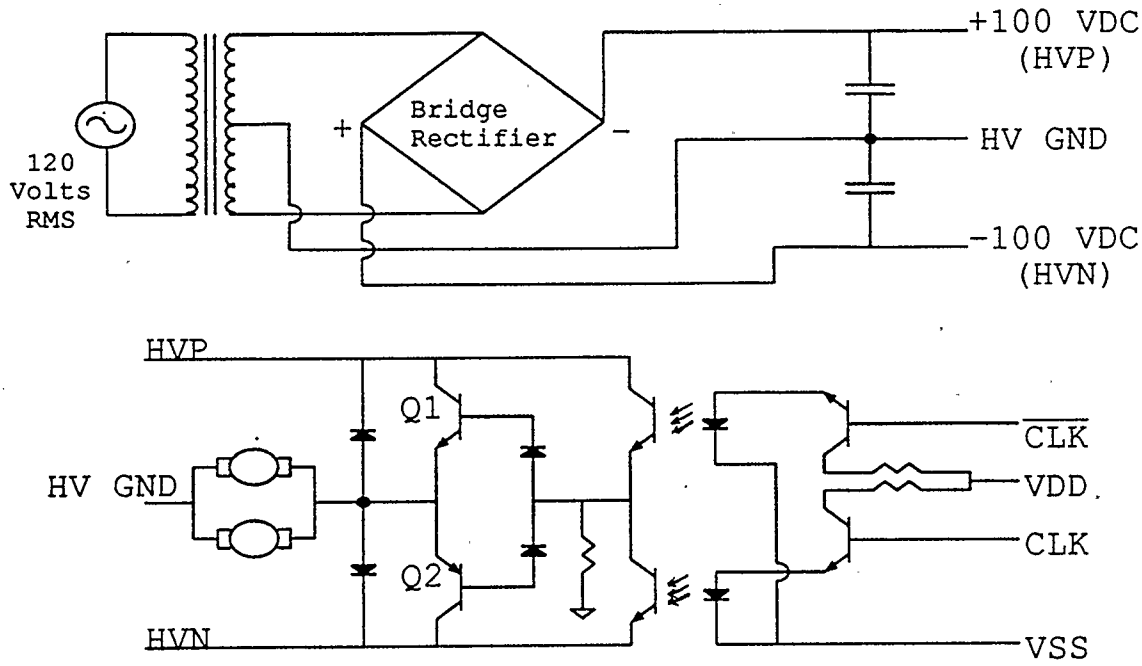

Figure 4.17 - Motor control.

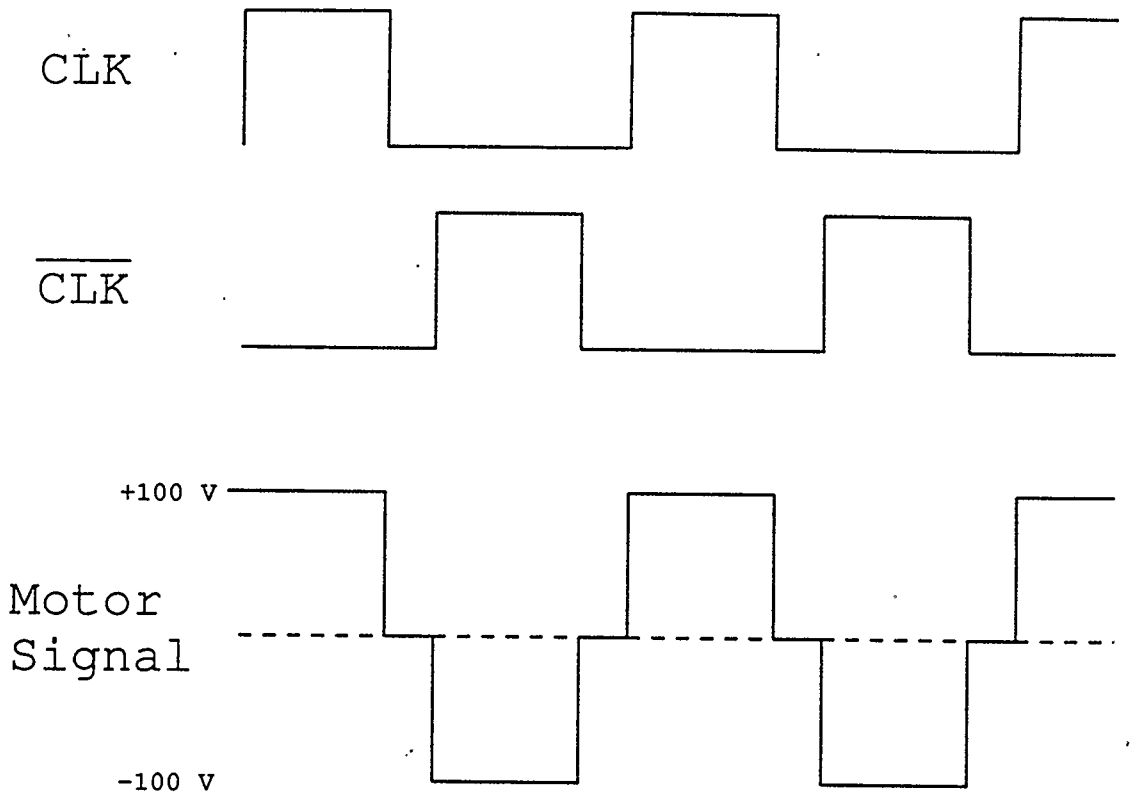

Figure 4.18 - The motor driving voltage signal.

4.6 Testing and Results

All testing was performed in circuit under one of two conditions; where possible, laboratory testing was performed, and field testing was performed on both the 8 inch Celestron telescope that was available and a smaller 130mm Newtonian reflector telescope.

4.6.1 Input Amplification and Calibration

Because of the nature of these circuits, and the extent to which they were designed to be adjustable, little data is available for comparison to theoretical values. However, both circuits were observed to have performed their required tasks.

Input amplification required notch filtering to remove 60 Hz pickup noise. While this does reduce the speed response of the overall circuit, stellar motion is not expected to be rapid and response above 60 Hz is subsequently not a consideration.

The calibration circuitry was observed to "lock on" to OPS output voltages to within 1/2 bit resolution. For the 12 bit DAC used, this error was measured to be of the order of 2 millivolts maximum. Any offset error incurred in the calibration section will simply shift the "locked on" position of the telescope by a small amount. For this reason, after the system is "locked on", a short amount of time must be allowed for the DC offsets in the system to be accounted for and tracking to become consistent.

4.6.2 Dampened Space Circuit

Because this subcircuit was designed to be completely adjustable, the static output voltage can take on one of many different shapes responses. However, theory and measured responses for a fixed set of component values may be seen in Fig. 4.19.

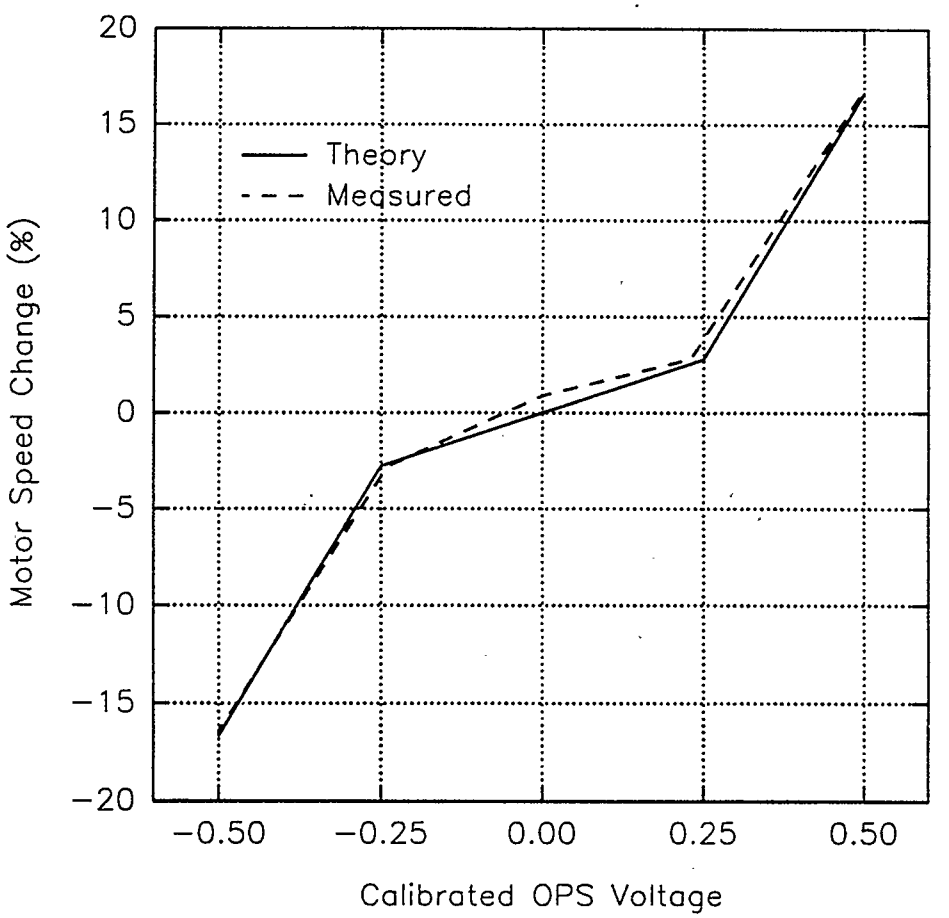

Figure 4.19 - Theoretical and measured static response of the dampened space circuit.

4.6.3 Voltage to Frequency Conversion

Fig. 4.20 shows both the measured and the theoretical voltage to frequency conversion.

The CLK and CLKNOT signals were observed to be square waves and non-overlapping as specified.

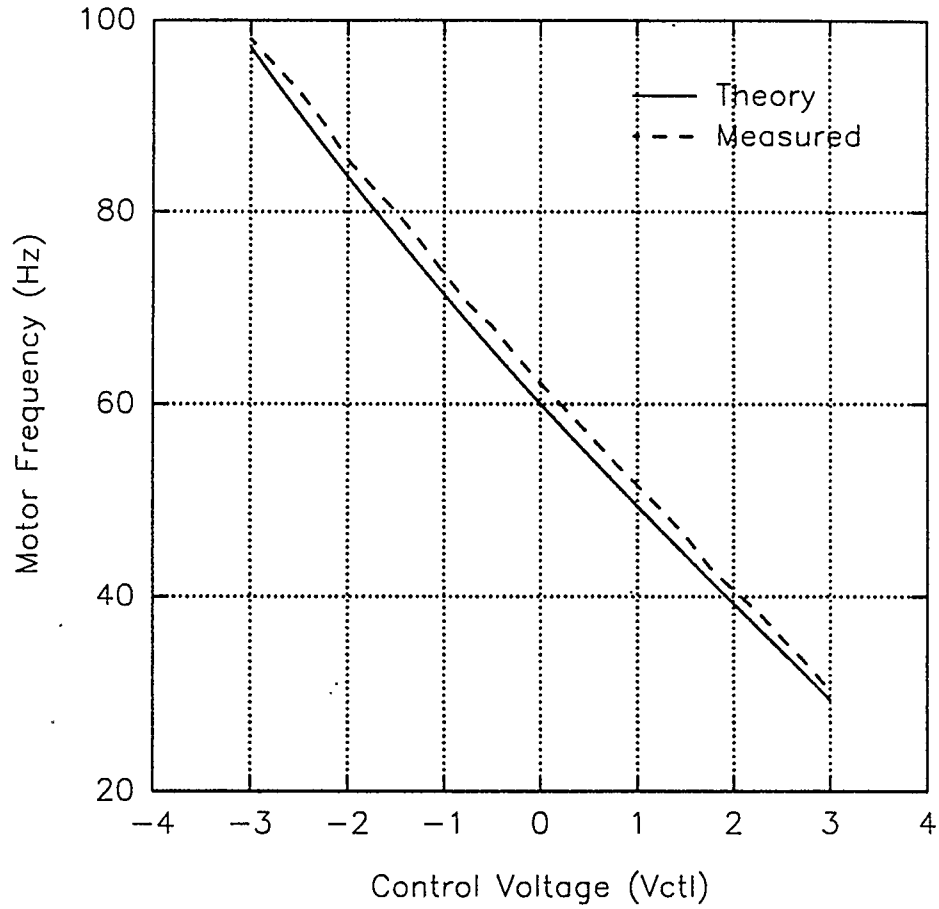

Figure 4.20 - Measured and theoretical voltage to frequency conversion.

4.6.4 Overall Functionality

Again, because of the nature of this circuit, quantitative results are difficult to produce. The entire tracking system has been found to work well under ideal laboratory conditions and high light levels. However, in field testing, noise pickup problems became apparent. The trouble arises from the second order effect of low light levels on OPS output voltage

full scale swing. At the light levels encountered when stellar images or even lunar images are used for tracking, the output swing of the OPS is small enough that the signal is almost entirely lost in RF and 60 Hz pickup noise. This reduction of output voltage swing has been observed in other similar applications of the OPS and has been assumed to be due to photocurrents dropping into the range of the phototransistor dark currents and thus being swamped. While the low pass filtering at the eyepiece of the telescope did improve the situation, noise from either the power supplies (which are suspect) or some other source continued to leak into the tracking signal and tracking became impossible.

4.7 Conclusions and Future Work

While telescope tracking was not possible with the current generation of OPS arrays, the control system retains its validity. The requirement is for OPS arrays which do not suffer from the second order full scale swing problems. Work on just such an OPS has been pioneered by S. Balasubramanian [4] but the devices are not yet available as more research in this direction has yet to be performed.

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Appendices

Appendix A - The CA3280 Linearized OTA

Throughout this thesis, there has been a need for simple, gain controllable multipliers. The Harris CA3280 linearized transconductance amplifier (LOTA) [12] has served well as this crucial building block. However, to fully understand the operation of presented circuits, a full characterization will be presented here [13].

A.1 The Basic Circuit

A simplified schematic of the CA3280 is shown in Fig. A.1, along with external linearization resistors. Two internal linearization diodes are connected across the OTA differential pair as shown in the figure. These diodes are biased into forward conduction via internal current mirrors. Normally, the input resistances R_1 and R_2 are equal (of value R) and sized such that the dynamic impedance of the linearization diodes is negligible. The resulting transfer equation of the circuit is

$$I_{out} = \frac{I_B V_{in}}{2 I_L R} \tag{A.1}$$

where I_L is the diode biasing current, and I_B is the differential pair biasing current. To first order, this equation is seen to be wholly independent of parameters of the LOTA's active devices. However, to obtain the higher order errors inherent in the LOTA, a full derivation of the transfer function is necessary.

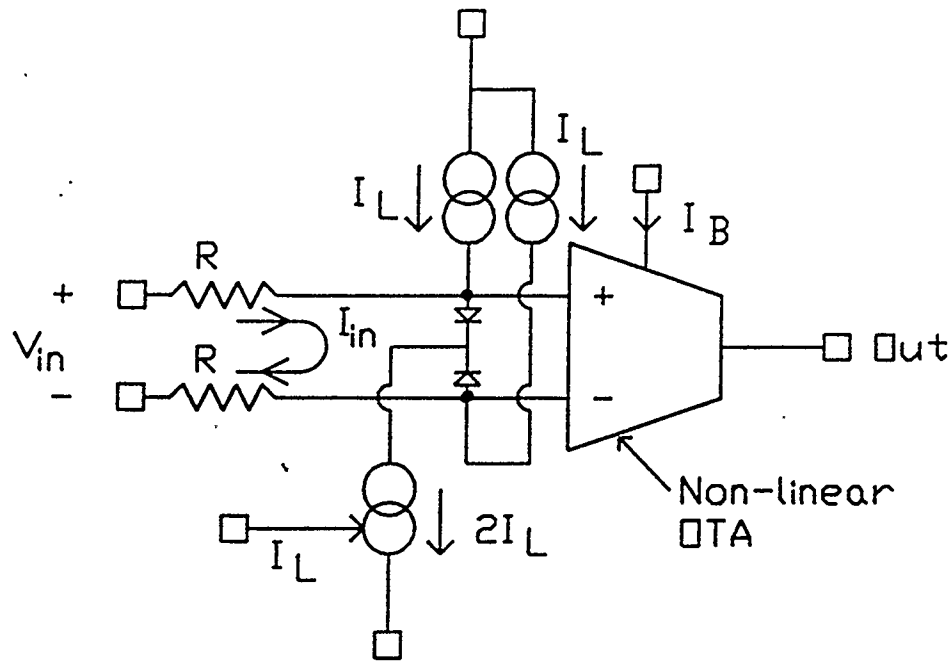

Figure A.1 - A Simplified Linearized OTA

A.2 The linearization Process

When voltage V_{in} is applied to the input nodes of the circuit in Fig. A.1, the voltage appearing across the linearization diodes can readily be shown to be

$$V_{12} = V_{TH} \ln\left(\frac{I_L + I_{in}}{I_L - I_{in}}\right) \tag{A.2}$$

where V_{TH} is the thermal voltage kT/q. The transfer function from the bases of the differential pair to the output has been shown to be [14]

$$I_{out} = I_B \tanh\left(\frac{V_{12}}{2V_{TH}}\right) \tag{A.3}$$

or,

$$I_{out} = I_B\left(\frac{e^{\frac{V_{12}}{2V_{TH}}} - e^{-\frac{V_{12}}{2V_{TH}}}}{e^{\frac{V_{12}}{2V_{TH}}} + e^{-\frac{V_{12}}{2V_{TH}}}}\right) . \tag{A.4}$$

When Eqn. (A.2) is substituted into the above equation, the very simple transfer function characteristic

$$I_{out} = \frac{I_B\, I_{in}}{I_L} \tag{A.5}$$

results, where

$$I_{in} = \frac{V_{in} - V_{12}}{2\,R} . \tag{A.6}$$

For the case when $V_{in} >> V_{12}$, V_{12} can be taken to be zero, Eqn. (A.5) will reduce to Eqn. (A.1) and the device will behave in a near ideal manner. However, V_{12} is often not negligible and must be taken into account. This occurs when either the input resistances are small, resulting in values for I_{in} which approach I_L, or small values of I_L are used. Both these cases arise when a high gain is desired. Fig. A.2 shows the measured values of V_{12} along with a plot of Eqn. (A.2). It can be seen that the

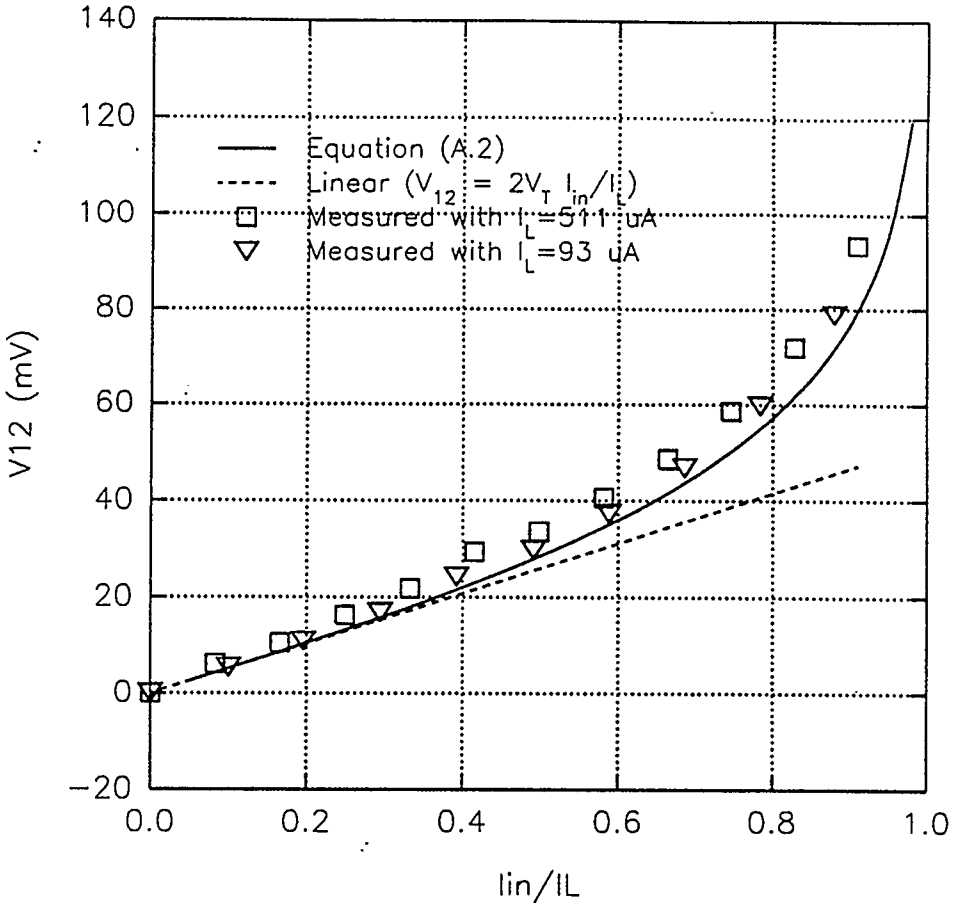

Figure A.2 - Typical Differential Input Voltage

magnitude of V_{12} is large even at relatively small values of I_{in}/I_L and far outstrips the inherent V_{off} of a typical bipolar differential pair due to device mismatches.

A second important source of active device error arose while taking measurements for the above. The current mirrors supplying the linearization diodes are implemented in bipolar technology with the sources for I_L being based on PNP transistors, and the source for $2I_L$ being NPN transistor based. As I_L increases, the gain of the PNP transistors decreases as a result of Webster's effect [15].

This effect arises when minority carriers at the base-emitter junction of a bipolar transistor approach the semiconductor doping levels causing the emitter efficiency to be decreased, and, since the mobility of holes (μ_p) is typically 1/3 of electron mobility (μ_n), the emitter efficiency of PNP type devices is reduced by a greater amount. With transistor gain expressed as

$$\beta_o = \frac{\alpha_o}{1 - \alpha_o} \quad , \tag{A.7}$$

where α_0 is the transistor's emitter efficiency and β_0 is the transistor's forward DC gain, very small changes in emitter efficiency will thus greatly affect transistor gain.

The result is that the current mirrors based on PNP transistors will supply less current to the anodes of the linearization diodes than is being drawn off by the NPN based mirror. The remaining current is drawn in through the two linearization resistors in an approximately balanced fashion. This has the net effect of causing the common mode voltage of the differential pair to move towards the negative supply rail as I_L is increased. These error currents (I_3 and I_4 if Fig. A.4) have been seen to be quite substantial even at small values of I_L.

An empirical fit to measured data was performed with the equation

$$I_{3,4} \approx Constant \cdot 10^{-4} \cdot I_L^2 \tag{A.8}$$

where both I_L and $I_{3,4}$ are in microamps. This equation, along with the measured data can be seen in Fig. A.3. It should be well noted, however, that *Constant* can and does vary greatly from one chip to another.

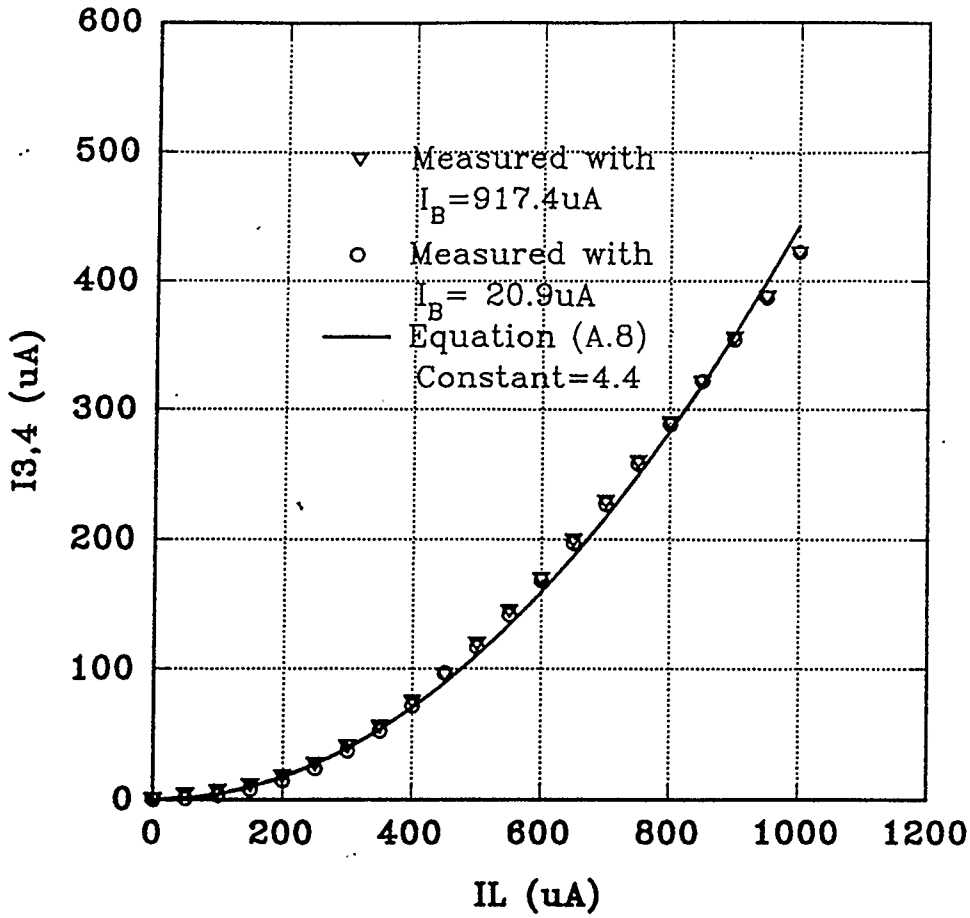

Figure A.3 - Typical DC Input Currents as a Function of I_L

A.3 A Non-Ideal Equivalent Circuit

Fig. A.4 shows a non-ideal equivalent circuit that may be used for complete analysis of circuits containing LOTAs. It incorporates all the standard OTA errors such as differential pair offset voltage, V_{off}, and input bias currents, I_1 and I_2, as well as the LOTA specific errors mentioned above.

$$V_{off} = dc\ offset\ error$$

$$I_1 = I_B^- \ ,\ I_2 = I_B^+ \ ,\ dc\ input\ bias\ currents$$

$$V_{12} = V_T \ln\left(\frac{I_L + I_{in}}{I_L - I_{in}}\right) \approx 2V_T I_{in}/I_L \ ,\ I_{in} < I_L$$

$$I_3 \approx I_4 \approx Constant \times 10^{-4} I_L^2$$

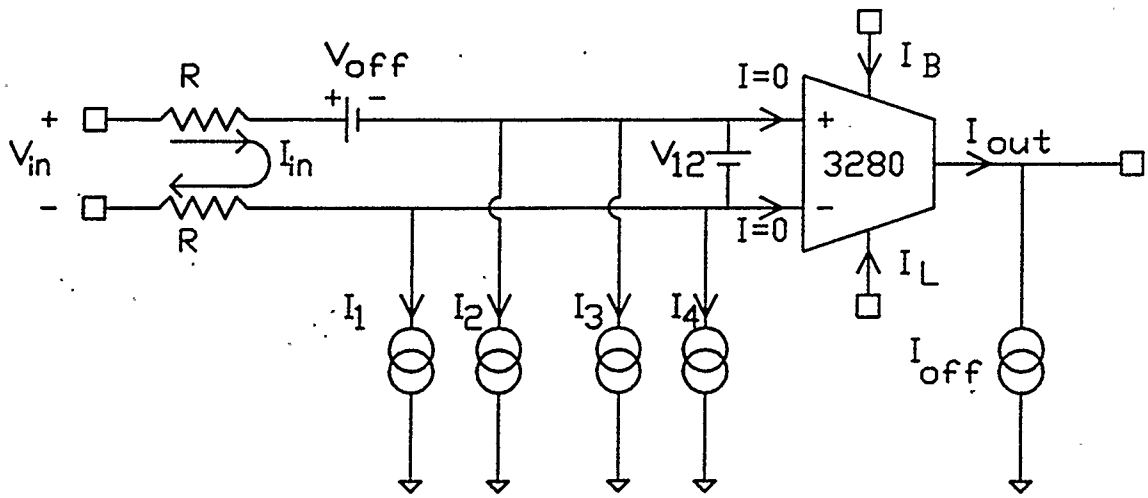

Figure A.4 - A Full Non-ideal LOTA Model Incorporating an Ideal CA3280.

Appendix B - Effects of Overdriven LOTA Multipliers

The importance of designing the OPS differential voltage/current multipliers properly is significant whether or not a linearized OTA is used. The main limiting factor is that the output current may not exceed the input bias current I_B because the internal differential pair simply acts as a current director, nothing more. This means that if an LOTA is used (bipolar), the gain parameter $K(V^+-V^-)$ may not exceed unity in the equation

$$I_{out} = K\ (V^+-V^-)\ I_B \tag{A.1}$$

where

$$K = \frac{1}{I_L\ (R_1+R_2)} \tag{A.2}$$

or if a non-linearized MOS OTA is used,

$$\left|(V^+-V^-)\right| \leq \sqrt{\frac{2\ I_B\ L_D}{\beta\ W_D}} \tag{A.3}$$

where I_B is the differential pair bias current, β and W_D/L_D are the MOS differential pair transistor transconductances (A/V^2) and width to length ratios [14]. The absolute maximum value that (V^+-V^-) can reach (while maintaining proper output operation) is $(V^+_{REF}-V^-_{REF})$ which when bipolar reference voltages are supplied is simply $2V_{REF}$.

If these conditions are not met, then the multipliers will saturate and will simply pass the bias current (or inverted bias current) on to the output and thereby effectively reducing the width of the sensor array (number of sensors) to an amount based on the

light source's standard deviation. Fig. B.1 shows the simulated expected non-clipped LOTA multiplier output and the clipped output along with the input photocurrent. The regions where the clipped current and the input photocurrent coincide are the regions where failure occurs.

Fig. B.2 shows the typical effects that this overdriving has on the OPS output of an LOTA based system. The regions where the output is increasing rapidly are the regions where a multiplier is behaving properly. The plateau regions are where all multipliers are saturated.

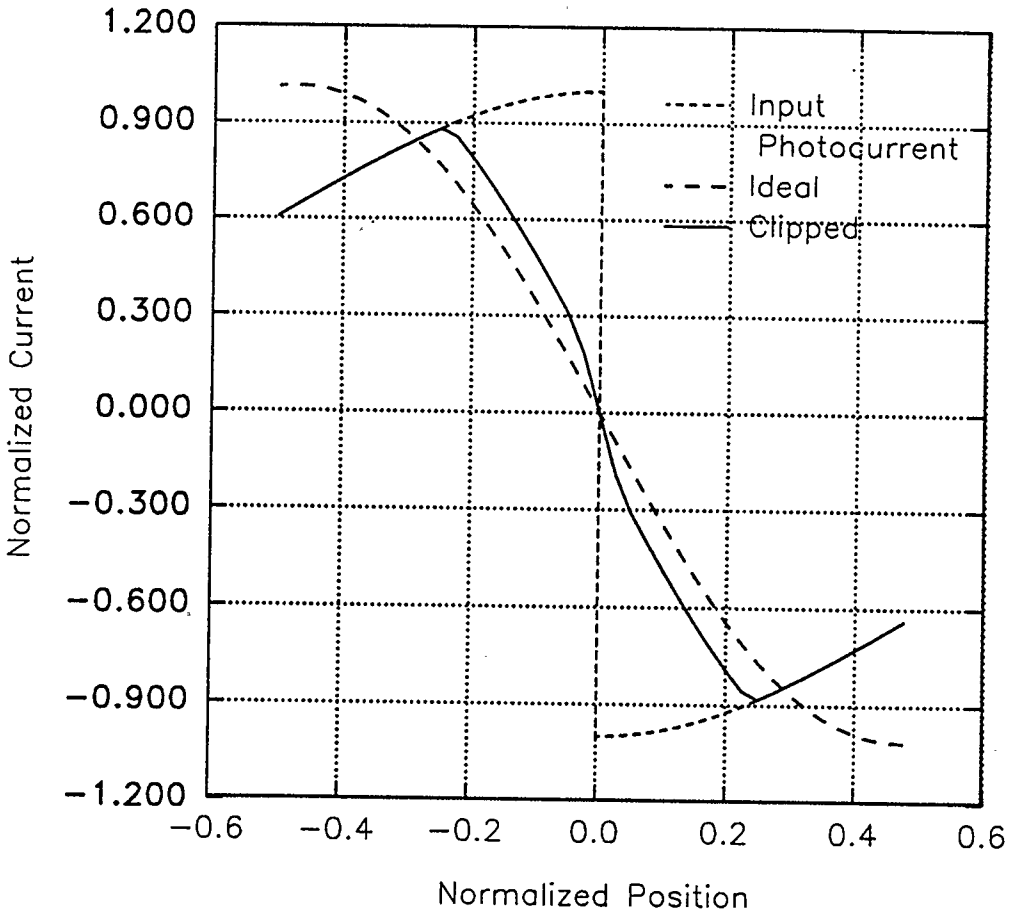

Figure B.1 - Saturating LOTA multiplier expected and actual current output.

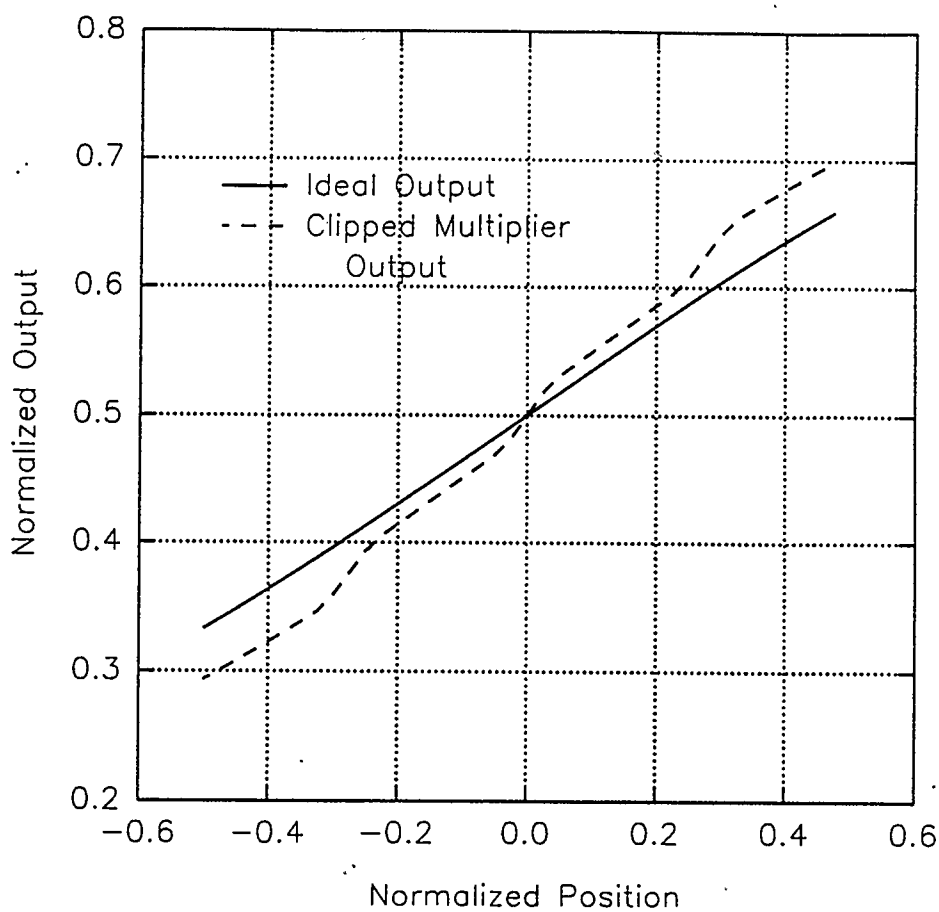

Figure B.2 - Effect of $K(V^{+}-V^{-})=4$ on LOTA based OPS output.