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Modeling and Calibration of Multi-Port Based Receiver Systems Mitigating System Imperfections and Hardware Impairments

Hasan, Abul

UNIVERSITY OF CALGARY

Modeling and Calibration of Multi-Port Based Receiver Systems Mitigating System Imperfections and Hardware Impairments

by

Abul Hasan

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Abstract

Six-port based homodyne receiver architecture is a low power and low cost alternative to the conventional homodyne receiver using diode based mixers. The problems of dc-offset, I/Q cross-talk, high conversion loss and nonlinearities due to diode mixers are some of the issues that make the conventional homodyne receiver architecture not very useful for practical low power communication systems employing envelope varying modulation scheme signals. The radio frequency (RF) front-end in a typical six-port based receiver (SPR) consists of a linear and passive six-port junction circuit that can be easily designed to cover a very large bandwidth. This makes the SPR concept an attractive candidate for software defined radio (SDR) receiver applications. The six-port based RF front-end provides low loss and doesn't pose any nonlinearity issues. Sources of errors due to circuit and system components impairments can be easily calibrated and compensated in a SPR system as shown in this thesis.

Acknowledgements

In the name of Allah, the Most Gracious, the Most Merciful

All praises and thanks be to Allah, the Lord of the worlds, who sent His last messenger (peace and blessings be upon him) who taught the humanity ‘whoever doesn’t thank people, doesn’t thank Allah’.

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In the loving memory of my Grandfather…

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List of Symbols, Abbreviations and Nomenclature

Symbol	Definition
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Controller
BER	Bit Error Rate
BPF	Band Pass Filter
BW	Bandwidth
CW	Continuous Wave
DC	Direct Current
EVM	Error Vector Magnitude
f_c	Carrier Frequency
f_{im}	Image Frequency
GHz	Giga Hertz
DSP	Digital Signal Processor/Processing
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communication
ICT	Information and Communication Technology
IF	Intermediate Frequency
kHz	Kilo Hertz
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LUT	Look-Up-Table
LTCC	Low Temperature Co-fired Ceramic
NCO	Numerically Controlled Oscillator
MHz	Mega Hertz
NMSE	Normalized Mean Square Error
PA	Power Amplifier
PC	Personal Computer
PAPR	Peak-to-Average-Power-Ratio
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RMS/rms	Root Mean Square
Rx	Receiver
SDR	Software Defined Radio
SPR	Six-port Based Direct Conversion Receiver
Tx	Transmitter
UMTS	Universal Mobile Telecommunications System
VNA	Vector Network Analyzer
VSA	Vector Signal Analyzer
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

Chapter One: **Introduction**

Continuous evolution of communication standards in today's information and communication technology (ICT) sphere demands frequent changes in the communication hardware and the supporting software. Also, a single communication device supporting multiple communication standards might require multiple transceiver units to cater for each standard requirement. The global research community is looking for a generic architecture for communication transceiver units, which can accommodate multiple communication standards or changes in the communication standards and protocols without requiring multiple transceiver units or replacing the existing hardware systems. Software defined radio (SDR) architecture promises to fulfill this requirement by virtue of its flexibility and adaptability to the new communication standard and protocol by changing the accompanying software running on its platform [1]. An SDR transceiver system would include both the transmitter and the receiver subsystems, but the focus of the work carried out in this thesis is on the architectures and performances of wireless receivers suitable for SDR applications with special consideration to multi-port based receiver systems. An ideal SDR receiver system will sample the communication signal directly at the receiving antenna [1]. Such a system will require a very broadband (frequency band over which the SDR system is expected to function) antenna and an analog-to-digital converter (ADC) operating at a sampling frequency of at least twice that of the maximum frequency supported by the receiver system. A comparably faster digital signal processor will be required to process the digitized information. The requirement on the sampling speed of the ADC system and thus the signal processor speed can be relaxed by employing another receiver architecture based on subsampling or bandpass sampling technique [2], [3]. The subsampling receiver architecture provides relaxation in the sampling speed at the cost of performance degradation due to inherent

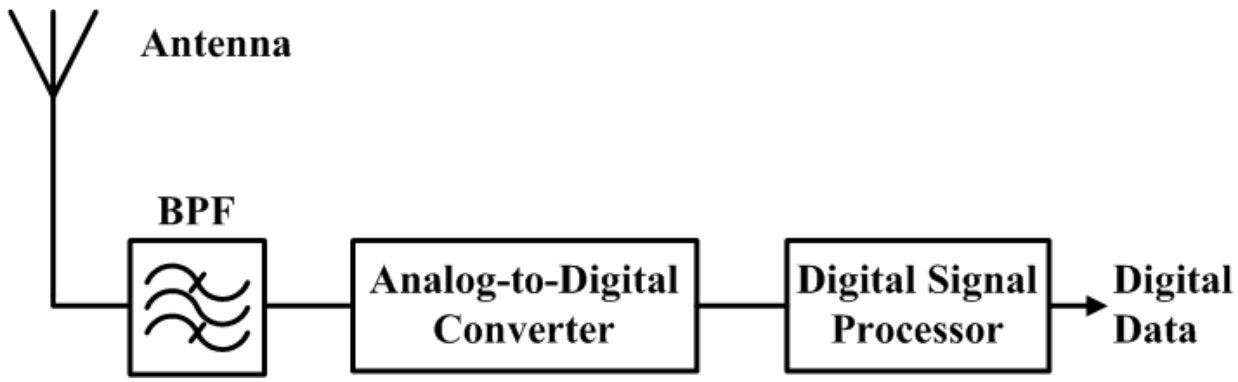


Figure 1.1: Block diagram of an ideal software defined radio receiver system.

issues of sampling jitter and folded noise problem [3]. The block diagram of an ideal SDR receiver system is shown in Figure 1.1. The requirements from the ADC system for a truly SDR system can't be met with the existing state-of-art technology nor are foreseeable in near future [1]. Another interesting option to implement the SDR concept using physically realizable components is to bring down the required information-bearing signal present in a frequency band around a carrier frequency to a lower frequency band where it can be processed more efficiently. This implementation of the SDR system concept necessitates the use of a local oscillator (LO) signal to select a particular band of frequency. The block diagram of this implementation of the SDR receiver concept is shown in Figure 1.2. There are a number of implementations for the frequency down conversion circuitry; the most common of which are a) Super-heterodyne architecture b) Homodyne or Direct down conversion or Zero-IF architecture, and c) Low IF architecture. The details and the pros and cons of these architectures for SDR applications are discussed in Sections 1.2 and 1.3. In most cases, the frequency down-conversion receiver architectures use diode based mixer circuitry to perform the frequency down conversion operation. Traditional diode based mixers require high LO power and are very power inefficient [4], [5].The LO signal must switch the diodes on and off, and drive them deep into the saturation.

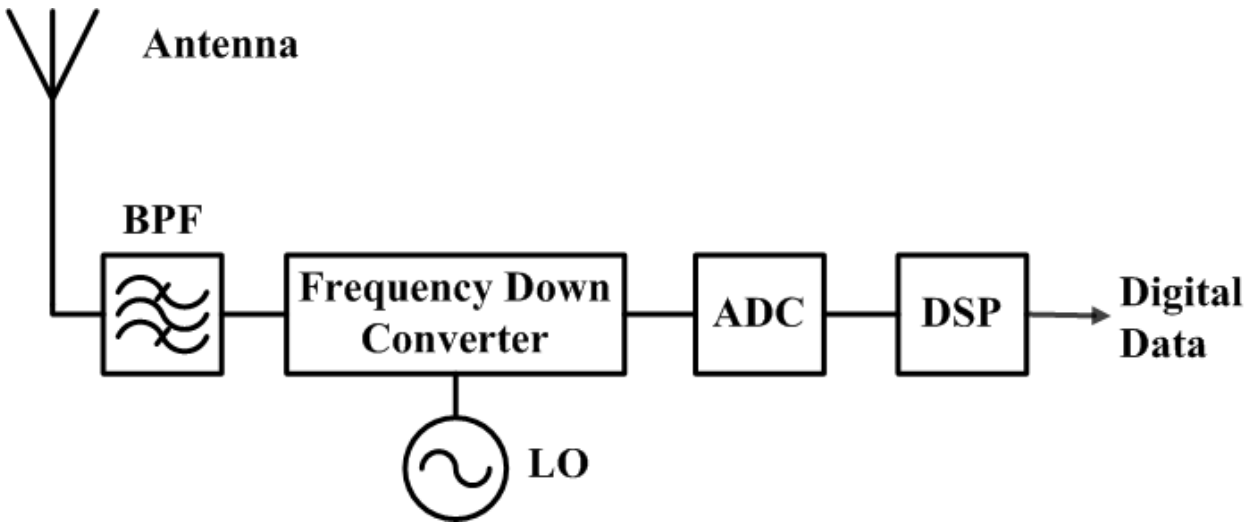


Figure 1.2: A practical implementation of the software defined radio receiver system.

This requires high LO signal power and generates harmonics and distortion at the output port of the mixer. They introduce nonlinearities and thus undesired frequency harmonics in the RF chain of the receiver system [6]. In this thesis, we have explored an alternative for the conventional mixers that is low power and cost effective and it can be designed for a very broad frequency band using passive RF and microwave circuit components. The investigated receiver architecture is known as six-port based direct down conversion receiver (SPR) architecture [7]-[11]. The SPR system consists of a passive, linear, six-port based microwave circuit, the four ports of which are terminated with microwave power detectors. The other two ports are used to supply the received communication signal and the LO signal. The details of a generic SPR system and the principles behind its working are explained in Section 1.4. Before delving into the details of the modern receiver architectures, we will briefly describe the mathematical model for modern communication signals and their representations in the frequency domain for system analysis purposes.

1.1 Signal Representations

Modern communication systems use complex signal representation for the baseband signals. A real world message is digitized and coded in terms of a bit sequence $\{d_i\}$ which is further modulated digitally and mapped to a stream of message symbols with the help of two orthogonal signals, namely, the in-phase component signal and the quadrature component signal. If $s_I(t)$ and $s_Q(t)$ represent the in-phase and the quadrature components, respectively, of a digitally modulated baseband signal, then the complex baseband signal $\widetilde{s(t)}$ is written as

$$\widetilde{s(t)} = s_I(t) + js_Q(t); j = \sqrt{-1} \tag{1.1}$$

The Fourier transforms of the real signals $s_I(t)$ and $s_Q(t)$ will be complex conjugate symmetric in the frequency domain which is not the case for the complex baseband signal $\widetilde{s(t)}$ [12]. The complex baseband signal $\widetilde{s(t)}$ is frequency up-converted to a desired carrier frequency f_c in the transmitter using a complex mixer. The passband or bandpass representation of the communication signal transmitted by the transmitter is denoted as $s(t)$.

$$s(t) = Re\{\widetilde{s(t)}e^{j2\pi f_c t}\} = s_I(t)\cos(2\pi f_c t) - s_Q(t)\sin(2\pi f_c t) \tag{1.2}$$

The model for the complex baseband signals, the complex mixer and the bandpass signal used in this thesis is shown pictorially in Figure 1.3. The fundamental task of a communication receiver is to faithfully recover the complex baseband signal $\widetilde{s(t)} = s_I(t) + js_Q(t)$, that will in turn provide the originally transmitted information bits $\{d_i\}$.

1.2 Modern Receiver Architectures

To prepare ground for the introduction of the six-port based receiver system, we will first discuss about some of the modern receiver architectures being researched and prevalent in most of the today's commercially successful products. We will also discuss their advantages, disadvantages

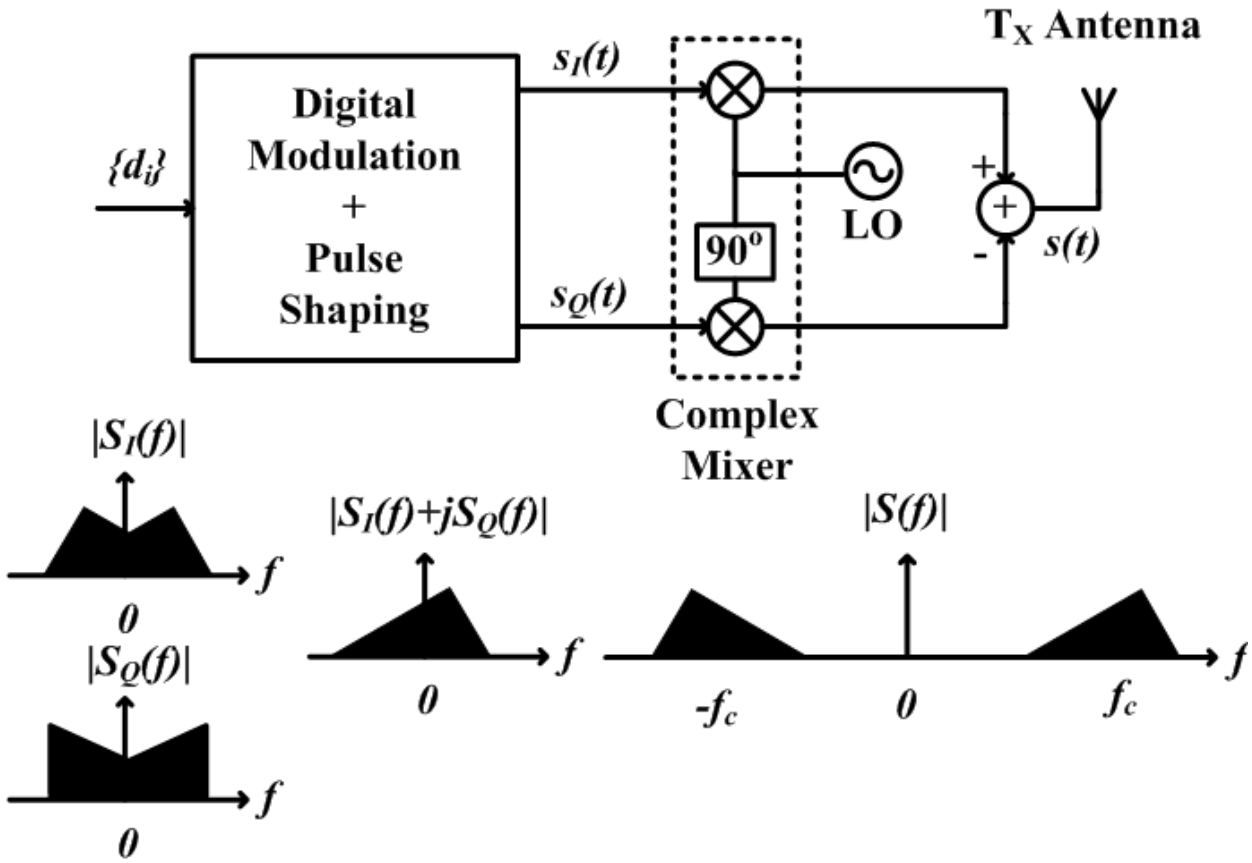


Figure 1.3: Complex signal representation and frequency up-conversion in a typical modern transmitter.

and suitability for the software defined radio (SDR) applications.

1.2.1 Super-heterodyne Receiver Architecture

The overwhelming majority of the contemporary radio receivers employ super-heterodyne architecture, which is also called the heterodyne architecture, [13], [14] to bring down the desired passband signal to the original baseband in two (or more) steps. In the first step of the frequency down conversion process, the desired passband signal is brought down to a fixed intermediate frequency (IF) band. In the last stage of the down conversion process, the IF band signal is brought down to the baseband frequency with the help of a complex mixer for further

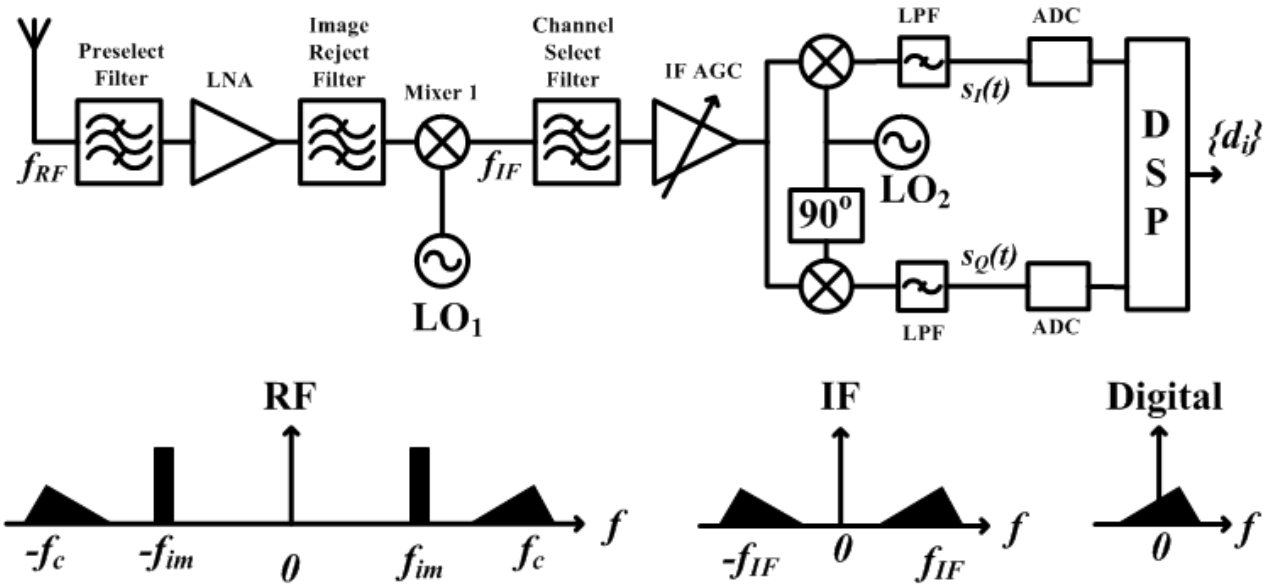


Figure 1.4: Block diagram of a typical super-heterodyne receiver.

processing and data extraction. The block diagram of a typical super-heterodyne receiver is shown in Figure 1.4. The fundamental problem with this architecture is the issue of image frequency. To eliminate this problem a bunch of filters are employed in this architecture that increases the overall size and the cost of the receiver system. The implementation of image reject filters limit the usefulness of this architecture for SDR applications. Modification in this basic super-heterodyne architecture (Weaver architecture, Hartley architecture) [15] is also used to solve the image frequency problem. Another problem with this architecture is the tedious frequency planning and the limitations on the frequency bands for different sections of the receiver in which the system or the subsystem could operate. This architecture is not ideally well suited for SDR applications covering a wide band of frequency in the receiver band supporting multiple communication standards.

1.2.2 Homodyne or Direct Conversion or Zero-IF Receiver Architecture

Homodyne or Direct Conversion or Zero-IF receiver architecture reduces the complexities and limitations of super-heterodyne receiver by eliminating the need of an IF stage [13], [14]. This architecture brings down the passband signal directly to the baseband in a single step. Homodyne architecture greatly simplifies the design of a receiver system. It takes much less space, it is more suitable for integration and the overall system cost is significantly reduced compared to the super-heterodyne architecture. The savings in terms of space and cost comes primarily due to removal of the image reject and other bulky and costly off-chip filter components. In homodyne architecture, the LO frequency is set exactly equal to the carrier frequency of the desired signal band and its phase is locked with the carrier signal phase. Though this architecture appears to be a natural one for frequency down conversion, it comes with some practical problems. The most severe of these problems are; DC offset, I/Q mismatch, self-mixing, LO leakage, $1/f$ noise and the second order distortions. If these problems are resolved, the homodyne architecture will make an ideal candidate for SDR applications. The six-port based direct down conversion receiver architecture solves these issues by using linear circuits and by avoiding the use of conventional diode based mixers. Sources of errors are calibrated and accounted for in the digital signal-processing block of the six-port based receiver system. It has been reported in [13] that the direct conversion architecture has not been used in any commercially successful product where the communication protocol employs a non-constant envelope signal. This is because the inherent errors in the conventional direct conversion receivers are corrected based on the signal profiles using DSP algorithms. The six-port based direct down-conversion architecture, investigated in this thesis, shows the usefulness of direct conversion receivers for non-constant envelops signals too. Block diagram of a typical direct

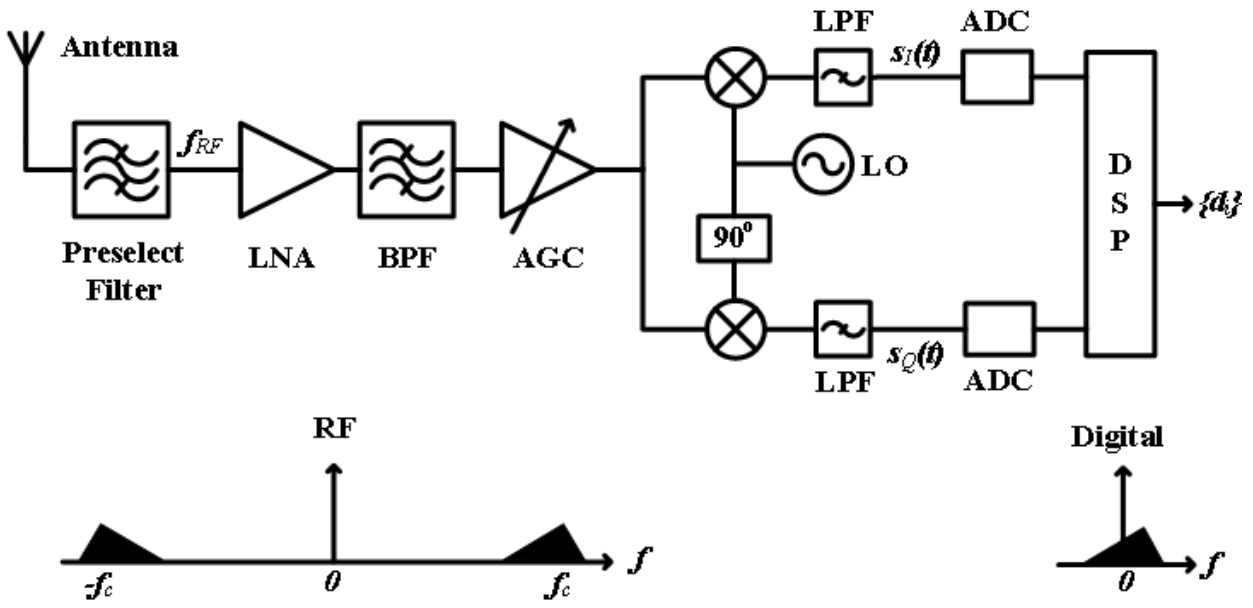


Figure 1.5: Block diagram of a typical direct conversion receiver.

conversion receiver is shown in Figure 1.5.

1.2.3 Low-IF Receiver Architecture

To harness the advantages of both the super-heterodyne and the homodyne architectures a new architecture for the receiver systems is used, which is called the low-IF receiver architecture [13], [14]. This architecture attempts to take advantage of super-heterodyne architecture by eliminating the DC-offset problem of homodyne architecture. In this architecture, the intermediate frequency (IF) is selected at a frequency from half of the signal bandwidth to some small multiple of it. Low-IF architecture brings the image band much closer to the desired band compared to super-heterodyne architecture. This image problem in low-IF architecture is solved using a complex bandpass filter known as polyphase filter, that removes the image frequency signal. The signal at the IF band is digitized and passed to the DSP block of the receiver system. In the DSP block, this digitized signal is brought down to the baseband using a numerically controlled oscillator (NCO) and processed further to extract the original transmitted data. This

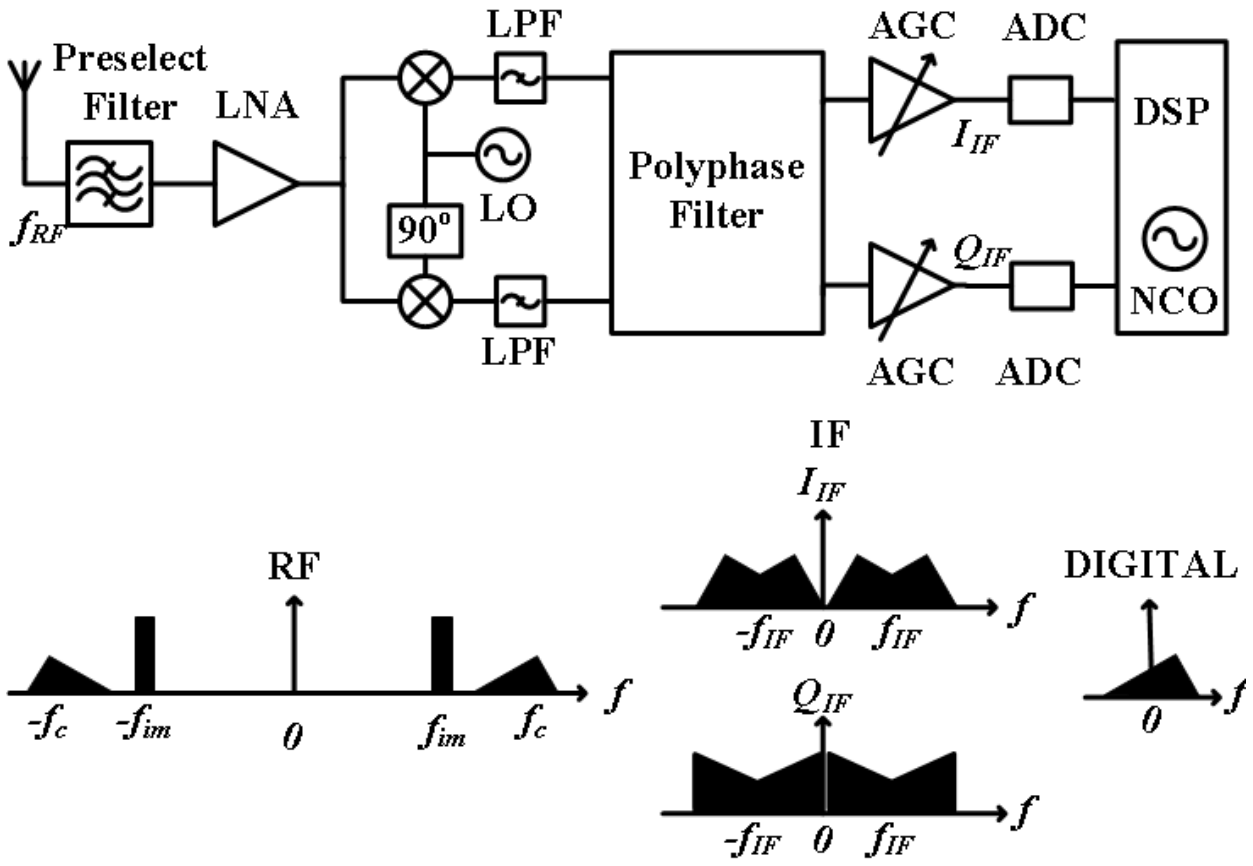


Figure 1.6: Block diagram of a typical low-IF receiver.

architecture can achieve very high image rejection by using efficient signal processing algorithms in the DSP block of the system. Block diagram of a typical low-IF receiver system is shown in Figure 1.6.

1.3 Architecture Comparison and Trade-off

The most robust and superior performance architecture, employed in almost all the modern receiver systems, is the super-heterodyne architecture. This architecture offers superior sensitivity, selectivity, higher dynamic range but suffers from the image frequency problem and requires a tedious frequency planning. Image problem of this architecture necessitates the use of multiple bulky and costly filter components at different stages in the receiver line-up which put

limitations on the frequency bands over which the receiver system could operate. Ideally this architecture will not be suited for SDR applications that demand a very broad coverage in the frequency band.

Direct conversion receiver is well suited for SDR applications but it suffers from major disadvantages such as DC offset problem, self-mixing, LO leakage, $1/f$ noise and nonlinear distortions. Effect of some of the issues in this architecture is minimized if constant envelop modulation scheme signals are used in the communication. The signal statistics and the receiver calibration are used to minimize the error caused by some of these architectural problems. If non-constant envelop signals are employed in the communication, the direct conversion receiver performance deteriorates and is not suitable for major communication applications.

Most of the problems of the direct conversion receiver architecture arise around the zero frequency or DC component of the signal in a narrow bandwidth. This problem is greatly simplified in the low-IF receiver architecture. One disadvantage of low-IF receiver architecture is the requirement of high levels of matching accuracy between components. The suppression of the image must be higher. In some cases, the image signal can be higher than the desired signal. Though the DC offset problem is resolved but image frequency is still a greater problem in this architecture. Selection of the IF is also very important as it plays a crucial role in terms of achievable suppression of the image signal. This architecture is also not quite well suited for SDR applications. If we can solve the existing issues in the direct conversion receiver architecture and make the ancillary circuitry broadband, this architecture is close to the ideal requirements of an SDR receiver system.

1.4 Six-Port Based Receiver System

In the previous section, we have briefly described the existing fundamental receiver architectures for modern communication systems. There are numerous improvements on these basic architectures to enhance the overall system performance, e.g. Weaver and Hartley architectures for improving the image rejection of the super-heterodyne receivers, dual digital quadrature down conversion in the low-IF architecture receivers for higher image rejection. Super-heterodyne and low-IF architectures are not quite well suited for SDR applications as they require tedious frequency planning, put restrictions on the uses of frequency bands, require bulky off-chip high-Q filter components, take more physical space, introduce nonlinear distortions because of the use of nonlinear mixers, consume more power, and are relatively architecturally complex and costly. If we could remove the DC-offset problem, I/Q mismatch and nonlinear distortions in the homodyne receiver architecture, this architecture would prove to be more suitable for SDR applications. I/Q mismatch and nonlinear distortions can be calibrated and accounted for in the homodyne architecture but DC-offset is an issue, which must be precisely resolved especially when the signals involved in the communication have very high peak-to-average power ratio (PAPR).

An alternative direct conversion receiver architecture based on six-port technology has been proposed in [8]-[9]. Six-port technique has been used successfully in a variety of applications such as; in microwave metrology as a reflectometer and as a low cost vector network analyzer (VNA), in other applications such as; device characterization, material characterization, load-pull and source-pull measurements, time domain voltage and current measurement systems, phased array system, antenna measurement systems, and radar systems [11]. In the six-port based architecture of homodyne receiver, the DC-offset, I/Q mismatch and other sources of error can

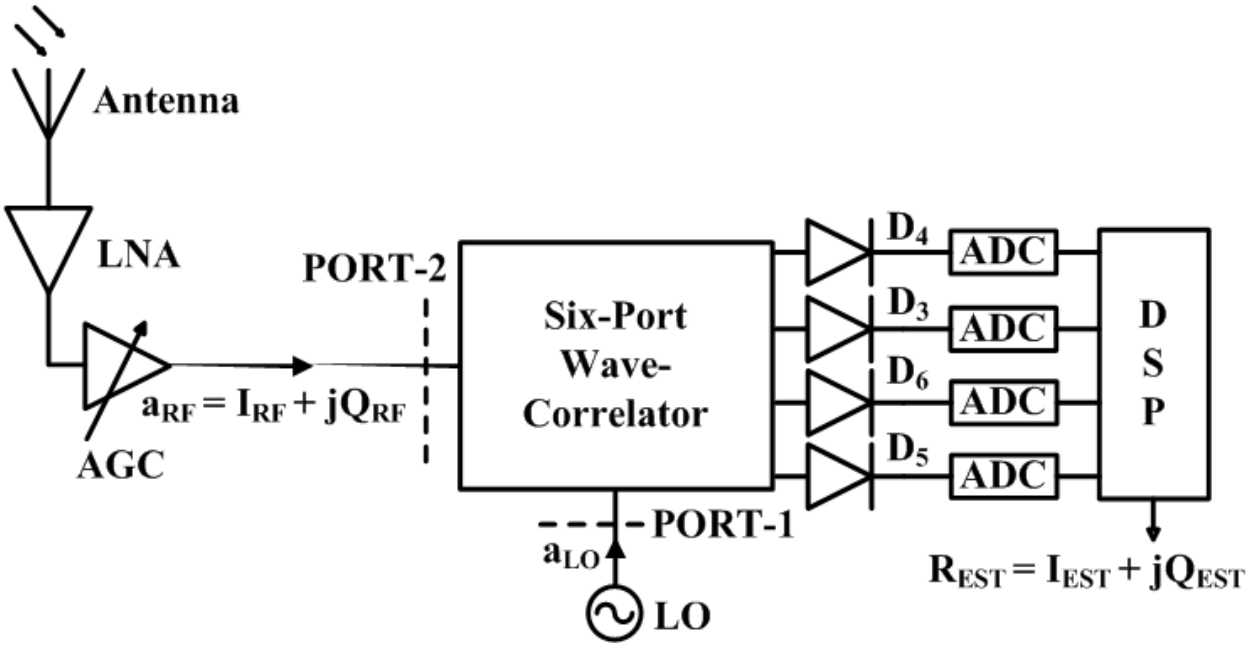


Figure 1.7: Block diagram of a generic six-port based receiver.

be precisely calibrated and accounted for as shown in this thesis. The six-port based homodyne receiver doesn't require nonlinear mixers and hence removes the nonlinearity errors in the RF chain of the receiver system. The block diagram of a typical six-port based receiver system is shown in Figure 1.7. At the core of a six-port based receiver (SPR) system, there resides a passive, linear, six-port circuit, which can be designed to cover a very large bandwidth, which is an ideal requirement for the SDR systems. The six-port junction circuitry is also known as wave-correlator or wave-interferer. The received communication signal from the antenna is fed to one of the ports of the six-port junction. Another port is supplied with a phase stable local oscillator (LO) signal. The remaining four ports of the six-port junction are terminated with microwave power detectors. The output voltages from the four power detectors are sampled and digitized, and sent to a digital signal processor (DSP) for further processing. The DSP block processes the digitized information and finds an estimate of the originally transmitted symbol. The beauty of

the SPR is in its capability to decode a complex (vector) signal ($\boldsymbol{a_{RF}}$) by measuring four scalar signals (output voltages from the four power detectors). The construction of a vector signal from four scalar voltages measurements requires a calibration algorithm running on the DSP platform of the SPR system.

1.4.1 Theory of a Six-Port Based Receiver

In Equation (1.2) the signal represented in the form $\boldsymbol{a_{RF}(t)} = Re\{\widetilde{a_{RF}(t)}e^{j2\pi f_c t}\}$, where $\widetilde{a_{RF}(t)} = I_{RF}(t) + jQ_{RF}(t)$, is a generic representation of a passband or bandpass signal centred at a carrier signal of frequency f_c. Here $\widetilde{a_{RF}(t)} = I_{RF}(t) + jQ_{RF}(t)$ is the phasor representation of the signal $\boldsymbol{a_{RF}(t)}$ in the Cartesian coordinate system. In the polar coordinate system, the same phasor $\widetilde{a_{RF}(t)}$ can be represented as

$$\widetilde{a_{RF}(t)} = r(t)e^{j\varphi(t)};\ \text{where}\ r(t) = \sqrt{\{I_{RF}(t)\}^2 + \{Q_{RF}(t)\}^2},\ \text{and}$$

$$\varphi(t) = \tan^{-1}\{Q_{RF}(t)/I_{RF}(t)\} \tag{1.3}$$

Here $r(t)$ is the magnitude and $\varphi(t)$ is the phase of the phasor $\widetilde{a_{RF}(t)}$. Any bandpass signal can be represented in terms of its phasor if we know the frequency of the carrier signal.

If $\boldsymbol{a_{RF}} = I_{RF} + jQ_{RF} = A_{RF}e^{j\varphi_{RF}}$; $A_{RF} = \sqrt{I_{RF}^2 + Q_{RF}^2}, \varphi(t) = \tan^{-1}(Q_{RF}/I_{RF})$, is the phasor representation of the original bandpass transmitted signal then the real transmitted passband signal at the receiver antenna path reference plane (PORT-2) can be written as

$$s_{RF} = Re\{\boldsymbol{a_{RF}}e^{j2\pi f_c t}\} = I_{RF}\cos(2\pi f_c t) - Q_{RF}\sin(2\pi f_c t) \tag{1.4}$$

Similarly the phasor for local oscillator (LO) signal at a reference plane in LO port (PORT-1) can be written as $\boldsymbol{a_{LO}} = A_{LO}e^{j\varphi_{LO}}$, where A_{LO} and φ_{LO} are the magnitude and the phase of the LO signal phasor, respectively. An important point to be noted here is that the magnitude and the phase of the RF signal phasor are time dependent and varying while those of the LO signal

phasor are constant and fixed. The phase noise in the LO signal will cause error in the phase of the LO signal phasor.

If $S_{ij}; i, j = 1,2, \dots ,6$ are the S-parameters of the six-port junction, then the phasors of the signals at PORT – 3, 4, …, 6 can be written as

$$\boldsymbol{a}_k = S_{k2}\boldsymbol{a}_{\boldsymbol{RF}} + S_{k1}\boldsymbol{a}_{\boldsymbol{LO}}; k = 3,4, \dots ,6 \tag{1.5}$$

The signal powers reaching to the four power detectors can be written as in equation (1.6).

$$P_k = |S_{k2}\boldsymbol{a}_{\boldsymbol{RF}} + S_{k1}\boldsymbol{a}_{\boldsymbol{LO}}|^2; k = 3,4, \dots ,6 \tag{1.6}$$

Here P_k is the power detected by the kth power detector. Equation (1.6) can be simplified further and solved for $\boldsymbol{a}_{\boldsymbol{RF}}$ in primarily two different ways, resulting in two different modeling and calibration approaches; namely the linear and the nonlinear modeling and calibration approaches for the six-port based receiver systems. Each way of modeling and calibration comprises of certain model parameters which must be determined before making an estimate of the received signal $\boldsymbol{a}_{\boldsymbol{RF}}$. In chapter three of this thesis the nonlinear modeling and calibration approach for an SPR system is described in detail. The linear modeling and calibration approach for the SPR system is dealt with in detail in chapter four.

1.5 Limitations of the Six-Port Based Receiver Systems

The core of a six-port based receiver system consists of a passive six-port junction and four power detectors. In most cases, the six-port junction circuit comprises of the quadrature hybrids and power dividers. The performance of these microwave components are best guaranteed at the design frequency but it deviates from the ideal performance when the frequency of operation is changed. The deviation in the performance of a six-port junction from its ideal behavior results in degraded performance of the whole receiver system. The diode based power detectors are used most frequently in the SPR systems because of their low power requirements and smaller sizes.

These power detectors generate voltages in response to the microwave power at their input ports. The input power range, in which the voltage generated by a power detector is proportional to its input power, is called the linear range of the power detector. The diode based power detectors are notorious for their limited linear dynamic range. When these detectors are used in a SPR system, they limit the dynamic range of the whole receiver system. The diode detectors characteristics are linearized to open up this limitation on the dynamic range. Another problem with the diode detectors is their different dynamic behaviour as compared to static behaviour. The input power-output voltage characteristic of a diode power detector is dependent on the frequency of the input excitation signal. All these issues in a typical SPR system results in heavily degraded receiver performance when real wideband modulated signals are used in the communication. An accurate modeling of the six-port junction and linearization of the power detectors is required to solve the limitations/problems of the SPR system including the dynamic range limitations of the power detectors and the trade-off between dynamic range and linearity of the power detectors for good quality reception.

1.6 Building Blocks of an SPR System

The basic components required for integrating an SPR system for SDR applications are:

1) Wideband Antenna
2) Broadband Low noise amplifier (LNA)
3) Broadband Automatic gain controller (AGC)
4) Broadband Six-port junction
5) High dynamic range wideband diode power detectors
6) Analog-to-digital converters (ADC)
7) Digital signal processor (DSP)

The antenna, LNA, AGC, and the six-port junction circuitry should be broadband that cover the whole frequency band over which the SDR system is expected to operate. ADCs should be fast enough to sample a signal having the highest possible frequency bandwidth expected from the SDR system. DSP should be operating at a speed fast enough to process the sampled data and run the SPR calibration algorithm. Diode power detectors should have high dynamic range to cover the dynamic range requirement of the SDR receiver system. Detectors should be broadband and also fast enough to accommodate the detection of signal with the highest possible bandwidth.

1.7 Thesis Outline

The outline of this thesis is as follows. The first chapter of this thesis discusses the usefulness and limitations of the modern receiver architectures for software defined radio (SDR) applications. A linear homodyne receiver architecture based on the six-port technique is introduced in this chapter and its suitability for SDR applications is discussed in detail. This chapter also highlights the limitations of the existing six-port based receiver (SPR) systems and the contributions of this thesis. Characteristics of the diode power detectors used in a typical SPR system are studied in chapter two. A survey of existing detector linearization is provided in this chapter and a new linearization technique, suitable for linear calibration of the SPR systems, is proposed. The nonlinear and the linear modeling and calibration techniques for the SPR systems are discussed in detail in chapter three and chapter four, respectively. Chapter five concludes the thesis and gives pointers to the future research works.

1.8 Thesis Contributions

The fundamental contributions of the works, carried out for this thesis, to the RF and the microwave community can be summarized in the following three points:

1) A nonlinear calibration approach based on the use of training sequence inserted at the beginning of an actual test data burst is proposed in chapter three of this thesis. The proposed nonlinear calibration approach avoids the frequent connection/disconnection of the standard loads at the RF port of the six-port junction as was the practice in six-port based microwave metrology applications. The proposed calibration algorithm is useful for six-port based receiver applications where removal of the antenna for connection/disconnection of the standard loads for calibration purpose is not feasible and practical.
2) After a survey of the existing linearization techniques for the diode power detectors, it was found out that the existing linearization techniques for the diode detectors are based on a continuous wave (CW) measurement that ignores the dynamic effects of the time varying real communication signals. A new diode power detector linearization technique suitable for wideband signals having high peak-to-average power ratios (PAPR) is proposed in chapter two of this thesis. The new proposed detector linearizer takes into account the nonlinearity and the memory effect displayed by the real diode power detectors.
3) In chapter four of this thesis, an integrated calibration approach for the whole SPR system is proposed, that combines the existing two steps process of diode detector linearization and six-port junction calibration. The proposed SPR system calibration approach is a single step approach that takes into account all the identified system imperfections in a real SPR system, such as; the non-flat frequency responses (S-parameters magnitude response) of six-port junction and components, deviation of phase responses from the ideal behaviour (S-parameters phase response), and nonlinearity and

memory effect displayed by the diode power detectors. All these identified system and component imperfections become part of the SPR model developed in chapter four of this thesis and are taken care of during the proposed calibration procedure.

The work carried out for this thesis resulted in the following peer-reviewed publications:

1. A. Hasan and M. Helaoui, "Non-Linear Auto-Calibration Method for Six-Port Based Direct Conversion Receivers," *IET Microwaves, Antennas and Propagation* (under preparation).
2. A. Hasan and M. Helaoui, "Novel Modeling and Calibration Approach for Multi-Port Receivers Mitigating System Imperfections and Hardware Impairments," *IEEE Transaction on Microwave Theory and Techniques,* vol. 60, no. 8, pp. 2644-2653, Aug. 2012.
3. A. Hasan, M. Helaoui and F. M. Ghannouchi, "Dynamic Linearization of Diodes for High Speed and Peak Power Detection Applications," in *2012 IEEE MTT-S International Microwave Symposium Digest (IMS'2012),* Montreal, QUE, Canada, pp. 1-3, Jun. 2012.

1.9 Conclusions

The importance of multi (six)-port based receiver architecture for software defined radio (SDR) applications is highlighted in this chapter. Architectural comparison of the six-port based receiver system with the modern receiver architectures is provided to illustrate the advantages and drawbacks of different receiver architectures. The six-port based receiver architecture is a homodyne type receiver architecture which has some practical problems, such as; DC-offset, I/Q mismatch, I/Q cross-talk, and nonlinear distortions. Because of these inherent problems in the homodyne receivers, this architecture has not been used successfully in any commercial products using non-constant envelope modulation scheme signals. For constant envelope modulation scheme signals, the signal statistics are used to minimize the effect of some of the problems of this architecture. These sources of errors can be precisely modeled and calibrated in a six-port

based receiver system as proposed in this thesis. The proposed model and the calibration approach for six-port based homodyne receiver shows its usefulness for the non-constant envelope modulation scheme signals too. The outline and the contributions of the thesis are highlighted in this chapter.

Chapter Two: **Diode Detector Modeling and Linearization**

Historically bolometer, thermistor, diode, and transistor based power detectors have been used in a variety of microwave power measurement applications, such as: multi-port based measurement systems, radar applications, and power measurement and control applications in modern cellular communication systems. Diode based power detectors are widely used nowadays because of their low power and simplified support circuitry requirement. The dynamic range of the diode power detectors, where the output voltage from the detector is proportional to the input microwave power, is quite limited [11]. This limits the useful range of operations of the diode power detectors for many applications. For example, when the diode power detectors are used in a six-port based receiver system, the dynamic ranges of the diode power detectors limit the dynamic range of the whole receiver system. To extend this dynamic range, the power detector can be operated close to its saturation region, where it exhibits nonlinear characteristic. Linearization of the diode power detectors characteristics is performed to open up this limitation and to extend their dynamic range without affecting the received signal quality. The output voltage of the diode power detector is used to predict its characteristic and compensate for its nonlinear behaviour. The concept of linearization for the diode power detectors is shown in Figure 2.1. The detector output voltage is input to the linearizer block that outputs the linearized power. Ideally, the linearized power should be equal to the actual input microwave power to the diode power detector. To linearize the characteristics and extend the dynamic ranges of the real diode power detectors, a number of linearization techniques have been proposed in open literature [16]-[19]. All the existing linearization techniques for the diode power detectors use a continuous wave (CW) excitation signal for detector modeling and characterization. In this chapter we show that the characteristic of a diode based power detector is not static. It is dependent

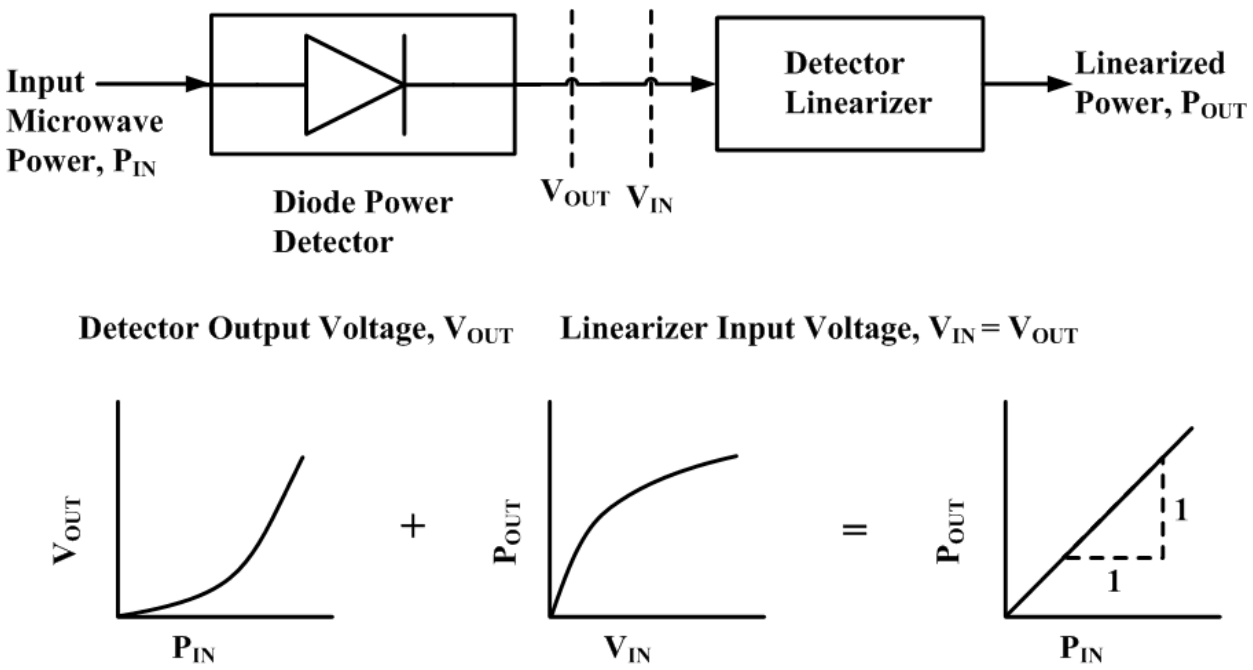


Figure 2.1: Block diagram of a diode based power detector cascaded with its linearizer.

on the type of input excitation signal. This power-voltage characteristic of a diode detector deviates from its usual CW characteristic, when real wideband modulated signals are used to characterize and linearize the diode power detector.

2.1 CW Linearization Techniques

Four different techniques found in open literature to linearize the diode power detectors characteristics are briefly described in the following subsections.

2.1.1 Look-up-table (LUT) Based Linearization Technique [16]

This technique is a crude and direct measurement based method to linearize the diode detector characteristic. In this technique a look-up-table consisting of detector output voltage against the input microwave power at the carrier frequency is constructed and stored. A simple interpolation (e.g. `interp1` function of MATLAB) is applied on the detector output voltage V_{OUT} to linearize the detector characteristic and to obtain the linearized power P_{OUT}.

2.1.2 'Hoer-Roe-Allred (HRA)' Model [17]

In this model the relationship governing the linearized power and the detector output voltage is given by equation (2.1).

$$P_{OUT} = Kv^{(1+b_1v+b_2v^2+b_3v^3+\cdots+b_Nv^N)} \tag{2.1}$$

Here $v = q(V_{IN} - V_O)$, where V_O is the diode power detector output voltage when $P_{IN} = 0$, and q is a scale factor. The linearizer parameters K, q, and b_i are obtained during the detector characterization step. These parameters are stored in the linearizer block and are used to linearize the detector characteristic according to equation (2.1).

2.1.3 'Zhaowu-Binchun (ZB)' Model [18]

When the output voltage is reduced to zero for zero-bias Schottky diodes, the deviation from the square law according to the model in equation (2.1) tends to infinity. To solve this problem, a new model to linearize the Schottky diode detectors was proposed in [18]. The linearized power according to this model is given by equation (2.2).

$$P_{OUT} = KV_{IN} \times 10^{(a_1x+a_2x^2+a_3x^3+\cdots+a_Nx^N)} \tag{2.2}$$

Here x is a function of V_{IN}, defined as $x = \ln(V_{IN}/q + 1)$; where q is a scalar factor chosen so that x is positive and has a maximum value of 0.5.

2.1.4 'Polynomial (P)' Model [19]

The linearizer characteristic in this model is approximated by a polynomial of the form given in equation (2.3).

$$P_{OUT} = c_0 + c_1V_{IN} + c_2V_{IN}^2 + c_3V_{IN}^3 + \cdots + c_NV_{IN}^N \tag{2.3}$$

All the four models described here are static and do not consider any dynamic behaviour of the diode power detectors or in other words the frequency response or the memory effect of the diode power detectors. When the input excitation signal has a wide bandwidth, the frequency

response and hence the memory effect of the diode power detectors comes into picture. Any linearization technique which ignores this effect will cause error in the linearized output power. The three latter models (HRA, ZB, and P models) fit the model equations' parameters to the measured data and therefore may include fitting residual errors. The look-up-table is therefore more accurate and will be used in the following analyses.

2.2 Diode Detectors for Peak Power Detection Applications

In power control applications, the diode power detectors are used in a variety of applications such as; peak power detection, root-mean-square (rms) power detection, and envelope detection. In power control applications of the cellular mobile communication, diode based power detectors are used for measuring the transmitted power levels. Peak power detector is a good choice for RF power detection application for the communication standards employing constant envelope modulation scheme such as the GMSK (Gaussian Minimum Shift Keying) for GSM. However, for communication systems with high crest factors or PAPR like UMTS, the rms power detection is used. The use of diode power detector in cellular handsets power control application is shown in Figure 2.2.

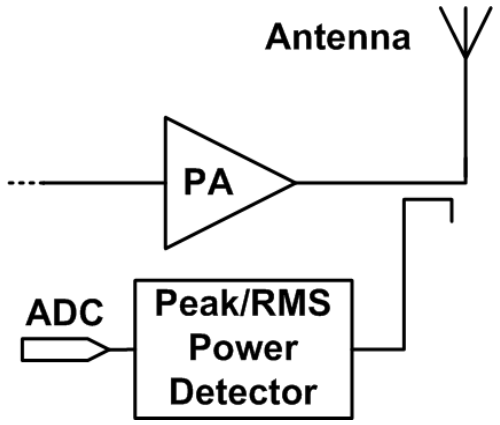


Figure 2.2: Diode based peak/rms power detector in cellular handset power control application.

In six-port based receiver applications, the diode power detectors are used as envelop power detectors. Linearization of diode power detectors for envelop power detection application will be discussed in Section 2.3. Here we describe a linearization technique for diode power detectors for peak power detection applications. When the usual CW linearization techniques are used for peak power detection applications, the linearized peak powers result in error as compared to the actual input peak powers. This deviation is much pronounced when the input excitation signal has a very high value of peak-to-average-power-ratio (PAPR). A test bench is setup to measure the peak power detector characteristic for different excitation signals. A linearizer based on CW measurement and characterization data is designed to linearize the diode based peak power detector characteristic as explained in Section 2.1.

2.2.1 Measurement Test Setup

The test setup to characterize and linearize a diode based peak power detector is shown in Figure 2.3. The baseband quadrature amplitude modulation (QAM) modulated symbols are generated on a desktop PC in MATLAB. The baseband symbols are passed through a raised-cosine filter with a roll-off factor 0.3 (up-sampled by 8) and a delay of 3 taps. These pulse shaped symbols are further passed to an I/Q modulation generator (AMIQ from Rhode & Schwarz GmbH & Co.) to generate an I/Q modulated signal. This pulse shaped and I/Q modulated signal is frequency up-converted to a desired carrier frequency (2.5GHz) using a SMIQ03B vector signal generator from Rhode & Schwarz. The power level for the input excitation is set in the SMIQ and this passband signal is then fed to the diode power detector (8472B from Agilent Technologies, Inc.). Voltage generated by the Schottky detector in response to a particular excitation signal is captured using a synchronized dual-channel VSA (89600 series VSA from Agilent Technologies). The captured voltage waveform is used to linearize the diode detector

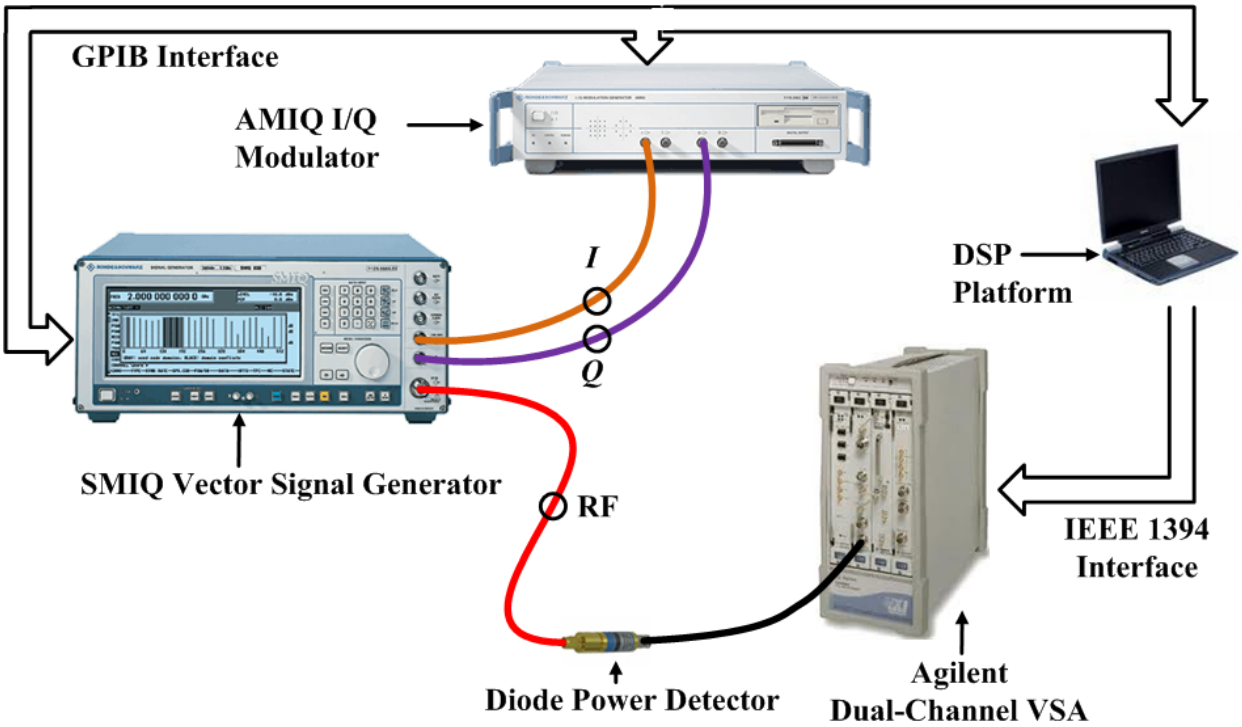


Figure 2.3: Test setup for the peak power detector characterization and linearization.

characteristic as discussed in the next subsection.

2.2.2 Measurement Results

The actual input peak power and the corresponding output peak voltage characteristics for the diode power detector in response to different excitation signals are shown in Figure 2.4. From the plots in Figure 2.4, it is obvious that the peak power detector behaves differently for different input excitation signals. The deviation from the CW response is much more pronounced as the PAPR of the excitation signal increases. Peak power detector characteristic for the Wideband Code Division Multiple Access (WCDMA) signal having the highest PAPR value (≈ 9.5dB) has the highest deviation from the CW characteristic. Deviation of the peak power detector characteristics for QAM modulated signals (PAPR ≈ 6.8dB) is intermediate of the WCDMA (PAPR ≈ 9.5dB) waveform excitation and the Wireless Local Area Network (WLAN) excitation

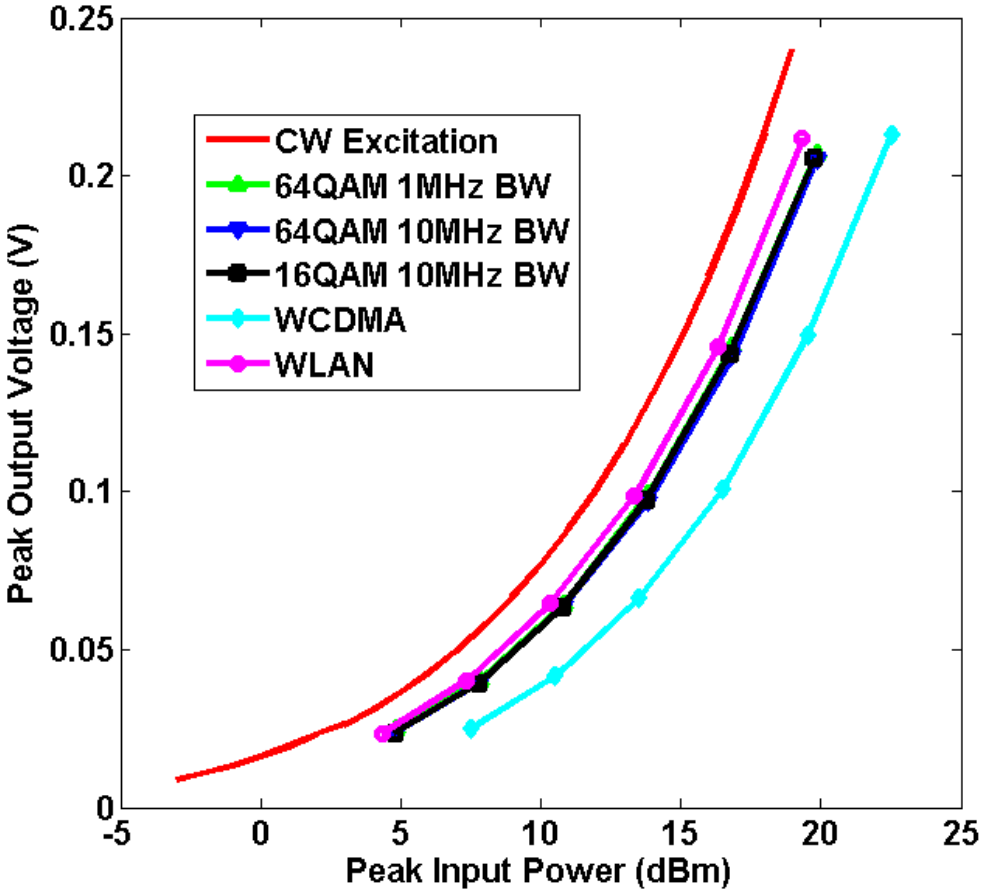


Figure 2.4: Peak power detector characteristics for different excitation waveforms at a carrier frequency of 2.5GHz.

(PAPR ≈ 6.3dB) as shown in Figure 2.4. The carrier frequency for all the excitation waveforms is kept same at 2.5GHz.

In order to show the error in the CW linearized output peak power for the peak power detector, we pass the output voltage waveforms from the diode detector to a CW linearizer. The linearized peak power for different test excitation signals is plotted against the actual input peak power of the excitation signal in Figure 2.5.

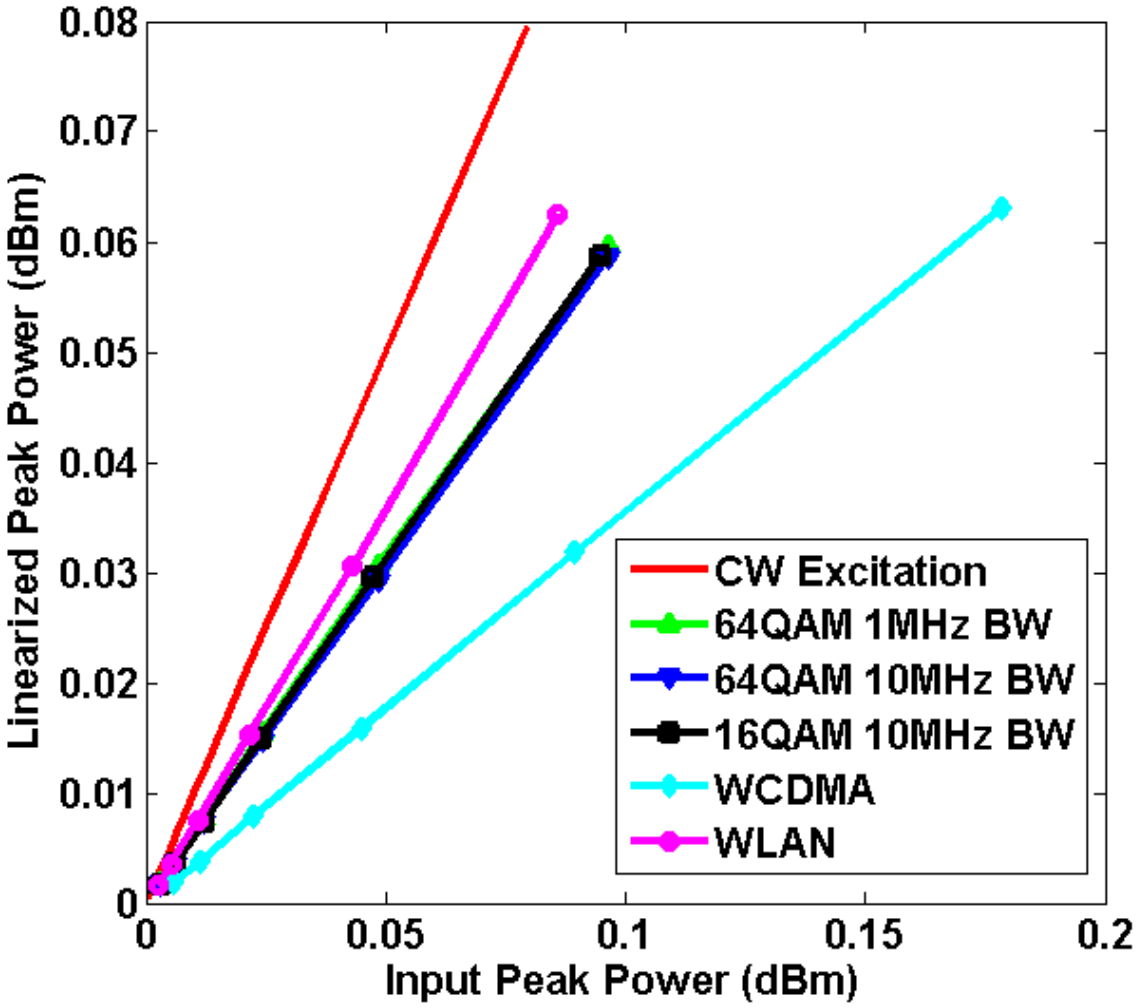


Figure 2.5: Linearized peak power versus the actual input peak powers for different types of excitation signals.

The ideal slope for such plots should be equal to unity, if the linearizer block is linearizing perfectly as expected from the theoretical analysis. In practice, the linearizer providing the slope closest to the unity offers the best performance. According to the plots as shown in Figure 2.5, we observe that the signal having the highest PAPR (WCDMA) deviates the maximum from the unity slope of the linearized peak power versus the actual input peak power line plot. The slope of the CW excitation when linearized with the CW characterization data is unity. Slopes for all

other excitation signals are constant for each of the signals but are other than unity. Based on these observations, it is concluded that the behaviour of the power detector changes depending on the type of excitation. Therefore, dynamic characterization and linearization are required for accurate peak power detection. Two different linearization techniques are proposed in [20] to linearize the diode peak power detector characteristic for excitation signals other than the CW.

1) The diode based peak power detector must be linearized for the specific excitation signal type using the similar approach as is done in case of a CW excitation signal. The peak input powers and peak output voltages are recorded for a particular excitation signal and a linearizer of the form discussed in Section 2.1 is obtained. All the future linearization for the peak power detector will be done according to these stored linearizer parameters using the output voltage from the peak power detector for the specific excitation signal.

2) We observed from the plots in Figure 2.5, that, even though the slope of the CW linearized peak power versus the actual input peak power plot is not unity, it is constant for a specific excitation type. This slope for a specific excitation signal type can be stored along with the CW linearizer parameters. The detector output voltage will be passed to a CW linearizer and the corresponding output peak linearized power will be multiplied further by a constant factor accounting for the difference between the CW slope and the slope for that specific excitation. This second linearization technique for peak power detector is more efficient in terms of memory as it requires only one parameter corresponding to the excitation signal type apart from the fixed CW linearization parameters (usually 6). For the approach described in 1), individual linearization parameters (usually 6 for each) are stored for each excitation signal type. Figure 2.6 shows the block diagram of the proposed peak power linearizer 2) using the signal specific calibration constant.

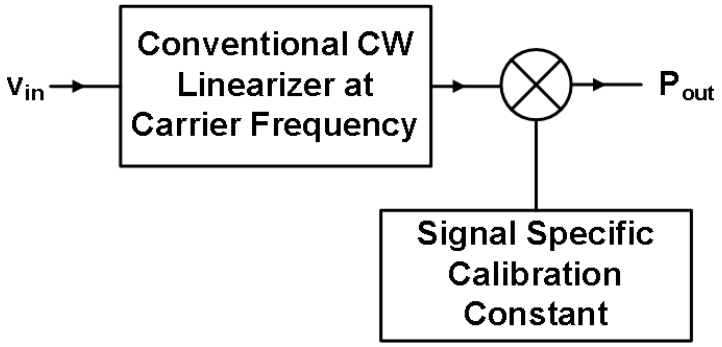


Figure 2.6: Proposed peak power linearizer using calibration constant.

Table 2.1 summarizes the actual linearization errors in terms of normalized mean square error (NMSE), as defined in equation (2.5), when a CW linearizer and the proposed linearizer 2) is used to linearize the peak power detector for different excitation signals.

Table 2.1: Comparison of CW and proposed peak power detector linearizer

Excitation Waveform	PAPR (dB)	NMSE (dB)	
		CW Linearizer	Proposed Linearizer 2
WLAN	6.3	-7.98	-32.94
64QAM 1MHz BW	6.8	-5.29	-35.61
64QAM 10MHz BW	6.8	-5.29	-44.29
16QAM 10MHz BW	6.8	-5.30	-41.61
WCDMA	9.5	-0.65	-41.95

2.3 Diode Detector Linearizer for Wideband Signals

In the previous section we showed that the characteristic of the diode power detector was dependent on the input excitation signal type. The diode power detectors used in multi-port based receiver systems are expected to accurately detect the instantaneous envelope power of the continuous time microwave signals at the input port of the detector. Errors in the linearized

detected powers for the power detectors have a direct bearing on the performance of the multi-port based receiver system. Figure 2.7 shows the input power waveform and the linearized power

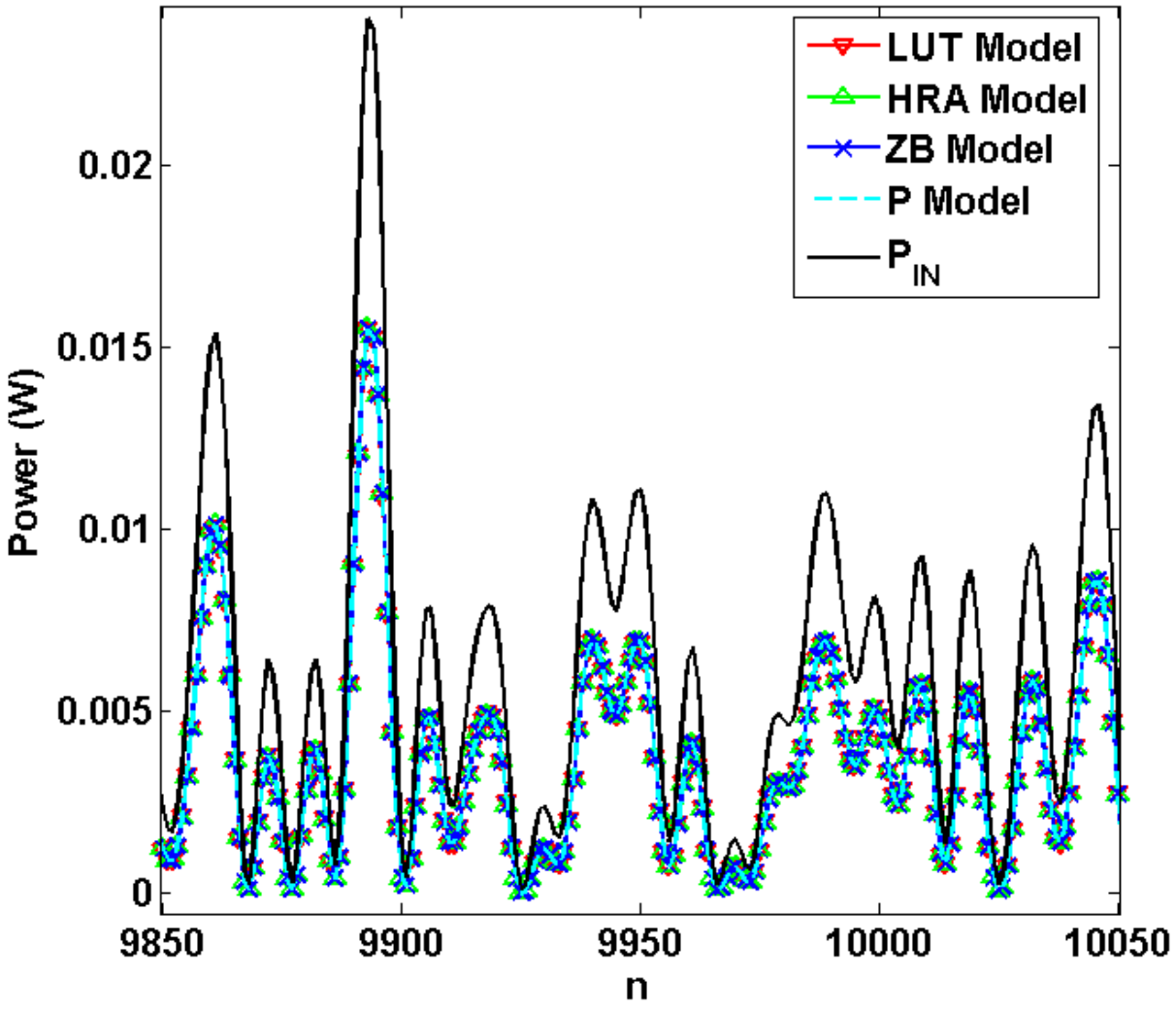


Figure 2.7: Input envelope power waveform and the linearized envelope power waveforms using CW linearizers for a diode power detector.

waveforms for a diode power detector using CW linearizers for a 64QAM modulated signal having 1MHz bandwidth. The CW linearizer corrects for the nonlinearity of the diode power detector but fails to account for the frequency response of the detector. To highlight the frequency response of the diode power detectors, the measured characteristic of a diode power

detector when excited by a 64QAM modulated signal having 1MHz bandwidth and that with a CW excitation at a carrier frequency of 2.5GHz are plotted and compared in Figure 2.8.

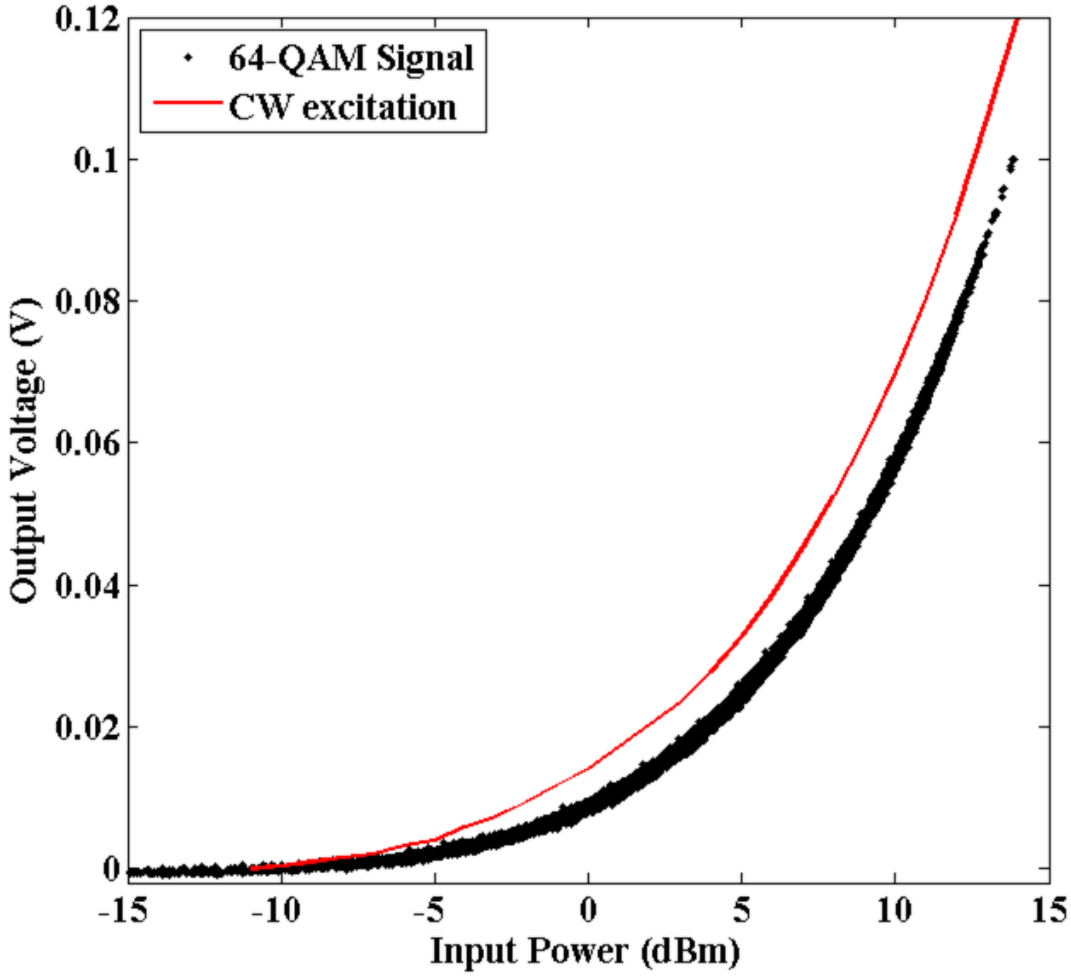


Figure 2.8: Behaviour of a diode power detector excited by a 64QAM modulated signal having 1MHz bandwidth and by a CW excitation at a carrier frequency of 2.5GHz.

In order to increase the dynamic range of the whole six-port based receiver system, the diode power detectors must be operated beyond their square law regions. It is obvious from Figure 2.8 that even in their square law regions, the linear relationship of output voltage and input power is not valid when the detector is excited by a modulated wireless signal. It shows that the nonlinearity and the memory effect displayed by the diode detectors must be modeled and

calibrated to reduce the error in the detections of the received symbols and to increase the dynamic range of the receiver system. CW linearizer models described in Section 2.1 fail to capture both the dynamic behaviour and the memory effect displayed by the diode detector under a wideband modulated wireless signal operation. A new method to model and linearize the diode power detectors is proposed in this section.

2.3.1 Diode Detector Linearizer for Modulated Signals

Memory polynomial [21] has been used effectively to linearize the power amplifier (PA) and transmitter characteristics. The diode power detector characteristic in this thesis is linearized using a modified memory polynomial [22]. The output voltage v_k corresponding to the input microwave power $P_{in,k}$ for the diode detector D_k is used to linearize its characteristic. The relationship between the linearized output power, $P_{out,k}$ from the proposed linearizer and the output voltage from the diode detector, $v_k[n]$ at any instant of time is modeled by equation (2.4). We call this diode detector linearizer model as memory polynomial (MP) model.

$$P_{out,k}[n] = \sum_{q=0}^{M_k} \sum_{p=1}^{N_k} c_{pqk} v_k^p[n-q] \tag{2.4}$$

Here c_{pqk} are the coefficients of the above memory polynomial, and N_k and M_k are the non-linearity order and the memory depth for the diode detector D_k, respectively, where $k = 3,4,\ldots,6$ is the number of the diode detector.

The metric normalized mean square error (NMSE) between the actual input power $P_{in,k}$ and the linearized output power $P_{out,k}$ is used to assess the performance of the proposed linearizer. NMSE calculated over N samples of the actual input power and the linearized output power is defined as in equation (2.5).

$$NMSE = 10\log_{10}\left(\frac{\sum_{n=1}^{N}\left|P_{out,k}[n] - P_{in,k}[n]\right|^2}{\sum_{n=1}^{N}\left|P_{in,k}[n]\right|^2}\right) \tag{2.5}$$

The same test setup as described in subsection 2.2.1 is used to evaluate the performance of the proposed linearizer. First 100 symbols from the 2500 randomly generated test symbols are used as a training sequence to extract the model coefficients for the diode detector linearizer. Equation (2.4) is written in a matrix form as in equation (2.6).

$$P_{out,k}[n] = \boldsymbol{V}^T[n]\boldsymbol{C} \tag{2.6}$$

where $\boldsymbol{C}^T = [c_{10k} \quad \cdots \quad c_{N_k0k} \quad c_{11k} \quad \cdots \quad c_{N_k1k} \quad \cdots \quad c_{1M_kk} \quad \cdots \quad c_{N_kM_kk}]$ and

$\boldsymbol{V}^T[n] = \left[v_k[n] \quad \cdots \quad v_k^{N_k}[n] \quad v_k[n-1] \quad \cdots \quad v_k^{N_k}[n-1] \cdots v_k[n-M_k] \quad \cdots \quad v_k^{N_k}[n-M_k]\right]$

Solution to the equation (2.6) can be obtained from the normal equation given in equation (2.7) using the method of least squares [23].

$$\Phi\boldsymbol{C} = \boldsymbol{z} \tag{2.7}$$

where Φ is the correlation matrix of the input data $\boldsymbol{V}[n]$, and $\boldsymbol{z}$ is the cross-correlation vector between the inputs $\boldsymbol{V}[n]$ and some desired response $d[n]$.

The correlation matrix Φ can be written in terms of a data matrix $\boldsymbol{A}$**,** whose Hermitian transpose is defined by $\boldsymbol{A}^H = [\boldsymbol{V}[M] \quad \boldsymbol{V}[M+1] \quad \cdots \quad \boldsymbol{V}[N]]$

$$= \begin{bmatrix} V(M) & V(M+1) & \cdots & V(N) \\ V(M-1) & V(M) & \cdots & V(N-1) \\ \vdots & \vdots & \vdots & \vdots \\ V(1) & V(2) & \cdots & V(N-M+1) \end{bmatrix} \tag{2.8}$$

Here M is related to the size of the coefficient matrix $\boldsymbol{C}$ and N is related to the size of the input data. Using the definition in equation (2.8), the correlation matrix Φ can be written in a compact from as in equation (2.9).

$$\Phi = \boldsymbol{A}^H \boldsymbol{A} \tag{2.9}$$

Similarly, if we introduce a desired data vector $\boldsymbol{d}$, consisting of the desired response $d(i)$, depending on the input power $P_{in,k}[i]$ for the values of i in the interval $[M, N]$ then

$$\boldsymbol{d}^H = [d(M) \quad d(M+1) \quad \cdots \quad d(N)] \tag{2.10}$$

and the cross-correlation vector $\boldsymbol{z}$ can be written as in equation (2.11).

$$\boldsymbol{z} = \boldsymbol{A}^H \boldsymbol{d} \tag{2.11}$$

Equation (2.7) can be rewritten to get the coefficient vector $\boldsymbol{C}$ directly in terms of data matrices.

$$\boldsymbol{C} = (\boldsymbol{A}^H \boldsymbol{A})^{-1} \boldsymbol{A}^H \boldsymbol{d} \tag{2.12}$$

Here $\boldsymbol{A}$ is the data matrix representing the time evolution of the input vectors $\boldsymbol{V}[n]$, and $\boldsymbol{d}$ is the desired data vector representing the time evolution of the desired response.

If we define a matrix

$$\boldsymbol{A}^+ = (\boldsymbol{A}^H \boldsymbol{A})^{-1} \boldsymbol{A}^H \tag{2.13}$$

then we may rewrite the equation (2.12) simply as

$$\boldsymbol{C} = \boldsymbol{A}^+ \boldsymbol{d} \tag{2.14}$$

The matrix $\boldsymbol{A}^+$ is called the pseudoinverse or the Moore-Penrose generalized inverse of the matrix $\boldsymbol{A}$ [23]. Using equation (2.14), the coefficient matrix $\boldsymbol{C}$ for the diode detector linearizer can be obtained, given the input data matrix $\boldsymbol{A}$ and the desired response vector $\boldsymbol{d}$.

In order to determine the optimal model coefficients, the memory depth M_k and the non-linearity order N_k are varied and the corresponding NMSEs are recorded. The (M_k, N_k) pair having the least acceptable NMSE is fixed for the diode detector D_k. The corresponding linearizer model coefficients vector $\boldsymbol{C}$ for the particular test waveform is used to linearize the power detector using equation (2.6). The NMSE performance a typical Shottky diode detector is shown in

Figure 2.9. The measured and the modeled behavior of a diode power detector using the modeling approach developed here are shown in the Figure 2.10.

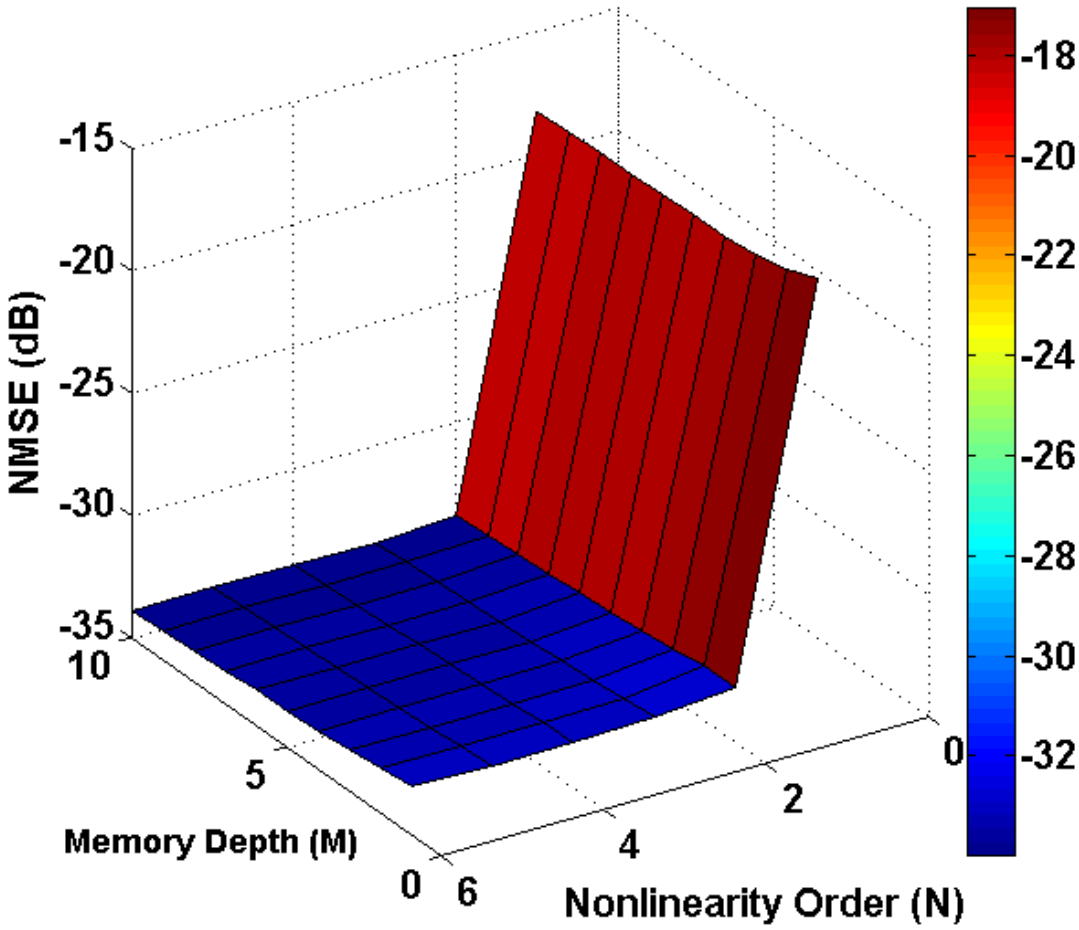


Figure 2.9: NMSE performance of a memory polynomial based linearizer for Shottky diode power detector.

Table 2.2 summarizes the performance of the proposed linearizer model for the detector in terms of NMSE.

Table 2.2: Performance summary of the proposed model of the power detector linearizer

Signal Type	N_k	M_k	Normalized Mean Square Error (NMSE)
64QAM 1MHz BW	4	9	-36.8 dB

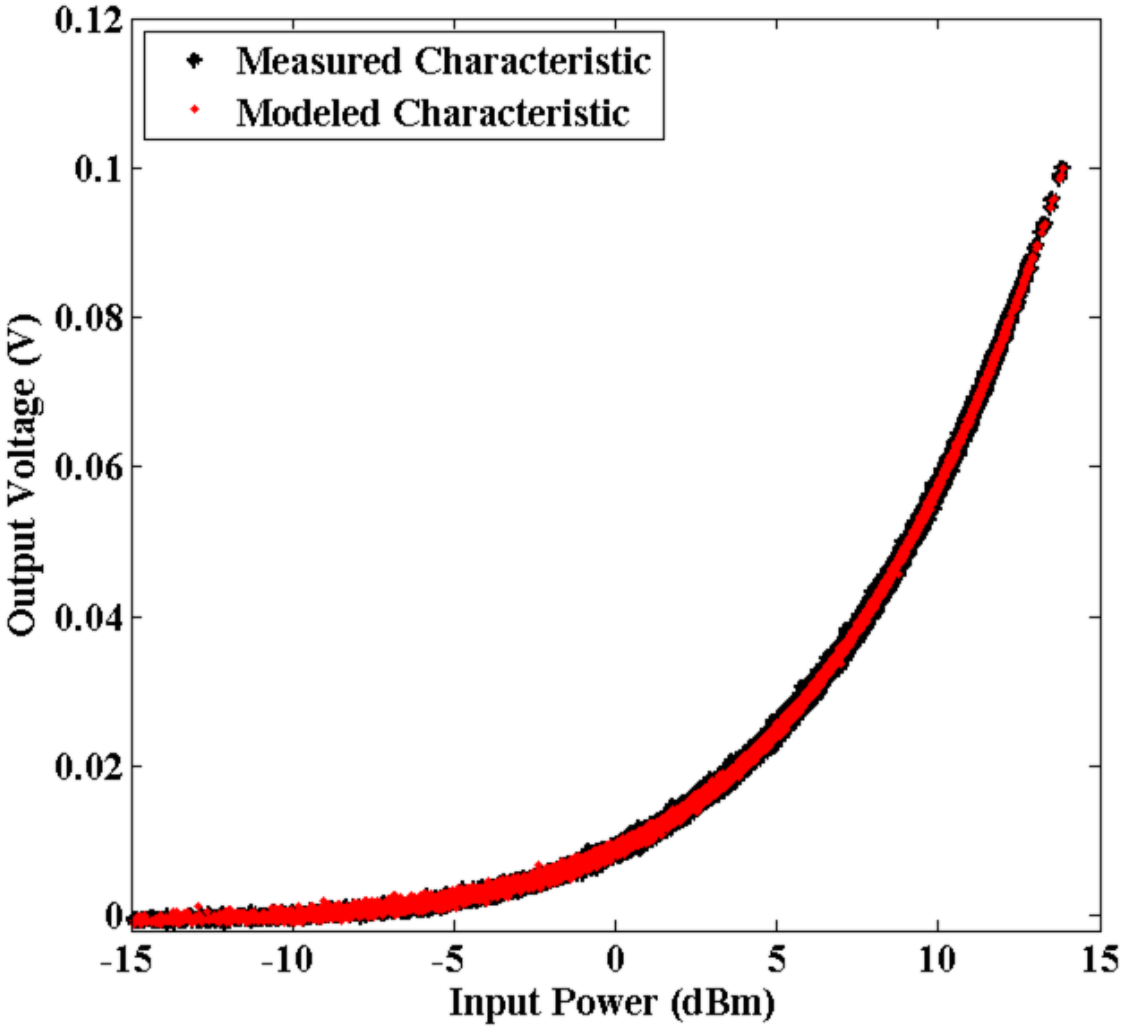


Figure 2.10: Measured and modeled behaviour of a diode power detector excited by a 64QAM modulated signal having 1MHz bandwidth at a carrier frequency of 2.5GHz.

Figure 2.11 shows the comparison of the linearized output envelope power waveforms with the actual input envelope power waveform from the different diode detector linearizer studied in this chapter. All the CW detector linearizers have similar performance but the proposed memory polynomial based detector linearizer model (MP model) outperforms all of the CW linearizers as expected. In chapter four of this thesis, we use this proposed diode detector linearizer model for accurate modeling and calibration of a six-port based receiver system.

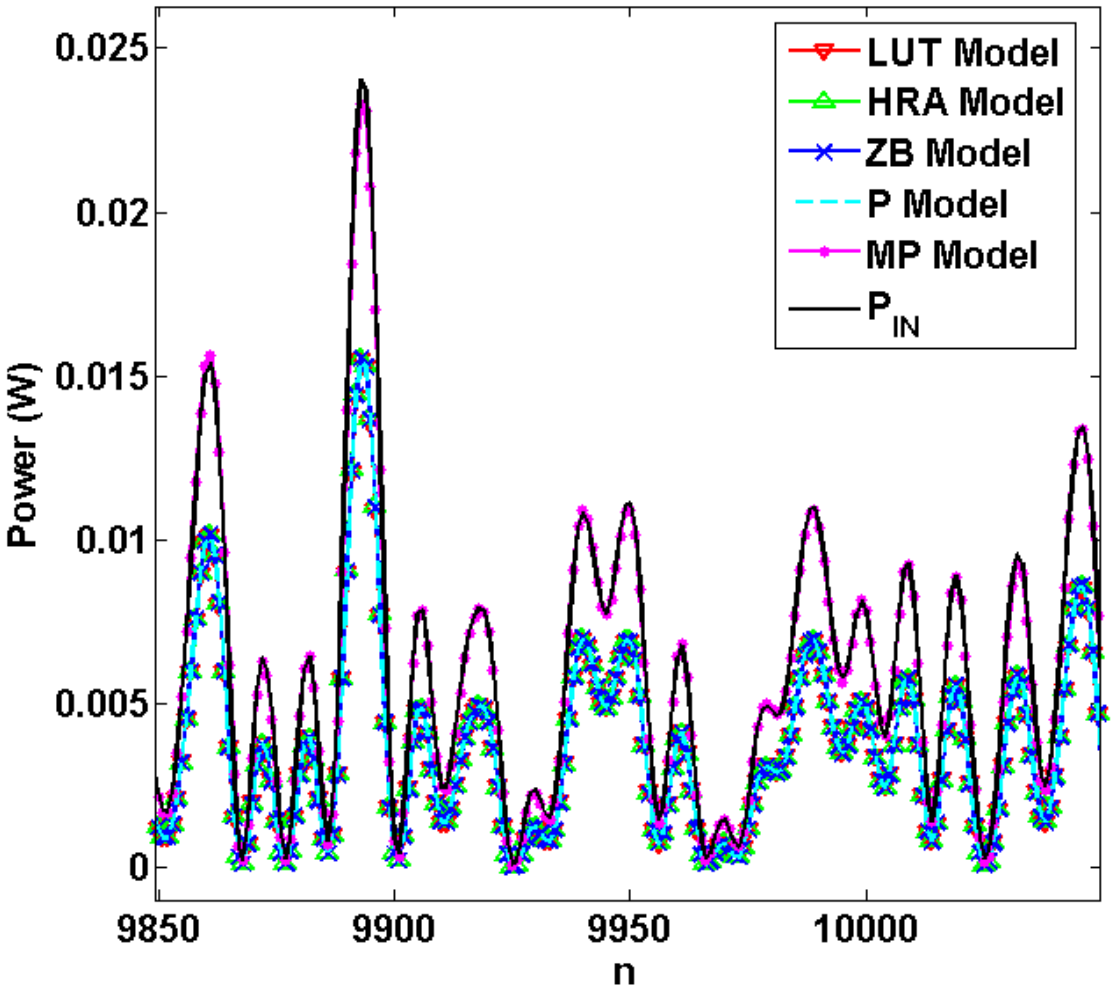


Figure 2.11: Actual input power waveform and the linearized output power waveforms for a 64QAM modulated signal having 1MHz bandwidth at a carrier frequency of 2.5GHz.

The ideal slope of the linearized output power versus actual input power plots should be unity. Figure 2.12 shows the comparison of the proposed linearizer performance with the existing CW linearizers. The CW linearizers deviate from the usual unity slope characteristic while the proposed memory polynomial based linearizer attempts to account for the nonlinearity and the memory effect of the diode detector and follows the ideal unit slope characteristic.

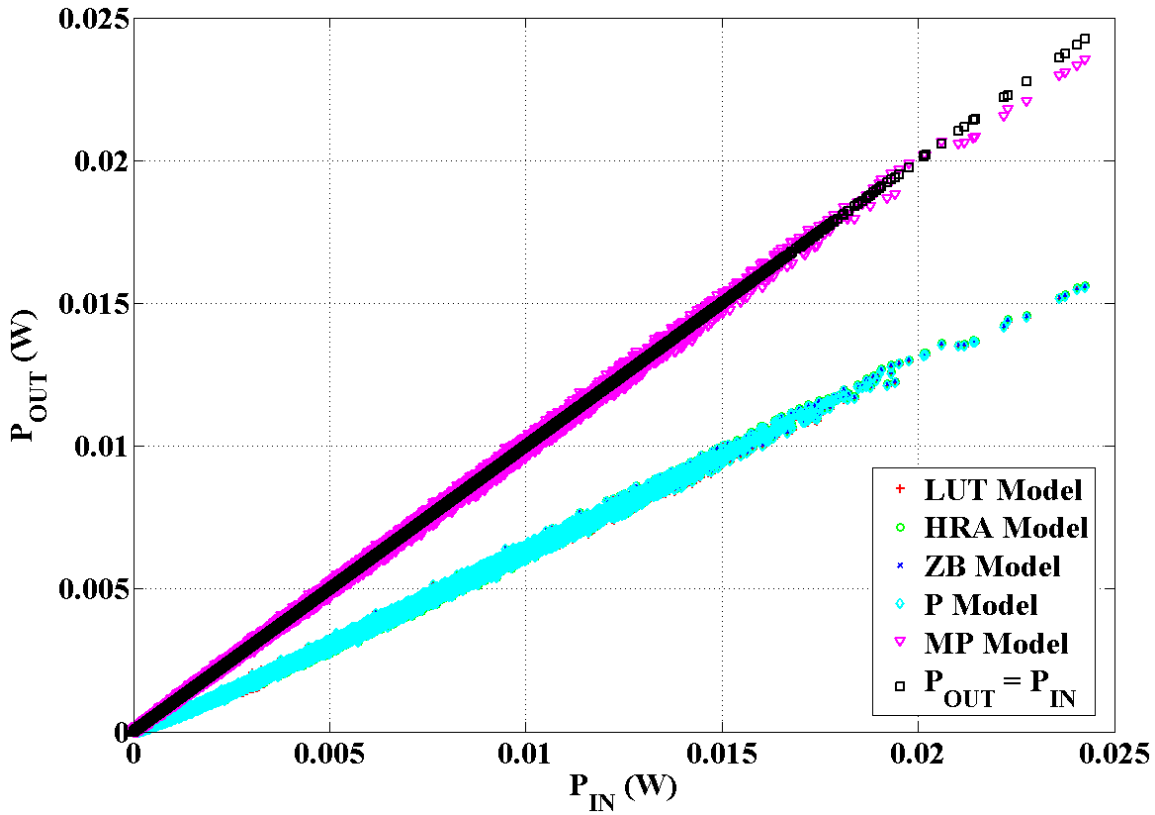


Figure 2.12: Plots of linearized output envelope powers versus actual input envelope power for different diode detector linearizers.

2.4 Conclusion

In this chapter we saw that the behaviour of the diode power detector is different for different excitation signals. This behaviour is remarkably altered from the continuous wave (CW) characteristic of the diode power detector. The CW linearizers based on CW characterization of the diode power detectors result in error when the voltages generated in response to the real modulated signals are given as input to the CW linearizers for linearization. Based on the observations in this chapter, we have proposed a peak power detector linearizer for peak power detection applications. We also proposed a new memory polynomial based linearizer for the diode power detectors that corrects for the nonlinearity and the memory effect displayed by the

detectors. The memory polynomial based linearizer is a wideband signal detector linearizer which accounts for the frequency response of the diode power detectors. The linearizer model for the diode power detector developed in this chapter will be used in modeling the six-port based receiver system. It will be shown in chapter four of this thesis that the memory polynomial based detector linearizer improves the performance of the overall six-port based receiver system employing diode power detectors.

Chapter Three: **Nonlinear Modeling and Calibration of Six-Port Receiver**

We mentioned briefly in chapter one that the modeling and calibration approaches for a six-port based receiver (SPR) system can be broadly categorized into two approaches; namely the linear and the nonlinear modeling and calibration approaches. In this chapter we describe and propose a nonlinear modeling and calibration approach for the SPR systems. We know from equation (1.6) that the microwave power detected by the kth diode power detector in an SPR system is given by

$$P_k = |S_{k2}\boldsymbol{a_{RF}} + S_{k1}\boldsymbol{a_{LO}}|^2; k = 3,4,\dots,6 \tag{3.1}$$

If $q_k = -\frac{S_{k1}}{S_{k2}}$, then the equation (3.1) can be written as in equation (3.2) [11].

$$P_k = |c_k|^2|R - q_k|^2; k = 3,4,\dots,6 \tag{3.2}$$

Here $|c_k|^2 = |S_{k2}|^2|\boldsymbol{a_{LO}}|^2$ is a real parameter depending on the S-parameters of the six-port junction and the LO power. $R = \frac{\boldsymbol{a_{RF}}}{\boldsymbol{a_{LO}}}$ represents the phasor of the received RF signal with respect to the LO signal phasor. R and q_k are complex parameters depending on the RF and the LO signals, and the six-port junction S-parameters, respectively. The four equations in (3.2) represent circles in a complex R-plane whose centres and radii are given by q_k and $r_k = \frac{\sqrt{P_k}}{|c_k|}$, respectively. The centres of these circles are fixed for a given SPR system as they are functions of the S-parameters of the six-port junction. The set of equations in (3.2) is an over determined system of equations as the complex received signal R corresponds to the point of intersection of the four circles in the complex R-plane. Theoretically only three circles are enough to describe a point in a complex Cartesian coordinate system plane. From equation (3.2), we find that a total of 12 real parameters (four complex parameters q_k and four real parameters r_k) are required to describe the SPR system fully. These parameters must be determined before calculating any received signal R. Number of the calibration parameters can be reduced if some forms of

transformations are used on the over determined system of equations. We next describe a two-step nonlinear modeling and calibration approach using a bilinear transformation for the SPR systems.

3.1 Nonlinear Modeling of SPR systems

Microwave powers measured from the detectors 4, 5, and 6 in equation (3.2) can be normalized with respect to a reference port power P_3 to eliminate the influence of LO power ($|a_{LO}|^2$) on the calibration procedure. This normalization process produces three normalized powers

$$p_k = \frac{P_k}{P_3} = h_k^2 \frac{|R-q_k|^2}{|R-q_3|^2}, k = 4,5,6. \tag{3.3}$$

Here $h_k^2 = \frac{|S_{k2}|^2}{|S_{32}|^2}$. Equation (3.3) represents three circles in a complex R-plane, the centers and radii of which are independent of the LO power, and are determined solely by the system parameters and the readings of the four power detectors. Equation (3.3) can be simplified further and made more tractable by introducing an intermediate complex signal T [11] such that

$$p_4 = |T|^2 \tag{3.4a}$$

$$p_5 = \frac{1}{A^2}\left|T - |m|\right|^2 \tag{3.4b}$$

$$p_6 = \frac{1}{B^2}|T - n|^2 \tag{3.4c}$$

Here n is a complex constant, and A, B, and $|m|$ are real constants functions only of the system parameters. Once the intermediate complex signal T is known, it can be used to get R and hence the received signal $R' = a_{RF} = I_{RF} + jQ_{RF}$ through a bilinear transformation given in equation (3.5).

$$T = \frac{d'R+e'}{c'R+1} = \frac{dR'+e}{cR'+1} \tag{3.5}$$

Here $c, d,$ and e are three complex constants, functions only of the system parameters and the LO

signal a_{LO}. Equations (3.3), (3.4), and (3.5) represent the nonlinear model of an SPR system. Nonlinear calibration of the SPR system involves determining the model parameters embedded in these three equations. The nonlinear model for the SPR system developed here involves 11 real constants (4 complex parameters $c, d, e,$ and n, and 3 real parameters A,B, and $|m|$). We next describe the nonlinear calibration approach for an SPR system.

3.2 Nonlinear Calibration of SPR systems

The nonlinear calibration procedure for an SPR system can be divided into two steps: the 'receiver calibration' step (P_k to T reduction) and the 'phase alignment' step (T to R' estimation) to simplify the calibration procedure.

3.2.1 Receiver Calibration Step (P_k to T reduction)

From equation (3.4), the intermediate complex signal T can be eliminated [24] to get equation (3.6) which is independent of both the LO power as well as the RF signal. This equation depends only on the receiver system parameters and we will call this step as 'Receiver Calibration' Step or 'P_k to T reduction' step.

$$pp_4^2 + qA^4p_5^2 + rB^4p_6^2 + (r-p-q)A^2p_4p_5 + (p-q-r)A^2B^2p_5p_6 + (q-p-r)B^2p_6p_4 + p(p-q-r)p_4 + q(q-r-p)A^2p_5 + r(r-p-q)B^2p_6 + pqr = 0 \quad (3.6)$$

Here $p = \left||m| - n\right|^2, q = |n|^2, r = |m|^2, A^2,$ and B^2 are five real parameters to be determined in this step of the nonlinear calibration procedure. Once these calibration parameters are known, the real and the imaginary parts of the intermediate complex signal T can be determined from equation (3.7). Process of getting (3.7) is summarized in Figure 3.1 by plotting equation (3.4) in a complex- T plane.

$$Re\{T\} = \frac{r_0^2 - r_m^2 + |m|^2}{2|m|} \quad (3.7a)$$

$$Im\{T\} = \frac{1}{\sqrt{1-z^2}}\left[\frac{r_0^2 - r_n^2 + |n|^2}{2|n|} - \frac{z\left(r_0^2 - r_m^2 + |m|^2\right)}{2|m|}\right] \tag{3.7b}$$

where $r_0^2 = p_4$, $r_m^2 = A^2 p_5$, $r_n^2 = B^2 p_6$, and $z = \frac{q+r-p}{2\sqrt{qr}}$.

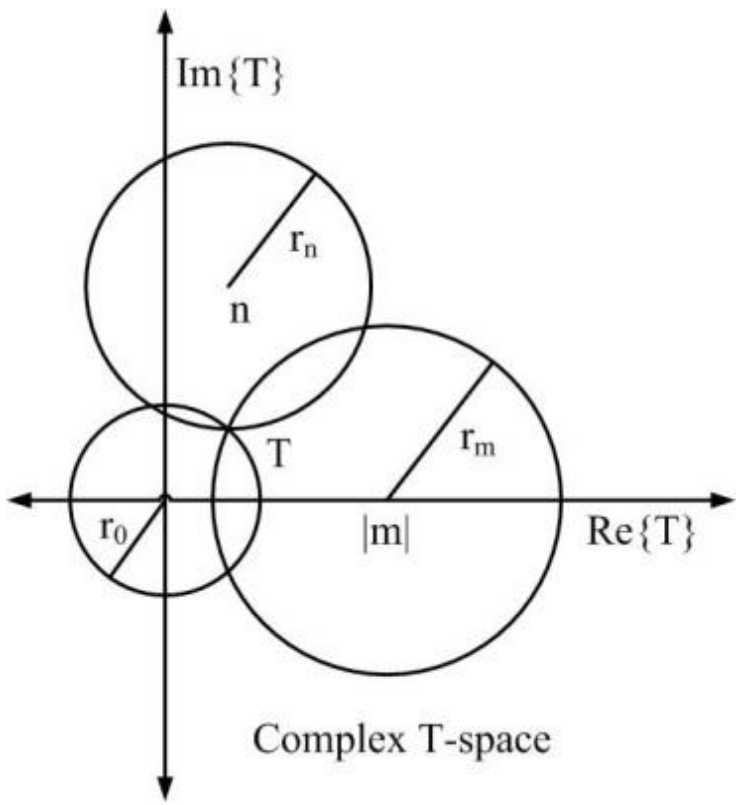


Figure 3.1: Evaluation of T from equation (3.4) in the 'Receiver Calibration' step.

The receiver calibration is a 'one-time' process and can be carried out at the beginning of a communication process or occasionally to take care of any 'aging' effect on the receiver system. The primary difference between a linear calibration approach and a nonlinear calibration approach lies in the computation of LO power independent receiver calibration parameters.

3.2.2 Phase Alignment Step (T to R estimation)

In the 'Phase Alignment' step or the 'T to R' estimation' step, the intermediate received signal T is corrected for its amplitude and phase to get back the original received signal R'. From equation (3.5), the received signal R' can be estimated from the intermediate received signal T

by an inverse bilinear transformation using equation (3.8), if the three complex phase alignment parameters $c, d,$ and e are known.

$$R' = \frac{T-e}{d-cT} \tag{3.8}$$

Calibration procedure to get the five real 'receiver calibration' parameters and the three complex 'phase alignment' parameters will be discussed in Section 3.4.

The process of nonlinear calibration of an SPR system involving the 'receiver calibration' step and the 'phase alignment' step is summarized in Figure 3.2.

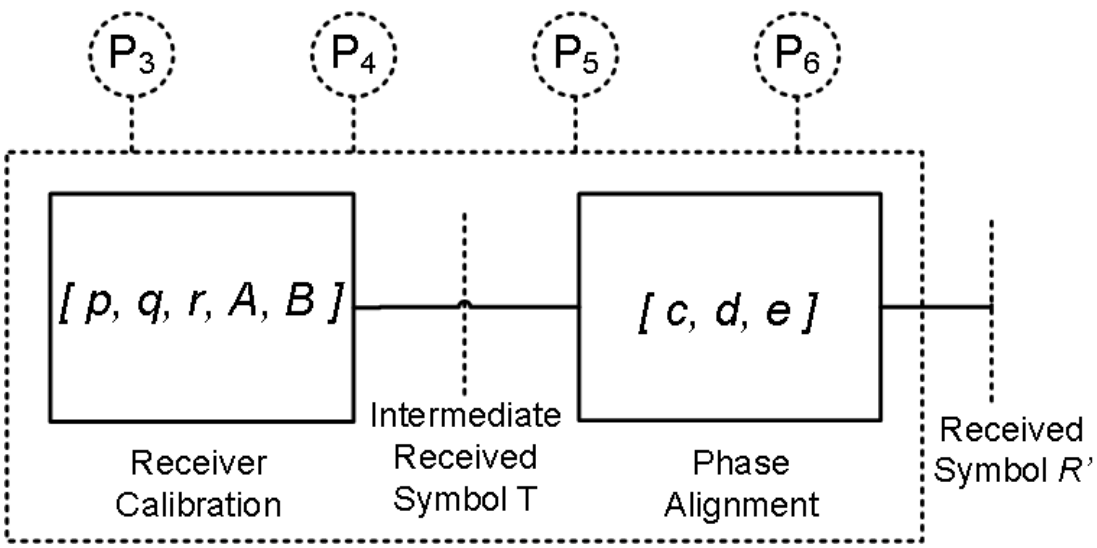


Figure 3.2: Receiver calibration and phase alignment steps for nonlinear calibration of a SPR system.

3.3 Implementation of SPR System

A SPR system is configured and implemented as modified Engen's structure for six-port junction [26]. The structure is reproduced here for convenience in Figure 3.3. Implementation of the receiver for six-port junction structure and detectors has been done using off-the-shelf available microwave components. Q_1 is a quadrature hybrid of C3200 series from MAC Technology, Inc. Q_2, Q_3, and Q_4 are 3dB directional couplers (P/N: 2032-6371-00), D is a 3dB power divider

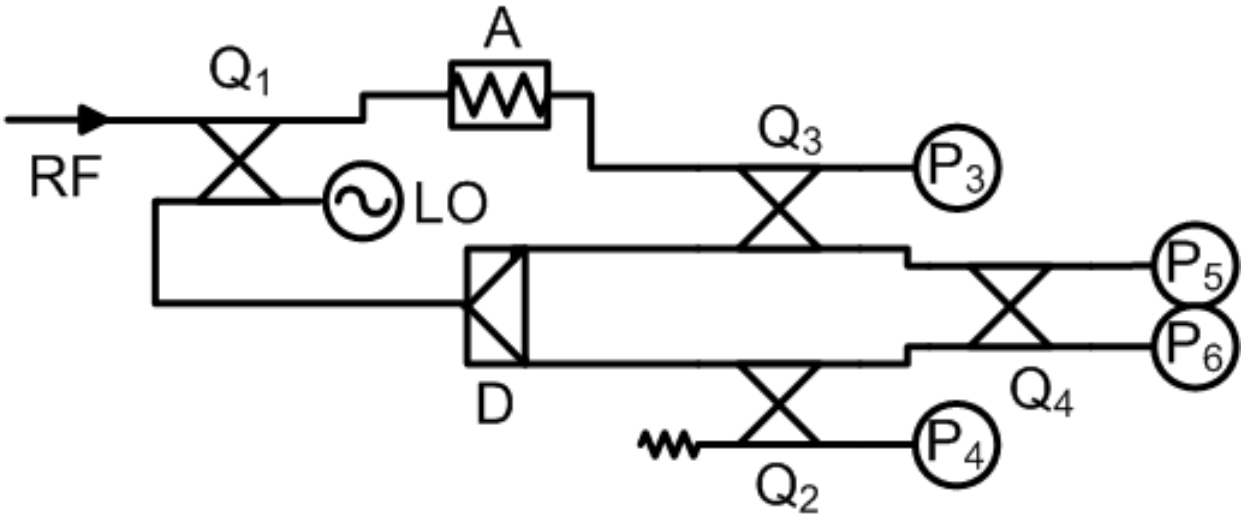


Figure 3.3: Structure of six-port junction for receiver architecture.

(P/N: 2090-6205-00), and A is a 3dB attenuator (P/N: 2082-6145-03), all from M/A-COM Technology Solutions. Four zero-bias low barrier Schottky diode detectors (P/N: 8472B) from Agilent Technologies, Inc. have been used as power detectors. The complete set-up for the six-port based receiver test-bench is shown in Figure 3.4. In the test-bench set-up shown in Figure 3.4, the baseband I/Q data is generated on a desktop PC in MATLAB. This base-band data is raised cosine filtered before passing to an I/Q modulation generator (AMIQ from Rhode & Schwarz GmbH & Co.). The I/Q modulated data is then frequency up-converted to 2.5GHz using SMIQ 03B vector signal generator from Rhode & Schwarz. The LO signal at 2.5GHz is supplied by a PSG CW Signal Generator (E8247C from Agilent Technologies). Voltages generated by the Shottky detectors are captured using two synchronized dual-channel VSAs (89600 series VSA from Agilent Technologies). The captured voltages are used for linearization of the power detectors, calibration of the complete SPR, and for the detection of the received symbols. The nonlinear calibration procedure for the SPR system and the linearization of the power detectors are explained in the next section.

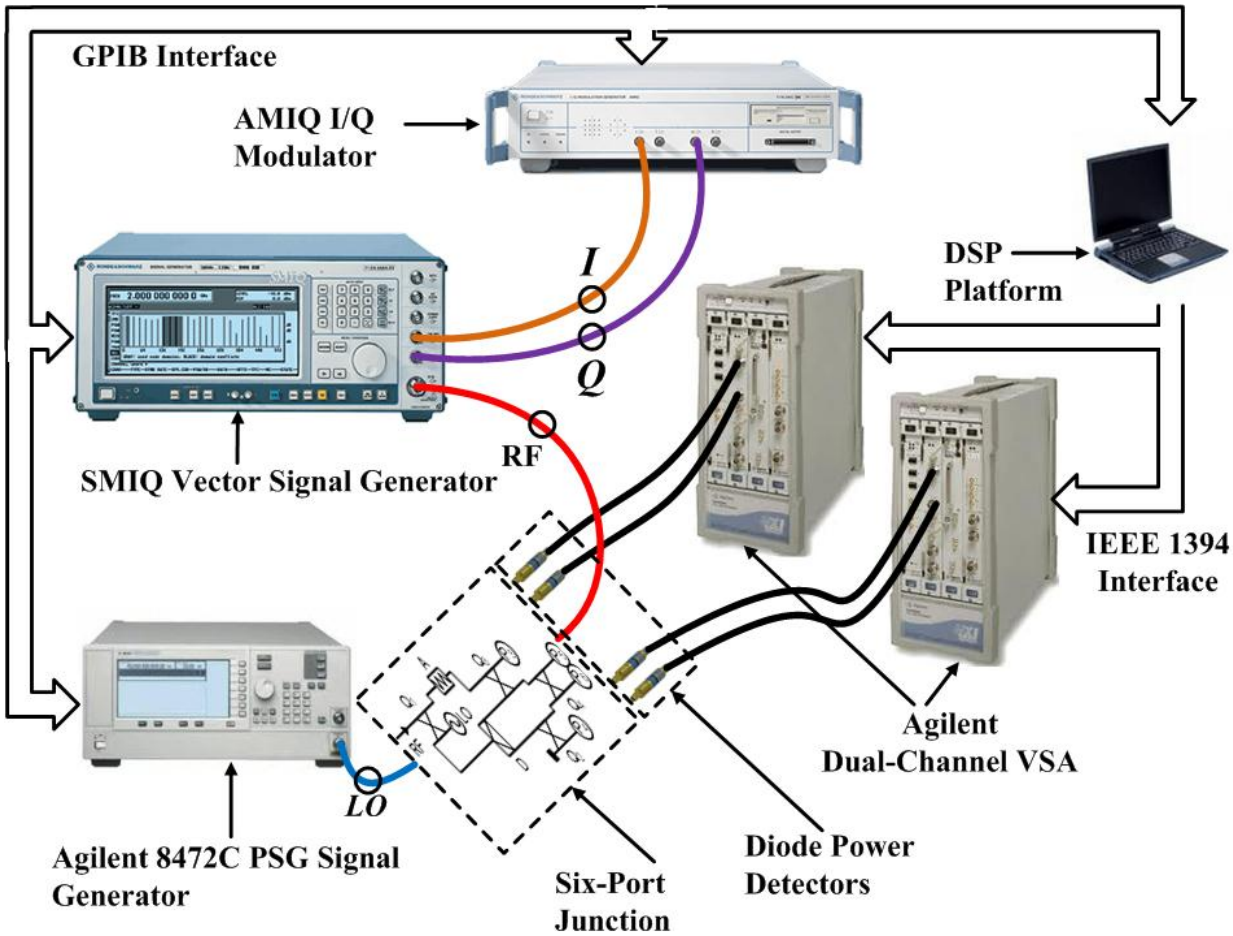


Figure 3.4: Test set up for the six-port based receiver system.

3.4 Nonlinear Auto-Calibration Procedure

We know from Section 3.2 that the nonlinear calibration procedure is divided into two steps: the receiver calibration step and the phase alignment step. The first step results in the calibration of five real parameters (p, q, r, A, and B) for the SPR system while the second step yields three complex calibration parameters (c, d, and e). In order to be able to accurately receive the signal R', very precise calibration for the phase alignment parameters has to be done. The calculation of the phase alignment parameters in this thesis is realized by sending a stream of known symbols sequence. This known training sequence is added at the beginning of an actual test data burst.

The training sequence requirement for the phase alignment parameters calculation in real communication systems can be met by standard communication headers. The use of training sequence for calibration purpose is a dynamic procedure which takes care of any 'aging' effects on the SPR system. The training sequence in this thesis consists of twenty-five different known constellation points in the signal space as shown in Figure 3.5. Each symbol of the training sequence is repeated twenty-five times before sending a new symbol from the training sequence constellation points. This repetition is done to bypass the frequency response of the six-port circuit so that we are able to get the phase alignment parameters very accurately by incorporating the middle symbols of each repetition bursts in the calculations.

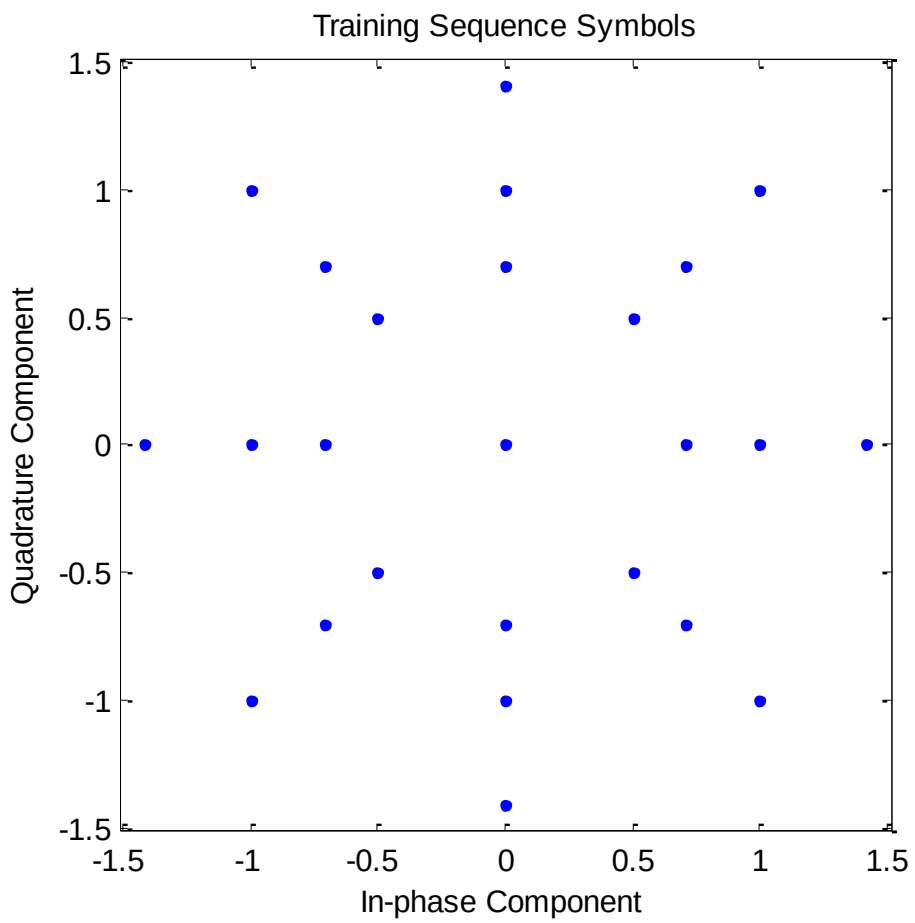


Figure 3.5: Constellation points of training sequence symbols.

3.4.1 Receiver Calibration

For the receiver calibration step, the three normalized power readings corresponding to the thirteen random symbols (minimum nine as obvious from equation (3.9) for unique solution) from the actual test data burst are recorded and equation (3.6) is re-written for each symbol in a matrix form as shown in equation (3.9). Equation (3.9) is solved using the steepest descent gradient method till a precision of better than 5×10^{-2} is achieved in the norm of $\boldsymbol{X} = [x_1 \quad \cdots \quad x_9]^T$.

$$\begin{bmatrix} p_4^2(1) & p_5^2(1) & p_6^2(1) & p_4p_5(1) & p_5p_6(1) & p_6p_4(1) & p_4(1) & p_5(1) & p_6(1) \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ p_4^2(13) & p_5^2(13) & p_6^2(13) & p_4p_5(13) & p_5p_6(13) & p_6p_4(13) & p_4(13) & p_5(13) & p_6(13) \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_9 \end{bmatrix}$$

$$= [-1 \quad -1 \quad \cdots \quad 13\ terms]^T \tag{3.9}$$

Receiver calibration parameters are obtained from $x_1, x_2, \ldots, x_9$ using equation (3.10).

$$r = (2x_5 - x_7x_9)/(2x_1x_9 - x_5x_7) \tag{3.10a}$$

$$q = (2x_4 - x_7x_8)/(2x_1x_8 - x_4x_7) \tag{3.10b}$$

$$p = r + q + x_7/x_1 \tag{3.10c}$$

$$A = \sqrt[4]{x_2pr} \tag{3.10d}$$

$$B = \sqrt[4]{x_3pq} \tag{3.10e}$$

Using the above calibration parameters and the normalized power readings from the power detectors, intermediate received signal *T* is calculated for the whole test data burst from equation (3.7). This intermediate received signal *T* should be corrected for its phase and magnitude to get back the original transmitted symbol *R'*.

3.4.2 Phase Alignment Box Calibration

The intermediate T signals $T^{(1)}, T^{(2)}, \text{and } T^{(3)}$ corresponding to three well-distributed known symbols $R^{(1)}, R^{(2)}, \text{and } R^{(3)}$ of the training signal, evaluated in the previous step, are used for the phase alignment calibration. Equation (3.5) can be manipulated and re-written as follows for the three measurements corresponding to three different known symbols [28].

$$\begin{bmatrix} -T^{(1)}R^{(1)} & R^{(1)} & 1 \\ -T^{(2)}R^{(2)} & R^{(2)} & 1 \\ -T^{(3)}R^{(3)} & R^{(3)} & 1 \end{bmatrix} \begin{bmatrix} c \\ d \\ e \end{bmatrix} = \begin{bmatrix} T^{(1)} \\ T^{(2)} \\ T^{(3)} \end{bmatrix} \tag{3.11}$$

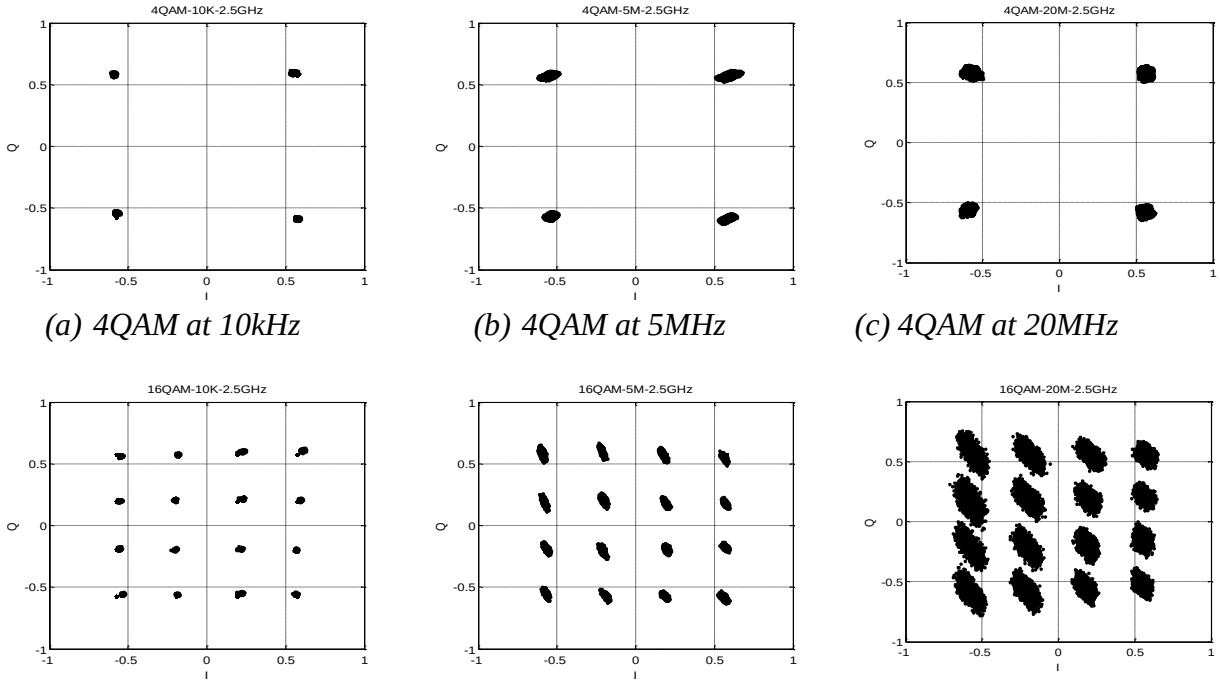
The phase alignment calibration parameters *c*, *d*, and *e* are the only unknowns in equation (3.11), which can be solved for these 'phase-alignment' parameters.

3.4.3 Power Detectors Linearization

In order to increase the dynamic range of the receiver system, a look-up-table (LUT) based linearization technique for diode detectors has been used [16]. Though all the four power detectors are from the same manufacturer bearing the same part numbers, their power detection characteristics do not match to each other precisely. To minimize the error during the receiving process of I/Q modulated symbols, four individual LUTs are maintained to linearize the four power detectors used in the receiver system. Input power to the power detectors is varied from -19dBm to 19dBm with a step of 1dBm and the output voltages are recorded to make LUT for individual diode detectors. LUT is used to linearize the individual diode detector characteristic and power readings corresponding to the recorded voltages are found out using interpolation based on the corresponding LUT entries. The entire process of power detector linearization, nonlinear calibration of the SPR system, and the decoding of the received symbols has been implemented in MATLAB.

3.5 Measurement Results

In order to evaluate the performance of the calibration procedure and the receiver system, 2000 random 4QAM and 16QAM symbols are generated in MATLAB. These test symbols are passed through a raised cosine filter of roll-off factor 0.3 and a delay of 3 taps (up sampled by 4). A training sequence is added before the actual test data burst and then the combined signal is sent to an I/Q modulation generator. I/Q modulated baseband data is frequency up-converted to 2.5GHz to simulate an actual RF modulated received signal. This I/Q modulated pass-band data is fed to the RF port (PORT-*2*) of the SPR system. LO signal at 2.5GHz is supplied by a PSG generator as described in section 3.3. LO power is set to be 18dBm and the mean RF power is set to 13dBm (peak power = 17.5dBm). Voltages generated by the four power detectors are captured using two synchronized dual channel VSAs.

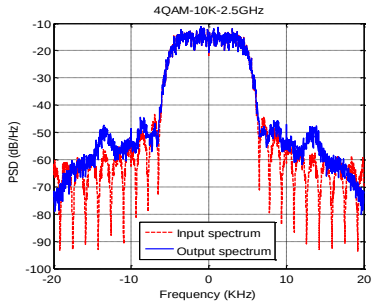


(a) 4QAM at 10kHz *(b) 4QAM at 5MHz* *(c) 4QAM at 20MHz*

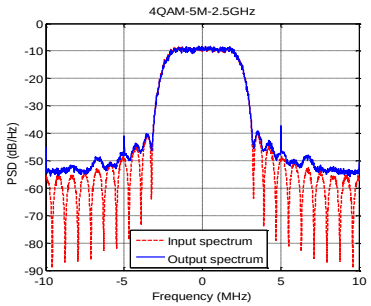
(d)16QAM at 10kHz *(e)16QAM at 5MHz* *(f)16QAM at 20MHz*

Figure 3.6: Constellation points of transmitted and received symbols of 4QAM and 16QAM symbols at different symbol rates.

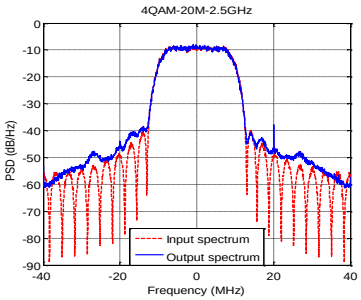
Power detectors are linearized using an LUT based linearization technique and the whole system is calibrated as explained in Section 3.4. The calibrated system is used to decode the received symbols in an actual test data burst. Baseband data with symbol rates of 10kHz, 5MHz and 20MHz were generated, transmitted and decoded in this six-port based receiver system evaluation. The measurement results obtained for the 4QAM and 16QAM test symbols at different symbol rates are shown in Figures 3.6 and 3.7. Figure 3.6 shows the constellation points of 4QAM and 16QAM signals received and sent at different symbol rates. The frequency spectrum of the transmitted and received symbols for this receiver system at different symbol rates employing different modulation schemes are shown in Figure 3.7.



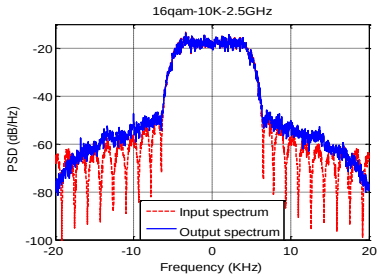
(a) 4QAM at 10kHz



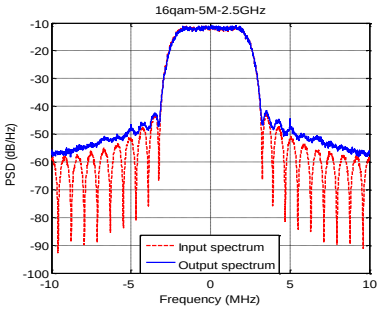
(b) 4QAM at 5MHz



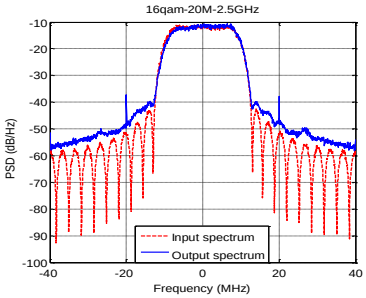
(c)4QAM at 20MHz



(a) 16QAM at 10kHz



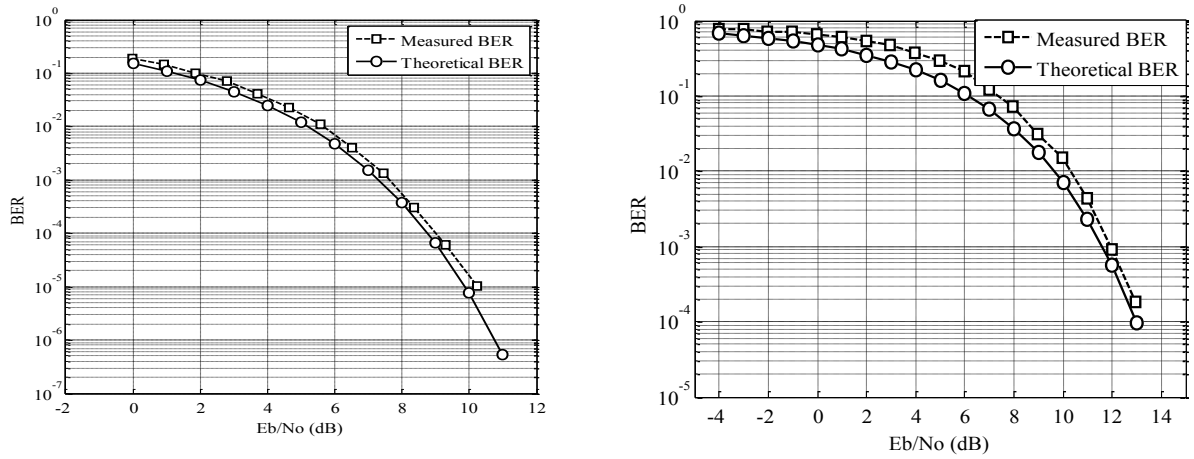
(b) 16QAM at 5MHz



(d)16QAM at 20MHz

Figure 3.7: Frequency spectrum of the transmitted and the received symbols for 4QAM and 16QAM symbols at different symbol rates.

Frequency spectrums of the received symbols, as decoded by the nonlinearly calibrated receiver system, follow the spectrums of the ideal transmitted symbols. The receiver system does not distort the spectrum of the transmitted symbols in the desired band of frequency and it does not generate any spurious frequencies within or outside the desired band. For all the test cases in the system evaluation, the carrier to side band generated noise ratio is found out to be better than 30dB.The theoretical and the measured bit error rate (BER) plots as obtained from the receiver system for two different modulation scheme signals are shown in Figure 3.8. From the BER plots, we can observe that the bit error rates for a wide range of E_b/N_0 values are close to their theoretical limits. Validity of the calibration approach and its accuracy is verified from all the above measurement results. The results are found out to be satisfactory and acceptable for a real communication system.



(a) 4QAM *(b) 16QAM*

Figure 3.8: Theoretical and measured BER plot for (a) 4QAM, and (b) 16QAM symbols at 10kHz symbol rate.

3.6 Linear vs. Nonlinear Modeling of Six-Port Receiver system

In this chapter, we have provided the details of a proposed nonlinear modeling and calibration approach for the six-port based receiver systems. We proposed a nonlinear auto-calibration method that used a known training sequence to calibrate the SPR system. If the nonlinearities and the memory effects displayed by the diode power detectors are included in the nonlinear modeling of the SPR system, the modeling and the calibration of the whole system become intractable and impractical. In the next chapter we describe an alternative modeling and calibration approach for the SPR system where the imperfections displayed by the diode power detectors and other circuit components are included in the modeling and calibration of the whole receiver system. The imperfections are easily compensated for thorough a suitable calibration means in this modeling approach for an SPR system. We call this approach as the linear modeling and calibration approach for the SPR systems. Before going into the details of linear modeling and calibration of an SPR system, we will first describe some architectural differences between the linear and the nonlinear modeling approaches for the six-port based receiver systems. As mentioned in Section 1.4, the six-port junction comprises of many passive microwave circuits and components. There are a variety of configurations proposed in the open literature to implement the six-port junction circuitry [11]. The most common implementations of the six-port junction circuitry use quadrature hybrids, Wilkinson power dividers, ring hybrids, T-junctions and even discrete resistors, capacitors, and inductors. All the implementations can be largely classified into two broad categories for the ease of their modeling and calibration. We call them ‘linear’ and ‘nonlinear’ modeling and calibration approach for the six-port junction.

3.6.1 Nonlinear Modeling of Six-Port Junction

We have already discussed the details of a nonlinear modeling and calibration approach for a SPR system. Here we intend to elaborate on the six-port junction circuitry suitable for nonlinear modeling and calibration for more insight and clarity. In the nonlinear modeling of the six-port junction, one of the four power detectors is chosen as a reference port detector. A six-port junction suitable for nonlinear calibration is designed in such a way that theoretically no power from the RF port reaches the reference port detector. The power reading from the reference port power detector is proportional to the LO power. In this model of the six-port junction power ratios from the other three detectors with respect to the reference port detector are used to obtain the in-phase component (I_{RF}) and the quadrature component (Q_{RF}) of the received communication signal. Figure 3.9(b) shows an implementation of the six-port junction suitable for nonlinear modeling and calibration.

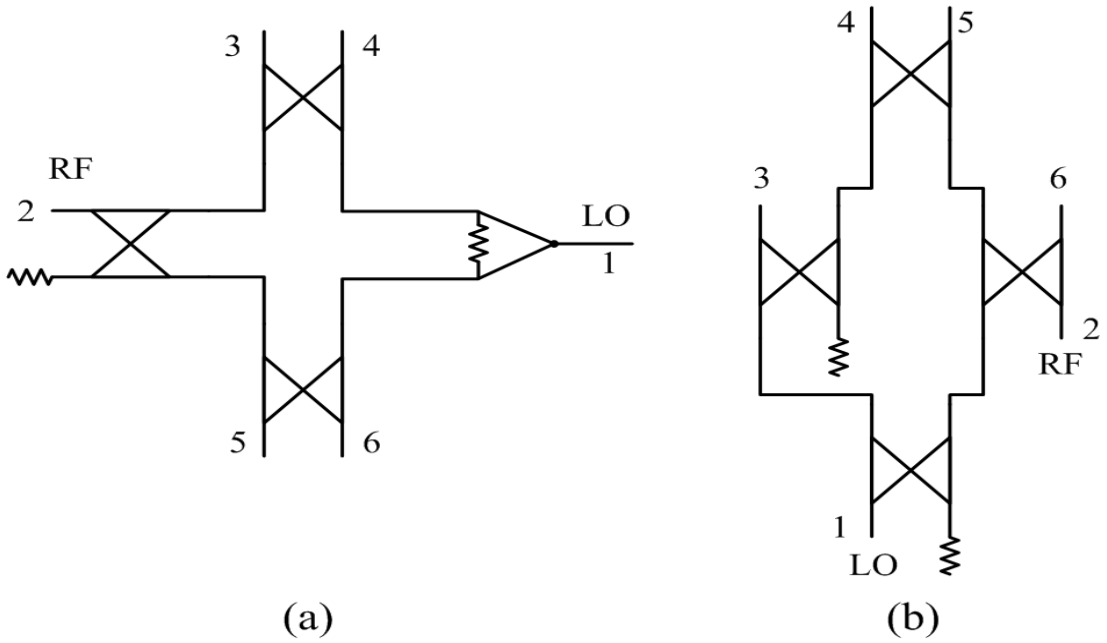


Figure 3.9: Implementation of the six-port junction suitable for (a) linear modeling and calibration (b) nonlinear modeling and calibration.

3.6.2 Linear Modeling of Six-Port Junction

In the linear model of six-port junction, the in-phase and the quadrature components of received communication signal is written as a linear combination of the four power readings from the power detectors. In this configuration of six-port junction, signification amount of powers from both the RF port and the LO port reach all the four power detectors. Figure 3.9(a) shows the implementation of a six-port junction using three quadrature hybrids and one Wilkinson power divider suitable for linear modeling and calibration. The details of the linear modeling and calibration for a six-port based receiver system are discussed in detail in the next chapter.

3.7 Conclusions

Theoretical analyses and measurement results are provided for a nonlinear modeling and calibration approach in the context of a six-port based direct down-conversion receiver. A new automatic nonlinear self-calibration method suitable for SPR systems is proposed in this chapter. The nonlinear calibration method makes use of a training sequence to auto-calibrate the system. It doesn't require any standard loads to be connected to the RF port of the receiver system. The calibration process of the receiver is divided into two steps: the receiver calibration and the phase alignment. The linearized power readings of the power detectors corresponding to thirteen different symbols are used to calculate the five real receiver calibration parameters. For phase alignment parameters calculation a training sequence of known symbols are added at the beginning of an actual test data burst. Three well-distributed symbols are chosen from the training sequence to extract three complex phase alignment parameters. An LUT based technique of diode-linearization is used for enhanced dynamic range of the receiver system. The whole process of diode linearization and receiver system calibration was verified on a real six-port based working receiver system with 4QAM and 16QAM signals having symbol rates up to

20MHz. The measurement results obtained during the system evaluation showed that the carrier-to-sideband noise ratio is better than 30dB. BER results were compared against the ideal system performance and found out to be satisfactory.

Chapter Four: **Linear Modeling and Calibration of Six-Port Receiver**

In chapter three of this thesis, we proposed a nonlinear modeling and calibration for the six-port based receiver system. We pointed out there that the nonlinear modeling and calibration approach become intractable if the nonlinearities and the memory effects of the diode detectors are included in the system modeling. The linear modeling and calibration approach for a six-port based receiver system simplifies this problem which is discussed in detail in this chapter.

4.1 Linear Modeling and Calibration of Six-Port Receiver

From equation (1.6), we know that the power detected by the kth power detector D_k is given by

$$P_k = |S_{k2}\boldsymbol{a_{RF}} + S_{k1}\boldsymbol{a_{LO}}|^2; k = 3,4, \dots ,6 \tag{4.1}$$

Equation (4.1) can be expanded and re-written in a matrix form as follows in equation (4.2).

$$\begin{bmatrix} P_3 \\ P_4 \\ P_5 \\ P_6 \end{bmatrix} = \begin{bmatrix} T_{31} & T_{32} & T_{33} & T_{34} \\ T_{41} & T_{42} & T_{43} & T_{44} \\ T_{51} & T_{52} & T_{53} & T_{54} \\ T_{61} & T_{62} & T_{63} & T_{64} \end{bmatrix} \begin{bmatrix} 1 \\ I_{RF}^2 + Q_{RF}^2 \\ I_{RF} \\ Q_{RF} \end{bmatrix} \tag{4.2}$$

where $T_{k1} = |S_{k1}|^2|a_{LO}|^2$,

$T_{k2} = |S_{k2}|^2$,

$T_{k3} = 2|S_{k1}||S_{k2}||a_{LO}|\cos(\angle S_{k2} - \angle S_{k1} - \emptyset_{LO})$, and

$T_{k4} = -2|S_{k1}||S_{k2}||a_{LO}|\sin(\angle S_{k2} - \angle S_{k1} - \emptyset_{LO})$ for $k = 3, \dots ,6$.

Matrix $[T]_{4\times4}$ in equation (4.2) is dependent only on the S −parameters of the six-port junction and the LO signal. From equation (4.2), I_{RF} and Q_{RF} can be written as a linear combination of $P_3, P_4, P_5,$ and P_6 by inverting $[T]$ as follows in equation (4.3).

$$I_{RF} = \sum_{k=3}^{6} \alpha_k P_k \tag{4.3a}$$

$$Q_{RF} = \sum_{k=3}^{6} \beta_k P_k \tag{4.3b}$$

Here α_k and β_k are the entries in the third and the fourth row of $[T]_{4\times4}^{-1}$ matrix, respectively.

These are constants for the SPR system dependent only on the S −parameters of the six-port junction and the LO signal. State-of-the-art linear calibration approach determines these eight calibration constants using a known training sequence and uses these determined calibration constants to receive an unknown RF signal.

If the training sequence consists of N samples then equation (4.3) can be written for the whole training sequence as follows in equation (4.4).

$$\begin{bmatrix} I^{(1)} & \dots & I^{(N)} \\ Q^{(1)} & \dots & Q^{(N)} \end{bmatrix} = \begin{bmatrix} \alpha_3 & \cdots & \alpha_6 \\ \beta_3 & \cdots & \beta_6 \end{bmatrix} \begin{bmatrix} P_3^{(1)} & \dots & P_3^{(N)} \\ \vdots & \vdots & \vdots \\ P_6^{(1)} & \dots & P_6^{(N)} \end{bmatrix} \tag{4.4}$$

Equation (4.4) is solved using the least square algorithm to get the eight linear calibration parameters (α_k and β_k). These parameters are used to estimate any future symbols according to equation (4.3).

4.2 Single Step Linearization and Calibration of Six-Port Receiver

It is obvious from equation (4.4) that it uses four powers readings ($P_3^{(n)}, \dots, P_6^{(n)}$) from the four detectors corresponding to the nth sample in the training sequence. The outputs from the power detectors are voltages which will be proportional to their corresponding input powers if the detectors are operating in their linear regions. In the linear region of the diode power detectors, the relationship between the input powers and the output voltages can be written as in equation (4.5),

$$P_i = k_i v_i, i = 3,4, \dots ,6 \tag{4.5}$$

where k_i is a parameter dependent on the characteristic of the ith power detector. In the linear regions of operations of the diode power detectors, equations (4.3) and (4.4) can be written directly in terms of the output voltages from the four detectors by changing the calibration

parameters from α_i and β_i to $\alpha_i' = \alpha_i k_i$ and $\beta_i' = \beta_i k_i$, respectively.

The linear dynamic range (region where the output voltage is proportional to the input microwave power) of the diode power detectors is quite limited and this limits the dynamic range of the whole receiver system. With the above formulation in equation (4.5) in terms of detector output voltages, the SPR system will result in error [increased Error Vector Magnitude (EVM)/Bit Error rate (BER)], if the detectors cross their linear regions of operations. To avoid this problem and to increase the dynamic range of the receiver system, the detectors must be allowed to operate beyond their linear ranges. In that case, equation (4.5) is not valid and a linearization technique must be used to linearize the diode detector characteristic. We have outlined a number of existing diode detector linearization techniques in chapter two of this thesis. The conventional diode linearization process and the receiver calibration process are two different steps. In the first step, the output voltages of the diode power detectors are used to linearize the diode detectors characteristics and obtain a linearized output power. The following stage is that of the receiver calibration, where the linearized detector powers are used to calibrate the SPR system using a linear or nonlinear calibration approach.

In the next section, we identify many other component and system imperfections which could degrade the overall SPR system performance. We develop an integrated black box model to take into account all the identified imperfections. Also, we propose a novel calibration approach for the SPR systems that compensates for all the identified system imperfections during the calibration step.

4.3 Practical Limitations of a Real Six-Port Based Receiver

A typical six-port based receiver system suitable for linear modeling and calibration is shown in Figure 4.1.

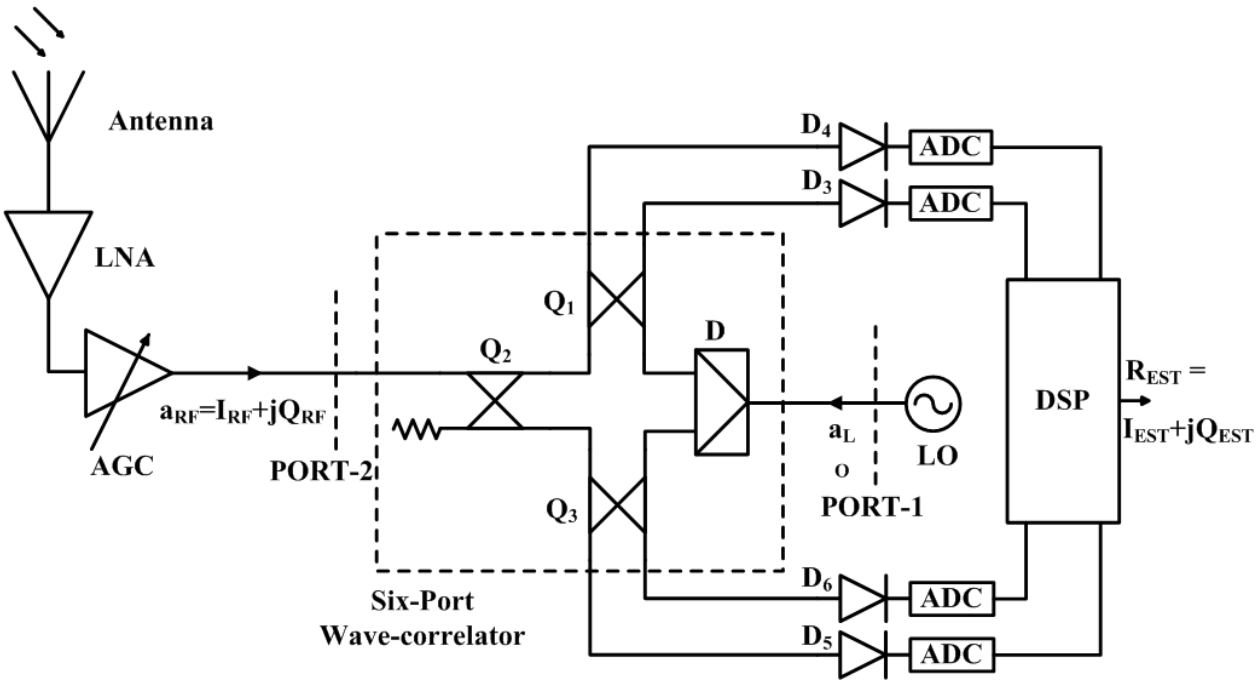


Figure 4.1: A typical six-port based receiver system architecture suitable for linear modeling and calibration.

SPR is an extension of the six-port based reflectometry technique where the reflection coefficient (Γ) of a device under test (DUT) is determined as a ratio of continuous wave (CW) reflected wave and CW excitation wave [24]. Behavior of the six-port wave-correlator circuit as well as those of power detectors change under a wideband modulated signal operation. A real SPR system needs to be calibrated before use in an actual communication system. A number of calibration approaches have been proposed in open literature [29]-[37], but none of these approaches takes into account all the actual limitations of SPR components and system when excited by a wideband modulated signal, such as:

a) Non-flat frequency response of the hybrids, power divider, connectors,

b) Unequal power divisions for the power dividers and hybrids,

c) Deviation of phase differences from ideal 90° for the hybrids in the whole band of operation,

d) Memory effects displayed by the diode power detectors as reported in [38], [39] and in this thesis, and

e) Nonlinearities of the diode power detectors.

In order to minimize the error in the demodulation process because of these system imperfections and bypass the calibration step, a recent approach for SPR technique consists of the design of quasi-ideal components used in the system [40]-[48] and limiting the operation of the whole receiver system to the square law regions of the diode detectors (where output voltage from the power detector is proportional to the input microwave power). This architecture employing quasi-ideal system components is shown in Figure 4.2. It consists of three quadrature hybrid couplers and a power divider all designed to match their ideal characteristics. Two voltage difference amplifiers are used to get back the baseband in-phase and quadrature components of the received signal as explained later in this section. While this architecture is simpler since no calibration is required, two main factors make it not practical for real applications. First, quasi-ideal performance can be guaranteed only for a limited bandwidth around the center frequency for which the six-port was designed. A change in the carrier frequency will result in a shift in performance. Second, the square law region where the output voltage of a diode detector is proportional to the input RF power is quite limited and this restricts the dynamic range of the whole receiver system. In [38], [39], and in this thesis it is observed that the behaviour of diode power detectors change under a wideband modulated wireless signal operation as compared to CW input signal, and the assumption of voltage-power proportionality is invalid even in the square law region of CW operation. In this thesis, all these system imperfections are acknowledged and a new formulation is deduced for the SPR system employing diode power detectors.

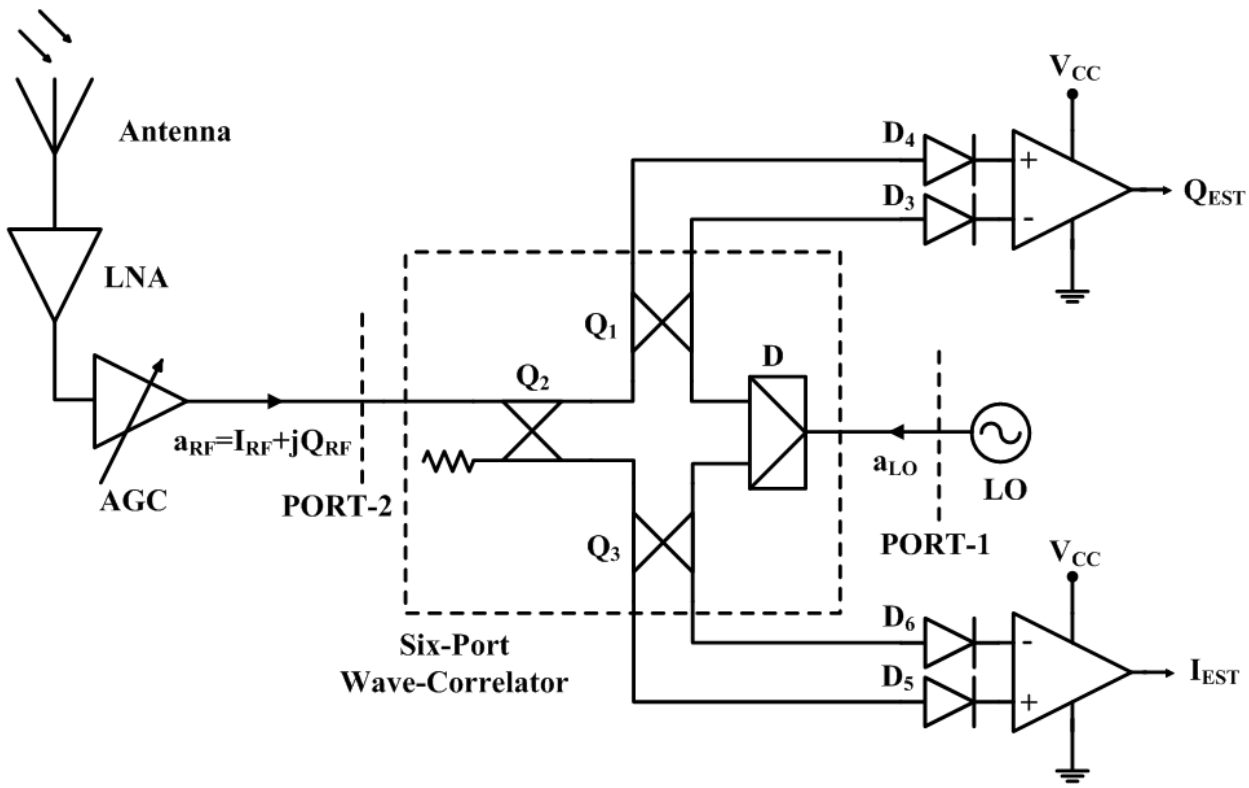


Figure 4.2: A typical six-port based receiver system architecture employing quasi-ideal system components.

A suitable calibration approach based on the developed mathematical modeling is proposed that corrects the above mentioned system impairments during the calibration process.

From equation (4.1), power difference between any two output ports from the SPR system can be expressed in terms of LO signal, RF signal, and the circuit parameters as in equation (4.6).

$$\begin{aligned} P_i - P_j = {} & \left(|S_{i1}|^2 - \left|S_{j1}\right|^2\right)|a_{LO}|^2 + \left(|S_{i2}|^2 - \left|S_{j2}\right|^2\right)(I_{RF}^2 + Q_{RF}^2) \\ & + 2I_{RF}|a_{LO}|\{|S_{i1}||S_{i2}|\cos(\angle S_{i2} - \angle S_{i1} - \emptyset_{LO}) \\ & - \left|S_{j1}\right|\left|S_{j2}\right|\cos\left(\angle S_{j2} - \angle S_{j1} - \emptyset_{LO}\right)\} \\ & - 2Q_{RF}|a_{LO}|\{|S_{i1}||S_{i2}|\sin(\angle S_{i2} - \angle S_{i1} - \emptyset_{LO}) \\ & - \left|S_{j1}\right|\left|S_{j2}\right|\sin\left(\angle S_{j2} - \angle S_{j1} - \emptyset_{LO}\right)\} \end{aligned} \tag{4.6}$$

For an SPR system architecture shown in Figure 4.3, the four power detectors output voltages can be used to get back the $Q_{RF}(I_{RF})$ from voltage difference $v_4 - v_3(v_5 - v_6)$ under the following assumptions valid for the whole bandwidth of the signal:

1) The power detectors D_3 and D_4 (D_5 and D_6) are operating within their square law regions i.e. $P_k = K_k v_k, k = 3,4$ ($P_k = K_k v_k, k = 5,6$) and their characteristics are identical i.e. $K_3 = K_4 = K_1 (K_5 = K_6 = K_2)$, and the performance of the six-port wave-correlator circuit is ideal (conditions 2)-5))
2) $|S_{41}| = |S_{31}| (|S_{61}| = |S_{51}|)$
3) $|S_{42}| = |S_{32}| (|S_{62}| = |S_{52}|)$
4) $\angle S_{41} = \angle S_{31} + 90^{\circ}$ and $\angle S_{32} = \angle S_{42} + 90^{\circ}$ ($\angle S_{51} = \angle S_{61} + 90^{\circ}$ and $\angle S_{62} = \angle S_{52} + 90^{\circ}$)
5) $\angle S_{42} - \angle S_{31} - \emptyset_{LO} = 2n\pi, n = 0,1,2, \ldots$($\angle S_{52} - \angle S_{61} - \emptyset_{LO} = \left(2n + \frac{1}{2}\right)\pi, n = 0,1,2, \ldots$)

If the above conditions 1)-5) are satisfied, and if A_I and A_Q are the gain of the differential amplifiers in the in-phase and the quadrature component recovery path, respectively, then the estimated values of the in-phase and the quadrature components in the received symbol are given by equation (4.7).

$$I_{EST} = \frac{A_I K_2 (v_5 - v_6)}{4|S_{51}||S_{52}||a_{LO}|} \tag{4.7a}$$

$$Q_{EST} = \frac{A_Q K_1 (v_4 - v_3)}{4|S_{31}||S_{32}||a_{LO}|} \tag{4.7b}$$

We observe from equation (4.7) that the estimated I and Q components are proportional to the voltage differences $v_5 - v_6$ and $v_4 - v_3$, respectively. If the proportionality constants

$\frac{A_I K_2}{4|S_{51}||S_{52}||a_{LO}|}$ and $\frac{A_Q K_1}{4|S_{31}||S_{32}||a_{LO}|}$ are not equal for the whole bandwidth of the signal, it will result in gain and phase imbalance in the received symbols (compression/expansion and rotation in the received constellation points with respect to the transmitted constellation). This additional source of error may be caused due to non-identical and non-flat gain of the difference amplifiers, different behaviors of the power detectors in their square law region, and non-identical and non-flat frequency responses of the hybrids and the power divider in the whole frequency band of operation.

Assumptions 1)-5) are very stringent to meet for any real system, especially when the bandwidth of operation is large. Let us analyze the behavior of a SPR system when these assumptions are not satisfied by a real implementation of the system concept. Failure of assumption 1) for the real implemented system causes nonlinear distortion and smearing in the constellation of received symbols because of non-linearity and memory effect (frequency response) of the diode detectors. Failure of assumption 2) results in DC-offset and that of 3) introduces additional smearing around a symbol point in the received constellation. If assumption 4) is not satisfied by the actual implementation of the SPR system, it results in diminished peak-to-peak value for the recovered I and Q signals and can also cause gain imbalance in the received constellation. Though assumption 5) may be met by shifting the reference plane 1(imaginary theoretical plane) at PORT-1 for the LO signal in some cases, effect of its failure is quite expensive for the overall system performance as demonstrated by the improved overall system performance in [26]. Failure of assumption 5) causes cross-talk between I_{RF} and Q_{RF}, and its effect can't be mitigated without calibration and further processing of the received symbols.

4.4 Black Box Modeling of Six-Port Receiver

As explained in equation (4.3), calibration constants α_k and β_k for the linear calibration approach are dependent on the S −parameters of the six-port junction, which are frequency dependent parameters. An attempt has been made in [30] to model this frequency dependent behavior of the calibration parameters. The bandwidth of the received signal is sub-divided into multiple sub-bands and separate calibration parameters are calculated for each of the individual sub-bands. The estimated I and Q components for each sub-band are summed-up to get I and Q components for the whole received RF signal. In order to get the optimum performance from a real SPR system, apart from the frequency dependent behaviours of the S −parameters of the six-port junction and in turn the frequency dependent behavior of the calibration constants, other system imperfections must also be modeled and accounted for through a suitable calibration.

4.4.1 Modeling Diode Detector Nonlinearity and Memory Effect

To increase the dynamic range of the receiver system, the diode power detectors must be operated beyond their square law regions. Even in their square law regions, the linear relationship of output voltage and input power is not valid when excited with a modulated wireless signal. The non-linearity and memory effect for the diode detectors is modeled in this thesis using a modified memory polynomial as explained in chapter two. The equation governing this relationship between the input microwave power to the kth diode detector, $P_{in,k}[n]$ and the output voltage of the detector, $v_k[n]$ at any instant of time is given by equation (4.8).

$$P_{in,k}[n] = \sum_{q=0}^{M_k} \sum_{p=1}^{N_k} c_{pqk} v_k^p[n-q] \tag{4.8}$$

Here c_{pqk} are the coefficients of the above memory polynomial, and N_k and M_k are non-linearity order and memory depth for the diode detector D_k, respectively.

4.4.2 Modeling Frequency Response of Six-Port Junction

Frequency dependent six-port junction behavior is modeled by an 'ideal' six-port junction followed by an element approximating the frequency dependent behavior of six-port junction as shown in Figure 4.3.

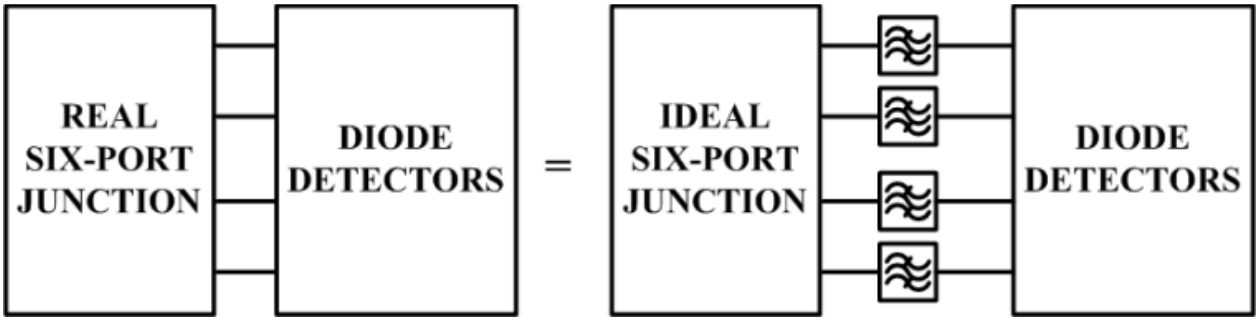


Figure 4.3: Modeling the frequency response of the six-port junction.

The model of the diode detectors as developed in equation (4.8) models the frequency dependent behavior (memory effect) of the power detector; it will also model the combined frequency dependent behavior of the element modeling six-port frequency response as well as the diode power detector. Thus, the model of the diode detectors as developed in equation (4.8) accounts for the frequency dependent behavior of the six-port junction as well as the nonlinearities and the memory effects displayed by the diode detectors.

In practice, the behaviors of the commercially available diode detectors are not exactly identical due to the fabrication process variations. It is not practical to take out each detector from the receiver system for modeling and linearization or an extra step for linearization apart from the system calibration may not be feasible in practical cases. Even if the modeling for diode detectors is done outside the system, it will not be optimum when put into the system. An *in-situ* model for the detectors is therefore highly desired. In the next sub-section a black-box model for the whole SPR system is developed that will allow a single step calibration for all the limitations

as well linearization of all the diode detectors. In the black-box model and the calibration approach developed in the next sub-section, linearization of the diode detectors is a part of the system calibration and both are combined to form a single step process rather than two as done for the linearization of diode detectors and the calibration of six-port in network analyzer applications [49].

4.4.3 Black-Box Model for Complete SPR System

Models of the diode detectors and the six-port junction developed in equation (4.8) are applied to equation (4.3) to correct for the diode nonlinearity, its memory effects, and the frequency response of the six-port junction, which the model in equation (4.3) failed to account for. The resulting expressions for the estimated values of the I and Q components in this case can be written as given in equation (4.9).

$$I_{EST}[n] = \sum_{k=3}^{6} \sum_{q=0}^{M_k} \sum_{p=1}^{N_k} x_{pqk} v_k^p[n-q] \tag{4.9a}$$

$$Q_{EST}[n] = \sum_{k=3}^{6} \sum_{q=0}^{M_k} \sum_{p=1}^{N_k} y_{pqk} v_k^p[n-q] \tag{4.9b}$$

Here x_{pqk} and y_{pqk} are real constants for the receiver system depending on the LO signal, properties of the six-port junction and the diode power detectors. For simpler expression and convenience, (4.9a) and (4.9b) can be combined to estimate the received symbol $R_{EST} = I_{EST} + jQ_{EST}$.

$$R_{EST}[n] = \sum_{k=3}^{6} \sum_{q=0}^{M_k} \sum_{p=1}^{N_k} c_{pqk} v_k^p[n-q] \tag{4.10}$$

Equation (4.10) provides the definitive model of a SPR system, which relates the output voltages of the diode power detectors directly to the estimated transmitted symbol. Here $c_{pqk} = x_{pqk} + jy_{pqk}$ are the complex constants for the overall receiver system to be determined using a suitable calibration means. These complex calibration constants are dependent on the properties of the

six-port junction, the diode detectors and the LO signal. The model for an SPR system as developed in equation (4.10) is not restricted only to the square law region of the diode detectors. It opens up the limitations on the range of operation of diode detectors from their minimum sensitivity level to their maximum power handling capability. Hence this model increases the dynamic range of the whole receiver system. Diode detectors nonlinearities and their memory effects are part of the model and so the linearization step becomes part of the calibration process as the model in equation (4.10) deals directly with the output voltages of the diode power detectors. The frequency response of the six-port junction is also a part of the model in equation (4.10). Problems of DC-offset, smearing of the received constellation points, cross-talk between I and Q components and the reduced peak-to-peak amplitudes of the I and Q signals due to circuit imperfections are also resolved as the sources of these errors are part of the model in equation (4.10). The developed model in equation (4.10) for a SPR system is summarized in Figure 4.4. Inputs to the model are four output voltages $(v_3, v_4, \dots, v_6)$ of the diode detectors and the output from the model is received symbol $R_{EST} = I_{EST} + jQ_{EST}$, an estimation of the original transmitted symbol $I_{RF} + jQ_{RF}$. This developed model for the SPR system must be trained or calibrated before use in a real communication environment. This calibration step involves determining the model parameters for the SPR system model. We next describe the calibration procedure of a SPR system based on the model developed in this section.

4.5 Calibration Procedure

The calibration process for the SPR system modeled in the way described in Section 4.4 involves determining the model parameters $c_{pqk}; p = 1, \dots, N_k; q = 0, \dots, M_k; k = 3, .,6$ that relate the output voltages v_k from the diode power detectors straight to an estimate R_{EST} of the original transmitted symbol $R = I_{RF} + jQ_{RF}$ through equation (4.10). The calibration step makes use of a

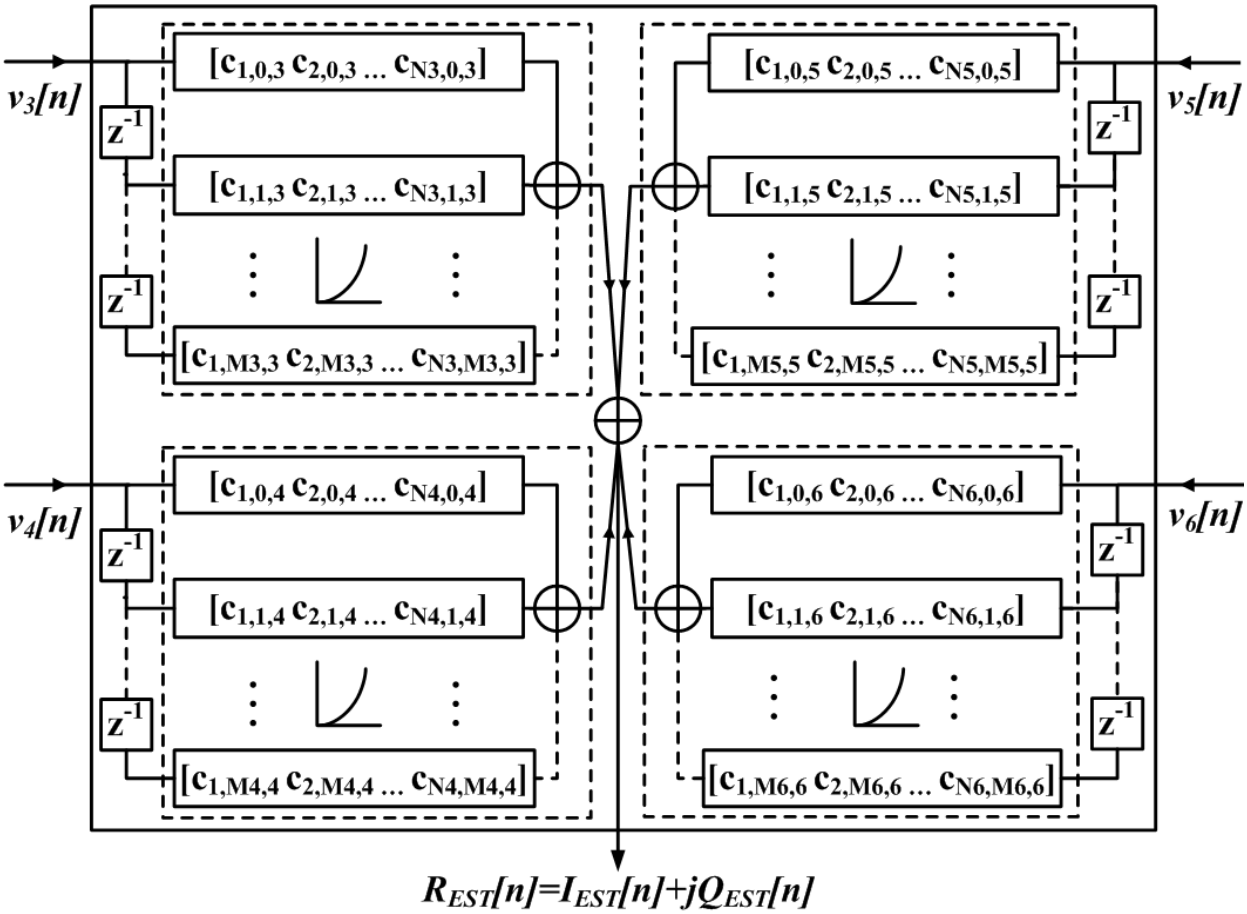


Figure 4.4: Proposed model for a SPR system taking into account all the identified system impairments.

known training sequence inserted at the beginning of an actual test data burst to determine the calibration parameters. Though the characteristics of the diode detectors used in the SPR system are not exactly the same in practice, the non-linearity order and memory depth for the four detectors are taken to be equal to simplify the calibration procedure. The variations in their characteristics will be captured by different calibration parameters corresponding to each diode detector. The system model after this simplification can be written as in equation (4.11).

$$R_{EST}[n] = \sum_{k=3}^{6} \sum_{q=0}^{M} \sum_{p=1}^{N} c_{pqk} v_k^p[n-q] \tag{4.11}$$

Note that in equation (4.11), the non-linearity order and memory depth are chosen to be the same for all the four diode detectors. Indeed, while the diodes may be slightly different, the order of magnitudes of their distortion and memory effect are about the same. In order to determine the calibration parameters, a string of K known symbols is sent before sending an actual test data. If $S[n]; n = 0,1, \dots, K-1$ is the nth known sent symbol and $v_k[n]$ is the corresponding output voltage from the diode detector $D_k, k = 3,4,5,$ and 6, then a calibration equation for the SPR system can be written as in equation (4.12).

$$R_{EST}[n] = \boldsymbol{V}^T[n]\boldsymbol{C} \tag{4.12}$$

where $\boldsymbol{C}^T = [c_{103} \quad \cdots \quad c_{N03} \quad c_{113} \quad \cdots \quad c_{N13} \quad \cdots \quad c_{1M3} \quad \cdots \quad c_{NM3} \quad \cdots \quad c_{1M6} \quad \cdots \quad c_{NM6}]$,

and

$$\boldsymbol{V}^T[n] = \begin{matrix} [v_3[n] & \cdots & v_3^N[n] & v_3[n-1] & \cdots & v_3^N[n-1] \\ \cdots & v_3[n-M] & \cdots & v_3^N[n-M] & \cdots & v_6[n-M] & \cdots & v_6^N[n-M]] \end{matrix}$$

In equation (4.12) vector $\boldsymbol{C}$ (of size $4[M+1]N \times 1$) is the calibration parameters vector determined during this calibration step. Equation (4.12) is solved for $\boldsymbol{C}$ using the least square algorithm as explained in chapter two. Once $\boldsymbol{C}$ is calculated in this manner, it is used to estimate any received symbols using equation (4.12).

To assess the performance of the calibration procedure, a performance metric in terms of error vector magnitude (EVM) is used to compare the estimated symbols with the original transmitted symbols. EVM between the estimated symbols (R_{EST}) and the corresponding ideal transmitted symbols (S_{TMT}) is defined [50] as in equation (4.13).

$$EVM = \sqrt{\frac{\frac{1}{K}\sum_{n=1}^{K}|R_{EST}[n] - S_{TMT}[n]|^2}{\frac{1}{K}\sum_{n=1}^{K}|S_{TMT}[n]|^2}} \times 100\ \% \tag{4.13}$$

In order to determine the optimal calibration parameters, the memory depth M and the non-linearity order N are varied and the corresponding EVMs are recorded. The (M, N) pair having the least acceptable EVM is fixed for the system and the corresponding calibration parameters vector $\boldsymbol{C}$ obtained in this communication environment is used to estimate all the future symbols. Once M, N and $\boldsymbol{C}$ are decided for the system, any future n^{th}received symbol is estimated according to equation (4.12).

4.6 Implementation of SPR system

The architecture of the SPR system is configured and implemented as shown in Figure 4.1. Implementation of the complete set-up for the SPR system test-bench is shown is Figure 4.5. In the test-bench set-up shown in Figure 4.5, the baseband I/Q data is generated on a desktop PC in MATLAB. This baseband data is raised cosine filtered before passing to a I/Q modulation generator (AMIQ from Rhode & Schwarz GmbH & Co.). The I/Q modulated baseband data is then frequency up-converted to a desired carrier frequency using a SMIQ 03B vector signal generator from Rhode & Schwarz. The LO signal at the carrier frequency is supplied by a PSG CW Signal Generator (E8247C from Agilent Technologies). Voltages generated by the Schottky diode detectors are captured using two synchronized dual-channel VSAs (89600 series VSA from Agilent Technologies). The captured voltages are further processed in MATLAB to get an estimate of the received symbol as explained in Section 4.5.

4.7 Measurement Results

In order to evaluate the performance of the proposed calibration procedure, 2500 random 64QAM symbols are generated in MATLAB. The first 100 symbols are treated as a training sequence and are used to calibrate the SPR system. This test packet of 2500 symbols is passed through a raised cosine filter of roll-off factor 0.3 (up-sampled by 8) and a delay of 3 taps. This

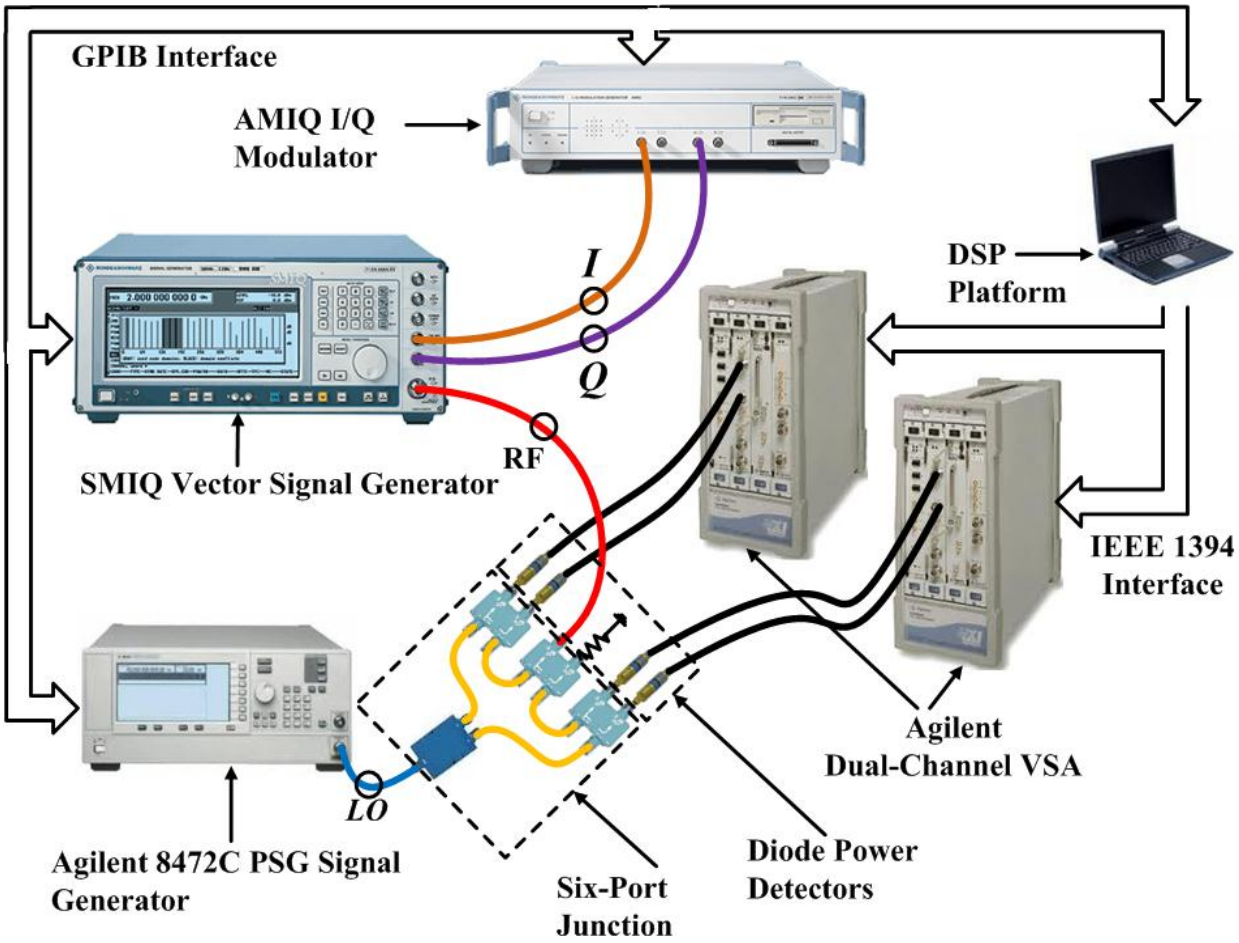


Figure 4.5: Complete test set-up for wideband six-port based communication receiver.

pulse shaped signal is I/Q modulated and frequency up-converted to a desired carrier frequency to simulate an actual RF modulated received signal. This I/Q modulated passband data is fed to the RF port (PORT-2) of the SPR system. LO power is set to be 12dBm and the mean RF power is set to be 7dBm (peak power = 11.5dBm). Voltages generated by the four power detectors are used to calibrate the whole SPR system as explained in Section 4.5. The calibrated system is used to receive the symbols in an actual test data burst. The measurement results obtained for 64QAM signals at a carrier frequency of 2.5GHz are shown in Figures 4.6 and 4.7. Figures 4.8 and 4.9 show the comparison of the constellation points of the transmitted and the received

signals when the diode detectors are linearized using conventional CW linearization approach at a carrier frequency of 2.5 GHz and when the SPR system is calibrated according to the proposed approach. The calibration of the SPR system using the conventional approach is governed by equation (4.3). Here, only the power detectors nonlinearities are modeled using CW approach at the carrier frequency and the detectors memory and frequency response of six-port are not accounted for. The comparison results of the conventional two steps process of diode detector linearization and six-port calibration with the proposed single step wideband linearization and calibration for the SPR system is provided in Table 4.1.

Table 4.1: Comparison of conventional and proposed calibration approach

Signal Type	EVM (%)	
	Conventional Method	Proposed Method
64-QAM 2 MHz BW	7.93	1.66
64-QAM 4 MHz BW	16.04	2.81

Figure 4.10 shows the demodulation results obtained for WCDMA signal at carrier frequencies of 2.14 GHz. Figure 4.11 shows the transmitted and the received I/Q components and spectrums for a WLAN signal at carrier frequencies of 2.4 GHz.

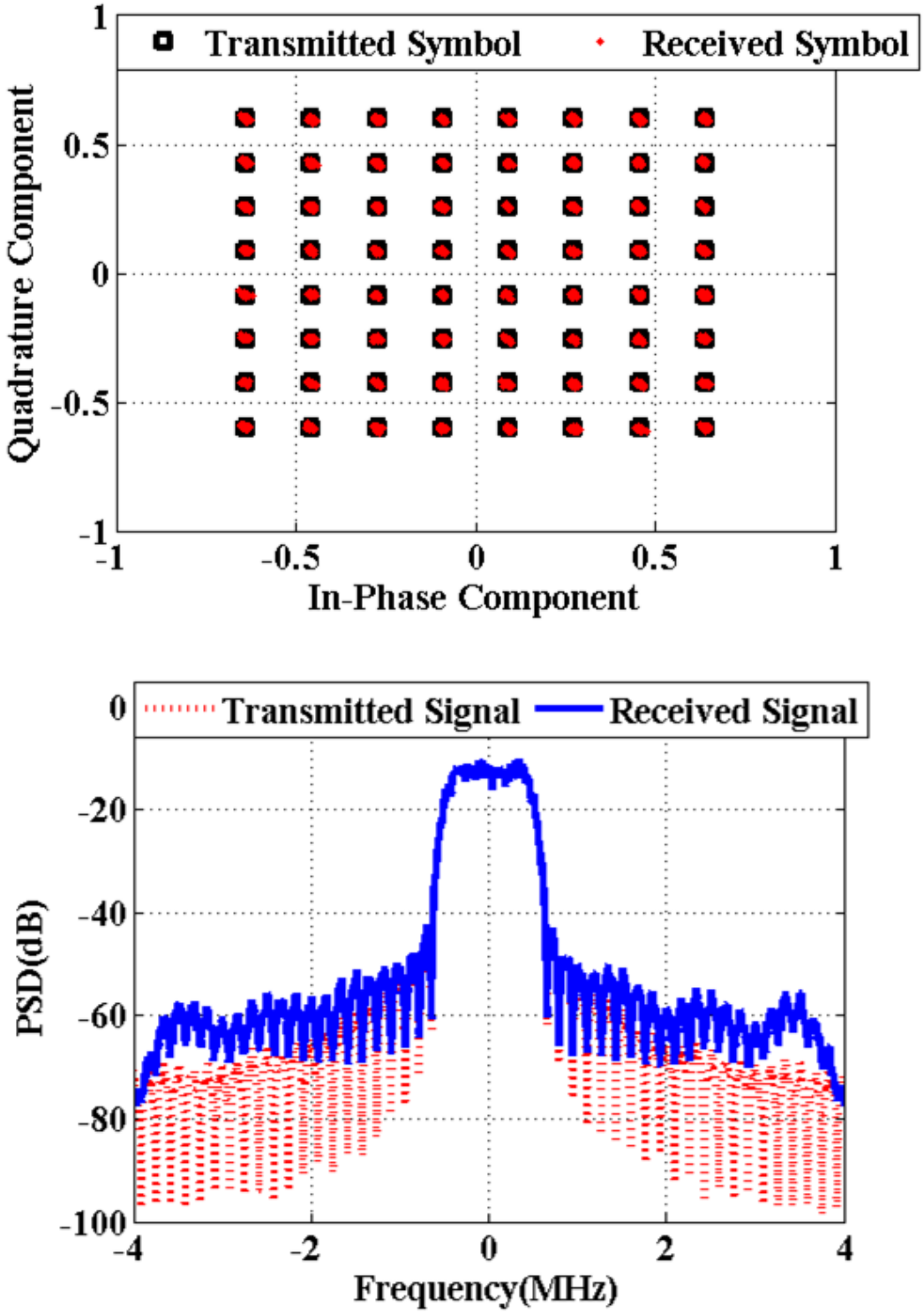


Figure 4.6: Constellations (Top) and spectrums (Bottom) of received and transmitted symbols for 64-QAM signals having 1MHz bandwidths [6Mb/s].

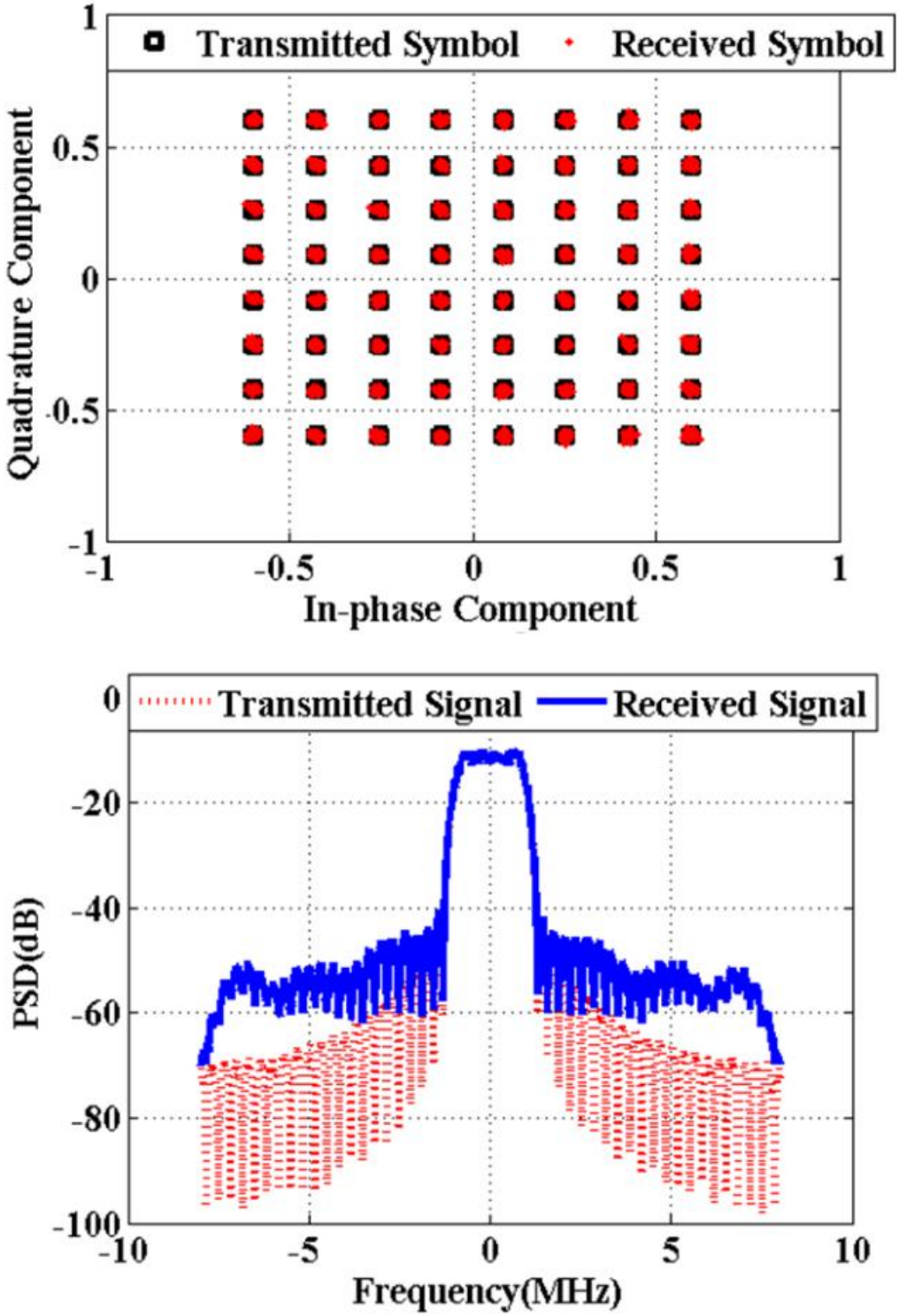


Figure 4.7: Constellations (Top) and spectrums (Bottom) of received and transmitted symbols for 64-QAM signals having 2MHz bandwidths [12Mb/s].

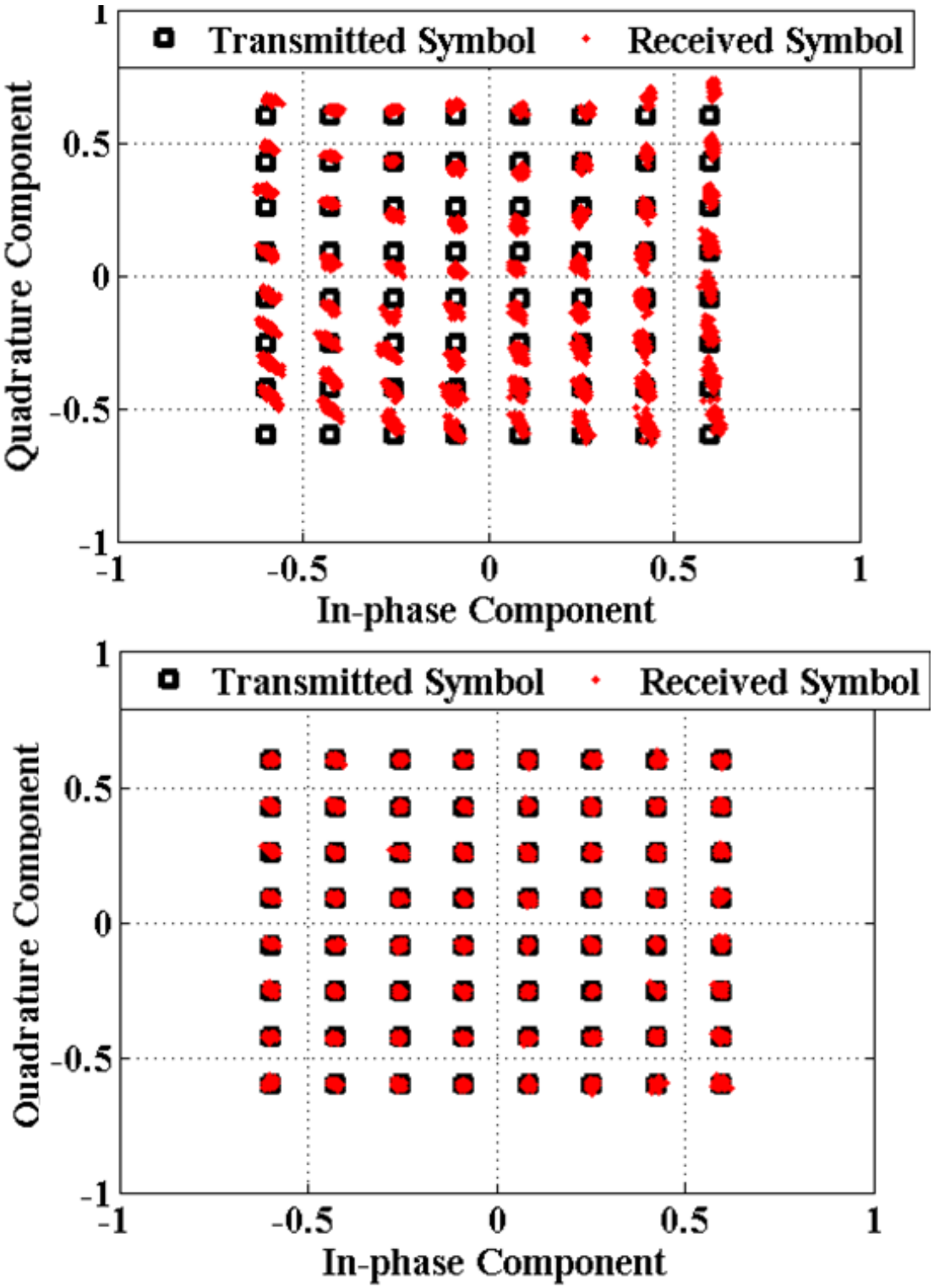


Figure 4.8: Constellations of 64-QAM modulated transmitted and received symbols having 2MHz bandwidths; Conventional Approach (Top), Proposed Approach (Bottom).

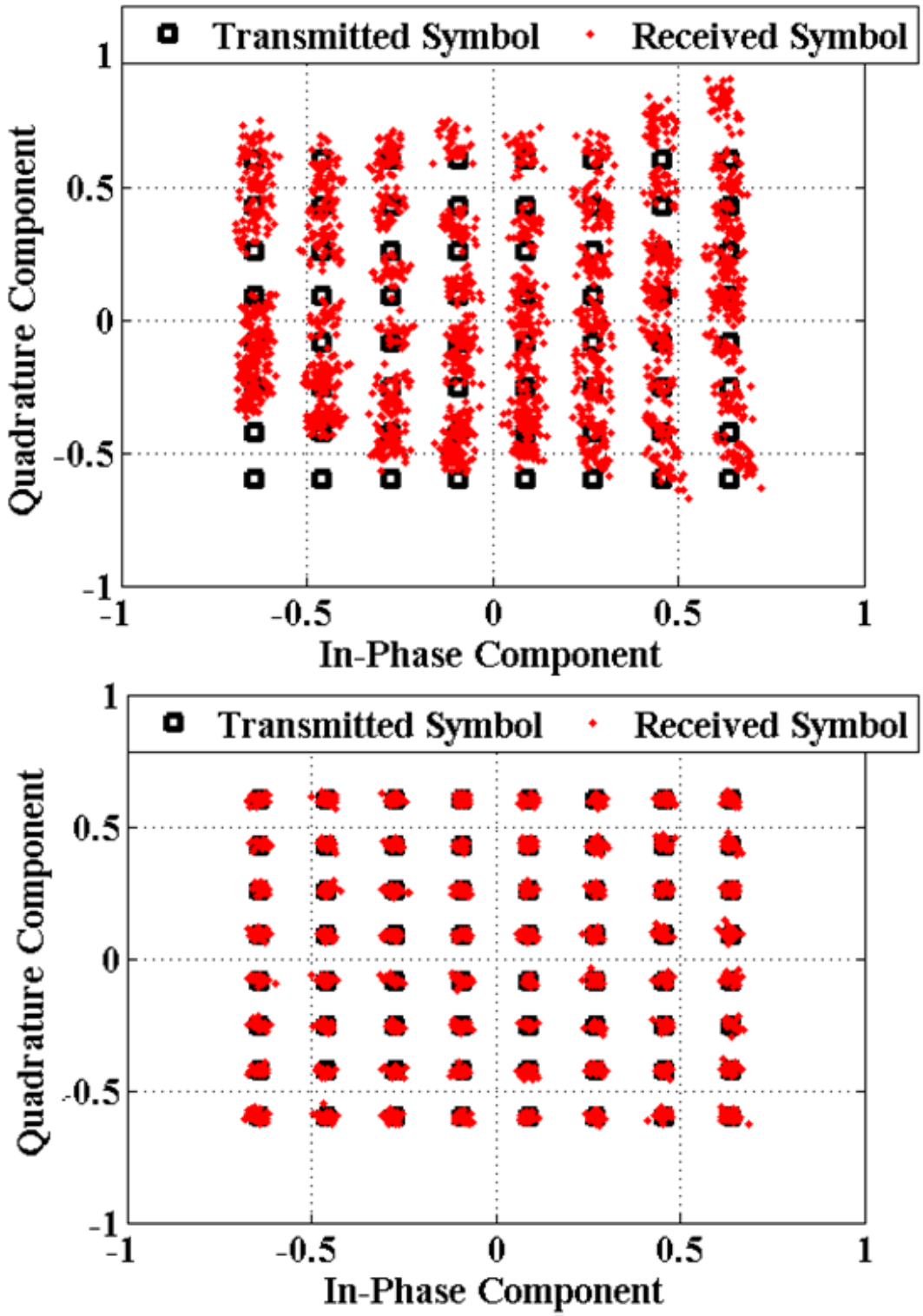


Figure 4.9: Constellations of 64-QAM modulated transmitted and received symbols having 4MHz bandwidths; Conventional Approach (Top), Proposed Approach (Bottom).

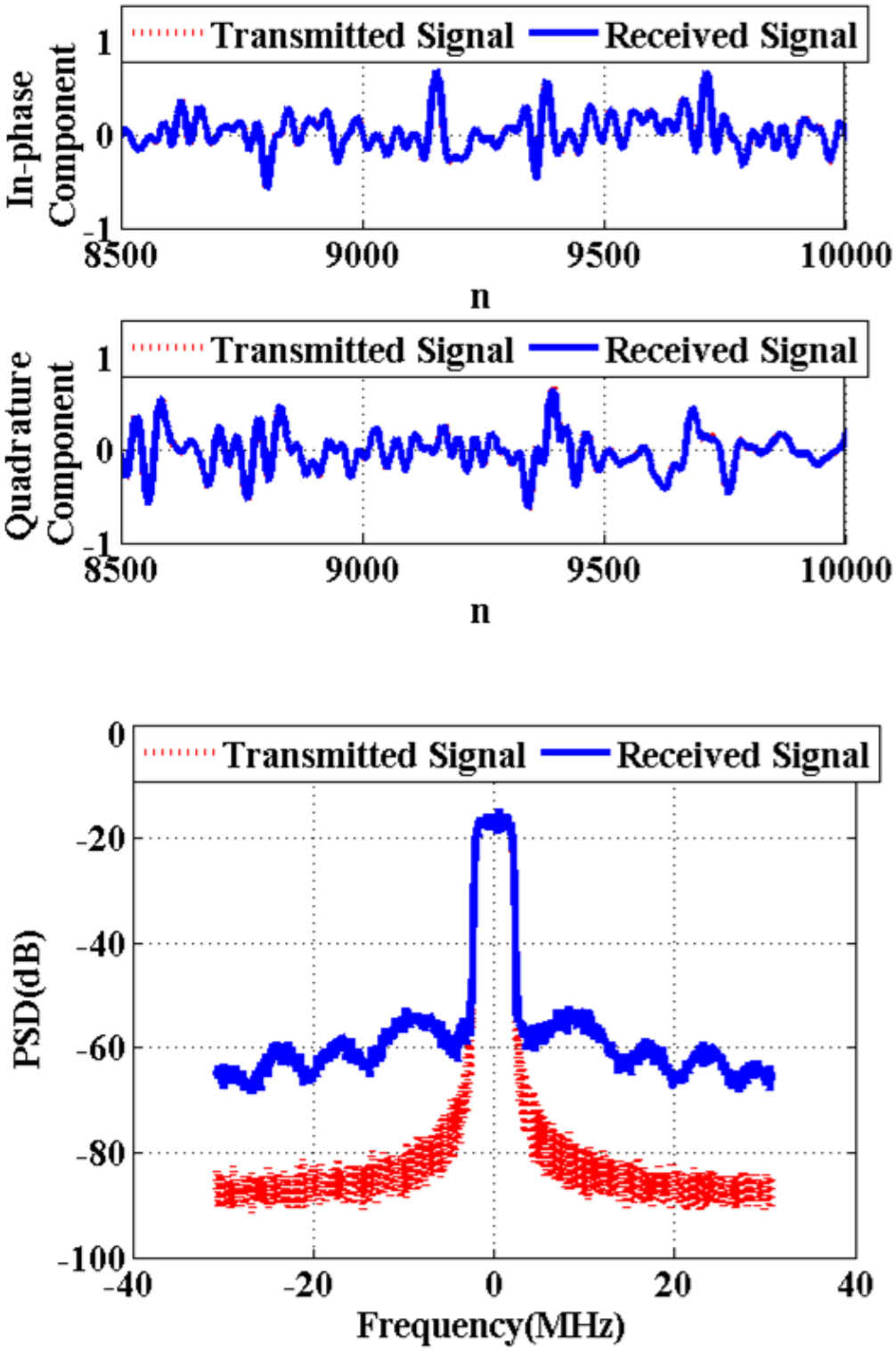


Figure 4.10: Transmitted and received I/Q components (Top) and frequency spectrums (Bottom) of WCDMA signal.

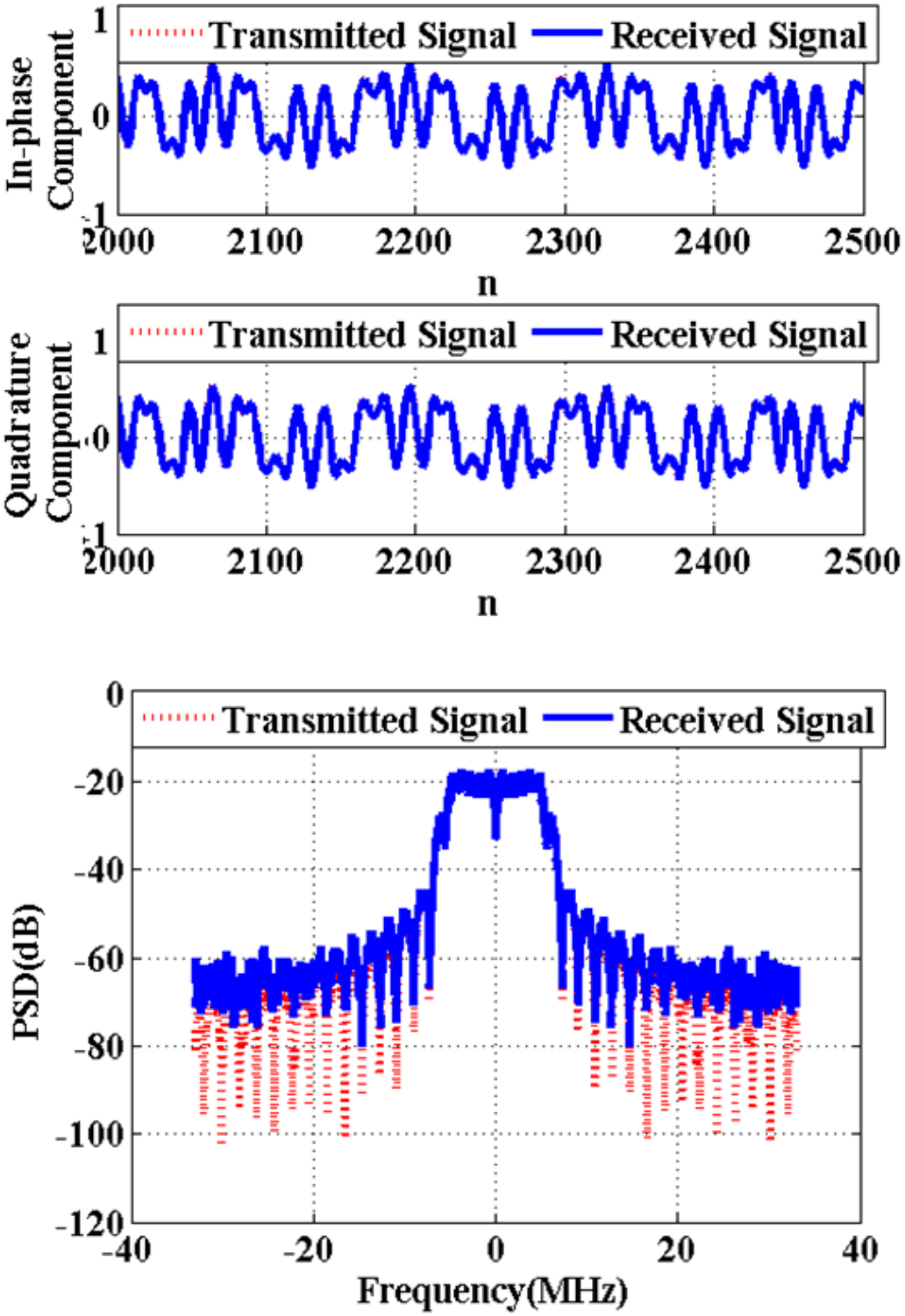


Figure 4.11: Transmitted and received I/Q components (Top) and frequency spectrums (Bottom) of WLAN signal.

The results obtained from the system for different types of signals at different carrier frequencies having different bandwidths are summarized in Table 4.2.

Table 4.2: SPR system performance summary

Signal Type	Signal BW	Carrier Frequency	M	N	Performance (EVM, %)
64-QAM	1.00 MHz	2.50 GHz	9	3	1.17@6Mb/s
64-QAM	2.00 MHz	2.50 GHz	9	3	1.66@12Mb/s
WCDMA	5.00 MHz	2.14 GHz	9	3	4.70
WLAN	10.0 MHz	2.40 GHz	9	3	3.43

In all the test cases, satisfactory results are obtained and the comparison with the recent works is provided in Table 4.3.

Table 4.3: Comparison with recent reported works

Ref.	A*	B*	C*	D*	E*	Performance (EVM)
[1] 2011	No	No	No	Yes	8	10.9% @1.67Gb/s [16-QAM]
[2] 2011	No	No	Yes	Yes	8	4.5% @93.75Mb/s [64-QAM]
[6] 2010	No	No	No	Yes	-	5.9% @400 kb/s [QPSK]
This work	Yes	Yes	Yes	Yes	12	1.17% @6Mb/s [64-QAM] 1.66% @12Mb/s [64-QAM] 2.88% @24Mb/s [64-QAM]

*A: Detector Nonlinearity, B: Detector Memory Effect, C: Frequency Response of the Six-Port Junction, D: I/Q cross-talk, E: ADC bit-size.

4.7.1 Measurement Limitations

The diode power detectors used in the test set-up have typical rise times of about 6 to 12ns [51]. This limits the usable bandwidth of the power detector and thus the bandwidth of the signal which can be faithfully recovered with the SPR system test set-up. The relationship between x-dB bandwidth and rise time [52] can be approximated by equation (4.14).

$$BW_{x-dB} \approx \frac{\ln(9)\sqrt{10^{x/10}-1}}{2\pi t_{rise}} \tag{4.14}$$

3dB bandwidth and 0.1dB bandwidth of the used diode detector are limited to 29MHz and 4.4MHz respectively. When signals having very high bandwidths are demodulated with system using slow power detectors, it causes additional error in the EVM. This problem can be solved by using faster diode detectors having much smaller rise times for high bandwidth signals. Another limitation for the test set-up, which restricts the data rate of SPR system is the sampling frequency of VSAs used to capture analog voltages generated by the power detectors. If high data rates are targeted from the SPR system then Analog-to-Digital (ADC) components having higher sampling rates must be used in the system.

4.8 Conclusions

The suitability of linear modeling and calibration approaches for different real communication signals is highlighted in this chapter. Effects of deviations of multi-port receiver system and components from their ideal behaviors are studied, and a new model for the SPR system, that takes into account these limitations posed by the real system and components, is developed in this chapter. An appropriate calibration method is proposed to correct these system impairments and the overall system performance is improved. Usefulness of the model and the calibration approach is verified by demodulating 64QAM signals up to 24 Mb/s bit rate. WCDMA and

WLAN signals are demodulated and the obtained results are reported to show its usefulness for the real communication systems. The proposed linearization and calibration algorithm allowed reducing the EVM from 7.93% to 1.6% and from 16.04% to 2.81% for 64QAM signals having 2MHz and 4MHz Bandwidths, respectively at a carrier frequency of 2.5 GHz.

Chapter Five: **Conclusions and Future Works**

The ideal requirements from a typical software defined radio receiver are highlighted and various practical implementations of this concept are studied in brief. The homodyne or the zero-IF receiver architecture is found out to be realistic and practical solution for SDR receiver applications. An alternative architecture for homodyne receiver based on six-port technique is explored and it's suitability for the SDR application is studied in this thesis. The RF front-end of a typical six-port based receiver system comprises a passive and linear six-port circuit that can be easily designed to cover a very wide frequency bandwidth. Wide bandwidth coverage is a fundamental requirement from SDR system and components. Apart from a wideband six-port junction circuitry, a typical six-port based receiver system uses four microwave power detectors that too can be designed to cover a very wide bandwidth. Six-port junction for the receiver system is formed using equal power dividers and quadrature hybrids. The magnitude and the phase response of these system components deviate from their ideal behaviours and that causes performance degradation of the whole receiver system. Also the diode power detectors used in the six-port based receiver systems display memory effect for wideband modulated signal applications that must be modeled to improve the overall receiver performance. In this thesis we have proposed a new linearization technique to linearize the diode power detector characteristics for wideband signals that increases the dynamic range of the diode power detectors from their minimum sensitivity level to their maximum power handling capability. We have used this detector model to develop a novel model for the complete six-port based receiver system taking into account all the identified system and component imperfections. A suitable calibration technique is proposed to account for the identified impairments and the overall system performance is improved. Usefulness of the model and the calibration approach is verified by

demodulating 64QAM signals up to 24 Mb/s bit rate. WCDMA and WLAN signals are demodulated and the obtained results are reported to show its usefulness for the real communication systems. The proposed linearization and calibration algorithm allowed reducing the EVM from 7.93% to 1.6% and from 16.04% to 2.81% for 64QAM signals having 2MHz and 4MHz Bandwidths, respectively at a carrier frequency of 2.5GHz. Table 5.1 summarizes the conventional linear, and the proposed linear and the nonlinear modeling and calibration approaches for six-port based receiver system studied in this thesis.

Table 5.1: Summary of the conventional linear, and the proposed linear and the nonlinear modeling and calibration approaches

Conventional Linear Approach	Proposed Nonlinear Approach	Proposed Linear Approach
Two-step process	Two-step process	One-step process
8 calibration parameters, 24 detector linearizer parameters	11 calibration parameters, 24 detector linearizer parameters	Total 144 parameters
Calibration parameters dependent on the LO power level, independent of RF signal	Receiver calibration step (one-time process) independent of LO and RF power levels	Calibration parameters dependent on the LO power level, also on the RF signal
Fails to model frequency response of six-port, memory effect of diode detectors	Fails to model frequency response of six-port, memory effect of diode detectors	Models the frequency response of six-port, memory effect of diode detectors
Complexity Level: ++	Complexity Level: +++	Complexity Level: ++
Performance: ++	Performance: ++	Performance: ++++
Robustness: +++	Robustness: ++	Robustness: ++++

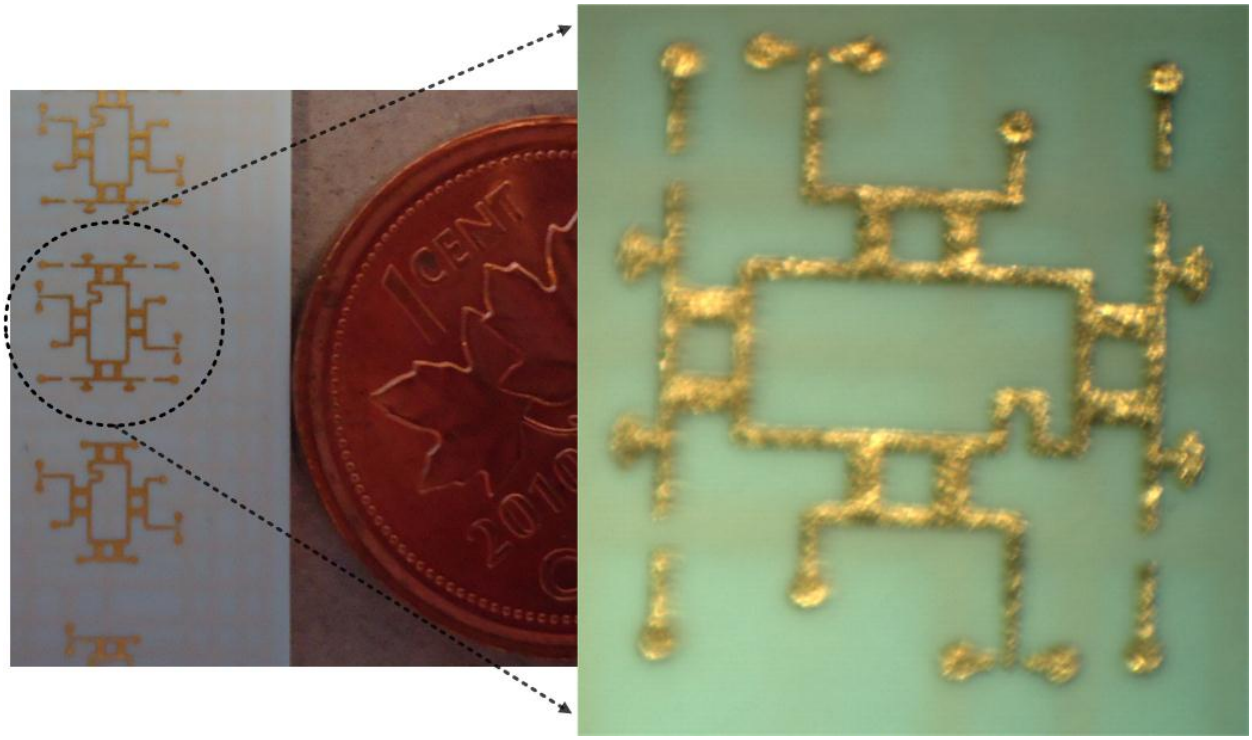


Figure 5.1: Six-port based receiver RF front-end circuit designed in LTCC technology for 60 GHz applications.

5.1 Future Works

The current test set-up to validate the proposed calibration algorithm uses off-the-shelf microwave circuit components covering a frequency band of 2-18GHz that makes the overall system size larger in space. A six-port circuit for 60GHz band operation comprising of one 90° phase shifter and four quadrature hybrids along with the four power detectors has been designed in low temperature co-fired ceramic (LTCC) technology for higher integration and smaller size. Figure 5.1 shows the complete receiver front-end circuit designed in LTCC technology for 60 GHz applications. The input and the output matching network have been optimized for 60GHz band and maximum bandwidth signal operation, respectively. The design of the complete RF front end circuit in the LTCC technology provides multi-layer integration and smaller footprint

for chip size packaging. The future work would include the design of the complete receiver RF front end circuit in LTCC or other suitable technology (GaN/MMIC/MHMIC) for integration in a smaller chip size package. This future design should explore the option of on chip adaptive antenna array for integration with the above six-port based homodyne receiver. It should include the digitally controlled on chip frequency synthesizer for channel selection. The complete RF front end circuit consisting of the adaptive antenna array,

six-port junction, diode detectors with their input and output matching circuits, and the digitally controlled frequency synthesizer should be integrated in a single package with a minimum number of package pins (at least two power pins, VCC and VEE for powering the chip, four pins for the four power detector outputs and others for the frequency synthesizer). The outputs of the four power detectors can be sampled and digitized by the ADC components in the receiver back end circuit comprising of the four ADCs, control circuitry for channel selection and a digital signal processor for running the calibration and DSP algorithm developed in this thesis. The integrated hardware along with the calibration and DSP algorithm developed in this thesis will make a very low cost and low power receiver alternative for 60GHz applications.

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