THE UNIVERSITY OF CALGARY

Analysis and Design of Higher-Order Sigma-Delta Analog-to-Digital Converters

by

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La difficulté d'aboutir ne fait qu'ajouter
à la nécessité d'entreprendre.

Beaumarchais
Le Barbier de Séville

Abstract

This thesis is concerned with the analysis and design of higher-order sigma-delta (Σ-Δ) analog-to-digital (A/D) converters. An equivalent open-loop system is derived for the analysis of the conventionnal multi-loop Σ-Δ converters. This open-loop system is applied to the investigation of the spectral characteristics of the corresponding third-order converter. Then, a new enumeration technique is presented for the design of low-order Σ-Δ converters. An application to the design of first-order converters leads to the rediscovery of the conventional Σ-Δ converter along with the discovery of a new LDI-based converter. Finally, the design of higher-order bandpass Σ-Δ converters is considered. A careful comparison of two known configurations leads to the development of a new resonator-based converter which exhibits the best features of both converters.

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In memory of my late father

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Introduction

1.1 Digital Signals and Systems

A signal (from the Latin word *signum*) is an object, a symbol, a sound, a gesture, used to represent a piece of information. Signals have been used since prehistory.

Electricity has only been used as a vehicle for information interchange since the first half of the 19th Century. This is when Samuel Morse developed the telegraph. Its use of a discrete set of symbols (dots and hyphens) make the telegraph the first digital system in the history of electrical engineering. The invention of the transistor (1948) and the microprocessor (1972) have helped making the digital processing of data faster and cheaper than ever. As a matter of fact, the computing power of digital machines is doubling every 18 months. With the development, in the 1980s, of application specific integrated-circuits (ASICs) and specialized processors, more and more people tend to favor digital processing of signals as opposed to the corresponding analog processing.

In electrical engineering, several classes of signals have been defined. The

most important definitions relate to the notions of domain (region of support) and range. A *continuous-time* signal is a signal which is defined at each instant of time (continuous region of support). On the other hand, a *discrete-time* signal is only defined at discrete instants of time. In a similar way, signals with continuous and discrete range (or amplitude) can be defined. Moreover, continuous-time continuous-range signals are commonly referred to as analog signals and discrete-time discrete-amplitude signals are known as digital signals. (see Table 1.1)

	Continuous-time	**Discrete-time**
Continous Amplitude	Voice	Daily Precipitations
Discrete Amplitude	Traffic Lights	Closing price on the Stock Market

Table 1.1: **Examples of Different Classes of Signals.**

One of the most important features of digital processors is their programmability. No modification of the hardware components is required to modify the task of the processor. On the other hand, limitations on the processing speed of digital systems may reduce the number of applications.

Because every real-life signal is analog (*e.g.* sound, image), there must be a device whose task is to convert the analog input signal into a digital signal (Fig. 1.1). Such a device is called an analog-to-digital (A/D) converter. A

Figure 1.1: **A Generic Digital Processing System**

specific class of A/D converters known as Sigma-Delta (Σ-Δ) converters is the subject of the present thesis. In the following, the underlying principles of A/D conversion with an emphasis on Σ-Δ converters are explained.

Conversely, it is important to convert digital signals back to their analog form. This is perfomed by digital-to-analog (D/A) converters.

1.2 An Introduction to Sigma-Delta A/D Conversion

1.2.1 A/D Conversion

As seen in Section 1.1, A/D conversion is a critical operation. A very accurate conversion is absolutely necessary in order to perform an accurate processing of data. The task of an A/D converter is to map an analog input signal into a binary number that represents the amplitude of the input signal at a given instant of time, and at a given rate called sampling rate. If the input signal amplitude falls within a given range of values, the A/D converter will issue a codeword corresponding to the value of the input signal at that moment.

Example 1 *Suppose the input signal $u(t)$ is constrained between the values 0 and $+V$. Also, assume the A/D converter gives a 2-bit binary number as output. Then, the output of the A/D converter will be as given in Table 1.2.*

$$\begin{array}{lll} (00)_2 & \textit{if} & 0 \leq u(t) < V/4 \\ (01)_2 & \textit{if} & V/4 \leq u(t) < V/2 \\ (10)_2 & \textit{if} & V/2 \leq u(t) < 3V/4 \\ (11)_2 & \textit{if} & 3V/4 \leq u(t) < V \end{array}$$

Table 1.2: **Output of a 2-bit A/D Converter.**

This method of mapping a continuous signal into a binary codeword is commonly known as pulse code modulation (PCM) and is widely used in digital signal processing.

There are two classes of A/D converters, namely, indirect converters and direct converters.

Indirect Converters

Indirect converters use an intermediate quantity (frequency, time, etc.) to convert the signal. For instance, some converters make use of a voltage controlled oscillator along with a counter for the A/D conversion. Indirect techniques yield high resolutions but have very low conversion speeds. They are mainly used in instrumentation (*e.g.* digital multimeters).

Direct Converters

As opposed to the previous class of converters, the direct converters do not make use of an intermediate quantity. In most cases, the value to be converted is compared to a set of known levels and a decision is made based on the result of the comparison. One can distinguish between five important subclasses of direct converters : parallel converters (also known as flash converters), successive approximation converters, hybrid converters, electromechanical converters, and the important subclass of oversampled converters.

1. *Parallel Converters (Flash Converters)*

   In this class of converters, the magnitude of the input signal is compared to a set of predetermined reference values. The result of the comparison is then encoded into a binary code. Because $2^N - 1$ comparators are required for a N-bit binary code, this technique is usually limited to

8-bit A/D conversion. The general structure of a 2-bit flash converter is shown in Fig. 1.2.

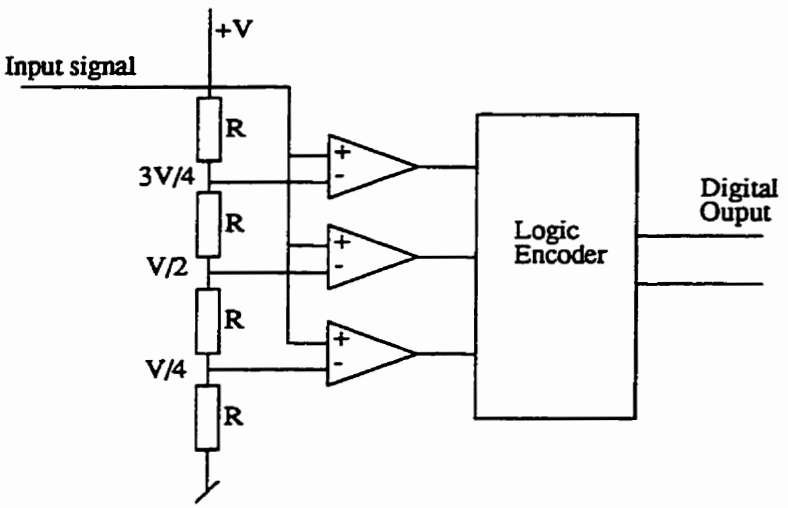

Figure 1.2: **Structure of a Flash A/D Converter**

2. *Successive Approximation Converters*

   Converters belonging to this class successively try to approximate the analog signal through the use of a D/A converter embedded in a feedback loop. This technique provides a high level of accuracy (up to 16 bits) but leads to a relatively low conversion speed.

3. *Hybrid Converters*

   These converters combine the features of the flash converters and those of the successive approximations converters in an attempt to obtain a compromise between speed and precision.

4. *Electromechanical Converters*

   By the mean of successive opaque and transparent sections along with photoelectric detectors, a mechanical position can be digitally encoded

(see Fig. 1.3). Note that a more practical implementation would use a Gray code.

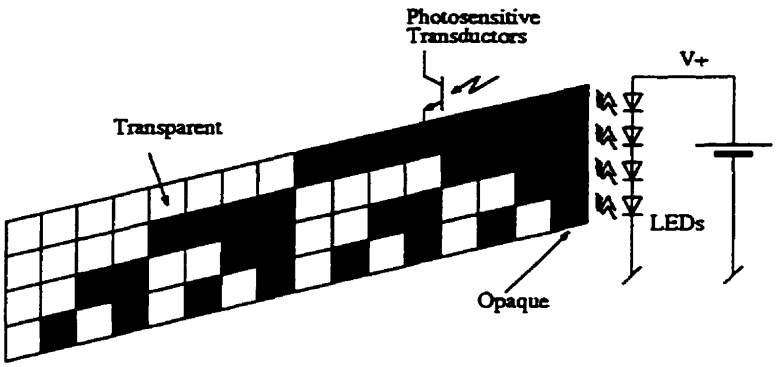

Figure 1.3: **A 4-bit Linear Electromechanical Encoder**

5. *Oversampling Converters*

   Oversampling corresponds to the case when the sampling frequency of the analog input signal takes place at a rate much higher than the Nyquist rate. As shown in the subsequent sections, this technique very efficiently increases the precision of the conversion. It is also very robust in the sense that one-bit quantizers can be combined with low tolerance components. On the other hand, the need for data postprocessing (decimation) and high sampling rates reduces the number of potential applications for this class of converters. Oversampling converters are often found in compact-disc (CD) players.

1.2.2 Quantization

The quantization process is the core of analog-to-digital conversion. Its main task is to compare the value to be converted to a set of reference values. The device which performs this task, the quantizer, maps a continuous range of

input values (usually a voltage) into a discrete set of values. The simplest quantizer that can be thought of is a comparator (Fig. 1.4) whose output can take on either the level $+V$ or the level $-V$, depending whether the input is positive or negative. As these two values, in turn, can be represented by one bit, the comparator shown in Fig. 1.4 is often referred to as a single-bit quantizer.

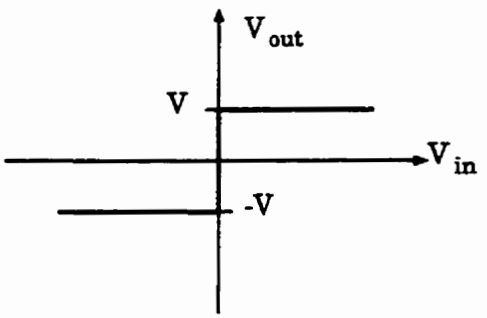

Figure 1.4: **A Single-Bit Quantizer.**

Obviously, multi-level quantizers can also be designed (see Fig. 1.5). The number of quantization levels Q is chosen to be a positive integer power of two, so as to be encoded into a binary number in the most efficient way. Assuming the number of bits to be N, the number of quantization levels Q is given by

$$Q = 2^N. \tag{1.1}$$

Since a quantizer is inherently a non-linear device, the analysis of a circuit containing such a device cannot be performed using standard linear analysis techniques. However, in 1948, Bennett [Ben48] showed that, under some conditions, the quantization noise can be considered as additive white noise (uniformly distributed). In particular, one of the conditions is that the quantizer should have a large number of levels. This condition, along with other

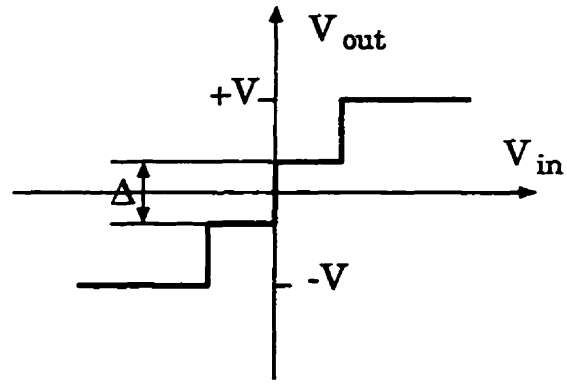

Figure 1.5: **A 2-Bit Quantizer (N=2, Q=4)**

ones, cannot usually be satisfied as most of the Σ-Δ modulators use single- or two-bit quantizers.

Notwithstanding the above restrictions, it is often convenient to use the white noise source model to predict the behaviour of an A/D converter. For all practical purposes in the study of Σ-Δ converters, the results obtained using this model are valid as a rough approximation for the first-order case and are quite accurate for higher order cases (see Sections 1.2.5 and 1.2.8). Therefore and unless mentioned otherwise, the white noise assumption will be assumed to be valid throughout the present thesis.

1.2.3 Nyquist-rate PCM Modulation

In the field of signal processing, the fact that the spectrum of a sampled signal is periodic is a well-known result. Nyquist's sampling theorem [OS89] dictates that any signal with limited bandwidth must be sampled at a frequency at least twice the highest frequency contained in that signal. In this way, the sampled signal can be processed and converted back to the analog domain without loss of information. Failure to sample a signal at a high enough rate

will introduce a phenomenon known as aliasing.

Very often, bandlimited signals do not readily exist. It is however possible to pass the analog signal to be sampled through a lowpass filter (also called an antialiasing filter) which will remove the frequency components that are above half the sampling frequency. The constraints on the antialiasing filter can be very tight in the case of Nyquist-rate sampling as shown in Fig. 1.6. In this case, the lowpass antialiasing filter must have a very narrow transition band; a condition which is usually very difficult to satisfy.

Throughout the present thesis, it will be assumed that all the input signal excitations used have had their high-frequency components removed by an appropriate antialiasing filter.

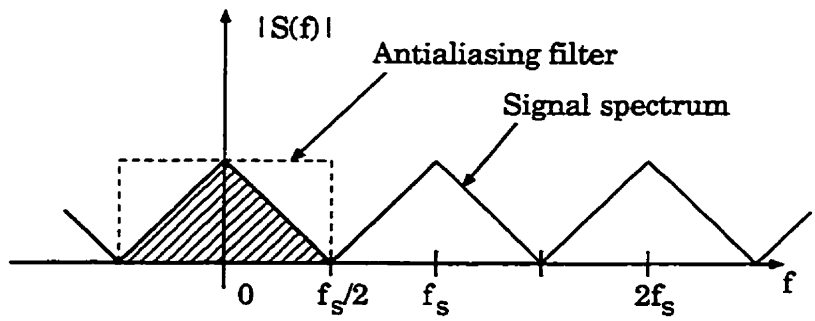

Figure 1.6: **Sampled Signal Spectrum.**

The most important quality criterion for an A/D converter is the signal-to-quantization-noise ratio (SQNR or SNR) which relates the power of the input signal to the power of the quantization noise introduced by the quantizer. Mathematically, the SQNR is defined as

$$\text{SQNR} = \frac{\sigma_x^2}{\sigma_{es}^2}, \tag{1.2}$$

with σ_x^2 being the signal power and σ_{es}^2 being the quantization noise power at

the output of the converter. Obviously, more noise for a given signal implies a reduced SQNR.

It has to be pointed out that, throughout the present thesis, powers are normalized with respect to a 1 Ω resistive load. In this way, the unit of power is V^2 instead of W. Moreover, power spectrum densities are normalized with respect to a 1 Hz frequency band (*i.e.* the unit becomes V^2 instead of W/Hz). In the case of multi-bit Nyquist-rate quantization, the quantization noise can be assumed to be uniformly distributed. If Δ is defined to be the quantization step, the power σ_{es}^2 of the quantization noise is given by [CT92]

$$\sigma_{es}^2 = \frac{\Delta^2}{12}. \tag{1.3}$$

Also, the quantization step Δ and the number of bits N are related in accordance with

$$\Delta = \frac{2V}{Q-1} = \frac{2V}{2^N - 1} \approx \frac{2V}{2^N}, N \gg 1, \tag{1.4}$$

where Q is the number of quantization levels. Replacing Eqn. (1.4) into Eqn. 1.3 and using the definition given in Eqn. 1.2, it is possible to obtain the SQNR (expressed in dB) of a Nyquist-rate quantizer with N bits as follows.

$$\text{SQNR}_{dB} \approx 10 \log \frac{\sigma_x^2}{V^2} + 6.02N - 4.77, \tag{1.5}$$

where σ_x^2 is the input signal power.

The well-known result given by Eqn. (1.5) implies that doubling the number of quantization levels increases the SQNR by 6 dB. When comparing two A/D converters, it is common to describe their performance in term of the number of resolution bits. For example, if a converter has a SQNR which is

9dB better than that of another converter, the former converter is said to have a 1.5 bit higher resolution.

Example 2 *From Eqn. (1.5), the maximum SQNR is obtained when the input signal power σ_x^2 is as large as possible. In the case of a sinusoidal signal, the largest sinusoid has amplitude V and power $V^2/2$. In this case, a 12-bit quantizer ($N = 12$) with the largest sinusoid possible at the input yields a maximum SQNR of 74 dB. Considering an audio signal of bandwidth $f_B = 20$ kHz, the sampling frequency must satisfy the condition $f_s > 40$ kHz. Typically, laser compact-disc signals are sampled at 44.1 kHz.*

1.2.4 Oversampled PCM Modulation

Sampling a signal at the Nyquist rate is often inconvenient because of the very tight constraints on the antialiasing filter. However, if the sampling frequency f_s is larger than twice the highest frequency f_B contained in the signal, the converter is said to be oversampled. The oversampling ratio (OSR) quantifies the amount of oversampling and is defined as

$$\text{OSR} = \frac{f_s}{2f_B}. \tag{1.6}$$

In the case of Nyquist-rate sampling, OSR is unity ($f_B = f_s/2$).

Fig. 1.7 shows the spectrum of an oversampled signal, along with the antialiasing filter constraints. One can observe that the transition band is larger than in the case of Nyquist-rate sampling. Consequently, the constraints have been relaxed and the implementation of the antialiasing filter is simplified.

The fact that too high a sampling frequency has been used implies that the digital output signal has to be passed through a decimation filter (shown

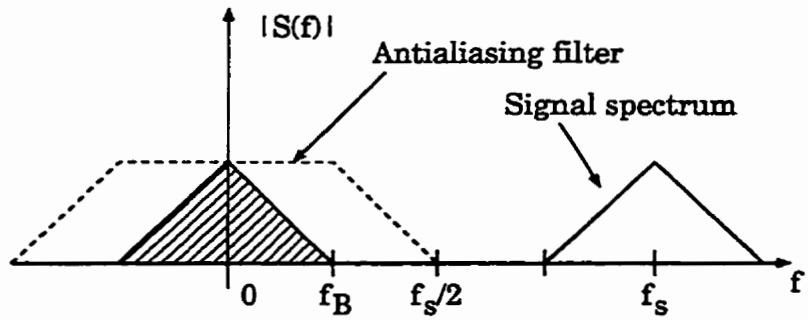

Figure 1.7: **Oversampled Signal Spectrum.**

in Fig. 1.8) and downsampled. Even though the transition band of the decimation filter is very narrow, the digital decimation filter is easier to implement than its analog counterpart. Oversampling also results in an increased SQNR as shown in the following.

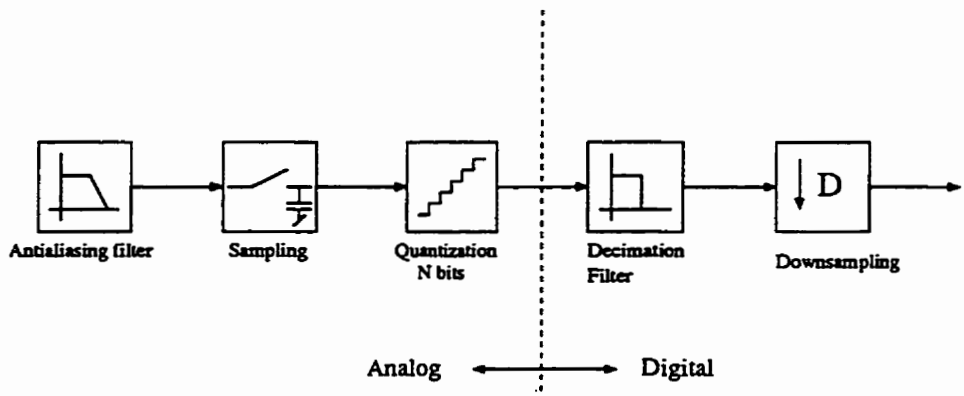

Figure 1.8: **An Oversampled A/D Converter.**

Assuming a white quantization noise with power $\sigma_{es}^2 = \frac{\Delta^2}{12}$, the power spectral density (PSD) of the quantization noise is a constant given by [ASS96]

$$E(f) = \frac{2\Delta^2}{12(f_s/2)}. \tag{1.7}$$

Therefore, the higher the sampling frequency, the lower the quantization noise in a given frequency band. Fig. 1.9 illustrates this phenomenon.

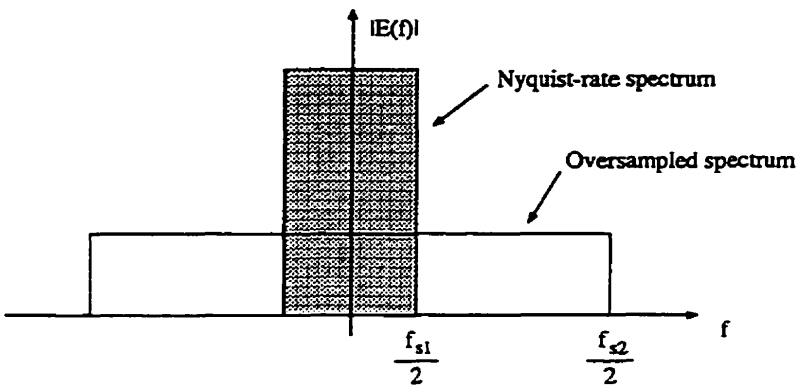

Figure 1.9: **Noise Spectra for Nyquist-rate and Oversampled PCM A/D Converters.**

Because the quantization noise power σ_{es}^2 is inversely proportional to the sampling frequency, the doubling of f_s improves the SQNR by 3dB. In this way, oversampling can be considered as a trade-off between speed and accuracy. This equivalently means that the number of quantization bits can be reduced as the oversampling ratio is increased.

Example 3 *Using a 6-bit quantizer for a 20 kHz band-limited signal, it is possible to obtain a SQNR of 74 dB if the sampling frequency is 164 MHz. This corresponds to an OSR of 4100.*

1.2.5 Sigma-Delta A/D Conversion

In oversampled PCM A/D conversion, the spectrum of the quantization noise is constant over the whole frequency range. In particular, the noise will be present both inside the signal frequency band and outside. By the mean of feedback loops and appropriate feedforward paths, it is possible to reduce the

presence of quantization noise inside a given frequency band at the cost of an increased quantization noise power outside that band. Developed in 1962 by Inose and Yasuda [IY63], Sigma-Delta (Σ-Δ) A/D conversion is the most well-known representative of a class of converters known as noise-shaping converters.

In its original configuration, a Σ-Δ A/D converter contains a one-bit quantizer and an integrator, both of which are embedded in a feedback loop as shown in Fig. 1.10, where $u_c(t)$ is a continuous-time continuous-amplitude input signal and $q(n)$ is a discrete-time discrete-amplitude output signal. The task of the quantizer shown in Fig. 1.10 is two-fold. Firstly, it acts as a

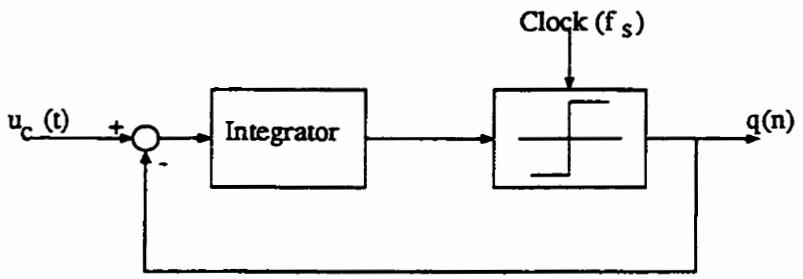

Figure 1.10: **Single-Loop Σ-Δ Converter.**

conventional quantizer; mapping a continuous set of values to a discrete set. Secondly, it performs this task at a given rate referred to as sampling rate (Often called sampling frequency and denoted f_s).

The behaviour of a Σ-Δ modulator can be described using an equivalent discrete-time model as shown in Fig. 1.11, with $T = 1/f_s$, $u(n)$ being a sampled version of $u_c(t)$ in accordance with $u(n) = u_c(nT)$, and $e(n)$ being the quantization-noise introduced by the quantization process and being modelled as an additive input.

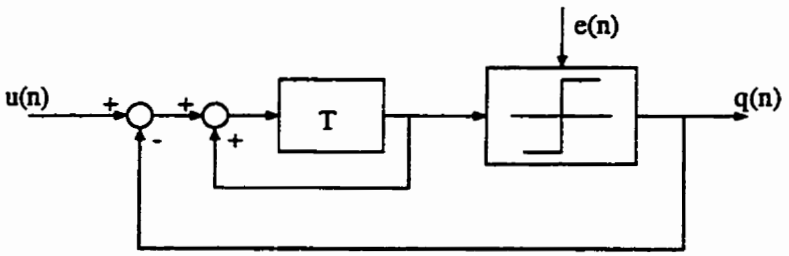

Figure 1.11: **Equivalent Discrete-Time Single-Loop Σ-Δ Converter.**

It can be shown [CT92, Eqn.(7)] that the output signal $q(n)$ is given by

$$q(n) = u(n-1) + e(n) - e(n-1). \tag{1.8}$$

Eqn. (1.8) shows that the output signal is composed of both the input signal delayed by one sampling period and a term which depends on the quantization noise.

Assuming the quantization noise to be white, the converter shown in Fig. 1.11 can then be modeled as a linear circuit. Consequently, conventional analysis tools such as the $\mathcal{Z}$-transform can be used. Introducing $U(z)$, $E(Z)$ and $Q(z)$ to be the $\mathcal{Z}$-transforms of $u(n)$, $e(n)$ and $q(n)$, respectively, Eqn. (1.8) becomes

$$Q(z) = z^{-1}U(z) + (1 - z^{-1})E(z). \tag{1.9}$$

From Eqn. (1.9), the signal transfer function STF(z) and the noise transfer function NTF(z) can be defined. The signal transfer function, is defined as

$$\text{STF}(z) = \frac{Q(z)}{U(z)}. \tag{1.10}$$

Similarly, the noise transfer function is defined

$$\mathrm{NTF}(z) = \frac{Q(z)}{E(z)}. \tag{1.11}$$

In the case of the Σ-Δ converter shown in Fig. 1.11 and described by Eqn. (1.9), STF(z) and NTF(z) are

$$\mathrm{STF}(z) = z^{-1} \tag{1.12}$$

$$\mathrm{NTF}(z) = (1 - z^{-1}). \tag{1.13}$$

The transfer functions STF(z) and NTF(z) can be considered as shaping functions which modify the spectrum of the input signal and the quantization noise, respectively. Through inspection of Eqns. (1.12) and (1.13), it can be seen that both STF(z) and NTF(z) are polynomials in z^{-1} of order one. Therefore, the Σ-Δ converter shown in Fig. 1.11 is said to be a first-order Σ-Δ converter. Moreover, $z = 1$ is a zero of NTF(z). Equivalently, NTF(z) = 0 around DC. This feature implies that the quantization noise is low at low frequencies (Fig. 1.12).

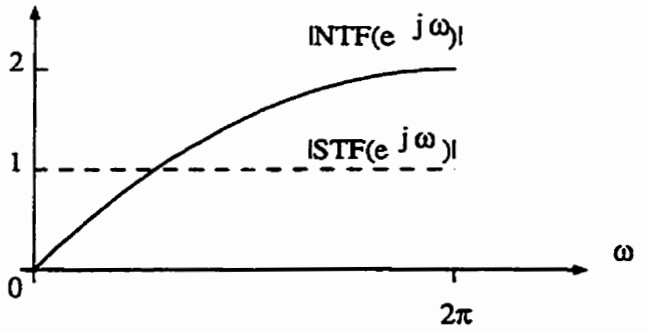

Figure 1.12: **Signal and Noise Transfer Function of the First-Order Σ-Δ Converter.**

By constraining the input signal spectrum to the low frequency part of the spectrum, it is possible to separate the signal and the quantization noise. Still using the white noise assumption, the overall spectral density $E_S(f)$ of the shaped quantization noise is given by [CT92, Eqn.(9)]

$$E_S(f) = \Delta\sqrt{\frac{2}{3f_s}}\sin\left(\frac{2\pi f}{2f_s}\right) \tag{1.14}$$

If the signal frequency band is defined to be in the range

$$0 \leq f \leq f_B, \tag{1.15}$$

the noise power in the signal band is given by

$$\sigma_{es}^2 = \int_{-f_B}^{f_B} |E_S(f)|^2 df. \tag{1.16}$$

By replacing $E_S(t)$ in Eqn. (1.16) by its value given by Eqn. (1.14) and assuming $f_s \gg f_B$, σ_{es}^2 can be approximated as

$$\sigma_{es}^2 \approx \frac{\Delta^2}{12}\frac{\pi^2}{3}\left(2\frac{f_B}{f_s}\right)^3 \;;\; f_s \gg f_B. \tag{1.17}$$

Using the oversampling ratio defined in Eqn. (1.6), the SQNR can be found to be

$$\text{SQNR}_{dB} \approx 10\log\frac{\sigma_x^2}{V^2} - 0.4 + 30\log\text{OSR}. \tag{1.18}$$

In a first-order Σ-Δ converter, each doubling of the oversampling ratio improves the SQNR by 9 dB or 1.5 bit.

Example 4 *For the same case a for Example 2, a 74dB resolution can be attained by a single-bit first-order Σ-Δ converter with an OSR of 380. For a 20 kHz bandwidth, this results in a sampling frequency of f_s = 15 MHz,*

about ten times less than that in Example 3.

1.2.6 Advantages of Σ-Δ Conversion

The first advantage of Σ-Δ conversion is that very coarse quantizers can be used. In the example presented above, a one-bit quantizer (comparator) was used.

Sigma-Delta converters are also very tolerant of non-linearities and other imperfections. Simulations and calculations have shown that leaky integrators do not influence significantly the behaviour of Σ-Δ converters [CT92].

1.2.7 Limitations of Σ-Δ Conversion

The converter shown in Fig. 1.11 can be equivalently represented by the converter in Fig. 1.13.

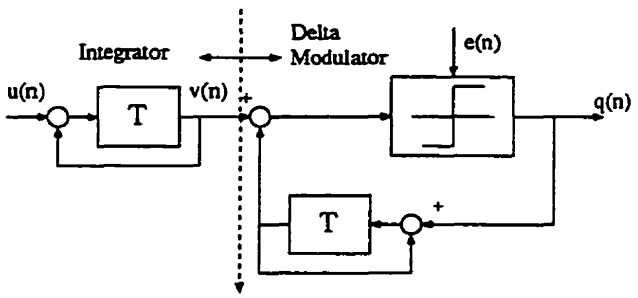

Figure 1.13: **Equivalent Representation of the First-Order Σ-Δ Converter in Fig. 1.11.**

This equivalent representation (see *e.g.* [Fon83, p.236]) exemplifies the behaviour of a Σ-Δ converter. The input signal is first integrated (Σ) and then passed through a conventional Δ modulator.

Delta modulation is limited by a phenomenon known as slope saturation [Fon83, p.230]. Because a Σ-Δ converter inherently contains a Δ modula-

tor, a similar limitation exists. In the converter shown in Fig. 1.13, if $v(n)$ exhibits too large a slope, then the Δ modulator will saturate. Moreover, because $v(n)$ is an accumulation (integral) of the input signal $u(n)$, a high amplitude of $u(n)$ will cause saturation of the Σ-Δ converter configuration under consideration. In 1995, Borsodi [Bor95, p.42] showed that the bound U_1 on the input signal for a single-loop converter is given by

$$U_1 \leq (Q-1)\frac{\Delta}{2}, \tag{1.19}$$

with Q being the number of quantization levels.

A saturated Σ-Δ converter is said to be unstable. It is a well-known result that configurations other than the first-order structure presented in this section are prone to instabilities.

1.2.8 Beyond First-Order Σ-Δ Conversion

Multi-Loop Configurations

High resolution in a first-order Σ-Δ converter often implies an impractically high sampling frequency (because of the required high OSR). In 1985, Candy [Can85] proposed an extension of the conventional single-loop Σ-Δ converter. Instead of integrating the input signal once, he suggested that the signal could be integrated twice (Fig. 1.14).

The corresponding relationship describing the behaviour of the double-loop Σ-Δ converter is

$$q(n) = u(n-1) + e(n) - 2e(n-1) + e(n-2). \tag{1.20}$$

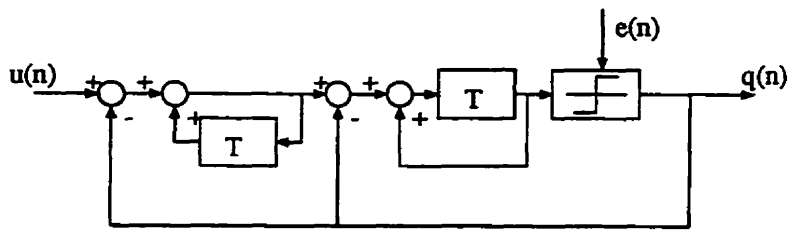

Figure 1.14: **Double-Loop Σ-Δ Converter.**

In the $\mathcal{Z}$-domain, the relationship becomes,

$$Q(z) = z^{-1}U(z) + (1 - z^{-1})^2 E(z). \tag{1.21}$$

Also, the transfer functions STF(z) and NTF(z) can be found to be

$$\text{STF}(z) = z^{-1}, \tag{1.22}$$

and

$$\text{NTF}(z) = (1 - z^{-1})^2. \tag{1.23}$$

The difference with the first-order structure is that NTF(z) exhibits a double-zero at the point $z = 1$ as opposed to a single zero. This structure is often called a second-order structure, due to the nature of NTF(z). Consequently, the quantization noise is even more reduced at low frequencies that in the first-order case. The maximum SQNR can be found to be

$$\text{SQNR}_{dB} = -11.1 + 50 \log \text{OSR} \tag{1.24}$$

for a sinusoidal input. In this case, each doubling of the OSR increases the SQNR by 15 dB.

Example 5 *In accordance with Eqn. (1.24), a SQNR of 74 dB for a 20kHz signal requires and oversampling ratio of 50. Therefore, the sampling frequency is $f_s = 2MHz$ which can easily be obtained by using conventional VLSI technologies.*

Similar multi-loop configurations can be devised. In the most general case, the SQNR is shown to increase by $3(2M + 1)$ dB for each doubling of the oversampling ratio, with M being the number of integrations (See Section 2.2).

Multistage Configurations

Other configurations include multistage (cascaded) configurations in which the quantization error from one converter is extracted and used as the input to another converter. The outputs of both converters are then combined in an attempt to reduce the quantization noise from the first stage. The simplest case is the so-called 1-1 cascade converter [ASS96] shown in Fig. 1.15

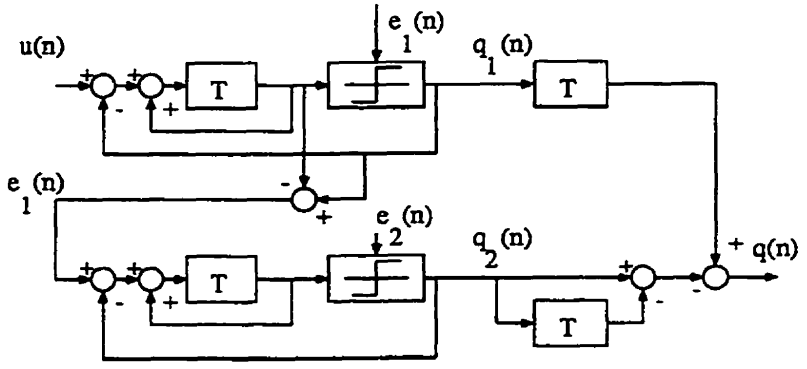

Figure 1.15: **1-1 Cascade Σ-Δ Converter.**

By inspection of Fig. 1.15 and with the help of Eqn. (1.9), the $\mathcal{Z}$-transforms $Q_1(z)$ and $Q_2(z)$ of $q_1(n)$ and $q_2(n)$, respectively, can be obtained

as

$$Q_1(z) = z^{-1}U(z) + (1 - z^{-1})E_1(z), \tag{1.25}$$

and

$$Q_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z). \tag{1.26}$$

The output signal $Q(z)$ is given by

$$Q(z) = z^{-1}Q_1(z) - (1 - z^{-1})Q_2(z). \tag{1.27}$$

Substituting for $Q_1(z)$ and $Q_2(z)$, Eqn. (1.27) becomes

$$Q(z) = z^{-2}U(z) - (1 - z^{-1})^2E_2(z). \tag{1.28}$$

In this way, the task of the second Σ-Δ converter is to cancel the quantization noise introduced by the first quantizer and to replace it with the quantization noise of the second quantizer shaped by a second-order function. As a matter of fact, this converter behaves the same way as the second-order converter shown in Fig. 1.14.

The advantage of cascaded structures is that they give higher order transfer functions while using low-order converters, thus avoiding the instability problem. The disadvantage is an increased circuit complexity. Also, due to the multi-bit nature of the output signal, the hardware for the subsequent decimation filter will be significantly complicated.

Bandpass Converters

Only structures with a noise transfer function having single or multiple zeros at the zero frequency (DC) have been studied so far. Due to their operation in the lower part of the spectrum, these converters have been named lowpass

converters. It has also been pointed out that an increased resolution implies a higher oversampling ratio, or, equivalently, an increased sampling frequency. Technology limitations often prevent a design to be implemented because of the requirements on the sampling frequency.

So far, the oversampling ratio has been defined as the ratio between half the sampling frequency, f_s, and the highest frequency in the input signal, f_B. However, in the case of a bandpass signal constrained between the frequencies f_l and f_h, with $f_l < f_h$, there is no need to have a reduced noise level below f_l. In other words, the frequency band $[0, f_l]$ can be used by the quantization noise spectrum. This also means that the zeros of the noise transfer function can be moved on the unit circle away from DC ($z = 1$) to a set of points corresponding to the signal frequency band (Figs. 1.16 and 1.17). At frequencies near the zeros of NTF(z), the quantization noise will

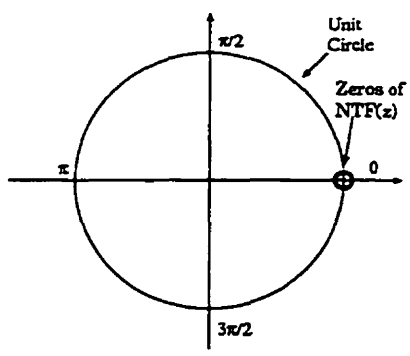

Figure 1.16: **Lowpass Noise Transfer Function.**

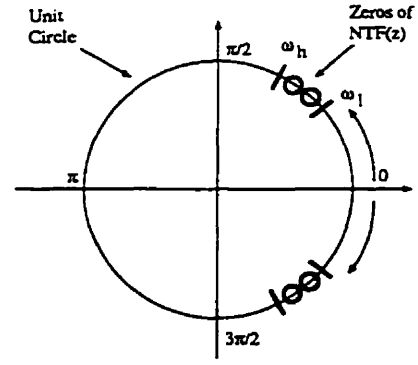

Figure 1.17: **Bandpass Noise Transfer Function.**

be reduced, thus allowing the signal to be separated from the quantization noise. Several structures for bandpass conversion have been proposed [LS87, JSF93, BN97] and will be discussed in greater detail in Chapter 4.

1.3 Open Problems In Sigma-Delta Conversion

1.3.1 Analysis and Characterization

The presence of a non-linear device precludes the use of conventional analysis tools to describe the quantization noise and the characteristics of Σ-Δ converters. Very often, the assumption of a white uncorrelated uniformly distributed quantization noise is made as an attempt to model the behaviour of Σ-Δ converters. It has been shown, however, that this assumption does not hold true for first- and second-order structures [CWG89]. Therefore, other tools have to be developed in order to predict the composition of the quantization noise. The works of Candy and Benjamin [CB81], Gray [Gra89, Gra90], Gray, Chou, and Wong [GCW89], He, Kuhlman, and Buzo [HKB90], Rangan and Leung [RL92], and Botteron and Nowrouzian [BN96] can be viewed as an attempt to solve that problem.

All the above approaches were only concerned with specific structures in mind. In 1995, Borsodi [Bor95] developed a technique based on a state-space approach to describe the quantization noise for a general class of converters having integer multiplier coefficients and a single quantizer. Since then, no attempt, to the author's knowledge, has been made to generalize this technique to structures containing non-integer multipliers or several quantizers.

1.3.2 Design

Due to the present lack of analysis tools, the design of Σ-Δ converters, especially in the bandpass case, is a challenging task. The method currently used is to employ known structures to implement a set of signal- and noise-

transfer functions. The establishment of a rigorous method still remains an open problem.

1.4 Overview Of The Thesis

The purpose of the present thesis is three-fold.

Firstly, an analysis of the quantization-noise in triple- and multi-loop Σ-Δ converters is presented in Chapter 2. The proposed approach makes use of the periodicity of the quantization noise function in an attempt to derive a closed-form solution for the quantization noise in a multi-loop Σ-Δ converter configuration. Then, the results are applied to a third-order structure and an analysis of the quantization noise spectral characteristics is given.

Secondly, Chapter 3 introduces the basic principles for the deterministic design of Σ-Δ converters. The critical building components are isolated and interconnected to each other. Enumeration of the possible interconnections enables one to generate all the possible structures meeting a specific set of criteria.

Thirdly, bandpass Σ-Δ A/D conversion is considered in Chapter 4. Analysis of two existing structures leads to the establishment of comparison criteria. These criterias are then used to discuss the performance of a new resonator-based Σ-Δ converter configuration.

Finally, Chapter 5 concludes the thesis by a review of the material presented in the previous chapters. It also reports on the parts of the thesis that are believed to be original contributions. Then, some ideas for future work are proposed. The chapter is then closed by concluding remarks of a more general nature.

Chapter 2

Quantization Noise in Multi-Loop Σ-Δ Converters

2.1 Introduction

One of the most important problems in the analysis of Σ-Δ converters is the absence of analytic analysis tools. Very often, computer simulations are carried out in order to obtain an estimation of the performance of the Σ-Δ converter configuration under consideration. The presence of the constituent (non-linear) coarse quantizer makes the analysis complicated, even in the case of simple converter configurations. Recently, Borsodi and Nowrouzian [BN95] developed an analytical technique for the analysis and characterization of a general class of Σ-Δ converter configurations. This technique is based on replacing the Σ-Δ converter by an equivalent open-loop system which circumvents the problems that normally arise as a result of the coarse quantizer being embedded in a feedback loop. The resulting equivalent open-loop system was subsequently applied to the determination of the shaped signal and the shaped quantization noise for the spectral analysis of Σ-Δ converters.

Some time ago, Rangan and Leung [RL92] developed a mathematical technique for the determination of the quantization error for a double-loop Σ-Δ converter. Their method is based on representing the internal quantization error by a corresponding Fourier series expansion. This technique was successfully applied to the spectral analysis of the output signal produced in response to a sinusoidal input excitation.

The present Chapter extends the results in [RL92] to higher-order (triple-loop, etc.) Σ-Δ converter configurations. In particular, Section 2.2 is concerned with the derivation of an open-loop equivalent for multi-loop Σ-Δ converters. This is achieved by taking advantage of the fact that the quantization error function is a periodic function of the input signal of the quantizer.

In Section 2.3, the results obtained in Section 2.2 are applied to the case of a triple-loop Σ-Δ converter configuration. In Subsection 2.3.3, the result is subsequently applied to sinusoidal input signal excitations. This procedure is facilitated by using the Fourier series expansion of the internal quantization error in conjunction with the *Jacobi-Anger* formula. A computational investigation and verification is undertaken in Subsection 2.3.4. Finally, Subsection 2.3.5 discusses the spectral characteristics of the quantization noise with a special emphasis on the white noise assumption made in Section 1.2.2.

2.2 Quantization Noise in Multi-Loop Σ-Δ Converters

2.2.1 Introduction

This section is concerned with the derivation of the open-loop equivalent of multi-loop Σ-Δ converters. The main reason for using third- and higher-order

Σ-Δ converters is that these structures yield better noise shaping performances for the same OSR when compared to lower-order converters. There is a cost however, namely, an increase in the order of the quantizer implies more sensitivity to parameter changes and decreased stability.

2.2.2 Closed-form Solution for the Internal Quantization Error

Introduction

This section is concerned with the derivation of the closed-form solution of the internal quantization error produced by a conventionnal multi-loop Σ -Δ converter in response to general input signal excitations.

Derivation of the Input-to-Output Relationship and of the Noise Transfer Function

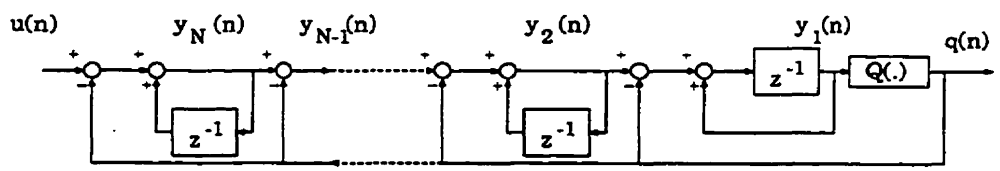

Figure 2.1: **A Conventional Multi-Loop Σ-Δ Modulator.**

The schematic diagram shown in Fig. 2.1 shows the multi-loop Σ-Δ converter under consideration of order N, where $u(n)$ represents the input signal sequence and $q(n)$ denotes the output signal sequence. The signals $y_1(n)$,$y_2(n)$, $\cdots$, $y_{N-1}(n)$, and $y_N(n)$ represent internal signals. $Q(.)$ represents a quantizer (single or multi-bit).

Assuming that the quantizer operates in its overload-free region [BN95],

the output $q(n)$ can be expressed as

$$q(n) = Q(y_1(n)) = 2\lfloor y_1(n)/2 \rfloor + 1, \tag{2.1}$$

where $\lfloor . \rfloor$ represents the floor operator (the largest integer less than or equal to the argument of the operator). It should be pointed out that the assumption of an overload-free quantizer operation implies that the Σ-Δ converter is free from the potential instability problems.

The internal quantization error $e(n)$ is defined in accordance with

$$e(n) = e\left(y_1(n)\right) = q(n) - y_1(n) \tag{2.2}$$

Then, by invoking Eqn. (2.1) into Eqn. (2.2), $e(n)$ becomes

$$e(n) = e\left(y_1(n)\right) = 2\left\lfloor \frac{y_1(n)}{2} \right\rfloor + 1 - y_1(n) \tag{2.3}$$

$$= 1 - 2\left\langle \frac{y_1(n)}{2} \right\rangle \tag{2.4}$$

where $< . >$ represents the fractional part operator in accordance with $x = \lfloor x \rfloor + < x >$. Assuming overload-free quantizer operation, $e(y_1(n))$ is therefore a periodic function of $y_1(n)$ with a period of 2 as shown in Fig. 2.2.

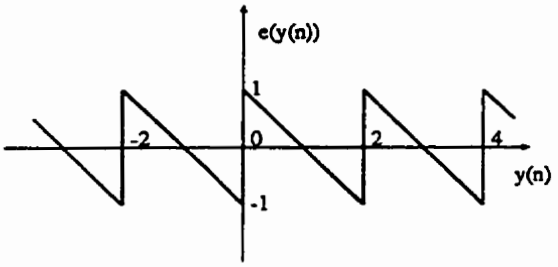

Figure 2.2: **The Internal Quantization Error Function.**

Lemma 1 *The input-to-output relationship of a conventional multi-loop Σ-Δ converter of order N shown in Fig. 2.1 is given by*

$$q(n) = u(n-1) + D^N e(n), \tag{2.5}$$

where $D(.)$ is the discrete differentiation operator defined in accordance with $Df(n) = f(n) - f(n-1)$. $D(.)$ is a linear operator and can be applied several times to the same sequence in order to obtain the successive discrete derivatives for this signal.

Proof : The proof follows an inductive argument similar to the one presented in [HKB92] as given in the following.

The lemma holds true for $N = 1$ [CT92], $N = 2$ [Can85] and for $N = 3$ [BN96]. It is therefore sufficient to prove that if the lemma holds true for $N = M$, then it is also valid for $N = M + 1$.

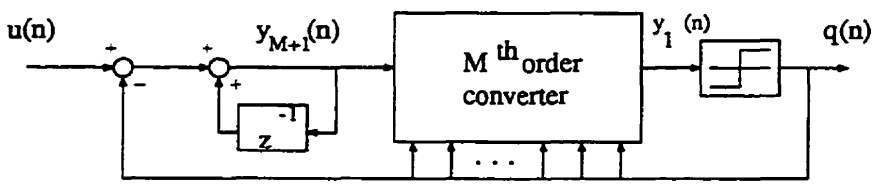

Figure 2.3: **A Conventional Multi-Loop Σ-Δ Modulator of order $M+1$.**

A $(M+1)$-order Σ-Δ converter can be represented as shown in Fig. 2.3.

By assumption,

$$q(n) = y_{M+1}(n-1) + D^M e(n) \tag{2.6}$$

holds true. Moreover, by inspection one obtains

$$y_{M+1}(n) = y_{M+1}(n-1) + u(n) - q(n) \tag{2.7}$$

or, equivalently,

$$y_{M+1}(n-1) = y_{M+1}(n-2) + u(n-1) - q(n-1). \tag{2.8}$$

Using the definition of the discrete differentiation equation, Eqn. (2.8) becomes

$$Dy_{M+1}(n-1) = u(n-1) - q(n-1). \tag{2.9}$$

Taking the discrete derivative of Eqn. (2.6) yields

$$Dq(n) = Dy_{M+1}(n-1) + DD^M e(n). \tag{2.10}$$

Using Eqn. (2.9), the result becomes,

$$\begin{aligned} q(n) - q(n-1) &= u(n-1) - q(n-1) + D^{M+1}e(n) && (2.11) \\ q(n) &= u(n-1) + D^{M+1}e(n). && (2.12) \end{aligned}$$

This completes the proof of the lemma. *q.e.d.*

Lemma 1 can be used to gain a better understanding of the behaviour of multiloop Σ-Δ converters. It has been shown that the higher the order of the converter, the closer the quantization noise to white noise. For a second-order converter, the quantization noise is already white for a DC input signal and almost white with an AC input signal, in the latter case provided that the oversampling ratio is large enough [WG90]. For higher-order converters, the internal quantization noise has been shown to be white in all cases [HKB92].

Taking the $\mathcal{Z}$-transform of Eqn.(2.5) yields

$$Q(z) = U(z)z^{-1} + E(z)(1-z^{-1})^N. \tag{2.13}$$

Eqn. (2.13) shows that the output signal spectrum $Q(z)$ is composed of the input signal spectrum $U(z)$ shaped by z^{-1} and of the internal quantization noise pectrum $E(z)$ shaped by $(1-z^{-1})^N$. In the Fourier domain (i.e. along the unit circle of the z-domain), Eqn. (2.13) becomes

$$Q(e^{j\omega}) = U(e^{j\omega})e^{-j\omega} + E(e^{j\omega})(1-e^{-j\omega})^N, \tag{2.14}$$

where ω is the normalized frequency defined in accordance with

$$z = e^{j\omega}. \tag{2.15}$$

In the same way as in Section 1.2.5, the signal transfer function and the noise transfer function can be introduced in accordance with

$$\mathrm{STF}\left(e^{j\omega}\right) = e^{-j\omega}, \tag{2.16}$$

and

$$\mathrm{NTF}\left(e^{j\omega}\right) = \left(1-e^{-j\omega}\right)^N. \tag{2.17}$$

The magnitude of $\mathrm{STF}(e^{j\omega})$ is

$$\left|\mathrm{STF}(e^{j\omega})\right| = \left|e^{-j\omega}\right| = 1, \tag{2.18}$$

and the magnitude of $\mathrm{NTF}(e^{j\omega})$ can be found to be

$$\begin{aligned} \left|\mathrm{NTF}(e^{j\omega})\right| &= \left|1-e^{-j\omega}\right|^N \\ &= \left|2\sin\frac{\omega}{2}\right|^N. \end{aligned} \tag{2.19}$$

The noise transfer functions for the cases of $N = 1, 2, 3$ are drawn in Fig. 2.4. Also, an enlarged version of the low-frequency part of the spectrum is provided in Fig. 2.5.

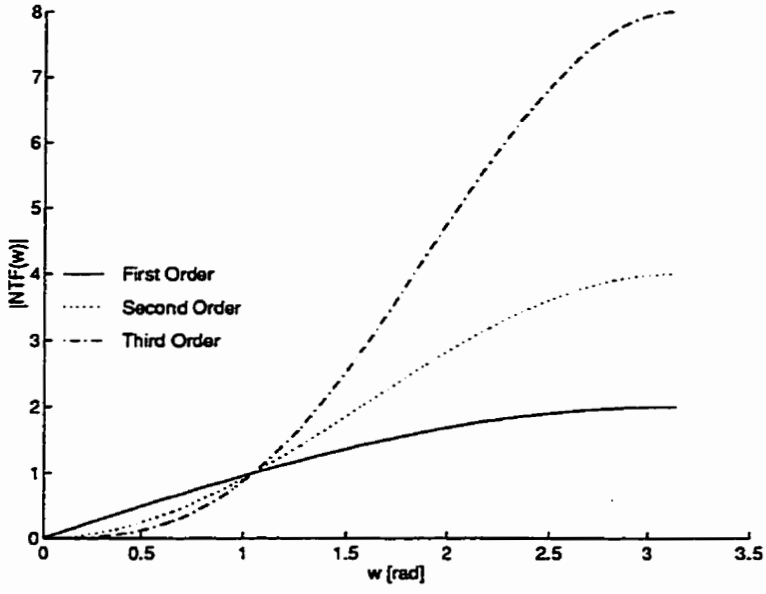

Figure 2.4: **Comparison of Noise-Transfer Functions of Order 1, 2, and 3.**

It is observed that as the order of the structure increases, the noise transfer function becomes flatter and attenuates more efficiently the low-frequency components of the quantization noise. Because the zeros of the noise transfer function are all located at the zero frequency, the converters are sometimes referred to as having Butterworth noise transfer functions.

Estimation of the SQNR

The noise power in the signal frequency band due to the quantization process can be expressed as

$$\sigma_{es}^2 = \int_{-f_B}^{f_B} \left|\mathrm{NTF}(e^{j\omega})\right|^{2N} \frac{\Delta^2}{12} df, \tag{2.20}$$

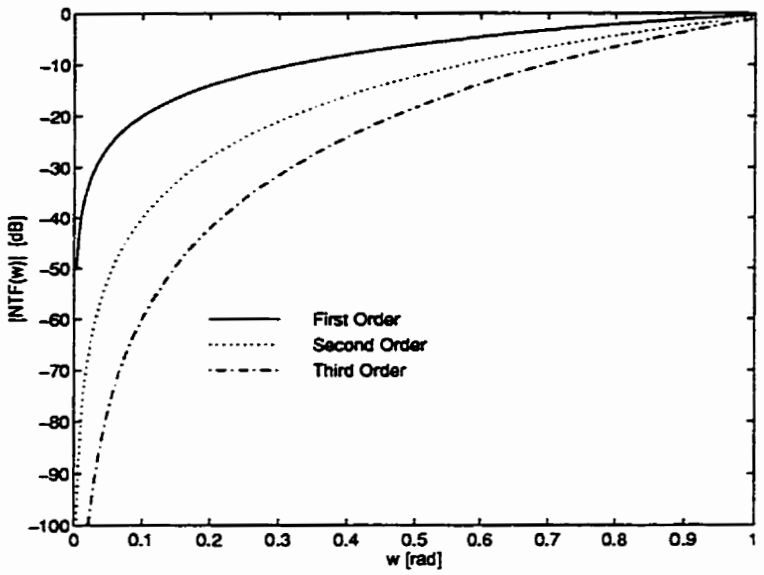

Figure 2.5: **Comparison of Noise-Transfer Functions of Order 1, 2, and 3 (Close-up of the Low-Frequency Range).**

with f_B being the bandwidth of the input signal and N being the order of the converter. Because of the symmetry of the spectrum, σ_{es}^2 can be rewritten

$$\sigma_{es}^2 = 2\frac{\Delta^2}{12}\int_0^{f_B}\left|\mathrm{NTF}(e^{j\omega})\right|^{2N} df. \tag{2.21}$$

Moreover, the frequencies ω and f are related one with each other in accordance with

$$\omega = \frac{\pi f}{f_s} \tag{2.22}$$

Substituting Eqns. (2.19) and (2.22) into Eqn. (2.21), σ_{es}^2 becomes

$$\sigma_{es}^2 = \frac{2\Delta^2}{12}\int_0^{f_B}\left|2\sin\frac{\pi f}{f_s}\right|^{2N} df. \tag{2.23}$$

Provided that

$$\frac{\pi f}{f_s} \ll 1, \tag{2.24}$$

which is the case when f_s is large (large OSR), Eqn. (2.23) can be simplified as

$$\sigma_{es}^2 \approx \frac{2\Delta^2}{12} 2^{2N} \int_0^{f_B} \left| \frac{\pi f}{f_s} \right|^{2N} df. \tag{2.25}$$

After solving for the integral and rearranging the terms, σ_{es}^2 finally becomes

$$\sigma_{es}^2 \approx \frac{\Delta^2}{12} \frac{\pi^{2N}}{(2N+1)} \mathrm{OSR}^{-(2N+1)}. \tag{2.26}$$

As shown in Example 2, the peak SQNR under a sinusoidal input is obtained when the input sinusoid has amplitude V and power $\sigma_x^2 = V^2/2$. Moreover, assuming a single-bit quantizer, Δ and V are related to each other in accordance with $\Delta = 2V$ (From Eqn. (1.4)). In this way, the SQNR is given by

$$\begin{aligned} \mathrm{SQNR}_{dB} &= 10 \log \frac{\sigma_x^2}{\sigma_{es}^2} \\ &= 10 \log \frac{3}{2\pi^{2N}} (2N+1) + 10(2N+1) \log \mathrm{OSR}. \end{aligned} \tag{2.27}$$

Eqn. (2.27) dictates that the SQNR increases by $3(2N+1)$dB for each doubling of the oversampling ratio, a well-known result.

2.2.3 Closed-Form Solution for the Quantization-Noise in a Multi-Loop Σ-Δ Converter

The purpose of this section is to prove the following theorem.

Theorem 1 *If the quantizer in the multi-loop Σ-Δ converter of order N shown in Fig. 2.1 operates in its overload-free region [BN95], then the closed-*

form solution of the quantization error $e(n)$ *is given by*

$$\begin{aligned} e(n) &= e(y_1(n)) \\ &= e\left(y_2(0) + \sum_{k=1}^{N} y_k(0) \begin{pmatrix} n+k-3 \\ k-1 \end{pmatrix} + \right. \\ &\quad \left. + \sum_{k=1}^{n-1} \begin{pmatrix} N-1+(n-1)-k \\ N-1 \end{pmatrix} u(k) - \begin{pmatrix} n-1+N \\ N \end{pmatrix} \right) \end{aligned} \tag{2.28}$$

The proof is based on the following lemma.

Lemma 2

$$\sum_{l_N=1}^{n-1} \sum_{l_{N-1}=1}^{l_N} \cdots \sum_{l_2=1}^{l_3} \sum_{l_1=1}^{l_2} u(l_1) = \sum_{k=1}^{n-1} \begin{pmatrix} N-1+(n-1)-k \\ N-1 \end{pmatrix} u(k), \tag{2.29}$$

where

$$\begin{pmatrix} a \\ b \end{pmatrix} = \frac{a!}{b!(a-b)!}, \tag{2.30}$$

holds.

Proof : See Appendix A.1 *q.e.d.*

Proof : Theorem 1 can be established by mathematical induction. By making use of Lemma 2, $e(n)$ can be rewritten

$$\begin{aligned} e(n) &= e\left(y_2(0) + \sum_{k=1}^{N} y_k(0) \begin{pmatrix} n+k-3 \\ k-1 \end{pmatrix} + \right. \\ &\quad \left. \sum_{l_N=1}^{n-1} \sum_{l_{N-1}=1}^{l_N} \cdots \sum_{l_2=1}^{l_3} \sum_{l_1=1}^{l_2} u(l_1) - \begin{pmatrix} n-1+N \\ N \end{pmatrix} \right). \end{aligned} \tag{2.31}$$

Let us consider the case of $N = 2$. Then, Eqn. (2.31) becomes

$$e(n) = e\left(y_2(0) + y_1(0)\binom{n-2}{0} + y_2(0)\binom{n-1}{1} + \sum_{l_2=1}^{n-1}\sum_{l_1=1}^{l_2} u(l_1) - \binom{n+1}{2}\right). \tag{2.32}$$

After performing binomial expansion, Eqn. (2.32) becomes

$$e(n) = e\left(y_1(0) + ny_2(0) + \sum_{l_2=1}^{n-1}\sum_{l_1=1}^{l_2} u(l_1) - \frac{n(n+1)}{2}\right). \tag{2.33}$$

The validity of the latter equation has been established in [HKB90, Theorem 1]. Therefore, the theorem holds true for $N = 2$.

In this way, it is sufficient to show that if the theorem holds true for $N = M$, then it is also valid for $N = M + 1$.

By inspection of Fig. 2.3, the relationship

$$y_{M+1}(n) = y_{M+1}(n-1) + u(n) - y_1(n) \tag{2.34}$$

holds. Solving for $y_{M+1}(n)$ recursively, Eqn. (2.34) becomes

$$y_{M+1}(n) = y_{M+1}(0) + \sum_{k=1}^{n} u(k) - \sum_{k=1}^{n} q(n). \tag{2.35}$$

Finally, taking the quantizer into consideration, $y_{M+1}(n)$ becomes

$$y_{M+1}(n) = y_{M+1}(0) + \sum_{k=1}^{n} u(k) - \sum_{k=1}^{n}\left(2\left\lfloor\frac{y_1(n)}{2}\right\rfloor + 1\right). \tag{2.36}$$

Also, by assumption,

$$e(n) = e\left(y_2(0) + \sum_{k=1}^{M} y_k(0) \begin{pmatrix} n+k-3 \\ k-1 \end{pmatrix} + \sum_{l_M}^{n-1} \sum_{l_{M-1}=1}^{l_M} \cdots \sum_{l_2=1}^{l_3} \sum_{l_1=1}^{l_2} y_{M+1}(l_1) - \begin{pmatrix} n-1+M \\ M \end{pmatrix}\right) \quad (2.37)$$

holds. Replacing for $y_{M+1}(n)$ into Eqn. (2.37) gives

$$\begin{aligned} e(n) = e\Bigg(& y_2(0) + \sum_{k=1}^{M} y_k(0) \begin{pmatrix} n+k-3 \\ k-1 \end{pmatrix} + \\ & \sum_{l_M=1}^{n-1} \sum_{l_{M-1}=1}^{l_M} \cdots \sum_{l_2=1}^{l_3} \sum_{l_1=1}^{l_2} y_{M+1}(0) + \\ & \sum_{l_M=1}^{n-1} \sum_{l_{M-1}=1}^{l_M} \cdots \sum_{l_2=1}^{l_3} \sum_{l_1=1}^{l_2} \sum_{k=1}^{l_1} u(k) - \\ & \sum_{l_M=1}^{n-1} \sum_{l_{M-1}=1}^{l_M} \cdots \sum_{l_2=1}^{l_3} \sum_{l_1=1}^{l_2} \sum_{k=1}^{l_1} \left(2\left\lfloor \frac{y_1(n)}{2} \right\rfloor + 1\right) - \\ & \begin{pmatrix} n-1+M \\ M \end{pmatrix}\Bigg). \end{aligned} \quad (2.38)$$

Using the fact that $\lfloor . \rfloor$ is an integer and that $e(.)$ is periodic with period 2 (Fig. 2.2), along with changing the indices on the summations, Eqn. (2.38) becomes

$$e(n) = e\left(y_2(0) + \sum_{k=1}^{M} y_k(0) \begin{pmatrix} n+k-3 \\ k-1 \end{pmatrix} + \sum_{k=1}^{n-1} \begin{pmatrix} M-1+(n-1)-k \\ M-1 \end{pmatrix} y_{M+1}(0) + \sum_{l_{M+1}=1}^{n-1} \sum_{l_M=1}^{l_{M+1}} \cdots \sum_{l_2=1}^{l_3} \sum_{l_1=1}^{l_2} u(l_1)\right)$$

$$-\sum_{k=1}^{n-1}\left(\begin{pmatrix} M+(n-1)-k \\ M \end{pmatrix}-\begin{pmatrix} n-1+M \\ M \end{pmatrix}\right). \tag{2.39}$$

Rewritting the fourth summation in Eqn. (2.39) and using the identity [Spi68, Eqn. 3.9]

$$\sum_{k=0}^{B}\begin{pmatrix} A+k \\ A \end{pmatrix}=\begin{pmatrix} A+B+1 \\ A+1 \end{pmatrix}, \tag{2.40}$$

$e(n)$ becomes

$$\begin{aligned} e(n) \;=\; e\Bigg(y_2(0)+\sum_{k=1}^{M+1}y_k(0)\begin{pmatrix} n+k-3 \\ k-1 \end{pmatrix}+\sum_{l_{M+1}=1}^{n-1}\sum_{l_M=1}^{l_{M+1}}\cdots\sum_{l_2=1}^{l_3}\sum_{l_1=1}^{l_2}u(l_1)- \\ \begin{pmatrix} M+n-1 \\ M+1 \end{pmatrix}-\begin{pmatrix} M+n-1 \\ M \end{pmatrix}\Bigg) \end{aligned} \tag{2.41}$$

Finally, using the identity [Spi68, Eqn. 3.6]

$$\begin{pmatrix} a \\ b \end{pmatrix}+\begin{pmatrix} a \\ b+1 \end{pmatrix}=\begin{pmatrix} a+1 \\ b+1 \end{pmatrix}, \tag{2.42}$$

the quantization error becomes

$$\begin{aligned} e(n) \;=\; e\Bigg(y_2(0)+\sum_{k=1}^{M+1}y_k(0)\begin{pmatrix} n+k-3 \\ k-1 \end{pmatrix}+\sum_{l_{M+1}=1}^{n-1}\sum_{l_M=1}^{l_{M+1}}\cdots\sum_{l_2=1}^{l_3}\sum_{l_1=1}^{l_2}u(l_1)- \\ \begin{pmatrix} (M+1)+n-1 \\ (M+1) \end{pmatrix}\Bigg), \end{aligned} \tag{2.43}$$

establishing the validity of the theorem for $N = M + 1$. This completes the proof of the theorem.

q.e.d.

2.3 Quantization Noise Spectrum in a Triple-Loop Σ-Δ Converter With Sinusoidal Excitations

2.3.1 Introduction

The presence of the constituent (non-linear) coarse quantizer makes the analysis of Σ-Δ converters complicated even in the case of simple converter configurations and simple input signal excitations. Some time ago, Rangan and Leung [RL92] developed a mathematical technique for the determination of the quantization error for a double-loop Σ-Δ converter. Their method is based on representing the internal quantization error by a corresponding Fourier series expansion. This technique was successfully applied to the spectral analysis of the output signal produced in response to a sinusoidal input excitation.

The present section extends the results in [RL92] to the determination of the closed-form solution of the internal quantization error for a conventional triple-loop Σ-Δ converter configuration under overload-free quantizer operation. The closed-form solution of the internal quantization error for a general input signal is derived in Section 2.3.2. In Section 2.3.3, this solution is specialized for the important case of sinusoidal input signal excitations. This is facilitated by using the Fourier series expansion of the internal quantization error in conjunction with the *Jacobi-Anger* formula.

2.3.2 Derivation of an Open-Loop Equivalent for the Internal Quantization Error

This section is concerned with the derivation of the closed-form solution of the internal quantization error produced by a conventional triple-loop Σ-Δ converter configuration in response to general input signal excitations.

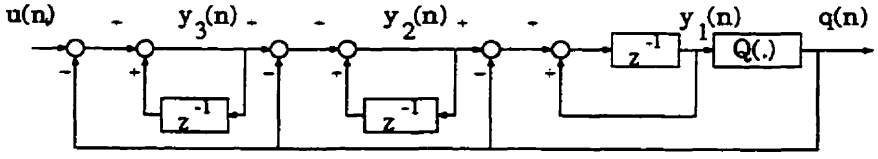

Figure 2.6: **A Conventional Triple-Loop Σ-Δ Modulator.**

The schematic diagram shown in Fig. 2.6 shows the triple-loop Σ-Δ converter configuration under consideration, where $u(n)$ represents the input signal excitation, and $q(n)$ represents the output response signal. The signals $y_3(n)$, $y_2(n)$, and $y_1(n)$ represent internal signals. Moreover, $Q(y_1(n))$ represents a coarse quantizer (single-bit or multi-bit).

By inspection, one can observe that

$$y_1(n) = y_1(n-1) + y_2(n-1) - q(n-1) \tag{2.44}$$

$$y_2(n) = y_2(n-1) + y_3(n) - q(n) \tag{2.45}$$

$$y_3(n) = y_3(n-1) + u(n) - q(n) \tag{2.46}$$

Lemma 3 *The output signal $q(n)$ in the triple-loop Σ - Δ converter shown in Fig. 2.6 is related to the input signal $u(n)$ via the internal quantization error $e(n)$ in accordance with*

$$q(n) = u(n-1) + D^3 e(n). \tag{2.47}$$

Proof : By applying Lemma 1 with $N = 3$. An alternate proof can be found in [BN96]. *q.e.d.*

Based on Lemma 3, the closed-form solution for $e(y_1(n))$ can be determined in accordance with the following theorem.

Theorem 2 *[BN96] If the coarse quantizer in the triple-loop Σ - Δ converter shown in Fig.2.6 operates in its overload-free region [BN95], then the closed-form solution of the internal quantization error $e(n)$ is given by*

$$\begin{aligned} e(n) &= e\left(y_1(n)\right) \\ &= e\left(y_1(0) + ny_2(0) + \frac{(n-1)n}{2}y_3(0) + \right. \\ &\quad \left. \sum_{i=1}^{n-1}\sum_{j=1}^{i}\sum_{k=1}^{j} u(k) - \frac{n(n+1)(n+2)}{6}\right) \end{aligned} \tag{2.48}$$

where $y_1(0)$, $y_2(0)$, and $y_3(0)$ are the initial values of the internal variables $y_1(n)$, $y_2(n)$, and $y_3(n)$, respectively.

Proof : Use Theorem 1 with $N = 3$. An alternate proof can be found in [BN96].

q.e.d.

2.3.3 Quantization Error for Sinusoidal Excitations

The result of Theorem 2 can be applied to the specific case of sinusoidal excitations. The final result will be obtained through a Fourier series expansion of the function $e(y_1(n))$ and by the use of the *Jacobi-Anger* formula.

Let us assume that the input signal is given by

$$u(n) = A_i \sin(\omega n + \phi_i), \tag{2.49}$$

with A_i being its amplitude and ϕ_i being its phase. By invoking Eqn. (2.49) into Eqn. (2.48), the internal quantization error becomes

$$e(n) = e\left(y_1(0) + ny_2(0) + \frac{(n-1)n}{2}y_3(0) + \sum_{i=1}^{n-1}\sum_{j=1}^{i}\sum_{k=1}^{j} A_i \sin(\omega k + \phi_i) - \frac{n(n+1)(n+2)}{6}\right) \tag{2.50}$$

It can be shown that the triple summation in Eqn. (2.50) can be reduced to

$$\sum_{i=1}^{n-1}\sum_{j=1}^{i}\sum_{k=1}^{j} A_i \sin(\omega k + \phi_i) = A_0 \sin(\omega n + \phi_0) + B_0 n^2 + C_0 n + D_0 \tag{2.51}$$

By solving the difference equation in Eqn. (2.51), the coefficients A_0, B_0, C_0 and D_0 and the phase angle ϕ_0 can be determined as

$$\begin{aligned}
A_0 &= \frac{A_i}{8\sin^3(\omega/2)}, \\
\phi_0 &= \phi_i + \frac{\omega}{2} - \frac{3\pi}{2}, \\
2B_0 &= A_i \sin(2\omega + \phi_i) + A_i \sin(\omega + \phi_i) - \\
&\quad A_0 \sin(3\omega + \phi_0) + 2A_0 \sin(2\omega + \phi_0) - \\
&\quad A_0 \sin(\omega + \phi_0), \\
C_0 &= A_i \sin(\omega + \phi_i) + A_0 \sin(\omega + \phi_0) - \\
&\quad A_0 \sin(2\omega + \phi_0) - 3B_0, \\
D_0 &= -A_0 \sin(\omega + \phi_0) - B_0 - C_0.
\end{aligned}$$

Furthermore, by taking into account the fact that $e(y_2(n))$ is a periodic function of $y_2(n)$ with period 2, the term $\frac{n(n+1)(n+2)}{6}$ in Eqn. (2.50) can be equivalently replaced by

$$\gamma(n) = \begin{cases} 0 & \text{for } n = \{0,2,3\} \bmod 4 \\ 1 & \text{for } n = 1 \bmod 4. \end{cases} \tag{2.52}$$

In this way, the internal quantization error $e(n)$ becomes

$$e(n) = e\left(A_0 \sin(\omega n + \phi_0) + \left(B_0 + \frac{y_3(0)}{2}\right) n^2 + \left(C_0 + y_2(0) - \frac{y_3(0)}{2}\right) n + D_0 + y_1(0) + \gamma(n)\right). \tag{2.53}$$

In order to proceed further, the internal quantization error $e(y_1(n))$ is represented by its Fourier series expansion in accordance with (see Fig. 2.2)

$$e\left(y_1(n)\right) = \sum_{\substack{l=-\infty \\ l\neq 0}}^{\infty} \frac{1}{j\pi l} e^{j\pi l y_2(n)} \tag{2.54}$$

By substituting Eqn. (2.54) into Eqn. (2.53), $e(n)$ becomes

$$e(n) = \sum_{\substack{l=-\infty \\ l\neq 0}}^{\infty} \frac{1}{j\pi l} e^{j\pi l(A_0 \sin(\omega n+\phi_0)+Bn^2+Cn+D+\gamma(n))} \tag{2.55}$$

where

$$B = B_0 + \frac{y_3(0)}{2}, \quad C = C_0 + y_2(0) - \frac{y_3(0)}{2}, \text{and } D = D_0 + y_1(0).$$

By invoking the *Jacobi-Anger* formula

$$e^{jA\sin(x)} = \sum_{m=-\infty}^{\infty} J_m(A) e^{jmx} \tag{2.56}$$

in Eqn. (2.55), the internal quantization error can be rewritten in the form

$$e(n) =$$

$$\sum_{\substack{l=-\infty \\ l\neq 0}}^{\infty} \frac{e^{j\pi l(Bn^2+Cn+D+\gamma(n))}}{j\pi l} \sum_{m=-\infty}^{\infty} J_m(A_0\pi l)e^{jm(\omega n+\phi_0)}, \tag{2.57}$$

where $J_m(.)$ represents the m-th order Bessel function of the first kind.

Before being able to take the Fourier transform of Eqn. (2.57) for computing the spectral characteristics of $e(n)$, one needs to explicitly determine the term $e^{j\pi l\gamma(n)}$. In accordance with Eqn. (2.52), $e^{j\omega l\gamma(n)}$ takes on the following value if l is even

$$e^{j\pi l\gamma(n)} = 1, \forall n \tag{2.58}$$

and

$$e^{j\pi l\gamma(n)} = \begin{cases} 1 & \text{for } \gamma(n)=0 \quad n=\{0,2,3\} \bmod 4 \\ -1 & \text{for } \gamma(n)=1 \qquad n=1 \bmod 4, \end{cases} \tag{2.59}$$

if l is odd. The case of l even is easy to handle. In the case of l odd, the following equality holds

$$e^{j\pi l\gamma(n)} = \cos^2\frac{\pi}{2}n - \sin\frac{\pi}{2}n. \tag{2.60}$$

Eqn. (2.57) thus becomes

$$\begin{aligned} e(n) &= \sum_{\substack{l=-\infty \\ l \text{ odd}}}^{+\infty} \frac{e^{j\pi l(Cn+D)}}{j\pi l} e^{j\pi lBn^2} \left(\cos^2\frac{\pi}{2}n - \sin\frac{\pi}{2}n\right) \sum_{m=-\infty}^{+\infty} J_m(A_0\pi l)e^{jm(\omega n+\phi_0)} \\ &+ \sum_{\substack{l=-\infty \\ l \text{ even} \\ l\neq 0}}^{+\infty} \frac{e^{j\pi l(Cn+D)}}{j\pi l} e^{j\pi lBn^2} \sum_{m=-\infty}^{+\infty} J_m(A_0\pi l)e^{jm(\omega n+\phi_0)} \end{aligned} \tag{2.61}$$

Eqn. (2.61) is the final form for the internal quantization error for a triple-loop Σ-Δ converter with sinusoidal excitations.

2.3.4 Computational Investigation

At this stage, it is useful to perform a computational investigation to check the validity of the results obtained so far. A corresponding verification through comparison to the results obtained by a direct simulation of the operation of the Σ-Δ converter is presented in this section.

Let us choose the input signal excitation to be arbitrarily fixed as

$$u(n) = 0.0501738174367 \sin(0.528764321n + 0.633435). \tag{2.62}$$

Moreover, let us select the initial conditions as

$$v_0 = 0.2 \quad y_3(0) = -0.45 \quad y_2(0) = 0.8$$

Then, one can use Eqns. (2.44), (2.45), (2.46) and (2.1) to evaluate the internal quantization error $e(n)$ as shown in Fig. 2.7. Similarly, one can use Eqn. (2.61), to obtain $e(n)$ as shown in Fig. 2.8. Clearly, the results shown in Fig. 2.8 are in agreement with those in Fig. 2.7. Any discrepancy can be attributed to the fact that the infinite summations in Eqn. (2.61) must be approximated by finite summations for numerical calculations. Having confirmed the validity of $e(n)$ in Eqn. (2.57), one can investigate the spectral characteristics of $e(n)$. According to Rangan and Leung [RL92], it appears that one should expect a continuous spectrum whereas lower-order Σ-Δ converters (first-order and second-order) exhibit discrete spectral components. Once the spectral characteristics of $e(n)$ are known, the next step will be to derive the power spectral density of the overall quantization error defined as $e(n) = D^3 e(n)$.

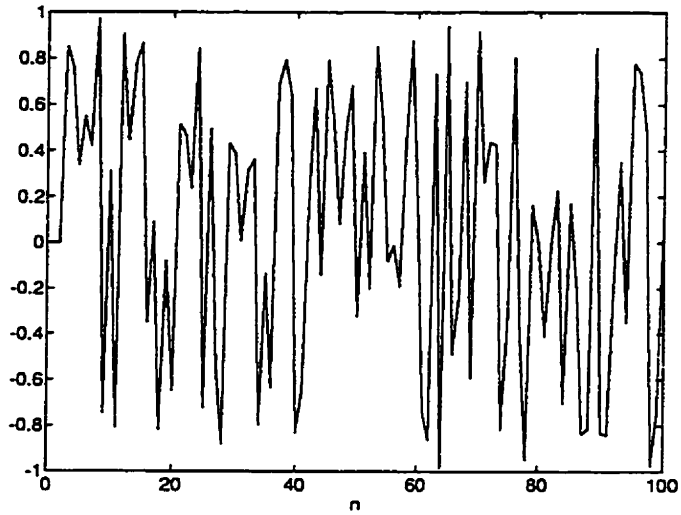

Figure 2.7: **Direct Simulation of the Internal Error.**

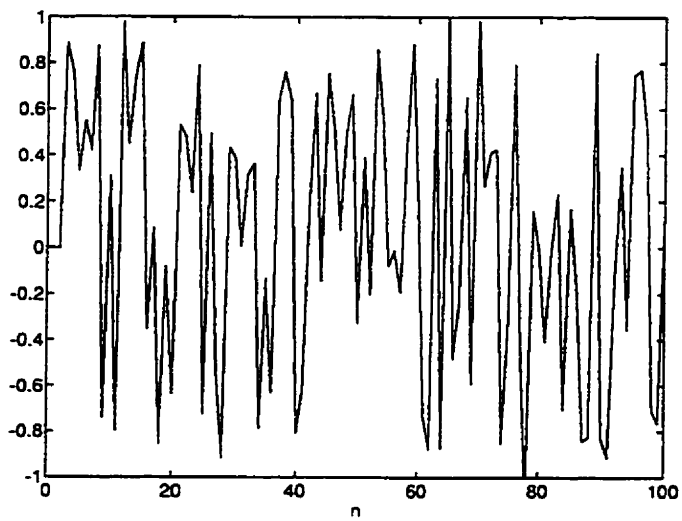

Figure 2.8: **Calculated Internal Error Using Eqn. (2.57).**

2.3.5 Spectral Characteristics of the Quantization Noise

Based on Eqn. (2.61), the next step is to evaluate the spectral characteristics of the quantization error $e(n)$. The presence of the term $e^{j\pi lBn^2}$ in Eqn. (2.61) precludes the straightforward calculation of the Fourier transform of $e(n)$. However, $e(n)$ can be seen as a linear combination of terms of the form

$$c(n) = e^{j(c_2n^2+c_1n+c_0)}. \tag{2.63}$$

Weyl's theorem (see *e.g.* [WG90]) states that if $c(t) = \langle a_0 + a_1t + \cdots \cdots + a_kt^k \rangle$ is the fractional part of a polynomial with real coefficients and if among $a_1, a_2, \cdots, a_k$, at least one coefficient is irrational, then the sequence $c(n), n = 1, 2, \cdots$ is uniformly distributed in the semi-open domain $[0, 1)$.

Making use of Weyl's theorem on Eqn. (2.63), it can be shown that the set of terms $\{c(n), n = 1, 2, \cdots\}$ is uniformly distributed on the unit circle. Estimating the autocorrelation of $c(n)$, it can also be shown that $c(n)$ is a white sequence [WG90].

To summarize, provided that either B or C in Eqn.(2.61) is irrational, the quantization error $e(n)$ is a white uniformly distributed sequence, thus justifying the assumption made in Chapter 1. This is further illustrated by the following example.

Example 6 *Let $c(n)$ denote the sequence*

$$c(n) = e^{jQn^2}, \tag{2.64}$$

with Q being a real number which is not a rational multiple of π. Eqn. (2.64)

can be rewritten as

$$c(n) = e^{j(Qn)n} = e^{j\omega_l(n)n}, \tag{2.65}$$

where $\omega_l(n) = Qn$ *represents a* local *frequency. As* n *increases, so does* $\omega_l(n)$. *In this way,* $\omega_l(n)$ *takes on values spreading between 0 and* $+\infty$, *when* Q *is positive. Also,*

$$e^{j\omega_l(n)n} = e^{j(\omega_l(n) \bmod 2\pi)n}. \tag{2.66}$$

Consequently, $a(n)$ *will have an infinite number of frequency components comprised between* 0 *and* 2π. *Moreover, because* Q *is an irrational multiple of* π, *these components will tend to be uniformly distributed on the unit circle. Fig. 2.9 shows the distribution of the first 16384 points of the sequence*

$$e^{jQn^2}, \tag{2.67}$$

with Q *arbitrarly chosen to be* $Q = 1.31926541786$.

Fig. 2.10 also shows the power spectral density of the same sequence.

In conclusion, the assumption of a white uniformly distributed quantization noise is justified for triple-loop and higher-order converters. This fact has been confirmed by the works of Chou, Wong and Gray [CWG89].

2.4 Conclusions

The present Chapter has been concerned with the extension of the results in [RL92] to higher-order Σ-Δ converter configurations. In particular, Section 2.2 has dealt with the derivation of an open-loop equivalent for multi-loop Σ-Δ converters. This was achieved by taking advantage of the fact that the quantization error function is a periodic function of the signal at the

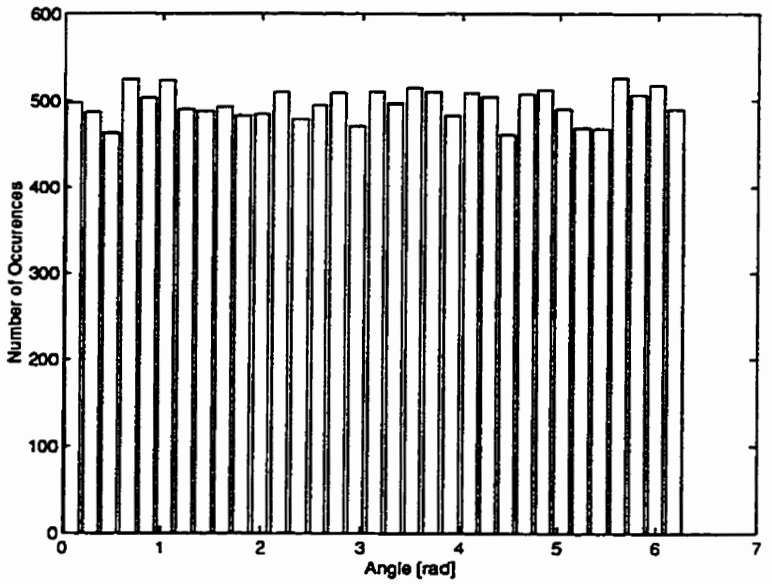

Figure 2.9: **Angular Distribution of the Sequence Given By Eqn. 2.67.**

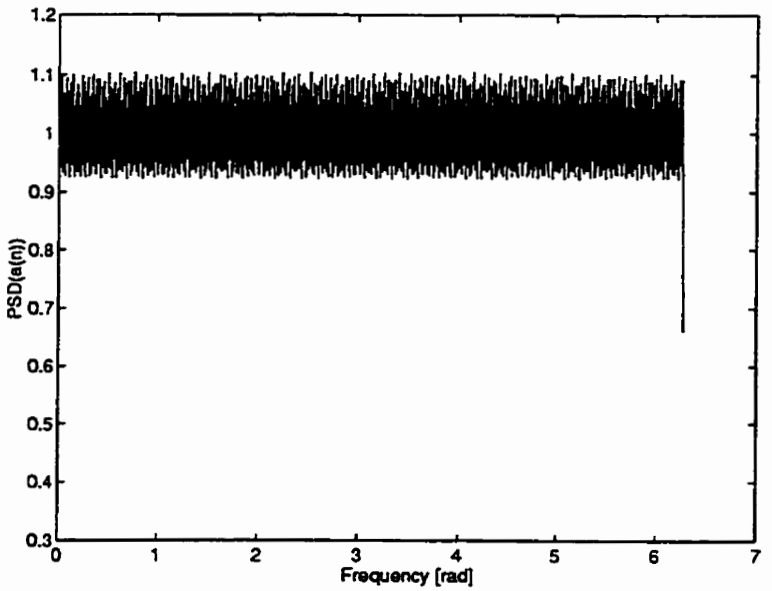

Figure 2.10: **Spectral Composition of the Sequence Given By Eqn. 2.67.**

input of the quantizer.

In Section 2.3, the results obtained in Section 2.2 has been applied to the case of a triple-loop Σ-Δ converter configuration. In Subsection 2.3.3, the result have been subsequently applied to sinusoidal input signal excitations. This procedure was facilitated by using the Fourier series expansion of the internal quantization error in conjunction with the *Jacobi-Anger* formula. A computational investigation and verification has been given in Section 2.3.4. Then, Section 2.3.5 has discussed the spectral characteristics of the quantization noise with a special emphasis on the white noise assumption made in Section 1.2.2.

Chapter 3

Design of Σ-Δ Converters

3.1 Introduction

The most important problem in electrical engineering, in general, is to develop a circuit, a system, or a device in such a manner that specific constraints are met. In the case of Σ-Δ converters, the design conditions usually include

- Sampling frequency, f_s;
- Signal characteristics (*i.e.* Bandwidth for lowpass signals or bandwidth and center frequency for bandpass signals);
- Desired resolution.

The knowledge of these specifications influence directly the order of the structure choosen. Intuitively, it appears that the lower the OSR for a given resolution, the higher the order of the structure. Otherwise, unless using the uniformly distributed white quantization noise assumption, the selection of the structure order can only be based on a *trial-and-error* procedure. Similarly, once the order of the structure is known, the topology still needs to be found.

The present chapter attempts to develop the bases for a procedure that would produce all the possible structures meeting specific criteria.

3.2 Design Methodology

3.2.1 Introduction

The proposed method using enumeration allows finding all the structures which meet a given set of criteria. The principle is to extract the important components of a Σ-Δ converter and to connect them together by external connections. Then, all the possibilities are analyzed and the realizable structures are then retained as valid structures.

3.2.2 Building Elements

The first step is to identify and extract the critical elements. These include input path, connection paths, quantizers, unit delays, multipliers, and adders as follows:

1. *Input Path*

   The input path, as one of the most obvious components, is shown in Fig. 3.1.

Figure 3.1: **Input Path.**

2. *Connection Path*

Such a path connects together the output of an element to the input of the next element. To each path is assigned a *weight* or multipling coefficient. For the present method, the weight of a path can be 1, 0, or -1 depending whether there is a connection, no connection or an inverting connection, respectively. (See Fig. 3.2)

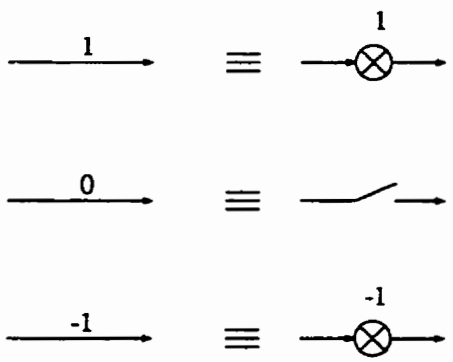

Figure 3.2: **Three Possible Connections.**

3. *Quantizer*

The most important component in a Σ-Δ converter, namely the quantizer, will be represented as shown in Fig. 3.3.

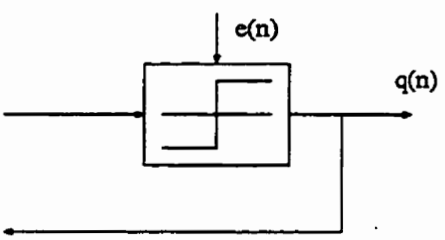

Figure 3.3: **Representation of the Quantizer.**

This representation allows the quantizer to include the feedback path.

4. *Unit delay*

   A unit delay is shown in Fig. 3.4.

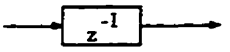

Figure 3.4: **Representation of a Unit Delay.**

5. *Multipliers*

   Figure 3.5 shows a constant coefficient multiplier.

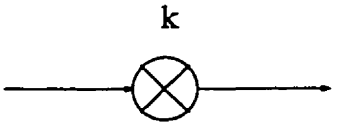

Figure 3.5: **Representation of a Multiplier of Multiplying Coefficient** k.

6. *Adders*

   Adders are considered but will not be represented explicitly. Note that two converging paths will imply an adder (see Fig. 3.6) .

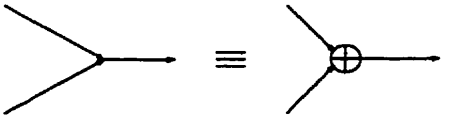

Figure 3.6: **Implicit Adder.**

The above elements are then connected together by the means of connection paths. Each node is numbered and the connection paths are defined.

By convention, a path connecting node a to node b will have a weight t_{ab}, where t_{ab} can take on the values $-1, 0$, or 1.

In the simplest case, a Σ-Δ converter contains one unit delay, one quantizer, and no multiplier. The resulting configuration is represented in Fig. 3.7.

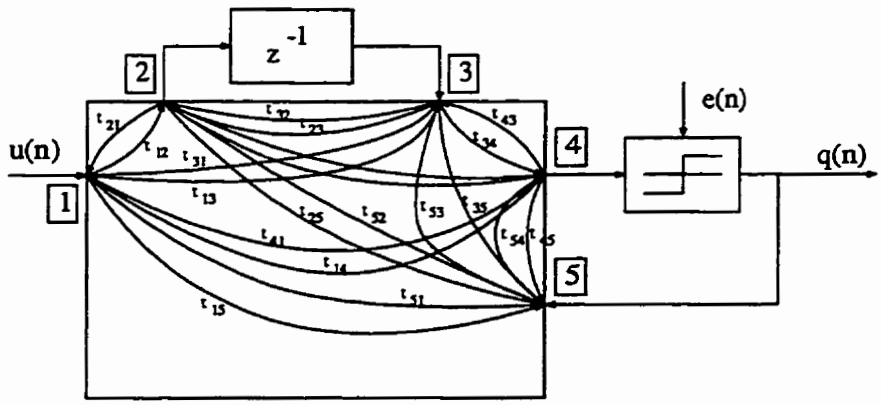

Figure 3.7: **Connections for the First-Order Σ-Δ Converter.**

Overall, 20 $(= 2(4 + 3 + 2 + 1))$ distinct connection paths can be found. Assuming each path can take three different values $\{-1, 0, 1\}$, the circuit in Fig. 3.7 has around 3.5 billion different transfer function sets. $(3^{20} \approx 3.5 \cdot 10^9)$.

In the most general case, the number of different transfer functions is given by

$$3^{(n_n-1)n_n}, \tag{3.1}$$

with n_n being the number of nodes in the circuit under consideration. Moreover, the number of nodes is given by

$$n_n = 3 + 2(n_d + n_m), \tag{3.2}$$

where n_d is the number of unit delays and n_m the number of multipliers in the structure under study.

In this way, a circuit having 2 unit delays and 2 multiplier coefficients will exhibit 11 nodes and the number of possible circuits amounts to $3^{110} = 30 \cdot 10^{51}$. Obviously, it is impossible to enumerate every single solution. Therefore, some additional design constraints have to be used in order to reduce the size of the search space.

3.3 Design Constraints

The reduction of the number of possible circuits can be obtained by introducing additional design constraints. Three different classes of constraints can be distinguished.

- *Realizability*

  Even though this is not a requirement for analog circuitry, the circuit will be designed in such a manner that no delay-free loop exists. This constraint becomes mandatory when considering a D/A converter where all the processing before the analog interface is done digitally. Practically, this condition implies that the connection t_{54} in Fig. 3.7 does not exist. Also, this condition implies that if an arbitrary path has a non-zero weight (*i.e.* $t_{ab} \in \{-1; 1\}$), the reciprocal path t_{ba} has to be have a zero weight. Also, *triangular* paths should be avoided. (*i.e.* if $t_{ab} = \pm 1$, then either $t_{ac} = 0$ or $t_{cb} = 0$ must hold so as to avoid the situation shown in Fig. 3.8).

- *Stability*

  The Bounded-Input Bounded-Output (BIBO) stability of the linear model of the Σ-Δ converter does not guarantee the stability of the non-linear converter. But, it is reasonable to assume that the Σ-Δ

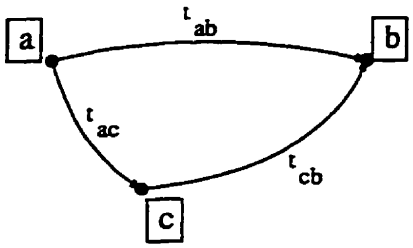

Figure 3.8: **Example of a Triangular Connection.**

converter under consideration is less likely to be unstable if its linear model is BIBO stable. BIBO stability, in the $\mathcal{Z}$-domain, is ensured if the poles of the transfer functions are located inside the unit circle.

- *Transfer Function Related Conditions*

  As will be discussed in Chapter 4, it is often convenient to have design constraints on the noise and signal transfer functions. More specifically, the number of possible circuits is reduced if these transfer functions are related to each other. The most important case is when the transfer functions are complementary in accordance with [Vai93]

$$\mathrm{NTF}(z) + \mathrm{STF}(z) = cz^{-n_0}, \tag{3.3}$$

  where n_0 is a positive integer and c is a real constant.

Other constraints or assumptions, as well as some common sense can further reduce the size of the search space.

3.4 Design of First-Order Converters

In this Section, the above design procedure is applied to the following example. The converter under consideration will contain one unit delay and

no multiplier coefficients. The corresponding configuration has already been shown in Fig. 3.7. As discussed in Section 3.2, the enumeration of all possible structures is practically impossible to perform. Therefore, additional constraints have to be given.

The first set of constraints is concerned with delay-free loops. This condition implies that

$$t_{54} = 0. \tag{3.4}$$

Also, most Σ-Δ converters include integrators implemented by the means of connecting the output of a unit delay to its input. Consequently,

$$t_{32} = 1 \quad , \quad t_{23} = 0. \tag{3.5}$$

Moreover, node 2 needs to have at least one input signal. Therefore,

$$t_{12} = \pm 1 \quad , \quad t_{52} = \pm 1,$$
$$t_{21} = 0 \quad , \quad t_{25} = 0,$$

Because $t_{12} \neq 0$ and $t_{52} \neq 0$, t_{15} must be zero to avoid a *triangular* path. Similarly, $t_{51} = 0$.

In order to simplify matters, it is assumed that there is no connection leaving nodes 2 and 4. Consequently,

$$t_{2k} = 0, k = 1, 3, 4, 5 \tag{3.6}$$

and

$$t_{4j} = 0, j = 1, 2, 3, 5. \tag{3.7}$$

Hence, the structure shown in Fig. 3.7 reduces to that shown in Fig. 3.9.

With the proposed constraints, there are only 8 remaining paths. Therefore,

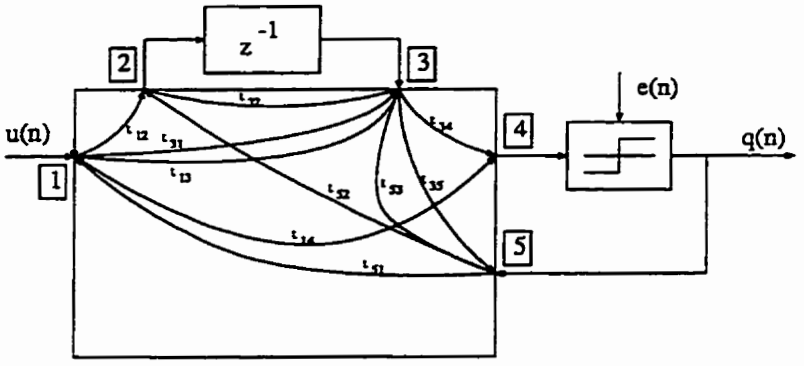

Figure 3.9: **The Simplifed Set of Connections for First-Order Example.**

the number of all possible circuits is reduced to

$$3^8 = 6561; \tag{3.8}$$

which indicates a dramatic change from the 3.5 billion different possibilities obtained before.

In order to avoid delay-free loops, the coefficients must satisfy the conditions

$$\begin{cases} t_{35}t_{53} = 0 \\ t_{34}t_{53} = 0. \end{cases} \tag{3.9}$$

Moreover, further *triangular* paths are avoided if the condition

$$t_{35}t_{52} = 0 \tag{3.10}$$

is satisfied.

The next step consists in running a symbolic analysis program written by Arthur Fuller, a member of Dr. Nowrouzian's research group at the University of Alberta, to obtain the transfer functions realized by the structure.

These can be found to be

$$\mathrm{STF}(z) = \frac{1 - t_{32}z^{-1}}{1 + (-t_{32} - t_{34}t_{52})z^{-1}}, \tag{3.11}$$

and

$$\mathrm{NTF}(z) = \frac{(t_{13}t_{34} + t_{14}) + (t_{12}t_{34} - t_{14})z^{-1}}{1 + (-t_{32} - t_{34}t_{52})z^{-1}}, \tag{3.12}$$

At this point, it can be observed that STF(z) and NTF(z) share the same denominator.

The second design constraint dictates that the poles of NTF(z) must lie inside the unit circle. From Eqn. (3.11) it appears that the real unique pole of NTF(z) is located at the point

$$z = -t_{32} - t_{34}t_{52}. \tag{3.13}$$

In order for the zeros of $D(z)$ to lie inside the unit circle, the condition

$$|t_{32} + t_{34}t_{52}| < 1 \tag{3.14}$$

must be satisfied. Because the coefficients t_{32}, t_{34}, and t_{52} are restricted to integer values, the equality

$$t_{32} + t_{34}t_{52} = 0, \tag{3.15}$$

is the only one which satisfies Eqn. (3.14).

Using Eqn. (3.15) in Eqns. (3.11) and (3.12) gives

$$\mathrm{STF}(z) = (t_{13}t_{34} + t_{14}) + (t_{12}t_{34} - t_{14})z^{-1}, \tag{3.16}$$

and

$$\mathrm{NTF(z)} = 1 - t_{32}z^{-1}. \tag{3.17}$$

The third design constraint is concerned with the relationship between STF(z) and NTF(z). Combining Eqns. (3.16) and (3.17) into Eqn. (3.3) yields

$$1 - t_{32}z^{-1} + (t_{13}t_{34} + t_{14}) + (t_{12}t_{34} - t_{14})z^{-1} = cz^{-n_0}, \tag{3.18}$$

where $n_0 \in \{0, 1\}$.

At his point, two cases can be distinguished: $n_0 = 0$ and $n_0 = 1$. In the present thesis, the study will be limited to the case of $n_0 = 0$. In this case, Eqn. (3.18) yields the conditions

$$1 + (t_{13}t_{34} + t_{14}) = c \tag{3.19}$$

$$-t_{32} + (t_{12}t_{34} - t_{14}) = 0, \tag{3.20}$$

where c is an arbitray real constant.

From Eqns. (3.19) and (3.20), two particular cases arise.

3.4.1 Case-1 : $c = 1$

The special case where $c = 1$ is of particular interest. The case $c = 1$ along with Eqn. (3.19) imply that

$$t_{13}t_{34} = -t_{14}. \tag{3.21}$$

Also, Eqn. (3.20) imply that at least one of the three terms t_{32}, $t_{12}t_{34}$, and t_{14} has to be zero. By choosing $t_{14} = 0$, Eqn. (3.20) yields

$$\text{From Eqn. (3.20)} \quad : \quad t_{32} = t_{12}t_{34} \tag{3.22}$$

$$\text{From Eqn. (3.21)} \quad : \quad t_{13}t_{34} = 0. \tag{3.23}$$

Moreover, choosing

$$t_{32} = 1, \tag{3.24}$$

Eqn. (3.22) implies that

$$t_{12}t_{34} = 1. \tag{3.25}$$

Also, combining Eqns. (3.23) and (3.25) implies that

$$t_{13} = 0. \tag{3.26}$$

Moreover, choosing

$$t_{34} = 1 \tag{3.27}$$

and using Eqn. (3.25) implies that

$$t_{12} = 1. \tag{3.28}$$

Combining Eqns. (3.15), (3.24), and (3.27) gives

$$t_{52} = -1. \tag{3.29}$$

Combining Eqn. (3.9) and (3.27) gives $t_{53} = 0$. Finally, replacing t_{52} in

Eqn. (3.10) by its value given in Eqn. (3.29) implies

$$t_{35} = 0. \tag{3.30}$$

To summarize, the coefficients given in Table 3.1 are found to satisfy the conditions given by Eqns. (3.19) and (3.20).

$t_{12} = 1$	$t_{31} = 0$	$t_{52} = -1$
$t_{13} = 0$	$t_{32} = 1$	$t_{53} = 0$
$t_{14} = 0$	$t_{34} = 1$	
	$t_{35} = 0$	

Table 3.1: **Value of the Coefficients for the case $c = 1$.**

The configuration given by Table 3.1 corresponds to the conventional first-order Σ-Δ converter shown in Fig. 3.10. Combining the transfer functions

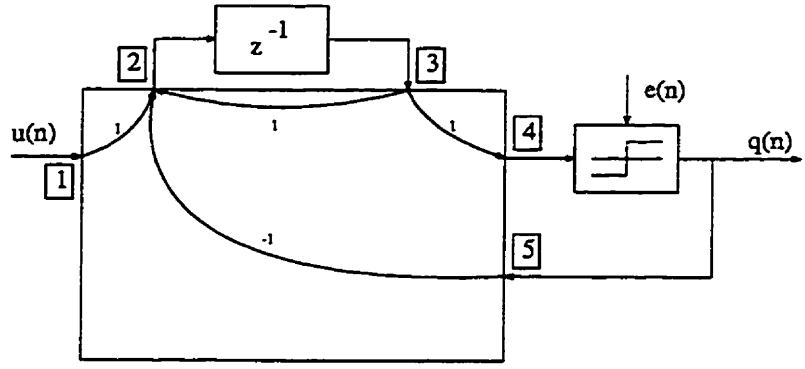

Figure 3.10: **Conventional First-Order Σ-Δ Converter Obtained Through Design.**

given by Eqns. (3.11) and (3.12) and the results given in Table 3.1 give

$$\mathrm{STF}(z) = 0 + z^{-1}, \tag{3.31}$$

and

$$\mathrm{NTF}(z) = 1 - z^{-1}. \tag{3.32}$$

3.4.2 Case-2: $c = 2$

In this case, Equation (3.19) implies that

$$t_{13}t_{34} + t_{14} = 1. \tag{3.33}$$

Using similar assumptions as before, the coefficients in Table 3.2 can be found to satisfy the design constraints.

$t_{12} = 1$	$t_{31} = 0$	$t_{52} = -1$
$t_{13} = 1$	$t_{32} = 1$	$t_{53} = 0$
$t_{14} = 0$	$t_{34} = 1$	
	$t_{35} = 0$	

Table 3.2: **Value of the Coefficients for the case $c = 2$.**

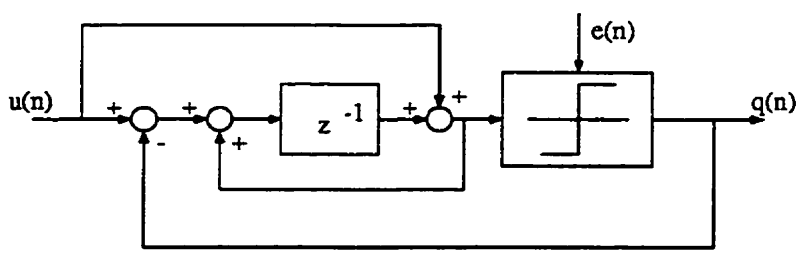

Figure 3.11: **Σ-Δ Converter Configuration (With $c = 2$).**

The corresponding circuit is shown in Fig. 3.11. The transfer functions are found to be

$$\mathrm{STF}(z) = 1 + z^{-1}, \tag{3.34}$$

and

$$\mathrm{NTF}(z) = 1 - z^{-1}. \tag{3.35}$$

and are shown in Fig. 3.12. In this case, the signal transfer function is not

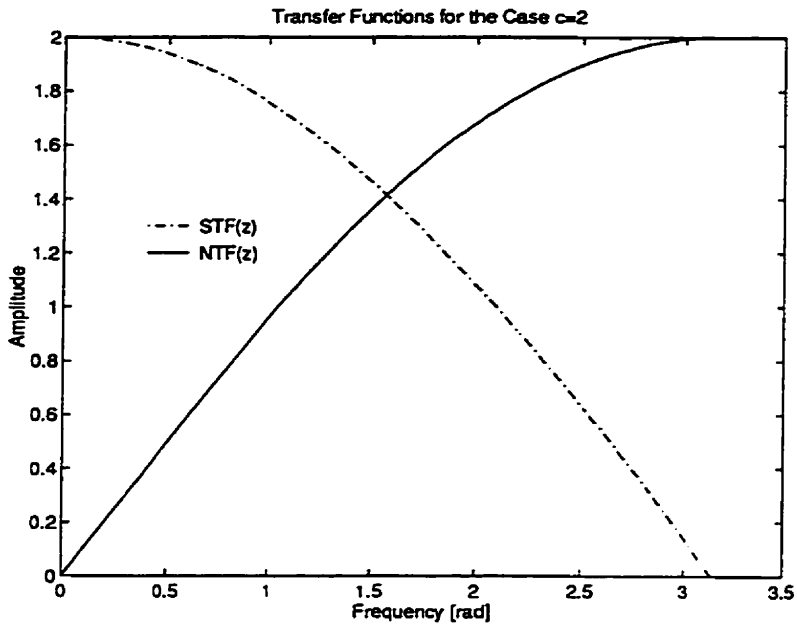

Figure 3.12: **Transfer Functions for the Σ-Δ Converter Configuration (With $c = 2$).**

of an allpass nature as it is in the conventional Σ-Δ converter presented in Section 1.2.5. However, at the point where $\mathrm{NTF}(z) = 0$ (*i.e.* at low frequencies), $|\mathrm{STF}(z)| \approx 2$ and its derivative with respect to the frequency is close to zero. Because high oversampling ratios are usually used, $\mathrm{STF}(z)$ can be considered as constant in the input signal frequency band.

An analysis of the structure shows that its performance is identical to that of the conventional first-order structure. A plot of the SQNR as a function of the input signal amplitude shows an identical maximum SQNR. Simulation results shown in Fig. 3.13 are compared with the expected SQNR estimated using the linear model approximation and with the model proposed by Candy and Benjamin [CB81]. The 0dB level is defined to be the level that saturates the Σ-Δ converter (see Section 1.2.7).

From Fig. 3.11, it can be observed that the new Σ-Δ converter configu-

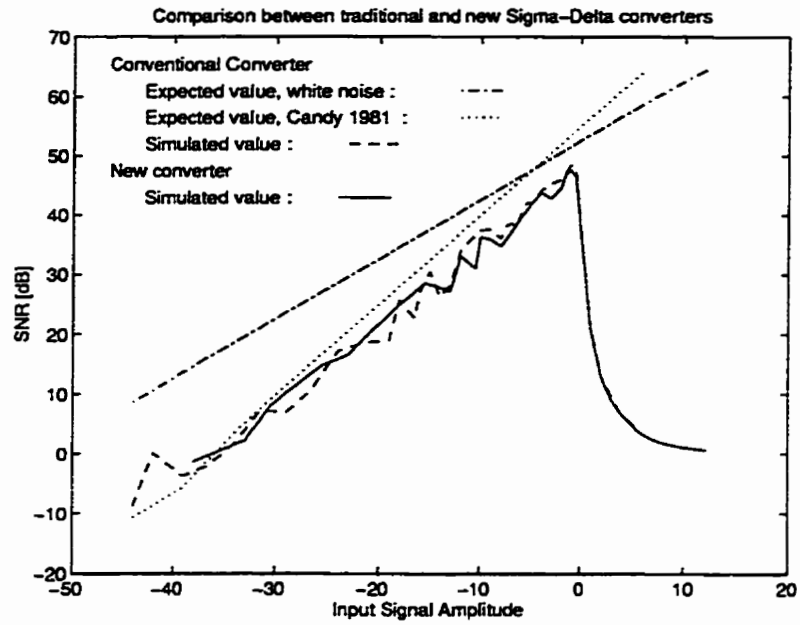

Figure 3.13: **Performance Comparison of the Conventional and the Σ-Δ Converter in Fig. 3.11.**

ration only differs from the conventional first-order configuration by the way the integrator is implemented. Conventional Σ-Δ converters use the so-called Euler integrator (Fig. 3.14) having for transfer function

$$H_{\text{Euler}}(z) = \frac{z^{-1}}{1 - z^{-1}}. \tag{3.36}$$

The proposed new Σ-Δ converter, on the other hand, uses a modified version of the bilinear-LDI[1] integrator shown in Fig. 3.15. The transfer function associated with the integrator shown in Fig. 3.15 is

$$H_{\text{LDI}}(z) = \frac{1 + z^{-1}}{1 - z^{-1}}. \tag{3.37}$$

[1]LDI stands for lossless discrete integrator.

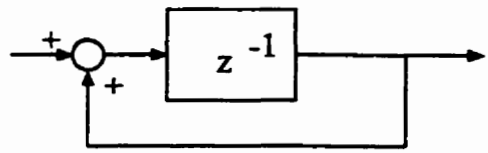

Figure 3.14: **First-Order Euler Integrator.**

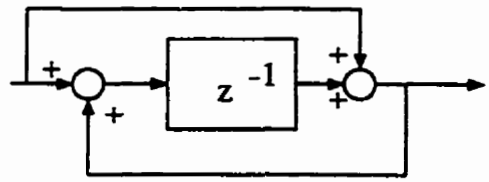

Figure 3.15: **First-Order Bilinear-LDI Integrator.**

Bilinear-LDI integrators are commonly used in ladder filters and are attractive as they preserve the low sensitivity features of such filters. However, the bilinear-LDI based Σ-Δ converter configuration has not shown any substantial improvement over the conventional Σ-Δ converter (which uses the Euler integrator).

3.5 Highpass Σ-Δ Converters

Using the technique proposed in Section 3.2, highpass Σ-Δ converter configurations can also be designed. It must be pointed out that such converters are not very attractive because of the increase in cost associated with the corresponding antialiasing and decimation.

Selecting the multiplier coefficient values in the converter configuration shown in Fig. 3.11 as given in Table 3.3, generates a highpass Σ-Δ converter. The resulting converter configuration is shown in Fig. 3.16. A spectral analysis of the output signal $Q(z)$ under a sinusoidal excitation proves that the noise power spectral density of this converter is indeed of lowpass nature, being zero at the frequency $\omega = \pi$ (see Fig. 3.17).

$t_{12} = -1$	$t_{31} = 0$	$t_{52} = 1$
$t_{13} = 0$	$t_{32} = -1$	$t_{53} = 0$
$t_{14} = 0$	$t_{34} = 1$	
	$t_{35} = 0$	

Table 3.3: **Value of the High-pass First-Order Σ-Δ Converter.**

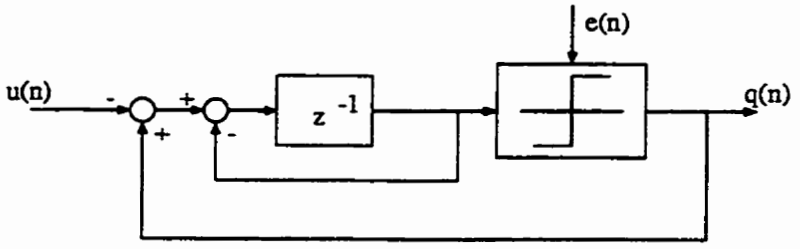

Figure 3.16: **First-Order Highpass Σ-Δ Converter.**

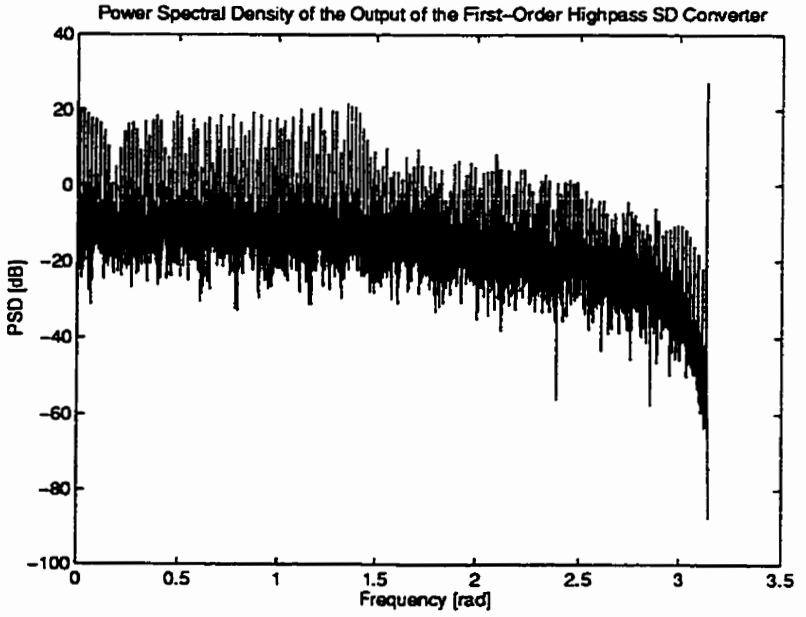

Figure 3.17: **Power Spectral Density of the First-Order Highpass Σ-Δ Converter.**

3.6 Conclusions

This chapter was concerned with the development of a new design technique for Σ-Δ converters. This technique is based on enumeration. However, the number of possible solutions grows exponentially with the number of components in the structure under consideration. As such, a first-order converter requires close to 6.5 billion iterations to generate all possible solutions. Therefore, additional design constraints have to be devised in order to reduce the complexity of the search space. These constraints are of three different categories.

- Realizability constraints,
- Stability constraints, and
- Transfer function related constraints.

Moreover, some common sense and personal preferences can be considered to further decrease the size of the set of possible solutions.

Such considerations have successfully been applied to the design of first-order converters. Using this new technique, the conventional first-order Σ-Δ converter configuration has been rediscovered. As well, a new structure based on bilinear-LDI integrators instead of bilinear integrators has been discovered. Finally, the concept of highpass Σ-Δ converter has briefly been introduced.

The proposed new design technique may prove more useful when applied to higher order Σ-Δ converters. However, the complexity of the related transfer functions and the number of possible solutions may reduce the practicality of the proposed technique.

Chapter 4

Bandpass Sigma-Delta Conversion

4.1 Introduction

Conventionally, Σ-Δ converters are designed such that the quantization noise transfer function, NTF(z), has a highpass characteristic while the signal transfer function, STF(z), has a lowpass characteristic. The main drawback of lowpass Σ-Δ converters is that any increase in the performance, as measured by the SQNR for a given structure requires an increase in the sampling frequency. However, such an increase is not always possible due to the technology limitations.

In 1989, Schreier and Snelgrove [SS89] developed a new methodology for Σ-Δ converter design, where the converter (called bandpass Σ-Δ converter) is designed such that its quantization noise is small around a mid-band frequency, away from DC. This is achieved by moving the zeros of the quantization-noise transfer function away from DC to locations close to the desired mid-band frequency on the unit circle. The resulting bandpass

Σ-Δ converters give rise to low quantization noise around the mid-band frequency. Schreier and Snelgrove also showed that the oversampling ratio is a function of the passband width instead of the signal frequency, thus relaxing the constraints on the sampling frequency.

This chapter reviews the existing design techniques for bandpass Σ-Δ A/D conversion and presents a set of comparison criteria. A new Σ-Δ converter configuration based on existing structures is presented along with its corresponding design procedure.

Section 4.2 introduces some definitions and general considerations related to the transfer functions. Some special cases are discussed and the important notion of transfer function complementarity is introduced.

Section 4.3 reviews the design specifications relating to the noise transfer functions. The general form of the noise transfer function is then derived. This is followed by the discussion of issues such as the order of both the noise and signal transfer functions. A formula for the estimation of the performance of the converter based on its noise transfer function concludes this section.

Section 4.4 applies the results of Section 4.3 to the design of transfer functions satisfying a set of design specifications as an example.

The resulting transfer functions are applied to the design of a cascade-of-integrators Σ-Δ converter configuration in Section 4.5. The resulting design is then investigated and a switched-capacitor implementation of the design is discussed.

In Section 4.6, the design (based on the results of Section 4.4) of a cascade-of-resonators is investigated. The procedure parallels the procedure used in Section 4.5.

Section 4.7 presents a comparative discussion of the structures synthesized

in Sections 4.5 and 4.6.

Finally, Section 4.8 introduces a new Σ-Δ converter configuration which combines the best features of the structures synthesized in Sections 4.5 and 4.6. Its switched-capacitor implementation is also considered.

4.2 General Considerations

Generally, a single quantizer Σ-Δ A/D converter configuration can be represented as shown in Fig. 4.1, where $U(z)$ represents the input signal, $E(z)$ represents the quantization error and $Q(z)$ represents the quantized output signal. Also, $G(z)$ and $H(z)$ are two rational transfer functions in z.

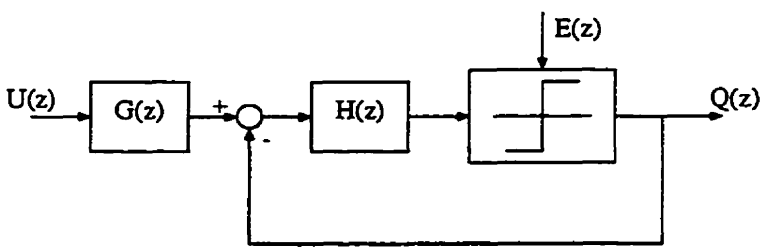

Figure 4.1: **A Generic Σ-Δ A/D Converter.**

By inspection of Fig. 4.1, the relationship between the signals $U(z)$ and $E(z)$, and the output signal $Q(z)$ can be found to be

$$Q(z) = G(z)\frac{H(z)}{1-H(z)}U(z) + \frac{1}{1-H(z)}E(z). \tag{4.1}$$

The signal and the noise transfer functions therefore correspond to

$$\mathrm{STF}(z) = \frac{G(z)H(z)}{1-H(z)}, \tag{4.2}$$

and

$$\mathrm{NTF}(z) = \frac{1}{1 - H(z)}, \tag{4.3}$$

respectively.

The transfer function $H(z)$ is a rational function in z and can be written

$$H(z) = \frac{N_H(z)}{D_H(z)}, \tag{4.4}$$

where $N_H(z)$ and $D_H(z)$ are two polynomials in z which represent the numerator and the denominator of $H(z)$, respectively. In this way, Eqns. (4.2) and (4.3) can be rewritten

$$\mathrm{STF}(z) = G(z)\frac{N_H(z)}{D_H(z) - N_H(z)}, \tag{4.5}$$

and

$$\mathrm{NTF}(z) = \frac{D_H(z)}{D_H(z) - N_H(z)}. \tag{4.6}$$

At this point, two special cases can be distinguished.

Firstly, if the denominator of $G(z)$ is unity (*i.e.* if $G(z)$ itself is a polynomial instead of being a rational transfer function in z), then it follows from Eqns. (4.5) and (4.6) that $\mathrm{STF}(z)$ and $\mathrm{NTF}(z)$ share the same denominator. In this case, the polynomials $N(z)$, $S(z)$ and $D(z)$ are introduced in accordance with

$$\mathrm{NTF}(z) = \frac{N(z)}{D(z)} = \frac{D_H(z)}{D_H(z) - N_H(z)}, \tag{4.7}$$

and

$$\mathrm{STF}(z) = \frac{S(z)}{D(z)} = G(z)\frac{N_H(z)}{D_H(z) - N_H(z)}. \tag{4.8}$$

Secondly, if $G(z) = 1$, then $\mathrm{STF}(z)$ and $\mathrm{NTF}(z)$ are related to each other

in accordance with

$$\mathrm{STF}(z) = \mathrm{NTF}(z) - 1. \tag{4.9}$$

Two transfer functions respecting Eqn. (4.9) will be said to be complementary.

Also, from Eqns (4.7) and (4.8), the relationships

$$S(z) = N_H(z), \tag{4.10}$$

$$N(z) = D_H(z), \tag{4.11}$$

and

$$D(z) = D_H(z) - N_H(z) \tag{4.12}$$

hold.

Equivalently, $H(z)$ can be represented as

$$H(z) = \frac{S(z)}{N(z)}, \tag{4.13}$$

provided that

$$G(z) = 1. \tag{4.14}$$

Eqn. (4.9) implies that in the vicinity of the zeros of $\mathrm{NTF}(z)$, the magnitude of $\mathrm{STF}(z)$ is approximately unity. Therefore, a Σ-Δ converter such as the one shown in Fig. 4.1 ensures that the signal transfer function will have a minimal effect on the input signal in the region where the quantization noise is minimized. Eqn. (4.9) also means that there is only a need to design an acceptable noise transfer function, the signal transfer function being fixed by Eqn. (4.9).

4.3 Transfer Function Design

4.3.1 Design Specifications

In the design of bandpass Σ-Δ A/D converters, the design specifications usually include the specifications given in Table 4.1. These specifications are

Center frequency of the signal	f_c
Bandwidth	BW
Sampling Frequency	f_s
SQNR to achieve (usually in dB)	SQNR_{dB}

Table 4.1: **General Design Specifications for a Bandpass Σ-Δ Converter**

also shown in Fig. 4.2.

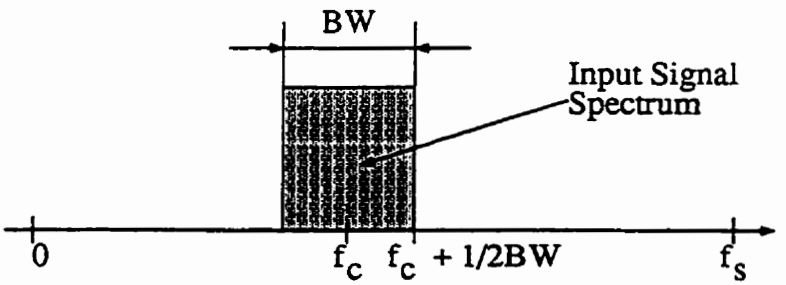

Figure 4.2: **Graphical Representation of the Specifications in Table 4.1.**

In the case of bandpass Σ-Δ conversion, it has been shown [SS89] that the oversampling ratio (OSR) becomes

$$\text{OSR} = \frac{f_s}{2\text{BW}}. \tag{4.15}$$

The advantage is that a higher OSR can be achieved by a bandpass Σ-Δ converter when compared to lowpass converters.

4.3.2 Optimization Constraints

Because there is no readily available technique for the transfer function design, these have to be obtained by optimization. As shown in Section 4.2, if a suitable structure is chosen, STF(z) and NTF(z) will be complementary in accordance with Eqn. (4.9). Consequently, only the problem of the design of NTF(z) will be considered.

According to Jantzi *et al.* [JOS94], the noise transfer function must satisfy three design constraints. Firstly, the inband attenuation must be as large as possible, *i.e.*

$$|\mathrm{NTF}(z)| = 0. \tag{4.16}$$

Secondly, the Σ-Δ converter must be BIBO stable. It has been found empirically that a Σ-Δ converter is less likely to become unstable if the out-of-band gain of NTF(z) is less than 2 (6dB) [Lee87]. In order to keep a security margin, NTF(z) will be constrained to

$$|\mathrm{NTF}(z)| \leq 1.6 \quad (4\mathrm{dB}). \tag{4.17}$$

Thirdly, in order to have a realizable circuit, NTF(z) should not exhibit a delay free path. Equivalently, the first sample of the impulse response of NTF(z) should be unity. Therefore, the relationship

$$\lim_{z \to \infty} \mathrm{NTF}(z) = 1, \tag{4.18}$$

must hold true.

If these constraints are satisfied, the designed noise transfer function should exhibit a reasonable margin against instability.

4.3.3 Structure of the Noise Transfer Function

Because the zeros of NTF(z) are not supposed to be at $z = 1$ (DC), it becomes obvious that they will appear in complex conjugate pairs[1]. Therefore, the order of $N(z)$ (the numerator of NTF(z)) has to be even. Also, in order to ensure a maximal attenuation of the quantization noise, the zeros of $N(z)$ have to be located on the unit circle. Denoting by ω_{0k} the frequency of the the k-th zero of $N(z)$ and by $2N$ its order, $N(z)$ can be expressed as

$$N(z) = \prod_{k=1}^{N} \left(1 - 2\cos\omega_{0k} z^{-1} + z^{-2}\right). \tag{4.19}$$

The poles of NTF(z), on the other hand, are constrained to remain inside the unit circle in order to ensure the BIBO stability of the converter. Moreover, in order to achieve a feasible noise transfer function, the order of the denominator of NTF(z) has to be less than or equal to the order of $N(z)$. Also, to ensure a successful design, the largest possible number of degrees of freedom is desired. Therefore, the order of the polynomial $D(z)$ will be set to the largest possible value, $2N$. Denoting by ω_{pk} the frequency of the k-th zero of $D(z)$ and by p_k the distance between the k-th zero of $D(z)$ and the point $z = 0 + j0$, $D(z)$ can be written

$$D(z) = \prod_{k=1}^{N} \left(1 - 2p_k \cos\omega_{pk} z^{-1} + p_k^2 z^{-2}\right). \tag{4.20}$$

[1]With the notable exception of $z = -1$ which corresponds to the case of a highpass Σ-Δ converter

Combining Eqns. (4.19) and (4.20) into Eqn. (4.7) gives the desired form of NTF(z),

$$\mathrm{NTF}(z) = \frac{\prod_{k=1}^{N}(1 - 2\cos\omega_{0k}z^{-1} + z^{-2})}{\prod_{k=1}^{N}(1 - 2p_k\cos\omega_{pk}z^{-1} + p_k^2 z^{-2})}. \tag{4.21}$$

At this point, the following lemma can be given.

Lemma 4 *The transfer function*

$$NTF(z) = \frac{\prod_{k=1}^{N}(1 - 2\cos\omega_{0k}z^{-1} + z^{-2})}{\prod_{k=1}^{N}(1 - 2p_k\cos\omega_{pk}z^{-1} + p_k^2 z^{-2})}, \tag{4.22}$$

where $2N$ denotes the order of the transfer function, ω_{0k} represents the frequency of the k-th zero of $NTF(z)$, ω_{pk} is the frequency of the k-th pole of $NTF(z)$ and p_k represents the distance between this pole and the point $z = 0 + j0$, satisfies the realizability condition

$$\lim_{z\to\infty} NTF(z) = 1. \tag{4.23}$$

Proof : By working out the limit

$$\lim_{z\to\infty} \frac{\prod_{k=1}^{N}(1 - 2\cos\omega_{0k}z^{-1} + z^{-2})}{\prod_{k=1}^{N}(1 - 2p_k\cos\omega_{pk}z^{-1} + p_k^2 z^{-2})}. \tag{4.24}$$

Assuming that the condition $z \neq 0$ holds, the substitution

$$x = z^{-1} \tag{4.25}$$

can be done. In this way, Eqn. (4.24) becomes

$$\lim_{x\to 0} \frac{\prod_{k=1}^{N}(1 - 2\cos\omega_{0k}x + x^2)}{\prod_{k=1}^{N}(1 - 2p_k\cos\omega_{pk}x + p_k^2 x^2)}. \tag{4.26}$$

If $x = 0$ is not a pole of NTF(z), the limit exists and the relationship

$$\lim_{x \to 0} \frac{\prod_{k=1}^{N} (1 - 2\cos\omega_{0k}x + x^2)}{\prod_{k=1}^{N} (1 - 2p_k \cos\omega_{pk}x + p_k^2 x^2)} = 1. \tag{4.27}$$

holds true. This completes the proof of the lemma. *q.e.d.*

A direct consequence of Lemma 4 is that selecting a noise transfer function of the form given by Eqn. (4.21) ensures that the corresponding Σ-Δ converter is realizable.

4.3.4 Order of the Signal and Noise Transfer Functions

The selection of the order of the signal and noise transfer functions cannot be perfomed in a deterministic manner. However, analysis of a linear model [SS89] suggests that the SQNR increases by $3(2N + 3)$dB per each doubling of OSR, with $2N$ being the order of the transfer function of the Σ-Δ converter configuration under consideration. Non-linear simulations of several bandpass Σ-Δ converter configurations confirmed this expectation [JSS91]. Consequently, the order of the noise transfer function must be chosen based on previous knowledge of similar situations.

4.3.5 Optimization of the Noise Transfer Function

At this point, the optimization of NTF(z) can be performed using commercially available software such as MATLAB, the optimization constraints being given by Eqns. (4.16) and (4.17).

If the transfer functions STF(z) and NTF(z) are chosen in accordance with Eqn. (4.9) (*i.e.* they are complementary), there is no need to perform the optimization of STF(z).

4.3.6 Estimation of the Performance of the Optimized Noise Transfer Function

This method was proposed by Jantzi [Jan92] and is based on a linear model.

In the case of a sinusoidal input signal, the final form of the SQNR can be found to be [JSF93, Eqn.(8)]

$$\mathrm{SQNR}_{dB} = 10\log\frac{\sigma_x^2}{\sigma_{es}^2} = 20\log\frac{2A}{\Delta} + 4.77 - 20\log\overline{\mathrm{NTF}(f)} + 10\log\mathrm{OSR}, \tag{4.28}$$

where A being the amplitude of the input sinusoid and where $\overline{\mathrm{NTF}(f)}$ is the average attenuation of the noise transfer function defined as

$$\overline{\mathrm{NTF}(f)} = \frac{1}{f_h - f_l}\int_{f_l}^{f_h} |\mathrm{NTF}(f)|df. \tag{4.29}$$

Also, f_l and f_h correspond to the lowest and the highest frequency in the signal frequency band, respectively and are defined in accordance with

$$f_l = f_c - 1/2\mathrm{BW} \tag{4.30}$$

and

$$f_h = f_c + 1/2\mathrm{BW} \tag{4.31}$$

4.4 Synthesis of the Noise Transfer Function

4.4.1 Introduction

A number of Σ-Δ converter configurations have been published. Among them, two are of particular interest: the cascade-of-integrators [LS87] and the cascade-of-integrators (see *e.g.* [JSF93]). This section uses these two

structures for the design of a bandpass Σ-Δ converter respecting a set of given design constraints as an example.

4.4.2 A Practical Example

Two different structures will be designed to implement the specifications given in Table 4.2.

Sampling frequency	$f_s = 15$ MHz
Center frequency	$f_c = 380$ kHz
Bandwidth	$BW = 100$ kHz
SQNR to achieve	$\text{SQNR}_{dB} = 70$ dB

Table 4.2: **Specifications for the Design of a Bandpass Sigma-Delta Converter.**

Based on Table 4.2 and after using Eqn. (4.15), the oversampling ratio can be found to be

$$\text{OSR} = \frac{f_s}{2\text{BW}} = 75. \tag{4.32}$$

Note that if a lowpass Σ-Δ converter were to be used in this situation, the OSR would be approximately 16.

Using Eqn. (4.28) and with an input signal having for amplitude $A = \Delta/2$, the average inband attenuation of $\text{NTF}(z)$ must satisfy the constraint

$$\overline{\text{NTF}(z)} \leq -47\text{dB}. \tag{4.33}$$

After some iterations, it appears that the order of $\text{NTF}(f)$ must be at least 4. The optimization process gave for the noise transfer function

$$\text{NTF}(z) = \frac{N(z)}{D(z)} = \frac{1 - 3.9519z^{-1} + 5.9043z^{-2} - 3.9519z^{-3} + z^{-4}}{1 - 3.0492z^{-1} + 3.5971z^{-2} - 1.9240z^{-3} + 0.3901z^{-4}} \tag{4.34}$$

and for the corresponding complementary signal transfer function

$$\mathrm{STF}(z) = \frac{S(z)}{D(s)} = \frac{0 - 0.9026z^{-1} + 2.3072z^{-2} - 2.0279z^{-3} + 0.6099z^{-4}}{1 - 3.0492z^{-1} + 3.5971z^{-2} - 1.9240z^{-3} + 0.3901z^{-4}}. \tag{4.35}$$

In the present case, the zeros of NTF(z) can be found to be located at the frequencies f_{01} and f_{02} given by

$$\omega_{01} = 0.14419 \quad (f_{01} = 344.24\mathrm{kHz}) \tag{4.36}$$

$$\omega_{02} = 0.16567 \quad (f_{02} = 395.51\mathrm{kHz}). \tag{4.37}$$

Throughout this chapter, the polynomial $N(z)$ will be represented in its most general form as

$$N(z) = 1 + n_1 z^{-1} + n_2 z^{-2} + \cdots + n_{2N} z^{-2N}, \tag{4.38}$$

with $2N$ being the order of the transfer function. Also, Eqn. (4.38) can be written in the matricial format as

$$N(z) = \mathcal{Z}_{1,2N+1} \mathcal{N}_{2N+1,1}, \tag{4.39}$$

where

$$\mathcal{Z} = \begin{bmatrix} z^0 & z^{-1} & z^{-2} & \cdots & z^{-2N} \end{bmatrix}, \tag{4.40}$$

and

$$\mathcal{N} = \begin{bmatrix} 1 \\ n_1 \\ n_2 \\ \vdots \\ n_{2N} \end{bmatrix}. \tag{4.41}$$

Similarly, $S(z)$ can be represented as

$$S(z) = \begin{bmatrix} z^0 & z^{-1} & z^{-2} & \cdots & z^{-2N} \end{bmatrix} \begin{bmatrix} 0 \\ s_1 \\ s_2 \\ \vdots \\ s_{2N} \end{bmatrix} \tag{4.42}$$

$$= \mathcal{Z} \cdot \mathcal{S}. \tag{4.43}$$

Finally, $D(z)$ can be represented as

$$D(z) = \begin{bmatrix} z^0 & z^{-1} & z^{-2} & \cdots & z^{-2N} \end{bmatrix} \begin{bmatrix} 1 \\ d_1 \\ d_2 \\ \vdots \\ d_{2N} \end{bmatrix} \tag{4.44}$$

$$= \mathcal{Z} \cdot \mathcal{D}. \tag{4.45}$$

Fig. 4.3 shows the magnitude/frequency response of the signal- and noise-transfer function over the whole spectrum ($f \in [0; f_s/2]$) and Fig. 4.4 shows a close-up of the magnitude frequency response of STF(z) and NTF(z) in the vicinity of the signal frequency band.

4.4.3 Estimated Performance of the Designed Converter

An analysis of NTF(z) shows that the average in-band attenuation defined by Eqn. (4.29) is

$$\overline{\text{NTF}(z)} = -60.9\text{dB}. \tag{4.46}$$

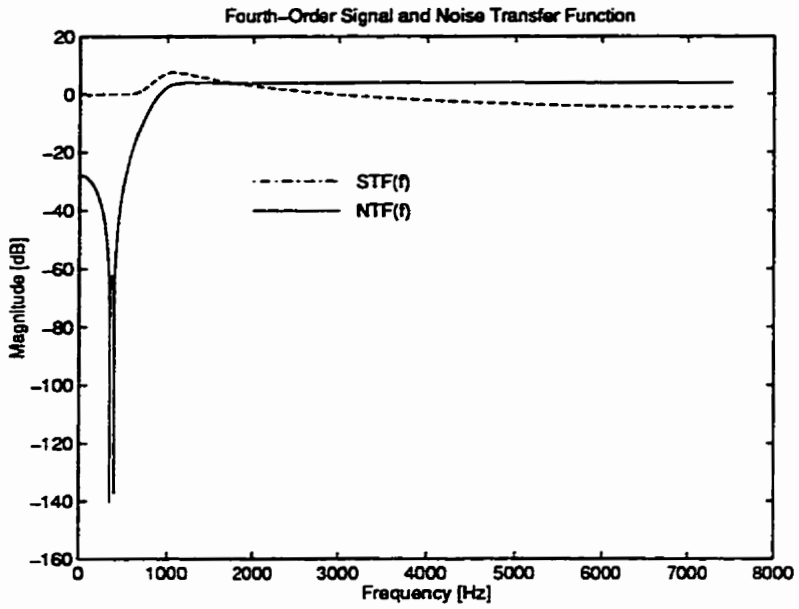

Figure 4.3: **Magnitude/Frequency Response of NTF(z) and STF(z) given by Eqns. (4.34) and (4.35).**

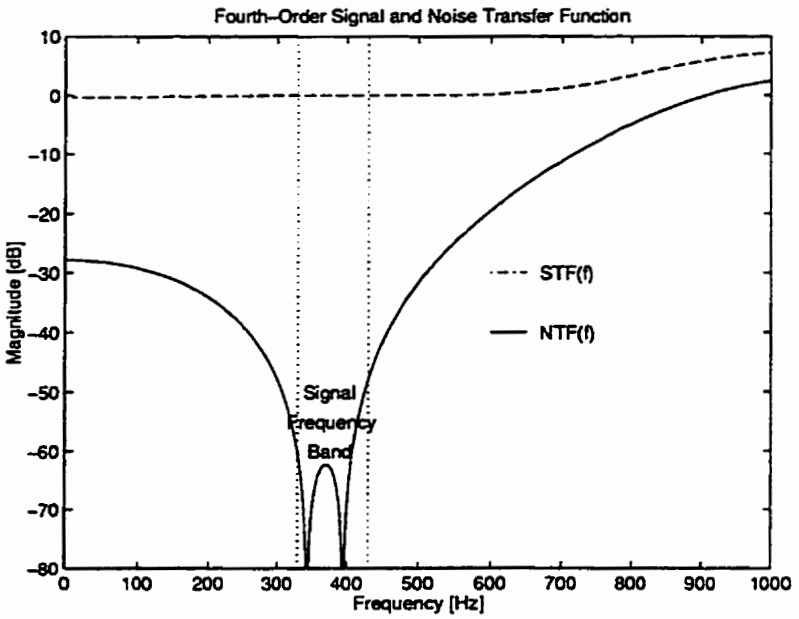

Figure 4.4: **Close-up of the Magnitude/Frequency Response of NTF(z) and STF(z) given by Eqns. (4.34) and (4.35) in the Signal Frequency Band.**

Using Eqn. (4.28), the estimated SQNR with an input sinusoid of amplitude $A = \Delta/4$ is

$$\mathrm{SQNR}_{dB} = 78.5\mathrm{dB}. \tag{4.47}$$

Therefore, the proposed transfer functions should result in a Σ-Δ converter configuration that fulfills the design specifications given in Table 4.2.

4.5 Synthesis of the Cascade-of-Integrators Σ-Δ Converter Configuration

4.5.1 The Structure

The cascade-of-integrators Σ-Δ converter configuration has first been proposed by Lee and Sodini in 1987 [LS87] in an attempt to improve the noise shaping characteristics of lowpass Σ-Δ converters.

The fourth-order configuration of the cascade-of-integrators structure is given in Fig. 4.5

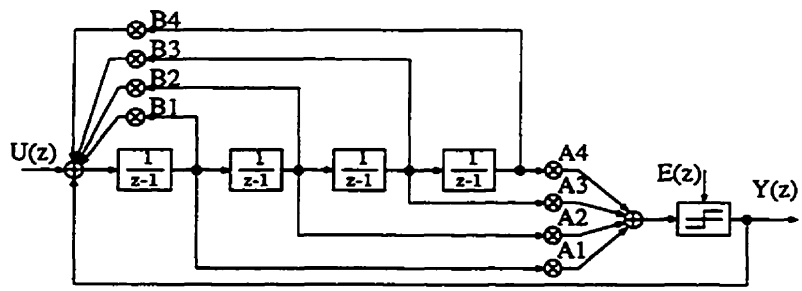

Figure 4.5: **The Fourth-Order Cascade-of-Integrators Σ-Δ Converter Configuration.**

Symbolic analysis of the Σ-Δ converter configuration in Fig. 4.5 shows

the polynomials $N(z)$, $S(z)$, and $D(z)$ to be

$$\begin{aligned} N(z) &= 1 + (-4 - B_1)z^{-1} + (6 + 3B_1 - B2)z^{-2} + \\ &\quad (-4 - 3B_1 + 2B_2 - B_3)z^{-3} + \\ &\quad (1 + B1 - B2 + B3 - B4)z^{-4} \qquad (4.48) \\ S(z) &= 0 + A_1 z^{-1} + (-3A_1 + A_2)z^{-2} + \\ &\quad (3A_1 - 2A_2 + A_3)z^{-3} + (-A_1 + A_2 - A_3 + A_4)z^{-4} \qquad (4.49) \\ D(z) &= N(z) - S(z). \qquad (4.50) \end{aligned}$$

4.5.2 Determination of the Polynomial $N(z)$

The polynomial $N(z)$ in Eqn. (4.48) can be rewritten in the product form

$$N(z) = \mathcal{Z} \cdot \mathcal{C}_N \cdot \mathcal{B}, \qquad (4.51)$$

with

$$\mathcal{Z} = \begin{bmatrix} z^0 & z^{-1} & z^{-2} & z^{-3} & z^{-4} \end{bmatrix}, \qquad (4.52)$$

$$\mathcal{C}_N = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -4 & -1 & 0 & 0 & 0 \\ 6 & 3 & -1 & 0 & 0 \\ -4 & -3 & 2 & -1 & 0 \\ 1 & 1 & -1 & 1 & -1 \end{bmatrix}, \qquad (4.53)$$

and

$$\mathcal{B} = \begin{bmatrix} 1 \\ B_1 \\ B_2 \\ B_3 \\ B_4 \end{bmatrix}. \tag{4.54}$$

Combining Eqns. (4.39) and (4.51) and solving for $\mathcal{B}$ results in

$$\mathcal{B} = \mathcal{C}_N^{-1}\mathcal{N}. \tag{4.55}$$

In this way, if the polynomial $N(z)$ or, equivalently, the matrix $\mathcal{N}$ is known, the coefficients B_k, $k = 1, 2, 3, 4$ can be determined.

Applying this method to the polynomial $N(z)$ in Eqn. (4.34) and solving for the matrix $\mathcal{B}$ gives

$$\mathcal{B} = \begin{bmatrix} 1 \\ -0.048140 \\ -0.048709 \\ -0.001137 \\ -0.000568 \end{bmatrix}. \tag{4.56}$$

4.5.3 Determination of the Polynomial $S(z)$

Eqn. (4.49) can be rewritten as

$$S(z) = \mathcal{Z} \cdot \mathcal{C}_S \cdot \mathcal{A}, \tag{4.57}$$

with

$$\mathcal{C}_S = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & -3 & 1 & 0 & 0 \\ 0 & 3 & -2 & 1 & 0 \\ 0 & -1 & 1 & -1 & 1 \end{bmatrix}, \tag{4.58}$$

and

$$\mathcal{A} = \begin{bmatrix} 0 \\ A_1 \\ A_2 \\ A_3 \\ A_4 \end{bmatrix}, \tag{4.59}$$

where the first row and the first column of the matrix $\mathcal{C}_S$ as well as the first element of the vector $\mathcal{A}$ have been introduced in order to remain consistent with the definitions related to the noise transfer function.

Combining Eqns. (4.43) and (4.57) results in

$$\mathcal{A} = \mathcal{C}_D^{-1}\mathcal{S}. \tag{4.60}$$

In a similar way as before, if the polynomial $S(z)$ is known, the coefficients A_k, $k = 1, 2, 3, 4$ can be uniquely determined. Applying this method to the polynomial $S(z)$ in Eqn. (4.35) gives

$$\mathcal{A} = \begin{bmatrix} 0 \\ -0.902637 \\ -0.400702 \\ -0.121368 \\ -0.013428 \end{bmatrix}. \tag{4.61}$$

4.5.4 Comments on the Polynomial $D(z)$

Eqn. (4.50) simply represents the fact that STF(z) and NTF(z) are complementary, in accordance with Eqn. (4.9).

4.5.5 Summary of the Synthesis of the Multiplier Coefficients

In this way, all the coefficients A_k and B_k, $(k = 1, 2, 3, 4)$ can be synthesized so as to satisfy a given set of transfer functions. Moreover, this procedure can easily be extended to higher order Σ-Δ converter configurations.

To summarize, the coefficients that implement the transfer functions given by Eqns. (4.34) and (4.34) are given in Table 4.3.

$A_1 = -0.902637$	$A_2 = -0.400702$	$A_3 = -0.121368$	$A_4 = -0.013428$
$B_1 = -0.048140$	$B_2 = -0.048709$	$B_3 = -0.001137$	$B_4 = -0.000568$

Table 4.3: **Multiplier Coefficients for a Bandpass Cascade-of-Integrators Sigma-Delta Converter.**

4.5.6 Computer Investigation of the Cascade-of-Integrators Σ-Δ Converter

The results given in Table 4.3 have been used to simulate the discrete-time behaviour of the Σ-Δ converter designed in Section 4.5.

The variation of the SQNR as a function of the input signal amplitude is investigated first. The input signal is chosen to be a sinusoidal signal of frequency $f = 375.2484$ kHz, close to the center frequency $f_c = 380kHz$ of the signal frequency band. The amplitude varies from $A = \Delta/2$, defined as

the 0dB level, to -90 dB, by increments of 1dB in the range $-20dB < A < 0dB$ and by increments of 5dB elsewhere. The resulting graph is plotted in Fig. 4.6.

Next, the variation of the SQNR as a function of the input signal frequency is investigated. In this experiment, the amplitude of the input signal is kept constant at -10 dB. The frequency of the input signal varies from 335 kHz to 425 kHz in 10 kHz increments. If the converter behaves in a manner close to the linear model, the SQNR should remain approximately constant, a fact which is confirmed by analysis of the results plotted in Fig. 4.7.

In an actual implementation using analog components, it is very unlikely that the multiplier coefficients A_k and B_k (with $k = 1, 2, 3, 4$) will be implemented with their exact optimized values. For example, in a switched-capacitor (SC) implementation, exact ratios of capacitor values cannot be obtained. Therefore, it is useful to study the behaviour of the cascade-of-integrators Σ-Δ converter under random variation of the multiplier coefficients. As no analytical tool is available for this purpose, a Monte-Carlo simulation has been employed.

It has to be pointed out that, in the present thesis, only variations of multiplier coefficients have been considered, even though it would be more realistic to consider capacitor variations in the actual SC implementation.

One thousand different circuits have been simulated and compared with respect to their SQNR. For each circuit, the ideal value of each multiplier coefficient is disturbed in accordance with

$$C' = C(1 + \epsilon), \tag{4.62}$$

where C is the optimized value of a given multiplier coefficient, ϵ is a random

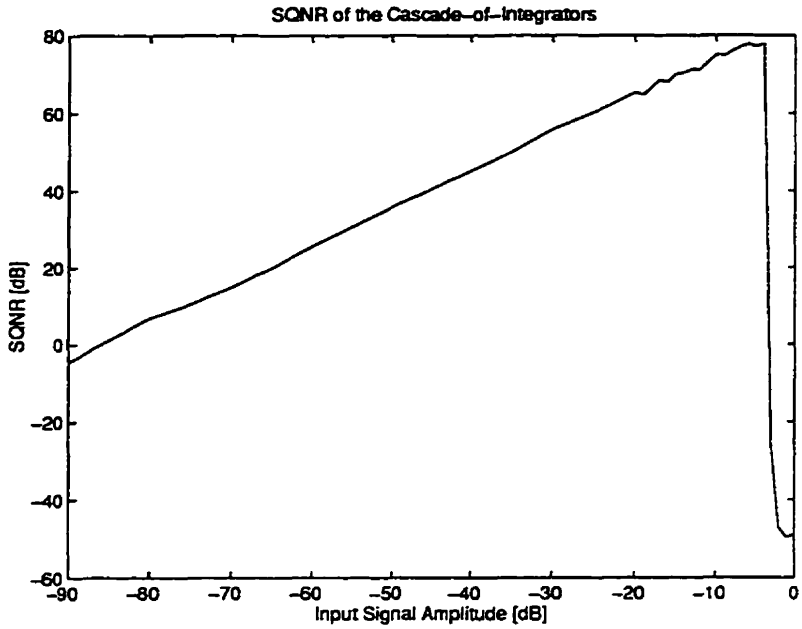

Figure 4.6: **SQNR vs. Input Signal Amplitude.**

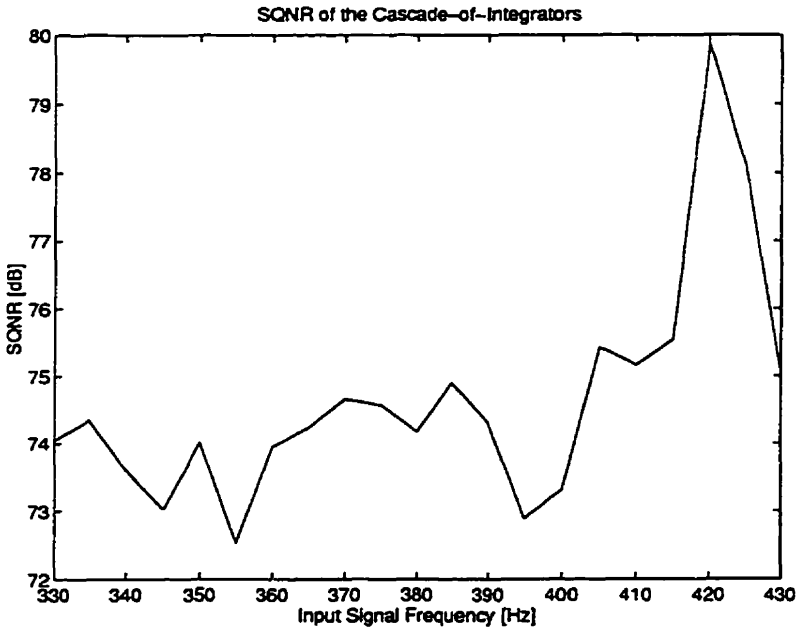

Figure 4.7: **SQNR vs. Input Signal Frequency.**

perturbation, and C' is the resulting value of the coefficient. In the present Monte-Carlo simulations, the perturbation has been chosen to be a white Gaussian distributed variable with the standard deviation $\sigma = 0.0333$. Thus, the perturbation is guaranteed to be within 10% of the optimized value in 99.7% of the cases [Pis87, p.533].

The histogram in Fig. 4.8 shows the distribution of the SQNR after 1000 Monte-Carlo simulations. The main results are summarized in Table 4.4.

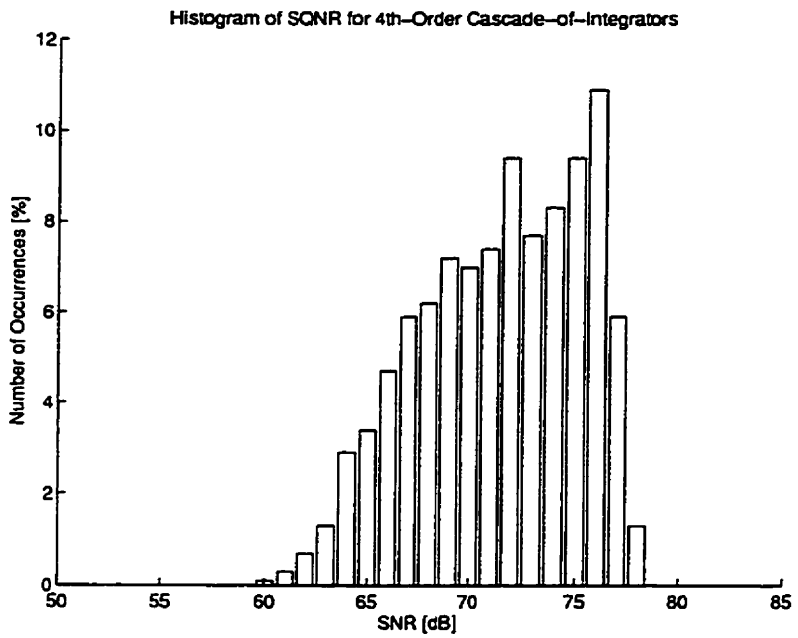

Figure 4.8: **Histogram of SQNR for the 4-th Order Cascade-of-Integrators.**

4.5.7 Switched-Capacitor Implementation of the Cascade-of-Integrators Σ-Δ Converter

One of the most commonly used technologies for the implementation of Σ-Δ converters is the SC technology. The cascade-of-integrators Σ-Δ converter is implemented in SC technology.

SQNR with Optimal Coefficients	75.1 dB
Average SQNR	71.4 dB
Minimum SQNR	59.6 dB
Maximum SQNR	78.2 dB
Median SQNR	71.8 dB
Standard Deviation of the SQNR	3.9 dB
Percentage of circuits above ideal SQNR	22.1 %

Table 4.4: **Statistical Datas Related to the Monte-Carlo Simulation of the 4th-Order Cascade-of-Integrators.**

The SC schematic diagram corresponding to the converter in Fig. 4.5 is presented in Fig. 4.9.

Each multiplier coefficient A_k and B_k (with $k = 1, 2, 3, 4$) is implemented by means of a capacitor ratio. Table 4.5 gives the capacitor ratios corresponding to the multiplier coefficients.

B_1	$CB1/CF1$
B_2	$CB2/CF1$
B_3	$CB3/CF1$
B_4	$CB4/CF1$
A_1	$CA1/CF5$
A_2	$CA2/CF5$
A_3	$CA3/CF5$
A_4	$CA4/CF5$

Table 4.5: **Relationship Between Multiplier Coefficients and Capacitor Ratios.**

In the first design stage, the capacitors $CX1$, $CX2$, $CX3$, $CX4$, $CF1$, $CF2$, $CF3$, $CF4$, $CF5$, and CFG are set to unity. Consequently, the other capacitor values are constrained to take the values given in Table 4.6. In an actual implementation, negative capacitor values are taken care of by imple-

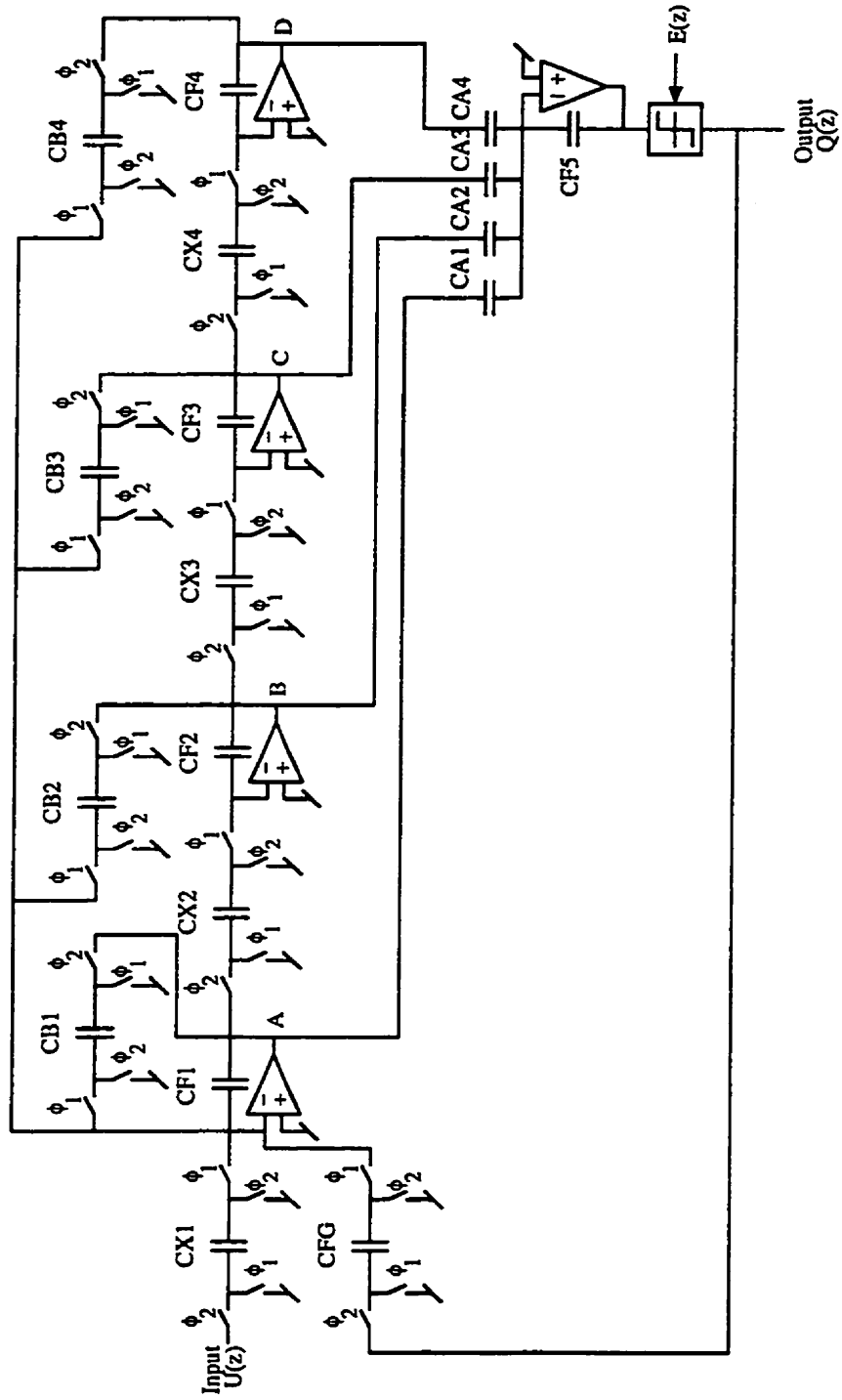

Figure 4.9: **Switched-Capacitor Implementation of the 4-th Order Cascade-of-Integrators.**

menting the SC circuit with a fully differential structure. Also, it should be pointed out that the capacitor values given in this chapter are dimensionless. This is due to the fact that the multiplier coefficients are fixed by capacitor ratios. Therefore, dimensionless capacitors can be used. In an actual implementation, a "unit" capacitor would be defined [2].

$CX1$	1	$CF1$	1
$CX2$	1	$CF2$	1
$CX3$	1	$CF3$	1
$CX4$	1	$CF4$	1
CFG	1	$CF5$	1
$CA1$	-0.902637	$CB1$	-0.048140
$CA2$	-0.400702	$CB2$	-0.048709
$CA3$	-0.121368	$CB3$	-0.001137
$CA4$	-0.013428	$CB4$	-0.000568

Table 4.6: **Initial Capacitor Value For the SC Implementation of the Cascade-of-Integrators.**

In order to optimize the performance of the SC Σ-Δ converter, the capacitors can be scaled in order to allow for a better dynamic range and a reduced overall chip area [GT86, p.338]. For the purpose of scaling, the SC Σ-Δ converter under consideration will be assumed to be linear (*i.e.* The quantization noise is assumed to be an additive white noise).

The capacitor scaling process proceeds in two phases. Firstly, the scaling of the capacitors connected to the node A, B, C, and D will be performed in order to guarantee the maximum of the magnitude/frequency response of the signal transfer function to be unity at each of the nodes. The capacitor values after the first scaling are given in Table 4.7.

The second scaling, also called scaling for unity minimum capacitor, is

[2]This value is usually in the pF range

$CX1$	1	$CF1$	1.3989
$CX2$	1.3989	$CF2$	4.6745
$CX3$	4.6745	$CF3$	17.038
$CX4$	17.038	$CF4$	77.748
CFG	1	$CF5$	1
$CA1$	-1.262699	$CB1$	-0.067343
$CA2$	-1.8730815	$CB2$	-0.22769
$CA3$	-2.0733295	$CB3$	-0.0194234
$CA4$	-1.044000	$CB4$	-0.0441609

Table 4.7: **Capacitor Values For the SC Implementation of the Cascade-of-Integrators After the First Scaling.**

useful to reduce the total capacitance[3], and, consequently to reduce the total chip area. The procedure is explained in detail in [GT86, p.345]. The final set of capacitor values is given in Table 4.8.

$CX1$	51.48429	$CF1$	72.02138
$CX2$	1	$CF2$	3.341554
$CX3$	1	$CF3$	3.644881
$CX4$	1	$CF4$	4.563211
CFG	51.48429	$CF5$	1
$CA1$	-1.262699	$CB1$	-3.467107
$CA2$	-1.8730815	$CB2$	-11.722458
$CA3$	-2.0733295	$CB3$	-1
$CA4$	-1.044000	$CB4$	-2.273593

Table 4.8: **Final Capacitor Values For the SC Implementation of the Cascade-of-Integrators.**

This concludes the design of the cascade-of-integrators Σ-Δ converter configuration.

[3]Defined as the sum of all the capacitor values on the circuit

4.6 Synthesis of the Cascade-of-Resonators Σ-Δ Converter Configuration

4.6.1 Presentation of the Structure

The cascade-of-resonators Σ-Δ converter configuration has first been proposed and used by Adams *et al.* [AJG+91] for a lowpass Σ-Δ converter. This structure has been successfully used by Jantzi *et al.* in 1993 [JSF93] and applied to bandpass conversion.

The schematic diagram for the fourth-order cascade-of-resonators structure is represented in Fig. 4.10. By symbolic analysis, the transfer functions

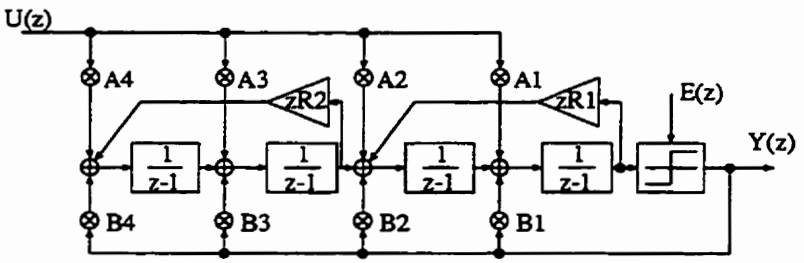

Figure 4.10: **The Fourth-Order Cascade-of-Resonators Σ-Δ Converter Configuration.**

STF(z) and NTF(z) can be found to be

$$N(z) = (1+(-2-R_1)z^{-1}+z^{-2})(1+(-2-R_2)z^{-1}+z^{-2}) \quad (4.63)$$

$$\begin{aligned} S(z) &= A_1z^{-1}+(A_2-3A_1-A_1R_1)z^{-2}+ \\ &\quad (A_3-2A_2+A_2R_1+3A_1+A_1R_1)z^{-3}+ \\ &\quad (A_4-A_3+A_2-A_1)z^{-4} \end{aligned} \quad (4.64)$$

$$\begin{aligned} D(z) &= 1+(-4-B_1-R_1-R_2)z^{-1}+ \\ &\quad (6-B_2+3B_1+R_1B_1+2R_1+R_1R_2+2R_2)z^{-2}+ \\ &\quad (-4-B_3+2B_2+B_2R_1-3B_1-B_1R_1-R_1-R_2)z^{-3}+ \end{aligned}$$

$$(1 - B_4 + B_3 - B_2 + B_1)z^{-4}. \tag{4.65}$$

In the case of the cascade-of-resonators Σ-Δ converter configuration, the complementarity of signal- and noise transfer functions is no longer ensured by the structure itself.

4.6.2 Determination of the Polynomial $N(z)$

A comparative analysis of Eqns. (4.63) and (4.19) shows that the zeros of $N(z)$ are constrained to be on the unit circle. Moreover, the relationship between the frequency f_{0l} ($l = 1, 2$) at which the l-th zero of $N(z)$ occurs and the corresponding multiplier coefficient R_l, is given by

$$R_l = 2\cos\left(2\pi\frac{f_{0l}}{f_s}\right) - 2, \tag{4.66}$$

with f_s being the sample frequency of the system.

Applying Eqn. (4.66) to the frequencies given by Eqns. (4.36) and (4.37), gives for R_1 and R_2 :

$$\begin{aligned} R_1 &= -0.020756 \\ R_2 &= -0.0273841. \end{aligned} \tag{4.67}$$

4.6.3 Determination of the Polynomial $S(z)$

In a similar way as in Section 4.5, the polynomial $S(z)$ in Eqn. (4.64) can be recast in the matricial form

$$S(z) = \mathcal{Z} \cdot \mathcal{R}_S \cdot \mathcal{A}, \tag{4.68}$$

with

$$\mathcal{Z} = \begin{bmatrix} z^0 & z^{-1} & z^{-2} & z^{-3} & z^{-4} \end{bmatrix}, \tag{4.69}$$

$$\mathcal{R}_S = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & -3-R_1 & 1 & 0 & 0 \\ 0 & 3+R_1 & -2-R_1 & 1 & 0 \\ 0 & -1 & 1 & -1 & 1 \end{bmatrix}, \tag{4.70}$$

and

$$\mathcal{A} = \begin{bmatrix} 0 \\ A_1 \\ A_2 \\ A_3 \\ A_4 \end{bmatrix} \tag{4.71}$$

Combining Eqns. (4.43) and (4.68) and solving for $\mathcal{A}$ yields

$$\mathcal{A} = \mathcal{R}_S^{-1}\mathcal{S}. \tag{4.72}$$

Replacing R_1 and R_2 by their numerical value given in Eqn. (4.67) in $\mathcal{R}_S$ and filling $\mathcal{S}$ with the coefficients obtained through optimization gives for $\mathcal{A}$

$$\mathcal{A} = \begin{bmatrix} 0 \\ -0.902637 \\ -0.381967 \\ -0.094705 \\ -0.005500 \end{bmatrix}. \tag{4.73}$$

4.6.4 Determination of the Polynomial $D(z)$

Finally, $D(z)$ can be rewritten

$$D(z) = \mathcal{Z} \cdot \mathcal{R}_D \cdot \mathcal{B}, \tag{4.74}$$

with

$$\mathcal{Z} = \begin{bmatrix} z^0 & z^{-1} & z^{-2} & z^{-3} & z^{-4} \end{bmatrix}, \tag{4.75}$$

$$\mathcal{R}_D = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -4 - R_1 - R_2 & -1 & 0 & 0 & 0 \\ 6 + 2R_1 + R_1R_2 + 2R_2 & 3 + R_1 & 1 & 0 & 0 \\ -4 - R_1 - R_2 & -3 - R_1 & 2 + R_1 & -1 & 0 \\ 1 & +1 & -1 & 1 & -1 \end{bmatrix} \tag{4.76}$$

and

$$\mathcal{A} = \begin{bmatrix} 0 \\ A_1 \\ A_2 \\ A_3 \\ A_4 \end{bmatrix}. \tag{4.77}$$

Solving for $\mathcal{B}$ from Eqns. (4.45) and (4.74) gives

$$\mathcal{B} = \mathcal{R}_D^{-1}\mathcal{D}. \tag{4.78}$$

A numerical application gives

$$\mathcal{B} = \begin{bmatrix} 1 \\ -0.902637 \\ -0.381967 \\ -0.094705 \\ -0.005500 \end{bmatrix}. \tag{4.79}$$

4.6.5 Summary of the Synthesis of the Multiplier Coefficients

To summarize, the multiplier coefficients of a fourth-order cascade-of-resonators Σ-Δ converter configuration implementing the transfer functions given by Eqns. (4.34) and (4.35) are given in Table 4.9

	$R_1 = -0.020756$	$R_2 = -0.0273841$	
$A_1 = -0.902637$	$A_2 = -0.381967$	$A_3 = -0.094705$	$A_4 = -0.005500$
$B_1 = -0.902637$	$B_2 = -0.381967$	$B_3 = -0.094705$	$B_4 = -0.005500$

Table 4.9: **Multiplier Coefficients for a Bandpass Cascade-of-Resonators Sigma-Delta Converter.**

4.6.6 Computer Investigation of the Cascade-of-Resonators Σ-Δ Converter

The results of the design of the multiplier coefficients given in Table 4.9 are used to simulate the discrete-time behaviour of the corresponding fourth-order cascade-of-resonators Σ-Δ converter. The conditions of the simulations are the same as the conditions given in Subsection 4.5.6.

For the investigation of the SQNR as a function of the signal amplitude,

the frequency of the input sinusoidal signal is chosen to be $f = 375.2485$ kHz. The 0dB reference corresponds to a sinusoid of amplitude $A = \Delta/2$. The amplitude then varies from 0 dB to -80 dB. The resulting SQNR plot can be found in Fig. 4.11.

Next, the variation of the SQNR as a function of the input signal frequency is investigated. In this experiment, the amplitude of the input signal is kept constant at -10 dB. The frequency of the input signal varies from 335 kHz to 425 kHz in 10 kHz increments. If the converter behaves in a manner close to the linear model, the SQNR should remain approximately constant, a fact which is confirmed by analysis of the results plotted in Fig. 4.12.

For the same reasons as in Subsection 4.5.6, its is very unlikely that the coefficients R_1, R_2, A_1, A_2, A_3, A_4, B_1, B_2, B_3, and B_4 may be implemented with their optimized value. In order to investigate the influence of multiplier coefficient variations on the SQNR, Monte-Carlo simulations are performed. Each multiplier coefficient will undergo a perturbation of the form given by Equation (4.62).

The histogram in Fig. 4.13 shows the distribution of the SQNR for 1000 different circuits. The main results are given in Table 4.10.

SQNR with Optimal Coefficients	75.1 dB
Average SQNR	76.2 dB
Minimum SQNR	70.4 dB
Maximum SQNR	78.8 dB
Median SQNR	76.3 dB
Standard Deviation of the SQNR	1.3 dB
Percentage of circuits above ideal SQNR	80.5 %

Table 4.10: **Statistical Datas Related to the Monte-Carlo Simulation of the 4th-Order Cascade-of-Resonators.**

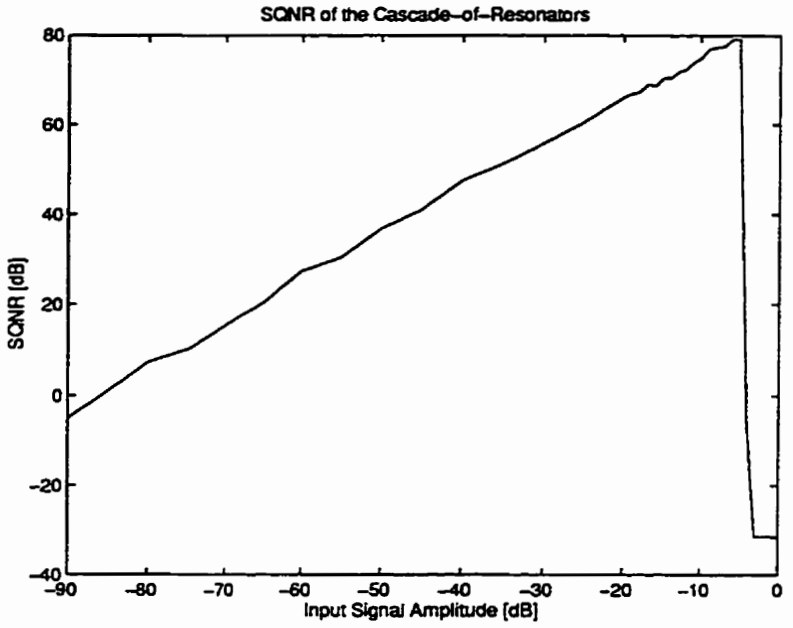

Figure 4.11: **SQNR vs. Input Signal Amplitude.**

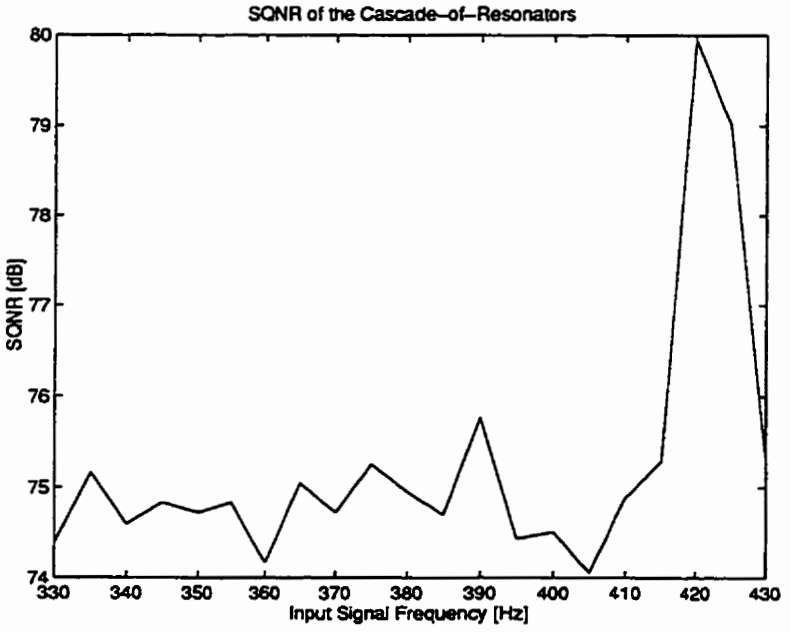

Figure 4.12: **SQNR vs. Input Signal Frequency.**

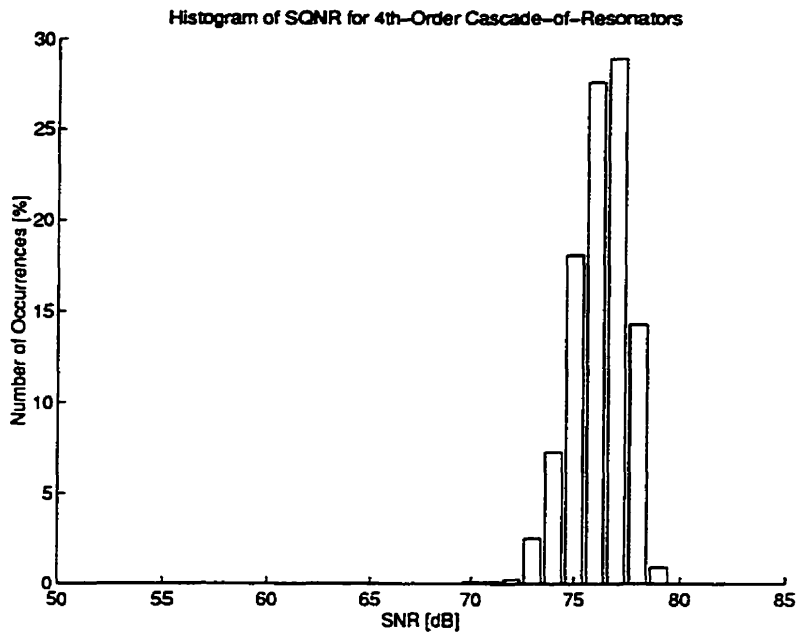

Figure 4.13: **Histogram of SQNR for the 4-th Order Cascade-of-Resonators.**

4.6.7 Switched-Capacitor Implementation of the Cascade-of-Resonators Σ-Δ Converter

The SC schematic diagram of the converter in Fig. 4.10 is represented in Fig. 4.14 and has been taken from [JSF93].

The multiplier coefficients are implemented by the means of the capacitor ratios given in Table 4.11. Following the procedure outlined in Subsection 4.5.7, the capacitor values obtained after scaling for dynamic range and for unity capacitance are given in Table 4.12.

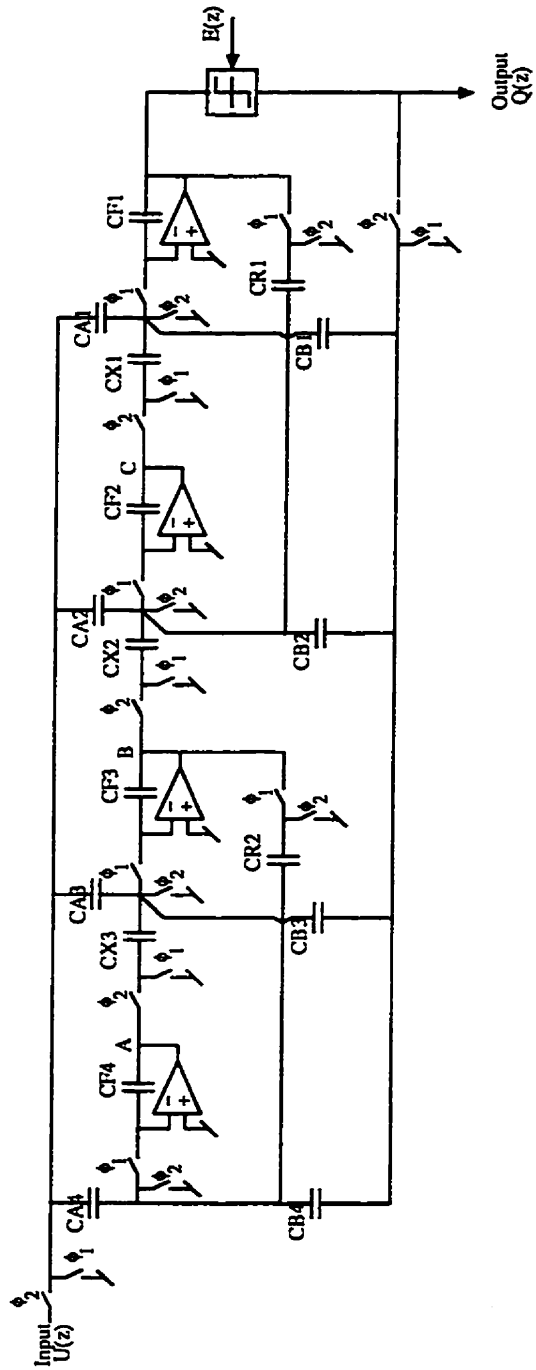

Figure 4.14: **Switched-Capacitor Implementation of the 4-th Order Cascade-of-Resonators.**

B_1	$CB1/CF1$
B_2	$CB2/CF2$
B_3	$CB3/CF3$
B_4	$CB4/CF4$
A_1	$CA1/CF1$
A_2	$CA2/CF2$
A_3	$CA3/CF3$
A_4	$CA4/CF4$
R_1	$-CR1/CF2$
R_2	$-CR2/CF4$

Table 4.11: **Relationship Between Multiplier Coefficients and Capacitor Ratios.**

4.7 Comparative Discussion of the Two Synthesized Structures

4.7.1 Introduction

The two circuits designed in Sections 4.5 and 4.6 can be compared together in the light of three different situations.

- Sensitivity of the structure
- Structure of the transfer functions
- Feasibility of the SC implementation

4.7.2 Sensitivity of the Structure

A practical SC implementation takes into account capacitor mismatches, causing deviations in the transfer functions realized by of the converter, and, consequently, degrading the SQNR. Therefore, the sensitivity of the structure to parameter variations is one of the most important criteria. Naturally, if a

$CX1$	1	$CF1$	2.2594785
$CX2$	5.4933513	$CF2$	21.3229909
$CX3$	1	$CF3$	10.365451
		$CF4$	3.5230439
$CA1$	-2.039489	$CB1$	-2.039489
$CA2$	-18.40272695	$CB2$	-18.4027269
$CA3$	-8.609546	$CB3$	-8.609546
$CA4$	-1.761522	$CB4$	-1.761522
$CR1$	1	$CR2$	1

Table 4.12: **Final Capacitor Values For the SC Implementation of the Cascade-of-Resonators.**

structure is less sensitive to random perturbations than another, then it will be more suitable for a practical SC implementation.

Throughout this chapter, the main performance criterion is the signal-to-quantization noise ratio, providing a good basis for the comparison of the above two bandpass Σ-Δ converter configurations. Because there is no readily available analytical tool to study the sensitivity of the cascade-of-integrators and the cascade-of-resonators Σ-Δ converter configurations, the only alternative to provide an insight into the sensitivity of these structures is to perform a detailed Monte-Carlo analysis. This has been performed successfully for both structures and its main results are given in Tables 4.4 and 4.10. It can be observed that the cascade-of-resonators Σ-Δ converter configuration has a better behaviour than the cascade-of-integrators. The statistical data shows, notably, that, in average, the SQNR of the cascade-of-resonators structure is almost 5dB better than the SQNR of the cascade-of-integrators. The main reason is due to the structure itself and is discussed in the next section.

4.7.3 Influence of the Topology of the Converter on the Transfer Functions

The topology of each Σ-Δ converter configuration directly influences the composition of the transfer functions. For example, Eqn. (4.50) indicates that the noise transfer function and the signal transfer function are complementary.

The main feature of the cascade-of-resonators is the presence of resonators which constrain the zeros of the noise transfer function on the unit circle. Any perturbation of the parameter R_l ($l = 1, 2, \cdots, N$, with $2N$ being the order of the structure) will only affect the frequency at which the zeros occurs but will not move any zero away from the unit circle. In this way, the degradation of the effectiveness of the noise transfer function is minimized.

The sensitivity $S_{R_l}^{\omega_{0l}}$ of the frequency $\omega_{0l} = 2\pi f_{0l}/f_s$ with respect to the coefficient R_l is defined as

$$S_{R_l}^{\omega_{0l}} = \frac{R_l}{\omega_{0l}} \frac{d\omega_{0l}}{dR_l}. \tag{4.80}$$

Replacing R_l by $\omega_{0l} = 2\pi f_{0l}/f_s$ from Eqn. (4.66) into Eqn. (4.80) gives

$$S_{R_l}^{\omega_{0l}} = \frac{-1/2R_l}{\arccos\left(\frac{R_l+2}{2}\right)\sqrt{1-\left(\frac{R_l+2}{2}\right)^2}}. \tag{4.81}$$

Fig. 4.15 plots the sensitivity $S_{R_l}^{\omega_{0l}}$ as a function of the multiplier coefficient R_l, in the range $-4 \leq R_l \leq 0$. As it can be observed, the magnitude of the sensitivity is less than unity in the range $-3.4 \leq R_l \leq 0$ (*i.e.* a 1% variation of R_l implies a 1 % or less variation of the frequency ω_{0l}). Therefore, it can be concluded from the analysis of the cascade-of-resonators Σ-Δ converter configuration that such a structure has a low sensitivity to parameter changes.

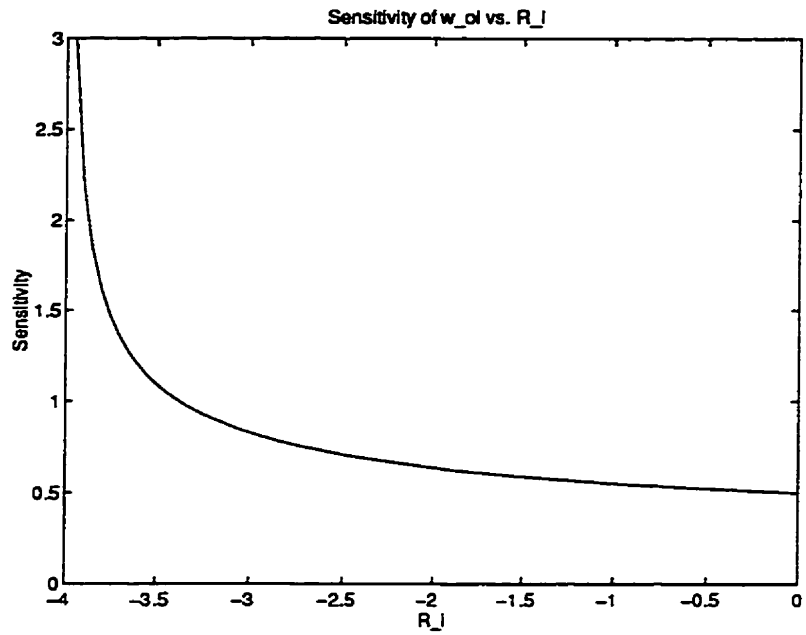

Figure 4.15: **Sensitivity of the Frequency ω_{0i} as a Function of R_i.**

4.7.4 Feasibility of the SC implementation

In order to reduce the cost of a SC implementation, it is important to ensure that the chip area is small. Moreover, the chip area is in direct proportion with the size of the capacitors as they are the ones that require the most area (the transistors and the switches being of a much smaller size). Therefore, it is important that the total capacitance is minimized. In much the same way, wide capacitor spreads are very difficult to obtain. Typically, the ratio between the smallest capacitor and the largest one must remain less than 50. Comparing the results of the SC implementation given in Tables 4.8 and 4.12 show that the cascade-of-resonators gives the best results in terms of capacitor spread as well as in terms of total capacitance (see Table 4.13).

4.7.5 Summary of the Comparison Criteria

From Table 4.13, it can be seen that in most aspects, the cascade-of-resonators Σ-Δ converter configuration appears to be more suitable for SC implementation. Of particular interest are the low sensitivity of the structure to parameter variations and the low capacitor spread. However, the cascade-of-resonators structure does not exhibit the important feature of transfer function complementarity.

Criterion	Cascade-of Integrators	Cascade-of Resonators
Total Capacitance	164.7	108.6
Capacitance spread	72.02	21.32
SQNR Std. Deviation (from Monte-Carlo Simulations)	3.9 dB	1.3 dB
Complementary Transfer Functions	Yes	No
Zeros of NTF(z) on Unit Circle	No	Yes

Table 4.13: **Comparison Between the Cascade-of-Integrators and the Cascade-of-Resonators Σ-Δ Converters.**

4.8 A New Resonator Based Structure for Bandpass Σ-Δ A/D Conversion

4.8.1 Introduction

In Section 4.7.5, it has been seen that the cascade-of-resonators is a very useful structure. Its low sensitivity to parameter changes makes this structure very interesting for a SC implementation. The cascade-of-integrators, on the other hand, proves to be more sensitive to parameters perturbations but exhibits the important feature of complementary transfer functions. This

section introduces a new structure which combines the best features of the above two structures and gives a formal design procedure.

4.8.2 The Proposed New Structure

The schematic diagram in Fig. 4.16 shows the general form of the proposed Σ-Δ converter configuration. This configuration is composed of a single-bit quantizer and N second-order resonators, leading to a structure of order $2N$.

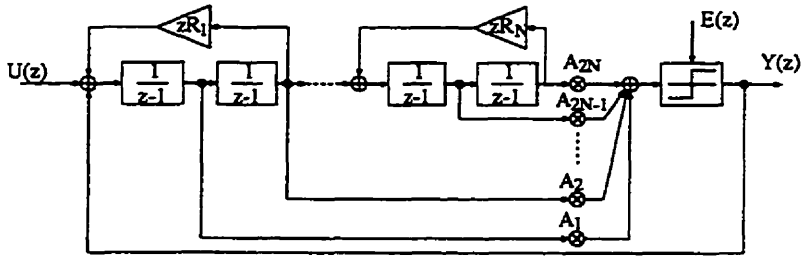

Figure 4.16: **The New Cascade-of-Resonators.**

At this point, it is useful to give the following lemma.

Lemma 5 *The schematic diagram of order $2N$ shown in Fig. 4.17 has the transfer function*

$$H_N(z) = \frac{\sum_{k=1}^{N} \left(H_A(z,k)\right) z^{-2k-2} \prod_{l=k+1}^{N} \left(1 + (-2 - R_l)z^{-1} + z^{-2}\right)}{\prod_{k=1}^{N} \left(1 + (-2 - R_k)z^{-1} + z^{-2}\right)}, \quad (4.82)$$

where

$$H_A(z,k) = A_{2k-1}z^{-1} + \left(-A_{2k-1} + A_{2k}\right) z^{-2}. \quad (4.83)$$

Proof : By mathematical induction. For $N = 1$, Fig. 4.17 reduces to the circuit shown in Fig. 4.18. Symbolic analysis shows the transfer function to be

$$H_1(z) = \frac{Y(z)}{X(z)} = \frac{A_1 z^{-1} + \left(-A_1 + A_2\right) z^{-2}}{1 + -(-2 - R_k)z^{-1} + z^{-2}}. \quad (4.84)$$

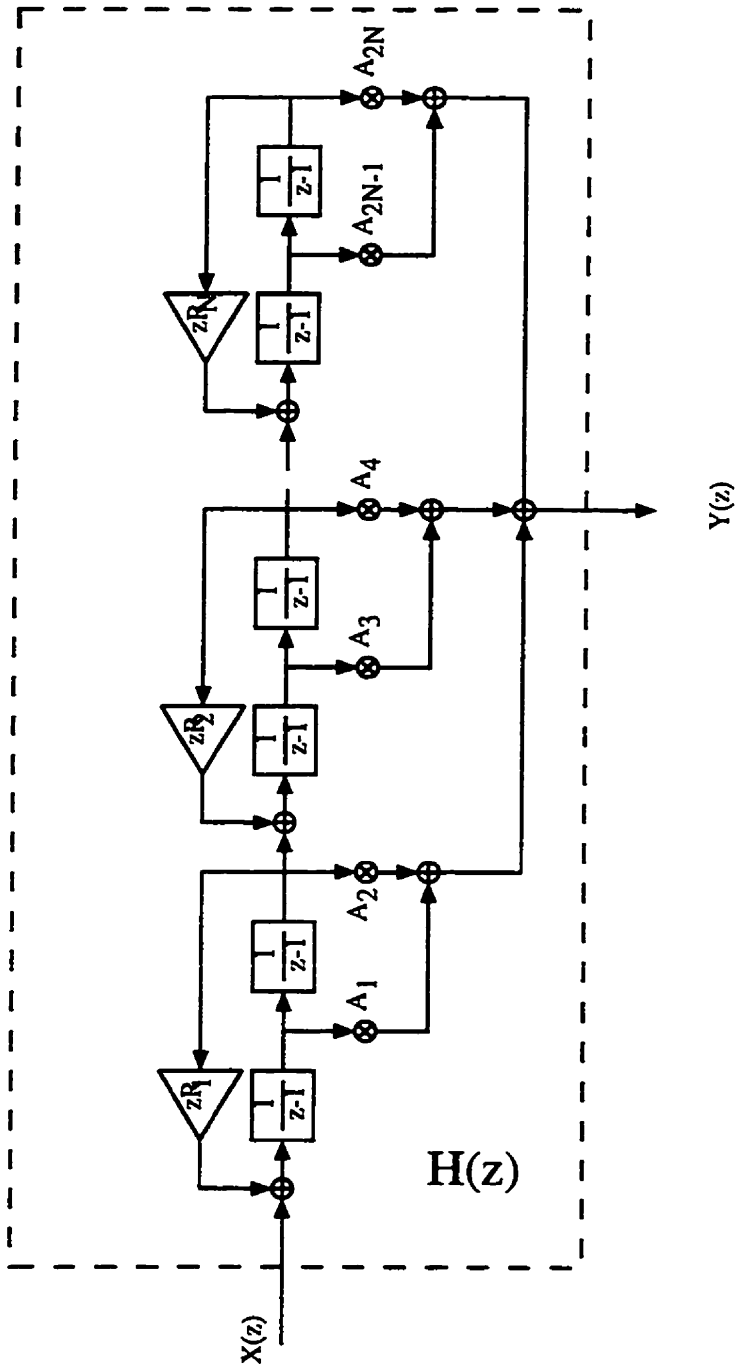

Figure 4.17: **Structure for Lemma 5.**

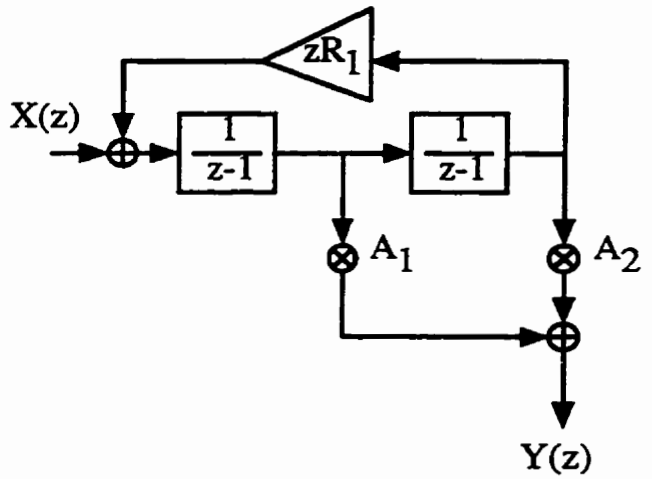

Figure 4.18: **Structure for** $N = 1$.

Substituting $N = 1$ in Eqn. (4.82) proves the validity of the lemma for $N = 1$. Therefore, it is sufficient to show that if the lemma holds true fr $N = M$, then it also holds true for $N = M + 1$.

In order to calculate the transfer function of the structure when $N = M + 1$, let the building block shown in Fig. 4.19 be introduced. Two transfer

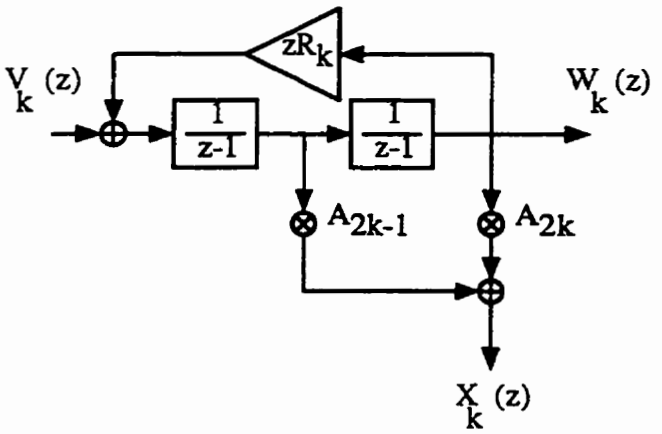

Figure 4.19: **Building Block.**

functions can be defined. The first one denoted by $H_{VW_k}(z)$ relates the signal

$V_k(z)$ to the ouput $W_k(z)$ and is given by

$$H_{VW_k}(z) = \frac{W_k(z)}{V_k(z)} = \frac{z^{-2}}{1 + (-2 - R_k)z^{-1} + z^{-2}}. \tag{4.85}$$

Similarly, $H_{VX_k}(z)$ relates $V_k(z)$ to $X_k(z)$ in accordance with

$$H_{VX_k}(z) = \frac{X_k(z)}{Y_k(z)} = \frac{A_{2k-1}z^{-1} + (-A_{2k-1} + A_{2k})\, z^{-2}}{1 + (-2 - R_k)z^{-1} + z^{-2}}. \tag{4.86}$$

The structure shown in Fig. 4.17 when $N = M + 1$ can be represented as shown in Fig. 4.20.

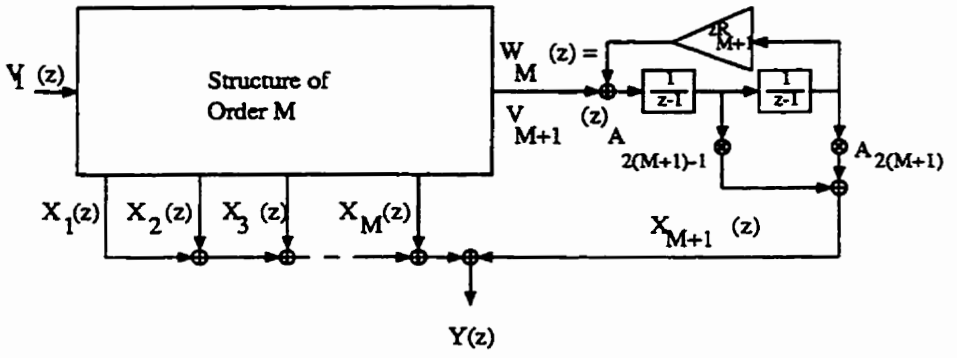

Figure 4.20: **Structure of order $M + 1$.**

At the final adder, the equality

$$Y(z) = \sum_{k=1}^{M} X_k(z) + X_{M+1}(z) \tag{4.87}$$

holds. But the term $\sum_{k=1}^{M} X_k(z)$ corresponds to the output of the structure of order M. In this way, the sum can be replaced by

$$\sum_{k=1}^{M} X_k(z) = V_1(z)H_M(z). \tag{4.88}$$

Also, using Eqn. (4.86), $X_{M+1}(z)$ becomes

$$X_{M+1}(z) = V_{M+1} \cdot \frac{A_{2(M+1)-1}z^{-1} + \left(-A_{2(M+1)-1} + A_{2(M+1)}z^{-2}\right)}{1 + (-2 - R_{M+1}z^{-1} + z^{-2})}. \quad (4.89)$$

Replacing Eqns. (4.88) and (4.89) into Eqn. (4.87) yields

$$\begin{aligned} Y(z) &= V_1(z)H_M(z) + \\ &\quad V_{M+1} \cdot \frac{A_{2(M+1)-1}z^{-1} + \left(-A_{2(M+1)-1} + A_{2(M+1)}z^{-2}\right)}{1 + (-2 - R_{M+1}z^{-1} + z^{-2})}. \end{aligned} \quad (4.90)$$

Using Eqn. (4.85), it becomes evident that

$$\begin{aligned} V_{M+1}(z) &= W_M(z) && (4.91) \\ &= V_M(z)\frac{z^{-2}}{1 + (-2 - R_M)z^{-1} + z^{-2}}. && (4.92) \end{aligned}$$

Applying iteratively Eqn. (4.85) to Eqn. (4.92) yields

$$V_{M+1}(z) = V_1(z) \cdot \prod_{k=1}^{M} \frac{z^{-2}}{1 + (-2 - R_k)z^{-1} + z^{-2}}. \quad (4.93)$$

Replacing $V_{M+1}(z)$ in Eqn. (4.90) by its expression in Eqn. (4.93) gives for $Y(z)$

$$\begin{aligned} Y(z) &= V_1(z)H_M(z) + V_1(z)\frac{A_{2(M+1)-1}z^{-1} + \left(-A_{2(M+1)-1} + A_{2(M+1)}z^{-2}\right)}{1 + (-2 - R_{M+1}z^{-1} + z^{-2})} \cdot \\ &\quad \cdot \prod_{k=1}^{M} \frac{z^{-2}}{1 + (-2 - R_k)z^{-1} + z^{-2}}. \end{aligned} \quad (4.94)$$

Dividing Eqn. (4.94) by $V_1(z)$ and reordering the terms in the quotient yields

$$\frac{Y(z)}{V_1(z)} = H_{M+1}(z) = H_M(z) +$$

$$(H_A(z, M+1))\, z^{-2M} \cdot \prod_{k=1}^{M+1} \frac{1}{1+(-2-R_k)z^{-1}+z^{-2}}. \quad (4.95)$$

But, by assumption, Eqn. (4.82) holds true. In this way, $H_M(z)$ in Eqn. (4.95) can be replaced in accordance with

$$H_{M+1}(z) = \frac{\sum_{k=1}^{M} (H_A(z,k))\, z^{-(2k-2)} \prod_{l=k+1}^{M} (1+(-2-R_l)z^{-1}+z^{-2})}{\prod_{k=1}^{M} (1+(-2-R_k)z^{-1}+z^{-2})} + (H_A(z, M+1))\, z^{-2M} \cdot \prod_{k=1}^{M+1} \frac{1}{1+(-2-R_k)z^{-1}+z^{-2}}. \quad (4.96)$$

Multiplying the first ratio by $(1+(-2-R_{M+1})z^{-1}+z^{-2})$ and re-grouping yields

$$H_{M+1}(z) = \frac{\sum_{k=1}^{M+1} (H_A(z,k))\, z^{-(2k-2)} \prod_{l=k+1}^{M+1} (1+(-2-R_l)z^{-1}+z^{-2})}{\prod_{k=1}^{M+1} (1+(-2-R_k)z^{-1}+z^{-2})}, \quad (4.97)$$

establishing the validity of the lemma for $N = M+1$. *q.e.d.*

The polynomials $N(z)$, $S(z)$, and $D(z)$ as defined in accordance with Section 4.2 are given by the following theorem.

Theorem 3 *The polynomials $N(z)$, $S(z)$, and $D(z)$ describing the proposed new cascade-of-resonators Σ-Δ converter configuration shown in Fig. 4.16 are given by*

$$N(z) = \prod_{k=1}^{N} \left[1+(-2-R_k)z^{-1}+z^{-2}\right], \quad (4.98)$$

$$S(z) = \sum_{l=1}^{N} \left[A_{2l-1}z^{-(2l-1)} + (-A_{2l-1}+A_{2l})z^{-2l}\right] z^{2l-2} \prod_{k=l+1}^{N} \left[1+(-2-R_k)z^{-1}+z^{-2}\right], \quad (4.99)$$

$$D(z) = N(z) - S(z). \quad (4.100)$$

Proof : By making use of Eqn. (4.13), the proof of the theorem reduces to the proof of lemma 5. *q.e.d.*

4.8.3 Design Procedure

From Eqn. (4.98), it can be shown that all the zeros of $N(z)$ lie on the unit circle, provided that

$$-4 \leq R_k \leq 0, \quad \forall k. \tag{4.101}$$

Also, in a similar manner as for the cascade-of-resonators (Section 4.6), the relationship between the frequency f_{0k} at which the k-th zero of $N(z)$ occurs and the corresponding parameter R_k, is given by

$$R_k = 2\cos\left(2\pi\frac{f_{0k}}{f_s}\right) - 2, \tag{4.102}$$

with f_s being the sampling frequency of the system.

In the synthesis process, the polynomial $N(z)$ is known. In this way, the frequencies f_{0k} are known. Eqn. (4.102) can then be applied in order to find the value for the coefficients R_k.

The polynomial $S(z)$ in Eqn. (4.99) can be rewritten

$$S(z) = \mathcal{Z}_{1,2N} \cdot \mathcal{R}_{2N,2N} \cdot \mathcal{A}_{2N,1}, \tag{4.103}$$

with

$$\mathcal{Z} = \begin{bmatrix} z^{-1} & z^{-2} & \cdots & z^{-2N} \end{bmatrix},$$

$$\mathcal{R} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 \\ r_{2,1} & 1 & 0 & & 0 \\ r_{3,1} & r_{3,2} & 1 & & 0 \\ \vdots & & & \ddots & \vdots \\ r_{2N,1} & r_{2N,2} & r_{2N,3} & \cdots & 1 \end{bmatrix},$$

$$\mathcal{A} = \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_{2N} \end{bmatrix}.$$

By inspection of Eqn. (4.99), it can be shown that the matrix $\mathcal{R}$ is lower triangular. Also, its principal diagonal is composed of unity elements.

Because of the complementarity of the transfer functions, the polynomial $S(z)$ can easily be determined by using Eqn. (4.100). Also, $S(z)$ can be written (in its most general form) as

$$S(z) = s_1 z^{-1} + s_2 z^{-2} + \cdots + s_{2N} z^{-2N}, \tag{4.104}$$

or, equivalently,

$$S(z) = \begin{bmatrix} z^{-1} & z^{-2} & \cdots & z^{-2N} \end{bmatrix} \begin{bmatrix} s_1 \\ s_2 \\ \vdots \\ s_{2N} \end{bmatrix} \tag{4.105}$$

$$\equiv \mathcal{Z}_{1,2N} \mathcal{S}_{2N,1}. \tag{4.106}$$

Therefore, combining Eqn. (4.106) and Eqn. (4.103) and solving for $\mathcal{A}$, results

in

$$\mathcal{A} = \mathcal{R}^{-1} \cdot \mathcal{S}. \tag{4.107}$$

4.8.4 Design Example

Synthesis of the Multiplier Coefficients

In this Section, the fourth-order transfer functions in Eqns. (4.34) and (4.35) are applied to the new structure of order 4. The schematic diagram of the converter configuration of order 4 ($N = 2$) is shown in Fig. 4.21.

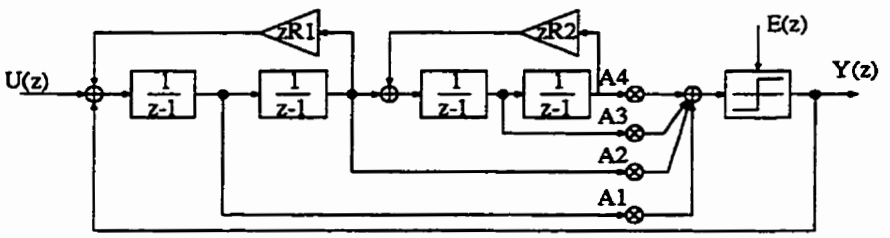

Figure 4.21: **New Resonator-based Structure of Order 4.**

Using Theorem 3 with $N = 2$, the polynomials $N(z)$, $S(z)$, and $D(z)$ of the new structure become

$$N(z) = \left(1 + (-2 - R_1)z^{-1} + z^{-2}\right)\left(1 + (-2 - R_2)z^{-1} + z^{-2}\right) \tag{4.108}$$

$$\begin{aligned} S(z) &= \left[A_1 z^{-1} + (-A_1 + A_2)z^{-2}\right]\left(1 + (-2 - R_2)z^{-1} + z^{-2}\right) + \\ &\quad \left[A_3 z^{-1} + (-A_3 + A_4)z^{-2}\right] z^{-2} \end{aligned} \tag{4.109}$$

$$\begin{aligned} &= A_1 z^{-1} + (-R_2 A_1 - 3A_1 + A_2)z^{-2} + \\ &\quad (3A_1 + R_2 A_1 - 2A_2 - R_2 A_2 + A_3)z^{-3} + \\ &\quad (-A_1 + A_2 - A_3 + A_4)z^{-4}, \end{aligned} \tag{4.110}$$

and

$$D(z) = N(z) - S(z). \tag{4.111}$$

Applying Eqns. (4.36) and (4.37) to Eqn. (4.102), the multiplier coefficients R_1 and R_2 are given by

$$R_1 = -0.020756, \text{and} \tag{4.112}$$

$$R_2 = -0.0273841. \tag{4.113}$$

The procedure for the synthesis of the coefficients A_k, $k = 1, 2, 3, 4$ is the same as the procedure described in Section 4.5.3. The resulting multiplier coefficients are

$$\mathcal{A} = \begin{bmatrix} A_1 \\ A_2 \\ A_3 \\ A_4 \end{bmatrix} = \begin{bmatrix} -0.902637 \\ -0.381967 \\ -0.094705 \\ -0.005500 \end{bmatrix}. \tag{4.114}$$

Computer Investigation of the New Cascade-of-Resonators Σ-Δ Converter

As in Sections 4.5.6 and 4.6.6, a computational investigation of the new cascade-of-resonators Σ-Δ converter configuration can be carried out. The first investigation is concerned with the variation of the SQNR as a function of the input signal amplitude. The input signal sinusoid is chosen to be $f = 375.2485$ kHz. The 0dB reference corresponds to a sinusoid of amplitude $A = \Delta/2$. The amplitude then varies from 0 dB to -80 dB. The resulting SQNR plot is shown in Fig. 4.22.

The variation of the SQNR as a function of the input signal frequency is not performed as the previous investigations were sufficient to prove the validity of the white quantization noise assumption.

A set of one thousand Monte-Carlo simuations is carried out. Each multiplier coefficient will undergo a perturbation of the form given by Eqn. (4.62).

The histogram shown in Fig. 4.13 shows the distribution of the SQNR for 1000 different circuits. The results are given in Table 4.14.

SQNR with Optimal Coefficients	75.1 dB
Average SQNR	76.3 dB
Minimum SQNR	-37.11 dB
Maximum SQNR	79.0 dB
Median SQNR	76.9 dB
Standard Deviation of the SQNR	6.6 dB
Percentage of circuits above ideal SQNR	88.5 %

Table 4.14: **Statistical Datas Related to the Monte-Carlo Simulation of the 4th-Order New Cascade-of-Resonators.**

As expected, the new cascade-of-resonators exhibits SQNR characteristics that are as good as the characteristics of the *conventional* cascade-of-resonators designed in Section 4.6. The only drawback is that in some circumstances during the Monte-Carlo simulations, the converter under consideration became unstable. No explanation could be found to explain the instabilities. By not taking the unstable circuits into account, the minimum SQNR is 72.0dB and the standard deviation is 1.3 dB. These values are comparable to the performance of the cascade-of-resonators investigated in Section 4.6.6.

Switched-Capacitor Implementation of the New Cascade-of-Resonators

The proposed new cascade-of-resonators structure can be implemented using SC technology. The corresponding schematic diagram is shown in Fig. 4.24.

The multiplier coefficients are implemented by pairs of capacitors as given in Table 4.15.

After scaling for dynamic range and for unity capacitor, as explained in

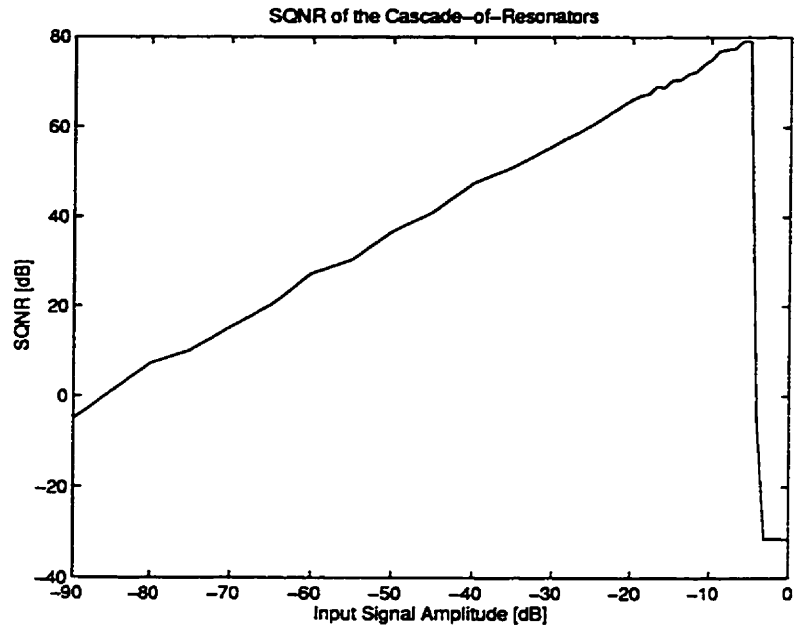

Figure 4.22: **SQNR vs. Input Signal Amplitude.**

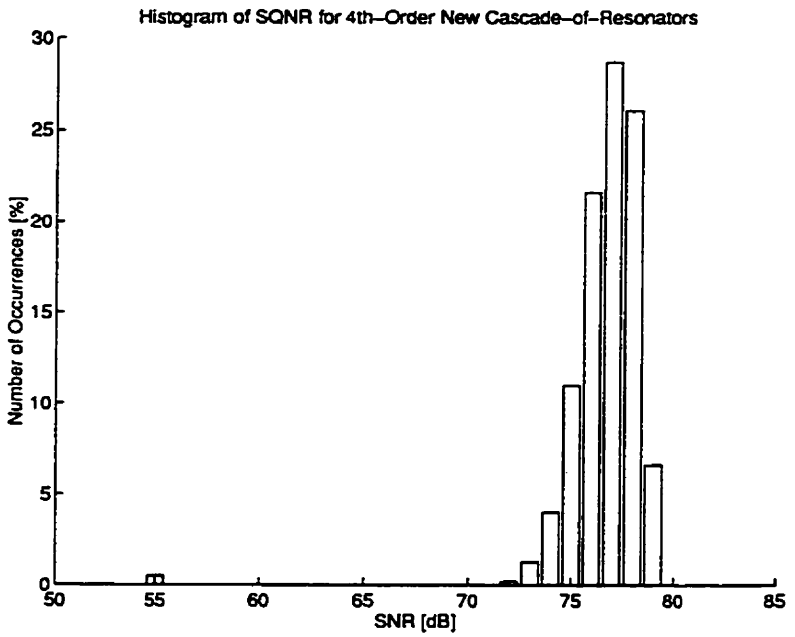

Figure 4.23: **Histogram of SQNR for the 4-th Order New Cascade-of-Resonators.**

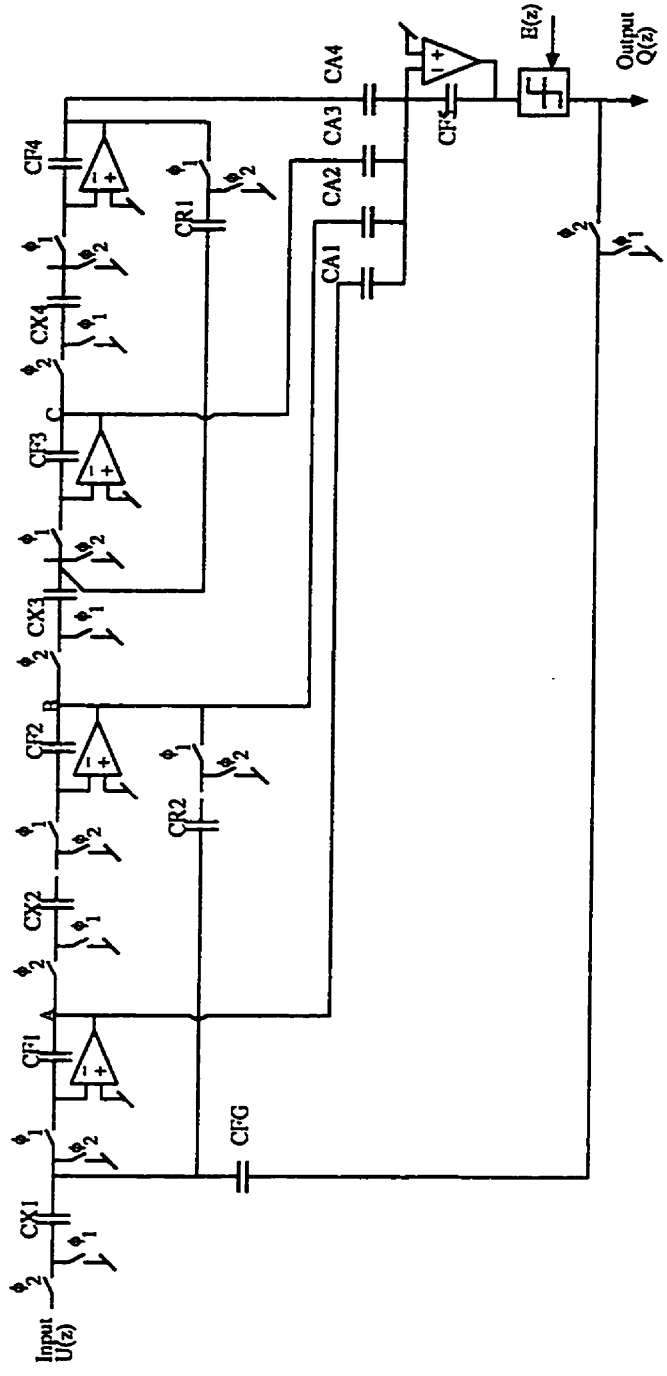

Figure 4.24: **Switched-Capacitor Implementation of the 4-th Order New Cascade-of-Resonators.**

A_1	$CA1/CF5$
A_2	$CA2/CF5$
A_3	$CA3/CF5$
A_4	$CA4/CF5$
R_1	$-CR1/CF3$
R_2	$-CR2/CF1$

Table 4.15: **Relationship Between Multiplier Coefficients and Capacitor Ratios.**

Section 4.5.7, the final capacitor values are given in Table 4.16.

$CX1$	14.1432513	$CF1$	16.0059175
$CX2$	1	$CF2$	3.0813820
$CX3$	1.9122152	$CF3$	9.5660113
$CX4$	1	$CF4$	3.8174262
CFG	14.1432513	$CF5$	2.7302077
$CA1$	-2.7889462	$CR1$	1
$CA2$	-3.6366238	$CR2$	1
$CA3$	-4.5106545		
$CA4$	-1		

Table 4.16: **Final Capacitor Values For the SC Implementation of the New Cascade-of-Resonators.**

The total capacitance is 81.34 and the capacitor value spread is 16.01.

4.8.5 Comments of the Performance of the New Structure

The cases where the converter becomes unstable discarded, the Monte-Carlo analysis of the new Σ-Δ converter configuration proves the structure to behave as expected. Its main characteristics include the zeros of the noise transfer function on the unit circle, a very efficient way of minimizing the

effect of non-ideal component values, and complementary transfer functions ensuring a minimal signal distortion in the low-noise frequency band.

The switched-capacitor implementation also shows a reduced capacitor spread as compared to the cascade-of-integrators (16.0 vs. 72.02) as well as a total capacitance reduced by half. All these considerations lead to the conclusion that the proposed resonator-based Σ-Δ converter configuration is a suitable candidate for A/D Σ-Δ conversion.

4.9 Conclusions

This chapter has reviewed the existing design techniques for bandpass Σ-Δ A/D conversion and presented a set of comparison criteria. A new Σ-Δ converter configuration based on existing structures has been presented along with its corresponding design procedure.

Section 4.2 has introduced some definitions and general considerations related to the transfer functions. Some special cases have been discussed and the important notion of transfer function complementarity has been introduced.

Section 4.3 has reviewed the design specifications relating to the noise transfer function. The general form of the noise transfer function has then been derived. This has been followed by the discussion of issues such as the order of the transfer functions. A formula for the estimation of the performance of the converter based on its noise transfer function concluded the section.

Section 4.4 has applied the results of Section 4.3 to the design of transfer functions satisfying a set of design specifications as an example. The resulting transfer functions have been applied to the design of a cascade-of-integrators

Σ-Δ converter configuration in Section 4.5. The resulting design has then been investigated and a switched-capacitor implementation of the design has been discussed.

In Section 4.6, the design (based on the results of Section 4.4) of a cascade-of-resonators has been investigated. The procedure paralleled the procedure used in Section 4.5.

Section 4.7 presented a comparative discussion of the structures synthesized in Sections 4.5 and 4.6. Comparison criteria have been established as well.

Finally, Section 4.8 has introduced a new Σ-Δ converter configuration which combines the best features of the structures synthesized in Sections 4.5 and 4.6. Its switched-capacitor implementation has been considered.

Chapter 5

Conclusions

5.1 Review of Material Presented

This thesis has been concerned with the analysis and design of higher-order (third-order or more) Σ-Δ converters.

Chapter 1 presented an overview of the basic principles of A/D conversion, leading to Σ-Δ conversion as introduced in 1962 by Inose and Yasuda [IY63]. A more specific attention to multi-loop, multi-stage and bandpass configurations has been given in this chapter.

Chapter 2 was concerned with the analysis of the quantization noise in multi-loop Σ-Δ converter configurations. The resulting mathematical derivations have than been applied to the case of triple-loop converters under sinusoidal input signal excitations. The results have been facilitated by the fact that the quantization error function is a periodic function of the input signal to the quantizer. A computer investigation confirmed the validity of the results. Finally, a discussion of the spectral characteristics of the quantization noise has justified the validity of the white noise assumption as a model for the quantizer.

In Chapter 3, a new approach to the design of Σ-Δ converters has been proposed. The leading idea was to enumerate all the possible connections between the elements that compose the Σ-Δ converter configuration. This method has then been applied to the design of first-order structures. A new structure for lowpass Σ-Δ conversion based on bilinear-LDI integrators has been introduced along with the idea of highpass Σ-Δ conversion.

Chapter 4 has discussed the design of bandpass Σ-Δ converters. The design criteria for the transfer functions have been discussed and a set of transfer functions have been successfully designed to meet specific design specifications. Two known structures have then been designed and compared. Comparison criteria were derived from a practical point of view. Of particular interest is the use of the notion of complementary transfer function. Finally, a new resonator-based structure has been proposed. A design and a subsequent comparison with the existing structures has been presented. Through the discussion, it appeared that the proposed new structure exhibits the best features of both known structures as it exhibits complementary transfer functions and has a low sensitivity to parameter variations. This new structure seems to be well suited for switched-capacitor implementation.

5.2 Original Contributions

To the best of the author's knowledge, the following contributions are believed to be original.

5.2.1 Chapter 2

- The open-loop equivalent for multi-loop Σ-Δ converter configurations (Section 2.1).

- The closed-form solution for the triple-loop Σ-Δ converter configuration with sinusoidal input signal excitations (Section 2.2).

5.2.2 Chapter 3

- The new approach to the design of Σ-Δ converter configurations.
- The new LDI-integrator based lowpass Σ-Δ converter (Section 3.4.2).
- The notion of highpass Σ-Δ conversion (Section 3.5).

5.2.3 Chapter 4

- The exploitation of the concept of transfer function complementarity (Section 4.2).
- The general form for the noise transfer function (Section 4.3).
- The use of matrices for the design of Σ-Δ converters (Sections 4.4, 4.5, and 4.6).
- The comparison criteria in Section 4.7.
- The new structure in Section 4.8.

5.3 Proposed Areas for Future Work

This thesis has presented several design techniques for the synthesis of Σ-Δ converters. In particular, the technique developed in Chapter 3 can be useful for the discovery of new Σ-Δ converters. In spite of the complexity of the search space, this technique can be applied to second or higher-order

structures in an attempt to discover new configurations. A more formal description of the proposed technique should also be investigated.

The comparison criteria proposed in Section 4.7 could be applied to other new structures. The analysis of a lattice-based structure such as the one in Fig. A.1 in Appendix A.2 or other structures should be attempted as well as their switched-capacitor implementation.

5.4 Concluding Remarks

From a more personal point-of-view, I admit I regret to have to wrap up the research work after just two years. As I am now well acquainted with the field of Σ-Δ conversion, every day brings a new idea or a new concept to explore. Eighteenth-Century French playwright Beaumarchais once wrote in his masterpiece "The Barber of Seville" : "*La difficulté d'aboutir ne fait qu'ajouter à la nécessité d'entreprendre*". A sentence that can be translated as "Obstacles to success only add to the necessity to undertake". If research is indeed difficult to undertake as this quotation may imply, the rewards associated with success make it worthwhile to be considered. I am very proud to have been part of a research group and to have helped, in a modest way, to further the understanding of the world that surrounds us, even though the present work is only a small brick in the wall of Knowledge.

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Appendix A

Appendix

A.1 Proof of Lemma 2

The proof of Lemma 2 will be given by mathematical induction.

The lemma holds true for $N = 1$. In this case, Eqn. (2.29) becomes

$$\sum_{l_1=1}^{n-1} u(l_1) = \sum_{k=1}^{n-1} \begin{pmatrix} 1-1+(n-1)-k \\ 1-1 \end{pmatrix} u(k). \tag{A.1}$$

Expanding the binomial coefficient yields

$$\sum_{l_1=1}^{n-1} u(l_1) = \sum_{k=1}^{n-1} \begin{pmatrix} n-1-k \\ 0 \end{pmatrix} u(k) \tag{A.2}$$

$$= \sum_{k=1}^{n-1} u(k). \tag{A.3}$$

Therefore, it is sufficient to prove that if the lemma holds true for $N = M$, then it is also true for $N = M + 1$.

When $N = M + 1$, the left-hand part of the equality in Eqn. (2.29)

becomes

$$\sum_{l_{M+1}=1}^{n-1} \sum_{l_M}^{l_{M+1}} \sum_{l_{M-1}}^{l_M} \cdots \sum_{l_2=1}^{l_3} \sum_{l_1=1}^{l_2} u(l_1). \tag{A.4}$$

Equivalently, Eqn (A.4) can be rewritten

$$\sum_{l_{M+1}=1}^{n-1} \left(\sum_{l_M=1}^{(l_{M+1}+1)-1} \sum_{l_{M-1}=1}^{l_M} \cdots \sum_{l_2=1}^{l_3} \sum_{l_1=1}^{l_2} u(l_1) \right). \tag{A.5}$$

But Lemma 2 is assumed to hold true for $N = M$. Therefore, Eqn. (A.5) becomes

$$\sum_{l_{M+1}=1}^{n-1} \sum_{k=1}^{l_{M+1}} \binom{M-1+l_{M+1}-k}{M-1} u(k). \tag{A.6}$$

Expanding the summations in Eqn. (A.6) yields

$$\overbrace{\binom{M-1+1-1}{M-1} u(1) +}^{l_{M+1}=1}$$

$$\overbrace{\binom{M-1+2-1}{M-1} u(1) + \binom{M-1+2-2}{M-1} u(2) + \cdots}^{l_{M+1}=2}$$

$$\cdots + \overbrace{\binom{M-1+(n-1)-1}{M-1} u(1) + \binom{M-1+(n-1)-2}{M-1} u(2) + \cdots +}^{l_{M+1}=n-1}$$

$$\overbrace{\cdots + \binom{M-1+(n-1)-(n-1)}{M-1} u(n-1).}^{l_{M+1}=n-1} \tag{A.7}$$

After regrouping the terms $u(\cdot)$ with similar arguments, Eqn. (A.7) becomes

$$\sum_{k=0}^{n-2} \begin{pmatrix} M-1+k \\ M-1 \end{pmatrix} u(1) + \sum_{k=0}^{n-3} \begin{pmatrix} M-1+k \\ M-1 \end{pmatrix} u(2) + \cdots$$
$$\cdots + \sum_{k=0}^{0} \begin{pmatrix} M-1+k \\ M-1 \end{pmatrix} u(n-1). \tag{A.8}$$

Using the identity [Spi68, Eqn. 3.9]

$$\sum_{k=0}^{m} \begin{pmatrix} n+k \\ n \end{pmatrix} = \begin{pmatrix} n+m+1 \\ n+1 \end{pmatrix}, \tag{A.9}$$

Eqn. (A.8) becomes

$$\begin{pmatrix} M+(n-1)-1 \\ M \end{pmatrix} u(1) + \begin{pmatrix} M+(n-1)-2 \\ M \end{pmatrix} u(2) + \cdots +$$
$$\begin{pmatrix} M+(n-1)-(n-1) \\ M \end{pmatrix} u(n-1). \tag{A.10}$$

Regrouping the terms gives

$$\sum_{k=1}^{n-1} \begin{pmatrix} M+(n-1)-k \\ M \end{pmatrix} u(k). \tag{A.11}$$

Using $N = M + 1$, Eqn. (A.11) becomes

$$\sum_{k=1}^{n-1} \begin{pmatrix} N-1+(n-1)-k \\ N-1 \end{pmatrix}, \tag{A.12}$$

establishing the proof of the Lemma for $N = M + 1$. *Q.E.D.*

A.2 Lattice-based Σ-Δ Converter Configuration

Fig. A.1 presents the schematic diagram for a lattice-based Σ-Δ converter configuration.

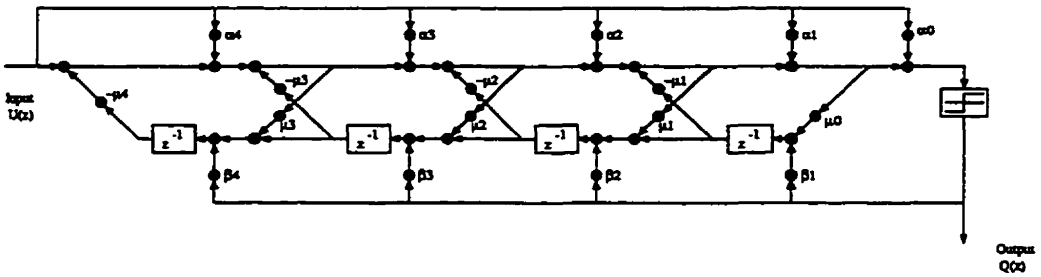

Figure A.1: **Lattice-based Σ-Δ Converter Configuration.**