UNIVERSITY OF CALGARY

Harmonic Reduction Analysis of Synchronized Phase-shifted Parallel PWM Inverters

by

Nacer Benaifa

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE

DEGREE OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

CALGARY, ALBERTA

JANUARY 2008

UNIVERSITY OF CALGARY

FACULTY OF GRADUATE STUDIES

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled "Harmonic Reduction Analysis of Synchronized Phase-shifted Parallel PWM Inverters" submitted by Nacer Benaifa in partial fulfilment of the requirements of the degree of Master of Science

Supervisor Dr E P Nowicki
Dept of Electrical and Computer Engineering

Dr Om P Malik
Dept of Electrical and Computer Engineering

Dr Ahmed Osman
Dept of Electrical and Computer Engineering

Dr Qiao Sun
Dept of Mechanical and Manufacturing Engineering

Jan 15, 2008

Date

Abstract

Renewable energy sources are quickly becoming incorporated into increasingly distributed electrical utility grids. An ever present issue when interfacing these sources is that of harmonic distortion reduction at the inter-tie point. Presented in this thesis is a rarely employed technique for harmonic reduction using synchronized phase shifted parallel PWM inverters with current-sharing reactors.

Our investigation includes analytical, simulated and experimental analyses for one inverter, as well as for two, and three, phase-shifted inverters operated in parallel using two carrier based modulation strategies with various modulation indices and carrier to reference frequency ratios. Our analyses, using three figures of merit, consider also the impact of a wide range of phase-shift delays between parallel inverters on the net output harmonic distortion.

Acknowledgements

I would like to take this opportunity to thank my supervisor Dr. Ed Nowicki for his constant support, advice and encouragement throughout the course of my study at the University of Calgary. Thank you very much Dr. Nowicki.

Dedication

To my beloved mother.

Table of Contents

List of Tables

List of Figures

List of Symbols, Abbreviations and Nomenclature

Acronyms	Definition
AC	Alternating current
BJT	Bipolar junction transistor
CSI	Current source inverter
DC	Direct current
IDE	Integrated development environment
IDP	In-phase disposition
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated gate bipolar transistor
MOSFET	Metal–oxide–semiconductor field-effect transistor
NPC	Neutral point clamped
NSPWM	Naturally sampled pulse width modulation
p.u.	Per unit
PIC	Programmable intelligent computer
PWM	Pulse width modulation
rms or RMS	Root mean square
RSPWM	Regularly sampled pulse width modulation
SHE	Selective harmonic elimination
SHM	Selective harmonic minimization
SPWM	Sinusoidal pulse width modulation
THD	Total harmonic distortion
VSI	Voltage source inverter
WTHD	Weighted total harmonic distortion
WTHD0	WTHD normalized to the inverter DC voltage

Mathematical Symbols	
fc	Frequency of the carrier waveform
fs	Frequency of the reference sine waveform
M	Modulation index
N	Number of parallel inverters
P = fc/fs	Carrier to sine reference frequency ratio
Tc	Period of the carrier waveform
Ts	Period of the reference waveform

Chapter One: INTRODUCTION

1.1 Power Electronics

Power electronics [1-4] is concerned with the economical design and control of efficient semi-conductor based electrical circuits that convert electrical energy from one form of dc or ac into another form that is near optimal for a given load. A power converter, or power conditioner, consists of one or more power semi-conductor switching devices and reactive components that operate in accordance with control electronics, often in the form of a microcontroller. A power converter converts electrical energy from one level of voltage (or current) and/or frequency to another level of voltage (or current) and/or frequency using the controlled semi-conductor power switches. Fig. 1.1 presents a classification of power electronic converters according to their type of electrical conversion.

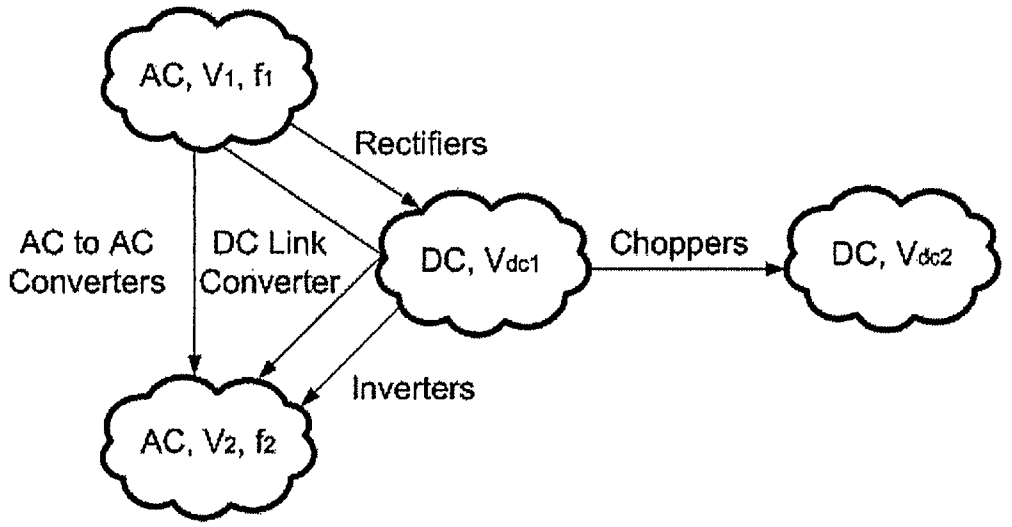


Fig. 1.1 Classification of power converters according to their conversion type.

The motivation for using a semi-conductor device in its switching mode (ie, the device is ideally in either the on or off state), as opposed to the linear-mode of operation, is to increase conversion efficiency, while decreasing size, weight, and cost. Power electronics has more to do with efficiency unlike linear analog electronics which is more

concerned with high performance (e.g. an audio power amplifier has low noise operation but is much less efficient and is heavier than a power converter rated for the same power output).

Converters that convert dc to ac are known as inverters. Generally speaking, an inverter may be classified as a voltage source inverter (VSI) or as a current source inverter (CSI). A voltage source inverter is an inverter fed by a stiff (ie, low impedance) dc voltage (ie, its voltage is not significantly affected by the variations in current flowing through it) whereas a current source inverter is fed by a stiff current source (ie, a source with near infinite internal impedance; its current is not significantly affected by the variations in voltage across its terminals).

Conventional power electronic inverters can switch connections from input to output such that two possible voltage levels appear at the output, namely the positive or negative of the dc input (sometimes a zero voltage level is also used at the output). Multilevel converters can switch connections to permit many voltage levels at the output, and have multiple dc input voltages (or simply capacitors) as part of their structure.

In this thesis we will be dealing solely with voltage source inverters and more precisely with paralleling inverters to emulate the operation of a multilevel inverter.

1.2 Pulse Width Modulation

The process of controlling the switching pattern of the semi-conductor devices in a power converter is sometimes referred to as modulation, and the development of near optimal strategies to implement this process has been the subject of intensive research efforts for the past 30 years or so.

The problem stems from the fact that basic square wave modulated inverters have outputs that are rich in harmonics and therefore need heavy filtering [5]. This problem can be solved using pulse width modulated (PWM) inverters which results in an output frequency spectrum having harmonics that are "pushed" to higher frequencies [6]. The concept of PWM is to vary the duty cycle of the converter switches at a high switching frequency to obtain a target average low frequency output voltage and hence the harmonic components in a PWM inverter output are easily filtered because they are

shifted to higher frequencies. Therefore the PWM technique is extensively used by industry in modern industrial power electronics including inverter design. Pulse width modulation has also been a major research area in power electronics community and continues to attract much attention and interest. This is expected, as pulse width modulation, in one form or another, is at the core of nearly every modern power converter, and improvements in this technology continue to be welcomed by industry.

1.3 Power Quality Concept

At present there is an increasing concern about the quality of power delivered to commercial, industrial, and residential sites. This is due, in part, to a reaction to some of the deleterious effects of harmonic-creating systems in use.

Math H. J. Bollen in [7] defines "Power Quality" as: "Power quality is the combination of voltage quality and current quality. Voltage quality is concerned with deviations of the actual voltage from the ideal voltage. Current quality is the equivalent definition for the current." where "the ideal voltage is defined as a sinusoidal voltage waveform with constant nominal amplitude and constant nominal frequency, and the ideal current is also of constant amplitude and frequency with its frequency and phase being the same as the frequency and phase of the voltage producing it".

The phenomena that mostly affect power quality can be characterized as one of the following categories [8]:

- Harmonic distortion;
- Supply interruption;
- Voltage swells;
- Voltage sags;
- Transients.

Harmonic distortion is one of the main issues of present day power quality deterioration because of the growing use of non-linear (power converter) loads and at the same time, the growing use of sensitive electronic loads. In power electronic circuits such as rectifiers (ac to dc converters), nonlinearity is the direct result of turn-on and turn-off operation of the semi-conductor switches that results in distortion of the waveforms, and

hence rectifiers often draw distorted line current from the utility supply. In addition traditional phase-controlled rectifiers have notches in the utility voltage waveforms. The resultant distorted current and voltage waveforms are "injected" into and "pollute" the power system and can have many effects on power system components and loads including resonance, reduced life-time of rotating machines, "nuisance trips" of power system protection devices, errors in power measurements, increased losses etc. Many commercial and residential electronic products in use today are susceptible to damage resulting from poor power quality issues; for example, one may loses work as a result of a computer shutdown or reboot which may be caused by poor power quality on the single-phase 120V line.

To address the growing power quality problem, many working groups have been formed to discuss power quality issues [9-11]. In North America the Institute of Electrical and Electronics Engineers (IEEE) has done much to define, detect, and mitigate poor power quality events. For example, IEEE Standard 519-1992 [10], titled "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems" addresses limits to harmonics and power quality events at the point of common coupling in power systems. One of the guidelines of this standard is setting the maximum permissible Total Harmonic Distortion (THD) for low-voltage applications to 5% and the maximum individual voltage harmonic to 3%.

1.4 Harmonic Distortion Factors

In order to measure and characterize current and voltage deviations from the ideal many indices have been proposed by power system engineers [6, 11-12].

Total Harmonic Distortion (THD) is the traditional and most commonly used performance measure (a higher THD indicates poorer performance); corresponding to the energy content of the waveform harmonics, and may be defined as,

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \qquad \text{with } V_1 \neq 0 \qquad (1.1)$$

where V_1 is the rms value of the fundamental-component voltage and V_h is the rms value of the h^{th} harmonic voltage component. Sometimes, the first 50 harmonics are used for calculation of THD (ie, we replace infinity by 50 in eqn. (1.1)) as suggested in the IEEE Standard 519 [10].

Fortunately the inherent distribution inductances in power systems cause higher order current harmonics to be attenuated. This means that high order harmonics are not as severe as a lower order harmonics in such cases. THD, however, disregards this distinction and includes all harmonics with equal weighting. Another performance measurement, known as the Weighted THD (WTHD) gives an alternative measure of harmonic distortion using the order of each harmonic component as a weighting factor [6, 11]. WTHD is defined as,

$$WTHD = \frac{\sqrt{\sum_{h=2}^{\infty}\left(\frac{V_h}{h}\right)^2}}{V_1} \qquad \text{with } V_1 \neq 0 \qquad (1.2)$$

A key issue with the above mentioned two figures of merit (THD and WTHD) as defined in eqn. (1.1) and eqn. (1.2) is the fact that those factors approach infinity if the fundamental component voltage approaches zero (ie, as the modulation index approaches zero in a dc fed power inverter), which clearly will not reflect the quality of converter operation accurately. The problem can be avoided by employing a reference quantity which is invariant; one such a constant is the dc voltage feeding an inverter. Such a figure of merit is denoted by WTHD0, and defined as,

$$WTHD0 = \sqrt{\sum_{h=2}^{\infty}\frac{1}{h^2}\left(\frac{V_h}{Vdc}\right)^2} \qquad \text{with } V_{dc} \neq 0 \qquad (1.3)$$

In this thesis we will be giving, in most cases, all the above three performance measures, even though THD remains the primary performance factor due to its ubiquitous use.

1.5 Thesis Motivation

Inexhaustible and environment friendly renewable energy sources such as wind, photovoltaic and fuel cell energy sources are becoming increasingly incorporated into increasingly distributed electrical utility grids. An ever present issue when interfacing these sources to the grid is that of harmonic distortion reduction at the grid inter-tie point (the point of common coupling). One very interesting approach to reduce harmonic distortion is to synchronize power transistor operation for inverters operating in parallel [13, 15].

In this thesis we endeavour to investigate and extend the body of knowledge about a rarely employed, possibly underutilized, technique for harmonic reduction. The undertaken task is an in-depth and methodological analysis of opportunities for harmonic reduction with carrier based Pulse Width Modulation (PWM) of synchronized phase-shifted parallel-operated inverters using current sharing reactors for the cases of one, two and three inverters. We limit the number to three, partly to reasonably curtail the investigation, but also because the incremental gains of synchronization decrease as the number of inverters increases.

With the increasing interest in renewable energy sources, we expect an increased attention in the near future to be given to parallel operation of multiple inverters.

1.6 Thesis Objective

The objective of the research work is to investigate analytically and by simulation as well as experimentally, the opportunities for harmonic reduction of synchronized phase-shifted inverters operating in parallel using current sharing reactors and modulated with carrier based PWM. The cases of one, two and three inverters operated in parallel are thoroughly analysed and the validity of our theoretical considerations and results is verified experimentally.

1.7 Thesis Outline

This thesis is composed of six chapters which present analytical, simulation and experimental results regarding the evaluation and characterization of several techniques

to reduce the harmonic content of power inverters with emphasis on parallel synchronously operated PWM inverters.

Chapter 2 presents background about PWM techniques, followed by a discussion of conventional multilevel inverters, and concludes with a discussion about parallel operation of inverters.

In Chapter 3 we discuss in greater detail alternative PWM methods including those methods adopted for the research underlying this thesis. In particular we employ double-edge naturally sampled PWM and double-edge asymmetrical regularly sampled PWM. The merits of the natural sampling process (ie, lower values of weighted distortion) are contrasted with the uniform sampling process.

In Chapter 4, we present simulation results (using MATLAB/Simulink and PSpice), including Fourier series analyses for a wide range of operating conditions. We include several figures of merit to characterize the harmonic content, as discussed above.

In Chapter 5, the experimental results corresponding to a sub-set of cases examined in Chapter 4 are presented. As expected, the experimental cases have slightly higher harmonic components than in the corresponding simulation cases. However the agreement is generally very good.

The conclusions of this thesis and some suggestions for future work are presented in Chapter 6.

Chapter Two: PARALLEL INVERTER OPERATION AS A MULTILEVEL CASE

2.1 Introduction

An inverter is a semi-conductor converter fed by a low-ripple dc input that produces an ac output. The semi-conductor devices in the inverter operate ideally in one of two modes, either "on" or "off". The inverter requires a control circuit (often a microcontroller) that provides the necessary gating signals to turn on and turn off each of the switching devices with the correct timing and relative sequence. In the most basic type of inverters, the switches are continuously operated in such a way as to deliver either the positive or negative dc input voltage to the inverter output ac terminals. An inverter may operate in an open-loop, or autonomous manner, if the turn-on and turn-off of the switches depends only on the switch controller with no system signals fed to the controller.

Static, ie, semi-conductor, inverters may be classified, based on their structure, as one of these two types [2]:

- Voltage-source inverter (VSI)
- Current-source inverter (CSI)

A VSI is fed by a dc-voltage supply while a CSI is fed by a dc-current supply. The output current or voltage of a CSI or VSI may be a simple square-wave, or square-wave-like (sometimes called a modified square-wave, ie, a zero voltage or current is placed between positive and negative inverter output half-cycles). If there is not a significant decrease in efficiency, it is very common today to have each half-cycle of the inverter output composed of several pulses, and sometimes these pulses have their pulse-width controlled to be proportional to a reference sine wave and hence the inverter is said to be pulse width modulated (PWM). Arguably one can say an inverter is PWM controlled even if there is only one voltage or current pulse in each half-cycle if the pulse width is controlled to vary the rms output voltage or current. In this thesis we will deal solely with the pulse width modulated autonomous VSI.

2.2 VSI Topologies

Voltage source inverter (VSI) is the most commonly used type of inverter. The ac that it provides on the output side functions as a low-impedance ac voltage source. The input is from a low-ripple dc voltage source having negligible internal impedance. The input dc voltage may be from the rectified output of an ac power supply, or from an independent source such as a battery (or set of batteries).

There are two circuit topologies commonly used for single-phase inverters. They are, (a) the half-bridge topology and (b) the full-bridge topology. For certain low power applications, the half-bridge inverter may suffice. The full-bridge inverter is more popular than the half-bridge and permits convenient adjustment of the output voltage by pulse width modulation techniques. Fig. 2.1 shows the half and full bridge configurations. The input dc voltage, here again, may be from the rectified output of an ac power supply, or from an independent source such as a batteries, solar cell, etc. In this thesis, we are mainly dealing with advanced pulse width modulation strategies, and so, the half-bridge topology will not be considered further.

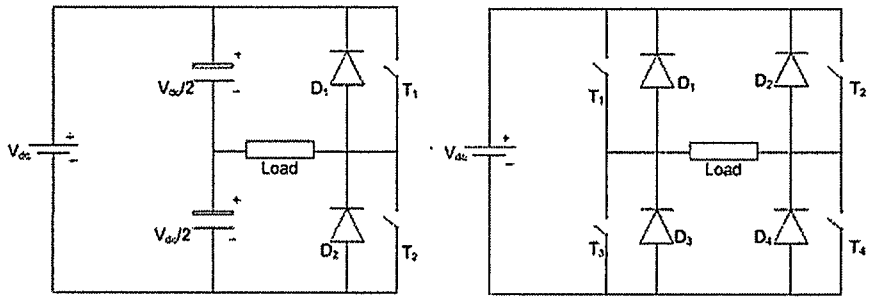


Fig. 2.1 (a) Half-bridge inverter; (b) Full-bridge inverter

2.3 Pulse Width Modulation

The process of controlling the switching pattern of the semi-conductor devices in a power converter is sometimes referred to as modulation, and the development of near optimal strategies to implement this process has been the subject of intensive research efforts for the past 30 years [6].

There are two benefits of PWM. The required filtering components can be made smaller and thus cost less because PWM has the effect of pushing the harmonics to higher frequencies. In addition, PWM permits the control of the output voltage fundamental amplitude.

2.3.1 Pulse Width Modulation Principles

Fig. 2.2 illustrates the output waveform of the PWM-controlled full-bridge VSI, along with the gating signals of switches T_1 to T_4 shown in Fig. 2.1(b). The particular waveform shown in Fig. 2.2(a) is often referred to as a modified square-wave, since it resembles a square-wave other than the zero-voltage states between positive and negative output voltage excursions. As seen in Fig. 2.1 (b), switching transistors in one leg (e.g. T_1 and T_3 compose one leg of the inverter) cannot be turned on simultaneously as this will short-out the dc input supply. In order to obtain the modified square-wave shown in Fig. 2.2(a), the transistors of the full-bridge inverter in Fig. 2.1 (b) can be gated as shown in Fig. 2.2(b). Consider one cycle of the ac output, beginning at time t1 in Fig. 2.2(a). From t1 to t2, transistors T1 and T4 should be on, to provide the desired positive output voltage. And from t3 to t4, transistors T2 and T3 should be on, to provide the desired negative output voltage. Note the two other intervals in each cycle, namely for t2 to t3 and from t4 to t5, having zero output voltage. These are sometimes called "zero voltage freewheeling" intervals since the current in the inverter output cycles through, or freewheels through, the inverter without passing through the dc source. Therefore, for the modified square-wave PWM technique, there are four intervals per cycle of the output waveform. Interval 1 from t1 to t2 produces a positive output voltage. Interval 2 from t2 to t3 produces zero output voltage while load current freewheels through the top transistors of the inverter. Interval 3 from t3 to t4 produces a negative output voltage. And interval 4 from t4 to t5 produces zero output voltage while load current freewheels through the bottom transistors of the inverter. Intervals 1 and 3 are usually of the same duration. Intervals 2 and 4 are usually also of the same duration. The actual length of time for the intervals is determined by the desired output frequency as well as the desired output rms voltage [4].

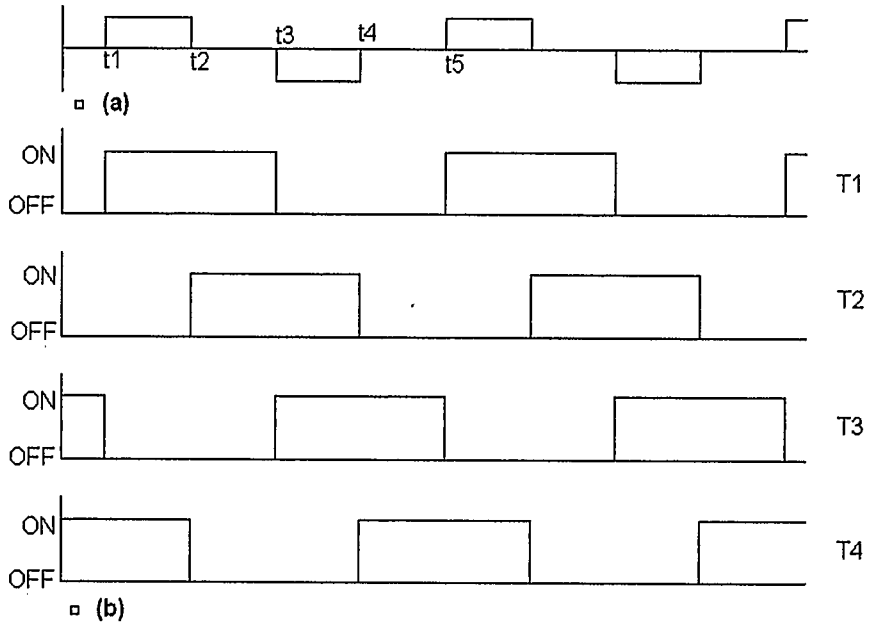


Fig. 2.2 (a) PWM modified square-wave output voltage for a single-phase full-bridge VSI; (b) Timing diagram of switches T1, T2, T3 and T4 of figure 2.1 (b)

2.3.2 PWM Implementation

There are many different ways of generating PWM switching patterns, but any technique can probably be placed into one of the following three categories [19]:

- Off-line or Pre-Calculated PWM techniques
- Hysteresis control
- Carrier based PWM.

2.3.2.1 Selective Harmonic Elimination

The following discussion illustrates the method by which inverter transistor gating times can be pre-calculated and later stored in non-volatile memory of a microcontroller based inverter control system for the case of Selective Harmonic Elimination (SHE) method [20, 21].

The cascaded H-bridge topology (see section 2.4.1) can be controlled to give a stepped waveform as in Fig. 2.3.

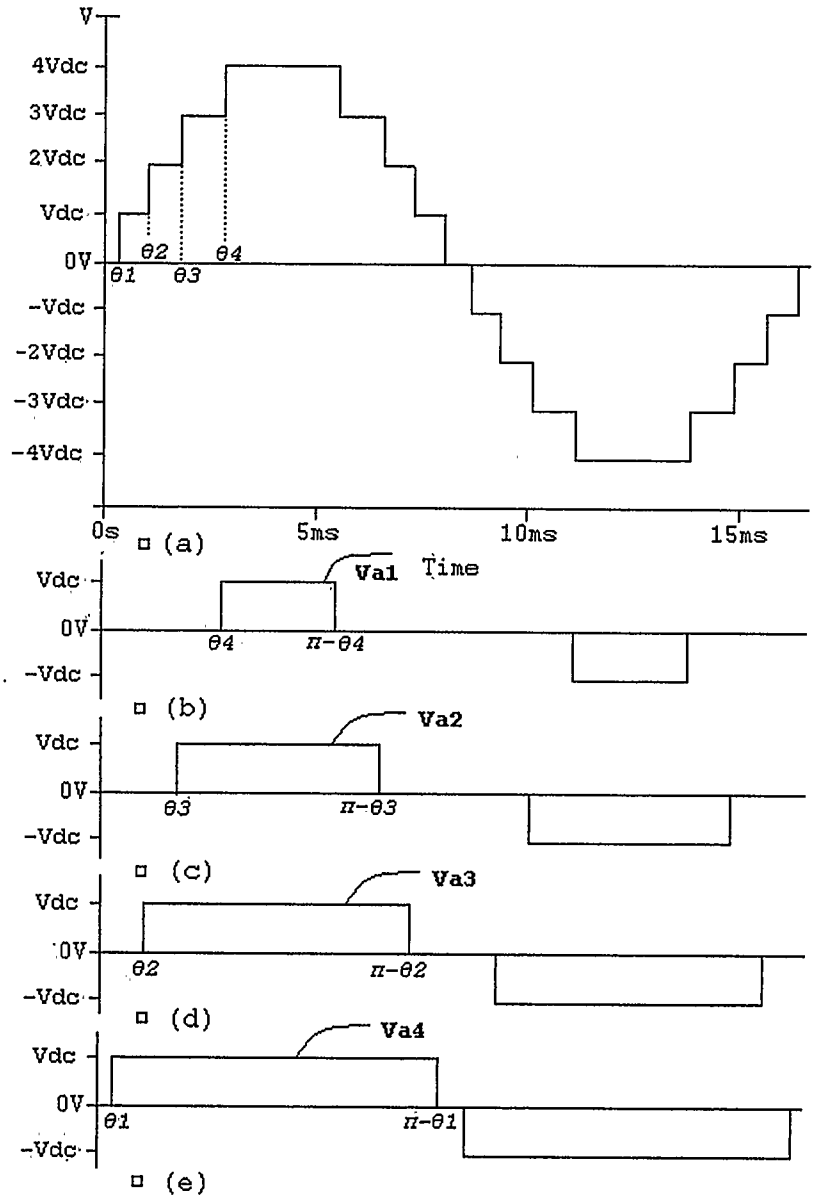


Fig. 2.3 (a) The 9 Level output voltage waveform of a cascaded inverter with 4 separate dc sources; (b) to (e) show the outputs of the individual cells.

The general case Fourier series of the stepped inverter waveform, similar to the one shown in Fig. 2.3, can be derived as in [20] to give:

$$F(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n} [\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_k)] \frac{\sin(n\omega t)}{n} \qquad (2.1)$$

for $0 \le \theta_1 < \theta_2 < \theta_3 < \theta_4 \le \pi/2$, and with n = 1, 3, 5, 7...is the order of the harmonic and k is the number of H-bridges (separate dc sources). The Selective Harmonic Elimination method is based on choosing the conducting angles $\theta_1, \theta_2, \theta_3, ..., \theta_k$ such that we eliminate the predominant lower frequency harmonics [21]. Aside from giving a low distortion resultant waveform, this also facilitates the filtering of remaining harmonics.

For the case of nine levels waveform depicted in Fig. 2.3, the 3rd, 5th and 7th harmonics can be eliminated by choosing $\theta_1, \theta_2, \theta_3$ and θ_4 such that:

$$\begin{aligned} &\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)=4M \\ &\cos(3\theta_1)+\cos(3\theta_2)+\cos(3\theta_3)+\cos(3\theta_4)=0 \\ &\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)=0 \\ &\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)=0 \end{aligned} \tag{2.2}$$

where M is the modulation index [21]. The above equations are a nonlinear transcendental system of equations that can be solved by an iterative method such as the Newton-Raphson method.

2.3.2.2 Hysteresis Current Control

The principle of hysteresis control is illustrated in Figs. 2.4 and 2.5 [22, 23]. The system structure of a hysteresis current controlled single-phase inverter is shown in Fig. 2.4. The output current of the inverter is fed back into the hysteresis controller (again, this is often a microcontroller based implementation). Shown in Fig. 2.4 is the acceptable time-dependent band, the hysteresis band, within which the output current is permitted to reside. The hysteresis controller of Fig. 2.5 calculates the error between the desired output and the measured output. The state of the switches is changed when this error exceeds a certain bound (leaves the hysteresis band) so as to drive the current back within the hysteresis band as can be seen in our simulated waveform of Fig. 2.5.

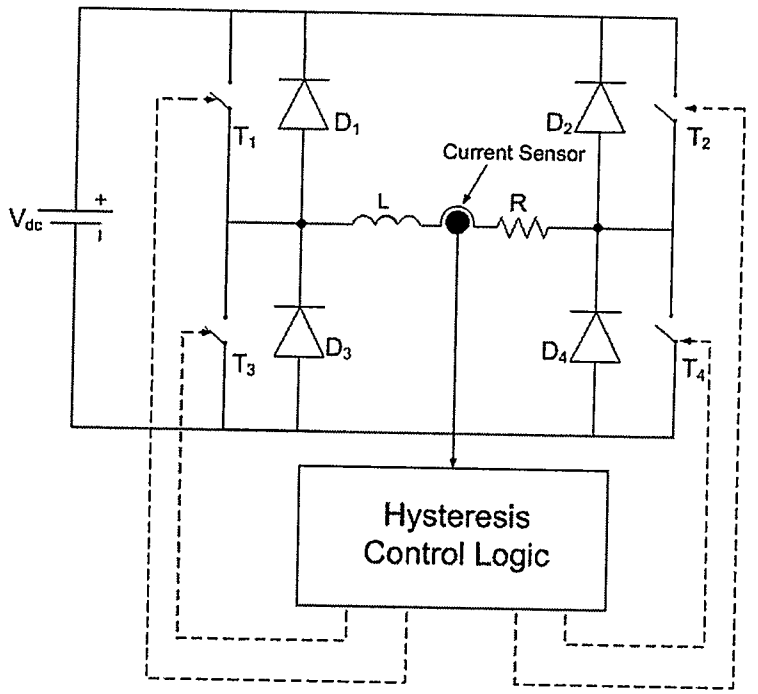


Fig. 2.4 Hysteresis current controlled inverter

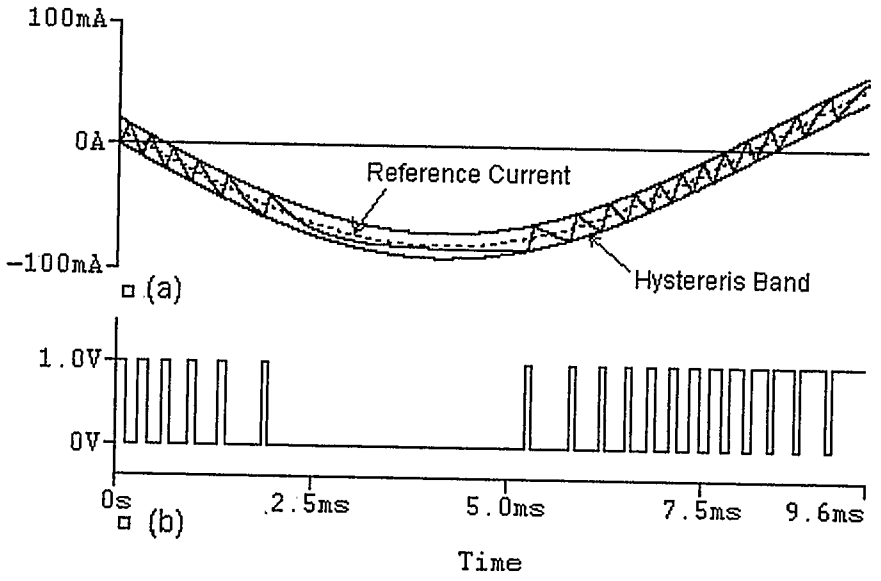


Fig. 2.5 Simulated waveform associated with the operation of an inverter under hysteresis current control; (a) Load current; (b) Switch function

2.3.2.3 Carrier based PWM

The major drawback of the off-line PWM techniques, such as Selective Harmonic Elimination, is that they need calculations that are complex and slow and are done off-line. Also a look-up table is needed by the controller that generates the gating pattern, and thus many tables may be needed to operate under a variety of conditions.

On the other hand, the hysteresis band technique, with its excellent dynamic performance and inherent current limiting ability has some drawbacks. The switch period of the hysteresis method is variable and this can lead to electromagnetic compatibility issues (ie, continuous spectrum spread) and to difficulties in ensuring transistor minimum pulse times. Also, the switching points are not synchronized to the fundamental and this can produce sub-harmonics [19].

In this thesis we will focus on carrier based PWM techniques and their application to phase-shifted parallel connected inverters. This is because carrier based PWM is straightforward to implement in analog or digital circuitry form and because it can be extended to all the multilevel parallel converter topologies discussed in this thesis.

In the next chapter we will examine in detail the two most advanced techniques of carrier based PWM [6], namely:

- Double-edge Naturally Sampled PWM
- Double-edge Asymmetrical Regularly Sample PWM

In particular, harmonic analyses of these two techniques will be performed, with an emphasize of its application to the parallel operation of voltage source inverters with a current sharing inductor for the cases of single inverter and two and three inverters operated in parallel.

2.4 Multilevel Power Inverters

Multilevel inverters provide a useful backdrop in which to discuss the parallel operation of voltage source inverters as can be seen in the next sections. Multilevel power inverters employ power semi-conductor switches in the inverter to select one or more of multiple dc voltage sources to create a staircase voltage waveform at the inverter output. Capacitors, batteries and/or renewable energy voltage sources can be used as the multiple

dc voltage sources. The control of the power switches permits the addition of the multiple dc sources in order to achieve the desired staircase waveform with high power at the output, without requiring voltage over-rating of the semi-conductor devices, in fact every device need only to be rated to the dc voltage source to which it is immediately connected

The two main advantages of multilevel inverters are the higher power capability and the reduced harmonics content of the output waveform due to the multiple levels in the output waveform [19].

The more restrictive harmonic standards now being proposed by various working groups highlight the attractiveness of multilevel inverters, since they provide a high quality voltage output, this may explain the much attention gained by multilevel power converters and the amount of research activities in the last decade.

Generally multilevel topologies can be divided into three groups [20]:

- Multistage inverters with separate dc sources
- Diode-clamped inverters
- Flying-capacitors inverters

2.4.1 Multistage Multilevel Topologies

A multistage multilevel inverter contains two or more inverter stages with output voltages that are electrically summed [20, 24- 25]. Each stage resembles the other stages; and each stage can be, for example, a single- or three-phase input rectifier plus single-phase full-bridge output voltage source inverter. Fig. 2.6 and Fig. 2.7 show a multistage inverter, consisting of three stages, that synthesizes a single-phase ac output voltage.

Note that isolated dc input voltages are required for each stage, which could be obtained with transformer fed rectifiers as shown in Fig. 2.6, or from separate dc sources (batteries, solar panels, fuel-cells, etc) as is the case of cascaded H-bridge inverter shown in Fig. 2.7. In either situation the multiple dc voltages are isolated from each other.

The purpose of the multi-pulse transformer in the transformer isolated design of Fig. 2.6 is to provide, in addition to the isolation just described, a phase shifting operation

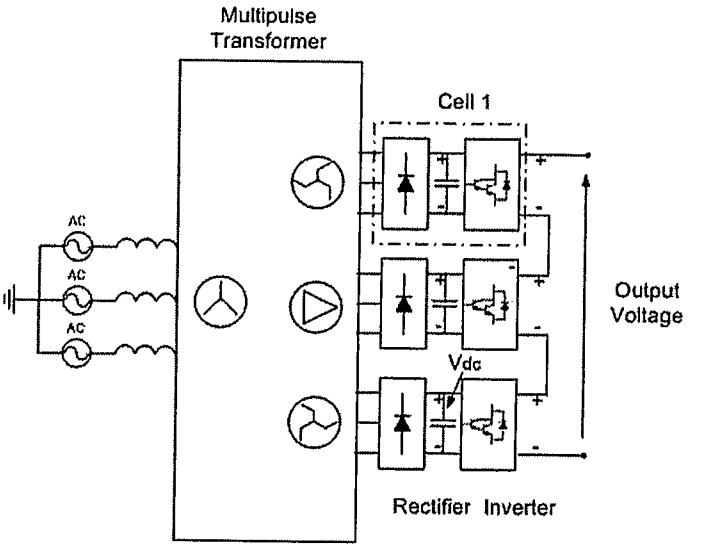


Fig. 2.6 Single-phase structure of a multilevel multistage inverter using a multipulse transformer

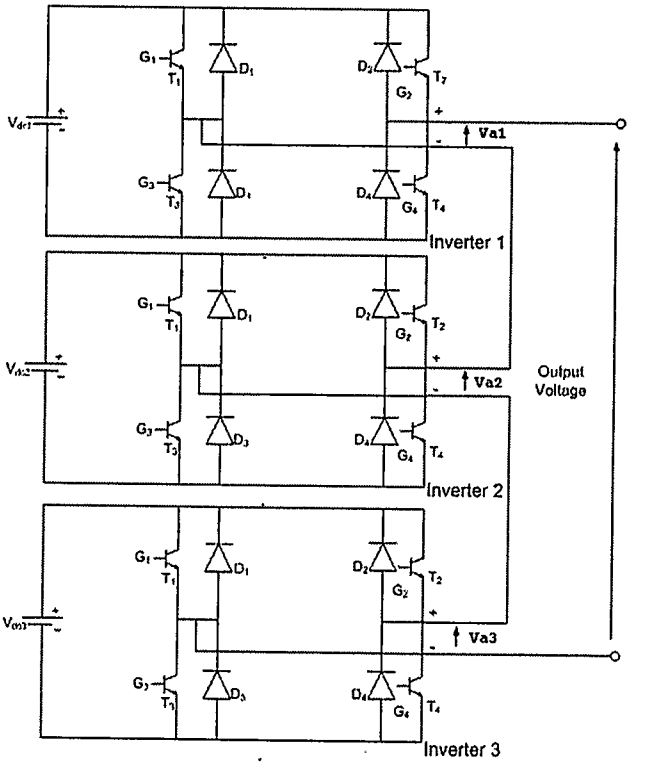


Fig. 2.7 Single-phase structure of a multilevel cascaded H-bridge inverter

applied to the rectifier input currents that produces harmonic cancellation at the grid inter-tie point, thus minimizing harmonic injection into the grid [21].

Fig. 2.8 shows the relevant simulated waveforms associated with the multistage PWM inverter, for the case of a modulation index M = 0.9 (M is defined as the ratio of the sine reference amplitude to the triangular carrier amplitude,) and a triangular carrier frequency to sine reference frequency ratio fc/fs = 11.

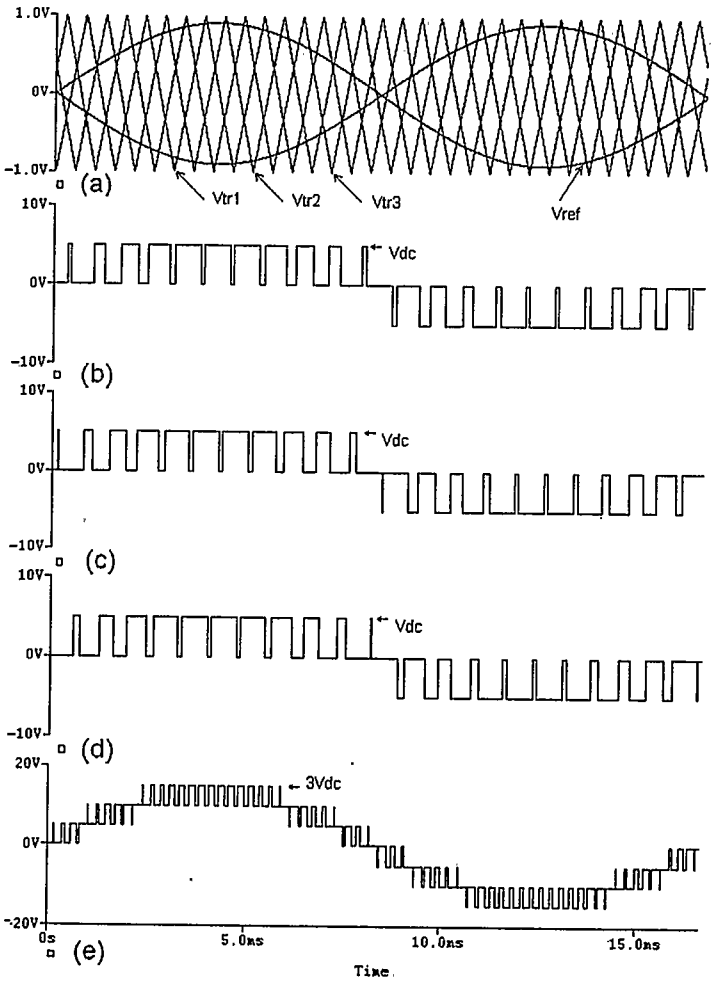


Fig. 2.8 Simulated waveform in the four-level multistage inverter using unipolar PWM with three phase shifted carriers with M = 0.9, fc/fs = 11 and V_{dc} = 5V (a) Carrier and modulating signals; (b), (c) and (d) indicate cells C1, C2, C3 output voltages respectively; (e) Output phase voltage

2.4.2 Diode-Clamped Multilevel Inverter

The diode-clamped multilevel inverter [20, 26- 27] employs clamping diodes and stacked dc capacitors on the input side to produce an ac voltage with multiple levels. A four-level single-phase diode-clamped inverter is shown in Fig. 2.9, where four-level refers to the number of inverter voltage levels during a half-cycle of operation. The inverter contains twelve semi-conductor switches and several clamping diodes. The dc supply voltage has a stack of three capacitors to provide access through the diode switching network to four dc terminals. The voltage across each capacitor is therefore one third of the dc supply V_{dc}. Table 2.1 provides the switch states and related output voltage levels obtained for one leg of the inverter.

Fig 2.11 provides the relevant simulated waveforms associated with the multistage PWM inverters shown in Fig. 2.9 and Fig. 2.10.

2.4.3 Flying-Capacitor Inverter

Fig. 2.10 shows a typical circuit topology of a four-level flying-capacitor inverter [21, 28-29]. Each inverter leg contains three complementary pairs of semi-conductor switches (e.g. in Leg one, transistor device T_1 complements device $T_{1'}$ and the same goes for (T_2, $T_{2'}$) and (T_3, $T_{3'}$) pairs. Table 2.2 provides the switch states and related output voltage levels possible for one leg of the flying-capacitor inverter.

Table 2.1 Switch status and corresponding inverter output voltages for the diode-clamped configuration (1 is on, 0 is off).

Switch State						
T_1	T_2	T_3	$T_{1'}$	$T_{2'}$	$T_{3'}$	V_a
1	1	1	0	0	0	Vdc
0	1	1	1	0	0	2Vdc/3
0	0	1	1	1	0	V_{dc}/3
0	0	0	1	1	1	0

Table 2.2 Switch status and corresponding inverter output voltages for the flying-capacitor configuration (1 is on, 0 is off).

Switch State						
T_1	T_2	T_3	$T_{1'}$	$T_{2'}$	$T_{3'}$	V_a
0	0	0	1	1	1	0
0	0	1	1	1	0	Vdc/3
0	1	0	1	0	1	V_{dc}/3
0	1	1	1	0	0	2Vdc/3
1	0	0	0	1	1	Vdc/3
1	0	1	0	1	0	2Vdc/3
1	1	0	0	0	1	2Vdc/3
1	1	1	0	0	0	Vdc

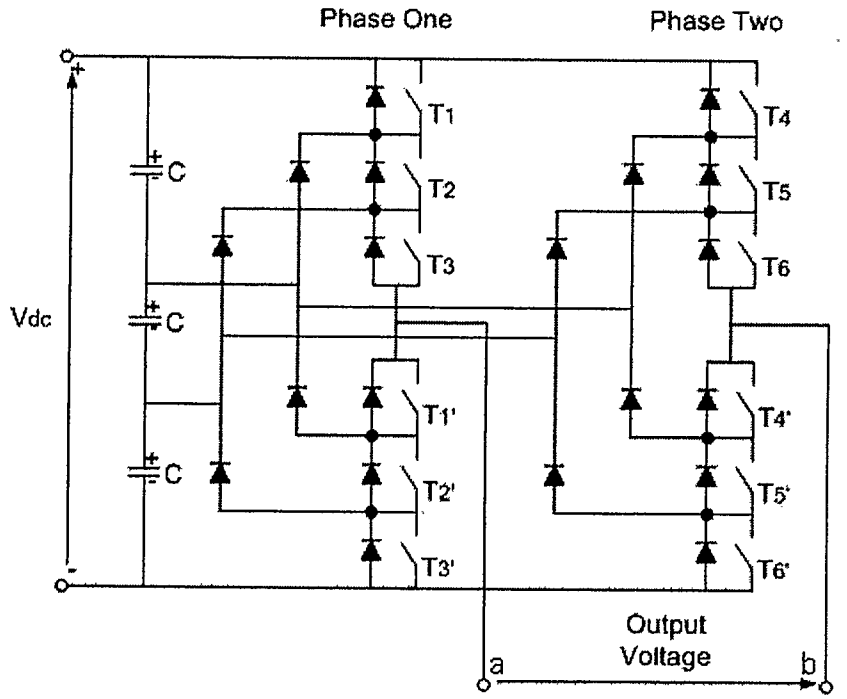


Fig. 2.9 Four-level diode-clamped inverter

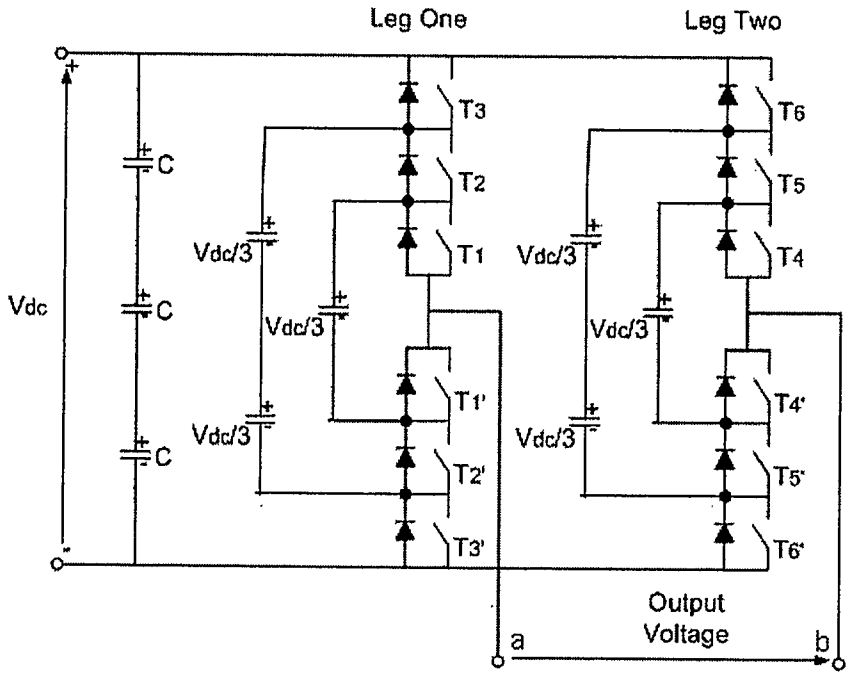


Fig. 2.10 Four-level flying capacitor inverter

Fig. 2.11 shows the relevant simulated waveforms associated with the multistage PWM inverters shown in Fig. 2.9 and Fig. 2.10 (see the footnote on this page).

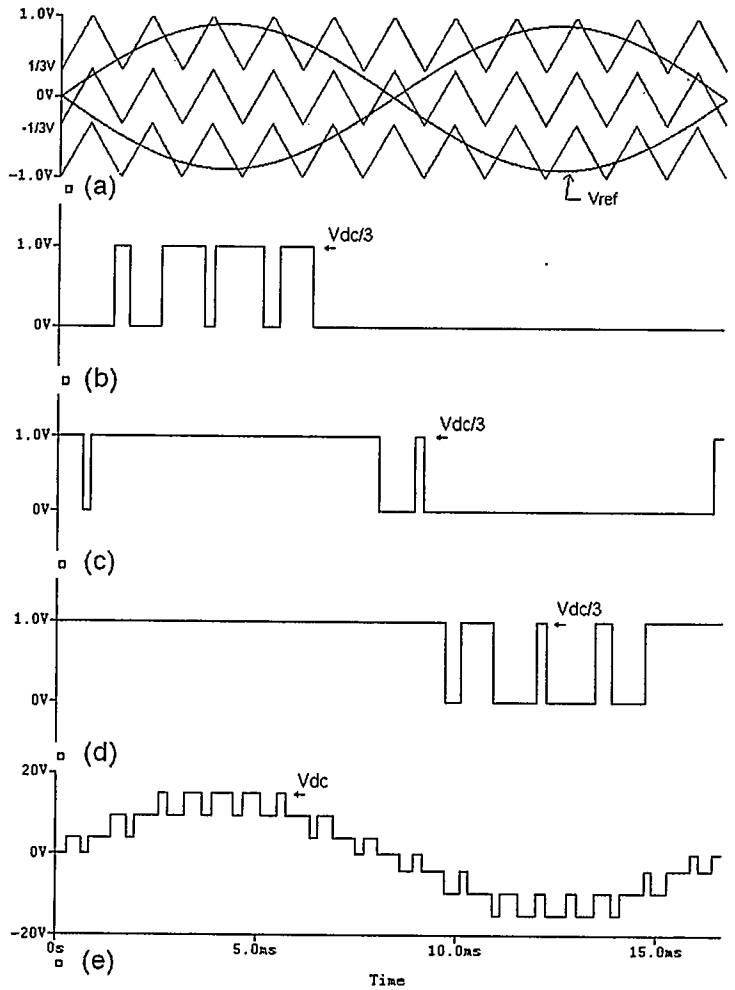


Fig. 2.11 Simulated waveform in the four-level diode-clamped (and four level flying-capacitor[1]) inverter using IPD modulation with M = 0.9, fc/fs = 11 and V_{dc} = 15V (a) Carrier and modulating signals; (b), (c) and (d) indicate transistor T1, T2 and T3 gating signals; (e) Output voltage

[1] For the implementation of the modulation scheme shown switches T_x and $T_{x'}$ denotes switches with complementary gate signal, and the switches order shown in Fig. 2.9 and Fig. 2.10 should be noted.

2.5 Parallel Inverter Operation

2.5.1 Proposed System Description

Fig. 2.12 shows the proposed parallel scheme (others have also employed this approach as discussed later in this chapter) of two and three full-bridge isolated inverters using inter-module inductors L, which act as a summing network for the current outputs of the multiple inverters. Although the load, in Fig. 2.12, is depicted as a pure resistor R, the load in our scheme can be any voltage receptor load; this will become clearer after reading next section. The H-bridges are synchronized and phases shifted relative to each other, and employ pulse width modulation as will be described in section 2.5.3. Two PWM strategies will be employed: three-level double-edge naturally sampled PWM (NSPWM) with a triangular carrier and three-level double-edge asymmetrical and regularly sampled PWM (RSPWM). Taking the carrier period to be Tc, the optimum delay in the semi-conductor gating pattern between the different blocks will be shown to be Tc/4 for the two H-bridges in the parallel configuration, and Tc/6 for the three H-bridges parallel configuration. That is to say, in the case of two parallel H-bridges the second inverter has its transistors gating signals lag (or lead) the other H-bridge by a time delay of Tc/4, and in the case of three H-bridges in parallel the second inverter has its transistors gating signals lag (or lead) those of the first inverter by Tc/6 while the third H-bridge lags (or leads respectively) the first by 2Tc/6. The optimum time delay in this context is the delay that yields minimum distortion figures as defined in Chapter 1.

The choice of the inter-module inductance L and load resistor R values (L = 100mH and R = 180Ω), in this thesis, are somewhat arbitrary; indeed due to the lack of specific application for our parallel operated inverters, those values have been chosen only so that our load gives a good range for our figures of merit (mainly THD) and be easy to implement in a laboratory experimental setup using bipolar technology transistors.

2.5.2 Parallel Inverters' Equivalent Circuit

Assuming that the batteries and the converter's switches in Fig. 2.12 are ideal, each inverter and its associated battery can be thought of as a voltage source whose voltage output is the unfiltered waveform seen directly across the bridge mid points of the two legs. This idealization is depicted in Fig. 2.13. Using Thevenin's theorem, ie, looking into the circuit as indicated by arrow A in Fig. 2.13 (b), we can arrive at the equivalent circuit of Fig. 2.13 (c).

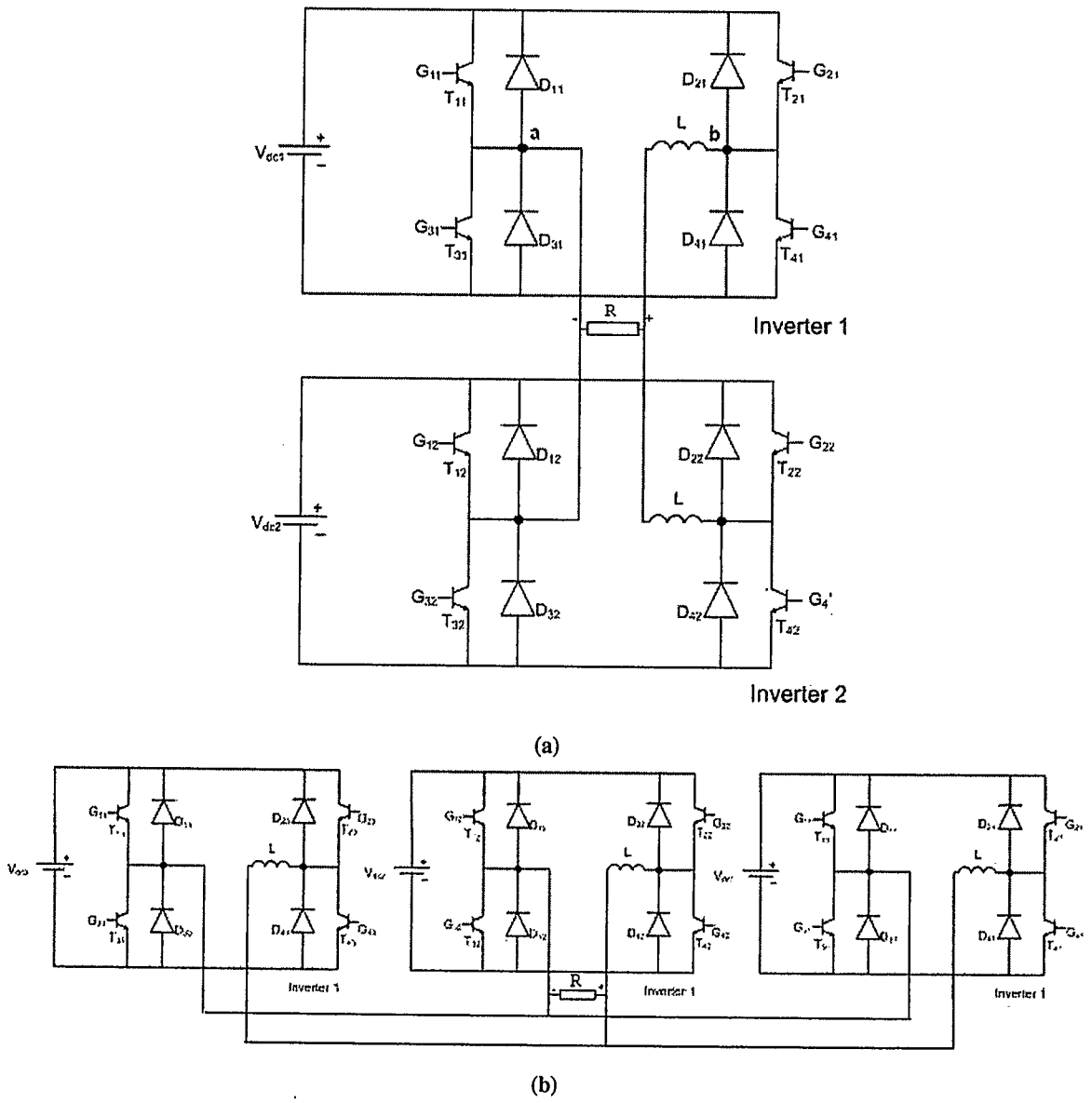


Fig. 2.12 Schematic diagrams of (a) two, (b) three H-bridge inverters in parallel

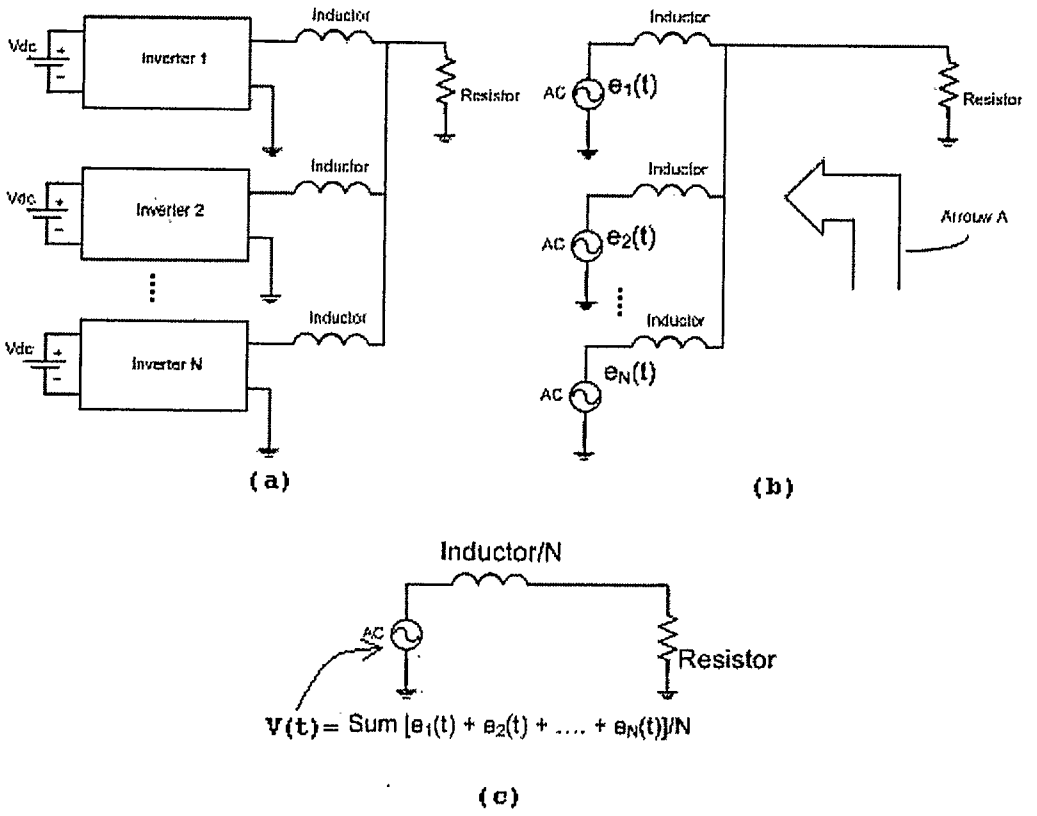


Fig. 2.13 (a) Parallel inverter configuration; (b) Equivalent circuit; (c) Simplified equivalent circuit

This simple approach is useful in understanding the operation of paralleling inverters. Indeed, now we can consider any number of inverters in parallel as equivalent to a single voltage source whose output voltage V(t) is given by the unfiltered voltage waveform:

$$V(t)=\frac{1}{N}\sum_{i=1}^{N}e_i(t) \tag{2.3}$$

where N is the number of inverters in parallel and $e_i(t)$ is the unfiltered output of the i^{th} inverter (this is the voltage between the inverter legs, ie, across the bridge output terminals V_{ab} as is clearly marked in the upper H-bridge in Fig. 2.12(a)). Note that we refer to V(t) in eqn. (2.3) as the effective resultant for the N parallel inverters since this voltage does not exist in the system, ie, there is no voltage waveform in the real parallel inverters system such as the one given by eqn. (2.3). Still, it is insightful to define the

effective resultant waveform as in eqn. (2.3) to simplify the understanding of paralleling techniques. In our MATLAB simulation, we will describe the operation of the parallel system using this simplified equivalent circuit of Fig. 2.13 (c) and eqn. (2.3).

2.5.3 Waveform Associated with Paralleling one, two and three Inverters

Figs. 2.14 to 2.16 show the waveforms associated with one, two and three inverters operating in parallel, respectively. The delays in the case of two and three inverters in parallel can be clearly seen in the effective resultant waveforms of Fig. 2.15 and Fig. 2.16.

Fig. 2.15 shows this unfiltered effective resultant for the case of two parallel inverters. Note that there are five voltage levels in the effective unfiltered load voltage waveform for each cycle of the fundamental (0V, 1/2Vdc, Vdc, -1/2Vdc, -Vdc) compared to three in the case of one inverter. In the case of three synchronized parallel inverters (see Fig. 2.16), the unfiltered effective resultant output voltage waveform will have seven voltage levels per cycle of the fundamental waveform (0V, 1/3Vdc, 2/3Vdc, Vdc, -1/3Vdc, -2/3Vdc, -Vdc), which is very similar to the multi-level operation referred to in Figs. 2.8(e) and 2.11(e) of the conventional multilevel inverter configurations. As more inverters are employed, the unfiltered effective resultant load voltage waveform becomes more sinusoidal-like with an effectively higher carrier frequency (ie, N fc) and with the number of levels equal 2N+1, where N is the number of parallel inverters and fc is the carrier frequency.

We can think of the inter-module inductors as working together to filter the effective resultant output voltage waveform V(t) given by eqn. (2.3). We will discuss this further in the following chapters.

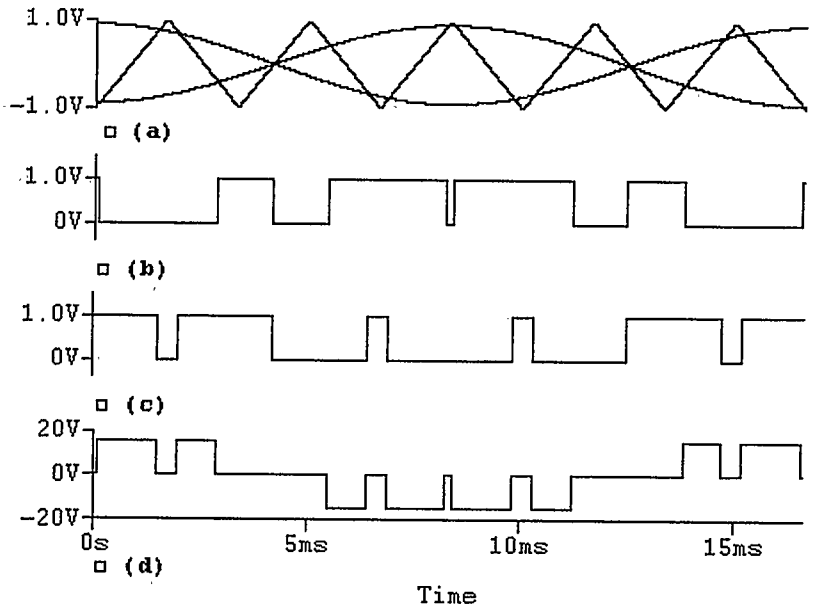


Fig. 2.14 Three-level NSPWM process for one single-phase inverter; (a) Identical carriers with inverted references; (b) Gating signals for T_{11}, its complementary will drive T_{31}; (c) Gating signals for T_{21}, its complementary will drive T_{41}; (d) Unfiltered voltage waveform at the output of one inverter with M = 0.9, fc/fs = 5 and Vdc = 15V.

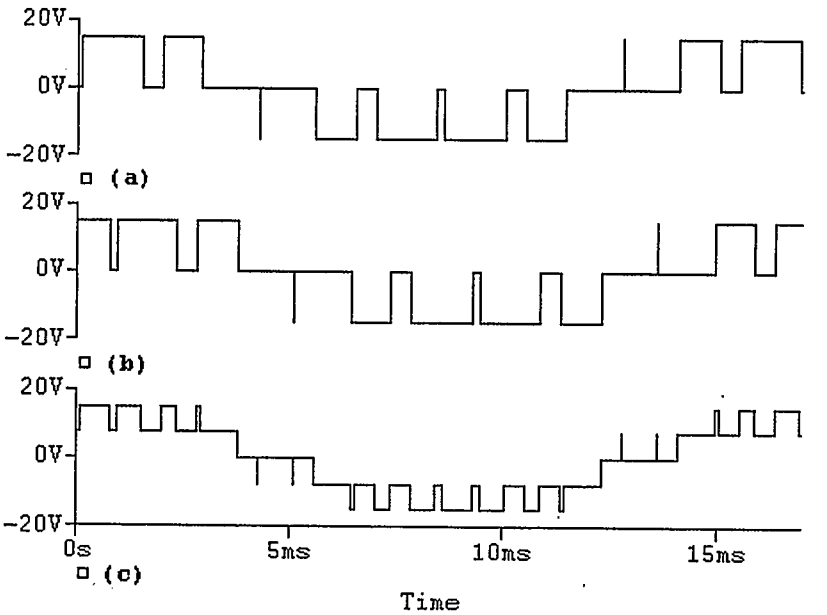


Fig. 2.15 Two parallel inverters operation: (a) Unfiltered effective voltage at the output of the first inverter; (b) Unfiltered effective voltage at the output of the second inverter; (c) The effective resultant output voltage waveform for two parallel inverters with M = 0.9, fc/fs = 5 and Vdc = 15V.

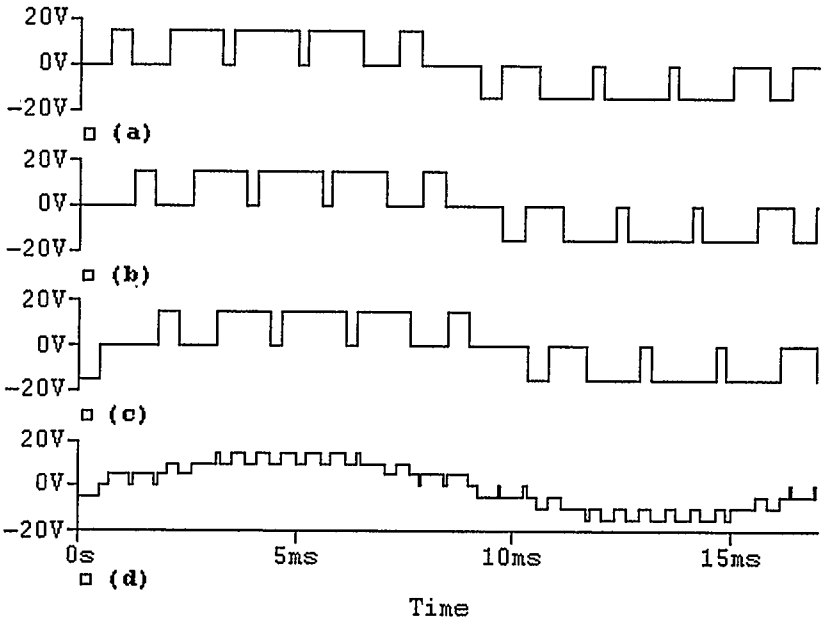


Fig. 2.16 Three parallel inverters operation (a) Unfiltered effective voltage at the output of the first inverter; (b) Unfiltered effective voltage at the output of the second inverter; (c) Unfiltered effective voltage at the output of the third inverter; (d) Effective resultant output voltage waveform for three parallel inverters with M = 0.9, fc/fs = 5 and Vdc = 15V.

2.6 Discussion

The operation of two or more inverters in parallel is possible in situations where two or more isolated dc sources are available (e.g. fuel cells, solar cells, some wind based sources, micro-turbine or other sources with a dc link) [30-34]. Parallel operation of multiple inverters has been identified as a means to reduce both relative and net harmonic distortion of an inverter system [13-15]. In more recent years, this idea has received renewed interest as alternative energy sources are being connected to electric utility grid systems [35, 38]. Many approaches employ an output reactor so that a voltage source inverter can be connected to the grid and at the same time provide current waveform control. Techniques have been suggested on how to minimize such reactors [15, 39]. Another group of researchers have suggested randomizing the operation of the power transistor gating functions so as to obtain uncorrelated harmonic spectra among the parallel inverters [36, 37]. It has also been pointed out that the need for communication

between the inverters control systems is not desirable [36]. A characterization of parallel inverter operation is given by H. Bierk in [40].

The parallel operation of inverters is useful for a number of reasons. If modularity and redundancy are advantageous for a given application, paralleling of inverters permits a scalable design implementation and reduced non-recurring engineering costs. One shortcoming is that many of these paralleling techniques depend on relatively large inter-tie inductors employed between inverter and the point of common coupling, to suppress the possible circulating currents and provide current control.

One group of researchers, A. M. Kamel *et al.* in [13], use a very similar phase shifting approach as discussed in this thesis, in conjunction with paralleling inverters as is show in Fig. 2.17.

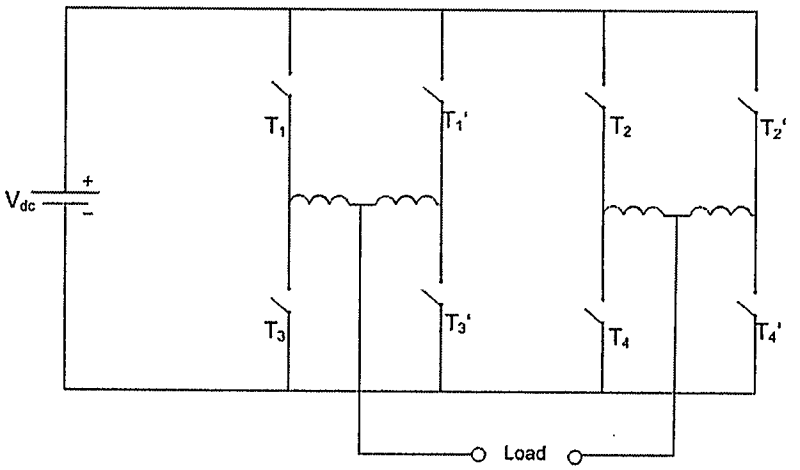


Fig. 2.17 Two full-bridge single-phase inverters in parallel, as in [13], with first H-bridge containing T_1 to T_4 and the second H-bridge containing T_1' to T_4'

A. M. Kamel *et al.* deal only with the case of two parallel inverters and the discussed technique uses two inductors as opposed to only one in our scheme per inverter. On the other hand, Kamel's scheme does not require isolated dc sources.

Regarding the optimum phase delay that yields the minimum voltage distortion factor, Kamel's paper suffered the unavailability of advanced computing resources at that time (1989), and in the opinion of the author the results were not precise.

Chapter Three: CARRIER BASED PWM

3.1 Introduction

The concept of carrier based pulse width modulation (PWM) is taken from electrical communication theory and refers to a high frequency signal, the carrier, which, in one of several possible ways, is compared to a modulating, or reference, signal. In power electronic inverter applications, a typical modulation scheme consists of a sine reference waveform and the modulation method is pulse width modulation where the on time (or off time) of one or more semi-conductor switching devices is proportional to the modulating sine reference waveform.

One of the characteristics of the carrier based PWM is that the switching frequency is constant, as opposed to hysteresis type PWM methods that have a time dependent switching period (c.f. Fig. 2.5 in Chapter 2). Carrier based PWM is also distinguished from Selective Harmonic Elimination (SHE) PWM, where all the switching instances are pre-calculated for the entire fundamental period so as to eliminate a set of low order harmonics. For SHE, no carrier information is needed, and as in the case of hysteresis, SHE PWM does not necessarily entail a constant switching period.

There are many variations of carrier based PWM proposed in the literature, which can be understood better by considering the following characteristics:

- Triangular vs. saw-tooth carrier waveform
- Uniform sampling vs. natural sampling
- Symmetric vs. asymmetric sampling

In general, it is now accepted that double-edge naturally sampled PWM and double-edge asymmetrically regular sample PWM give the best harmonic performance [41-43, 19 and 24].

In the following sections we perform in-depth harmonic analyses of these two techniques to evaluate the merits of each, and follow that with the application of these two techniques to parallel voltage source inverter (VSI) operation with current sharing inductors, for two and three inverters in parallel, as well as for a single inverter case

which serves as a reference case. We hope, by the end of this chapter, to be able to obtain some kind of conceptual framework with guidelines for selecting the best carrier based PWM technique applicable to the inverter design at hand.

3.2 Double-Edge Naturally Sampled PWM

3.2.1 Principles

Naturally sampled pulse width modulation with a triangular carrier is, by far the single most popular modulation in industrial applications, and hence is the most discussed in the literature [19]. Fig. 3.1 illustrates the principle of this technique applied to a single-phase full-bridge VSI. In this modulation strategy both phase legs use a triangular common carrier and are modulated with sinusoidal reference waveforms that are 180° out of phase, defined as,

$$V_{ref} = MV_{dc}\cos(\omega_s t) \tag{3.1}$$

and

$$V_{ref'} = -MV_{dc}\cos(\omega_s t) \tag{3.2}$$

where M is the modulation index defined as the ratio of the reference amplitude to the carrier amplitude, with 0<M<1 (M great than unity is referred to as over-modulation and is rarely used), and ω_s is the angular frequency of the modulating reference signal.

For double-edge naturally sampled PWM, an inverter leg midpoint (point a or b in Fig. 3.1) is connected through a semi-conductor switch to the positive dc terminal (sometimes called the positive dc rail) when the reference is greater than the triangular carrier wave, and connected to the negative dc terminal (or rail) when the carrier is greater than the reference, as can be seen in Fig. 3.2.

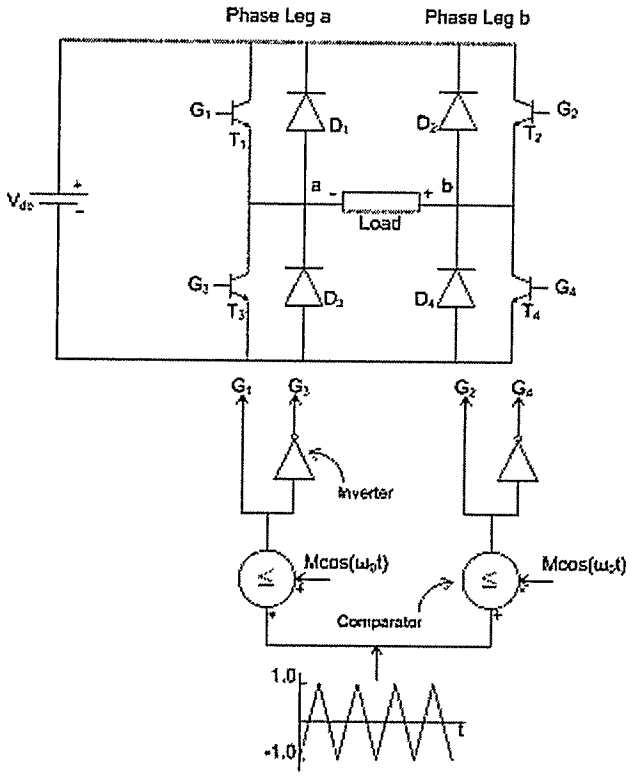


Fig. 3.1 NSPWM generation principle applied to a single-phase full-bridge voltage source inverter

Fig. 3.3 illustrates the double-edge naturally sampled switching process, showing the inverter unfiltered output voltage waveform (ie, between the inverter legs midpoints) at the bottom of the figure, for the single-phase full-bridge inverter with the particular operating conditions of a modulating index M = 0.9 and carrier ratio fc/fs = 21. In this figure, it can be seen clearly how both phase legs use a common carrier but they are modulated with inverted sine reference waveforms. Figs. 3.3 (a) and (c) show the carrier and reference waveforms while Figs. 3.3 (b) and (d) show T_1 and T_2 gating signals, T_3 and T_4 gating signals being the complementary (ie, the binary logic inverse) of T_1 and T_2 gating signals are not shown.

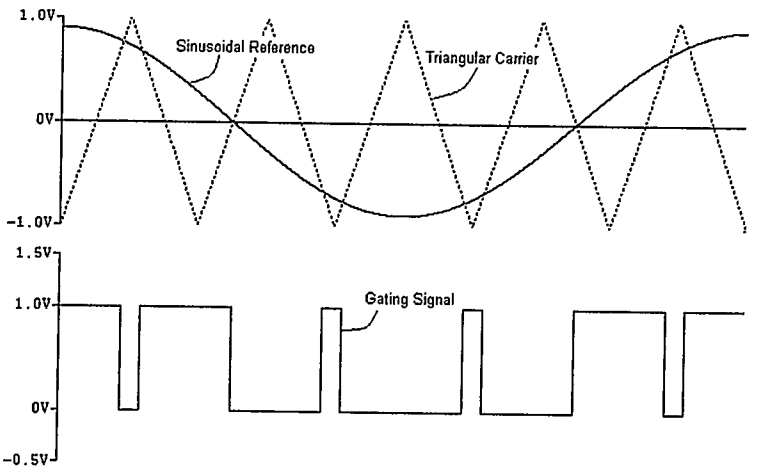


Fig. 3.2 Illustration of the NSPWM principle

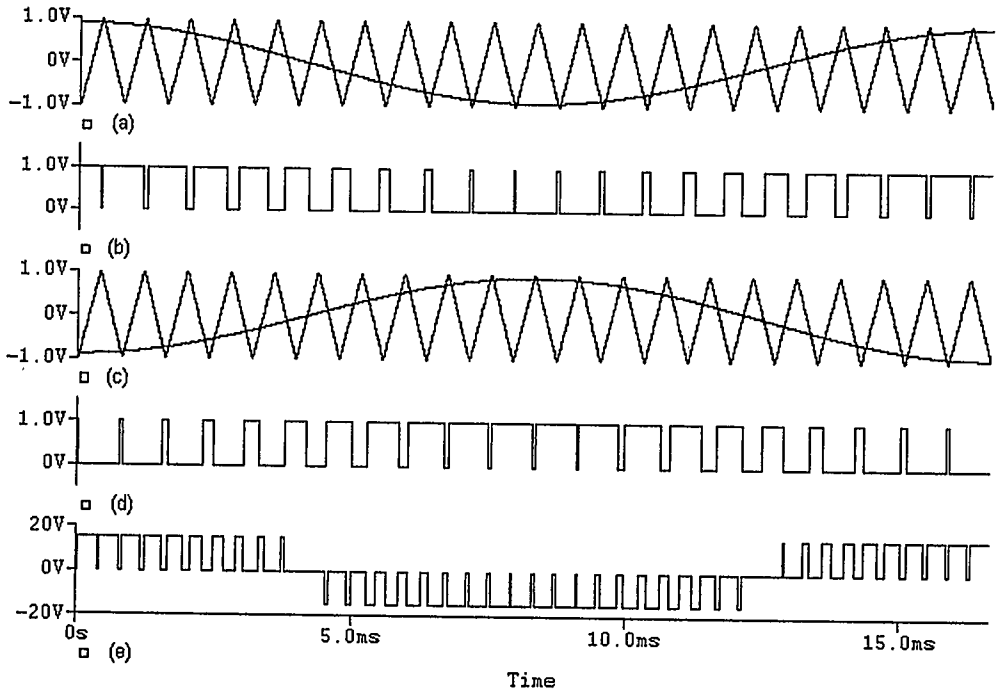


Fig. 3.3 Double-edge NSPWM process for one single-phase inverter, M = 0.9, fc/fs = 21 (a) and (c) triangular carrier and sine references waveforms; (b) T1 gating; (d) T2 gating; (e) Unfiltered voltage waveform at the output of the inverter (V_{ab})

3.2.2 Double-Edge NSPWM Spectrum Analysis

The most well-known analytical method for determining the Fourier expansion of a PWM signal is known as Bennett's technique. It was originally developed by W. R. Bennett [44] and Black [45] for communication systems, and later adapted to modulated converter systems by Bowes and Bird [46]. A much more thorough treatment of the carrier based modulation techniques is given in [6, 47]. A brief description of this method is given in Appendix A; only the final result is given here.

The Fourier description of a double edge carrier, naturally sampled PWM waveform is given by (a re-derivation of results in [6] is provided in Appendix A):

$$V_{ab}(t) = V_{dc} M \cos(\omega_s t) + \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2n-1}(m\pi M) \cos([m+n-1]\pi) \times \cos(2m\omega_c t + [2n-1]\omega_s t) \quad (3.3)$$

where M is the modulation index, ω_c is the carrier angular frequency, ω_s is the reference angular frequency and $J_n(\xi)$ denotes Bessel functions [6].

Fig. 3.4 uses the above formula to present the voltage spectrum for the unfiltered (ie, between point a and b in Fig. 3.1) output of a double-edge NSPWM modulated single-phase inverter for the particular operating conditions of a modulating index M = 0.9 and carrier to sine reference frequency ratio fc/fs = 21. This plot shows the fundamental low-frequency components produced by this modulation process, and the groups of odd sideband harmonics arranged around the even multiples of the carrier frequency; no odd carrier multiples and their associated sidebands are present. All the harmonics in this plot have magnitudes which have been normalized with respect to V_{dc} to allow comparison to be made with the plots in the next section dealing with asymmetrical regularly sampled PWM.

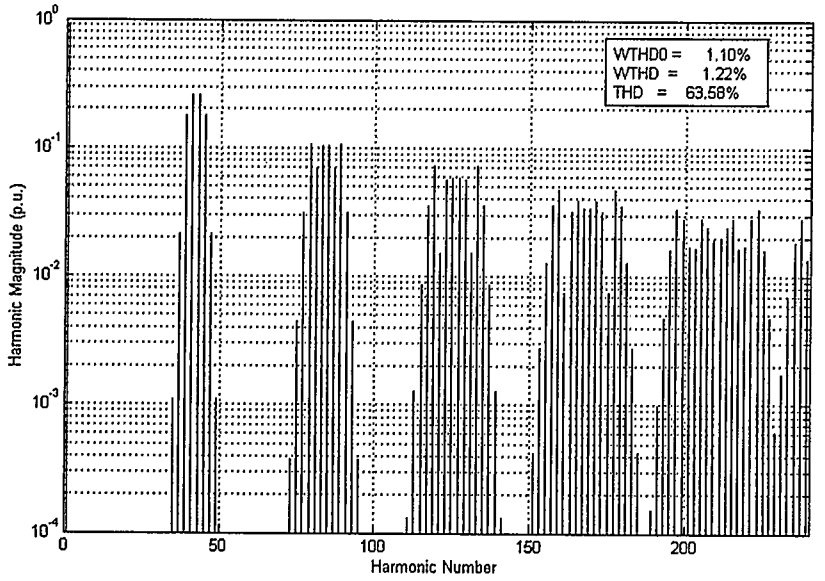


Fig. 3.4 Theoretical harmonics spectrum for the full-bridge single-phase inverter's unfiltered output voltage modulated with double edge NSPWM, M = 0.9, fc/fs = 21

3.2.3 Extension of NSPWM to Parallel Inverter Operation

Using eqn. (3.3) in conjunction with the parallel inverter equivalent circuit described in section 2.5.2, the unfiltered output voltage (taken between the mid points of the H-bridge legs) for N parallel inverters will have the following Fourier series:

$$V_{ab}(t)=\sum_{i=1}^{N}V_{dc}\frac{M}{N}\cos(\omega_s(t-\Delta_i)) + \frac{4V_{dc}}{\pi N}\sum_{i=1}^{N}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos([m+n-1]\pi) \times\cos(2m\omega_c(t-\Delta_i)+[2n-1]\omega_s(t-\Delta_i)) \quad (3.4)$$

Using the principle of superposition the filtered output voltage, taken across the load resistor's terminals, for N parallel inverters will have the following Fourier series:

$$V(t)=\frac{R}{\sqrt{R^2+(\frac{L}{N}\omega_s)^2}}\sum_{i=1}^{N}V_{dc}\frac{M}{N}\cos(\omega_s(t-\Delta_i)-\varphi_f)$$
$$+\frac{4V_{dc}}{\pi N}\sum_{i=1}^{N}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{R}{\sqrt{R^2+(\frac{L}{N}(2mP+[2n-1])\omega_s)^2}} \qquad (3.5)$$
$$\times\frac{1}{2m}J_{2n-1}(m\pi M)\cos([m+n-1]\pi)$$
$$\times\cos(2m\omega_c(t-\Delta_i)+[2n-1]\omega_s(t-\Delta_i)-\varphi_{mn})$$

where

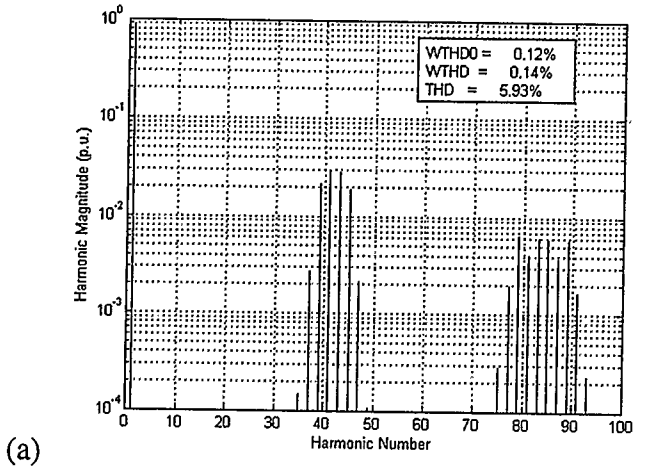
$$\tan(\varphi_f)=\frac{\frac{L}{N}\omega_s}{R} \qquad (3.6)$$

and

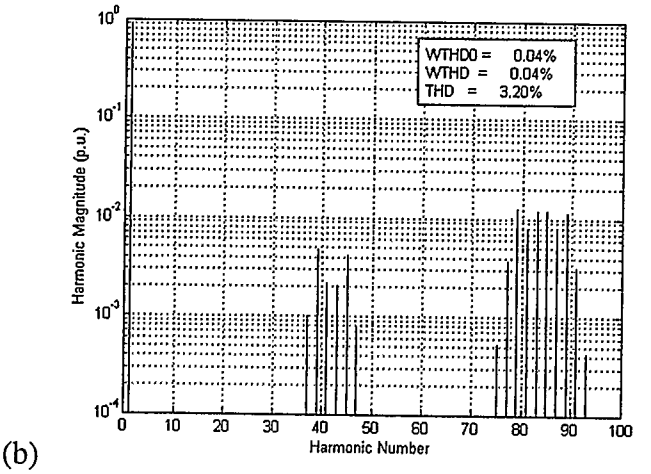
$$\tan(\varphi_{mn})=\frac{\frac{L}{N}(2mP+[2n-1])\omega_s}{R} \qquad (3.7)$$

with N being the number of parallel inverters, P = fc/fs is the carrier to reference frequency ratio, and Δ_i is the time shift of the i^{th} inverter with Δ_1 taken to be zero.

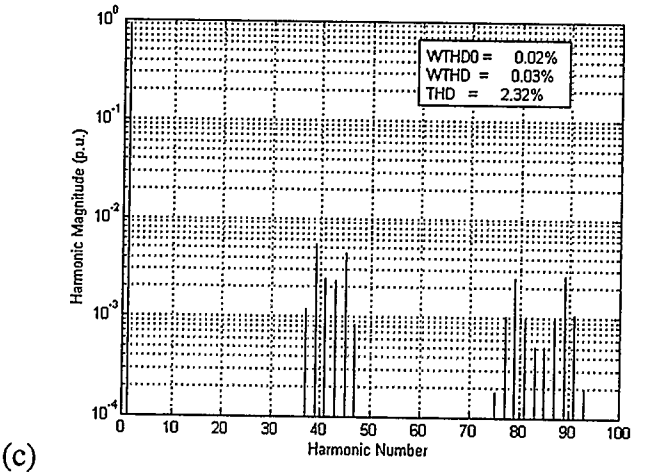
Using eqn. (3.5), we show in Fig. 3.5 the spectra of the filtered output voltages, for one, two and three inverters in parallel with M = 0.9, fc/fs = 21, R = 180Ω, and L = 100mH . For the cases of two or three inverters in parallel, the optimum phase delays have been employed (described below in section 3.4), for which the transistor gating pattern for successive inverters is delayed by Tc/(2N), where Tc is the carrier period and N is the number of parallel inverters. In the case of two inverters in parallel, one of the inverters will have its transistor gating signals shifted by Tc/4 relative to the other (N = 2 in this case), and in the case of three inverters in parallel, the second inverter will have its transistor gating patterns time shifted by Tc/6 relative to the first inverter (N = 3 in this case) while the third will have a time shift double that, ie, 2*Tc/6 equal to Tc/3. The corresponding figures of merit are summarized in Table 3.1.



(a)



(b)



(c)

Fig. 3.5 Harmonic spectra for the filtered output of (a) one single-phase inverter; (b) two inverters in parallel; (c) three inverters in parallel. The output is modulated by double edge NSPWM, M = 0.9, fc/fs = 21, R = 180Ω, and L = 100mH

3.3 Triangular Asymmetrical Regular Sampled PWM

3.3.1 Principles

A difficulty with naturally sampled PWM is its realization as a digital embedded system. This is because the carrier is compared to the reference sinusoid (see Fig. 3.2) resulting in the requirement of solving a transcendental set of equations. One of the solutions, popularly adopted to overcome this problem is a PWM implementation using regularly sampled pulse width modulation (RSPWM), where the reference sine waveform is discrete-time sampled and then compared to the carrier waveform to establish the gating signal, as illustrated in Figs. 3.6 and 3.7.

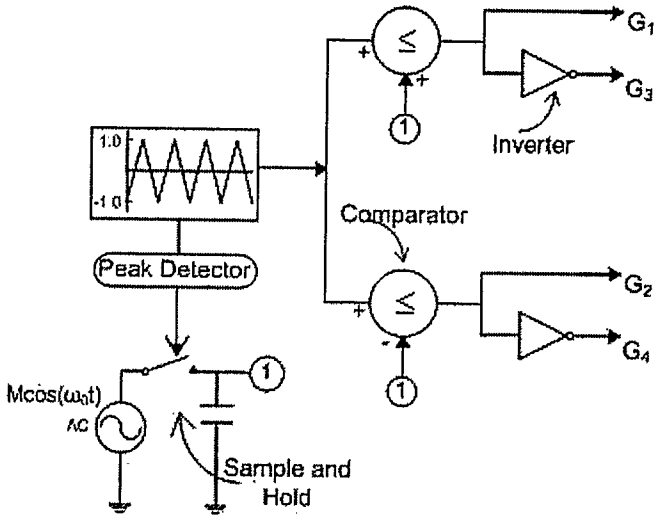


Fig. 3.6 RSPWM generation principle applied to a single-phase full-bridge voltage source inverter

For double-edge asymmetrical regularly sampled PWM, the reference is sampled every half period of the carrier at both the positive and the negative carrier peak, as can be seen in Fig. 3.7.

Table 3.1 Summary of the three figures of merit associated with Fig. 3.5

	One Converter	Two Converters	Three Converters
WTHD0	0.12075%	0.03645%	0.02463%
WTHD	0.13708%	0.04075%	0.02746%
THD	5.92652%	3.20428%	2.31559%

Here we note that the reference is being phase advanced by one quarter the carrier period to compensate for the phase delay produced by the sampling process. We illustrate the double edge asymmetrical regularly sampled PWM approach in Fig. 3.8.

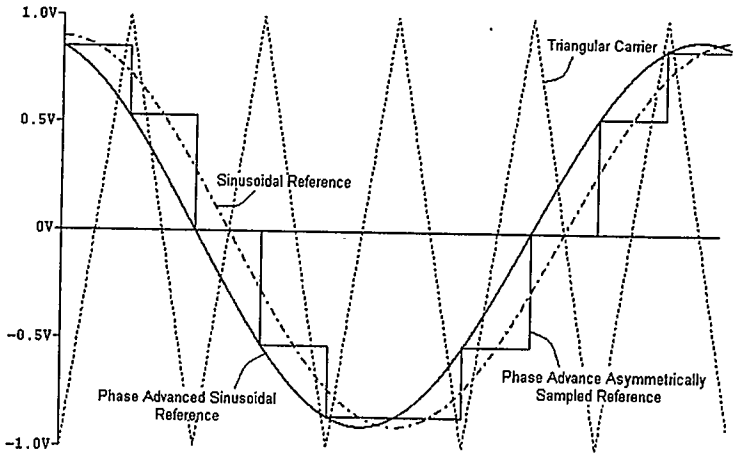


Fig. 3.7 Illustration of the Asymmetrical RSPWM principle

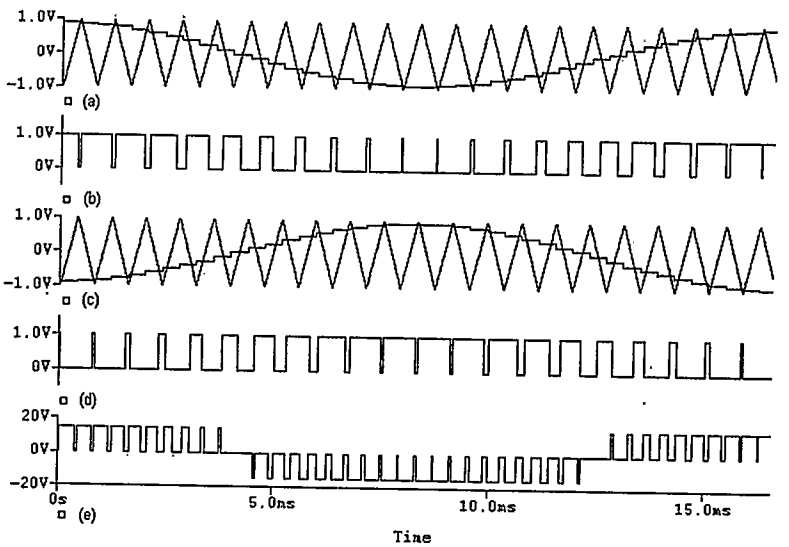


Fig. 3.8 Double-edge asymmetrical RSPWM process for one single-phase inverter, M = 0.9, fc/fs = 21 (a) and (c) triangular carrier and sine references waveforms; (b) T1 gating signal; (d) T2 gating; (e) Unfiltered voltage waveform at the output of the inverter (V_{ab})

3.3.2 Double-Edge RSPWM Spectrum Analysis

The Fourier description of a double edge carrier, asymmetrical regularly sampled PWM waveform is given by (see Appendix A),

$$V_{ab}(t)=\frac{4V_{dc}}{\pi}\sum_{n=1}^{\infty}\frac{1}{\left[n\frac{\omega_s}{\omega_c}\right]}J_n\left(n\frac{\omega_s}{\omega_c}\frac{\pi}{2}M\right)\sin\left(n\frac{\pi}{2}\right)\cos(n\omega_s t)$$

$$+\frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{\left[2m+[2n-1]\frac{\omega_s}{\omega_c}\right]}J_{2n-1}\left(\left[2m+[2n-1]\frac{\omega_s}{\omega_c}\right]\frac{\pi}{2}M\right)\cos([m+n-1]\pi) \quad (3.8)$$

$$\times\cos(2m\omega_c t+[2n-1]\omega_s t)$$

where M is the modulation index, ω_c is the carrier angular frequency, ω_s is the reference angular frequency and $J_n(\xi)$ denotes Bessel functions [6]..

Using eqn. (3.8), Fig. 3.9 presents the voltage spectrum for the unfiltered output of a double-edge asymmetrical RSPWM modulated single-phase inverter for the particular operating conditions of a modulating index M = 0.9 and carrier ratio fc/fs = 21. This plot shows the fundamental low-frequency component produced by this modulation process, and the groups of odd sideband harmonics arranged around the even multiples of the carrier frequency; no odd carrier multiples and their associated sidebands are present. All the harmonics in this plot have magnitudes which have been normalized with respect to V_{dc} to allow comparison to be made with the Fig. 3.4 in the previous section dealing with naturally sampled PWM.

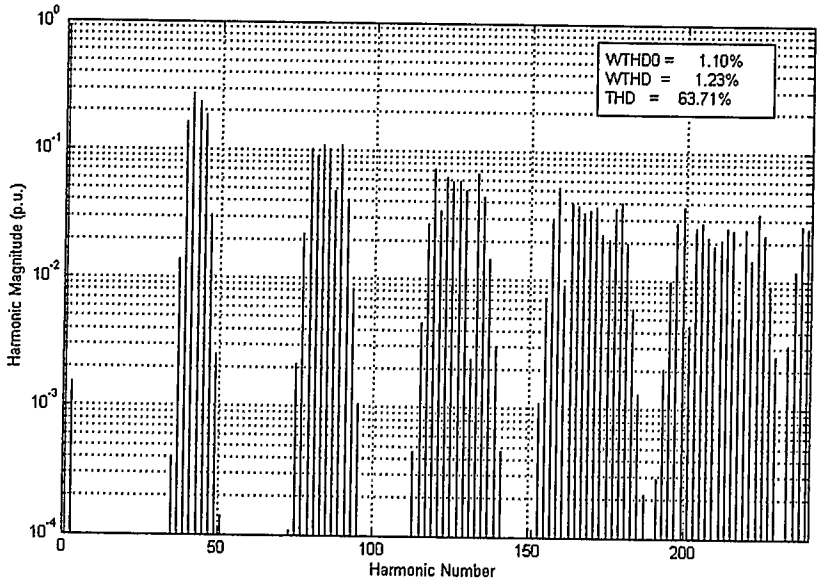


Fig. 3.9 Theoretical harmonics spectrum for the full-bridge single-phase inverter's unfiltered output voltage modulated with double edge asymmetrical RSPWM, M = 0.9, fc/fs = 21

3.3.3 Extension of RSPWM to Parallel Inverter Operation

Using eqn. (3.8) in conjunction with parallel inverter equivalent circuit described in section 2.5.2, the unfiltered output voltage for N parallel operated inverters will have the following Fourier series:

$$V(t)=\frac{4V_{dc}}{\pi}\sum_{i=1}^{N}\sum_{n=1}^{\infty}\frac{1}{\left[n\frac{\omega_s}{\omega_c}\right]}J_n\left(n\frac{\omega_s}{\omega_c}\frac{\pi}{2}M\right)\sin\left(n\frac{\pi}{2}\right)\cos(n\omega_s(t-\Delta_i))$$
$$+\frac{4V_{dc}}{\pi}\sum_{i=1}^{N}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{\left[2m+[2n-1]\frac{\omega_s}{\omega_c}\right]} \tag{3.9}$$
$$\times J_{2n-1}\left(\left[2m+[2n-1]\frac{\omega_s}{\omega_c}\right]\frac{\pi}{2}M\right)\cos([m+n-1]\pi)$$
$$\times\cos(2m\omega_c(t-\Delta_i)+[2n-1]\omega_s(t-\Delta_i))$$

Using the principle of superposition the filtered output voltage, taken across the load resistor's terminals, for N parallel inverters will have the following Fourier series:

$$V(t)=\frac{4V_{dc}}{\pi}\sum_{i=1}^{N}\sum_{n=1}^{\infty}\frac{R}{\sqrt{R^2+(\frac{L}{N}n\omega_s)^2}}\frac{1}{\left[n\frac{\omega_s}{\omega_c}\right]}J_n(n\frac{\omega_s}{\omega_c}\frac{\pi}{2}M)\sin(n\frac{\pi}{2})\cos(n\omega_s(t-\Delta_i)-\varphi_n)$$
$$+\frac{4V_{dc}}{\pi}\sum_{i=1}^{N}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{R}{\sqrt{R^2+(\frac{L}{N}(2mP+[2n-1])\omega_s)^2}} \qquad (3.10)$$
$$\times\frac{1}{\left[2m+[2n-1]\frac{\omega_s}{\omega_c}\right]}J_{2n-1}\left(\left[2m+[2n-1]\frac{\omega_s}{\omega_c}\right]\frac{\pi}{2}M\right)\cos([m+n-1]\pi)$$
$$\times\cos(2m\omega_c(t-\Delta_i)+[2n-1]\omega_s(t-\Delta_i)-\varphi_{mn})$$

with

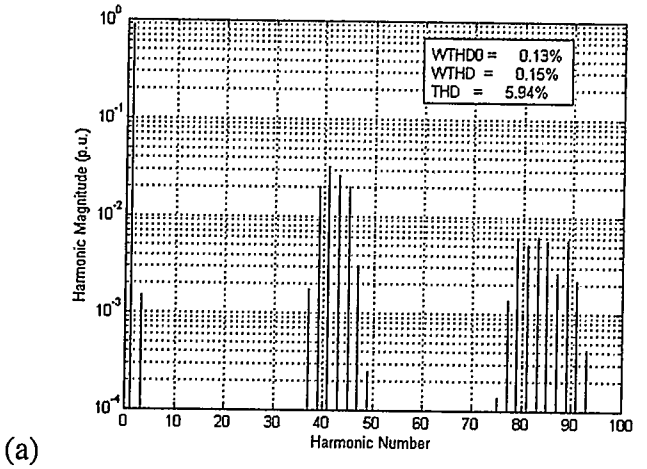
$$tg(\varphi_n)=\frac{\frac{L}{N}n\omega_s}{R} \qquad (3.11)$$

and

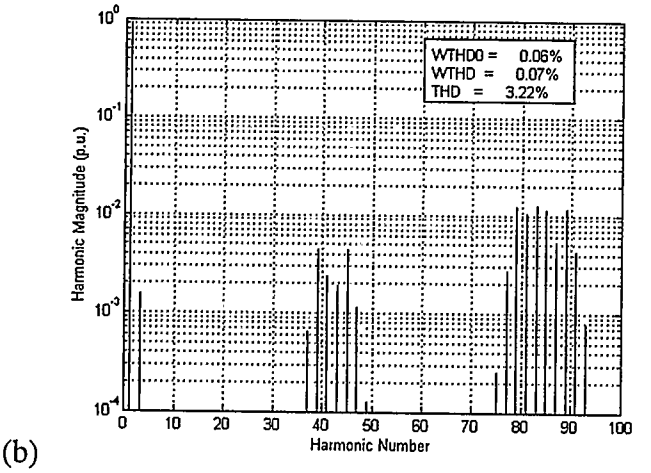
$$tg(\varphi_{mn})=\frac{\frac{L}{N}(2mP+[2n-1])\omega_s}{R} \qquad (3.12)$$

with N being the number of parallel inverters, P = fc/fs is the carrier to sine frequency ratio, and Δ_i is the time shift of the i^{th} inverter with Δ_1 taken to be zero.

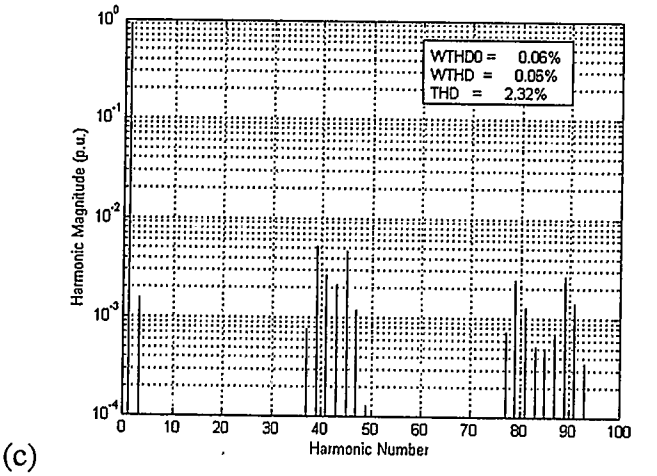
Using eqn. (3.10), Figs. 3.10 gives the spectra of the filtered output voltages for one, two and three inverters in parallel operated at the optimum phase delays of Tc/(2N) (as will be discussed in the next section). To reiterate, for two parallel inverters, a delay of Tc/4 is used, while successive inverters have a delay of Tc/6 for three parallel inverters. The corresponding figures of merit are summarized in Table 3.2.



(a)



(b)



(c)

Fig. 3.10 Harmonic spectra for the filtered output of (a) one single-phase inverter; (b) two inverters in parallel; (c) three inverters in parallel. The output is modulated by double edge asymmetrical RSPWM, M = 0.9, fc/fs = 21, R = 180Ω, and L = 100mH

Once again, in all the above graphs, all harmonics are normalized with respect to Vdc; this is to make comparison meaningful.

3.4 Optimum Phase Delay

In this thesis we examine the synchronized phase shifted operation of two and three inverters operated in parallel [13, 40]. Each inverter has its switches gated with the same set of pulses as the first inverter but delayed by some time shift (c.f. Fig. 2.14 to 2.16). A major contribution of this thesis is finding the optimum phase shift between parallel inverters that yields minimum harmonic distortion factors (namely, WTHD0, WTHD and THD as defined in Chapter 1).

Shown in Fig. 3.11 is the behavior of the fundamental voltage component and the first 50 harmonics as a function of the time delay in the second inverter, for two parallel operated inverters with the particular operating conditions of a modulating index M = 0.9 and carrier to sine frequency ratio fc/fs = 21 and for an operating load of R = 180Ω and L = 100mH using double-edge NSPWM. Fig. 3.12 shows similar fundamental and harmonics plots but for double-edge asymmetrical RSPWM.

It is clear from those two figures that harmonic amplitudes tend to become very small at a certain time delay defined by t = 0.1984ms, for the case depicted, we can therefore expect that the lowest total harmonic distortion (THD) is achieved at that point (as found in [13]). The time delay t = 0.1984ms happens to be equal to Tc/4, where Tc is the carrier period, this result will be established more rigorously and validated by simulation results in the next chapter where we will find that indeed the optimum time phase delay occurs exactly at

Table 3.2 Summary of the three figures of merit associated with Fig. 3.10

	One Converter	Two Converters	Three Converters
WTHD0	0.13061%	0.06229%	0.05623%
WTHD	0.14836%	0.06968%	0.06271%
THD	5.93828%	3.21739%	2.32317%

Tc/2N, for the case of two and three inverters in parallel, with N being the number of inverters in parallel.

Figs. 3.13 and 3.14, for double-edge NSPWM and double-edge asymmetrical RSPWM respectively, examine this reduced harmonic distortion phenomenon further by showing that indeed, all our three figures of merit namely WTHD0, WTHD and THD have a minimum occurring at exactly Tc/4 for the case of two parallel inverters and for the particular operating conditions of a modulating index M = 0.9 and carrier to sine frequency ratio fc/fs = 21, with an operating load of R = 180Ω and L = 100mH.

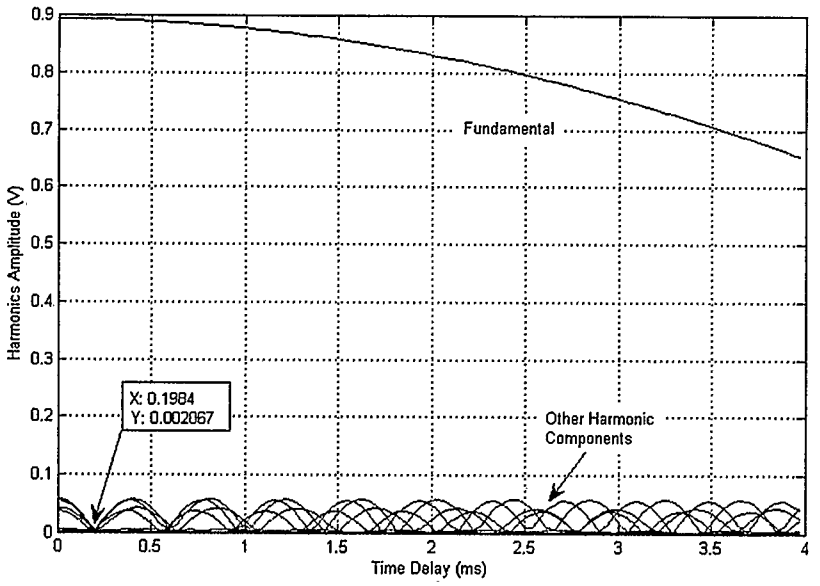


Fig. 3.11 Fundamental and harmonic components amplitude versus time delay for two inverter configuration with fc/fs = 21, M = 0.9 and a load of R = 180Ω and L = 100mH, modulated using NSPWM

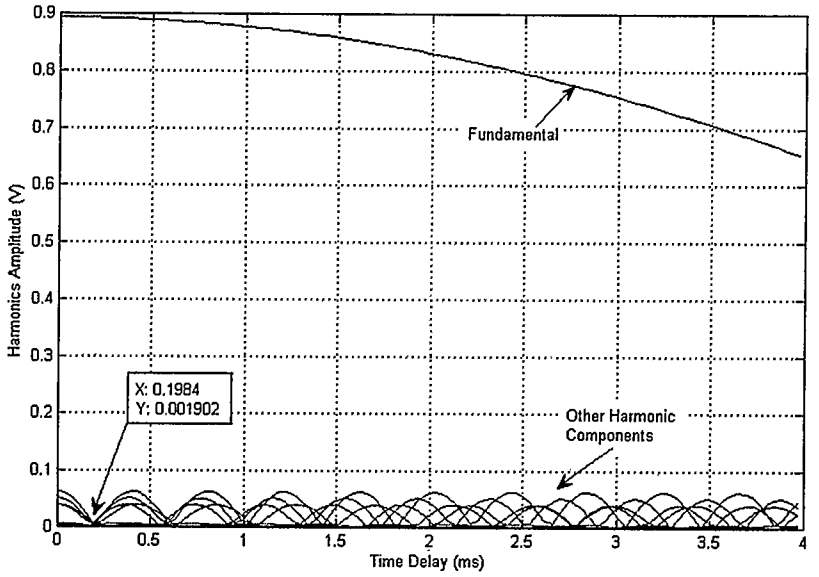
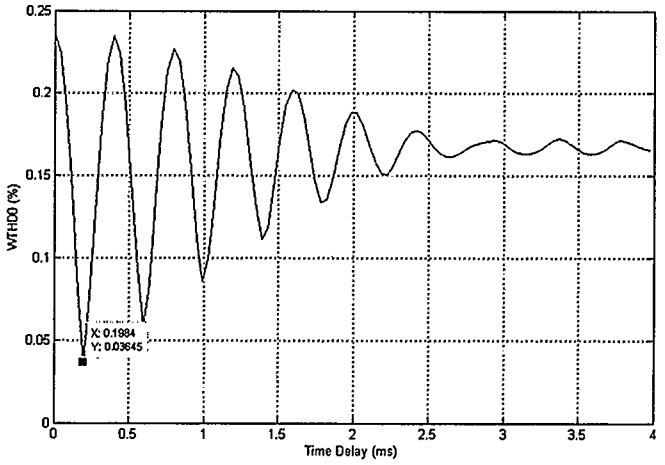


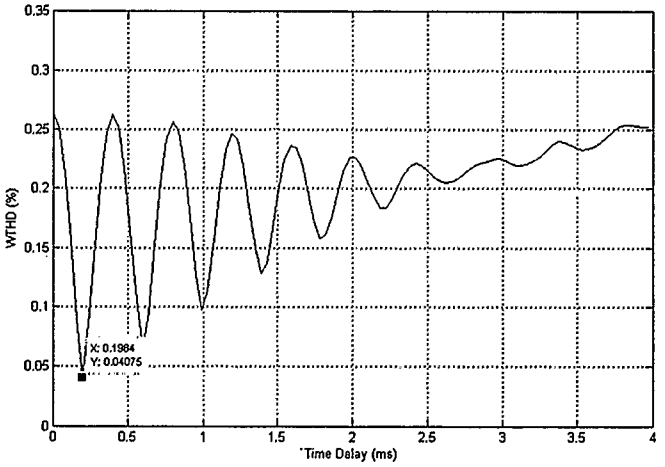
Fig. 3.12 Fundamental and harmonic components amplitude versus time delay for two inverter configuration with fc/fs = 21, M = 0.9 and a load of R = 180Ω and L = 100mH, modulated using RSPWM

3.5 Discussion of Modulation Strategies

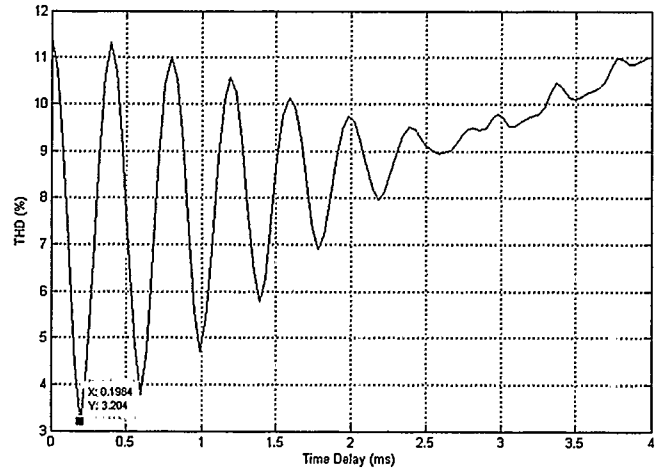
Fig. 3.15 contrasts the variation of WTHD0, WTHD and THD as a function of modulation index M, for the case of two parallel inverters, for two modulation strategies (double-edge NSPWM and asymmetrical RSPWM). Fig. 3.16 indicates a similar contrast but for the case of three parallel inverters. These figures show that WTHD0 is practically zero for M very small; this is understandable if we note that in eqn. (3.3) and eqn. (3.8) the harmonics have some form of $J_n(kM)$ as a factor in their amplitude and we know that as $x \to 0, J_0(x) \to 1$, and $J_{n\neq 0}(x) \to 0$ as can be seen from the Bessel function plots in Fig. 3.17.



(a)

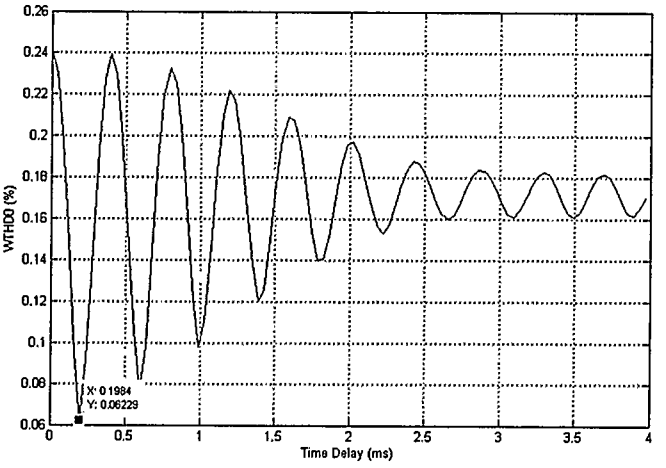


(b)

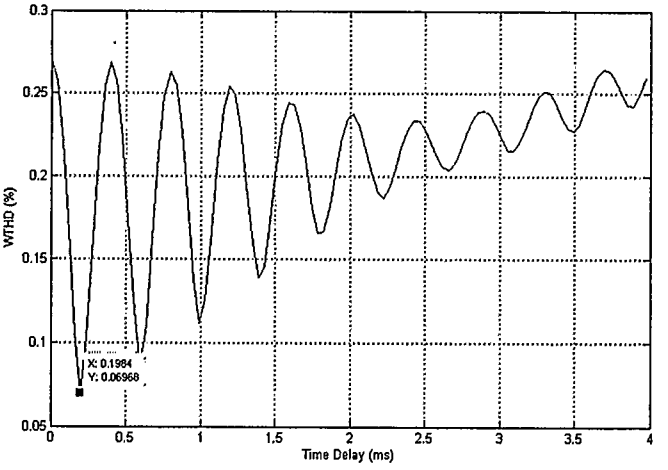


(c)

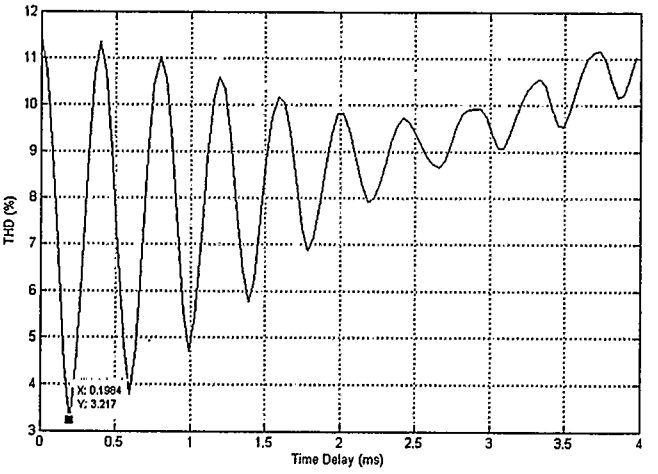
Fig. 3.13 (a) WTHD0, (b) WTHD and (c) THD versus time delay for fc/fs = 21 and M = 0.9 and a load of R = 180Ω and L = 100mH using NSPWM



(a)

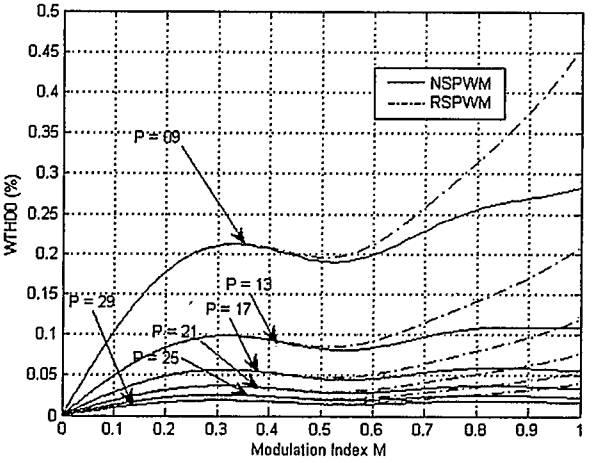


(b)

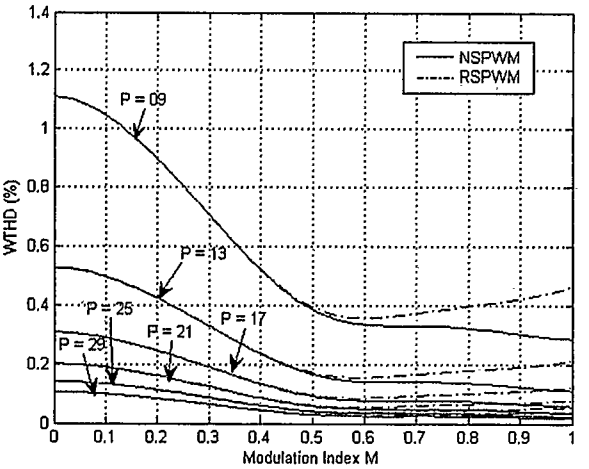


(c)

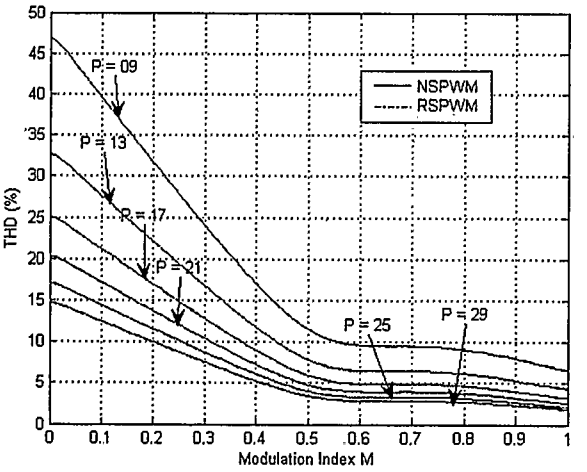
Fig. 3.14 (a) WTHD0, (b) WTHD and (c) THD versus time delay for fc/fs = 21 and M = 0.9 and a load of R = 180Ω and L = 100mH using RSPWM.



(a)

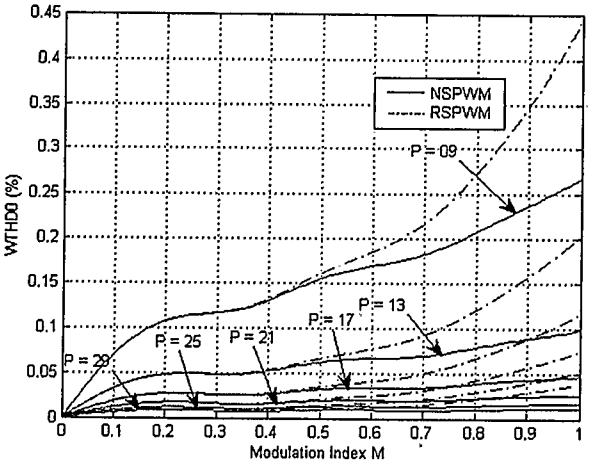


(b)

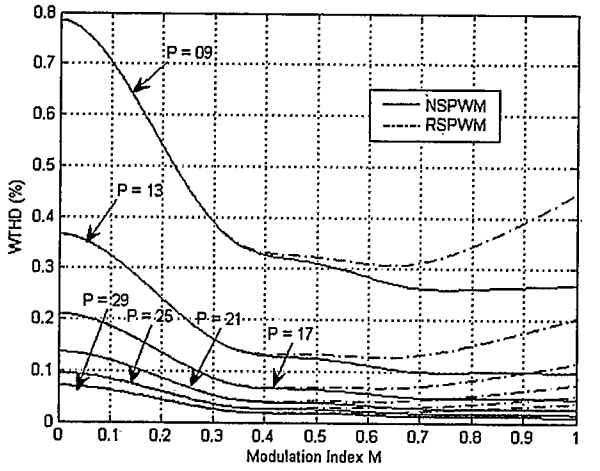


(c)

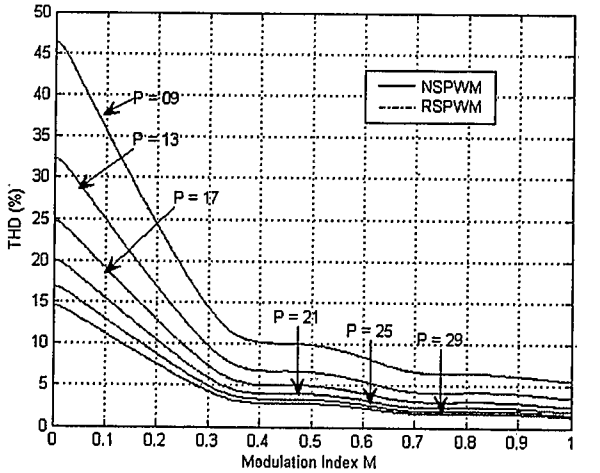
Fig. 3.15 WTHD0, WTHD and THD variation as a function of modulation index M for the case of two inverters operated in parallel



(a)



(b)



(c)

Fig. 3.16 WTHD0, WTHD and THD variation as a function of modulation index M for the case of three inverters operated in parallel

Because as M increases the fundamental increases (see for example eqn. 3.3), Figs. 3.15 (a) and 3.16 (a) will yields Fig. 3.15 (b) and 3.16 (b) giving the variation of WTHD as a function of M also we can see that as P = fc/fs increases WTHD0 and WTHD decrease. This is expected as the increase of P will push the harmonics higher, as can be seen in Fig, 3.5 and 3.10, and both WTHD0 and WTHD use the order of each harmonic component as its weighting factor.

Figs. 3.15 (c) and 3.16 (c) show THD variation as a function of modulation index M for different value of the carrier to sine frequency ratio (fc/fs = 9, 13, 17, 21, 25, and 29) for both modulation strategies (NSPWM and RSPWM). The invariance in THD with respect to the modulation used (indicated in Fig. 3.15 (c) and 3.16 (c) by the total overlapping of the two plots), indicates that the same quantity of total harmonics exist independent of the modulation strategy used. Examining Figs. 3.15 and 3.16 (a and b), we see that for the case of two and three inverters in parallel and for a modulation index above approximately 4.5, the WTHD0 and WTHD are always considerably higher in the case of double edge asymmetrical RSPWM as compared to double edge NSPWM. More on this are presented in section 3.7.

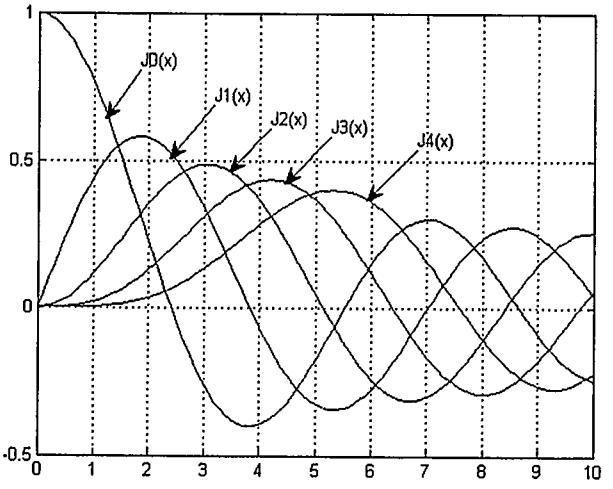


Fig. 3.17 The first five Bessel functions of the first kind $J_0(x)$, $J_1(x)$... $J_4(x)$ plotted as a function of x. Note that as $x \rightarrow 0$, $J_n(x) \rightarrow 1$ for $n = 0$ and $J_n(x) \rightarrow 0$ for $n \neq 0$.

3.6 Summary of Distortion Figures of Merit

We conclude this chapter with the results summarized in Tables 3.3 and 3.4 which are derived using eqns. (3.5) and (3.10). This data will be needed to evaluate our simulation and experimental results in the following two chapters.

Table 3.3 Theoretical figures of merit for the output filtered voltage for one, two and three inverters in parallel modulated with NSPWM for various values of modulation indices and frequency ratios with R = 180Ω and L = 100mH

		Double-edge NSPWM		
		One Inverter	Two Inverters	Three Inverters
P=11, M=0.3	WTHD0	0.3754%	0.1384%	0.0718%
	WTHD	1.2784%	0.4650%	0.2405%
	THD	29.5091%	19.7679%	11.6521%
P=11, M=0.6	WTHD0	0.5231%	0.1239%	0.1014%
	WTHD	0.8907%	0.2082%	0.1700%
	THD	19.7944%	7.7675%	6.6746%
P=11, M=0.9	WTHD0	0.4446%	0.1640%	0.1386%
	WTHD	0.5047%	0.1837%	0.1548%
	THD	11.2146%	6.3665%	4.9841%
P=21, M=0.3	WTHD0	0.1040%	0.0368%	0.0158%
	WTHD	0.3540%	0.1234%	0.0530%
	THD	15.6611%	10.3885%	5.9335%
P=21, M=0.6	WTHD0	0.1446%	0.0290%	0.0199%
	WTHD	0.2462%	0.0486%	0.0333%
	THD	10.5094%	3.9552%	3.2663%
P=21, M=0.9	WTHD0	0.1208%	0.0365%	0.0246%
	WTHD	0.1371%	0.0408%	0.0275%
	THD	5.9265%	3.2042%	2.3153%
P=31, M=0.3	WTHD0	0.0478%	0.0168%	0.0067%
	WTHD	0.1628%	0.0562%	0.0224%
	THD	10.6379%	7.0401%	3.9844%
P=31, M=0.6	WTHD0	0.0664%	0.0127%	0.0079%
	WTHD	0.1131%	0.0213%	0.0133%
	THD	7.1389%	2.6584%	2.1642%
P=31, M=0.9	WTHD0	0.0553%	0.0158%	0.0092%
	WTHD	0.0628%	0.0176%	0.0103%
	THD	4.0213%	2.1460%	1.5048%

3.7 Discussion and Chapter Summary

Observing Figs. 3.5 and 3.10, one sees how complex the resultant spectrum can be for phase shifted inverters operated in parallel. Indeed, by looking at the improvements in the figures of merit resulting from parallel inverter operation (see Tables 3.1 and 3.2), one may expect that more inverters operated in parallel will produce a spectrum with more attenuated harmonic components. This is not the case. In fact paralleling may lead to some harmonics being amplified, as is the case, for example, in Fig 3.10 (b) of sideband harmonics around the harmonic number 84 (where 84

Table 3.4 Theoretical figures of merit for the output filtered voltage for one, two and three inverters in parallel modulated with RSPWM for various values of modulation indices and frequency ratios with R = 180Ω and L = 100mH

		Doube-edge Asymmetrical RSPWM		
		One Inverter	Two Inverters	Three Inverters
P=11, M=0.3	WTHD0	0.3760%	0.1387%	0.0721%
	WTHD	1.2809%	0.4663%	0.2417%
	THD	29.5375%	19.7884%	11.6609%
P=11, M=0.6	WTHD0	0.5286%	0.1341%	0.1141%
	WTHD	0.9009%	0.2255%	0.1913%
	THD	19.8779%	7.7361%	6.7005%
P=11, M=0.9	WTHD0	0.4794%	0.2431%	0.2252%
	WTHD	0.5453%	0.2729%	0.2521%
	THD	11.2963%	6.4391%	5.0148%
P=21, M=0.3	WTHD0	0.1040%	0.0369%	0.0160%
	WTHD	0.3543%	0.1236%	0.0533%
	THD	15.6654%	10.3915%	5.9346%
P=21, M=0.6	WTHD0	0.1455%	0.0326%	0.0249%
	WTHD	0.2479%	0.0546%	0.0417%
	THD	10.5218%	3.9503%	3.2709%
P=21, M=0.9	WTHD0	0.1306%	0.0623%	0.0562%
	WTHD	0.1484%	0.0697%	0.0627%
	THD	5.9383%	3.2174%	2.3232%
P=31, M=0.3	WTHD0	0.0478%	0.0168%	0.0068%
	WTHD	0.1628%	0.0563%	0.0226%
	THD	10.6392%	7.0411%	3.9848%
P=31, M=0.6	WTHD0	0.0668%	0.0144%	0.0105%
	WTHD	0.1138%	0.0242%	0.0176%
	THD	7.1428%	2.6569%	2.1658%
P=31, M=0.9	WTHD0	0.0598%	0.0281%	0.0250%
	WTHD	0.0680%	0.0314%	0.0279%
	THD	4.0250%	2.1504%	1.5079%

correspond to four times the carrier to sine frequency ratio of 21). This is a major divergence from the traditional harmonic reduction schemes such as Selective Harmonic Minimization (SHM) [20].

For parallel operation of phase shifted inverters, WTHD0, WTHD and THD figures of merit provide a useful tool to look inside the complex system of phase shifted parallel inverters. Indeed examining again Tables 3.1 and 3.2 and Figs. 3.15 and 3.16, we see that for the case of two and three inverters in parallel and for a modulation index M above approximately 4.5, the WTHD0 and WTHD are always considerably higher in the case of double edge asymmetrical RSPWM as compared to double edge NSPWM. This tells us that, all in all, for double edge asymmetrical RSPWM modulation the low order harmonics are more significant than for double edge NSPWM, and thus are more difficult to filter out. At the same time, the total harmonic distortion is basically the same irrespective of the modulation strategy being used and this tells us that the weight gained by the low harmonics in double edge asymmetrical RSPWM correspond to the weight gained by the high frequency harmonics in double edge NSPWM.

Clearly then, double edge NSPWM is, in general, superior to double edge asymmetrical RSPWM but this superiority is application dependent and should be considered against the ease of implementing double edge asymmetrical RSPWM in a digital system. This result is indeed expected as RSPWM, in a sense, is an approximation of NSPWM that is more suited for digital system implementation (for example, using microcontrollers).

Chapter Four: SIMULATION RESULTS

4.1 Introduction

The simulations carried out in this thesis were completed using PSpice[2] version 9.2 and MATLAB / Simulink[3] version 7.1 running on a host PC with a 2GHz AMD Athlon 64x2 Dual Core Processor 3800+, 2 GB of RAM and hard drive of 300GB.

PSpice is an electric circuit simulation package originally developed at the University of California, Berkley as SPICE (**S**imulation **P**rogram for **I**ntegrated **C**ircuits **E**mphasis) [49]. SPICE was later modified by MicroSim (later bought by OrCAD and now part of Cadence Design Systems) to run on personal computers and became PSpice.

MATLAB is a high-level language and interactive environment that permits engineers to perform complex mathematic computations in a more efficient manner (both programming and execution) compared to programming languages such as C, and Fortran. Simulink, on the other hand, is a multi application simulation environment permitting model-based simulations with prepared macros, subroutines (often transparent to the user) and a customizable set of libraries[4], much of which is implemented with MATLAB code. Simulink permits one to design and simulate and test a wide variety of systems, including many aspects of communications, controls, signal processing, video processing, and image processing.

The use of both of the above two simulation platforms helped the author to eliminate any coding errors that traditionally slip in programs and this is by comparing the results outcome of each. Indeed, and due to the fact that PSpice and MATLAB uses totally different approaches in tackling the simulation task, bugs in the software become almost impossible This allowed us to be confident that the programs written were relatively bug free, and thus gave us confidence in the reliability of the results obtained in

---

[2] Cadence Design Systems, Inc. (http://www.cadence.com/)
[3] The MathWorks, Inc. (http://www.mathworks.com/)
[4] SimPowerSystems Libraries (the power electronics toolbox) were not used in our simulation because, in the opinion of the author, as it is now it has quite limited capabilities.

this thesis. Also by using these two tools we have the advantage of being able to choose the most convenient of them to attempt to solve the design at hand and then use the other software package as a verifying tool [47, 48].

PSpice is found, in the author's opinion, to be the most suitable tool for power inverter design and any electronics design for that matter. Still, there were some issues with PSpice that held us back from relying solely on it in performing simulation tasks. Some issues with PSpice we found are:

- The famous convergence problem.
- Very limited Transient output file options. For example limiting the Fourier analysis number of harmonics in the output file to 100 is not acceptable, and not having appropriate facilities in the software to help in the manipulation of the harmonic components complicates even further the problem.
- Very limited capability for saving the output of a simulation.

An upgrade to the latest version ORCAD 15.7 did not solve those problems. I used MATLAB to overcome all these obstacles.

4.2 Optimum Phase Delay

In the context of parallel inverter operation, the optimum phase delays are those delays that yield the minimum distortion factors (defined in Chapter 1). In this thesis, in order to find this optimum phase-shift a phase-shift delay sweep has been carried out in simulation, involving two and three parallel inverters. Fig. 4.1 shows the THD obtained when the second inverter is operated with a phase-shift delay swept from 0 to Ts (where Ts = 1/60 s = 16.67 ms is the modulating sine wave reference period) relative to the first inverter, for a two parallel inverter configuration with double-edge naturally sampled PWM (NSPWM). As can be seen in the inset of Fig. 4.1, the optimum phase-shift delay that yields the lowest total harmonic distortion is found to be Tc/4 equal to 0.1984ms in this case, where Tc is the triangular carrier period (ie, the second inverter has its power switching transistors receive an identical set of gating functions as the first inverter but with a delay of Tc/4). Also clearly seen on that figure is how a zero phase-shift delay produces a THD of 11.50% while the optimal phase-shift delay Tc/4 = 0.1984ms yields a

THD value of 3.208% for the set of operating parameters (modulation index M=0.9, and carrier to sine reference frequency ratio fc/fs = 21) and reactor (L = 100mH) and load (R = 180Ω) parameters.

Fig. 4.2 shows the THD obtained when the second and third inverters have their phase-shift delays swept simultaneously between 0 and Ts in a three parallel inverter configuration modulated by double-edge NSPWM. The optimum phase-shift that yields the lowest total harmonic distortion in this case is found to be Tc/6 equal to 0.1323ms (ie, the second inverter has gating functions that lag the first inverter one by Tc/6, and third inverter gating functions lag the first one by 2*(Tc/6)).

Fig 4.3 and Fig. 4.4 show the same sweep but with double-edge asymmetrical RSPWM. The optimum phase delays are exactly the same as in the case of the double-edge NSPWM.

Fig 4.5 and Fig.4.6 show the WTHD0 and WTHD factors respectively, obtained for the case of the three parallel inverter configuration modulated by double-edge NSPWM. Fig 4.7 and Fig.4.8 show the WTHD0 and WTHD factors respectively, obtained for the case of the three parallel inverter configuration modulated by double-edge asymmetrical RSPWM. The sweep here is limited to Tc/2 for convenience. The same optimum phase-shift delays are obtained here too.

The symmetries in the plots just discussed can be readily understood from the geometrical paralleling of the inverters, and the large peak distortion values in Figs. 4.1 to 4.4 (greater than 100% THD), are the direct result of a 60Hz fundamental that is approaching zero amplitude.

It is important to note that those optimum phase delays have been calculated in our MATLAB simulations with a numerical output precision of format "long e" (16 decimal digits), and in both cases of two and three inverters operated in parallel, we found the optimal delay to be exactly Tc/2N, where N is the number of inverters in parallel (N = 2 or 3) for both modulation strategies.

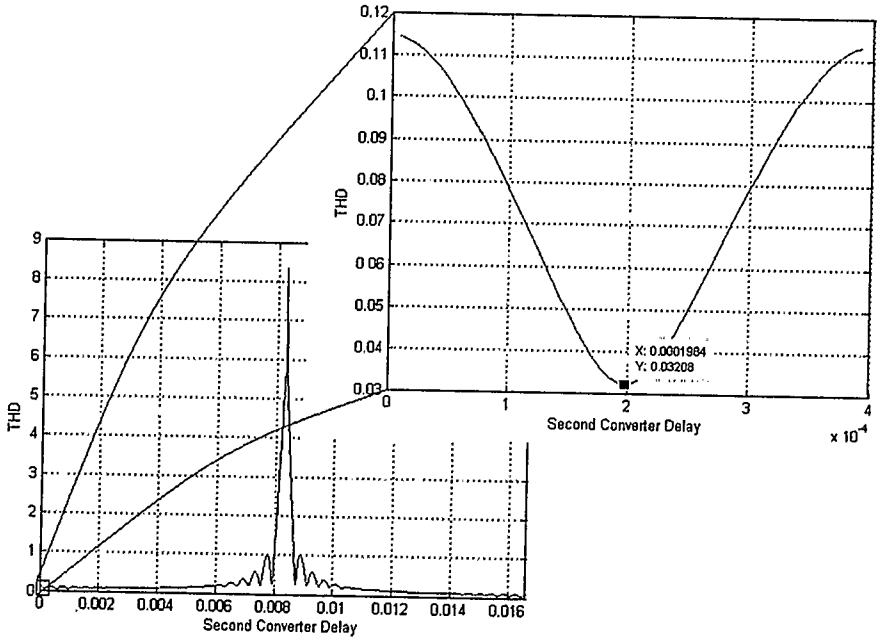


Fig. 4.1 THD as a function of time-shift delay for two parallel inverters with NSPWM, M = 0.9 and fc/fs = 21

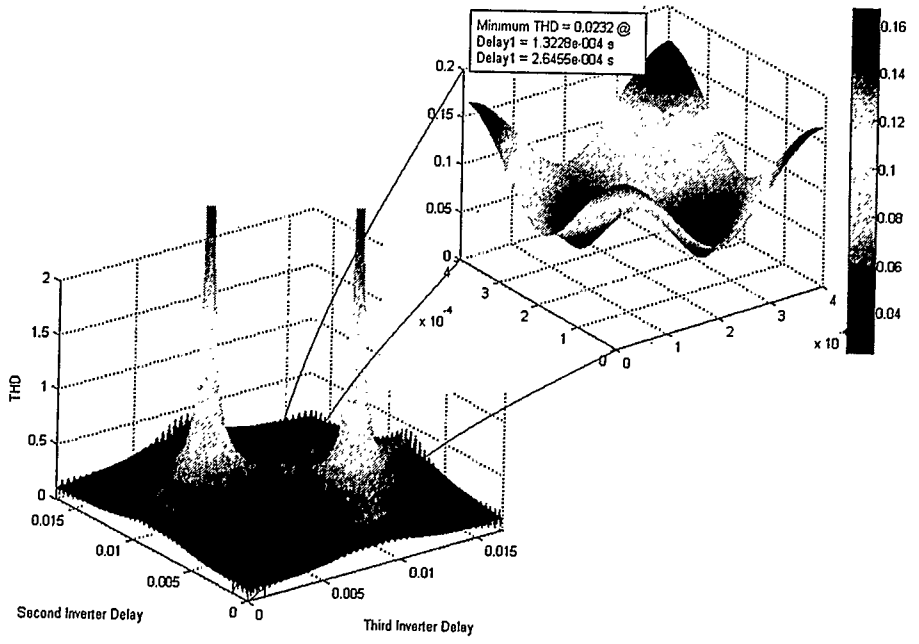


Fig. 4.2 THD as a function of time-shift delay for three parallel inverters with NSPWM, M = 0.9 and fc/fs = 21

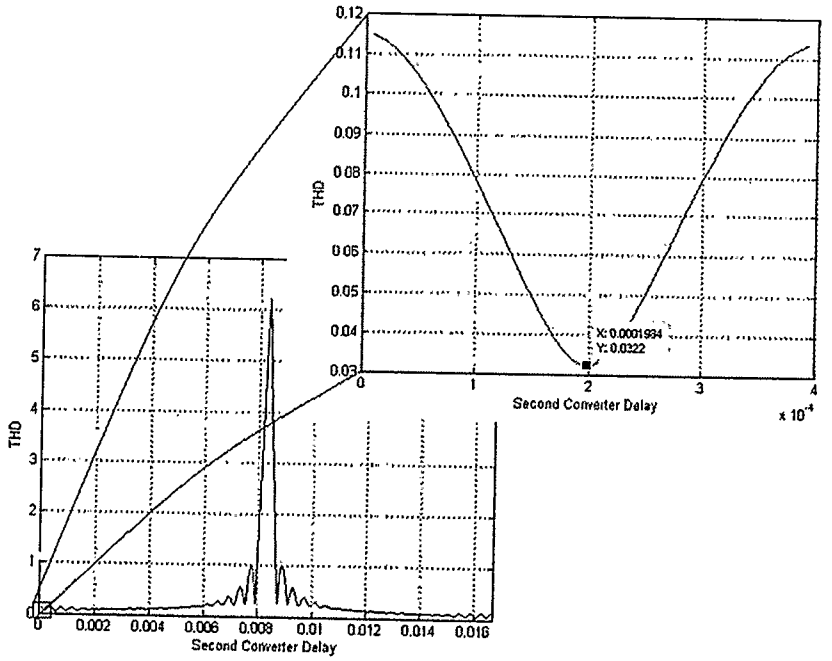


Fig. 4.3 THD as a function of phase-shift delay for two parallel inverters with RSPWM, M = 0.9 and fc/fs = 21

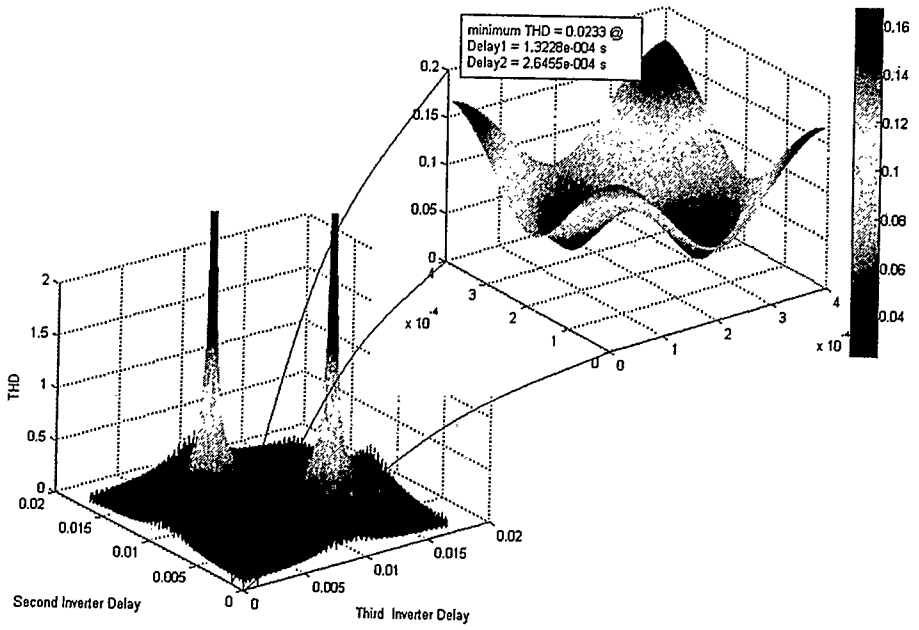


Fig. 4.4 THD as a function of phase-shift delay for three parallel inverters with RSPWM, M = 0.9 and fc/fs = 21

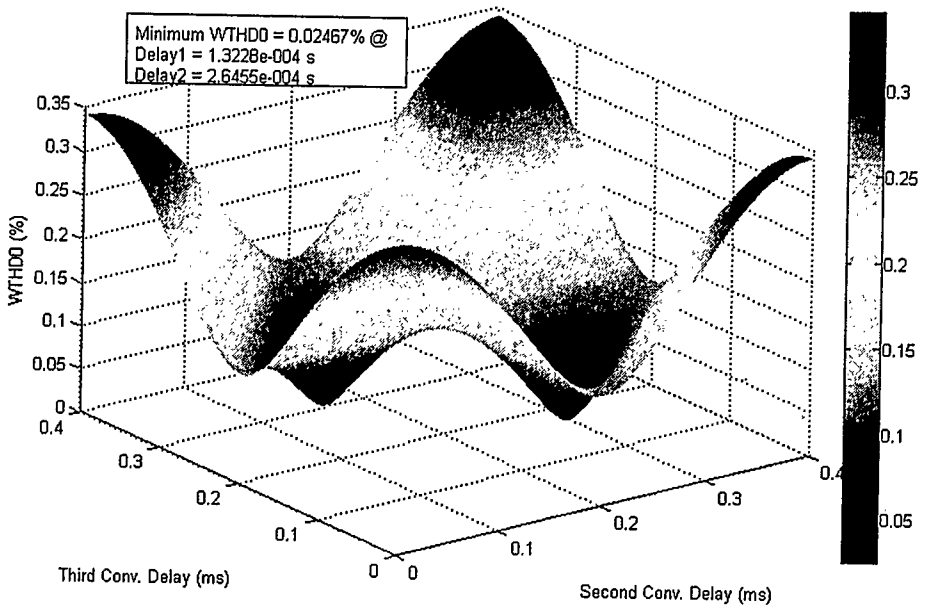


Fig. 4.5 WTHD0 as a function of phase-shift delay for three parallel inverters with NSPWM, M = 0.9 and fc/fs = 21

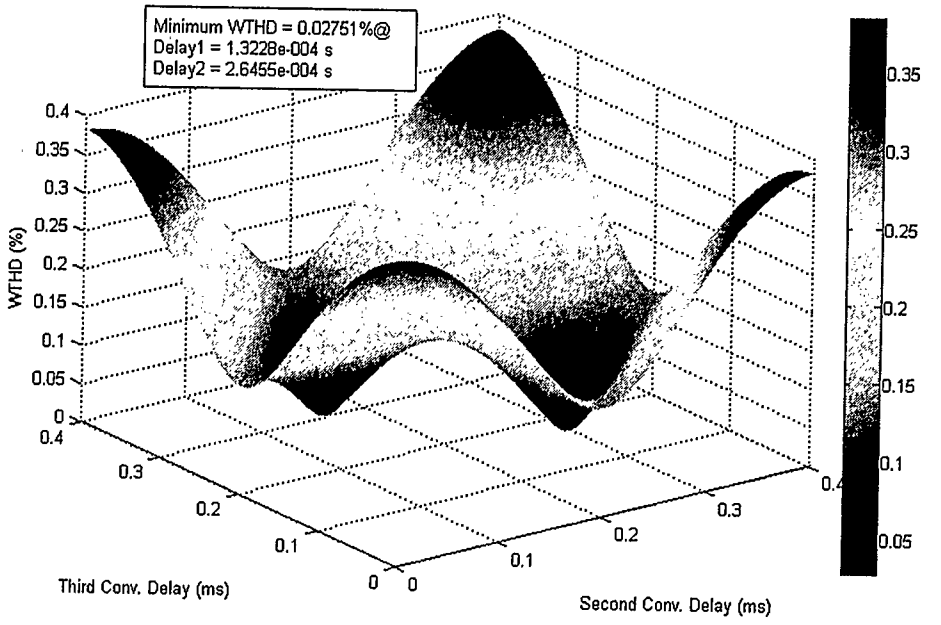


Fig. 4.6 WTHD as a function of phase-shift delay for three parallel inverters with NSPWM, M = 0.9 and fc/fs = 21

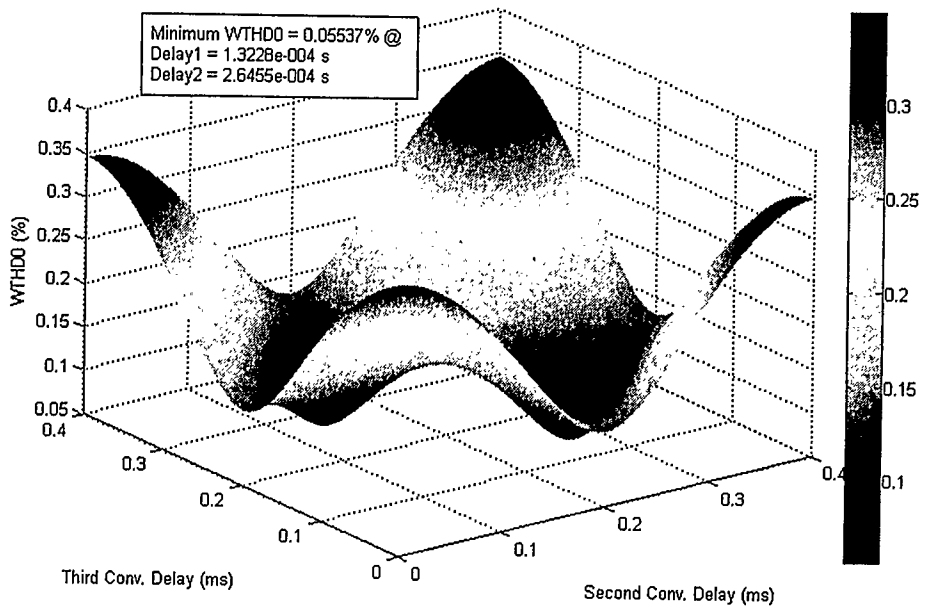


Fig. 4.7 WTHD0 as a function of phase-shift delay for three parallel inverters with RSPWM, M = 0.9 and fc/fs = 21

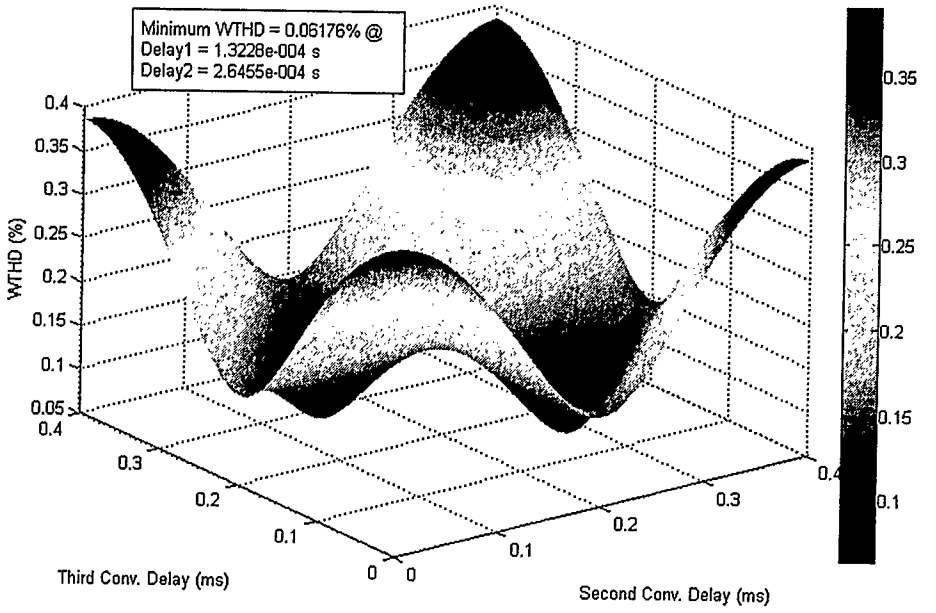


Fig. 4.8 WTHD as a function of phase-shift delay for three parallel inverters with RSPWM, M = 0.9 and fc/fs = 21

4.3 Sample Simulation Results

4.3.1 Double-edge NSPWM

Figs. 4.9 through 4.17 show samples of computer simulation results. In those figures the output voltage waveforms and their harmonic spectra for one, two and three synchronized optimally phase-shifted parallel inverters with various value of modulation index M and carrier to reference frequency ratio fc/fs, for a particular combination of load and inter-module reactor of R = 180Ω and L = 100mH, are plotted, all modulated by the double-edge NSPWM. The output voltages shown here are taken between the leads of the load resistor. Table 4.1 gives the associated figures of merit (namely WTHD0, WTHD and THD) for every plot in those figures.

Table 4.1 Figures of merit associated with Figs 4.9 through 4.17

		One Inverter		Two Inverters		Three Inverters	
		MATLAB	PSpice	MATLAB	PSpice	MATLAB	PSpice
P = 11, M = 0.3	WTHD0	0.3754%	0.3751%	0.1384%	0.1381%	0.0718%	0.0718%
	WTHD	1.2784%	1.2776%	0.4650%	0.4667%	0.2406%	0.2415%
	THD	29.5091%	29.5057%	19.7684%	19.8391%	11.6536%	11.7183%
P = 11, M = 0.6	WTHD0	0.5231%	0.5229%	0.1239%	0.1237%	0.1014%	0.1015%
	WTHD	0.8907%	0.8905%	0.2081%	0.2089%	0.1700%	0.1708%
	THD	19.7944%	19.7930%	7.7672%	7.7964%	6.6755%	6.7790%
P = 11, M = 0.9	WTHD0	0.4446%	0.4447%	0.1640%	0.1637%	0.1386%	0.1391%
	WTHD	0.5047%	0.5048%	0.1837%	0.1843%	0.1548%	0.1560%
	THD	11.2146%	11.2153%	6.3666%	6.3921%	4.9846%	5.1051%
P = 21, M = 0.3	WTHD0	0.1040%	0.1038%	0.0368%	0.0367%	0.0159%	0.0159%
	WTHD	0.3540%	0.3536%	0.1234%	0.1239%	0.0531%	0.0534%
	THD	15.6613%	15.6551%	10.3887%	10.4136%	5.9341%	5.9564%
P = 21, M = 0.6	WTHD0	0.1446%	0.1445%	0.0290%	0.0289%	0.0200%	0.0201%
	WTHD	0.2462%	0.2460%	0.0486%	0.0488%	0.0334%	0.0338%
	THD	10.5095%	10.5046%	3.9553%	3.9653%	3.2664%	3.2814%
P = 21, M = 0.9	WTHD0	0.1208%	0.1208%	0.0365%	0.0366%	0.0247%	0.0249%
	WTHD	0.1371%	0.1371%	0.0408%	0.0411%	0.0275%	0.0278%
	THD	5.9266%	5.9251%	3.2043%	3.2134%	2.3157%	2.3279%
P = 31, M = 0.3	WTHD0	0.0478%	0.0477%	0.0168%	0.0168%	0.0068%	0.0070%
	WTHD	0.1628%	0.1624%	0.0563%	0.0567%	0.0228%	0.0235%
	THD	10.6378%	10.6291%	7.0399%	7.0482%	3.9845%	3.9980%
P = 31, M = 0.6	WTHD0	0.0665%	0.0664%	0.0129%	0.0129%	0.0083%	0.0087%
	WTHD	0.1132%	0.1130%	0.0216%	0.0218%	0.0139%	0.0146%
	THD	7.1389%	7.1357%	2.6584%	2.6613%	2.1648%	2.1720%
P = 31, M = 0.9	WTHD0	0.0553%	0.0553%	0.0158%	0.0158%	0.0094%	0.0101%
	WTHD	0.0628%	0.0628%	0.0177%	0.0178%	0.0105%	0.0113%
	THD	4.0213%	4.0198%	2.1463%	2.1497%	1.5050%	1.5112%

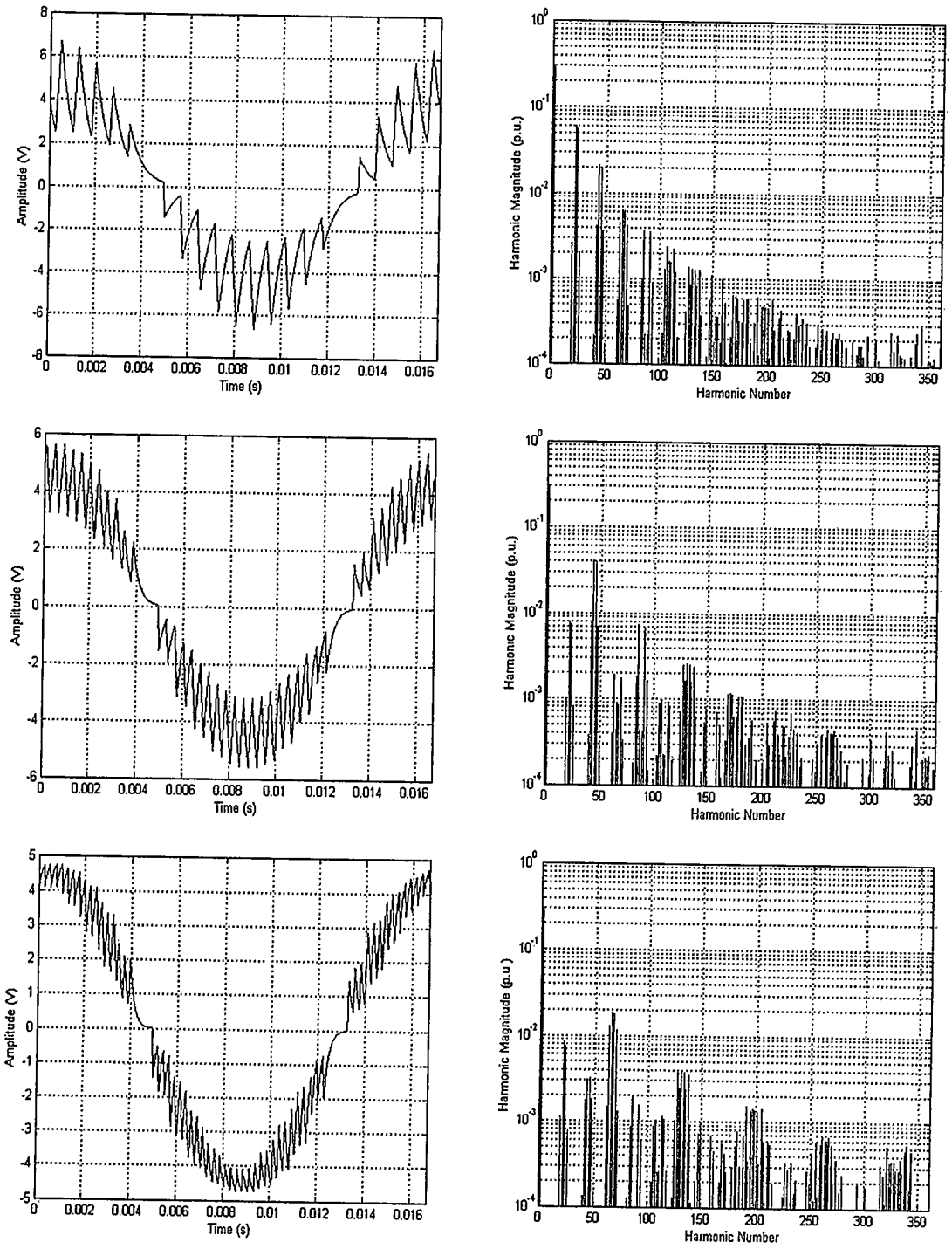


Fig. 4.9 Output voltage waveforms and their harmonic spectra for single, two and three parallel inverters modulated by double edge NSPWM with M = 0.3, fc/fs = 11

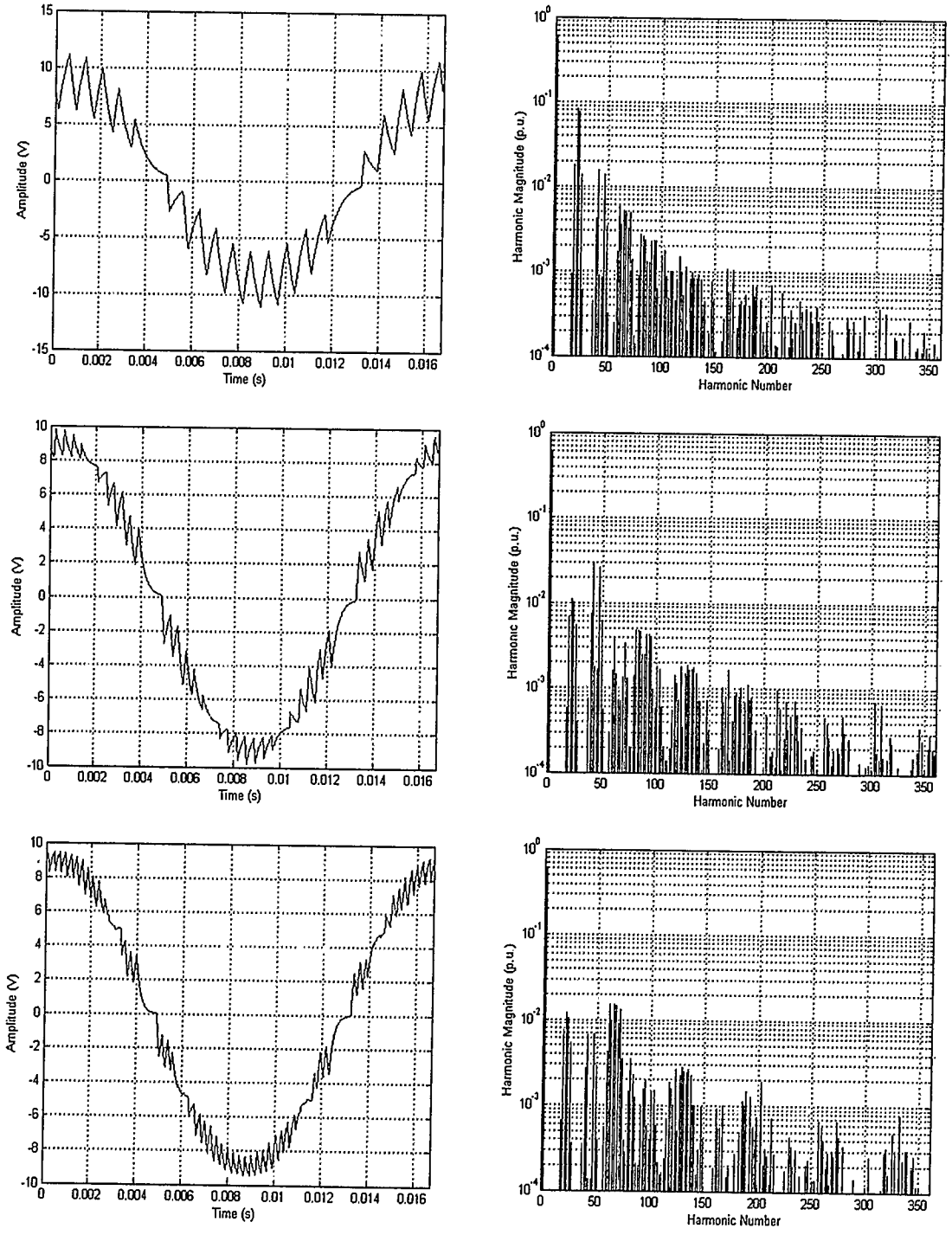


Fig. 4.10 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge NSPWM with M = 0.6, fc/fs = 11

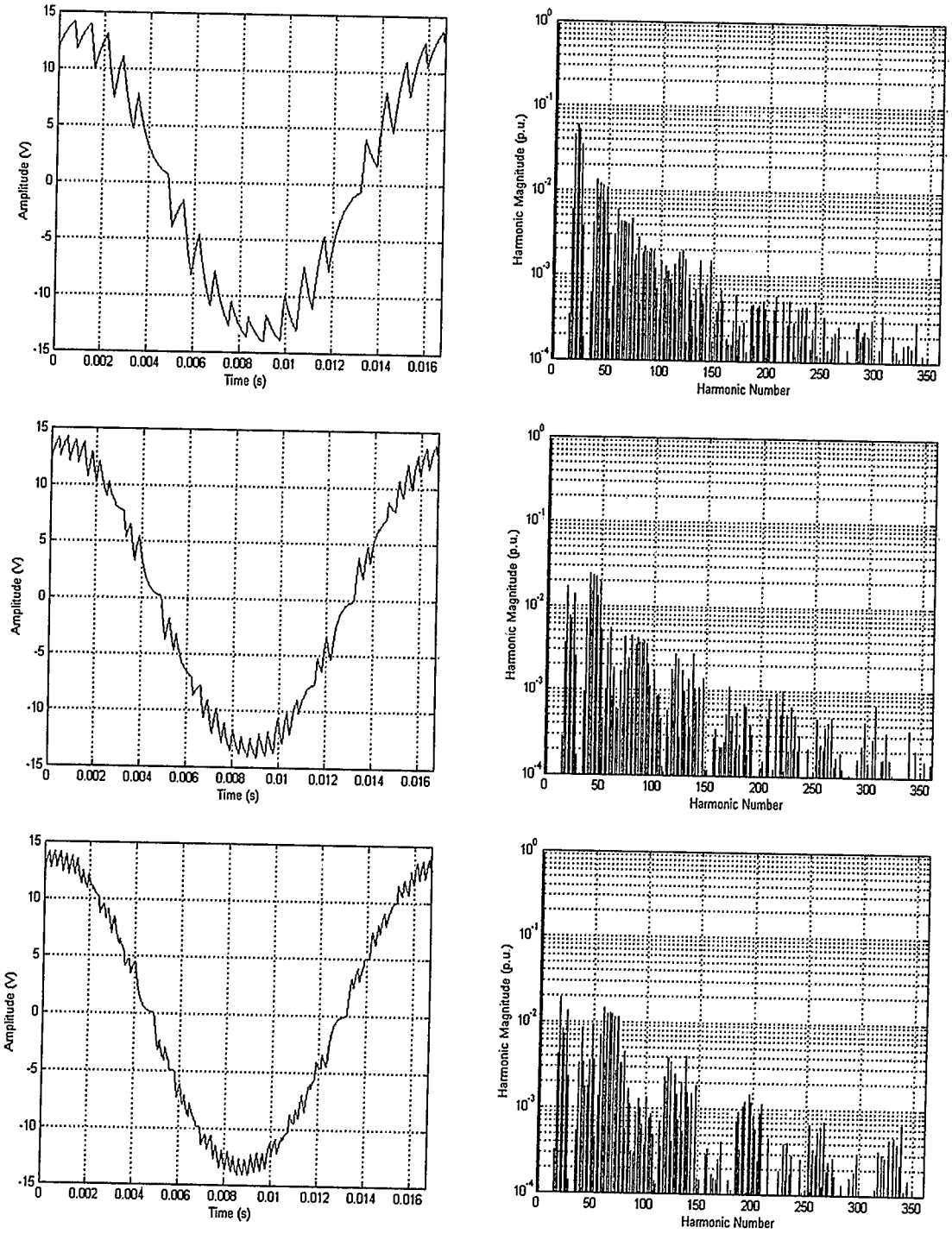


Fig. 4.11 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge NSPWM with M = 0.9, fc/fs = 11

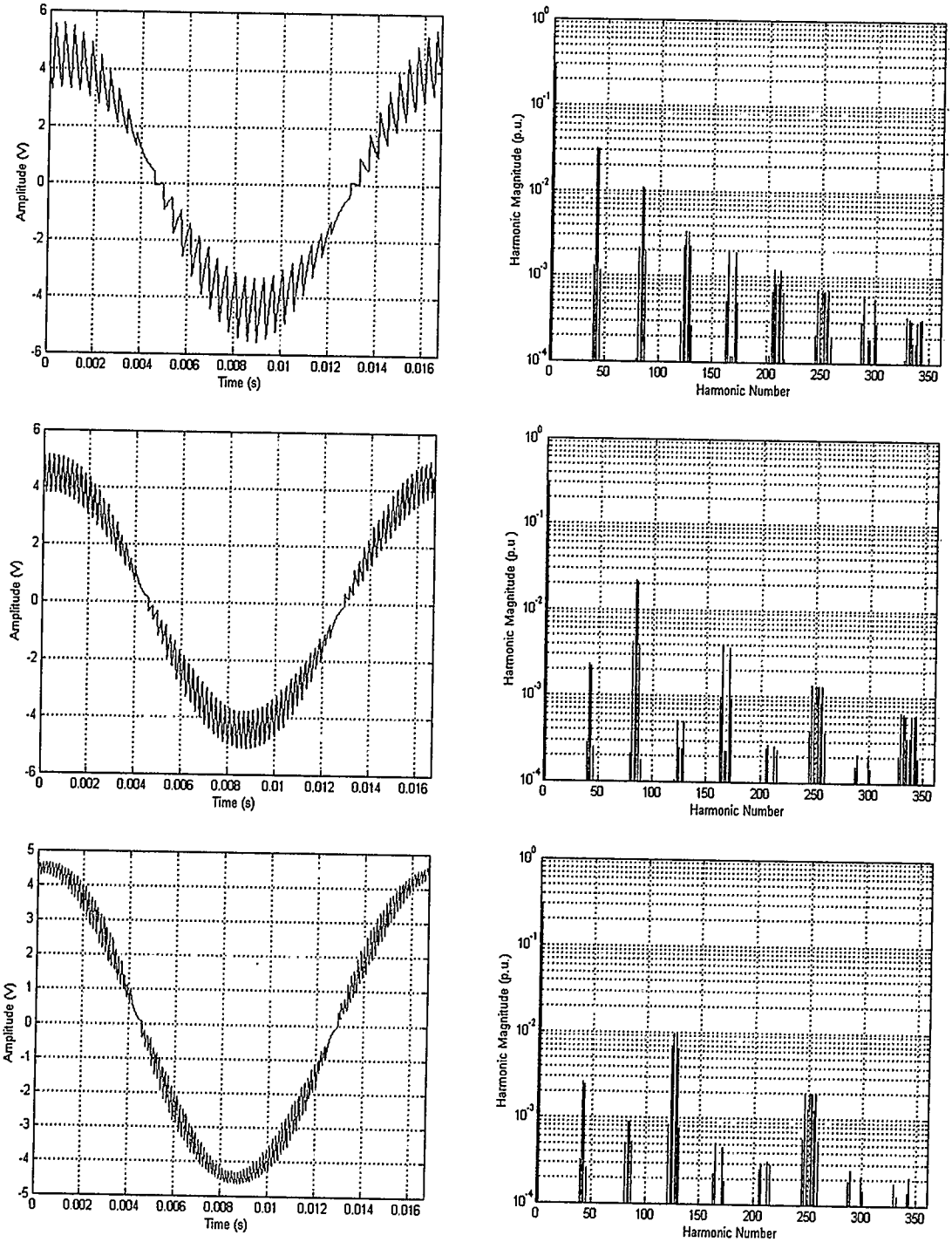


Fig. 4.12 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge NSPWM with M = 0.3, fc/fs = 21

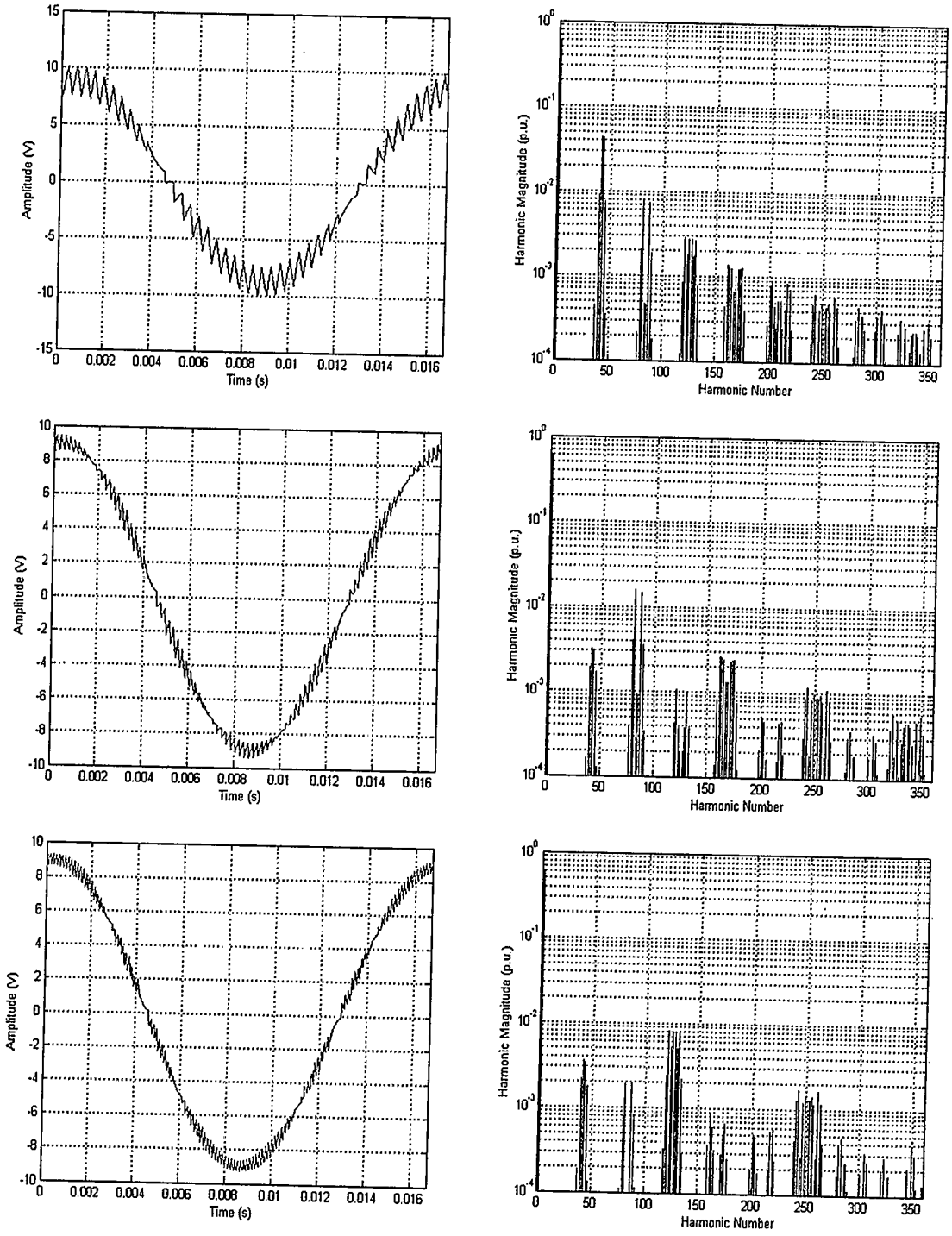


Fig. 4.13 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge NSPWM with M = 0.6, fc/fs = 21

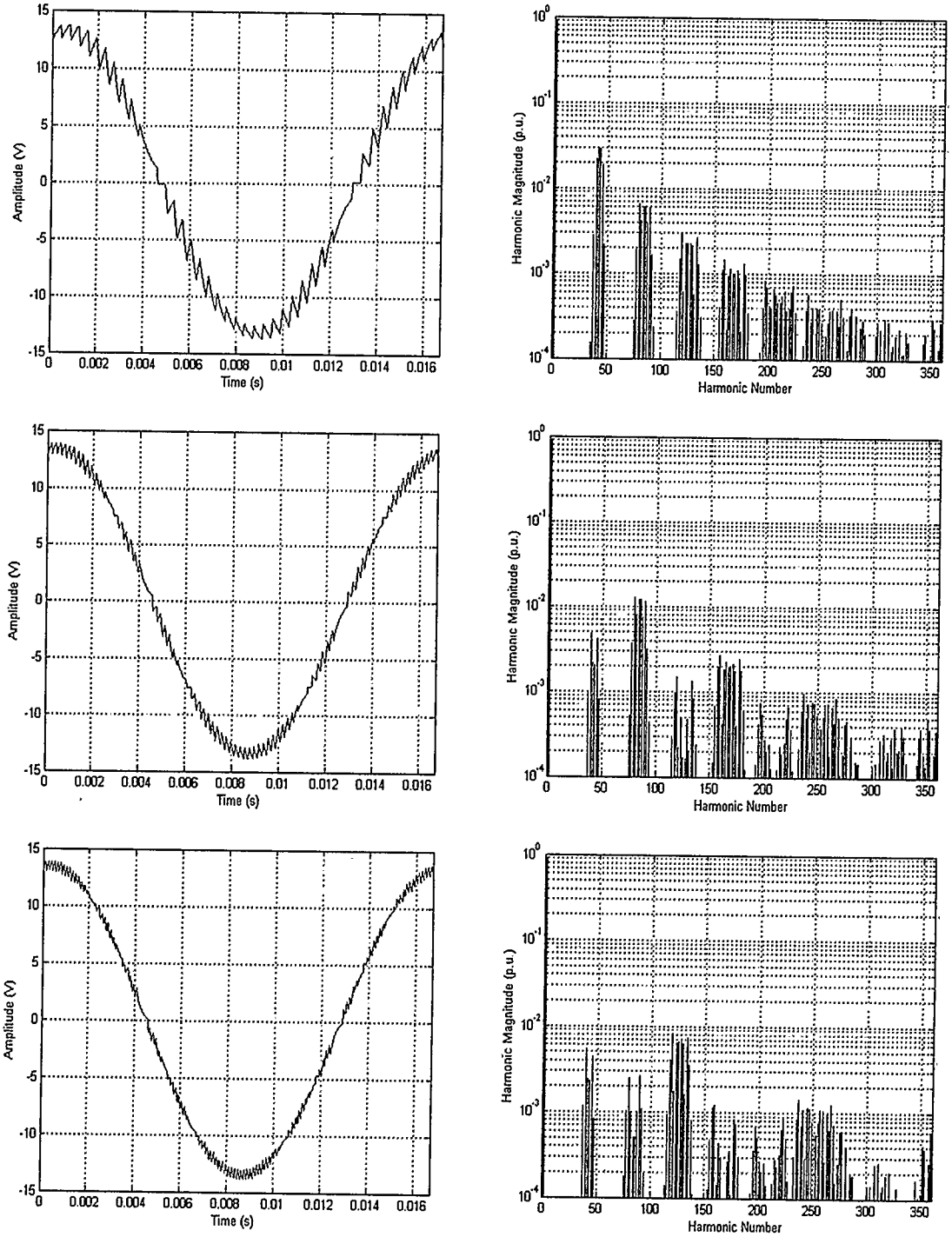


Fig. 4.14 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge NSPWM with M = 0.9, fc/fs = 21

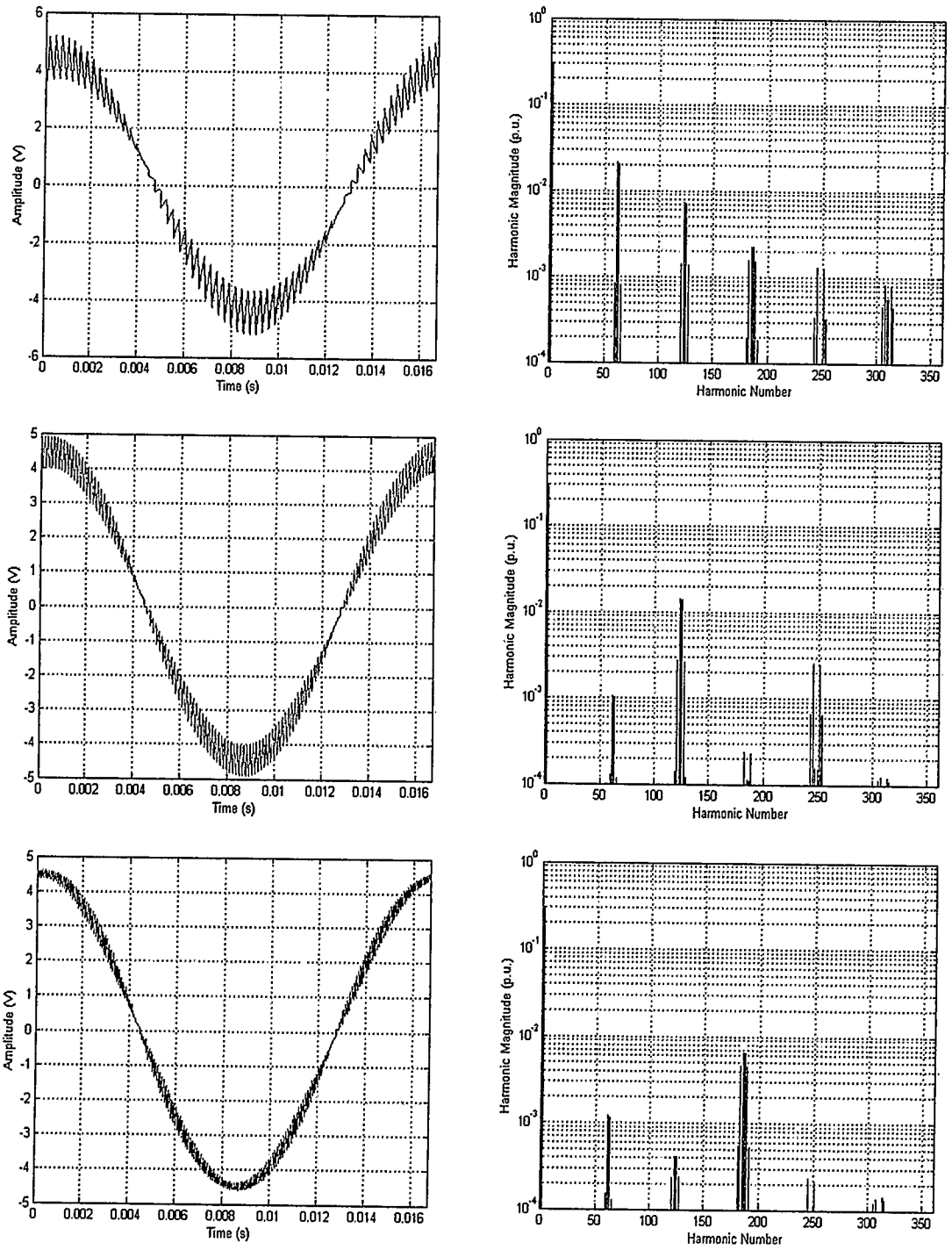


Fig. 4.15 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge NSPWM with M = 0.3, fc/fs = 31

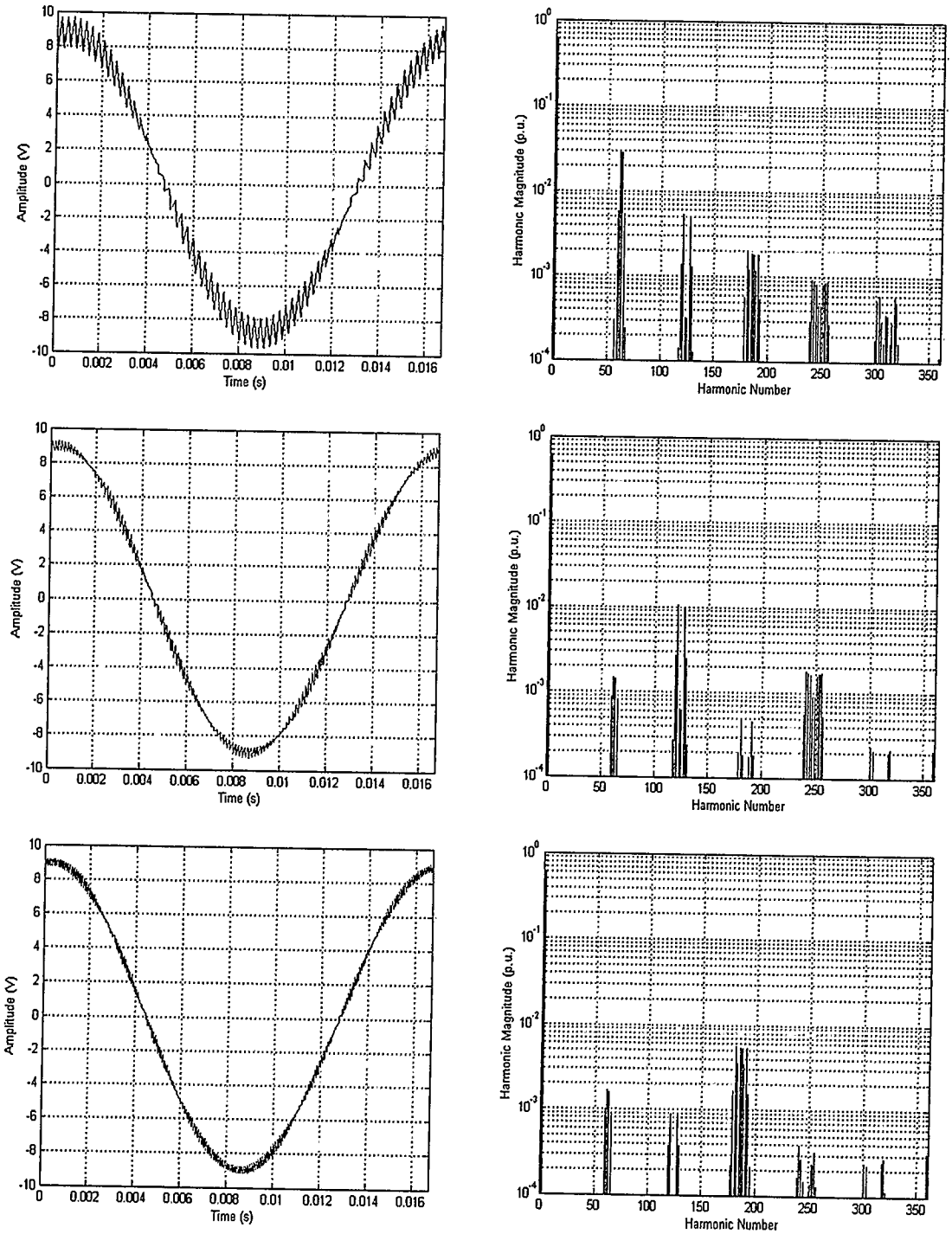


Fig. 4.16 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge NSPWM with M = 0.6, fc/fs = 31

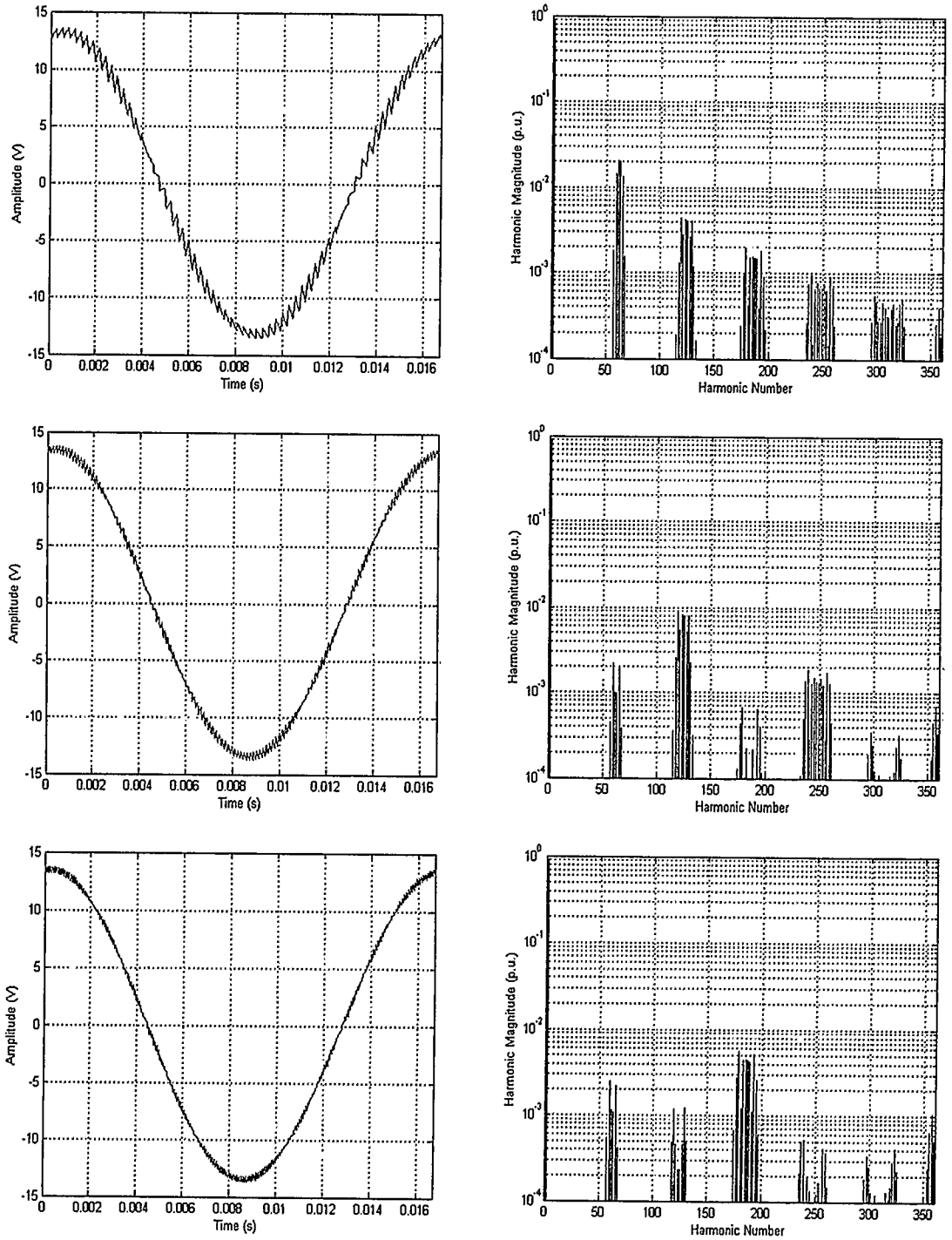


Fig. 4.17 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge NSPWM with M = 0.9, fc/fs = 31

4.3.2 Double-edge RSPWM

Figs 4.18 through 4.26 show sample computer simulation results. In those figure different output voltage waveforms and their harmonic spectra for one, two and three synchronized and optimally phase shifted parallel inverters for various value of the modulation index M and carrier to reference frequency ratio fc/fs, for a particular combination of load and inter-module reactor of R = 180Ω and L = 100mH, are plotted, all modulated by the double-edge asymmetrical RSPWM. The output voltages shown here are taken between the terminals of the load resistor. Table 4.2 gives the associate factor of merits (namely WTHD0, WTHD and THD) for every plot in those figures.

Table 4.2 Figures of merit associated with Figs. 4.18 through 4.26

		One Inverter		Two Inverters		Three Inverters	
		MATLAB	PSpice	MATLAB	PSpice	MATLAB	PSpice
P = 11, M = 0.3	WTHD0	0.3760%	0.3747%	0.1387%	0.1407%	0.0721%	0.0738%
	WTHD	1.2808%	1.2903%	0.4662%	0.4774%	0.2416%	0.2484%
	THD	29.5393%	29.8064%	19.7954%	19.7877%	11.6791%	11.2317%
P = 11, M = 0.6	WTHD0	0.5280%	0.5262%	0.1328%	0.1502%	0.1130%	0.1592%
	WTHD	0.8998%	0.9067%	0.2233%	0.2546%	0.1895%	0.2670%
	THD	19.8842%	20.0624%	7.7693%	8.0901%	6.7799%	6.5309%
P = 11, M = 0.9	WTHD0	0.4708%	0.4669%	0.2351%	0.2096%	0.2190%	0.2166%
	WTHD	0.5356%	0.5370%	0.2639%	0.2368%	0.2452%	0.2434%
	THD	11.3097%	11.4143%	6.4978%	6.9174%	5.0845%	4.9050%
P = 21, M = 0.3	WTHD0	0.1040%	0.1034%	0.0369%	0.0373%	0.0161%	0.0167%
	WTHD	0.3542%	0.3559%	0.1238%	0.1258%	0.0538%	0.0559%
	THD	15.6649%	15.7869%	10.3920%	10.3925%	5.9360%	5.9151%
P = 21, M = 0.6	WTHD0	0.1453%	0.1446%	0.0320%	0.0344%	0.0244%	0.0227%
	WTHD	0.2475%	0.2490%	0.0537%	0.0581%	0.0409%	0.0380%
	THD	10.5219%	10.6052%	3.9518%	4.0263%	3.2739%	3.2643%
P = 21, M = 0.9	WTHD0	0.1284%	0.1260%	0.0607%	0.0455%	0.0554%	0.0465%
	WTHD	0.1458%	0.1447%	0.0679%	0.0512%	0.0618%	0.0521%
	THD	5.9384%	5.9874%	3.2196%	3.3101%	2.3263%	2.3235%
P = 31, M = 0.3	WTHD0	0.0478%	0.0475%	0.0169%	0.0175%	0.0070%	0.0109%
	WTHD	0.1629%	0.1635%	0.0565%	0.0590%	0.0234%	0.0365%
	THD	10.6395%	10.7067%	7.0416%	7.0173%	3.9859%	3.9553%
P = 31, M = 0.6	WTHD0	0.0668%	0.0663%	0.0143%	0.0174%	0.0104%	0.0129%
	WTHD	0.1137%	0.1141%	0.0240%	0.0293%	0.0173%	0.0216%
	THD	7.1431%	7.1908%	2.6572%	2.6741%	2.1663%	2.1506%
P = 31, M = 0.9	WTHD0	0.0589%	0.0571%	0.0274%	0.0241%	0.0247%	0.0216%
	WTHD	0.0669%	0.0655%	0.0306%	0.0271%	0.0275%	0.0242%
	THD	4.0251%	4.0535%	2.1508%	2.1765%	1.5089%	1.4999%

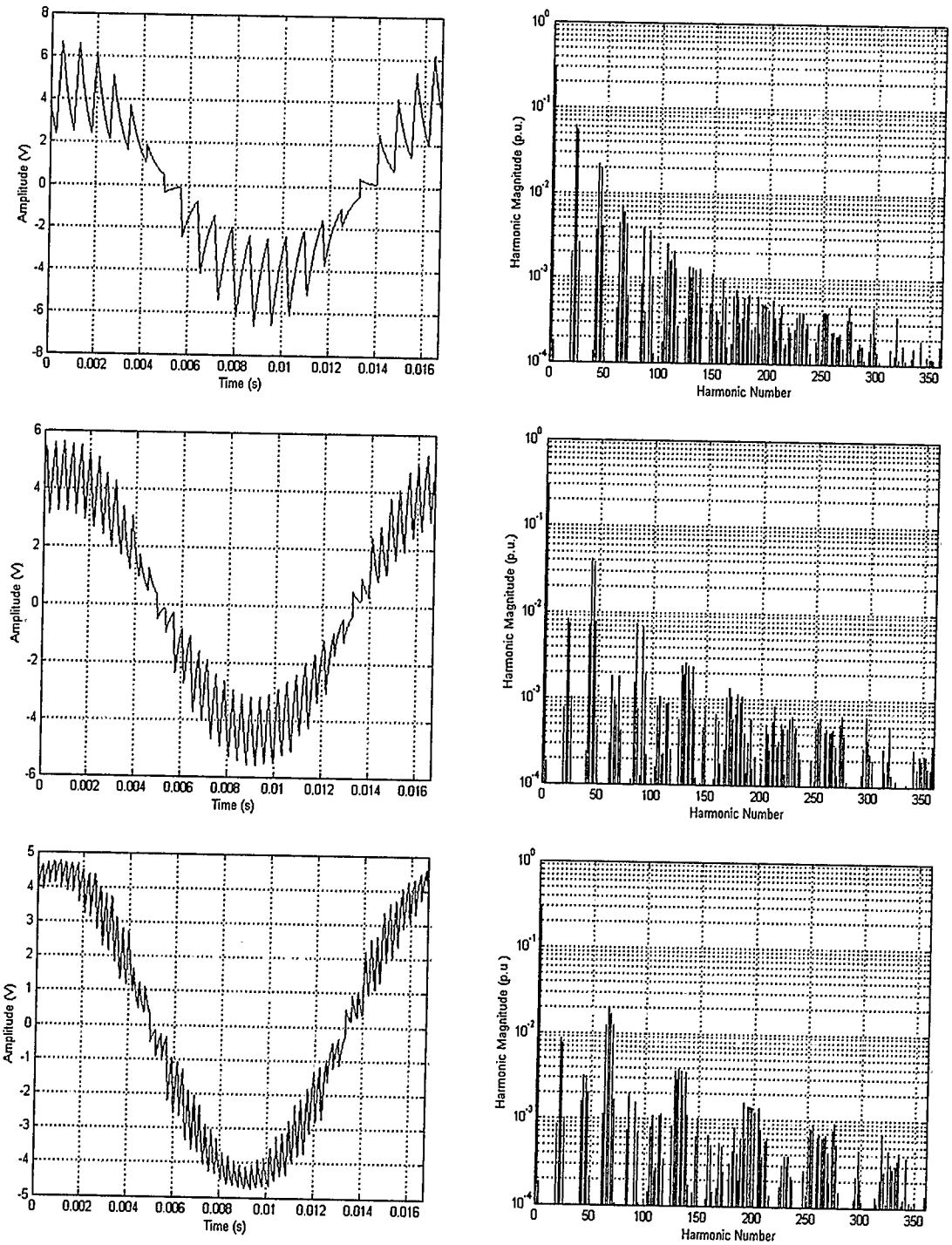


Fig. 4.18 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.3, fc/fs = 11

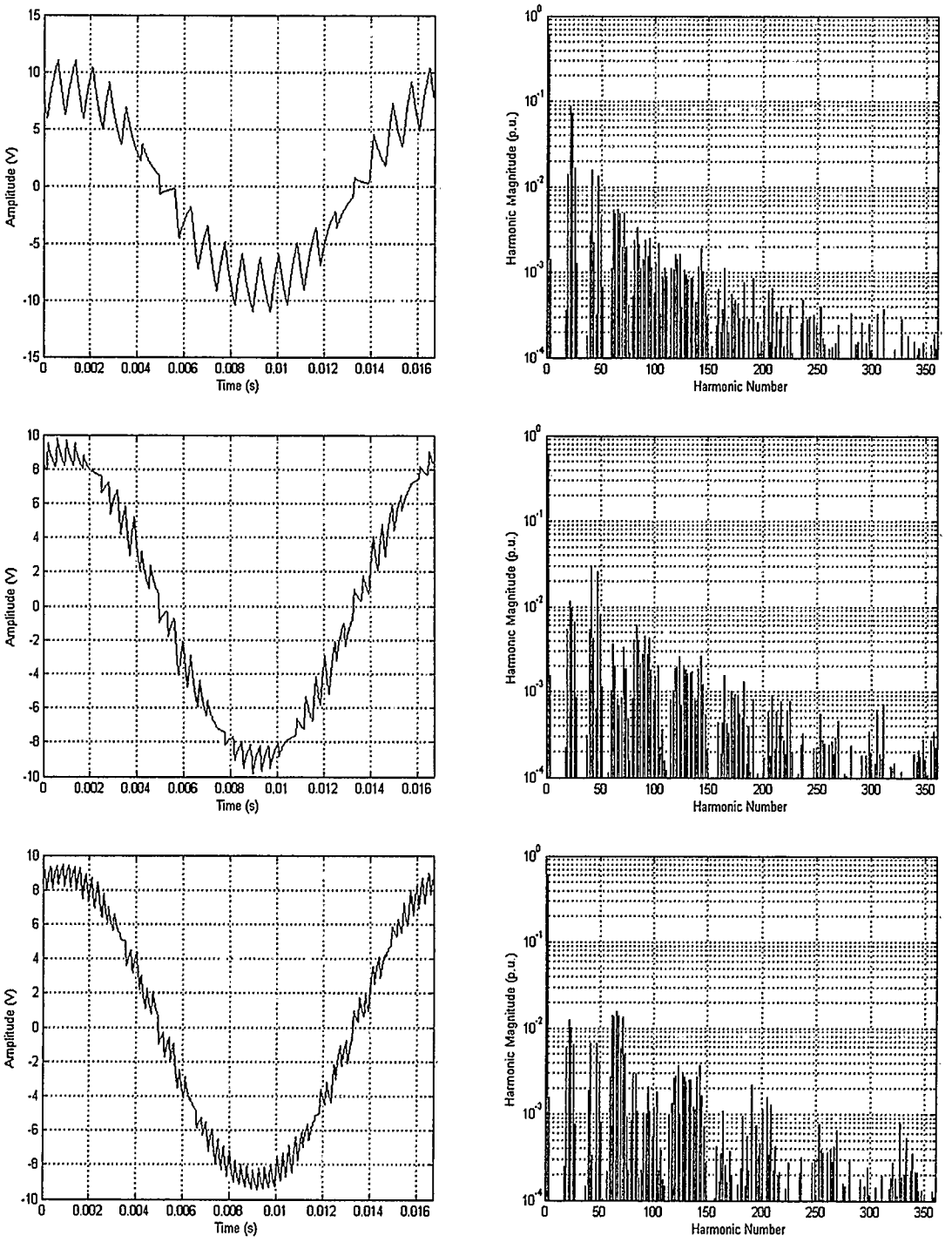


Fig. 4.19 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.6, fc/fs = 11

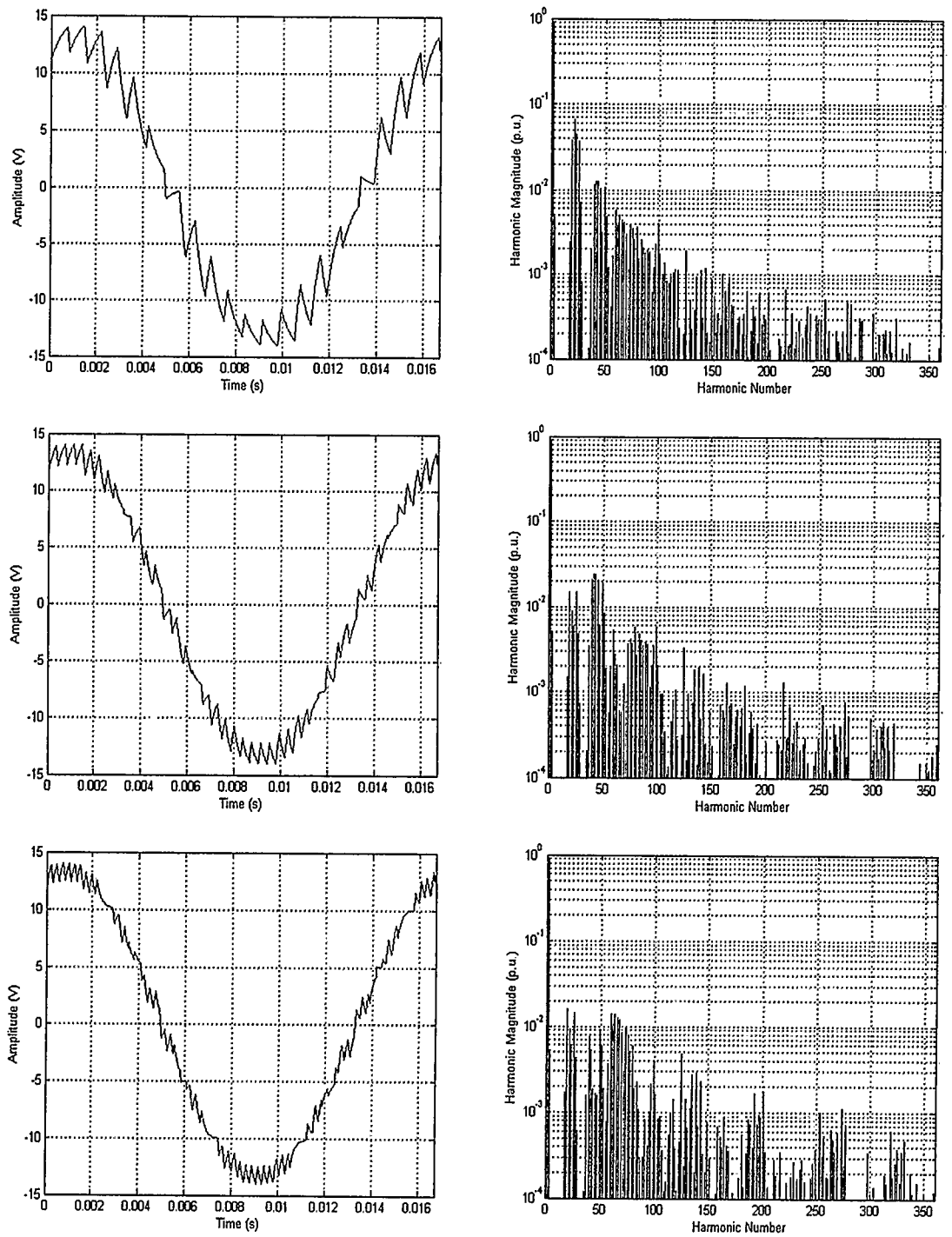


Fig. 4.20 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.9, fc/fs = 11

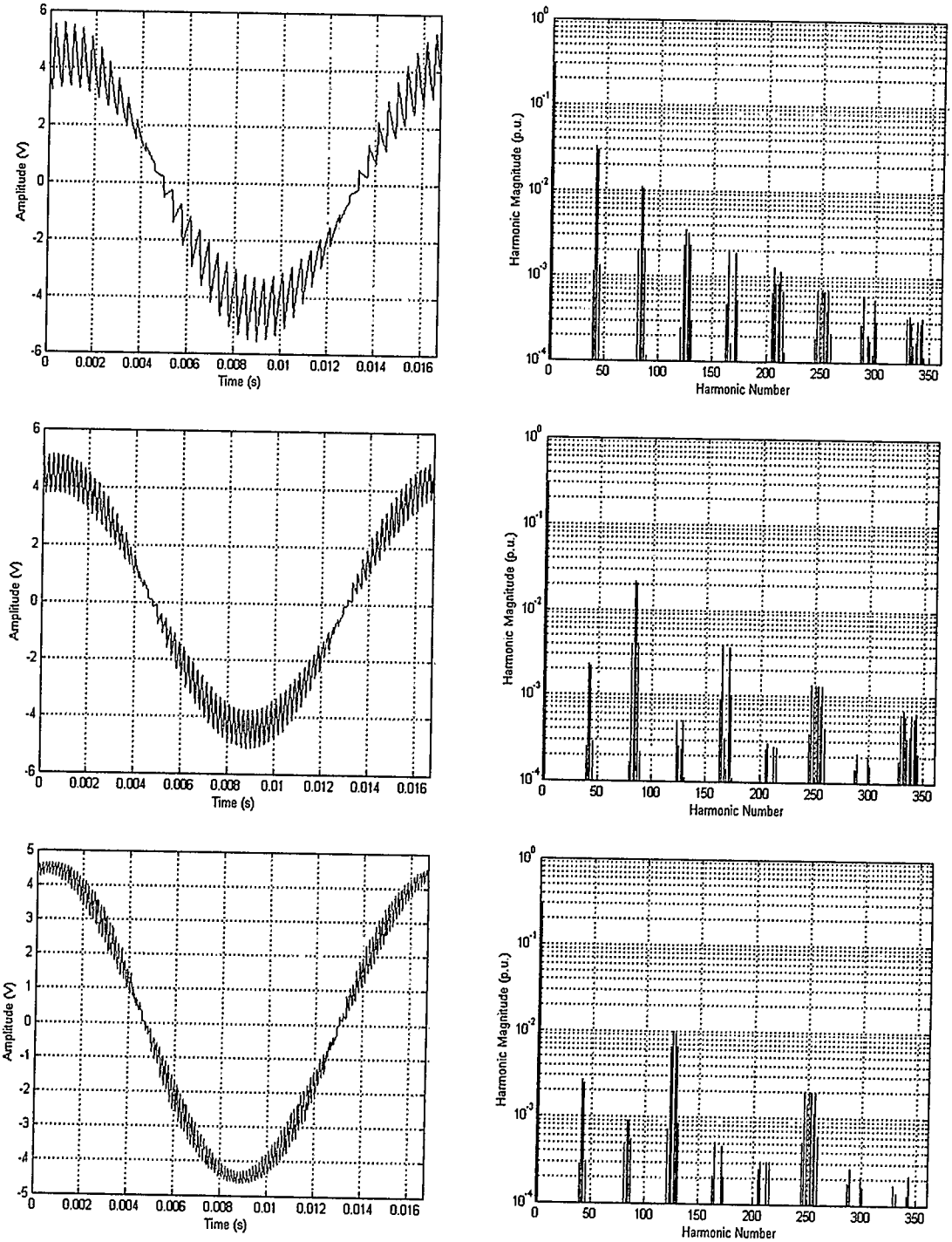


Fig. 4.21 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.3, fc/fs = 21

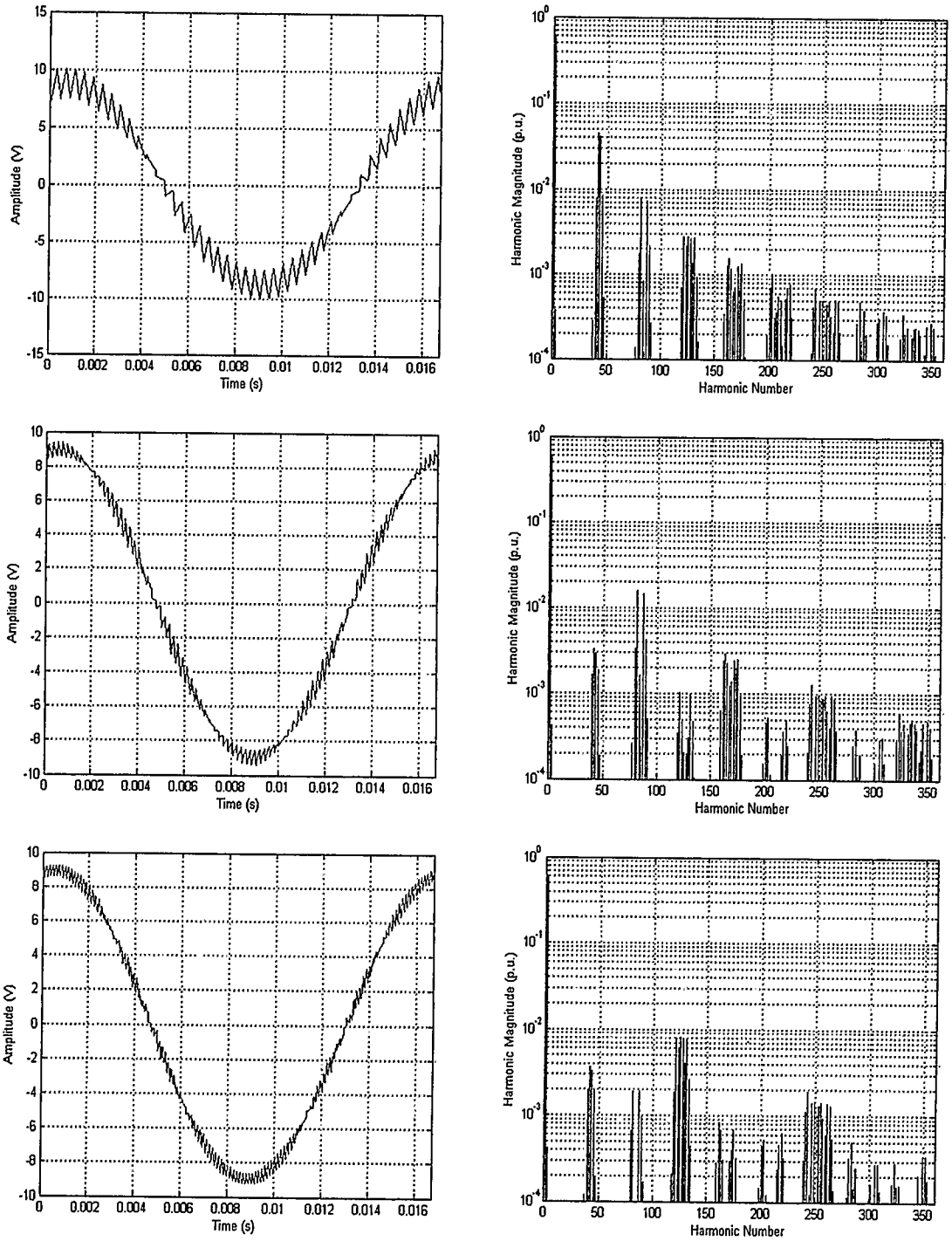


Fig. 4.22 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.6, fc/fs = 21

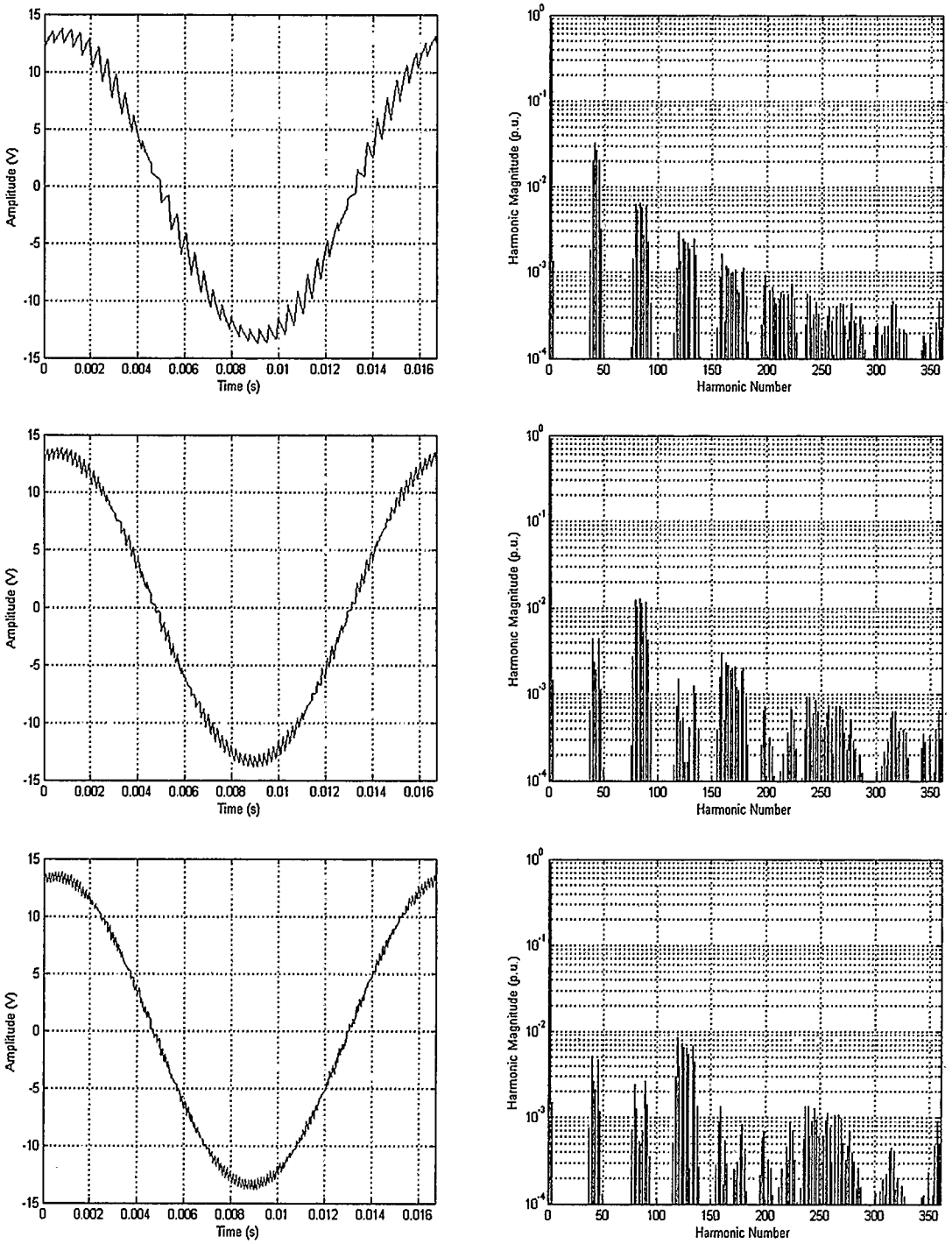


Fig. 4.23 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.9, fc/fs = 21

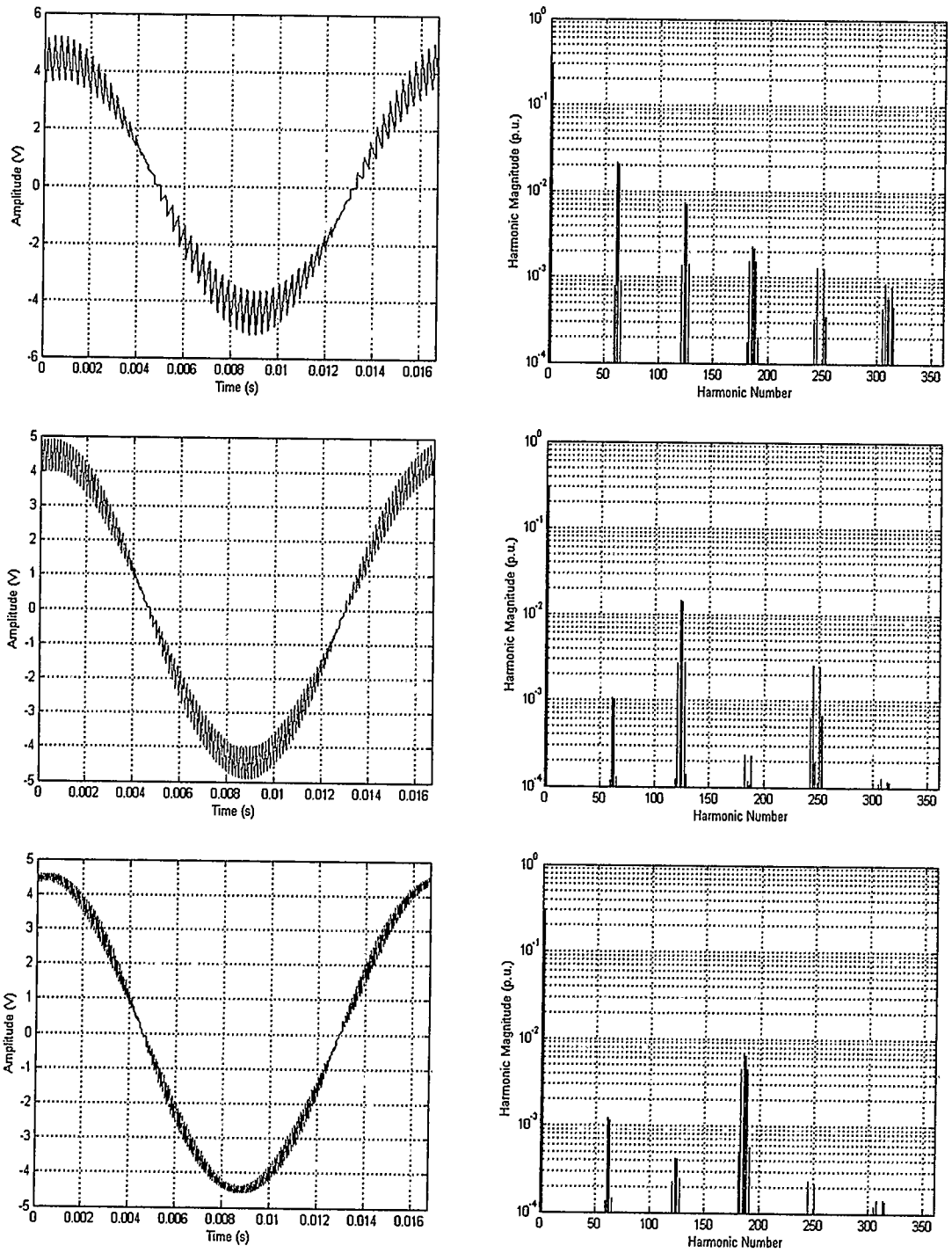


Fig. 4.24 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.3, fc/fs = 31

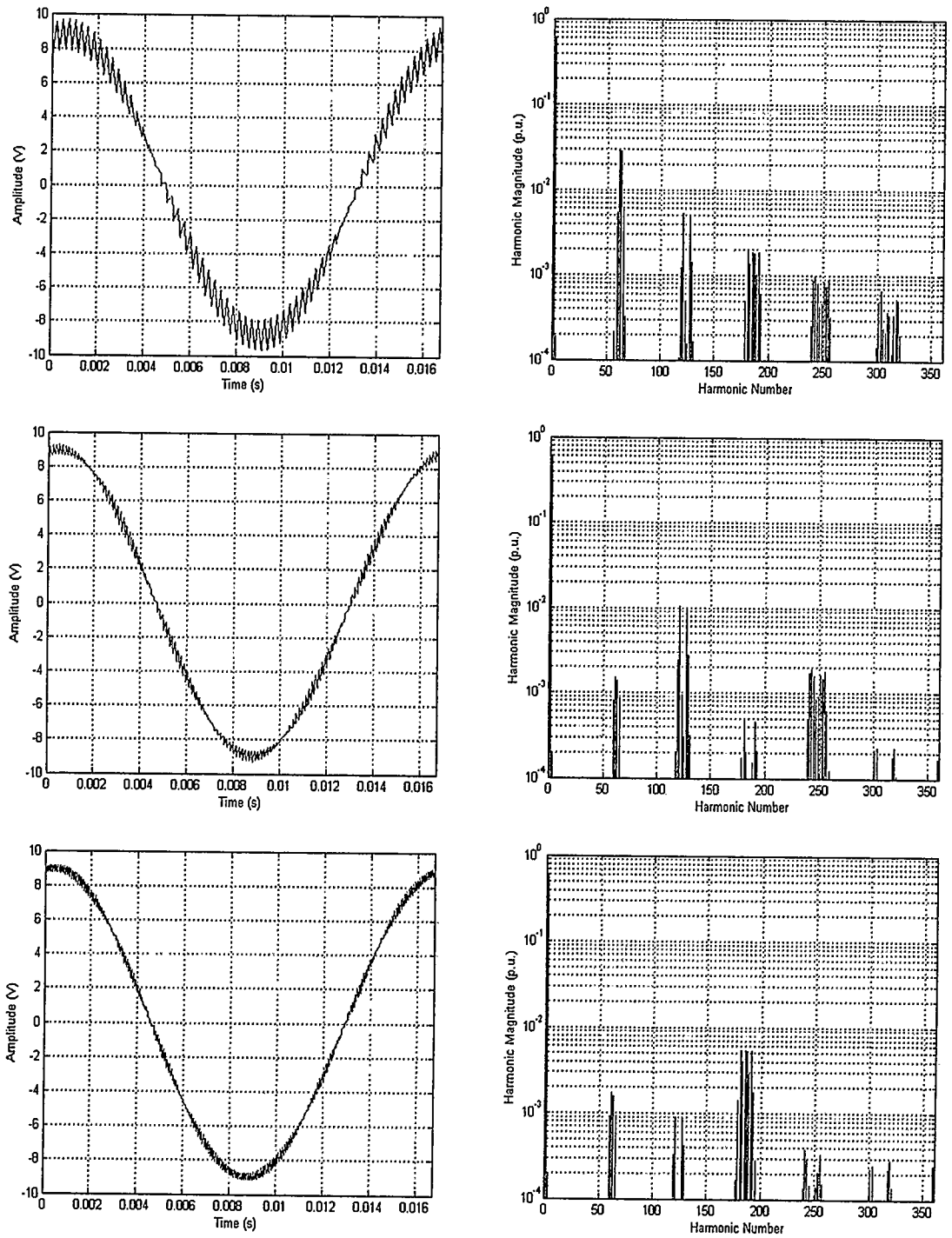


Fig. 4.25 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.6, fc/fs = 31

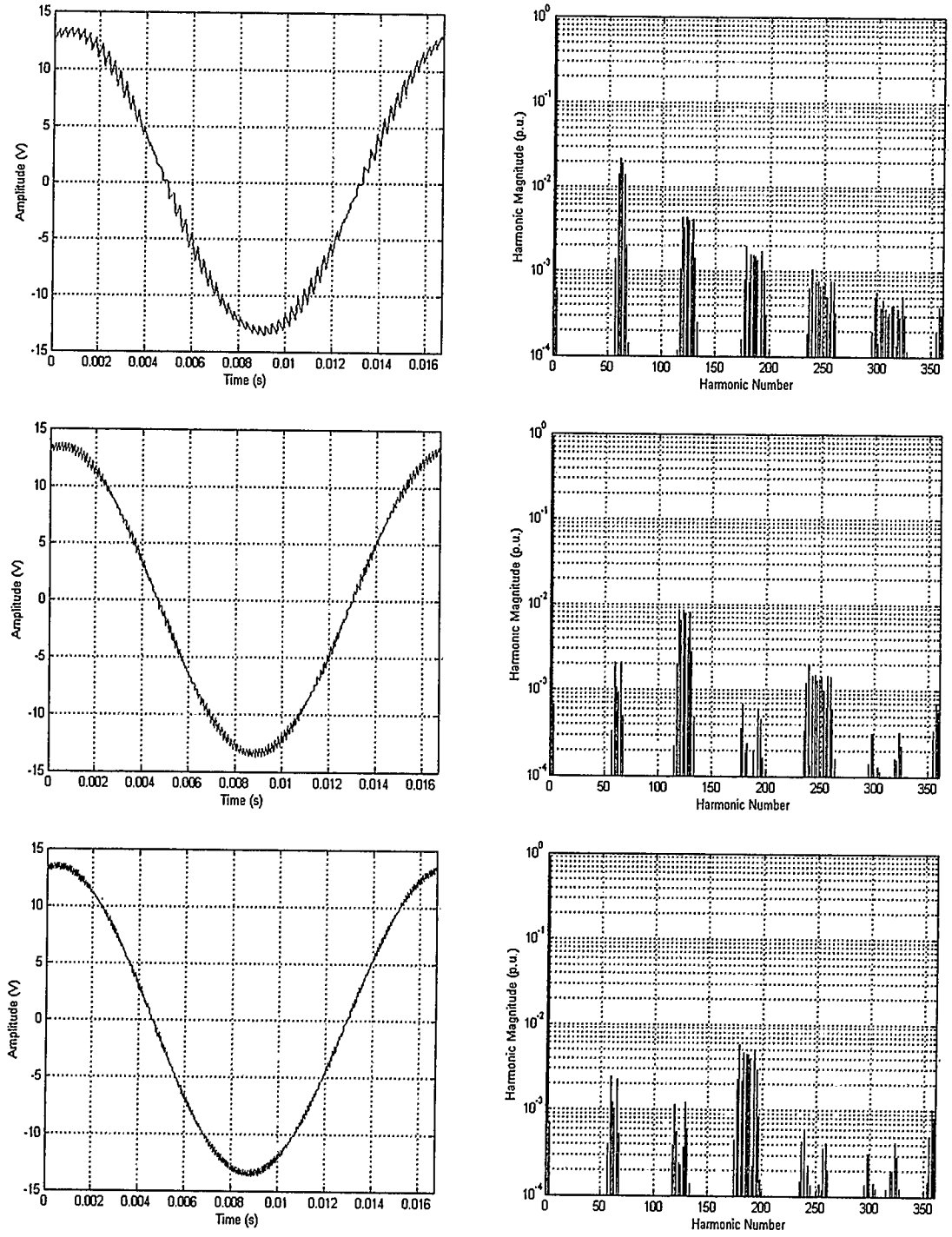


Fig. 4.26 Output voltage waveforms and their harmonics spectra for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.9, fc/fs = 31

4.4 Over-modulation Region

Fig.4.27 shows, for the case of one inverter, how the fundamental component of the unfiltered output voltage varies as a function of modulation index M. Note that in the limit, as M is increased, the output voltage waveform becomes a square wave, which of course has a fundamental amplitude of $4/\pi = 1.27$ times the dc input voltage.

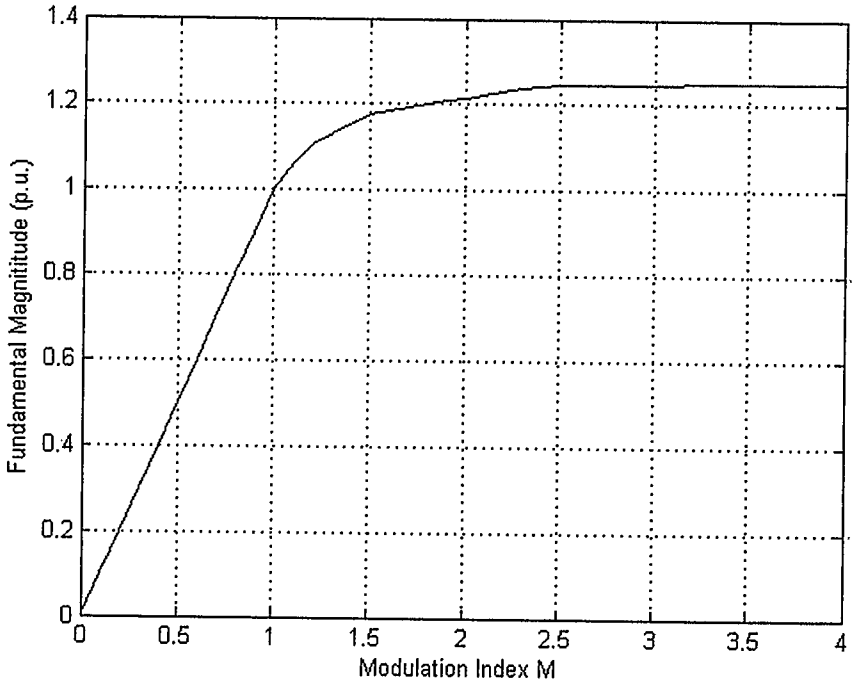


Fig. 4.27 Unfiltered output voltage fundamental amplitude as a function of modulation index M

The fundamental magnitude of the output voltage varies linearly with the modulation index M when $M \leq 1$, after which over-modulation occurs, ie, when the modulation index M increases beyond unity. In this over-modulation region the amplitude of the fundamental continues to increase but is no longer linear with M. This causes the output voltage to contain many more harmonic components in sidebands as compared with the linear range, as is clear on Fig. 4.28. Table 4.3 gives the associated figures of merit.

Figs. 4.29 to 4.31 give us a glimpse in the switching process occurring in the over-modulation region for the case of M = 2.0. It is clear form those figures how as M

becomes sufficiently large, the PWM inverter degenerates from a pulse width modulated inverter into a square wave inverter, the output voltage then becomes a square wave, whose fundamental voltage amplitude is 1.27Vdc, the highest possible value produced by two-level VSI. Over-modulation is seldom used in practice due to the difficulties in filtering out the low-order harmonics [50].

Table 4.3 Distortion figures of merit for the case of over-modulation double edge NSPWM with M = 1.5, fc/fs = 21

	One Inverter	Two Inverters	Three Inverters
WTHD0	3.7158%	4.1645%	4.2699%
WTHD	3.2431%	3.5796%	3.6595%
THD	13.4338%	14.5660%	14.8802%

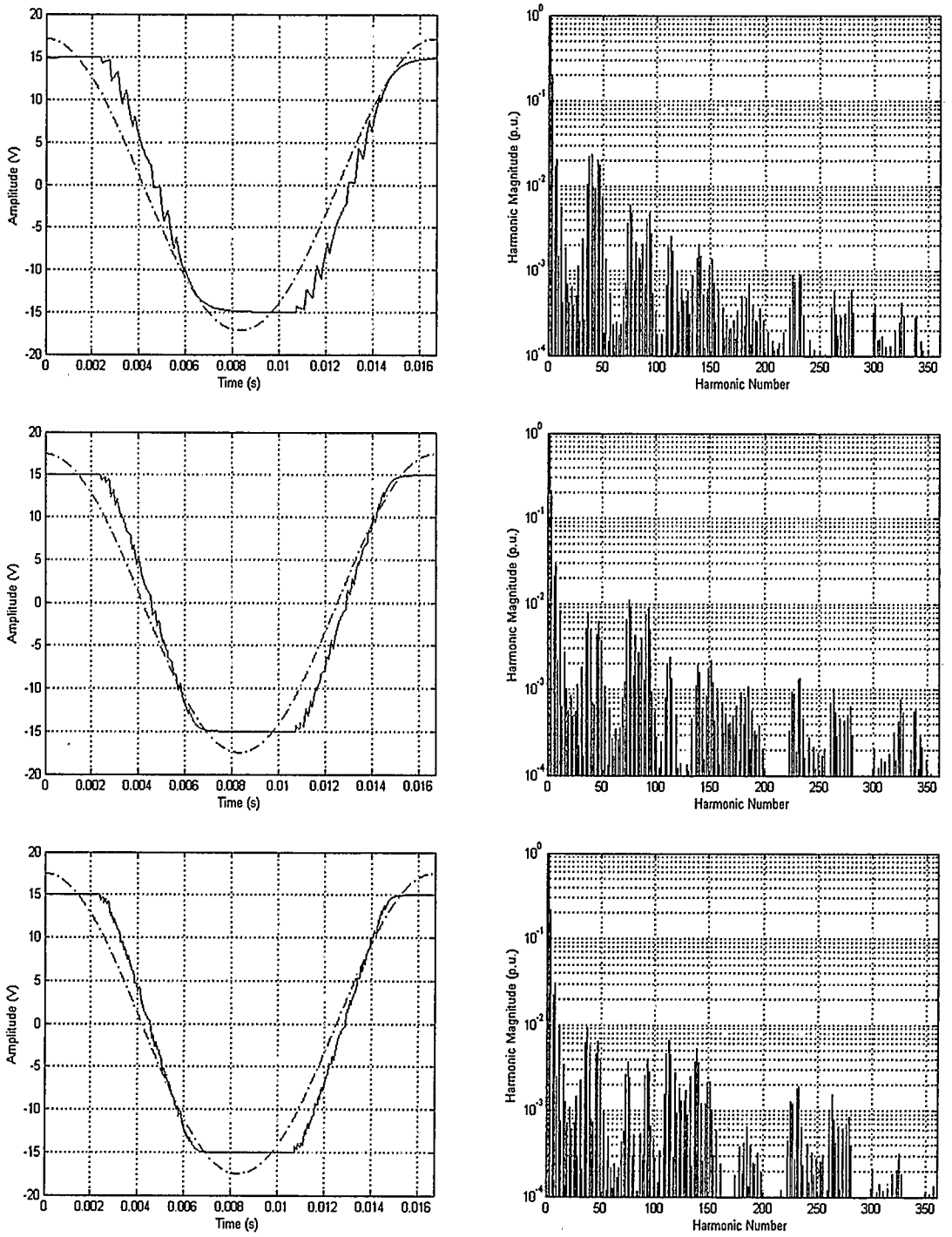


Fig. 4.28 Output voltage waveforms and their harmonic spectra for single (top), two (middle) and three (bottom) parallel inverters modulated by double edge NSPWM with M = 1.5, fc/fs = 21; the dashed line is the fundamental waveform.

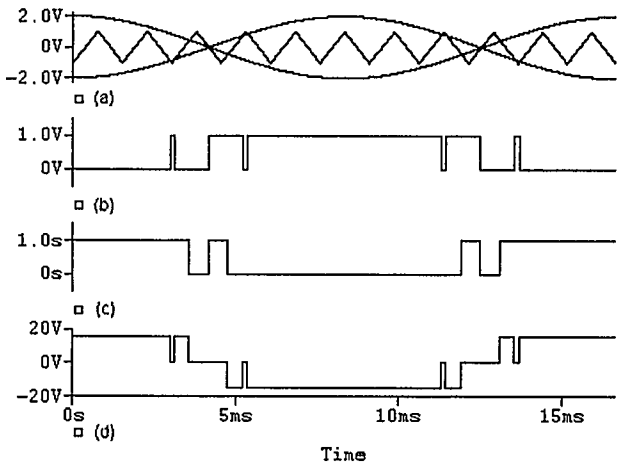


Fig. 4.29 Double-edge NSPWM process for one single-phase inverter, M = 2, fc/fs = 11; (a) Identical carriers with inverted references; (b), (c) Gating signals for the phase legs; (d) Unfiltered voltage waveform at the output of one inverter.

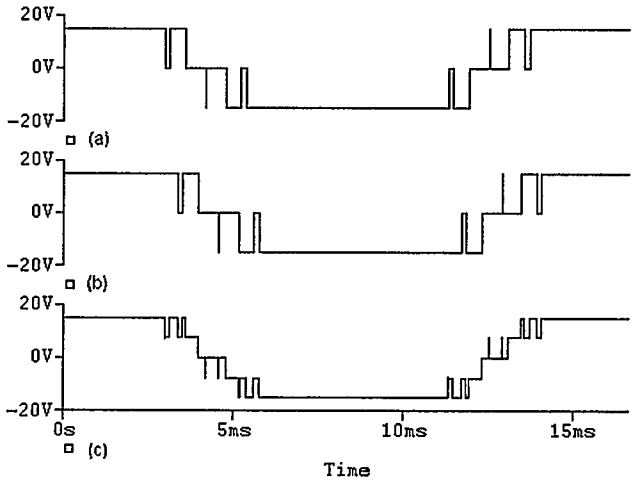


Fig. 4.30 Output voltage waveforms for two synchronized, optimally phase-shifted inverters operated in parallel with M = 2, fc/fs = 11; (a), (b) Unfiltered voltage waveform for each of the two inverters; (c) Equivalent unfiltered voltage waveform at the output of inverters

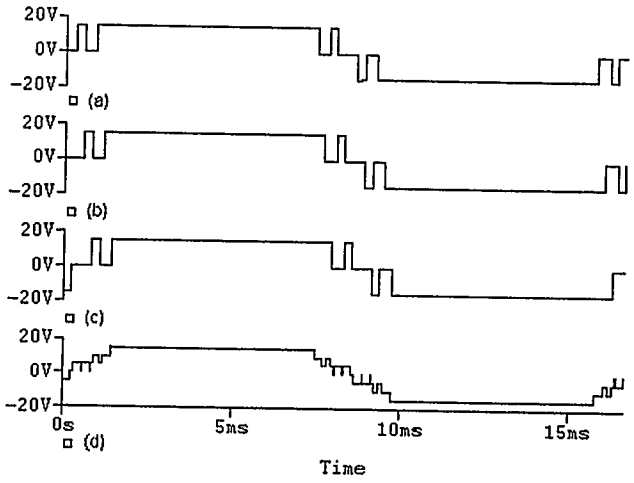


Fig. 4.31 Output voltage waveforms for three synchronized, optimally phase-shifted inverters operated in parallel with M = 2, fc/fs = 11; (a), (b) and (c) Unfiltered voltage waveform for each of the three inverters ; (d) Equivalent unfiltered voltage waveform at the output of inverters

4.5 Discussion of the Simulation Results

By comparing the results in Tables 4.1 and 4.2 with the theoretical ones given in Tables 3.3 and 3.4 of the previous chapter we can see that our simulation study agrees with the theoretical results. This agreement is more pronounced for the MATLAB results than for the PSpice results for the following reasons.

When we ran many of the above cases with the PSpice simulator we had to deal with convergence problems (basically the simulation hung-up sometime before finishing). To overcome this convergence problem we had to tweak several parameters to improve convergence, and a direct consequence of that is a loss of accuracy in the simulation. Indeed, in Tables 4.1 and 4.2 PSpice results accuracy is lower and differs from one cell to another.

Note also that Table 4.1 (Double-edge NSPWM) agrees completely with its counterpart in theory, Table 3.3, while Table 4.2 (Double-edge RSPWM) sometimes has slightly different values compared to Table 3.4. This is due to the complication added to the simulation by the sample and hold circuit used in the double-edge asymmetrical RSPWM. We know this because when we specify a higher precision in Simulink (see

Fig.C.4 in the Appendix C) we ran out of memory. This is understandable knowing that the sample and hold circuit is simulated using an embedded MATLAB function, and the overhead associated with function calling is known in numerical method programming.

In addition, Tables 4.1 and 4.2 show that THD decrease with an increase in both the modulation index M and the carrier to reference frequency ratio P. This is, of course, an intrinsic characteristic of the pulse width modulation techniques, indeed as the modulation index M increases the fundamental of the parallel inverters output voltage increases proportionally (see, for example, eqn. (3.3) in Chapter 3) while the accumulated harmonics' magnitudes remain relatively constant which leads to lower figures of merit; in the same manner increasing the carrier to reference frequency ratios leads to a better time domain approximation of the reference voltage waveform at the parallel inverters output (which is equivalent to pushing the harmonics towards higher frequency in the frequency domain) giving hence better figures of merit.

Tables 4.1 and 4.2 also indicate that the THD improvement resulting from operating multiple inverters in parallel is not linear; meaning that, for example, the decrease in THD values is not inversely proportional to the number of inverters in parallel (N). Indeed the above mentioned two tables show that THD added reduction is quite small when we go from two parallel inverters configuration to three parallel inverters configuration as compared to going from single inverter to two parallel inverters configuration especially for high value of carrier to reference frequency ratios P (P = 21 and 31 in Tables 4.1 and 4.2). And therefore the number of inverters practically being put in parallel should be carefully weighted against the gain in total harmonic distortion reduction obtained.

4.6 Chapter Summary

In this chapter, we started by presenting the results of simulations showing that the optimum phase delay for two synchronized and phase-shifted inverters, operated in parallel, is exactly Tc/4, ie, the optimum phase delay that yields the lowest harmonic distortion factors occurs when the second inverter has its power switching-transistor gating functions time-shifted by Tc/4 relative to the first inverter, where Tc is the period

of the triangular carrier. In the case of three synchronized and phase-shifted inverters operated in parallel, the optimum phase-delay becomes Tc/6, meaning that the second inverter has its power transistor gating functions time shifted by Tc/6 relative to the first inverter, and that the third inverter needs a gating time shift of double that (ie, Tc/3) relative to the first inverter. Also presented in this chapter are sample simulation results for one inverter, two and three synchronized, optimally phase shifted parallel inverters for various values of index modulation M and carrier to sine reference frequency ratios fc/fs for a particular combination of load and inter-module reactor of R = 180Ω and L = 100mH using both modulation techniques discussed in this thesis (namely, double-edge naturally sampled PWM and double-edge asymmetrical regularly sampled PWM). The chapter concludes with a discussion of operation in the over-modulation region.

Chapter Five: EXPERIMENTAL RESULTS

5.1 Introduction

A low voltage laboratory prototype was built, using bipolar technology transistors, to validate the simulation results presented in the previous chapter. Only the double-edge asymmetrical RSPWM method was used because it is easier to implement in a digital system, such as the microcontroller PIC 16F877[5], and as seen in Chapter 3 the THD degradation accumulated due to this modulation technique when compared to double-edge NSPWM are negligible. Fig. 5.1 illustrates the block diagram of the implemented scheme. Table 5.1 lists the parameters used in the experiment.

In the following sections we will give a brief description of the experimental setup used, to be followed by a selection of experimental results.

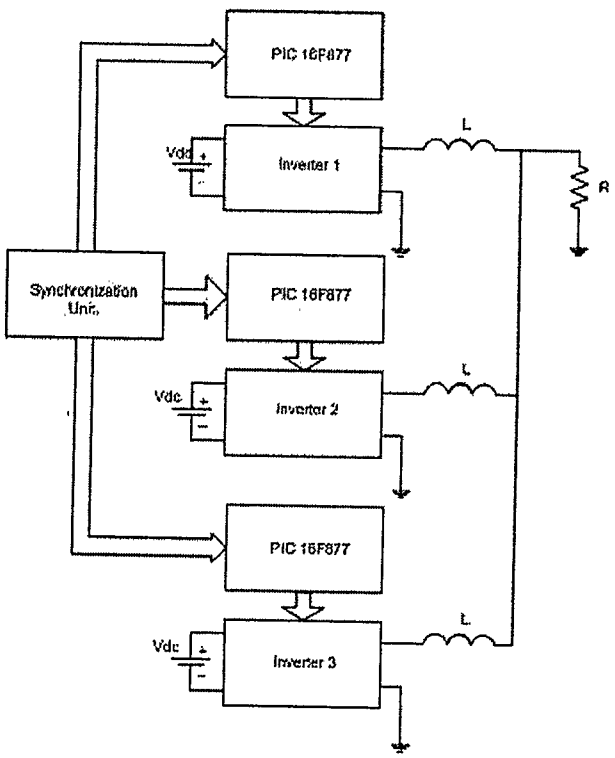


Fig. 5.1 Block diagram of the experimental set-up

[5] See Microchip Technology's website (http://www.microchip.com/) for the datasheet.

5.2 Experimental Set-up Description

The experimental results presented in this chapter were carried out in the Power Electronics Lab at the University of Calgary.

The hardware used is as follow:

- Tektronix TDS3032B 300MHz Two Channel Digital Phosphor Oscilloscope with a Sample Rate of 2.5 GS/s per Channel
- Tektronix P5205 High Voltage Differential Probe
- Agilent 33120A 15 MHz Function / Arbitrary Waveform Generator
- Fluke 8050A 4.5 Digit Digital Multi-meter
- Fluke 39 Power Quality Analyzer
- WAVETEK 182A 4MHz Function Generator
- Laboratory power supplies from Xantrex Technology Inc. and Brunelle Instruments Inc

In addition Microchip's PIC Programmer PICSTART Plus, operated with Microchip's MPLAB Integrated Development Environment software IDE[6] package, was used to program our controllers using assembly language.

5.2.1 Base Drive Circuits

A Bipolar Junction Transistor (BJT) base drive circuit is a circuit designed to minimize the turn-on and turn-off switching times of a power switching transistor and provide sufficient base current to keep the transistor saturated in the on-state.

Table 5.1 Parameters used in the experiment

Parameter	Value
fc/fs	11, 21 and 31
M	0.3, 0.6 and 0.9
Vdc	15 V
L	100 mH
R	180 Ω

[6] Freely available for download from Microchip Technology's website (http://www.microchip.com/)

To evaluate our need for a special base drive circuitry in the design at hand, we used the circuit shown in Fig. 5.2 to test drive our 2N4401[7] transistor (this is the NPN transistor used in the two bottom transistors in every H-bridges in the experimental set-up, see section 5.2.3 below). The element values shown are exactly the same as those used in our experimental set-up. The pulse generator denoted by V2 in Fig. 5.2 has a frequency of 1 KHz and a duty of 0.5 with a voltage alternating between 0V and 15V. In this section we present simulations of this circuit to see how fast our transistors may be turned on and off.

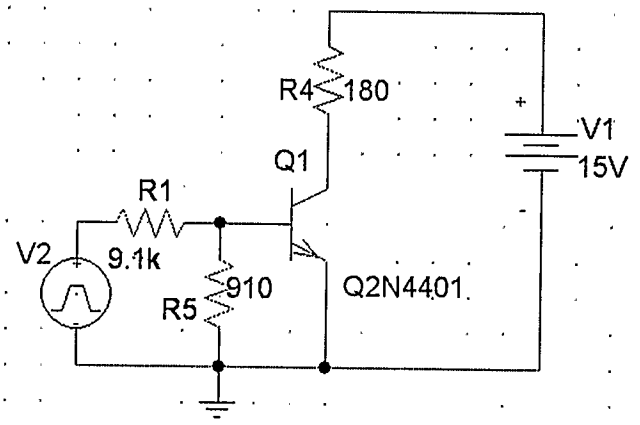


Fig. 5.2 2N4401 base drive circuit

Fig. 5.3 shows the base and collector currents of the 2N4401 at turn-on and Fig. 5.4 shows these currents at turn off. From these two figures we can see that the time taken by the transistor to turn on and off is less than 0.3 μs (the Fairchild datasheet specify those turn-on and turn-off switching times to be ≤ 200ns). Similar switching times were obtained for the 2N4003[8] (a PNP transistor used at the top of the H-bridges in the experimental set-up; see section 5.2.3). Since the shortest pulse that can be generated by the assembly code written for the PIC-16F877 microcontroller (see Appendix C) is ten

---

[7] Datasheet freely available for download from Fairchild Semiconductor's website (http://www.fairchildsemi.com)

[8] Datasheet freely available for download from Fairchild Semiconductor's website (http://www.fairchildsemi.com)

times the single op-code instruction cycle = 10*1/(¼*12MHz) = 3.33 μs[9], and because this is much larger than the turn on and off times obtained for the transistors in Figs 5.3 and 5.4, we conclude the transistors have enough time to reach their on or off steady-state and hence no additional base drive circuitry is necessary.

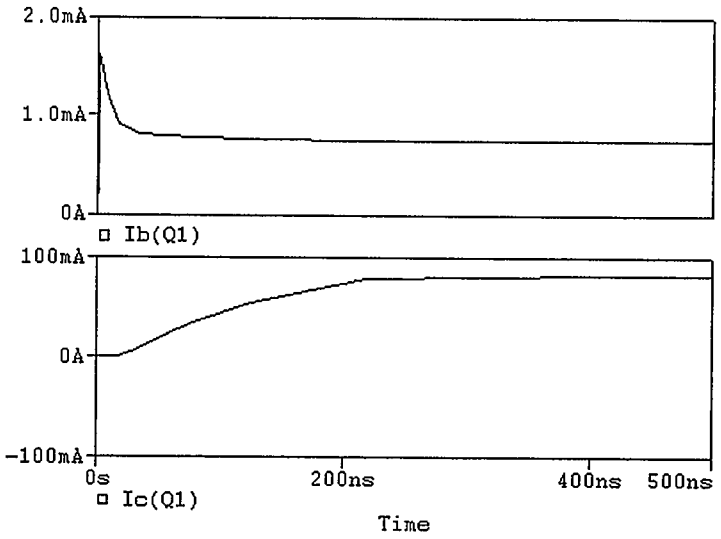


Fig. 5.3 2N4401 Base (Ib) and Collector (Ic) currents at turn-on

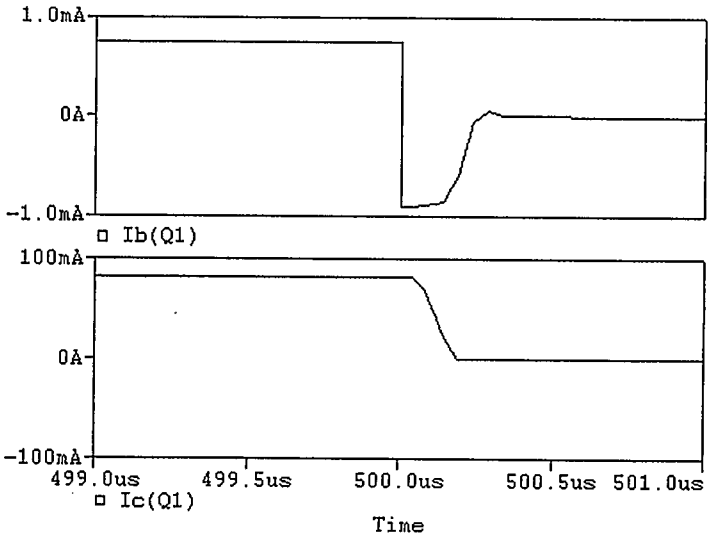


Fig. 5.4 2N4401 Base (Ib) and Collector (Ic) currents at turn-off

[9] In this calculation we use 12MHz corresponding to the maximum external clock source used in the experimental set-up.

5.2.2 Snubber Circuits

Snubber circuits minimize the over-current and over-voltage transient taking place during switching which reduces power loss in the switches. We choose to use the snubber circuit shown in Fig. 5.5 and described in [2]. In this circuit the purpose of L is to limit di/dt, where i is the transistor's collector current, while the capacitor C has the purpose of limiting dv/dt, with v is the transistor's collector to emitter voltage. The purpose of the resistor R is to limit the capacitor discharge current through the transistor when it is turned on, and the purpose of the diode Dc is to permit the capacitor C charging current to circumvent the resistor R when the transistor is turning off. On the other hand, the role of the resistor r is to provide an alternative path for the inductor current when the transistor turns off, while diode D_L is to keep the resistor r from conducting during turn on times of the transistor.

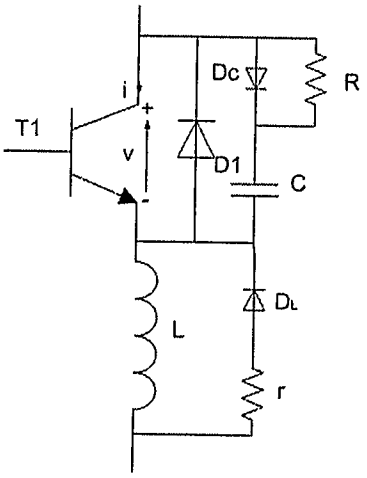


Fig. 5.5 A bipolar snubber circuit.

We used the charts provided in [2] in conjunction with the approximations in [1] to calculate the values of r, R, C and L, our results are shown in Table 5.2.

Table 5.2 Snubber parameters.

L	C	R	r
40uH	66nF	30Ω	2.5Ω

5.2.3 One Leg H-bridge Experimental Circuit

The PWM gating signals were generated using the Microchip Technology's PIC 16F877 microcontroller.

Fig. 5.6 shows one leg of the H-bridge used in our experimental set-up (the other leg is exactly the same); the galvanic isolation between the low power side (the microcontroller side) and the high power side (the H-bridges side) is depicted by different ground symbols in Fig. 5.6; Fairchild Semiconductor's 4N32 general purpose 6-pin photo Darlington opto-couplers are used to separate the two sides. V1, in Fig. 5.6, is one of the three power supplies we used when we operate three inverters in parallel; and diodes 1N4148 are the freewheeling diodes while the snubber circuits are not shown here for simplicity. Points A and A' are fed from the digital outputs of the microcontroller (PIC 16F877).

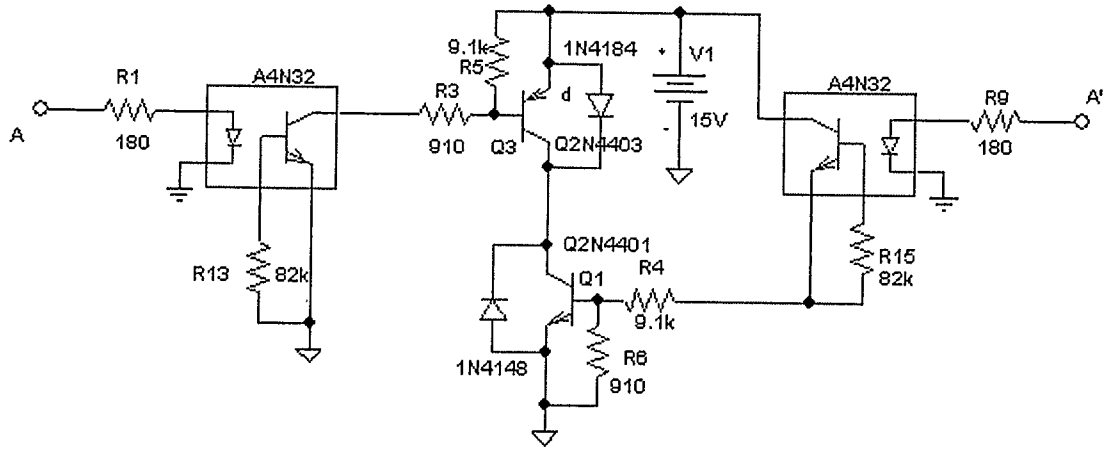


Fig. 5.6 One leg of the H-bridges used in the experimental set-up.

Finally, the synchronization unit in Fig. 5.1 consists of an external clock source (Agilent 33120A, operated at 4, 8, or 12MHz corresponding to a modulation index M = 0.3, 0.6, or 0.9 respectively) driving the OSC1/CLKIN pin of every PIC in the design (we used three PICs in our design, each one generating the necessary gating signals for one H-bridge), and a master reset connected to the MCLR pin of every PIC as depicted in Fig.5.7.

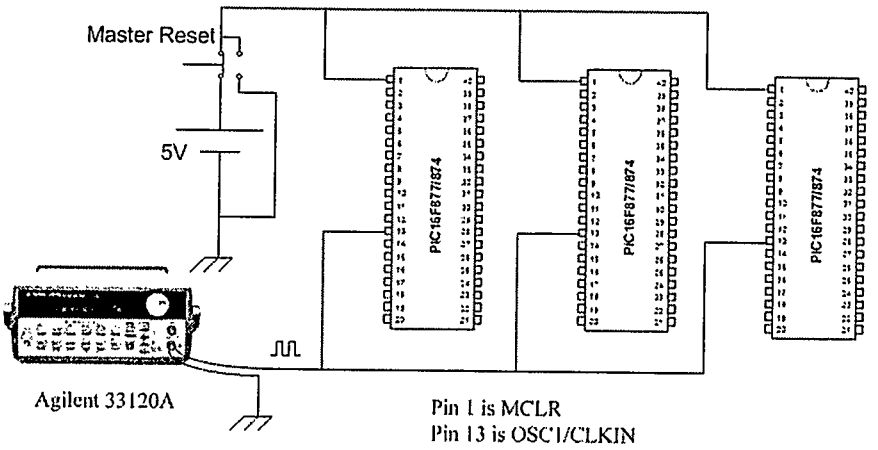


Fig. 5.7 Synchronization unit (see text for description).

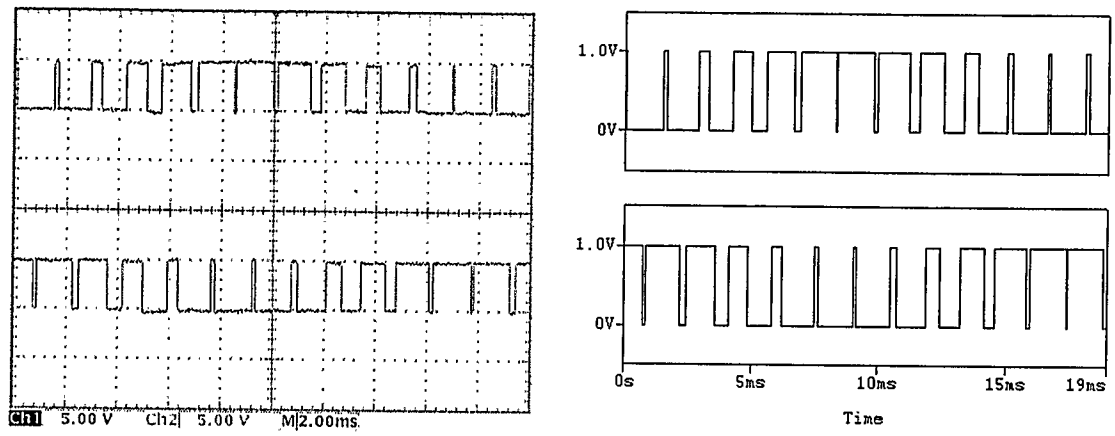
5.3 Sample Experimental Results

Fig. 5.8 provides some idea of the quality the PWM signals are generated at the output of the microcontroller. Fig. 5.8 (a) (left waveform) shows the two signals that go to the top two transistors of the inverter's H-bridge, on the right we see this signal as generated by simulation.

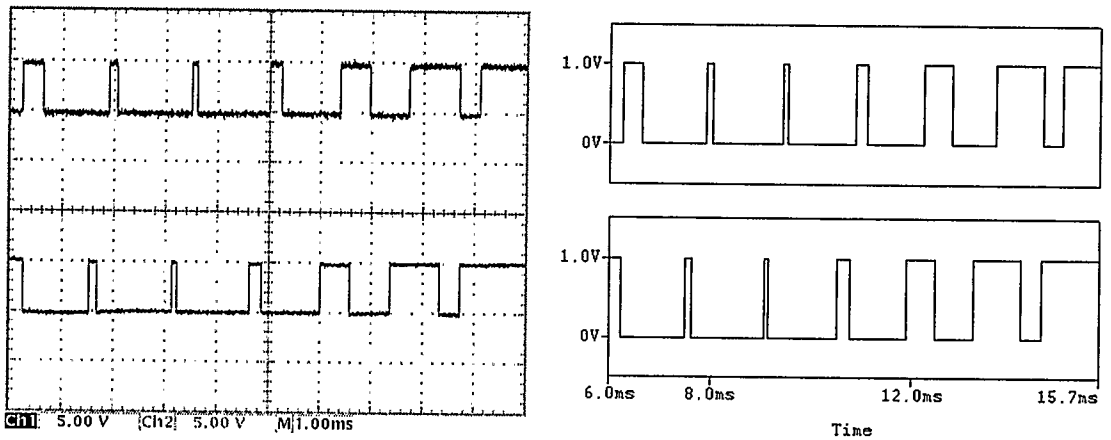
Fig. 5.8 (b) (left waveform) shows the two signals that go to the top left transistors of two different inverter's H-bridge; we can see here clearly the delay between inverters. Fig. 5.8 (b) (right waveform) shows this signal as generated by simulation. Fig. 5.8 (c) (left waveform) shows the unfiltered output signal of one H-bridge, while the right picture shows this signal as generated by simulation.

All the signals shown in Fig. 5.8 correspond to a modulation index M = 0.9 and carrier to sine reference frequency ratio fc/fs = 11.

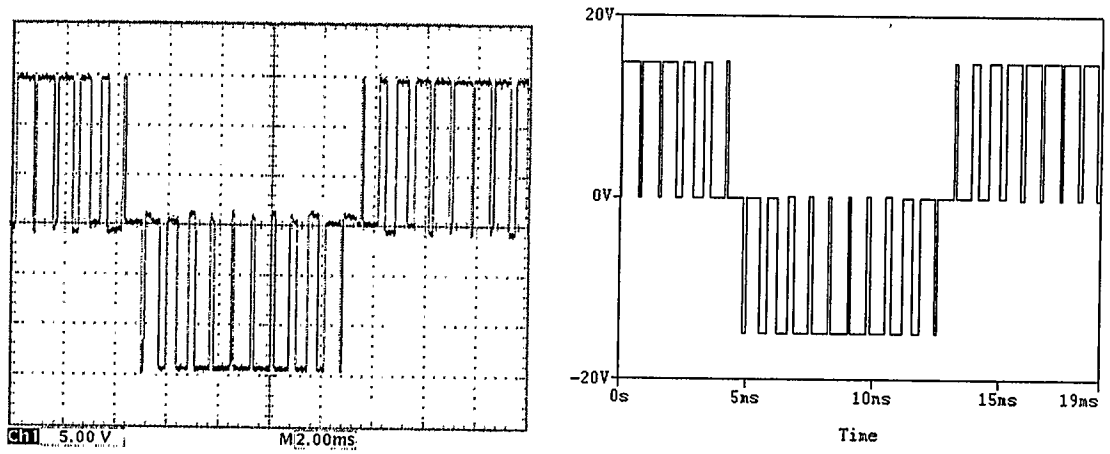
Figs. 5.9 through 5.17 show the experimental output voltage waveform, taken between the load's resistor leads, and its harmonic spectrum for the cases of a single, two and three synchronized and optimally phase-shifted parallel operated inverters modulated by double edge asymmetrical RSPWM with different modulation indices M and carrier to reference frequency ratios fc/fs. Table 5.3 gives the corresponding THD for all the cases presented in Fig. 5.9 through Fig. 5.17.



(a)



(b)



(c)

Fig. 5.8 PWM signals generated using the PIC 15F877 (see text for description.)

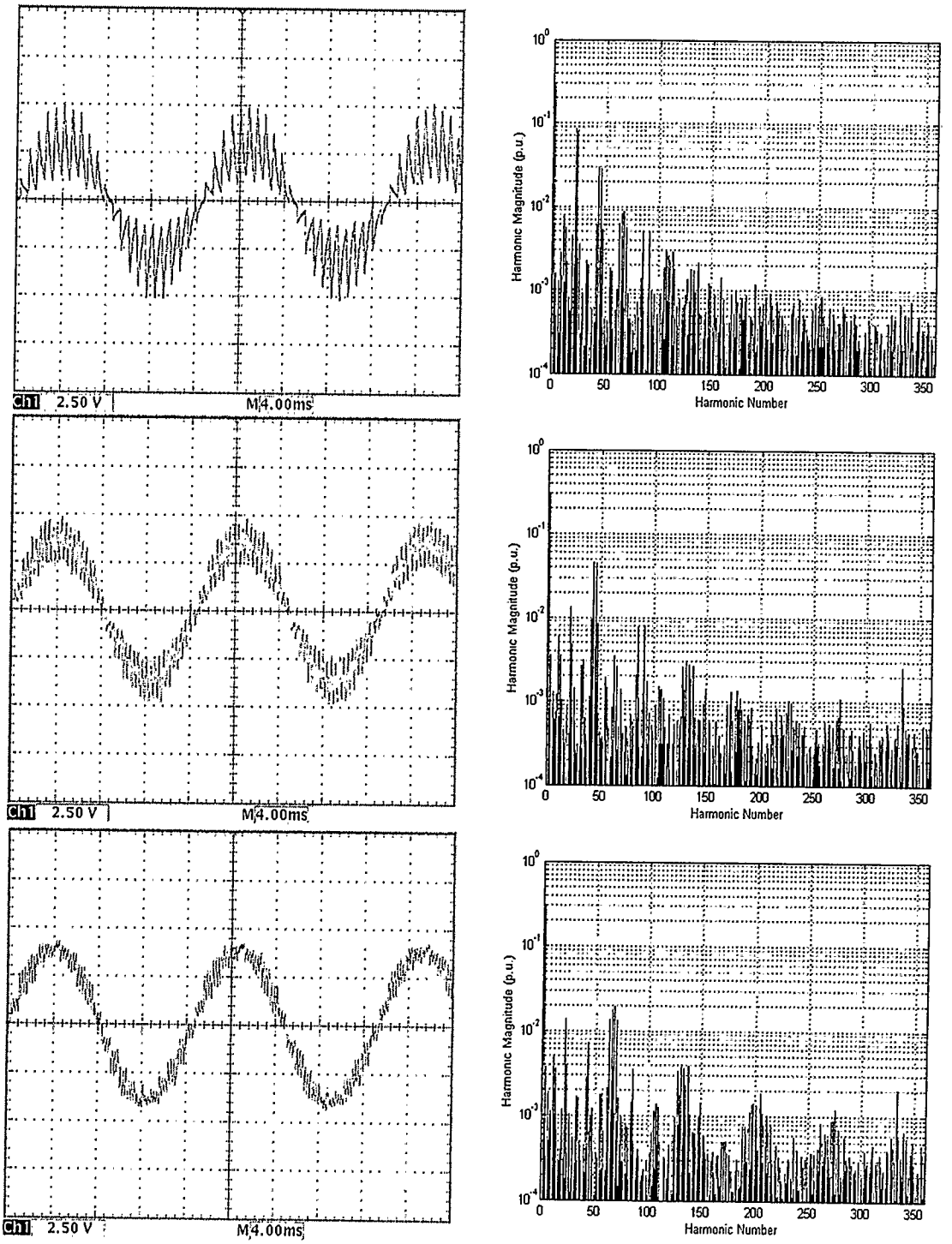


Fig. 5.9 Experimental output voltage waveform and its harmonic spectrum for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.3, fc/fs = 11

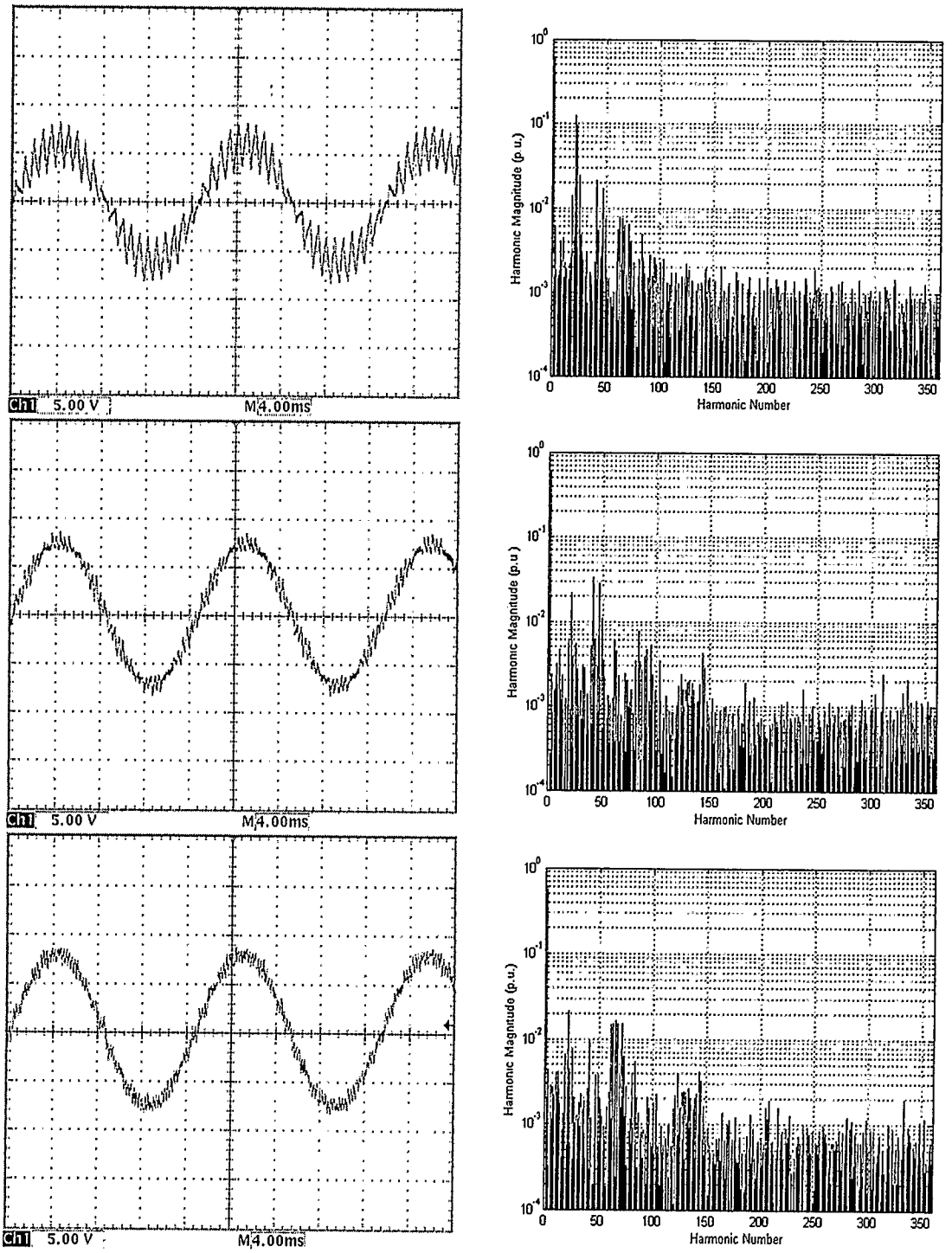


Fig. 5.10 Experimental output voltage waveform and its harmonic spectrum for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.6, fc/fs = 11

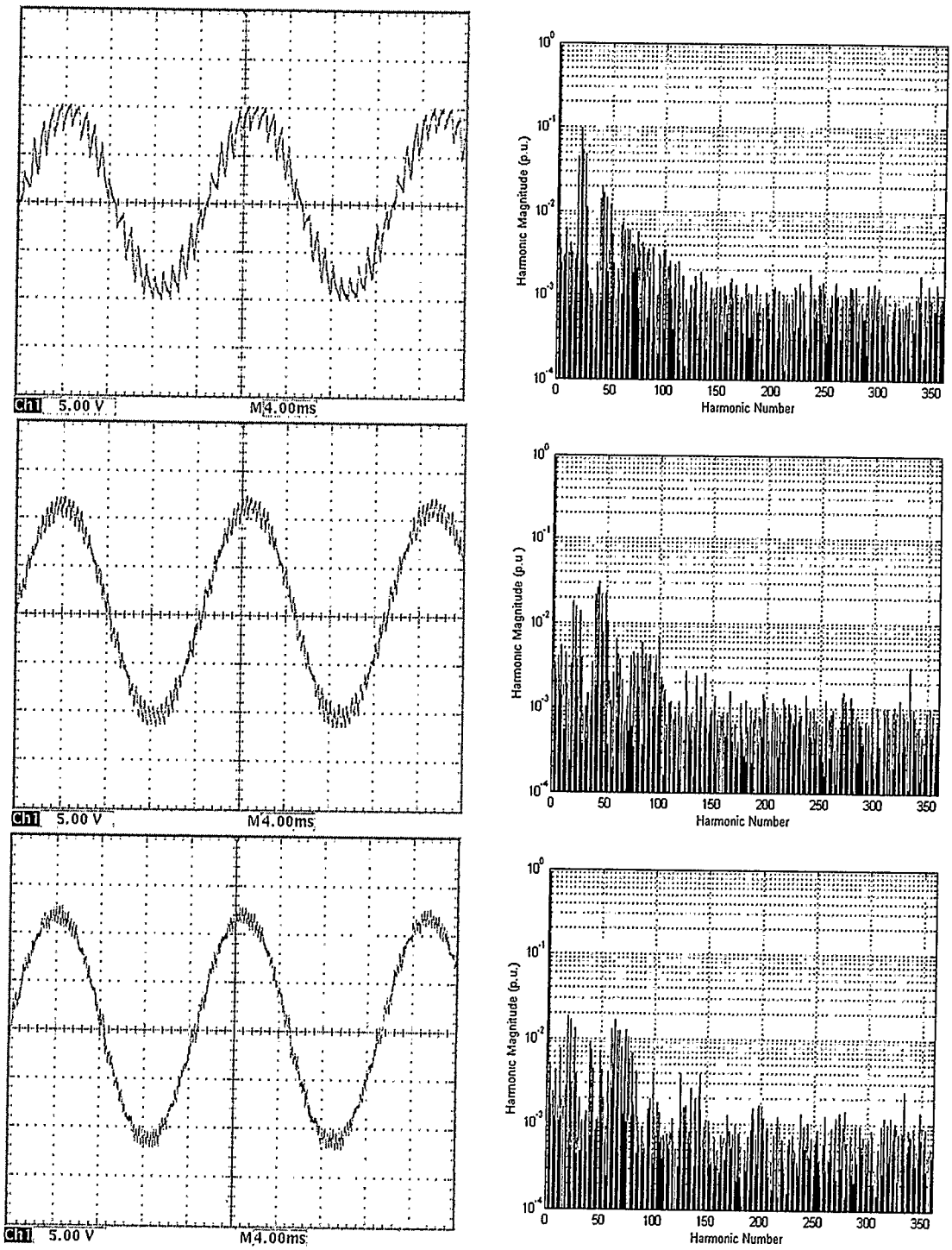


Fig. 5.11 Experimental output voltage waveform and its harmonic spectrum for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.9, fc/fs = 11

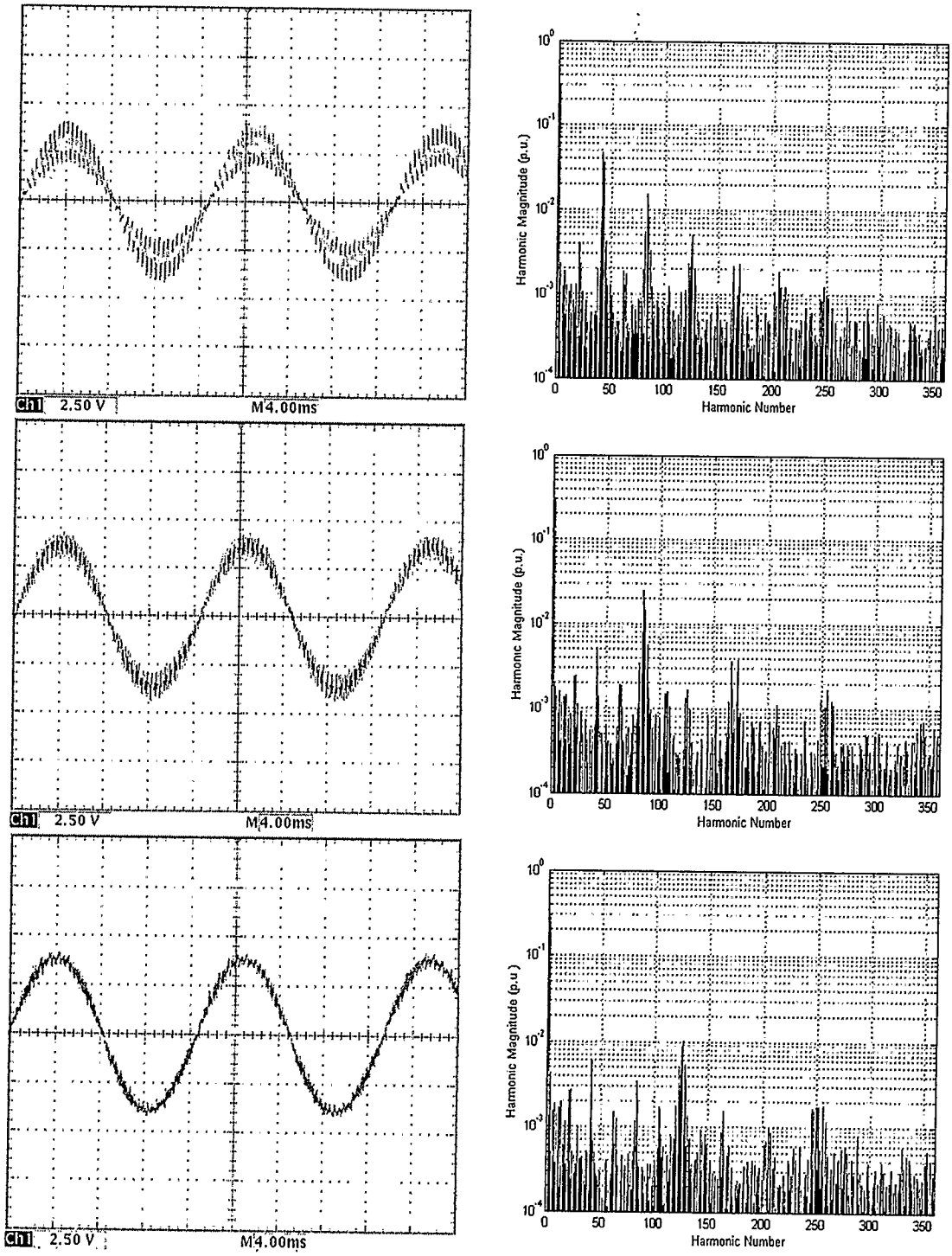


Fig. 5.12 Experimental output voltage waveform and its harmonic spectrum for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.3, fc/fs = 21

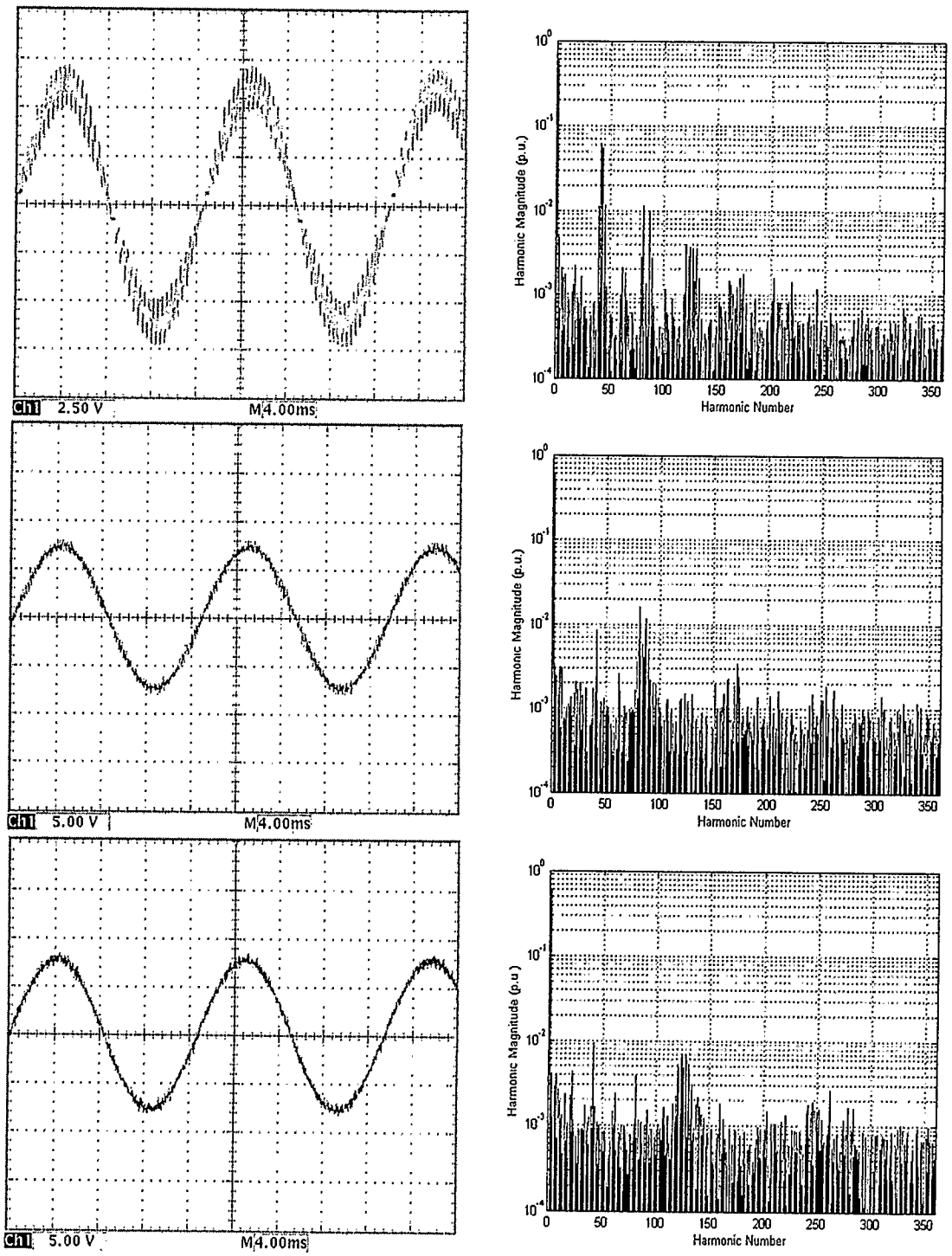


Fig. 5.13 Experimental output voltage waveform and its harmonic spectrum for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.6, fc/fs = 21

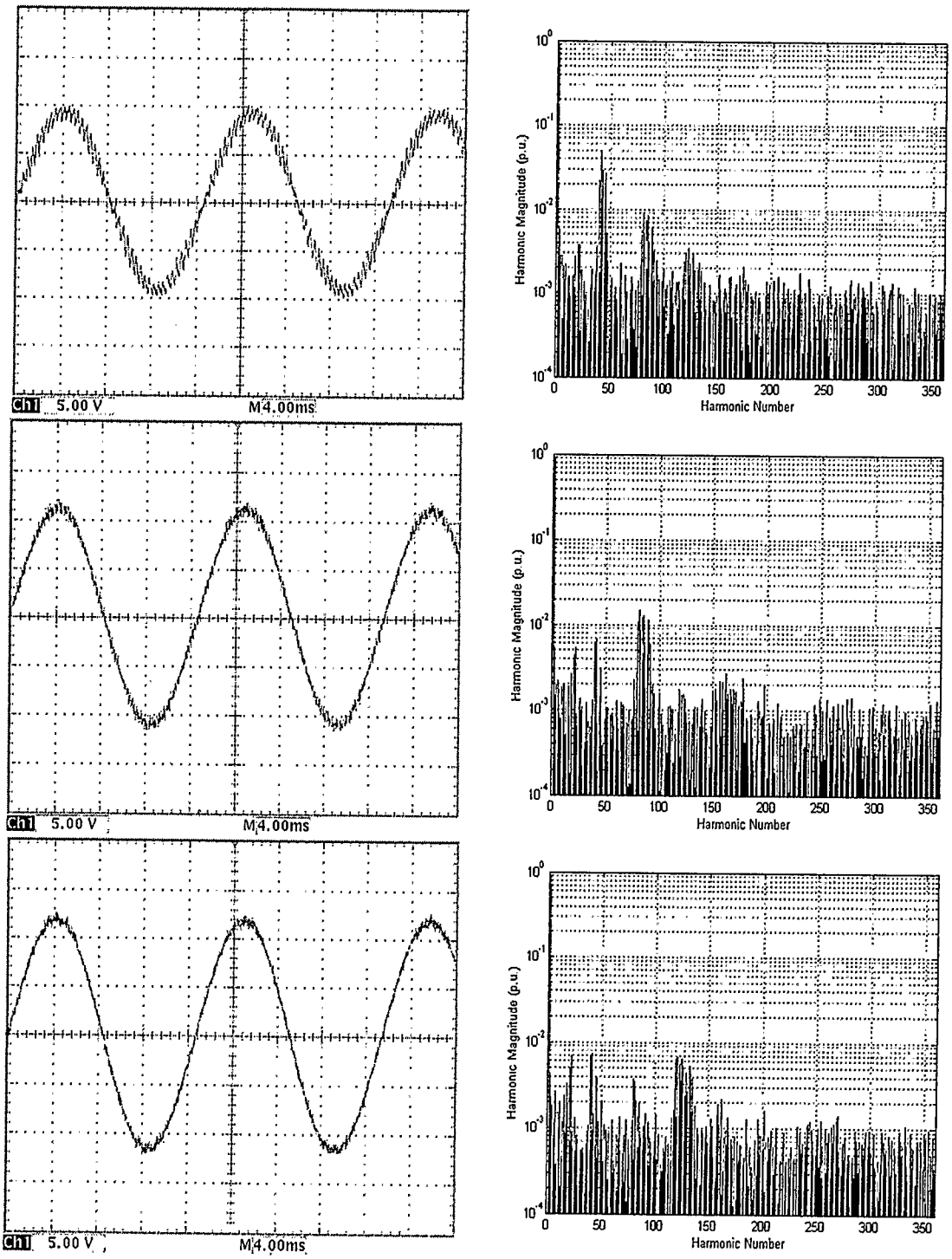


Fig. 5.14 Experimental output voltage waveform and its harmonic spectrum for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.9, fc/fs = 21

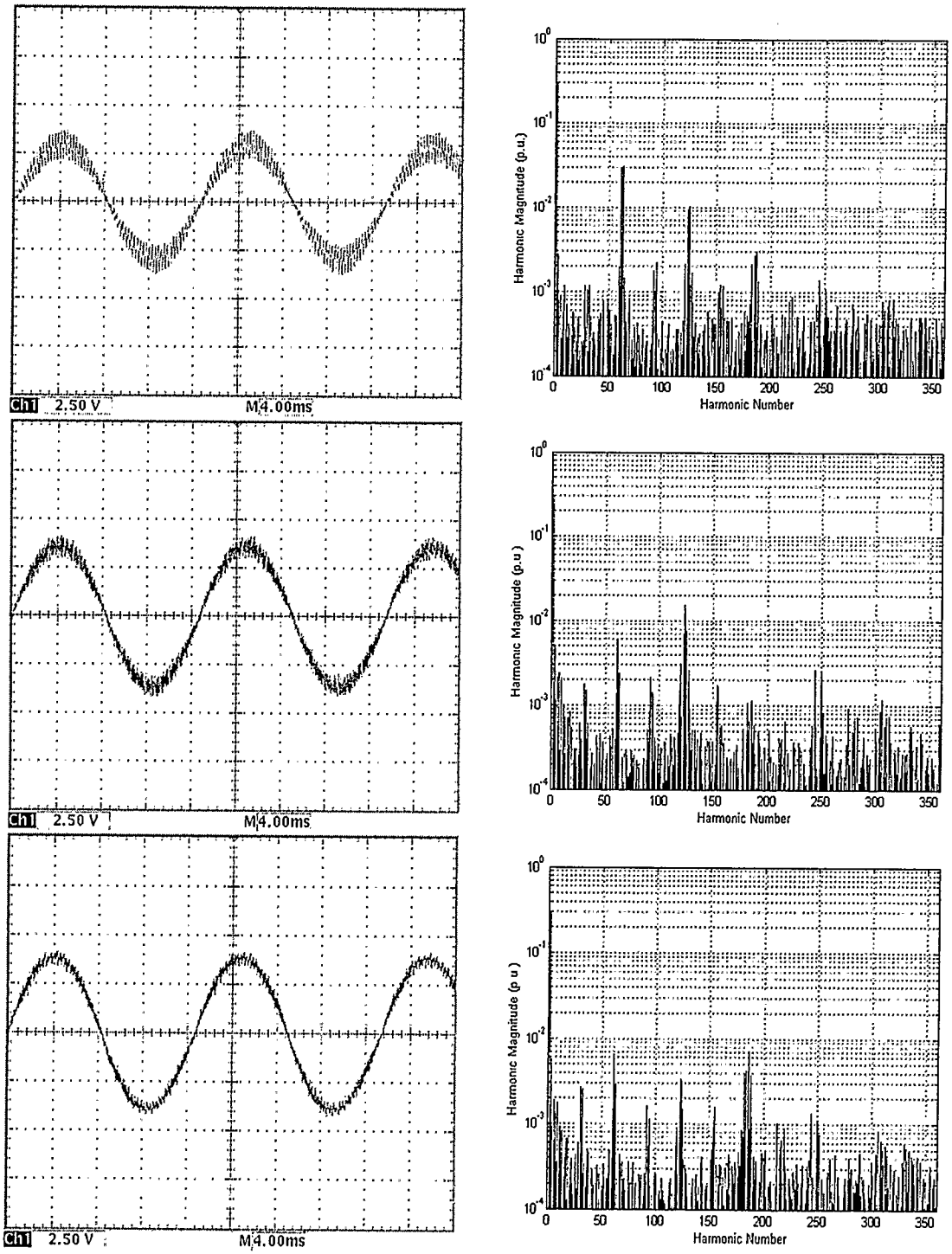


Fig. 5.15 Experimental output voltage waveform and its harmonic spectrum for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.3, fc/fs = 31

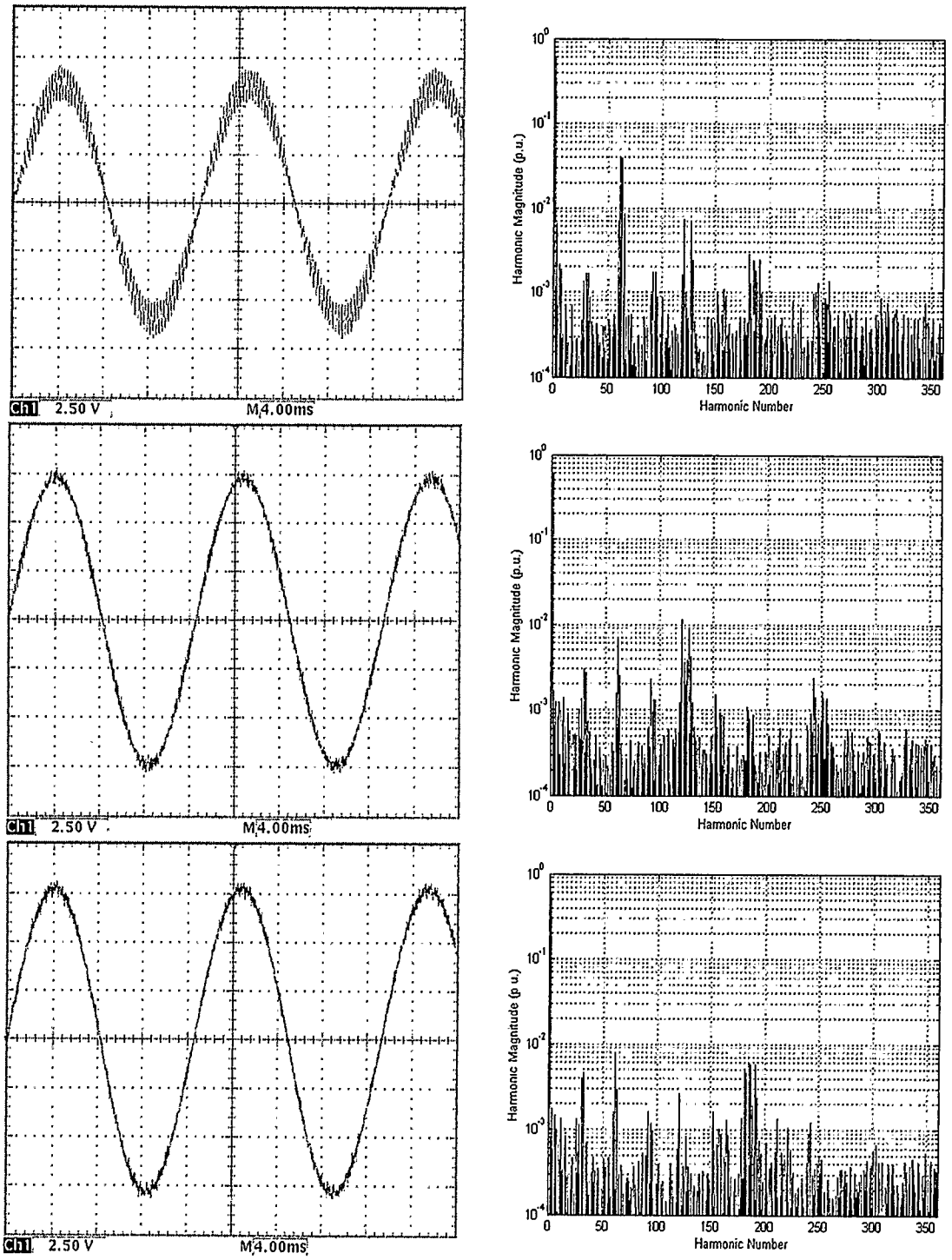


Fig. 5.16 Experimental output voltage waveform and its harmonic spectrum for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.6, fc/fs = 31

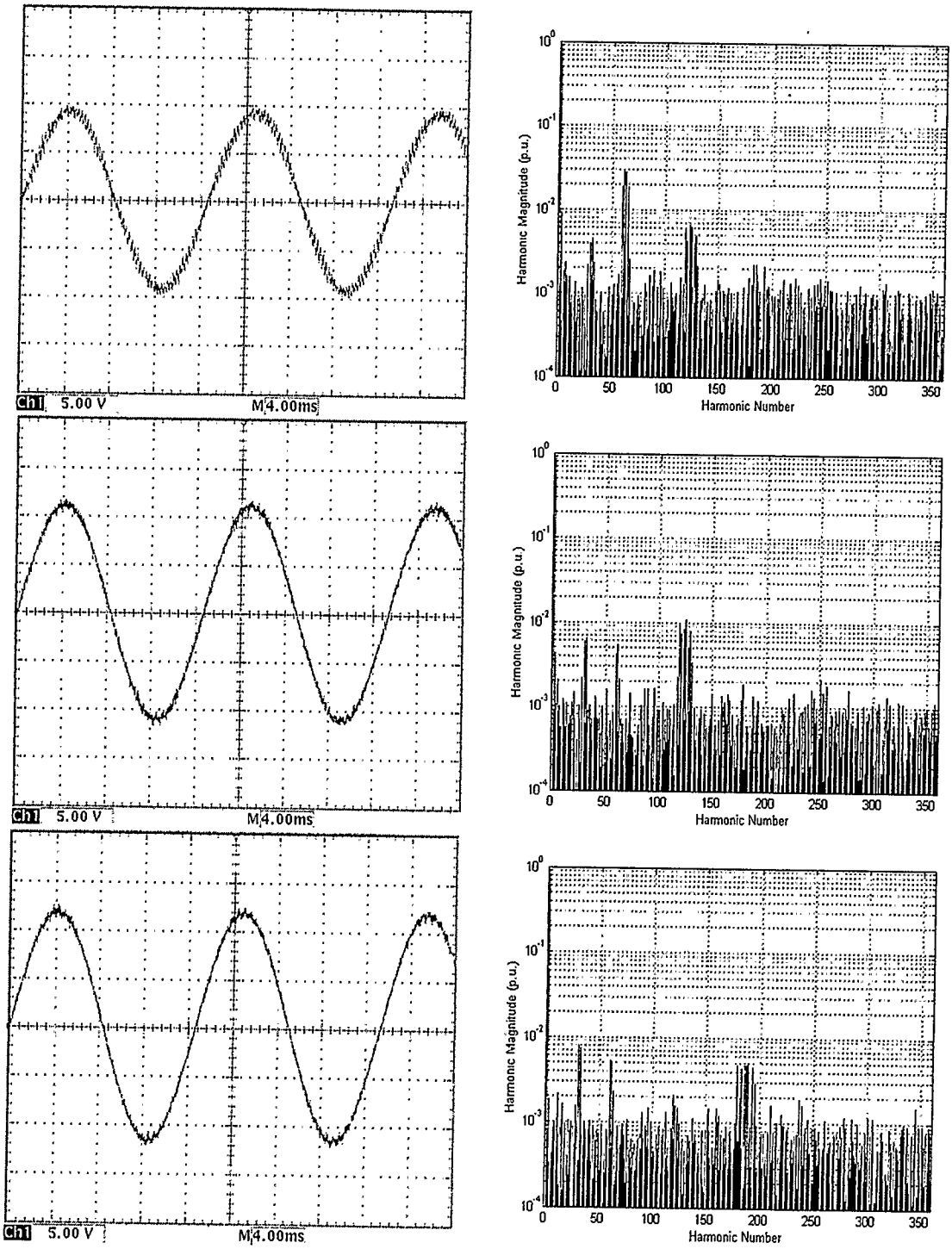


Fig. 5.17 Experimental output voltage waveform and its harmonic spectrum for single, two and three parallel inverters modulated by double edge RSPWM with M = 0.9, fc/fs = 31

5.4 Discussion of the Experimental Results

Comparing the experimental output waveforms and their spectra depicted in Figs. 5.9 through 5.17 with the simulated waveforms depicted in Figs. 4.18 through 4.26 in the previous chapter reveals the following:

- There is a very good agreement between the experimental waveform and their corresponding simulated counterparts.
- As expected, the spectra of the experimental waveforms contain more harmonics components compared to their simulated counterparts, but none of them appears in the first or the second decade of the semi-log scale, and only a portion of them are in the third decade (in the range of 1/100 th to 1/1000 th of the fundamental) indeed most of them rest in the fourth decade in the semi-log scale (below 1/1000th of the fundamental). It is interesting to note here that the experimental peak harmonics do indeed appear at the same frequency placement as their counterparts in the simulation (a sign that the experimental PWM signals generated with the microcontroller match quite well with their simulated counterparts).
- The accumulated weight of all the experimental harmonic components (ie, there are simply more harmonics present experimentally) shows up as higher THD values in Table 5.3 if compared to the theoretical THD values of the same cases given in Chapter 3 and repeated in Table 5.4 for convenience. Despite that, the agreement between our experimental and our theory is very good.
- A slight increase in the fundamental amplitude as we go from one inverter to two inverters operated in parallel is seen in Figs. 5.9 through Fig. 5.17, a phenomenon we did not see in simulation. This also happens when we go from two inverters operated in parallel to three inverters operated in parallel. This is due, probably, to the equivalent output impedance of the bipolar transistors being divided by two in the case of two parallel inverters and by three in the case of three inverters operated in parallel, in the exact same way as described in paragraph 2.5.2 in Chapter 2.

Table 5.3 Experimental THD values corresponding to the cases depicted in Fig. 5.9 through Fig. 5.17

	One Inverter	Two Inverters	Three Inverters
P = 11, M= 0.3	41.5558%	23.2230%	13.2957%
P = 11, M= 0.6	27.4110%	9.7812%	8.4296%
P = 11, M= 0.9	15.4128%	7.7982%	6.0306%
P = 21, M= 0.3	22.6549%	12.5801%	7.3638%
P = 21, M= 0.6	14.5453%	5.7300%	5.0580%
P = 21, M= 0.9	8.4899%	4.4519%	3.4944%
P = 31, M= 0.3	15.6351%	9.1065%	6.2062%
P = 31, M= 0.6	10.0966%	3.6178%	3.2083%
P = 31, M= 0.9	6.2281%	3.4735%	2.8869%

Table 5.4 Theoretical THD values corresponding to the cases depicted in Fig. 4.18 through Fig. 4.26

	One Inverter	Two Inverters	Three Inverters
P=11, M=0.3	29.5375%	19.7884%	11.6609%
P=11, M=0.6	19.8779%	7.7361%	6.7005%
P=11, M=0.9	11.2963%	6.4391%	5.0148%
P=21, M=0.3	15.6654%	10.3915%	5.9346%
P=21, M=0.6	10.5218%	3.9503%	3.2709%
P=21, M=0.9	5.9383%	3.2174%	2.3232%
P=31, M=0.3	10.6392%	7.0411%	3.9848%
P=31, M=0.6	7.1428%	2.6569%	2.1658%
P=31, M=0.9	4.0250%	2.1504%	1.5079%

Following are the reasons for the disagreement in the harmonic measures provided in Tables 5.3 and 5.4 (given in the order of importance, in the opinion of the author):

1. The bipolar technology: indeed bipolar transistors are not the best choice when it comes to approximating ideal switches, because their input impedance is low and their output impedance is high and, in most cases, both are biasing dependent as observed by the author. We used them here only because there were no readily available complementary MOSFETs in the Power Electronics Lab.

2. The microcontroller (PIC 16F877): this microcontroller has very basic PWM capabilities; this affects directly the width precision of our generated PWM pulses.
3. Earlier in the experimental design we found the impossibility of relying on crystals to drive the microcontroller's clock, indeed after only a couple of hours of operation of the parallel operated inverters, signs of de-synchronization start to appear, so we had to use an external clock source (the Agilent 33120A) to guarantee a total and a complete synchronization between inverters. The price paid for not using the very precise crystals is that our sine wave frequency will be as precise as the external clock used. In general we observed an output frequency approximately in the range of 59.90Hz to 60.10Hz.
4. There is non-linearity in the transistors and in the photo Darlington opto-couplers and to a lesser extend in the inductors.
5. There is tolerance in the discrete components used (resistors, capacitors...etc.).

5.5 Chapter Summary

In this chapter a general description of the experimental set-up is provided. This includes a listing of the available hardware at the Power Electronics Lab, followed by a general description and the schematics of the most important parts of the actual experimental design. Also, the synchronization unit is discussed.

We also present in this chapter experimental results consisting of the output voltage waveforms across the resistor load terminals with their associated spectra for the cases of one inverter, two synchronized optimally phase shifted inverters operated in parallel and three synchronized optimally phase shifted inverters operated in parallel, all modulated by double-edge asymmetrical RSPWM. We present those results for various modulation indices M and carrier to sine reference frequency ratios fc/fs combinations. The THD associated with every case is given, and compared with the THD obtained in simulation, and as expected, the experimental cases have slightly higher harmonic components than in the corresponding simulation cases; however the agreement is generally very good.

Chapter Six: CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this thesis we present a thorough and comprehensive analyses for the cases of two and three synchronized phase-shifted parallel pulse width modulated (PWM) inverters with current-sharing reactors, in addition to our analysis for the reference case of one inverter operation. This is done for a wide range of operating conditions.

In Chapter 3 we presented analytical treatment of the subject using the double Fourier series, this includes in-depth treatment of double-edge asymmetrical regularly sampled pulse width modulation and double-edge naturally sampled pulse width modulation methods followed by their extension to the operation of N synchronized and phase-shifted inverters operated in parallel. Following this we presented in Chapter 4 computer simulations using PSpice and MATLAB/Simulink. The optimum phase shift is hence determined that results in a considerable reduction in all distortion figures of merit defined in Chapter 1, namely, WTHD0, WTHD and THD. Our study then turns to a laboratory experimental investigation in Chapter 5, using bipolar transistors, which validates our numerical results. Three figures of merit (WTHD0, WTHD and THD) were used throughout this thesis permitting the detailed evaluation of the results obtained, and allowing comparison of our work to a broad range of related researches. The results obtained show that, indeed, the proposed technique is a potential candidate for the power electronics interface of renewable energy systems to the utility grid.

The thesis contributions are:

1. We quantify the merits of paralleling two and three synchronized phase-shifted parallel pulse width modulated inverters, and show that indeed there is a substantial distortion reduction, which in this thesis is measured in terms of three figures of merit, namely, WTHD0, WTHD and THD.
2. We show that the optimum phase-shift delay, yielding the minimum figures of merit WTHD0, WTHD and THD as defined in Chapter 1, occurs if the gating

signals of successive inverters are shifted by exactly Tc/2N for the operation of synchronized phase-shifted parallel pulse width modulated (PWM) inverters, as verified for N = 2 and N = 3, where Tc denotes the triangular carrier period and N is the number of inverters in parallel.

3. This thesis places, for the first time as far as the author is aware, parallel operation of voltage source inverters in the context of multilevel inverters. Indeed the similarity between the unfiltered outputs of multistage inverters, diode-clamped inverters and flying-capacitors inverters on the one hand and the unfiltered output of the parallel inverters scheme proposed in this thesis on the other hand is apparent, as seen in Chapter 2. Thus we decided to use multilevel inverters as a backdrop in which to discuss the parallel operation of voltage source inverters. By unifying the areas of research for parallel operated and multilevel inverters, we hope to stimulate more research interest in parallel inverters and look forward to seeing the parallel scheme employed more in the near future.
4. Our analytical analysis using the double Fourier series, presented in chapter 3, and our investigation of the spectral resultant from paralleling two and three synchronized phase-shifted inverters revealed the complex nature of the paralleling operation; giving us an in-depth understanding of the inner operation of this inverter scheme. In fact the divergence of the opportunities of harmonic reduction using paralleling inverters operation from the traditional harmonic reduction schemes (ie, filtering type) is made known only by the work presented in this thesis.
5. Our thorough analysis of the two modulation techniques used in this thesis reveals that, contrary to the generally accepted wisdom, double-edge naturally sampled PWM and double-edge asymmetrical regularly sampled PWM are not quite similar. Indeed, as we see in Chapter 3, with two and three inverters in parallel and for a modulation index M greater than about 4.5, WTHD0 and WTHD are always considerably higher in the case of double edge asymmetrical RSPWM as compared to double edge NSPWM. This result may have a huge impact on some applications, such as motor control, where low harmonics are a major concern.

6. The parallel inverter equivalent circuit, presented in Chapter 2, in conjunction with eqn. (3.5) and eqn. (3.10) is a novel modeling technique permitting any number of inverters operated in parallel (ie, any value of N) to be analyzed with accuracy, simplicity and ease (as is verified with MATLAB/Simulink results presented in this thesis and validated by PSpice).
7. Many simulation waveform samples, validated by experimental waveforms, are provided in Chapter 4. This is a precious resource of available data to help practicing designers minimize time-to-market for their parallel inverter products.
8. One practical implementation of two and three synchronized phase-shifted parallel pulse width modulated inverters is presented in Chapter 5. It took the author quite some time experimenting with different implementation schemes to evaluate the advantages and disadvantages of each scheme. The implementation scheme provided in Chapter 5 is, in the opinion of the author, a precise, effective and very cost-competitive approach.

6.2 Suggested Future Work

The following research topics would be a valuable addition to the research work presented in this thesis:

- An in-depth comparison between parallel operated voltage source inverters and multilevel inverters.
- A thorough investigation of the impact of the excellent dynamic performance and inherent current limiting ability of the hysteresis current control on parallel operated voltage source inverters.
- An extension of the present work to multi-phase configurations.
- A high power experimental implementation using power MOSFET (metal oxide semiconductor field-effect transistor) or IGBT (insulated gate bipolar transistor) switching devices.
- Investigation of the impact of other modulation strategies on parallel inverter operation, for example, space vector modulation.

References

[1] J. G. Kassakian, M. F. Schlecht and G. C. Verghese, *Principles of Power Electronics*, Addison-Wesley Publishing Company, ISBN: 0-201-09689-7, 1991.

[2] G. Seguier and F. Labrique , *Power Electronic Converters: DC-AC Conversion*, ISBN-10: 3540549749 Springer-Verlag Berlin and Heidelberg GmbH & Co. K, 1993.

[3] N. Mohan, T. M. Undeland and William P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, John Wiley & Sons, INC., Publication, ISBN-10: 0471226939, 2002.

[4] B. M. Bird, K. G. King and D. A. G. Pedder, *An Introduction to Power Electronics*, 2nd edition, John Wiley & Sons Inc, ISBN-10: 0471926175, 1992.

[5] M. H. Rashid, *Power Electronics: Circuits, Devices and Applications*, 3rd edition, Prentice Hall Publisher, ISBN-10: 0131011405, 2003.

[6] D. G. Holmes, T. A. Lipo, *Pulse Width Modulation for Power Converters*, Wiley-IEEE Press Publication, ISBN: 0-471-20814-0, 2003.

[7] M. H. J. Bollen, *Understanding Power Quality Problems: Voltage Sags and Interruptions*, Wiley-IEEE Press, ISBN: 978-0-7803-4713-7, 1999.

[8] K. Alexander, M. T. Thompson, *Power Quality in Electrical Systems*, McGraw-Hill, ISBN: 0071470751, 2007.

[9] "IEEE recommended practice for monitoring electric power quality", IEEE Standard 1159, ISBN: 1-55937-549-3, 1995.

[10] "IEEE recommended practices and requirements for harmonic control in electrical power systems", IEEE Standard 519, ISBN: 1559372397, 1992.

[11] "Voltage characteristics of the electricity supplied by public distribution systems", European Standard EN 50160:2007, Blackwell Publisher, ISBN13: 9780580558412, 2007.

[12] M. Marinelli, P. Zanchetta, and A. Dell'Aquila, "A new performance factor for weighted harmonic distortion evaluation", *11th IEEE International Conference on Harmonics and Quality of Power*, Lake Placid, NY, pp.728 - 733, Sept. 2004.

[13] A. M. Kamel and T. H. Ortmeyer, "Harmonic reduction in single-phase inverter using a parallel operation technique", *IEEE Applied Power Electronics Conference*, Baltimore, MD, pp. 101-108, Mar. 1989.

[14] M., K. Murai, Y. Watanabe, M. Kaneko, M. and Ueda, F. "A pulse-width-modulated inverter with parallel connected transistors using current-sharing reactors", *IEEE Transactions on Power Electronics*, vol. 8, no. 2, pp. 186-191,1993.

[15] L. Matakas Jr., C. Burlacu, and E. Masada, "High power, high performance parallel connected multi-converters: analysis and control", International Symposium on Industrial Electronics, Athens, Greece, pp. 121-126, Jul. 1995.

[16] S. Fukuda and K. Matsushita, "A control method for parallel-connected multiple inverter systems", *IEE Power Electronics and Variable Speed Drive Conference*, Publication no. 456, pp. 175-180, Sept.1998.

[17] Y. Komatsuzaki, "Cross current control for parallel operating three-phase inverter", *IEEE Power Electronics Specialists Conference*, pp. 943-950, June1994.

[18] B. Shi, G. Venkataramanan, "Parallel operation of voltage source inverters with minimal inter-module reactors", *Industry Applications Conference*, vol. 1, pp. 156-162, Oct. 2004.

[19] G. R.Walker, "Modulation and control of multilevel converters", Ph.D. thesis, Univ. of Queensland, St. Lucia, Australia, 1999.

[20] M. Rashid (Editor-in-Chief), *Power Electronics Handbook*, Second Edition, Academic Press, ISBN-10: 0-12-088479-8, 2007.

[21] B. Wu, *High-power Converters and AC Drives*, Wiley-IEEE Press, ISBN-10: 0471731714, 2006.

[22] S.R. Bowes, S. Grewal, and D. Holliday, "Hysteresis band PWM", *IEEE Electronics Letters,* vol. 35, no. 20, pp.1683 – 1685, 1999.

[23] C. Gatlan, and L.Gatlan, "AC to DC PWM voltage source converter under hysteresis current control", *IEEE International Symposium on Industrial Electronics*, Guimaraes, Portugal, vol. 2, pp.469 - 473, Jul. 1997.

[24] D. G Holmes and B. P. McGrath, "Opportunities for harmonic cancellation with carrier-based PWM for two-level and multilevel cascaded inverters", *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp.574-582, 2001.

[25] R. K. Behera, T.V. Dixit and S. P. Das, "Analysis of experimental investigation of various carrier-based modulation schemes for three level neutral point clamped inverter-fed induction motor drive", *International Conference on Power Electronics, Drives and Energy Systems*, pp. 1-6, Dec. 2006.

[26] A. Nabe, I. Takahashi, and H. Akagi , "A new neutral-point clamped PWM inverter", *IEEE Transaction on Industrial Applications*, vol. IA-17, No. 5, pp.518-523, I981.

[27] X. Yuan and I. Barbi, "Fundamentals of a new diode clamping multilevel inverter", *IEEE Transactionon Power Electronics*, vol. 15, no. 4, pp. 711–718, 2000.

[28] L. Xu and V. G. Agelidis, "Flying capacitor multilevel PWM converter based UPFC", *IEE Proceedings on Electric Power Applications*, vol. 149, no. 4, pp. 304-310, 2002.

[29] M. F. Escalante, J.C. Vannier, A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4 pp. 809-815, 2002.

[30] A. Tuladhar, H. Jin, T. Unger, K. Mauch, "Control of parallel inverters in distributed AC power systems with consideration of line impedance effect", *IEEE Transactions on Industry Applications*, vol. 36, no. 1, pp.131 – 138, 2000.

[31] A. Engler, "Control of parallel operating battery inverters", *Photovoltaic Hybrid Power Systems Conference*, Aix-en-Provenence, Jan./Feb. 2000.

[32] C. S. Lee, *et al,* "Parallel UPS with an instantaneous current sharing control", *IEEE Industrial Electronics Annual Conference*, vol. 1, pp. 568-573, Aug./Sep. 1998.

[33] S. J. Chiang, C. M. Liaw, W. C. Chang, and W. Y. Chang, "Multi-module parallel small battery energy storage system", *IEEE Transactions on Energy Conversion*, vol. 11, No. 1, pp. 146-154, 1996.

[34] T. Kawabata, and S. Higashino, "Parallel operation of voltage source inverters", *IEEE Transactions on Industry Applications*, vol. 24, no. 2, pp. 281-287, 1988.

[35] C. Liangliang, X. Lan, and Y. Yangguang, "A novel parallel inverter system based on coupled inductors", *The 25th International Telecommunications Energy Conference*, pp.46 – 50, Oct. 2003.

[36] M. Armstrong, D.J. Atkinson, C.M. Johnson and T.D. Abeyasekera, "Low order harmonic cancellation in a grid connected multiple inverter system via current control parameter randomization", *IEEE Transactions on Power Electronics*, vol. 20, no. 4, pp. 885- 892, 2005.

[37] P. Sernia and G.R. Walker, "Harmonic quality of multilevel cascade inverters with random carrier phase pulse width modulation", *Australasian Universities Power Engineering Conference (AUPEC 2004)*, Brisbane, Australia, 2004.

[38] N. L. Hinov, G. V. Kraev, B. N. Gilev and D. I. Vakovsky, "Parallel inverter analysis using mathematical software", Technical University, Sofia, Bulgaria, *Elec. Energ.* vol. 19, no. 1, pp. 99-107, 2006.

[39] J. K. Ji and S. K. Sul, "Operation analysis and new current control of parallel connected dual converter system without inter-phase reactors", *IEEE Industrial Electronics Annual Conference*, San Jose, CA, pp. 235-240, Nov./Dec.1999.

[40] H. Bierk, "Characterization of distortion reduction for single-phase multiple inverter operation", M.Sc. thesis, University of Calgary, December 2006

[41] J. Holtz, "Pulsewidth modulation – a survey", *IEEE Transactions on Industrial Electronics*, vol. 39, no. 5, pp. 410-420, 1994.

[42] M.A. Boost and P.D. Ziogas, "State-of-the-art carrier PWM techniques: a critical evaluation", *IEEE Transactions on Industry Applications*, vol. 24, no.2, pp.271–280, 1988.

[43] P. N. Enjeti, P.D. Ziogas, and J.F. Lindsay, "Programmed PWM techniques to eliminate harmonics: a critical evaluation", *IEEE Transactions on Industry Applications*, vol. 26, No. 2, pp. 302-316, 1990.

[44] W. R. Bennett, "New results in the calculation of modulation products", *Bell Systems Technical Journal*, pp. 228-243, 1933.

[45] H. S. Black, *Modulation Theory*, Van Nostrand Co., Out of print, 1953.

[46] S. R. Bowes, B. M. Bird, "Novel approach to the analysis and synthesis of modulation processes in power converters", *IEE Proceedings*, vol. 122, no. 5, pp. 507-513, 1975.

[47] P. Wood, *Switching Power Converters*, Van Nostrand Reinhold, ISBN-10: 0442243332, 1981

[47] M. H. Rashid, H. M. Rashid, *SPICE for power electronics and electric power*, Second Edition, CRC Press, ISBN-10: 0849334187, 2005.

[48] R. Shaffer, *Fundamentals of power electronics with Matlab*, Cengage Learning Publisher, ISBN-10: 1584508523, 2006.

[49] L. Nagel, "SPICE2: A Computer Program to Simulate Semiconductor Circuits", Ph.D. thesis, University of California, May 1975

[50] T. L. Skvarenina (Editor), *The Power electronics handbook (industrial electronics)*, CRC Press, ISBN-10: 0849373360, 2001.

[51] C. M. Wu, W.H. Lau, H. Chung, "Analytical technique for calculation of output harmonics in h-bridge inverter output with dead time", *IEEE Transactions on Circuits and Systems,* Part I, vol. 46, no. 5, pp. 617-627, 1999.

[52] Z. Ye, D. Boroyevich, and F. C. Lee, "Modeling and control of zero-sequence current in parallel multi-phase converters", *IEEE Power Electronics Specialists Conference*, vol. 2, pp. 680 - 685 June 2000.

APPENDIX A: SPECTRAL ANALYSIS OF PULSE WIDTH MODULATION

A.1. Method of Analysis

The following analytical method of determining the spectrum of a PWM signal was originally developed by W. R. Bennett [44] and Black [45] for communication systems, and later adapted to power converter systems by Bowes and Bird [46]. A much more thorough treatment of carrier based modulation techniques is given in [6, 47].

Bennett represented the pulse width modulation (PWM) signal by the projection on the plane $F(\theta, \phi)$-θ of the intersection of a three-dimensional geometrical function $F(\theta, \phi)$ and a plane P including the origin and having a slope of ω_s / ω_c, as illustrated in Fig. A.1.

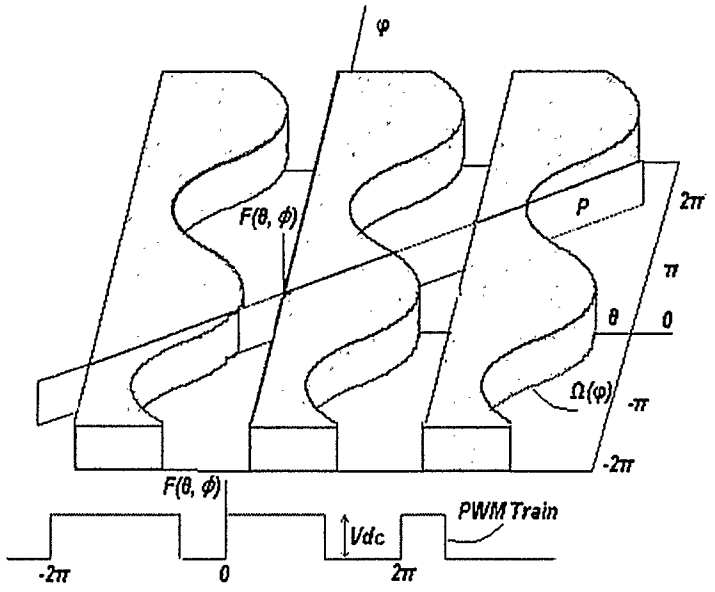


Fig. A.1 Bennett's 3D model

where θ and ϕ are defined as:

$$\theta = w_C t \tag{A.1}$$

and

$$\phi = w_S t \tag{A.2}$$

with w_S and w_C being the angular frequencies of the modulating (sine reference) and modulated (triangular carrier) signals respectively.

F(θ, ϕ) is defined so that it takes only one of two values, the supply voltage V_{dc} in the shaded area of Fig. A.1 and zero Volts outside it, with its shape, in the case illustrated, being flat on one side while the other side is defined by:

$$\Omega(\phi) = B + A\cos(\phi) \tag{A.3}$$

where A and B are constants that depend on the modulation method (see next section for an example). F(θ, ϕ) is hence cyclic along both the θ-axis and the ϕ -axis, with a period of 2π along each axis. The process can be represented in two dimensions as can be seen in Fig A.2.

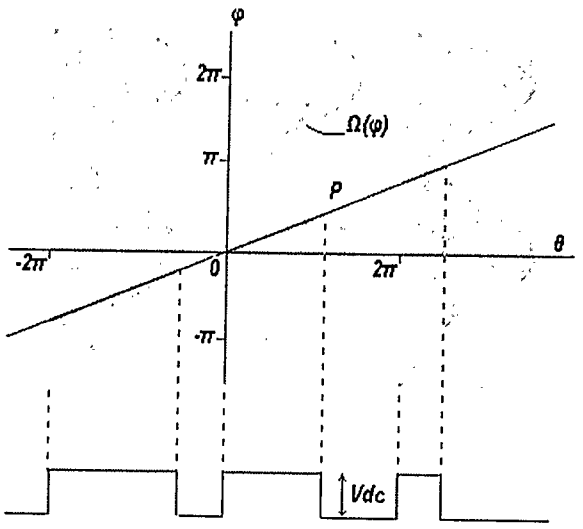


Fig. A.2 2D representation of Bennett's 3D model

Now if the $\theta 0 \phi$ plane (ie, the plane containing the θ-axis and ϕ -axis and the origin 0) in Fig. A.2 is sub-divided into square units with 2π long edges, the portions of $F(\theta, \phi)$ within the different squares are identical. This suggests that $F(\theta, \phi)$ can be expressed as a function of θ and ϕ by means of a double Fourier series, and our pulse width modulation signal train will be given by the Fourier series $F(\theta, \phi)$ with θ and ϕ replaced by (A.1) and (A.2) respectively.

The double Fourier series is defined as follow:

$$\begin{aligned} F(\theta,\phi) = \frac{1}{2}A_{00} &+ \sum_{n=1}^{\infty}[A_{0n}\cos(n\varphi) + B_{0n}\sin(n\varphi)] \\ &+ \sum_{m=1}^{\infty}[A_{m0}\cos(m\theta) + B_{m0}\sin(m\theta)] \\ &+ \sum_{n=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}[A_{mn}\cos(m\theta + n\varphi) + B_{mn}\sin(m\theta + n\varphi)] \end{aligned} \tag{A.4}$$

where

$$A_{mn} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} F(\theta,\phi)\cos(m\theta + n\phi)\, d\theta\, d\phi \tag{A.5}$$

and

$$B_{mn} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} F(\theta,\phi)\sin(m\theta + n\phi)\, d\theta\, d\phi \tag{A.6}$$

These coefficients can be re-written in complex form:

$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} F(\theta,\phi)e^{j(m\theta + n\phi)}\, d\theta\, d\phi \tag{A.7}$$

The method to determine the 3D shape in the above analysis is best illustrated by an example as illustrated in the next section.

A.2. Fourier analysis of double-edge naturally sampled PWM

This section describes the formulation of the 3-D model for generating a one phase leg PWM pulse train for the case of double-edge naturally sampled PWM using a triangular carrier. The basic configuration for such scheme is given in Figs. 3.1 and 3.2 in Chapter 3. The process of generating double-edge naturally sampled PWM for a half bridge, depicted in Fig. A.3, is repeated in Fig. A.4 for convenience. The time axis

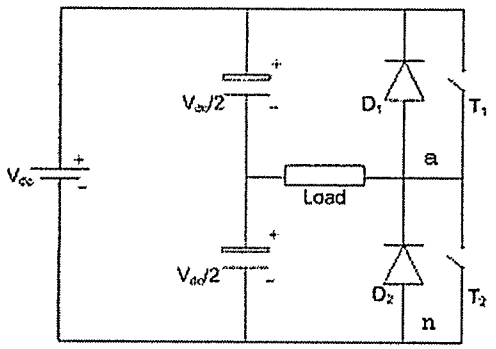


Fig. A.3 Half-bridge inverter

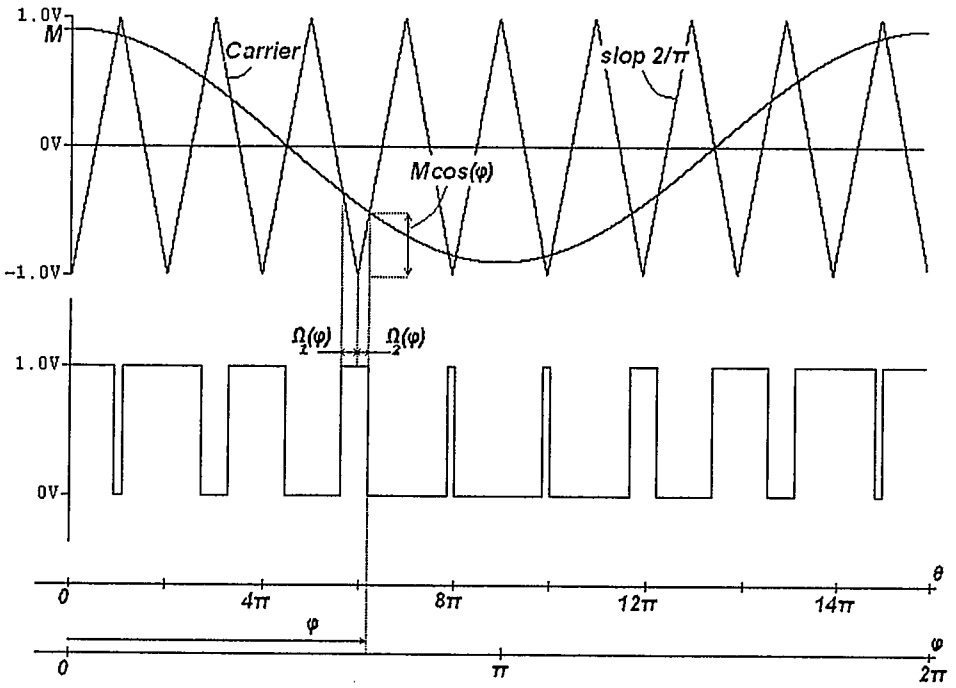


Fig. A.4 Double-edge naturally sampled PWM

is represented, in Fig. A.4, by two different angular abscissas $\theta = w_C t$ and $\phi = w_S t$, with w_S and w_C being the angular frequencies of the reference and carrier signals respectively.

The PWM pulse width $\Omega_1(\phi) + \Omega_2\phi)$ projected on the θ axis (see Fig. A.4) for a particular cycle of the carrier signal can be expressed as:

$$-1 + \frac{2}{\pi}\Omega_1(\phi) = M\cos(\phi) \tag{A.8}$$

and

$$-1 - \frac{2}{\pi}\Omega_2(\phi) = M\cos(\phi) \tag{A.9}$$

where M is the modulation index. Alternatively, (A.8) and (A.9) can be re-written as:

$$\Omega_1(\phi) = \frac{\pi}{2}(1 + M\cos(\phi)) \tag{A.10}$$

and

$$\Omega_2(\phi) = -\frac{\pi}{2}(1 + .M\cos(\phi)) \tag{A.11}$$

respectively. Hence the function F(θ, ϕ) can be defined, in one cell region, as

$$F(\theta,\phi) = \begin{cases} 0 & 0 \le \theta < \Omega_1(\phi) \\ V_{dc} & \Omega_1(\phi) \le \theta \le \Omega_2(\phi) \\ 0 & \Omega_2(\phi) < \theta \le 2\pi \end{cases} \tag{A.12}$$

A plot of the corresponding unit cell is given in the following figure, Fig. A.5

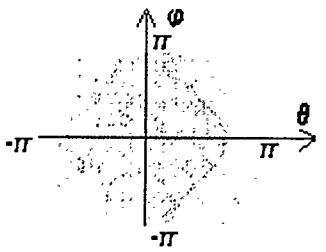


Fig. A.5 Unit cell for naturally sampled PWM with triangular carrier.

The one leg switched voltage $V_{an}(t)$ waveform(see Fig. A.3) is therefore the projection on the θ-axis of the intersection of $F(\theta, \phi)$ and the plane P as is illustrated in Fig. A.6.

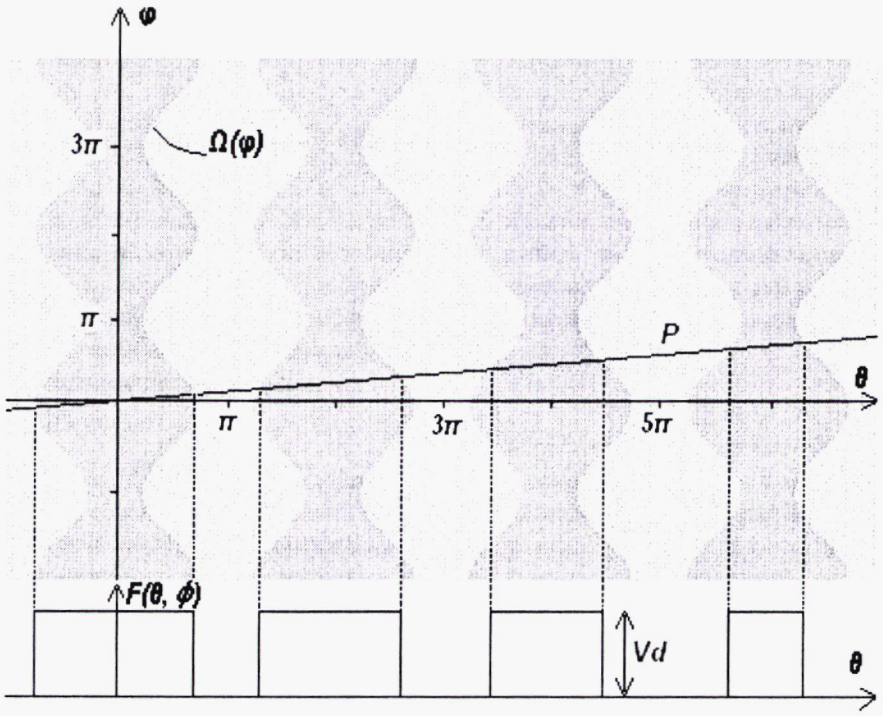


Fig. A.6 Bennett's process for half-bridge modulated using double-edge naturally sampled PWM, the upper graph shows the intersection of a 2D representation of Bennett's model and plan P, lower graph shows the resulting train of the PWM signal.

Using the unit cell, depicted in Fig. A.5, and the associated equations (A.10) to (A.12), the double Fourier series coefficients become:

$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{\frac{\pi}{2}(1+M\cos(\phi))}^{\frac{\pi}{2}(1+M\cos(\phi))} V_{dc} e^{j(m\theta + n\phi)} \, d\theta \, d\phi \qquad \text{(A.13)}$$

which now will be evaluated for various values of m and n as follow (the following derivation is based on the published work in [6]):

For m = n = 0 ⇒

$$C_{00} = A_{00} + jB_{00} = V_{dc}, \tag{A.14}$$

this gives, as expected, a dc value of Vdc/2.

For m=0, n>0 ⇒

$$C_{0n} = A_{0n} + jB_{0n} = \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \int_{\frac{\pi}{2}(1+M\cos(\phi))}^{\frac{\pi}{2}(1+M\cos(\phi))} e^{j(n\phi)}\, d\theta\, d\phi$$

$$= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \pi(1+M\cos(\phi)) e^{j(n\phi)}\, d\phi \tag{A.15}$$

$$= \frac{V_{dc}}{2\pi} \int_{-\pi}^{\pi} [e^{j(n\phi)} + \frac{M}{2}(e^{j(n+1)\phi} + e^{j(n+1)\phi})]\, d\phi$$

and because $\int_{-\pi}^{\pi} e^{j(n\phi)}\, d\phi = 0$ for n > 0, the above equation reduces to

$$C_{01} = A_{01} + jB_{01} = \frac{V_{dc}}{2\pi} \int_{-\pi}^{\pi} \frac{M}{2}\, d\phi = \frac{V_{dc}}{2} M \tag{A.16}$$

For m>0, n=0 ⇒

$$C_{m0} = A_{m0} + jB_{m0}$$

$$= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \int_{\frac{\pi}{2}(1+M\cos(\phi))}^{\frac{\pi}{2}(1+M\cos(\phi))} e^{j(m\theta)}\, d\theta\, d\phi \tag{A.17}$$

$$= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \frac{e^{j\left(m\frac{\pi}{2}(1+M\cos(\phi))\right)} - e^{-j\left(m\frac{\pi}{2}(1+M\cos(\phi))\right)}}{jm}\, d\phi$$

and knowing that $\int_{-\pi}^{\pi} e^{j\xi\cos(\phi)} \cos(-n\phi)\, d\phi = 2\pi j^{-n} J_{-n}(\xi)$, eqn. (A.17) can be re-written as:

$$C_{m0} = A_{m0} + jB_{m0}$$
$$= \frac{V_{dc}}{jm\pi}\left[e^{j\left(m\frac{\pi}{2}\right)} J_0\left(m\frac{\pi}{2}M\right) - e^{-j\left(m\frac{\pi}{2}\right)} J_0\left(-m\frac{\pi}{2}M\right)\right] \qquad \text{(A.18)}$$

and because $J_0(-\xi) = J_0(\xi)$ eqn. (A.18) gives

$$C_{m0} = A_{m0} + jB_{m0} = \frac{2V_{dc}}{m\pi^2} J_0\left(m\frac{\pi}{2}M\right) sin\left(-m\frac{\pi}{2}\right) \qquad \text{(A.19)}$$

These terms define the harmonics of the carriers itself.

For <u>m>0, n=0</u> $\Rightarrow$

$$C_{mn} = A_{mn} + jB_{mn}$$
$$= \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+M\cos(\phi))}^{\frac{\pi}{2}(1+M\cos(\phi))} V_{dc} e^{j(m\theta + n\phi)}\, d\theta\, d\phi \qquad \text{(A.20)}$$

which will give

$$C_{mn} = A_{mn} + jB_{mn}$$
$$= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} e^{jn\phi} \frac{e^{-j\left(m\frac{\pi}{2}(1+M\cos(\phi))\right)} - e^{-j\left(m\frac{\pi}{2}(1+M\cos(\phi))\right)}}{jm}\, d\phi \qquad \text{(A.21)}$$
$$= \frac{V_{dc}}{j2m\pi^2} \int_{-\pi}^{\pi} \left(e^{jm\frac{\pi}{2}} e^{jn\phi} e^{jm\frac{\pi}{2}M\cos(\phi)} - e^{-jm\frac{\pi}{2}} e^{jn\phi} e^{-jm\frac{\pi}{2}M\cos(\phi)} \right) d\phi$$

and using the formula $\int_{-\pi}^{\pi} e^{j\xi\cos(\phi)} e^{jn\phi}\, d\phi = 2\pi j^n J_n(\xi)$, eqn. (A.21) becomes:

$$C_{mn} = A_{mn} + jB_{mn} = \frac{V_{dc}}{jm\pi}\left[e^{jm\frac{\pi}{2}} j^n J_n\left(m\frac{\pi}{2}M\right) - e^{-jm\frac{\pi}{2}} j^{-n} J_n\left(m\frac{\pi}{2}M\right)\right]$$

$$= \frac{V_{dc}}{jm\pi} J_n\left(m\frac{\pi}{2}M\right)\left[e^{jm\frac{\pi}{2}} e^{jn\frac{\pi}{2}} - e^{-jm\frac{\pi}{2}} e^{-jn\frac{\pi}{2}}\right] \qquad \text{(A.22)}$$

$$= \frac{2V_{dc}}{m\pi} J_n\left(m\frac{\pi}{2}M\right) sin\left([m+n]\frac{\pi}{2}\right)$$

These terms define the sidebands of the modulated wave. The complete harmonic solution for double-edge naturally sampled modulation for the one-leg half-bridge is hence formed by substituting eqns. (A.14), (A.15), (A.18) and (A.21) back into (A.13):

$$\begin{aligned} V_{an}(t) &= V_{dc}/2 \\ &\quad + (V_{dc}/2)M\cos(\omega_s t) \\ &\quad + \frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\frac{1}{m} J_0\left(M\frac{\pi}{2}m\right)\sin m\frac{\pi}{2}\cos(m\omega_c t) \\ &= \frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty}\frac{1}{m} J_n\left(M\frac{\pi}{2}m\right)\sin\left([m+n]\frac{\pi}{2}\right)\cos(m\omega_c t + n\omega_s t) \end{aligned} \qquad \text{(A.23)}$$

which can be re-written as:

$$\begin{aligned} V_{an}(t) &= V_{dc}/2 + (V_{dc}/2)M\cos(\omega_s t) + \\ &= \frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m} J_n\left(M\frac{\pi}{2}m\right)\sin\left([m+n]\frac{\pi}{2}\right)\cos(m\omega_c t + n\omega_s t) \end{aligned} \qquad \text{(A.24)}$$

By including the 180° phase shift of the fundamental of leg b in a full-bridge configuration, the above relation will directly yield V_{bn} as follow:

$$V_{bn}(t)=V_{dc}/2+(V_{dc}/2)M\cos(\omega_s t-\pi)+$$
$$=\frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(M\frac{\pi}{2}m\right)\sin\left([m+n]\frac{\pi}{2}\right)\cos(m\omega_c t+n(\omega_s t-\pi)) \quad \text{(A.25)}$$

Now the voltage across the full-bridge (between the two legs of the full-bridge) given by $V_{ab} = V_{an} - V_{bn}$ is:

$$V_{ab}(t)=V_{dc}M\cos(\omega_s t)+$$
$$\frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(M\frac{\pi}{2}m\right)\sin\left([m+n]\frac{\pi}{2}\right)$$
$$\times(\cos(m\omega_c t+n\omega_s t)-\cos(m\omega_c t+n(\omega_s t-\pi)))$$
$$=V_{ab}(t)=V_{dc}M\cos(\omega_s t)+ \quad \text{(A.26)}$$
$$\frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(M\frac{\pi}{2}m\right)\sin\left([m+n]\frac{\pi}{2}\right)$$
$$\times(-2)\sin\left(m\omega_c t+n\omega_s t-n\frac{\pi}{2}\right)\sin\left(n\frac{\pi}{2}\right)$$

For an even n, $\sin\left(n\frac{\pi}{2}\right)$ will be null, so eqn. (A.26) simplifies to:

$$V_{ab}(t)=V_{dc}M\cos(\omega_s t)+$$
$$\frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_{(2n-1)}\left(M\frac{\pi}{2}m\right)\sin\left([m+(2n-1)]\frac{\pi}{2}\right) \quad \text{(A.27)}$$
$$\times\cos(m\omega_c t+(2n-1)\omega_s t)$$

It easy to see that for all odd values of m, $\sin\left([m+(2n-1)]\frac{\pi}{2}\right)$ will be null, so (A.27) can be rewritten as:

$$V_{ab}(t)=V_{dc}M\cos(\omega_s t)+ \frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{(2n-1)}\left(M\frac{\pi}{2}2m\right)\sin\left([2m+(2n-1)]\frac{\pi}{2}\right) \times\cos(2m\omega_c t+(2n-1)\omega_s t) \quad \text{(A.28)}$$

and, hence, the final form will be:

$$V_{ab}(t)=V_{dc}M\cos(\omega_s t) +\frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{(2n-1)}(M\pi n)\cos((m+n-1)\pi) \times\cos(2m\omega_c t+(2n-1)\omega_s t) \quad \text{(A.29)}$$

A.3. Fourier analysis of double-edge asymmetrical regularly sampled PWM

Using a procedure similar to that in section A.2 leads to the Fourier series description of a double-edge asymmetrical regularly sampled PWM waveform [6]:

$$V_{ab}(t)=\frac{4V_{dc}}{\pi}\sum_{n=1}^{\infty}\frac{1}{\left[n\frac{\omega_s}{\omega_c}\right]}J_n\left(n\frac{\omega_s}{\omega_c}\frac{\pi}{2}M\right)\sin\left(n\frac{\pi}{2}\right)\cos(n\omega_s t) +\frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{\left[2m+[2n-1]\frac{\omega_s}{\omega_c}\right]}J_{2n-1}\left(\left[2m+[2n-1]\frac{\omega_s}{\omega_c}\right]\frac{\pi}{2}M\right)\cos([m+n-1]\pi) \times\cos(2m\omega_c t+[2n-1]\omega_s t) \quad \text{(A.30)}$$

APPENDIX B: SIMULATION SCHEMATICS

B.1. PSpice Schematics

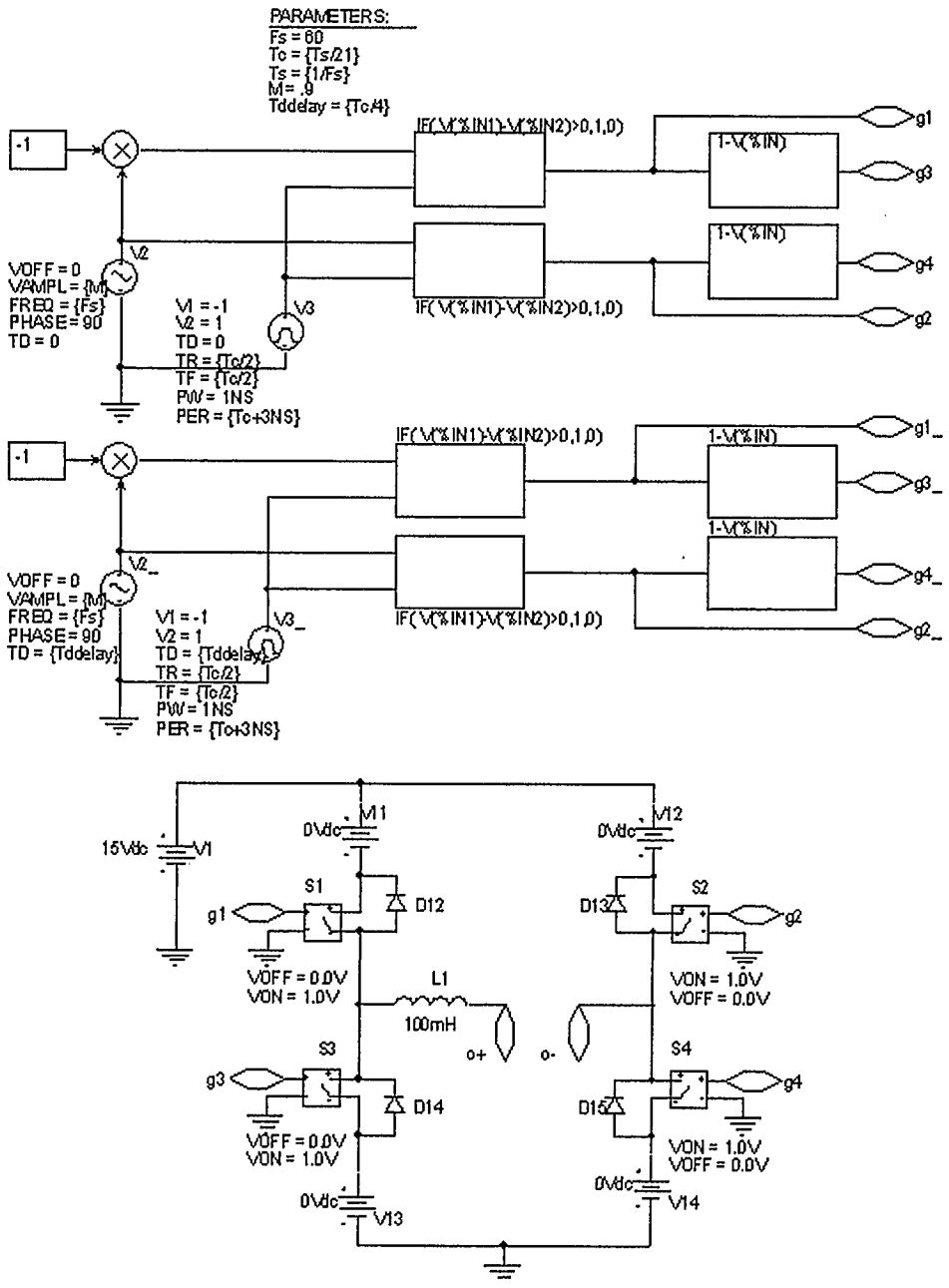


Fig. B.1 PSpice schematic for NSPWM generator (top graph) and two parallel single-phase inverters (bottom graph, only one H-bridge is shown)

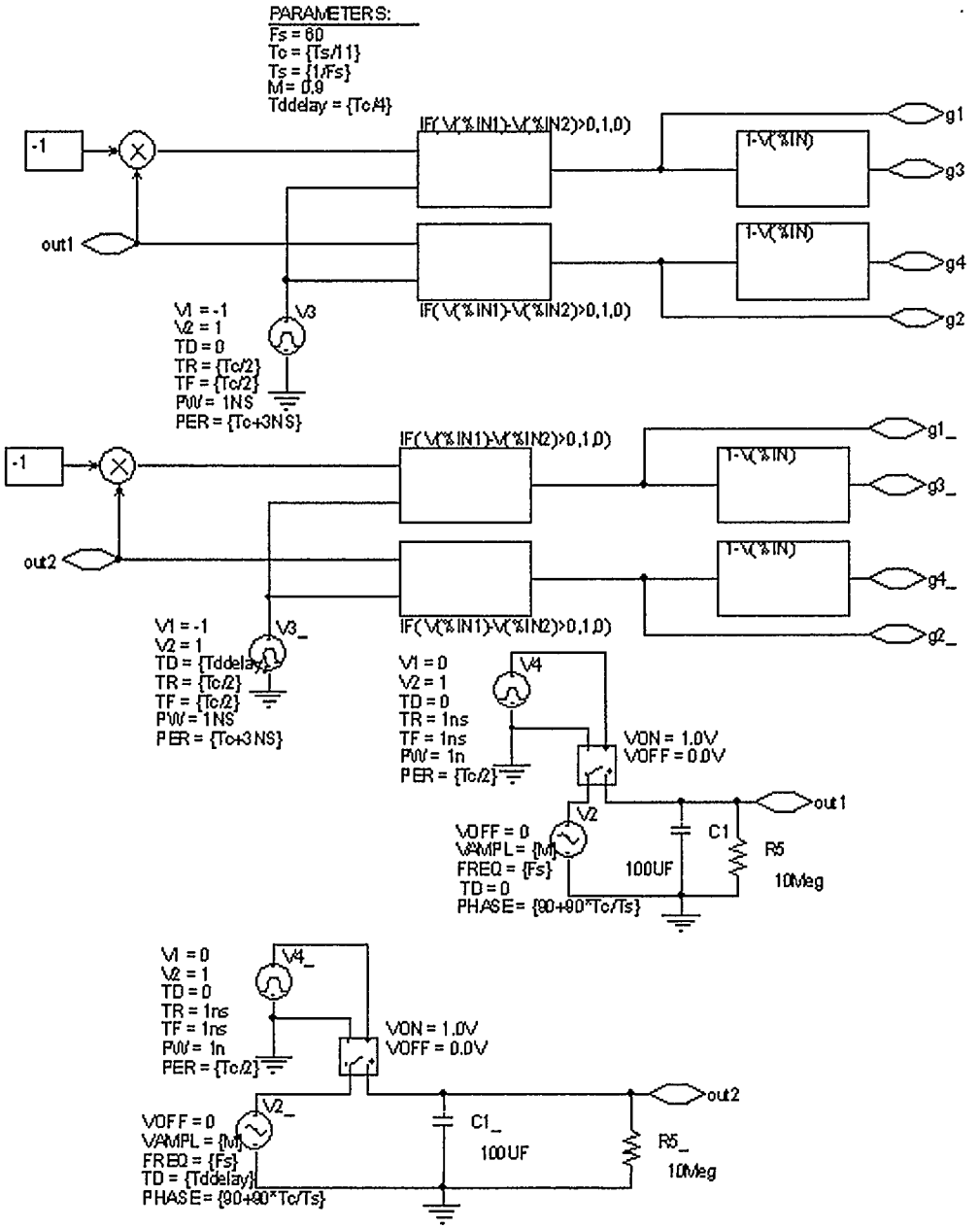


Fig. B.2 PSpice schematic for asymmetrical RSPWM generator for two parallel single-phase inverters

B.2. MATLAB Schematics

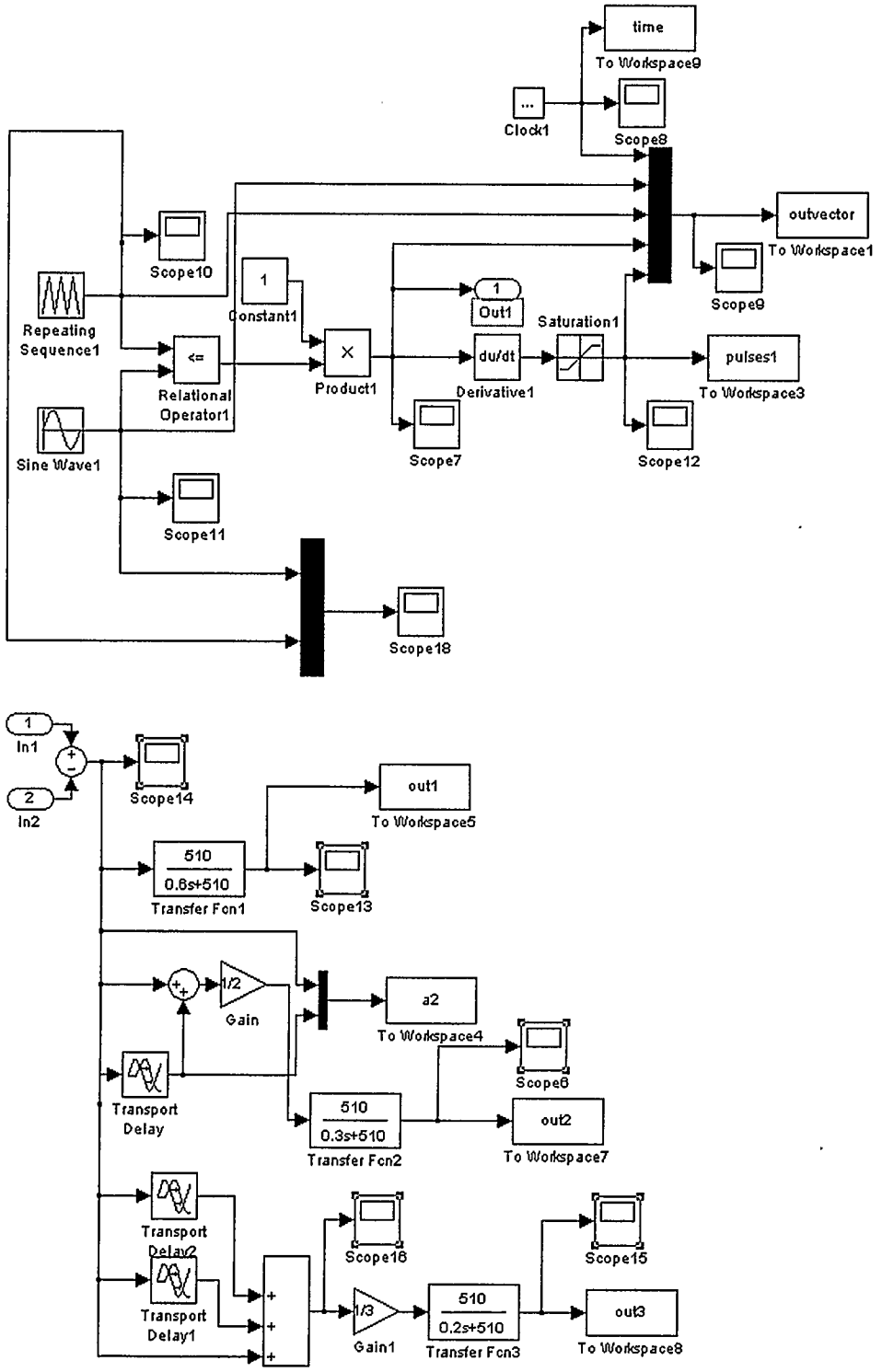
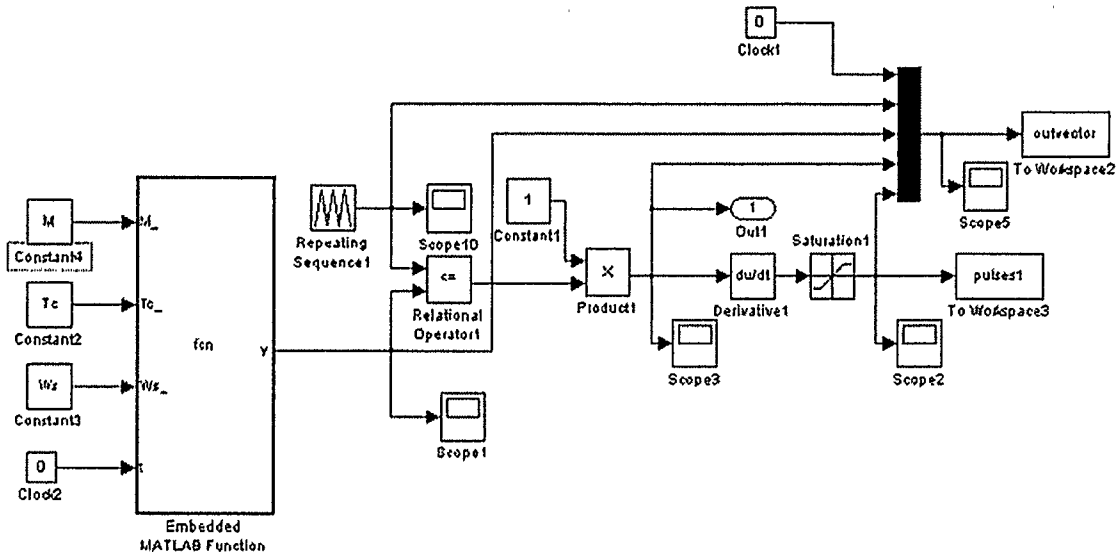


Fig. B.3 Top graph: MATLAB schematic for NSPWM generator, only one leg is shown (In2 comes from the other leg); bottom graph: one, two and three parallel single-phase inverters




```
function y = fcn(M_, Tc_, Ws_, t)
slot = floor(t/(Tc_/2));
y = M_*cos(Ws_*slot*Tc_/2);
```

Fig. B.4 MATLAB schematic for asymmetric RSPWM generator (only one leg shown, see Fig. C.3)

APPENDIX C: PIC16F877 ASSEMBLY CODE

Following is an excerpt of the PIC16F877 assembly program. Fig. C.1 (a) shows a flow chart of the control program as a whole, while the flow chart in Fig. C.1 (b) shows the time delay subroutine.

```
; ================================================================
;   This program generates the output PWM gates signal (for one H-bridge) on
;   PORTA0...3, register 0x7F holds pulse time width.
; ================================================================
        list    p=16f877            ; list directive to define processor
        #include <p16f877.inc>      ; processor specific variable definitions
        _CONFIG _CP_OFF & _WDT_OFF & _BODEN_OFF & _PWRTE_ON &
        _XT_OSC & _WRT_ENABLE_ON & _LVP_OFF & _DEBUG_OFF
        & _CPD_OFF
        ORG     0x000               ; processor reset vector
        clrf    PCLATH              ; ensure page bits are cleared
        goto    main                ; go to beginning of program
        ORG     0x004               ; interrupt vector location
        clrf INTCON
        retfie                      ; return from interrupt

        ; delay subroutine starts
Delay   nop
        .
        .
        nop
Here    decfsz 0x7F, F
        goto Here
        return
        ; delay subroutine ends

main
        bcf STATUS, RP0             ; ank0
        bcf STATUS, RP1             ; initialize PORTA by
        clrf PORTA                  ; clearing output
                                    ;
        bsf STATUS, RP0             ; Select Bank 1
        bcf INTCON, GIE             ; Configure all pins
        bsf INTCON, 4               ; as digital inputs
        movlw 0x06                  ; Value used to
```

```
        movwf ADCON1            ; initialize data
        movlw 0xC0              ; direction
        movwf TRISA
        bcf STATUS, RP0         ; Select Bank 0

        ; phase-shift delay starts
        movlw .124              ; load 0x7F with 124
        movwf 0x7F
        call Delay              ; call Delay subroutine
        ; phase-shift delay ends

LoopMain
        ; beginning of one output period
        movlw b'00000011'       ; load PORTA with the binary
        movwf PORTA             ; value 00000011
        movlw .9                ; load 0x7F with 09
        movwf 0x7F
        call Delay              ; call Delay subroutine

        movlw b'00001001'
        movwf PORTA
        movlw .165
        movwf 0x7F
        call Delay
        .
        .
        .
        ; end of one output period
        goto LoopMain           ; jump to LoopMain
        END                     ; directive 'end of program'
```

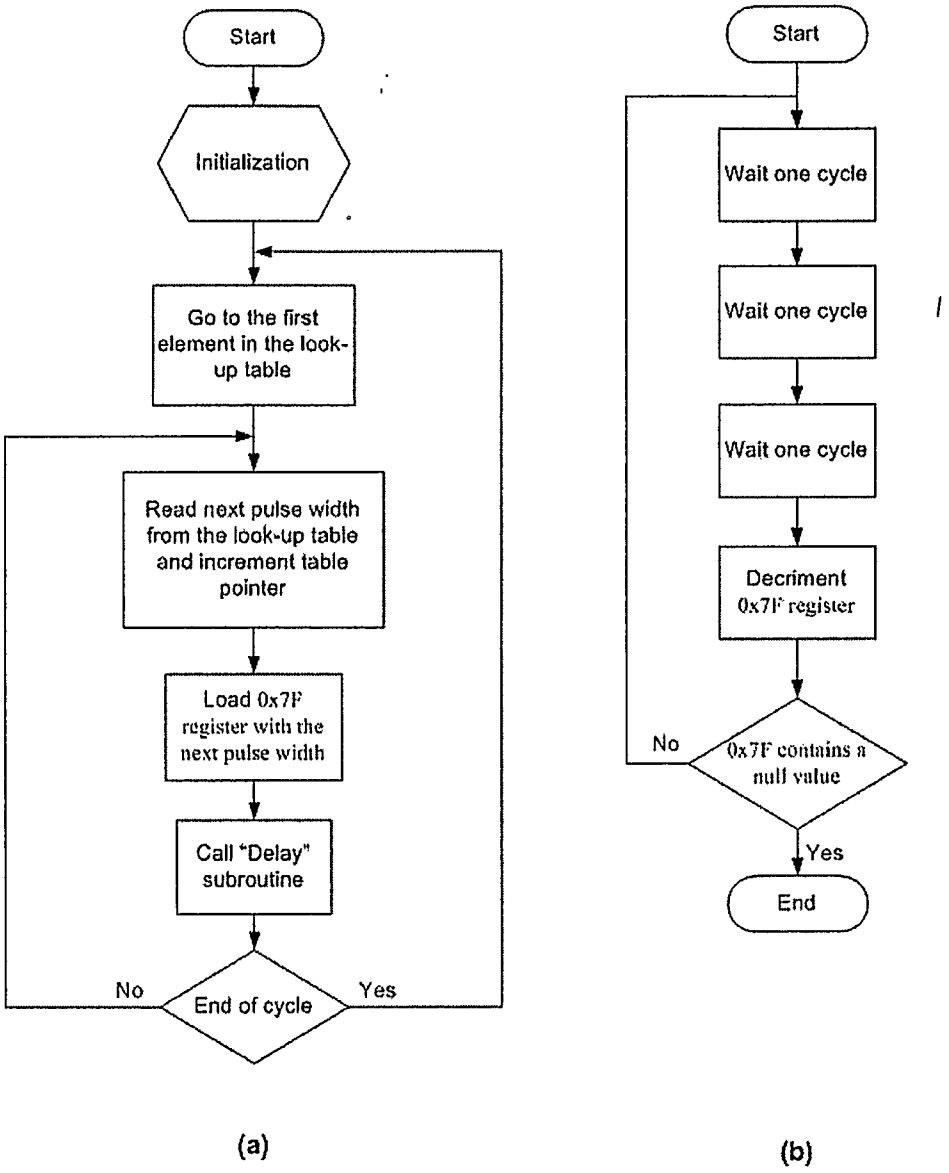


Fig. C.1 (a) Flow chart of the PIC 16F877 control program; (b) Flow chart of the time delay subroutine.