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A 460 GHz CMOS Substrate-Integrated-Waveguide Slot Antenna

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by

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A THESIS

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Abstract

The design of the Cerro Chajnantor Atacama Telescope (CCAT) is progressing within the international astronomical community. This thesis examines the feasibility of using CMOS technology to implement a 460 GHz SIW slot antenna for the CCAT Heterodyne Array Instrument.

A 46 GHz broadband high-gain SIW slot antenna was designed and tested to verify the SIW slot antenna design procedure. That design demonstrated good agreement between the simulated and measured results. The antenna has a measured gain of 7.8 dBi at 46.2 GHz and bandwidth of 4.72GHz. Then design of a 460GHz SIW antenna was conducted in a 65nm CMOS process. Several methods were used to simplify the design and sim-ulations: an inductor identification layer was introduced to minimize the design-rule re-strictions, and an equivalent dielectric layer was calculated to reduce the computational resource for 3D electromagnetic simulations. The proposed antenna has a gain of 0.09dBi, efficiency of 29.1% and bandwidth of 25.3GHz.

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Most importantly, I would like to thank my family and wife. I would never have been able to finish my thesis without the support from them.

For my parents and wife.

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Symbol	Definition
α	Attenuation Constant
ALMA	The Atacama Large Millimeter/Submillimeter Array
β	Phase Constant
C	Capacitance
c	Speed of Light in Vacuum
CCAT	Cerro Chajnantor Atacama Telescope
CHAI	CCAT Heterodyne Array Instrument
CMOS	Complementary Metal Oxide Semiconductor
ε_0	Electric Permittivity of Free Space
ε_r	Relative Electric Permittivity
E-ELT	The European Extremely Large Telescope
η	Intrinsic Impedance
f_c	Cutoff Frequency
γ	Propagation Constant
GMT	The Giant Magellan Telescope
HFSS	High-Frequency Structure Simulator
HPC	High Performance Computer
HPBW	Half-Power Beam Width
IRTF	Infrared Telescope Facility
JCMT	The James Clerk Maxwell Telescope
k	Wave Number
K	Kelvin

λ_0	Wavelength in Free Space
λ_g	Guided Wavelength
LTCC	Low-Temperature Co-fired Ceramic
μ_0	Permeability of Free Space
PCB	Printed Circuit Board
PEC	Perfect Electric Conductor
R_s	Sheet Resistance
ρ	Resistivity
σ	Conductivity
S_{11}	Scattering Parameter at Port 1 From Port 1
S_{21}	Scattering Parameter at Port 2 From Port 1
SiGe	Silicon-Germanium
SIW	Substrate-Integrated Waveguide
SPT	The South Pole Telescope
$\tan\delta$	Loss Tangent
TE	Transverse Electric
TM	Transverse Magnetic
TMT	The Thirty Meter Telescope
TSMC	Taiwan Semiconductor Manufacturing Company
UKIRT	UK Infrared Telescope
VNA	Vector Network Analyzer
Z_0	Characteristic Impedance
Z_{SIW}	Characteristic Impedance of SIW

Chapter 1

Introduction

Human beings have always been fascinated by and never stopped observing and discovering the Universe. Many legends from both east and west about what the Universe looks like and how it was created show humans' curiosity with the Universe. From Stonehenge to the great Pyramids, from the native North American structures at Chaco Canyon in New Mexico to the mysterious mounds of Bronze Age Britain, it is clear that the Universe, and the sky, was important to humanity. The observational astronomy is a branch of science dealing with collecting data pertaining to various aspects of the Universe evolution. Observational astronomy is continuously benefited and even at times revolutionized by new developments in astronomical instrumentation. Since Galileo Galilei improved the telescope and implemented it into the astronomical observation instrument, the development of observational astronomy has been accelerating.

1.1 Astronomy and Electromagnetic Spectrum

Observational astronomy is subdivided into regions of the electromagnetic spectrum: the radio astronomy, infrared astronomy, optical astronomy, ultraviolet astronomy, X-ray astronomy and gamma-ray astronomy. These regions as part of the electromagnetic spectrum are illustrated in Figure 1.1. The visible band stretches from wavelength $0.4\,\mu$m to $0.7\,\mu$m,
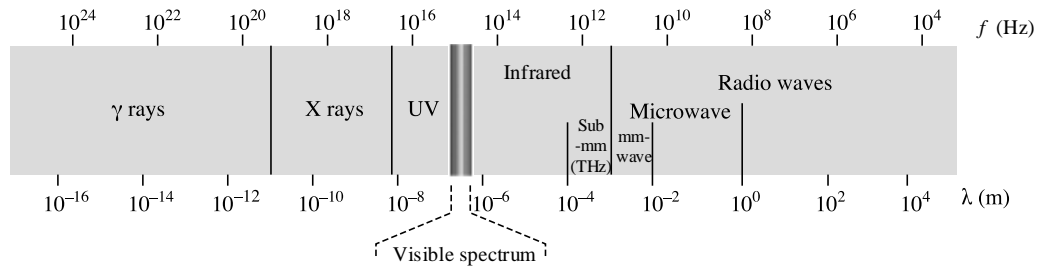
Figure 1.1: The electromagnetic spectrum, showing the gamma ray, x-ray, ultraviolet, visible, infrared and radio bands.

and the infrared band starts from $0.7\,\mu$m to $1\,$mm. The infrared band is so broad that it is often subdivided into a near infrared $(0.7-3\,\mu\text{m})$ band, a mid-infrared $(3-30\,\mu\text{m})$ band, a far infrared $(30-200\,\mu\text{m})$ band, and a submillimetre $(200-1000\,\mu\text{m})$ band [1].

The infrared radiation was first discovered by William Herschel in 1800 [2–4]. However, infrared astronomy progressed extremely slowly for the next 150 years. Jansky's discovery of the radiation from the Milky Way in 1933 is seen as the birth of the new science of radio astronomy [5, 6]. X-ray astronomy began in 1948 with the first detection x-rays from the Sun by using a captured German V2 rocket [7]. The father of submillimetre astronomy was Frank Low, who invented the gallium-doped germanium bolometer in 1961 [8, 9].

Optical astronomy mainly studies the surface of the stars and nearby gas ionized by those stars where the temperature brings thermal radiation into the visible range. X-ray astronomy deals with much hotter regions, where temperatures reach 1 million to 100 million degrees Kelvin (K). Infrared astronomy studies the cool universe, where the temperatures are in the range $3\,$K (at the wavelength of $1\,$mm) to $1000\,$K (at the wavelength of $3\,\mu$m) [1]. The average temperature of the Earth in 2013 according to NASA is $288\,$K (15°C). Therefore, the main radiation from the Earth is in the infrared band, which makes the sky extremely bright in the infrared making astronomical observations difficult. This is one reason why the infrared astronomy progressed slowly. Another two reasons are the slow technological development and a very strong absorption of the Earth's atmosphere. Strong absorbers such as water and carbon dioxide molecules attenuate infrared and submillimetre radiation significantly, and very little of it reaches the ground. The atmospheric transmission across the electromagnetic spectrum is illustrated in Figure 1.2. To improve the atmospheric transmission and reduce the attenuation of the incoming radiation, a high and dry location, like a mountain top, is preferred for an astronomical observatory especially for infrared and submilimetre astronomy [10].
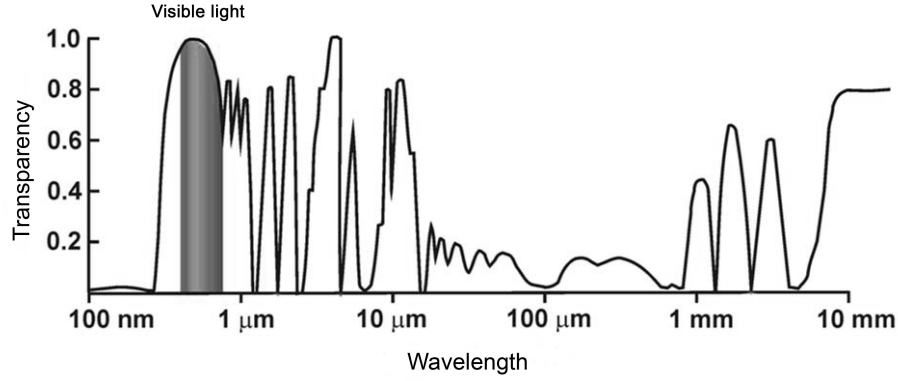
Figure 1.2: Atmospheric transmission across the electromagnetic spectrum.

1.2 Ground-Based Infrared and Submilimetre Telescopes

From the late 1970s, large near infrared and submillimetre telescopes were built on high altitude sites, especially on the 4200 m dormant volcanic peak of Mauna Kea, Hawaii. Such telescopes include the United Kingdom's 3.8-metre Infrared Telescope (UKIRT), NASA's 3-metre Infrared Telescope Facility (IRTF) and so on. The South Pole Telescope (SPT) is a 10 m diameter telescope at the 2800 m altitude Antarctic Plateau, which was designed for conducting large-area millimetre and sub-millimetre wave surveys of faint, low contrast emission [11]. The James Clerk Maxwell submillimetre telescope (JCMT), operated by a partnership among Canada, United Kingdom, and the Netherlands, is currently the largest single-dish telescope (diameter of 15 m) designed specifically to operate in the submillimetre region located at an altitude of 4092 m Mauna Kea, Hawaii [12,13]. The Atacama Large Millimeter/Submillimeter Array (ALMA) is the largest astronomical project in existence, composed of 66 high precision antennas located on the Chajnantor plateau, 5000 m altitude in northern Chile [14–16]. Some other ground-based telescopes are in an advanced stages of planing, with parts of their construction already under way: the European Extremely Large Telescope (E-ELT) with a mirror diameter of 39 m [17], the Thirty Meter Telescope (TMT) [18], the Giant Magellan Telescope (GMT) consisting of seven 8.4-metre-diameter telescopes [19], and the Cerro Chajnantor Atacama Telescope (CCAT) [20].
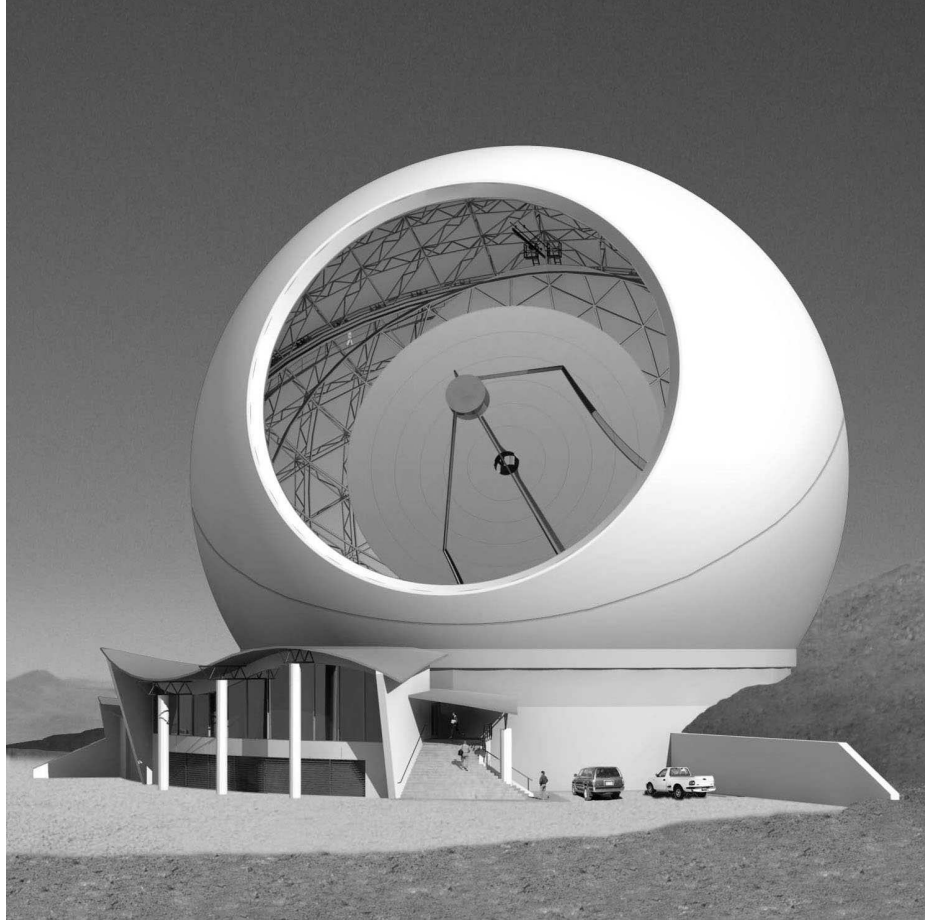
Figure 1.3: CCAT concept view at 5600 m Cerro Chajnantor, Chile. The image is taken from CCAT website: www.ccatobservatory.org.

1.3 CCAT and CCAT Heterodyne Array Instrument (CHAI)

CCAT will be a next-generation, 25 m diameter single dish telescope operating in the 2 to 0.2 mm wavelength range that will enable a broad range of astronomical studies, particularly those focused on the origins of stars, galaxies, and galaxy clusters. CCAT will be located at 5600 m altitude on Cerro Chajnantor in northern Chile [21, 22], where submillimetre observing conditions are better than on the 5000 m altitude of Chajnantor plateau where ALMA is located [23]. Figure 1.3 shows the concept view of the CCAT observatory at Cerro Chajnantor.

CCAT is presently a joint project between a number of countries and organizations:

Cornell University, Caltech, the University of Colorado at Boulder, the University of Cologne and the University of Bonn, McGill University, McMaster University, the University of British Columbia, the University of Calgary, the University of Toronto, the University of Waterloo, Dalhousie University, the Western University, and Associated Universities, Inc.

The initial plan for facility instruments for CCAT includes two large format bolometer cameras: a 32000-pixel short submillimetre $(200-650\,\mu\mathrm{m})$ camera using transition edge sensed bare bolometer arrays, and a 45000-pixel long wavelength camera $(850\,\mu\mathrm{m}-2\,\mathrm{mm})$ that uses slot dipole antenna coupled bolometer array [21]. Spectrometers, both direct detection and heterodyne, are also under consideration [22]. A 57160-pixel Short Wavelength Camera (SWCam) for CCAT was presented in [24], which consisted of 7 sub-cameras: 4 subcameras at $350\,\mu\mathrm{m}$, 1 at $450\,\mu\mathrm{m}$, 1 at $850\,\mu\mathrm{m}$, and 1 at $2\,\mathrm{mm}$ wavelengths. A design of a Long Wavelength Camera (LWCam), the long-wavelength imaging camera for CCAT, was proposed in [25]. LWCam will provide a $20'$ field-of-view with background-limited sensitivity in six bands: $750\,\mu\mathrm{m}$, $850\,\mu\mathrm{m}$, $1\,\mathrm{mm}$, $1.3\,\mathrm{mm}$, $2\,\mathrm{mm}$, and $3\,\mathrm{mm}$. A result of a design study for a multi-beam X-Spec survey spectrometer covering $190-520\,\mathrm{GHz}$ under development for CCAT was presented in [26].

CCAT Heterodyne Array Instrument (CHAI) [27] is also one of the first-light instruments for CCAT, which has two 64-pixel cameras for high resolution heterodyne spectroscopy. Specifically, CHAI is a modular, dual-frequency band array receiver covering $460\,\mathrm{GHz}$ and $830\,\mathrm{GHz}$ for simultaneous observations with $64-$ pixel arrays each, which is larger than any of the heterodyne array instruments currently in operation. The development of CHAI involves many countries and organizations: Universities of Cologne, University of Bonn (Germany), Cornell University, California Institute of Technology, and Jet Propulsion Laboratory (JPL) (US), University of Calgary, and University of Waterloo (Canada).

1.4 Thesis Goals

The subject of this thesis is an evaluation of the possibility of building a CMOS antenna for the CHAI to serve as either a feeding structure to a more traditional horn antenna, or to replace the horn antenna. So far, a design of a 470 GHz horn antenna[1] for CHAI was reported in [28], which presented a smooth-walled horn design. This antenna has a gain of 31.3 dBi. The horn is 46 mm long with an aperture diameter of 12.8 mm. The size of the horn and its gain are larger than what would be possible to fabricate in CMOS process. Therefore, it is not expected that the CMOS antenna could outperform the horn on its own but the integration of smaller CMOS antennas with the rest of the receiver circuitry on a single integrated circuit (IC) could significantly increase the number of CHAI pixels and compensate for lower gain of each individual antenna.

This thesis sets out to develop a front-end antenna on CMOS process. This work is a pilot project to investigate the feasibility of designing a 460 GHz on-chip antenna with the purpose of integrating with entire CHAI receiver on the same IC. While this work is not officially a part of CCAT CHAI development, it may provide alternatives to cost-effective implementation of CHAI.

In addition, due to limitations of our laboratory equipment at the start of the project, it would have been impossible to measure a 460 GHz antenna. Therefore, a 46 GHz antenna, which is a down-scaled prototype of the 460 GHz antenna, was designed, fabricated, and measured first for a verification of the design concept [29]. The 460 GHz antenna was also designed but not fabricated.

1.5 Thesis Outline

The rest of this thesis is structured as follows:

- Chapter 2 gives the relevant background information on the substrate-integrated waveg-

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[1]Note that CHAI frequency range has not been finalized yet and therefore slightly different frequencies have been selected by different groups.

uides (SIW) and slot antennas and discusses CMOS and printed circuit-board (PCB) antennas previously designed by others.

- Chapter 3 proposes a design of a 46 GHz SIW slot antenna and presents simulated and measured results.

- Chapter 4 presents a 460 GHz SIW slot antenna based on a 65 nm CMOS process.

- Chapter 5 provides conclusions, contributions, and suggestions for future work.

Chapter 2

Selection of CMOS Compatible Antenna Topology

This chapter describes the selection procedure of an antenna technology, which can be integrated on a CMOS integrated circuit (IC) and which has the promise of having high efficiency and gain. After a literature review of the properties of commonly used terahertz (THz) antennas in Section 2.1 and a review of previously published CMOS-integrated millimeter-wave and THz antenna designs in Subsection 2.1.1, a substrate-integrated-waveguide (SIW) slot antenna is selected for this thesis. A SIW and the slot antenna are discussed in more details in Sections 2.2 and 2.3. Section 2.2 begins with a short review of the advantages of SIWs, explains the propagation modes supported by the SIW, and gives an expression for calculating the effective width of the equivalent rectangular waveguide. Next Section 2.3 introduces the slot antenna. In Section 2.3.1 the Babinet's Principle is presented. Section 2.3.2 explains how a slot antenna operates and gives an expression for calculation of the impedance of a longitudinal slot radiator.

2.1 Terahertz Antennas

Generally, THz antennas can be made through the dimensional scaling of their low-frequency counterparts. However, the fabrication process and use of materials can be quite different. Table 2.1 lists the comparison of the distinct properties of the most commonly used THz antennas [30]. Some other antennas may also be designed as THz antenna, but not included in the Table 2.1. For example, dipole and dielectric resonator (DR) antennas, which will be demonstrated in the next subsection. The 460 GHz antenna discussed in this thesis is expected to be implemented in a standard CMOS process, which narrows down the candidates of antennas: only slot array, patch and dipole antennas can be fabricated on a CMOS process.

Table 2.1: Comparison of different millimeter-wave and terahertz antennas [30].

	Reflector	Slot array	Horn	Dielectric integrated lens	Patch
Frequency	Any	$< 0.5\,\mathrm{THz}$	$< 1\,\mathrm{THz}$	Any	$< 0.1\,\mathrm{THz}$
Gain	High++	High	Average	Low+	Low
Bandwidth	Wide-	Narrow	Wide	Average	Narrow
Cost	High++	High	Average+	Low+	Low
Fabrication	Difficult+	Average	Difficult	Easy+	Easy
Size	Large++	Large+	Average	Small	Small
Weight	Heavy++	Average	Average++	Light	Light

2.1.1 Antennas in CMOS Process

On-chip antennas are an essential building block in realizing fully integrated transceivers. However, achieving high efficiency and high gain is rather challenging. CMOS on-chip antennas with the operating frequencies from 24 GHz to THz will be demonstrated next and summarized in Table 2.2.

[31] reported a 24 GHz dipole fabricated on a 2-inch wafer with copper metallization process, which achieved $-17\,\mathrm{dB}$ impedance bandwidth from 20 GHz to 30 GHz and a gain of $-8\,\mathrm{dBi}$. Inverted-F and Yagi antennas operating at 60 GHz with efficiency below 10% and gain below $-10\,\mathrm{dBi}$ were reported in [32–34]. A 60 GHz SIW integrated high-gain horn antenna fed by co-planar waveguide (CPW) [35] with CMOS-compatible micro-fabrication steps achieved a gain of 14.6 dBi. However, the area of the horn is more than $500\,\mathrm{mm}^2$. Another 60 GHz 0.13 μm CMOS patch antenna, which has a peak gain of $-3.32\,\mathrm{dBi}$, efficiency of 15.9%, and size of $1220\,\mu\mathrm{m} \times 1580\,\mu\mathrm{m}$, was reported in [36]. Two 60 GHz CMOS dipole antennas with measured gain around $-7 \sim -9\,\mathrm{dBi}$ (far below the simulated gain) were reported in [37] and [38].

On-chip DRAs, which are dielectric resonators attached on a CMOS IC with opera-

tion frequency below 150 GHz, were reported in [39–43]. Placing the dielectric resonator precisely on such tiny IC chip is a challenge. The simulation in [44] indicated that placing a 12 mm diameter hemispherical quartz lens on a 90 GHz CMOS elliptical slot antenna could increase the antenna efficiency from 7% to 30%, bandwidth from 3.1% to 4.4% and gain form -5.7 dBi to 15 dBi. A 140 GHz tapered slot antenna fabricated in a 65 nm CMOS process was presented in [45]. This antenna has a gain of -25 dBi and occupies $180 \, \mu m \times 100 \, \mu m$ of die area. A 270 GHz circular-polarized SIW antenna with corner slots [46] was shown to have a broadside radiation pattern with a gain of -0.5 dBi and a radiation efficiency of 21.4%, when designed in a 65 nm CMOS process occupying an area of $0.17 \, mm^2$. A 410 GHz CMOS patch antenna with a simulated directivity of 5 and efficiency of 22% was presented in [47]. A 434 GHz SIW slot antenna with a transmitter/receiver chip-set was fabricated in SiGe BiCMOS process, which had a simulated gain of -0.55 dBi and efficiency of 49.8% [48]. Another 0.54 THz CMOS planar dipole antenna with a simulated gain of 1.33 dBi and efficiency of 28% was reported in [49].

Overall, the patch, dipole, Yagi, and Inverted-F antennas have lower gain and efficiency than other antennas. Although the dielectric resonator and lens antennas have high efficiency, they require post-processing to attach them onto a CMOS IC, thus increasing the fabrication complexity and cost. Only slot antenna appears as a good candidate for this project. Therefore a slot antenna feed by means of a SIW is selected in the thesis.

2.2 SIW

Over the last decades, the constantly increasing demands for more and more compact electronics devices and for more and more broadband radio communications services have been nudging their implementations to ever higher frequency bands. To keep up with this frequency increase, new technologies are required that can operate at high frequencies. The substrate integrated waveguide (SIW) technology is one of the new emerging technologies, which has been developed rapidly for use in millimetre-wave (mm-wave) and terahertz

Table 2.2: Comparison of on-chip antennas.

Ref.	Process	Antenna Type	Frequency (GHz)	-10 dB BW (GHz)	Gain (dBi)	Efficiency	Chip Size (mm^2)
[31]	CMOS Compatible	Dipole	24	20-30*	−8	NA	1.53
[32]	Back End of Line	Inverted-F	61	55-67.5	-19	3.5%	0.38
		Quasi-Yagi	65	55-65	-12.5	5.6%	0.55
[33]	0.18 μm CMOS	Yagi	60	55-65	-10	10%	1.05
[34]	0.18 μm CMOS	Inverted-F	60	55-65	-15.7	10%	0.58
[35]	CMOS Compatible	SIW Horn	60	56.9-63.2	14.4	NA	518
[36]	0.13 μm CMOS	Patch	60	0.81	-3.3	15.9	1.93
[37]	90 nm CMOS	Dipole	60	58-70	-7	4.6%	0.35
[39]	CMOS	DRA	135	126-144	3.7	62%	0.63
[40]	0.18 μm CMOS	DRA	130	123-137	4.7	43%	0.72
[44]	0.13 μm CMOS	Elliptical Slot	90	90-93	-5.7	7%	2.25
		With Dielectric Lens	90	89-91	15	30%	NA
[45]	65 nm CMOS	Tapered Slot	140	NA	-25	NA	0.02
[46]	65 nm CMOS	Circular-Polarized SIW	270	251.5-283.6	-0.5	21.4%	0.17
[47]	45 nm CMOS	Patch	410	NA	0.41	22%	0.04
[48]	0.13 μm SiGe BiCMOS	SIW Slot	434	~15	-0.55	49.8%	0.11
[49]	40 nm CMOS	Dipole	540	NA	1.33	28%	0.05
[50]	CMOS	Bowtie Slot	90	NA	-1.5	NA	1.26
	CMOS	Slot	140	136-141	-1.4	NA	0.72
	CMOS	SIW Slot	140	NA	-1	NA	1.2
	CMOS	Patch	140	138-148	-2	NA	0.49
[51]	0.18 μm SiGe BiCMOS	Patch	65	62-65	NA	NA	2.21

* −17 dB bandwidth
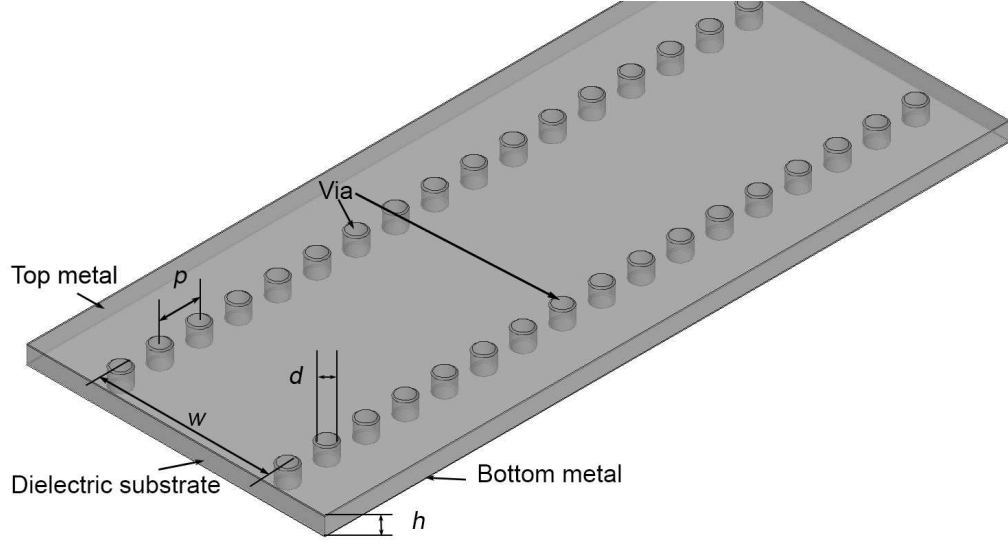
Figure 2.1: Geometry of a SIW.

$(30 - 10000\,\mathrm{GHz})$ frequency ranges [30, 52].

Figure 2.1 shows a typical geometry of a SIW when implemented on a PCB with some of its critical dimensions are: height h, width w, via diameter d, and via spacing p. A SIW is an integrated rectangular waveguide-like structure, which is synthesized in planar form by using rows of conducting vias or slots embedded in a dielectric substrate with the metalized top and bottom broadside walls [53]. In this way, the non-planar rectangular waveguide can be made in planar form, making it compatible with existing planar process, such as printed circuit board (PCB) and low-temperature co-fired ceramic (LTCC) processes. The intrinsic advantages of the planar circuits are numerous: small size, low weight, low cost, relatively simple manufacturing processes, accurate implementation, and ease of mass production. Whereas, most traditional planar circuits lack the high power carrying capacity and high-frequency quality-factors of conventional waveguides, SIWs not only preserve the advantages of planar circuits but also keep most of the advantages associated with conventional waveguides: electromagnetic shielding (eliminating radiation losses), low insertion loss, high power carrying capacity and high quality-factor. The most significant advantage of SIW technology is ease of integrating all components on the same substrate.
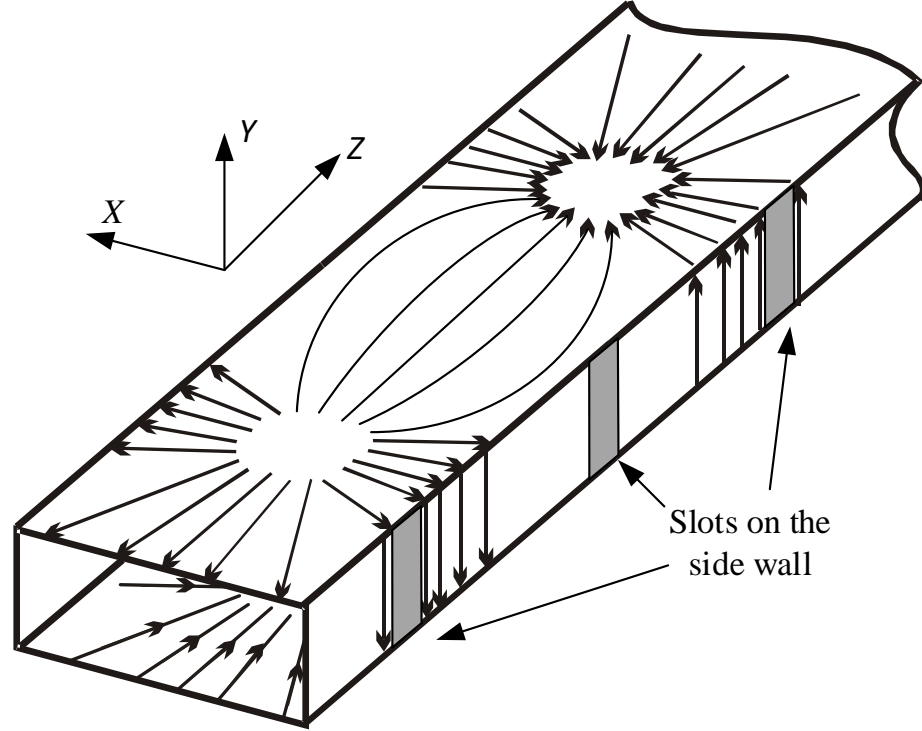
Figure 2.2: Surface current distribution of the TE_{10} mode in a rectangular waveguide with vertical slots in its side wall.

The propagation characteristics of a SIW is similar to that of rectangular waveguides. A SIW can be seen as a special rectangular waveguide filled with dielectric substrate and with some slots created by vias along its side walls. Figure 2.2 shows surface current distribution of the TE_{10} mode in a rectangular waveguide with vertical slots in its side wall. As can be seen, the vertical slots do not interrupt the surface currents of the TE_{10} mode. Thus, TE_{10} mode can propagate in the SIW. The higher TE_{m0} modes have similar surface current distribution and therefore TE_{m0} modes can propagate in SIW $(m = 1, 2, \cdots)$ as well. However TM modes produce longitudinal surface currents, which are interrupted by the presence of vertical slots, and hence TM modes would cause significant amount of radiation through side walls and these modes cannot be supported. Similarly, the same situation happens for TE_{mn} modes, for $n \neq 0$. As a result, only TE_{m0} modes $(m = 1, 2, \cdots)$ can propagate in SIW. A plot of the amplitude of the electric field of the dominant mode (TE_{10}) simulated at $46\,GHz$ in HFSS is presented in Figure 2.3. It illustrates how the
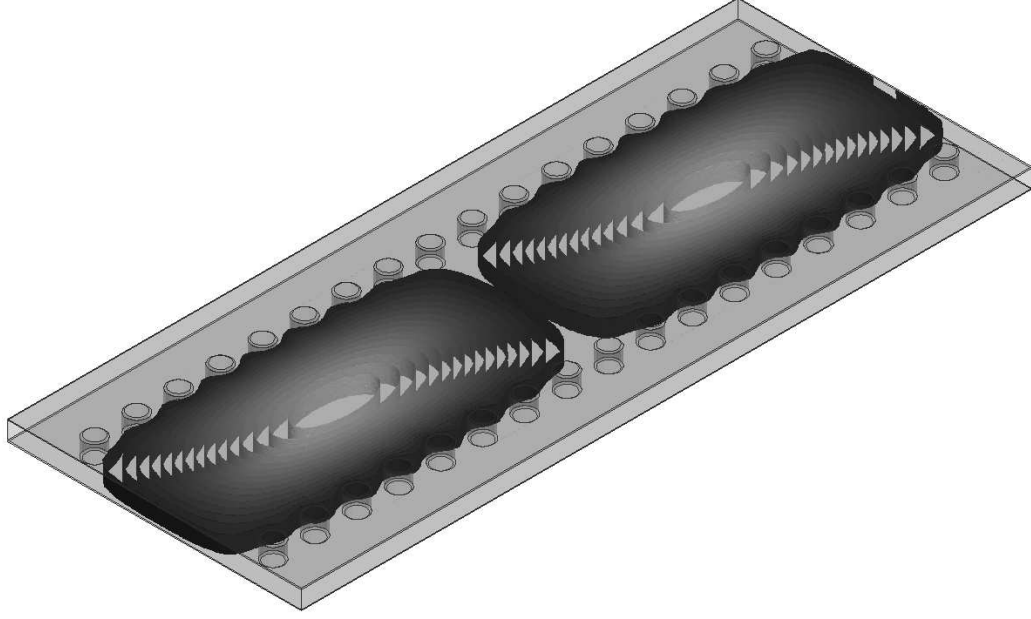
Figure 2.3: Plot of the amplitude of the electric field of the fundamental SIW mode (TE_{10}) in HFSS.

electric field intensity varies across the SIW. The fields are depicted as a grayscale map using white for maximum intensity and traversing to black for minimum field intensity. As can be seen, the radiation leakage can be neglected when the vias are closely spaced. A summary of propagation properties of the dominant mode (TE_{10}) in the rectangular waveguide is shown in Appendix A.

Due to the similarity between a SIW and a rectangular waveguide, an empirical relationship for calculation of the effective width w_{eff} of the rectangular waveguide was proposed in [54] as

$$w_{eff} = w - 1.08\frac{d^2}{p} + 0.1\frac{d^2}{w} \qquad (2.1)$$

where w is the width of SIW, d is the diameter of via and p is their longitudinal spacing as shown in Figure 2.1. It was also demonstrated that when $p/d < 3$ and $d/w < 1/5$, Equation 2.1 is very accurate [54]. From Equation 2.1, it is clear that the width of the rectangular waveguide is a little smaller than that of SIW.

Given a SIW with its w, d and p, the width of the equivalent rectangular waveguide

can be obtained. Sometimes a SIW needs to be transferred from a rectangular waveguide, where w is needed by transferring the Equation 2.1 to

$$w = \frac{w_{eff} + 1.08\frac{d^2}{s} + \sqrt{\left(w_{eff} + 1.08\frac{d^2}{s}\right)^2 - 0.4d^2}}{2} \tag{2.2}$$

Therefore, a design based on a rectangular waveguide can be easily transferred to SIW by using Equation 2.2.

2.3 Slot Antenna

A slot antenna is one of many aperture antennas, with the rectangular slot being one of the most common omnidirectional microwave antennas. Slot antennas often combine the feeding and radiating structures together by placing the slots in the wall of a waveguide, such as a SIW. The following subsections explain the principle of slot antenna operation.

2.3.1 Babinet's Principle

Babinet's Principle states that when a field behind a screen with an opening is added to the field of a complementary structure, then the sum is equal to the field where there is no screen [55]. H.G. Booker extended Babinet's Principle from optics to radio frequencies [56] by showing that the slot has the same radiation pattern as a dipole of the same dimensions as the slot but with its E-field and H-field are swapped as illustrated in Figure 2.4. In other words, a slot appears as a magnetic dipole rather than an electric dipole. As a result, its polarization is rotated $90°$. Thus, the radiation from a vertical slot is polarized horizontally. For example, a vertical slot has the same radiation pattern as a horizontal dipole of the same dimensions. Therefore, a longitudinal slot in the broad wall of a rectangular waveguide radiates like a dipole perpendicular to the slot in the same plane.

Moreover, Booker's extension of Babinet's Principle can be used to find a complemen-

15

H

E

E

H
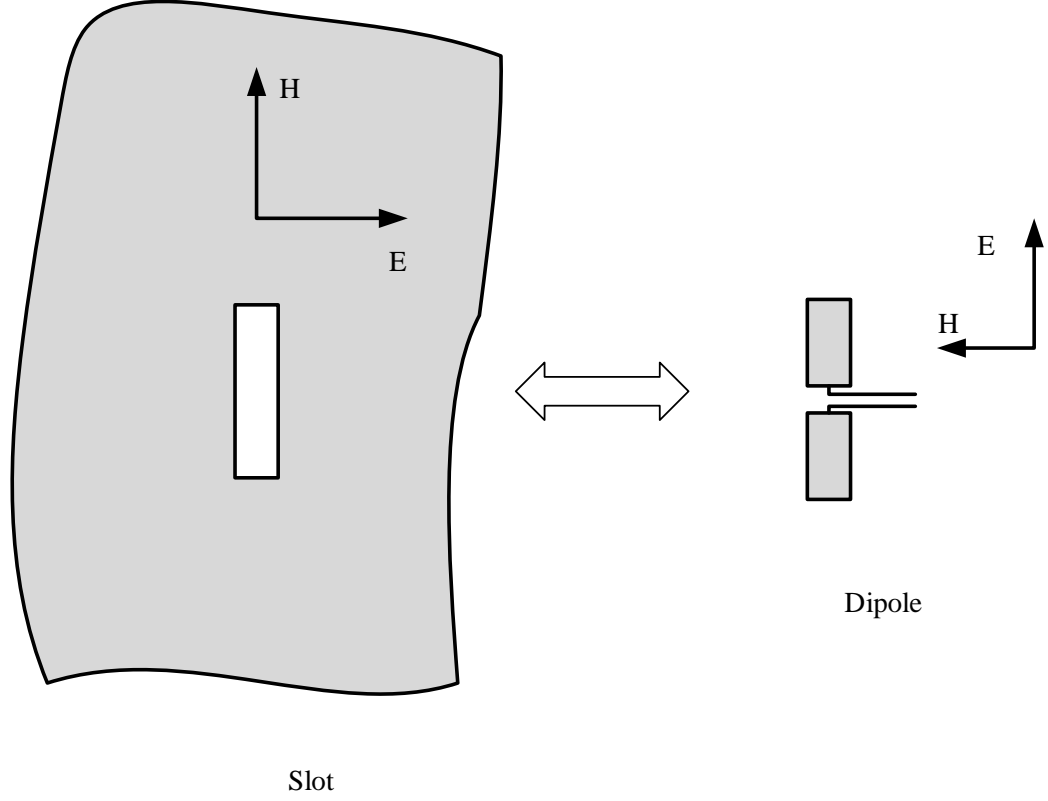
Dipole

Slot

Figure 2.4: Babinet's Principle.

tary impedance of the slot from:

$$Z_{slot}Z_{dipole} = \frac{\eta^2}{4} \tag{2.3}$$

$$\eta = \sqrt{\frac{\mu}{\varepsilon}} \tag{2.4}$$

where Z_{slot} and Z_{dipole} are input impedances of the slot and dipole antennas, respectively, η is the intrinsic impedance of the media in which the structure is immersed, and μ and ε are the permeability and permittivity of the media respectively.

2.3.2 Impedance of Longitudinal Slot Radiators

A longitudinal slot cut into the broad wall of a waveguide interrupts the transverse current flowing in the wall, which forces the current to travel around the slot thereby introducing
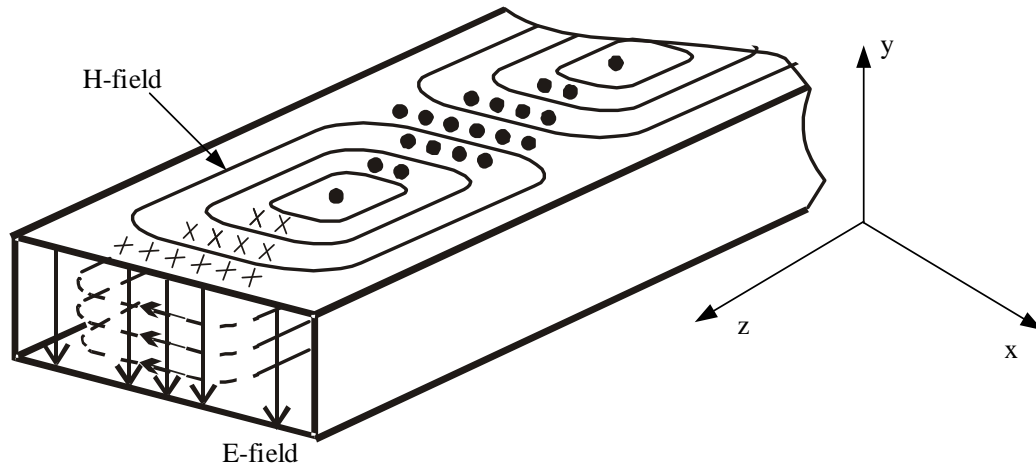
Figure 2.5: Electromagnetic field for TE_{10} mode of a rectangular waveguide.

an electric field in the slot. The position of the slot in the waveguide determines the current flow. Therefore, the position determines the impedance presented to the transmission line and the amount of energy coupled to the slot and radiated from the slot.

Figure 2.5 shows the electromagnetic field distribution for TE_{10} mode of a rectangular waveguide. The electric field is in $\pm y$ direction and its distribution is symmetrical about the centerline of the rectangular waveguide. The electric field component equation is shown in Table A.1 in the Appendix A. The current in the walls of the waveguide are proportional to the difference in electric field between any two points. Therefore, a slot in the exact center of the broad wall of the waveguide does not radiate as the electric field is symmetrical around the center of the waveguide as illustrated in Figure 2.5 and thus is identical at both edges of the slot. As the slot is moved away from the centerline, the difference in electric field intensity between the edges of the slot increases. This interrupts the flow of more current, which couples more energy to the slot and increases the radiated power. However, since the sidewalls are short circuits for the electric field, when a slot is placed too close to the sides of the waveguide, the electric field is very small and the induced current must also be small. Thus, longitudinal slots far from the center do not radiate significantly.

From the point of view of the waveguide, the slot is a shunt impedance, or an equiva-
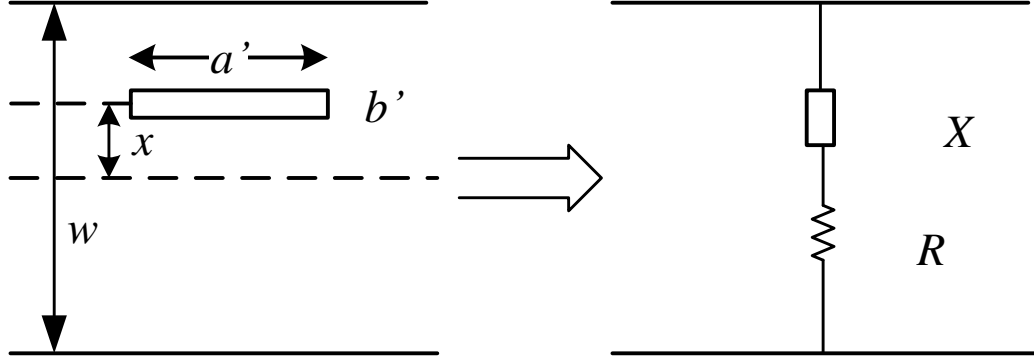
Figure 2.6: Longitudinal slot in a broad wall of rectangular waveguide equals to a shunt impedance across the transmission line.

lent admittance, across the transmission line loading the transmission line as illustrated in Figure 2.6. The following equation first obtained by A. F. Stevenson [57] indicates that the normalized conductance of a resonant longitudinal shunt slot in the broad wall of a rectangular waveguide is approximately equal to a constant times the square of the sine of an angle proportional to its offset

$$\frac{G}{G_0} = \left[2.09\frac{w/h}{\beta/k}\cos^2\left(\frac{\pi\beta}{2k}\right)\right]\sin^2\frac{\pi x}{w} \tag{2.5}$$

in which β is the propagation constant for the TE_{10} mode, k is the wave number, x is the offset from the center line of the broad wall, w and h are the width and height of the rectangular waveguide, respectively.

There is an assumption made when deriving Equation 2.5 that the network elements are purely real, the slot is resonant, and the length of the slot is near $\lambda/2$. A. A. Oliner re-developed the theory but now for any slot length [58] as

$$\frac{R}{Z_0} = \frac{8\pi w^3 h}{3\lambda^3\lambda_g} \cdot \frac{\left[1-\left(\frac{2a'}{\lambda_g}\right)^2\right]^2\left[1-0.374\left(\frac{a'}{\lambda}\right)^2+0.130\left(\frac{a'}{\lambda}\right)^4\right]}{\sin^2\left(\frac{\pi x}{w}\right)\cos^2\left(\frac{\pi a'}{\lambda_g}\right)} \tag{2.6}$$

where λ is the free space wavelength, λ_g is the guide wavelength, x is the offset of the slot from the center line of the rectangular waveguide, a' is slot length, and w and h are the

width and the length of the rectangular waveguide.

It was found that Equation 2.6 can be used directly in the analysis of dielectrically loaded waveguides as long as changing the following parameters:

$$
\begin{cases}
\lambda_g \implies \lambda_{g\varepsilon} = \dfrac{\lambda_0}{\sqrt{\varepsilon_r - \left(\frac{\lambda_0}{2w}\right)^2}} \\[3mm]
\lambda \implies \lambda_0
\end{cases}
\tag{2.7}
$$

where $\lambda_{g\varepsilon}$ is the guide wavelength in the dielectric, λ_0 is the wavelength in the free space, ε_r is the relative dielectric constant and w is the width of the rectangular waveguide, which also means that Equation 2.6 can be used for SIW.

2.4 Chapter Summary

After a comparison of the properties of THz antennas and a comparison of many antenna designs in CMOS process, this chapter identified a SIW slot antenna as the antenna technology that is capable of producing an efficient CMOS integrated antenna that does not require any post-processing. Then, the advantages of SIW structures comparing with conventional waveguides and planar circuits were discussed. Next, the SIW structure was presented and the reason for SIW supporting only TE_{m0} modes were explained. This was followed by the review of the principles of slot antenna operations, which included the Babinet's Principle and derivation of the impedance of longitudinal slot radiators.

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Chapter 3

46 GHz SIW Slot Antenna Design

As mentioned in Section 1.4, a 46 GHz SIW slot antenna is first designed, fabricated, and tested to verify the design concept, which is a down-scaled prototype of the 460 GHz SIW slot antenna. After a brief literature review in Section 3.1, a design of a 46 GHz SIW slot antenna is presented in Section 3.2. In Section 3.3 several parameters, which increase the gain of the antenna, are discussed. Section 3.4 explores the effect of the fabrication tolerances on the impedance of the antenna. Section 3.5 demonstrates the experimental results of the fabricated antenna and shows a good agreement with simulated results.

3.1 Brief Literature Review

To put this antenna in the context of previously published antennas operating in a similar frequency range, this chapter starts with a quick literature review of previously published antennas operating at frequency below 100 GHz as shown in Table 3.1.

A W-band SIW horn antenna was presented in [59], which was fabricated on a PCB and produced 1 GHz of bandwidth with a simulated gain of 9 dBi, fed by a $WR - 10$ waveguide. Another W-band SIW slot antenna with measured return loss of 20 dB was reported in [66]. [60] presented a 79 GHz SIW single slot, longitudinal slot array, and four-by-four antenna array using a flexible PCB process, which have achieved gains of 2.8 dBi, 6.0 dBi, and 11.0 dBi and bandwidths of 4.7%, 5.4% and 10.7%, respectively. In [61] a 94 GHz SIW 32×32 slot array was proposed with the maximal gain of 25.8 dBi and fed by WR-10 waveguides. A 27 GHz SIW H-plane horn antenna, a 1×4 horn array and a 1×8 horn array were fabricated on PCB process and tested to achieve gains of 5.75 dBi, 13.75 dBi and 15.65 dBi, respectively [64]. [62] presented a 4×4 SIW slot array antenna at X-band with a bandwidth of 0.6 GHz and a gain of 15.7 dBi. An X-band dual-slot broadband SIW antenna was presented in [63]. The antenna has a bandwidth of 8.5%, the maximum gain

Table 3.1: Comparison of SIW Antennas.

Ref.	Process	Antenna Type	Frequency (GHz)	-10 dB BW	Gain (dBi)	Efficiency
[59]	PCB	SIW horn	84	1.2%	9	-
[60]	FPCB	SIW slot	79	4.7%	2.8	47%
		1×4 slot array		5.4%	5.8	43%
		4×4 slot array		10.7%	11.1	38%
[61]	PCB	32×32 slot array	94	-	25.8	75%
[62]	PCB	4×4 SIW slot array	10	6%	15.7	-
[63]	PCB	SIW dual-slot	10	8.5%	8.1	75%
[64]	PCB	SIW H-plane Horn	27	-	5.8	-
		1×4 SIW H-plane Horn array		-	13.8	-
		1×8 SIW H-plane Horn array		-	15.7	-
[65]	PCB	2×2 patch array	12.5	10%	13.6	73%
		2×4 patch array		12%	16.7	73%
		4×4 patch array		11.5%	19.5	70%
		8×8 patch array		13%	24	50%

of 8.14 dBi and efficiency of 75%. [65] reported SIW cavity-backed microstrip patch arrays of 2×2, 2×4, 4×4, and 8×8 with measured gains of 13.6 dBi, 16.65 dBi, 19.46 dBi and 24 dBi at 12.5 GHz, respectively. [67] presented an X-band SIW leaky-wave antenna with transverse slots, which supports a leaky mode, a proper waveguide mode, and a surface-wave mode, depending on the frequency region.

3.2 46 GHz SIW Slot Antenna Design

First, SIW was designed for the SIW slot antenna. A thickness of 10 mil Rogers RT/duroid 5880 was chosen for the substrate, which has a dielectric constant ε_r of 2.2 and loss tangent of 0.0009. The SIW structure simulated in HFSS is shown in Figure 3.1. The final dimensions of the SIW are presented in the last four rows of Table 3.2. As discussed in Section 2.2, a SIW can be equivalent to a conventional dielectric-filled rectangular waveguide. From Equation 2.1, the width of the equivalent rectangular waveguide is selected as
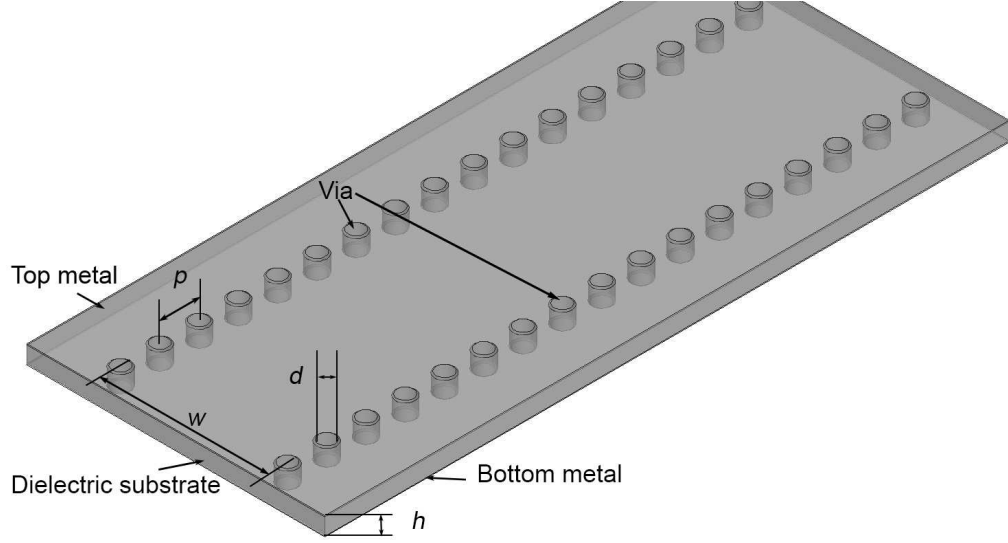
Figure 3.1: Configuration of a SIW.

2.48 mm, which has a cutoff frequency of 41.1 GHz for the dominant mode (TE_{10}). This cut-off frequency is sufficiently low to propagate the desired 46 GHz signal but also sufficiently high to reduce antenna width and prevent other propagation modes. The simulated S_{11} and S_{21} of the SIW are shown in Figure 3.2.

In the HFSS simulation, a wave port was setup to excite the antennas shown in Figure 3.3. An integration line from the center of the bottom plane to the center of the microstrip, also shown in Figure 3.3, defines the port impedance. The width of the wave port is 5 times the width of the microstrip and the height of the wave port is 10 times of the height of the substrate. There is an air box around the antenna to define the radiation boundary, which is one wavelength away from the antenna surfaces.

In this design, the slot length is chosen to be approximately a half wavelength in free space ($a' = 0.48\lambda$). The final antenna layout is shown in Figure 3.4. Also the dimensions of the antenna are listed in Table 3.2. The resulting normalized resistance of the shunt resistor $R/Z_0 = 0.85$ computed from Equation 2.6 demonstrated in the previous chapter. This means the equivalent resistance of the slot matches that of the SIW.

The top view of the SIW antenna fed by the microstrip is shown in Figure 3.4. The distance between the shorted end wall and the slot of a integer multiple of a one-quarter
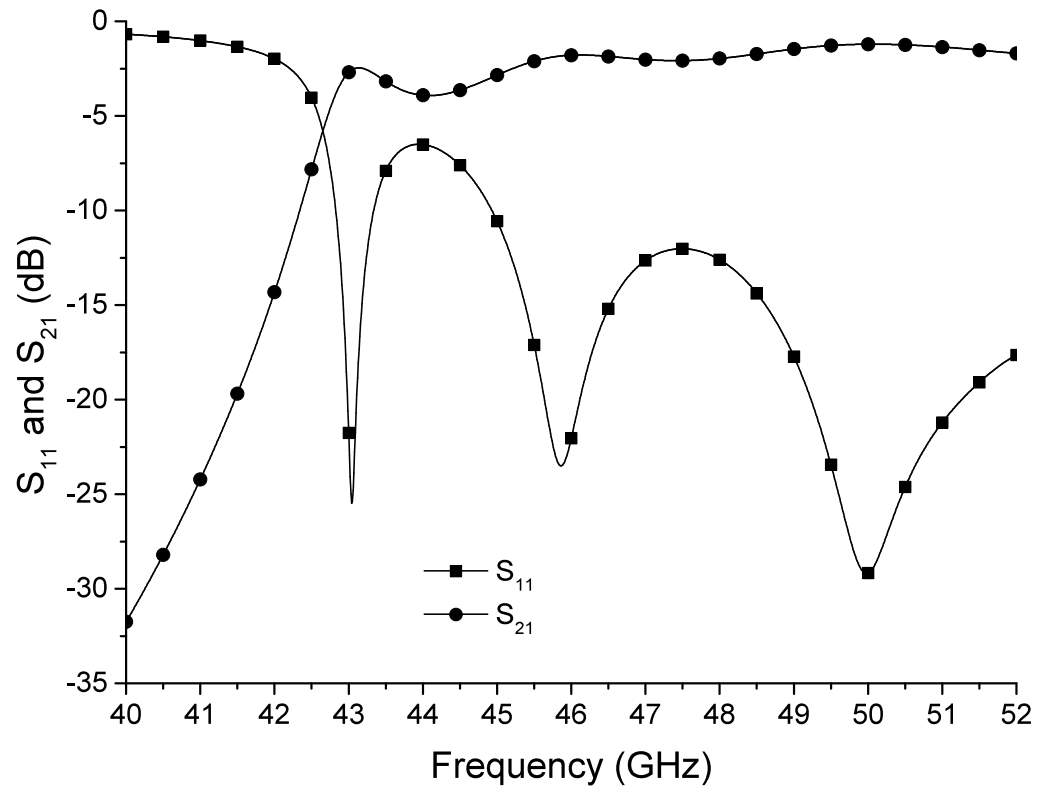
Figure 3.2: Simulated S_{11} and S_{21} of the SIW.
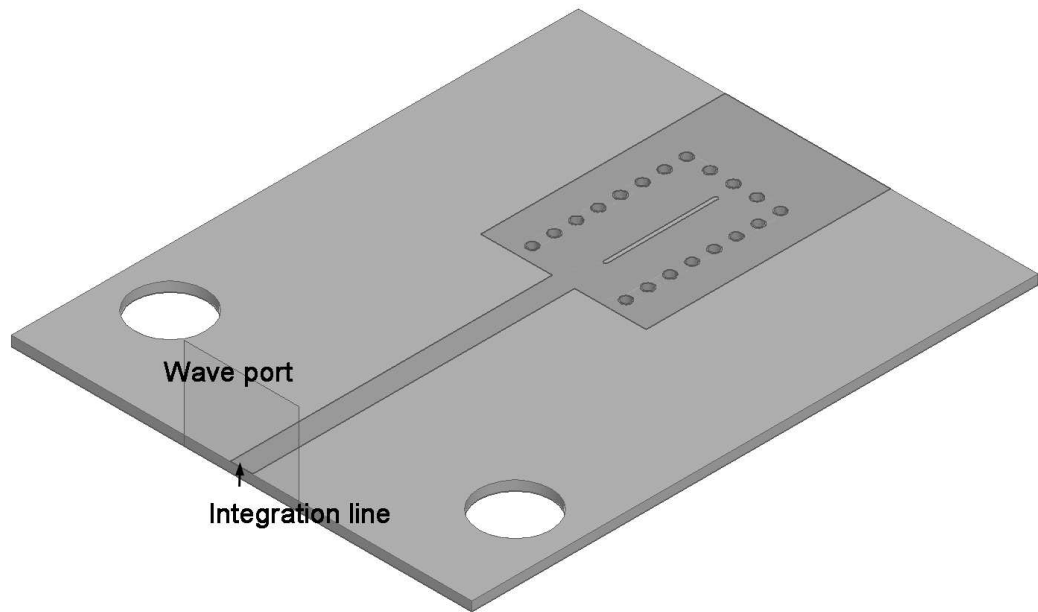
Figure 3.3: Excitation for the HFSS simulation.
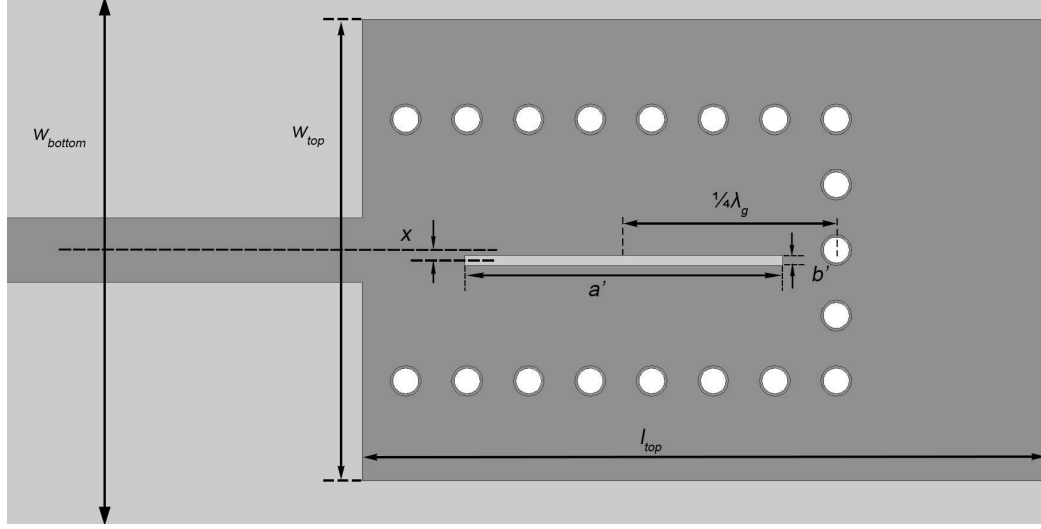
Figure 3.4: Top view of the SIW slot antenna and the microstrip feedline.

Table 3.2: Antenna dimensions of the 46 GHz SIW slot antenna.

Variable	Dimensions (mil)
Slot offset x	4
Slot length a'	124
Slot width b'	4
Top metal length l_{top}	266
Top metal width w_{top}	180
Bottom metal width w_{bottom}	500
Via diameter d	12
Via spacing p	24
SIW width w	102
Substrate thickness h	10

wavelength is needed, in most publications three-quarter wavelength was used because of the fabrication limitation. In this design, the cutoff frequency is close to the operating frequency and the dielectric constant of the substrate is low, thereby making the guide
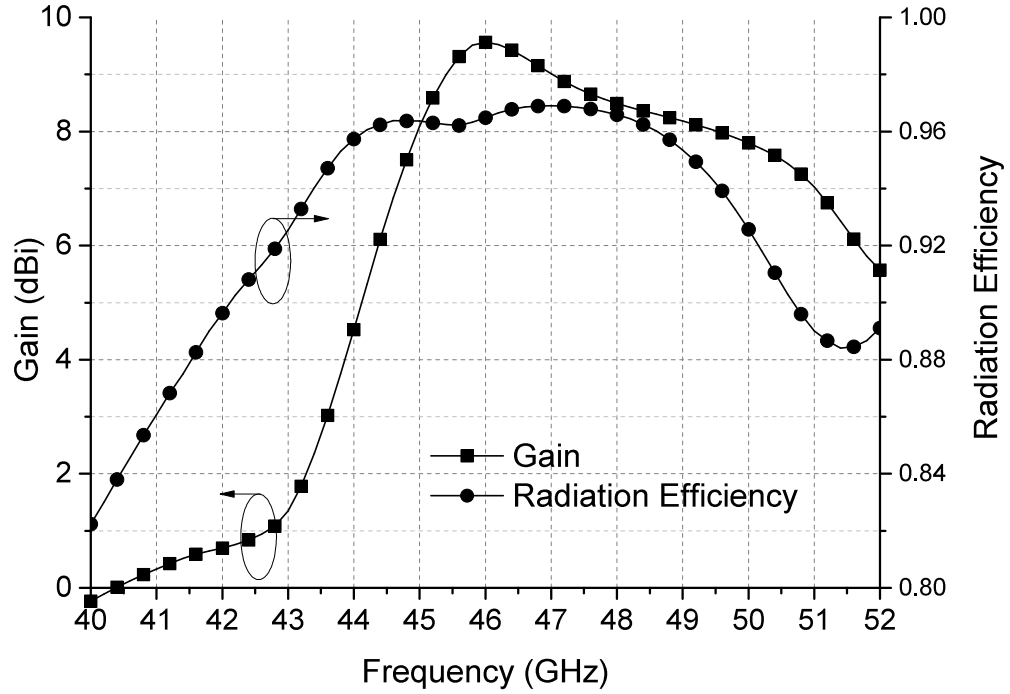
Figure 3.5: Simulated peak gain and radiation efficiency of the SIW slot antenna.

wavelength larger than the free space wavelength and permitting the fabrication of a quarter wavelength spacing. The simulated peak gain and radiation efficiency from HFSS are presented in Figure 3.5. In the frequency range from 45 GHz to 49 GHz the peak gain of the antenna is over 8 dBi and the radiation efficiency is more than 95%.

3.3 Factors Improving the Antenna Gain

The width of the top metal w_{top} affects the antenna radiation significantly as shown in Figure 3.6. Figures 3.6 (a) and (b) give the E-plane and H-plane radiation patterns with different widths of the top metal layer w_{top} at 46 GHz. When w_{top} is 180 mil and the width of bottom metal w_{bottom} is 500 mil, the antenna has a maximal gain of 9.6 dBi, which is 7.6 dB higher than for $w_{bottom} = 134$ mil due to the radiation from the longitudinal edges of the top metal generated by the leaking currents through the gaps between adjacent vias. Figure 3.7 shows the surface currents of the antenna, which prove that there are some

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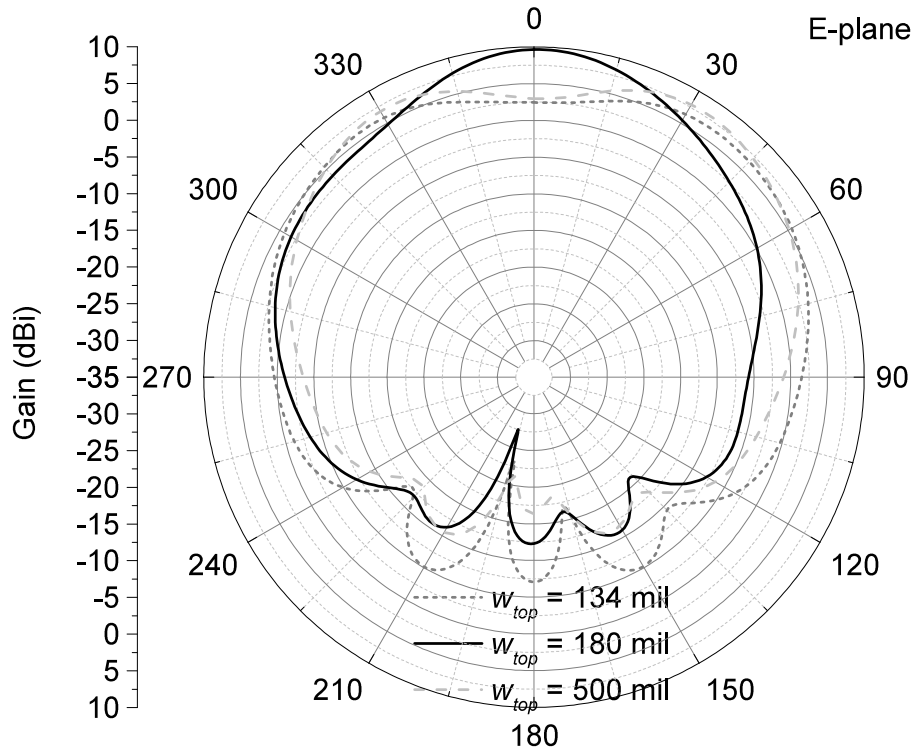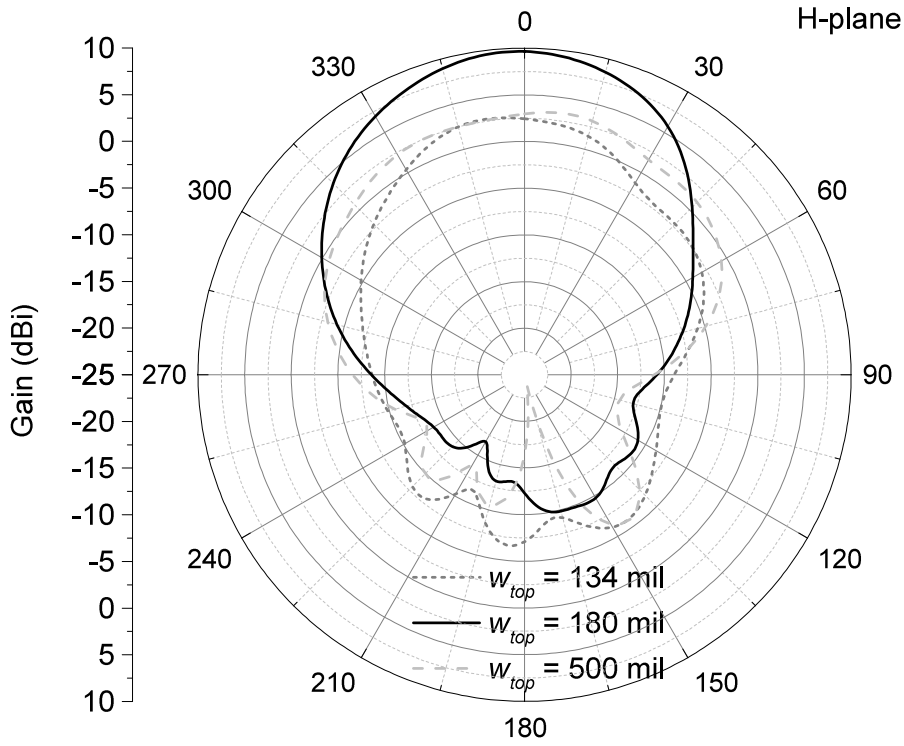
Figure 3.6: Simulated radiation pattern for varying width of top metal at 46 GHz. (a) E-plane. (b) H-plane.
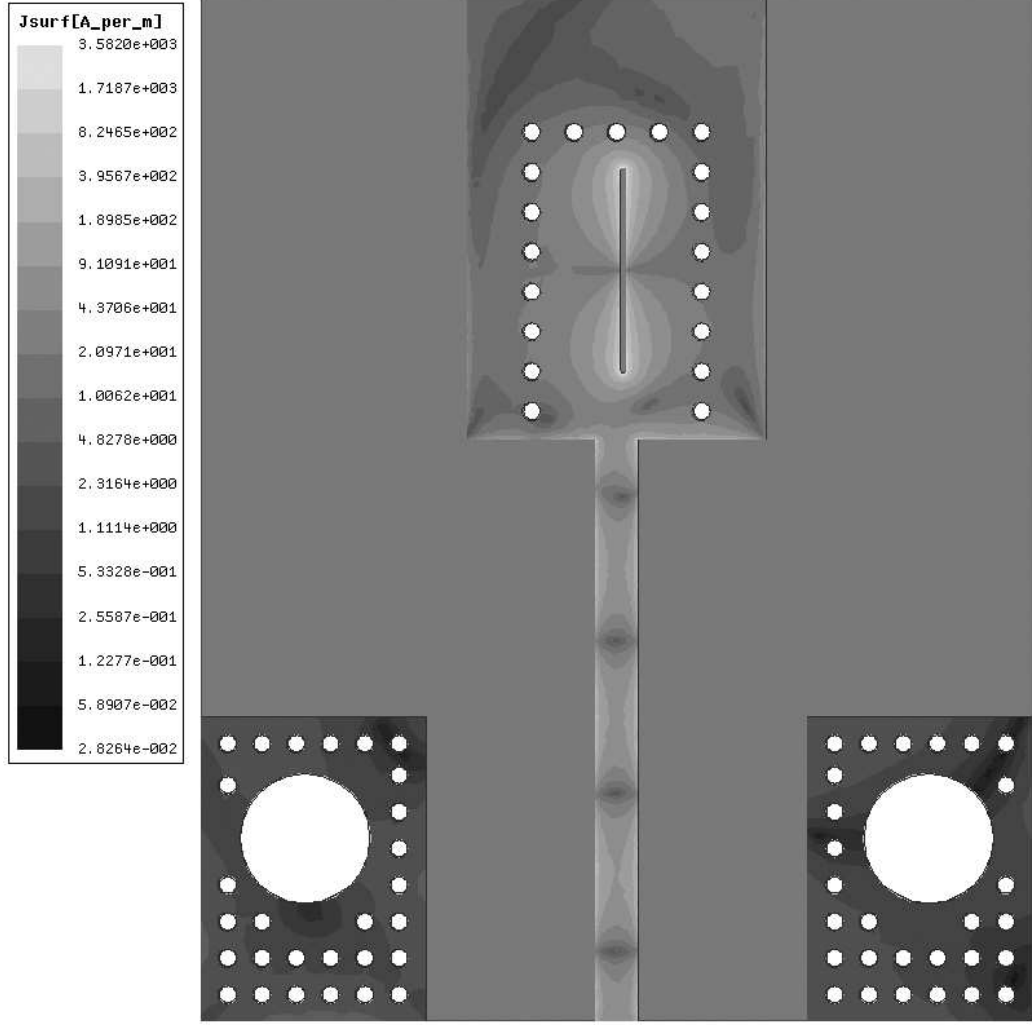
Figure 3.7: Surface currents of the proposed antenna from HFSS.

currents flowing out of the SIW and radiating at the longitudinal edges of the top metal. The front-to-back ratio is 19.6 dB due to the large ground plane ($w_{bottom} = 500$ mil), which provides good isolation for keeping radiation from back. As shown in Figure 3.6, the back lobe decreases when the width of top metal increases.

Another important factor, which affects back lobe, is the width of bottom metal w_{bottom}. The comparison of the back lobes for different widths of the bottom metal w_{bottom} is illustrated in Figure 3.8. Although the back lobe splits from one lobe into three small lobes in the E-plane as the width of ground plane increases, for the large ground plane the back lobe decreases by 10 dB and the main lobe increases by 4 dB when compared to an antenna with
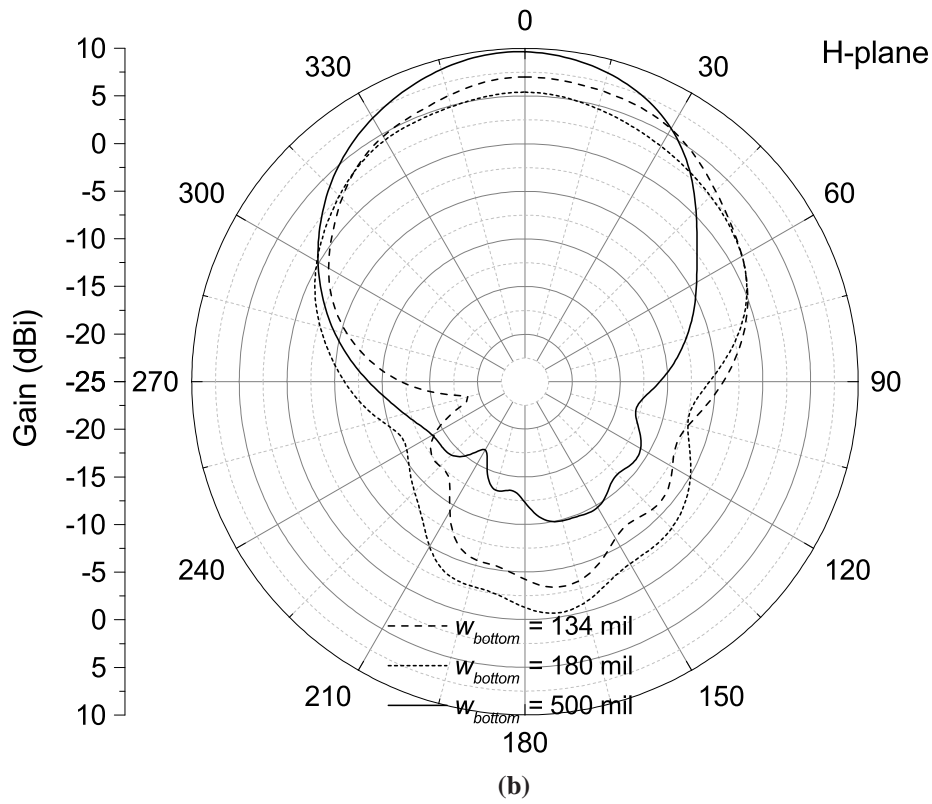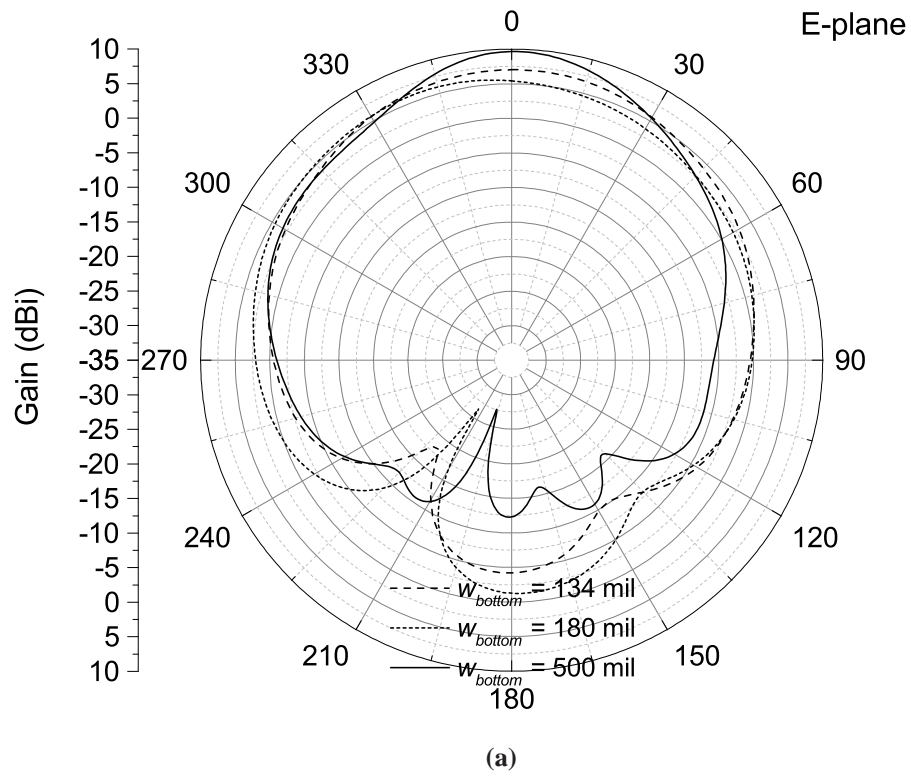
Figure 3.8: Simulated radiation pattern for varying width of the ground metal at 46 GHz.
(a) E-plane. (b) H-plane.
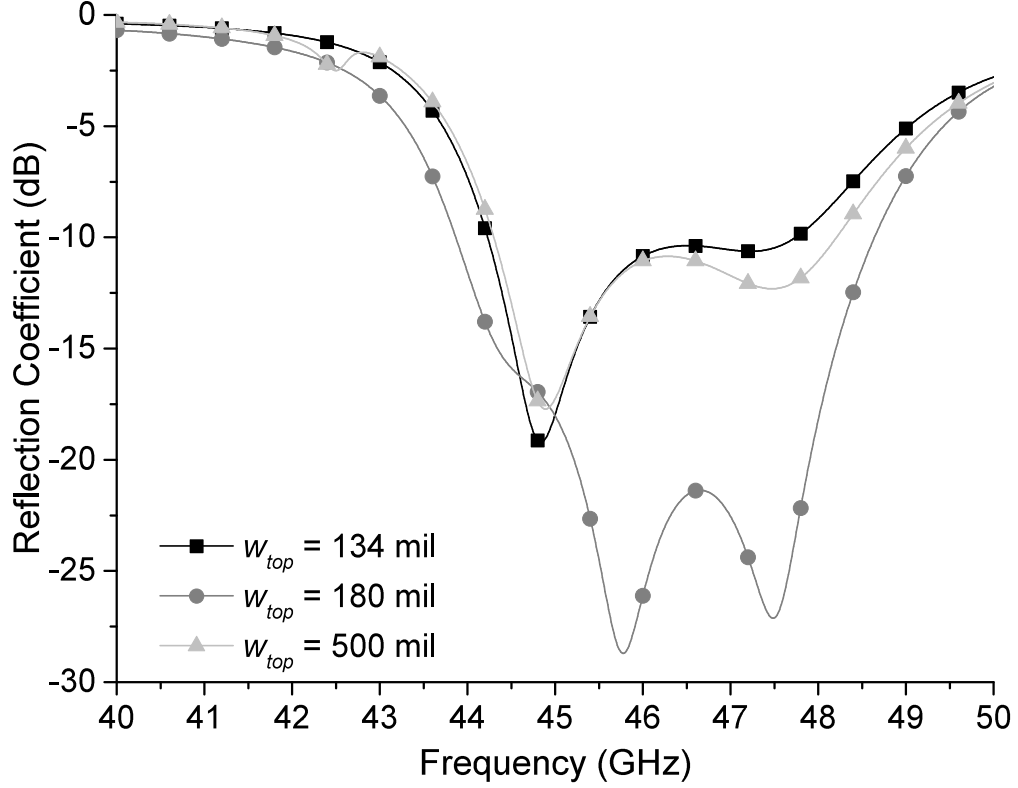
Figure 3.9: Simulated reflection coefficients of the SIW antennas with different widths of top metal.

$w_{bottom} = 180\,\text{mil}$.

The width of top metal w_{top} also affects the reflection coefficient of the SIW slot antenna as shown in Figure 3.9. One difference between a traditional waveguide slot antenna design and a SIW slot antenna design is that there is an extension area of the top and ground metals beyond sidewalls or the vias. This extension area is usually ignored in SIW slot antenna designs. The large ground plane is able to compress the back lobe as presented in Figure 3.8. Proper dimensions of the top metal result in higher gain and better impedance matching as illustrated in Figure 3.6 and 3.9.

3.4 Fabrication Tolerance Test

The PCB manufacturer may have as much as a $\sim 5\,\text{mil}$ error on the via placement. This error was observed from previous PCBs fabricated by the same PCB fabrication facility.
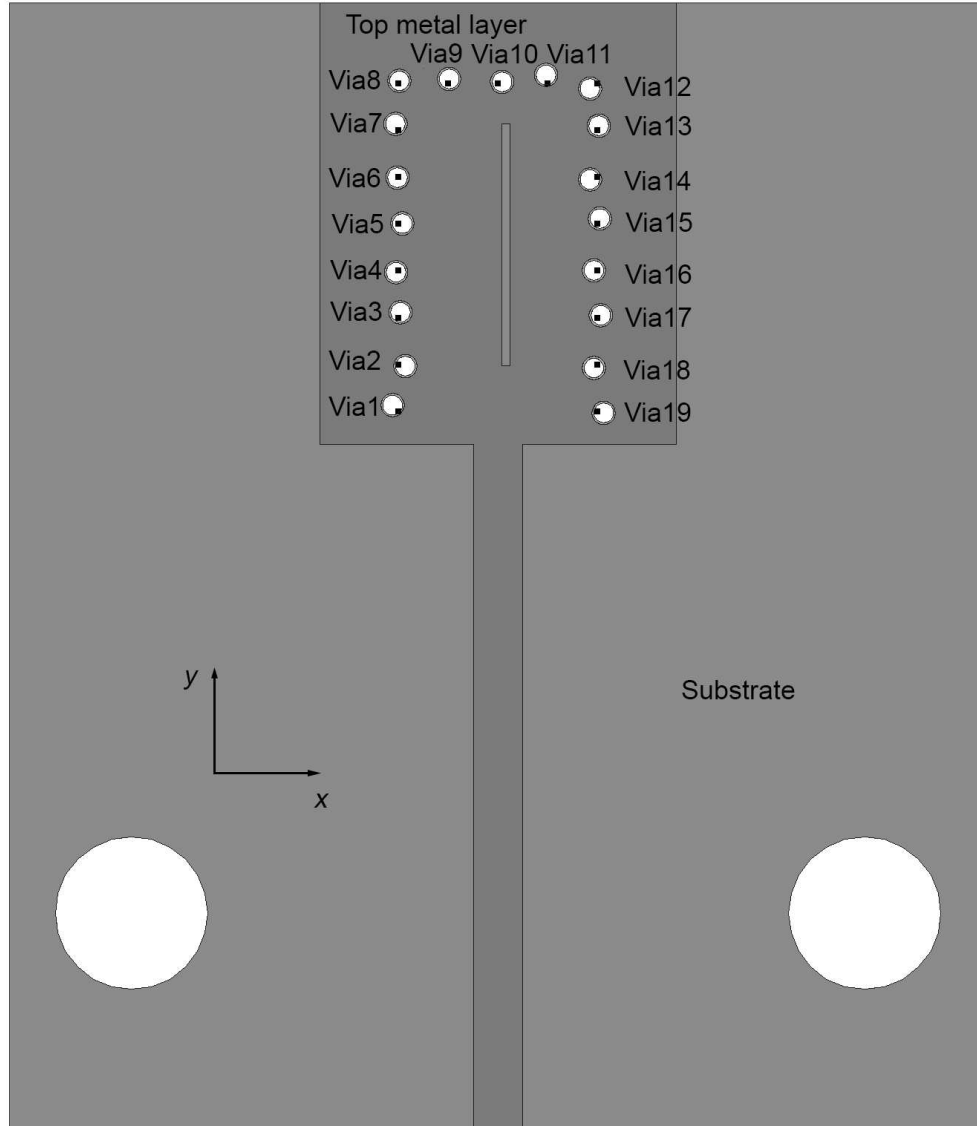
Figure 3.10: Top view of the simulation model for via fabrication tolerance. The black square dot is the center of the original via.

Therefore, some simulations were done to investigate the influence of the fabrication errors on the antenna performance. In the simulations, each via was located with a random offset within 5 mil range in both horizontal and vertical directions. Figure 3.10 shows the top view of the PCB modeled in HFSS. The black square dot is the center of the original via. The set-up data for each via is presented in the Table 3.3. Figure 3.11 compares the simulated S_{11} of the original antenna with antennas with offset vias . As can be seen, antennas whose
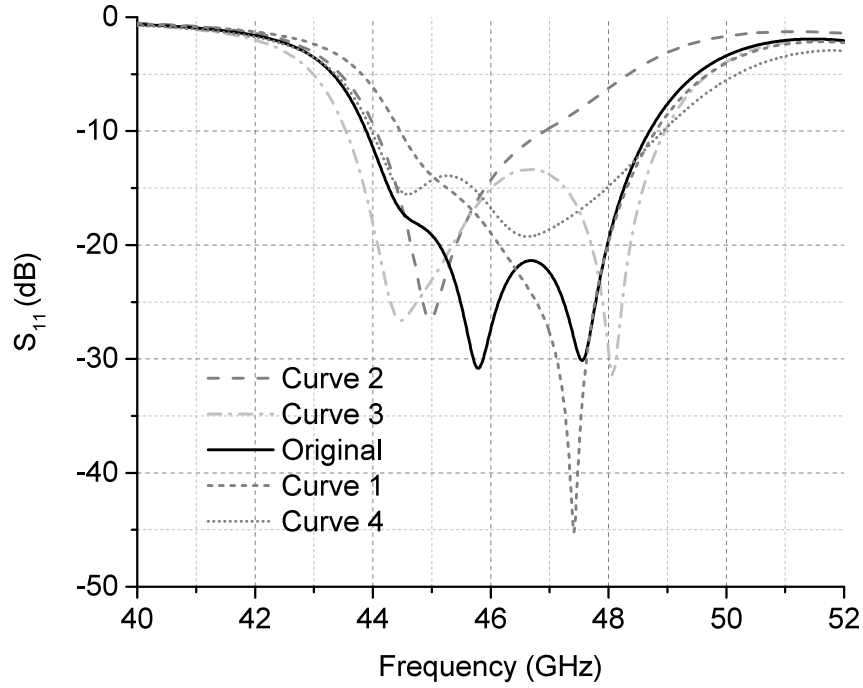
Figure 3.11: S_{11} of different via offset of the SIW slot antenna.

S_{11} is represented by curve 3 and 4 have larger bandwidths, whereas antennas with S_{11} represented by curve 1 and 2 have smaller bandwidths. However, at 46 GHz all curves exhibit S_{11} of better than -10 dB and therefore it was assumed that the antenna would not be significantly affected by fabrication tolerances.

3.5 Experimental Performance of the Antenna

The photographs of a fabricated antenna are shown in Figure 3.12. The width and length of the PCB are 500 mil and 616 mil, respectively. The antenna is fed by a microstrip with the width of 25 mil and length of 350 mil. The dark gray substrate in the Figure 3.12(a) is the 10-mil-thick RT/duroid 5880 substrate. There are two extra solid-ground copper layers on a FR4 substrate attached to the bottom of the antenna to increase the thickness and stiffness of the antenna. These two copper layers are connected to the antenna ground with vias. A photograph of the bottom ground plane is shown in Figure 3.12(b). All vias are through
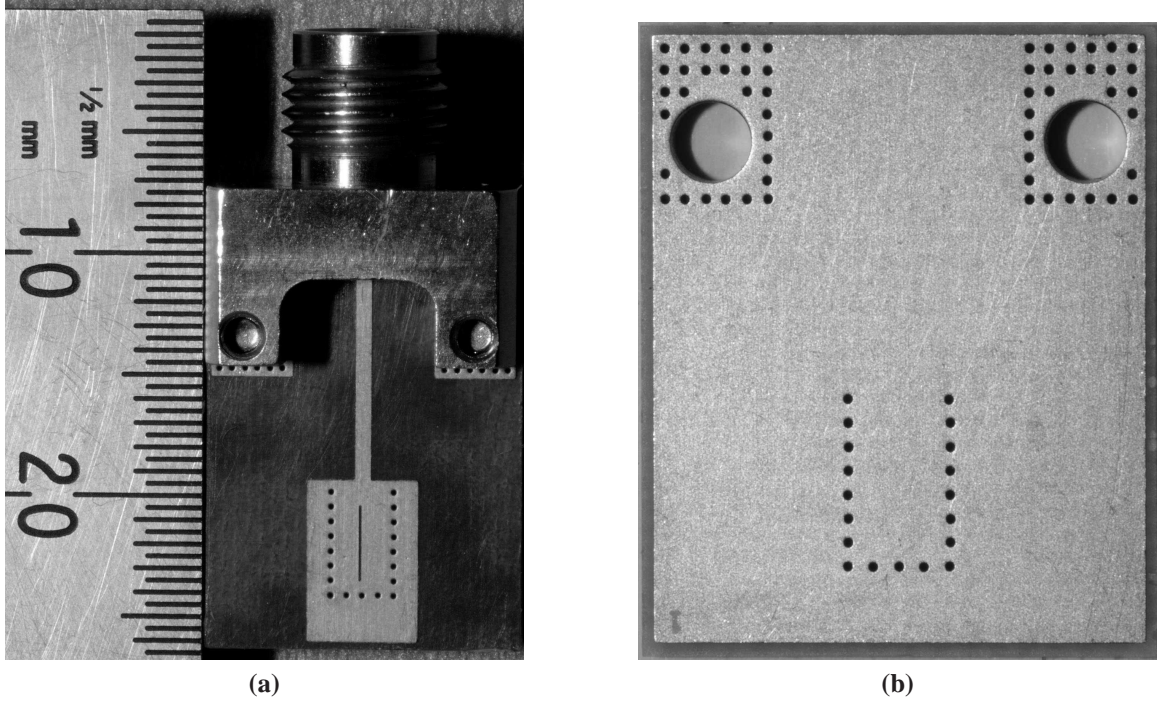
Figure 3.12: Photographs of the fabricated SIW slot antenna. (a) Top view. (b) Back view.

holes from top layer to bottom layer. The total thickness of the PCB is 62 mil. A 2.4-mm RF connector as shown in Figure 3.12(a) was used for measurements. The measured and simulated S_{11} are shown in Figure 3.13. The measurements were performed with an R&S ZVA67 vector network analyzer (VNA). The -10 dB S_{11} bandwidth was measured as 4.72 GHz from 43.08 GHz to 47.80 GHz, which is close to the simulated bandwidth of 4.80 GHz. The measured S_{11} shows a 0.9 GHz frequency shift comparing with the simulations. This discrepancy is likely because of fabrication tolerances and the presence of the connector, which was not included in the simulations.

The radiation pattern was measured on both E-plane and H-plane from 43 GHz to 47 GHz to compare with the simulated results as shown in Figure 3.14. Theoretically, the E-plane and H-plane radiation patterns at 0° are identical. Due to measurement errors, the measured E-plane and H-plane radiation patterns at 0° have small difference as shown in Figure 3.14, which is acceptable. However, from 45.2 GHz to 46.1 GHz the measured antenna gain shows same drastic ups and downs in E-plane and H-plane and co- and cross-
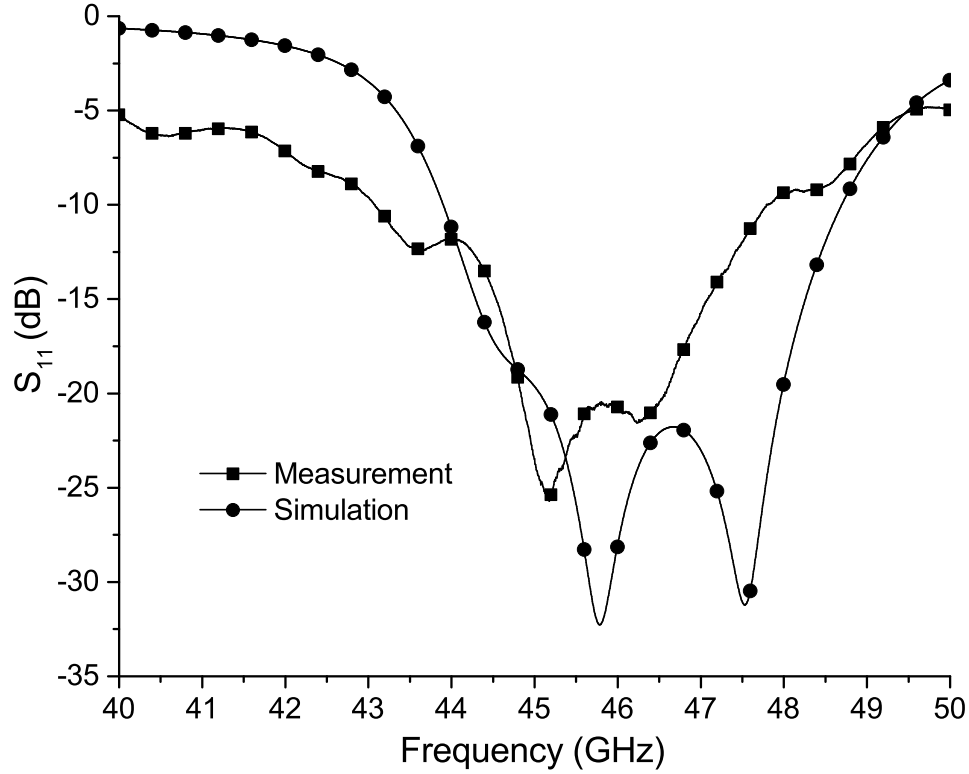
Figure 3.13: Simulated and measured S_{11} of the antenna.

polarizations. Since the measurements were conducted at Jean-Jacques Laurin laboratory at École Polytechnique de Montréal, it was not possible for us to determine the exact cause for these anomalies. However since antenna does not have highly resonant structures that could cause such a drastic variation in the antenna gain, these anomalies are attributed to measurement errors.

The test was performed in azimuth. The feed antenna (the source) was placed on a rotary actuator. There were two scans for each frequency. For the first scan E-field of the feed antenna was oriented vertically, and for the second scan the E-field was oriented horizontally. Two antennas were tested: a standard gain horn antenna and the 46 GHz SIW slot antenna. By comparing the measured gain of the standard gain horn antenna and the gain from the data sheet, the difference of the gain was obtained. Adding the difference to the 46 GHz antenna measurement results, the gain of the 46 GHz was calculated. For the 46 GHz SIW slot antenna measurement, the antenna (the slot) was placed vertically
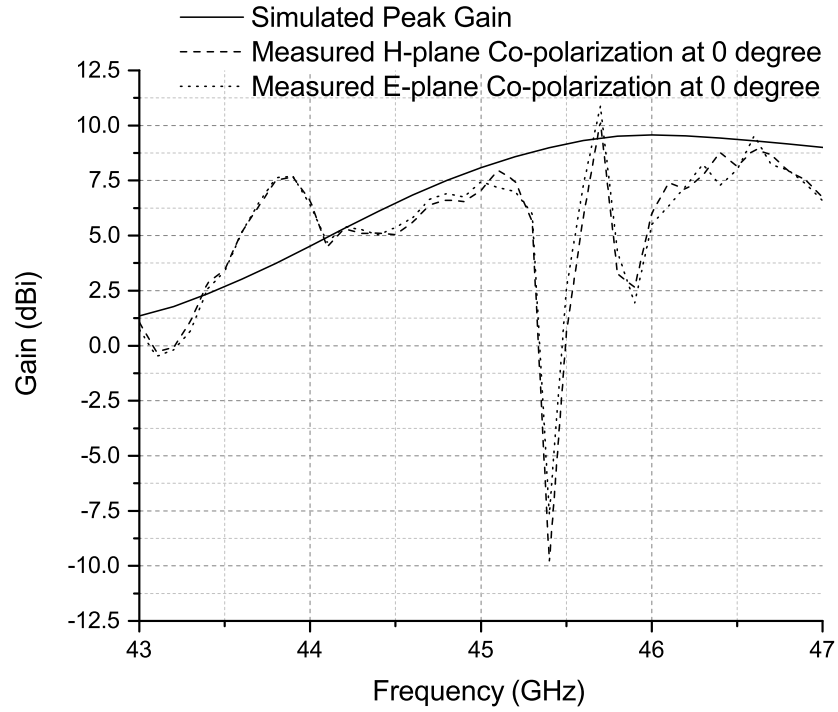
(a)
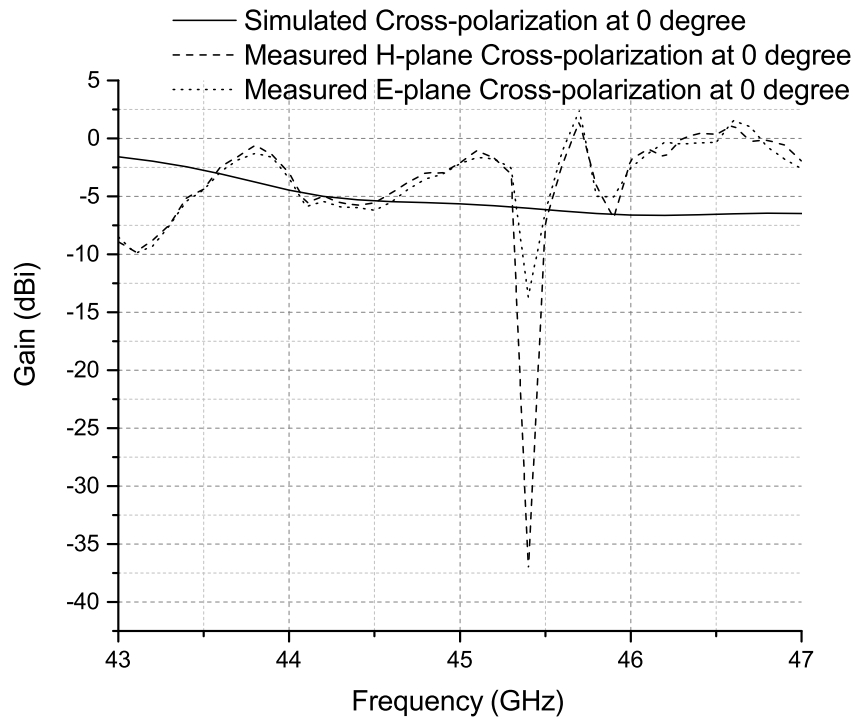
(b)

Figure 3.14: Simulated and measured antenna gain from 43 GHz to 47 GHz. (a) Co-polarization. (b) Cross-polarization.

first. After measuring all frequencies, the antenna was rotated to horizon position around the center of the slot. The measurement was repeated at all frequencies again. Finally the E-plane and H-plane co-polarization and cross-polarization were obtained.

The frequency range from 45.2 GHz to 46.1 GHz was skipped in the following discussion. The measured co-polarization gains agree with the simulated ones except from 45.2 GHz to 46.1 GHz as shown in Figure 3.14 (a). However, Figure 3.14 (b) shows that the measured cross-polarization gain is larger than the simulated result above 44.5 GHz. To find the reason why the cross-polarization gains are higher than the simulation, the radiation patterns at 46.2 GHz were studied. The antenna achieved the measured gain of 7.8 dBi at 46.2 GHz while simulated gain was 9.6 dBi. The simulated and measured E-plane and H-plane radiation patterns for co-polarization and cross-polarization are shown in Figure 3.15 and 3.16, respectively. In Figure 3.15 (a) the HPBWs are 45° and 63° for simulated and measured co-polarization patterns, respectively. Meanwhile, in Figure 3.15 (b) the HPBWs are 56° and 63° for simulated and measured co-polarization patterns, respectively. There is a good agreement between the measured co-polarization radiation pattern and simulated patterns for both E-plane and H-plane. Ripples can be found in the measurements, especially in the angular regions where the radiation is weak. These are likely due to reflections in the test setup. The 2.4-mm RF connector was found to increase the cross-polarization in both the H-plane and the E-plane significantly as illustrated in Figure 3.15. In HFSS a short coax cable and the connector were modeled and simulated with the antenna model, which consists of four layers of copper as shown in Figure 3.17. In Figure 3.16(b) the cross-polarization gain is 10 dB higher than the simulated gain of the antenna without the connector in the H-plane below -60° region, where the connector blocks the radiation of the antenna. Moreover, in the E-plane the cross-polarization gain is about 5 dB higher as compared to the simulated cross-polarization gain from the antenna without the connector. The measured cross-polarization gain and the simulated gain with the connector agree well. From this, it is concluded that the real cross-polarization of the antenna without the
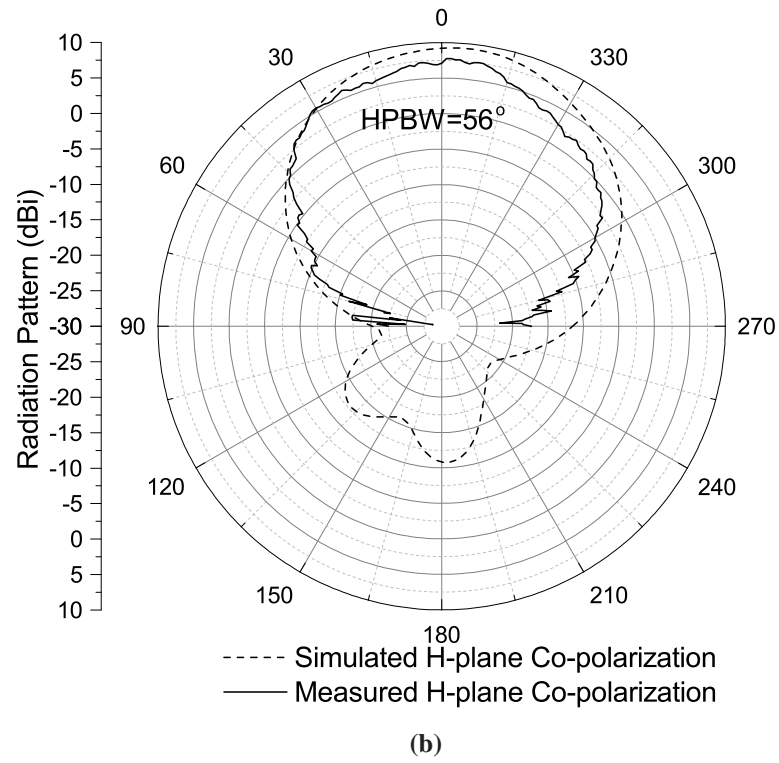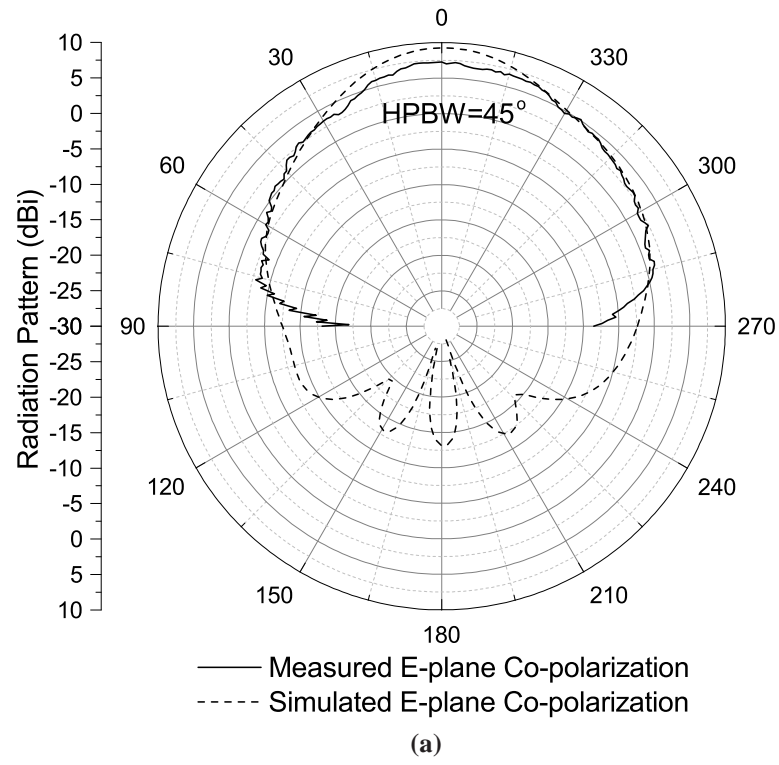
Figure 3.15: Simulated and measured co-polarization radiation patterns at 46.2 GHz. (a) E-plane. (b) H-plane.
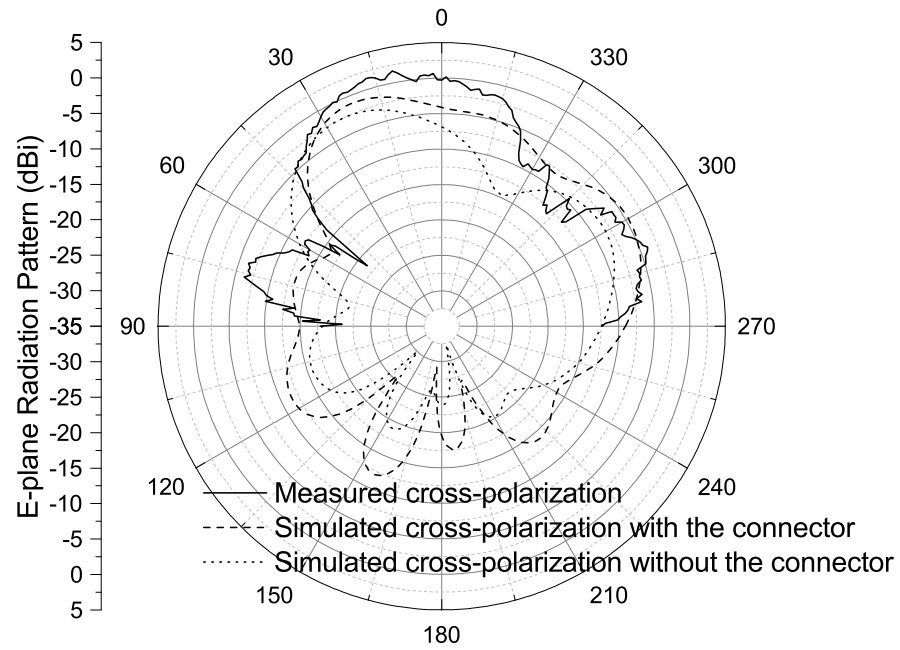
(a)
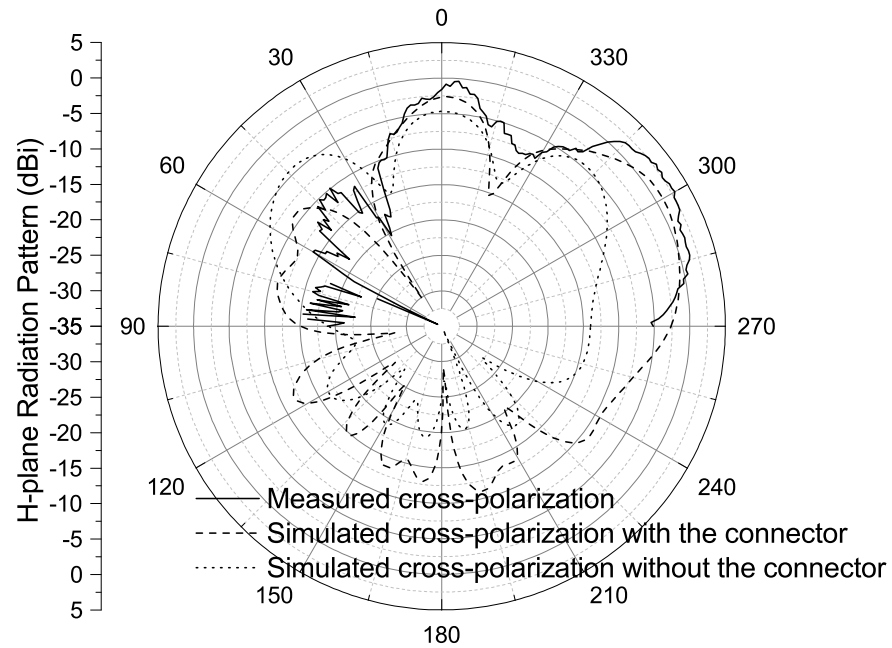
(b)

Figure 3.16: Simulated and measured cross-polarization radiation patterns at 46.2 GHz. (a) E-plane. (b) H-plane.
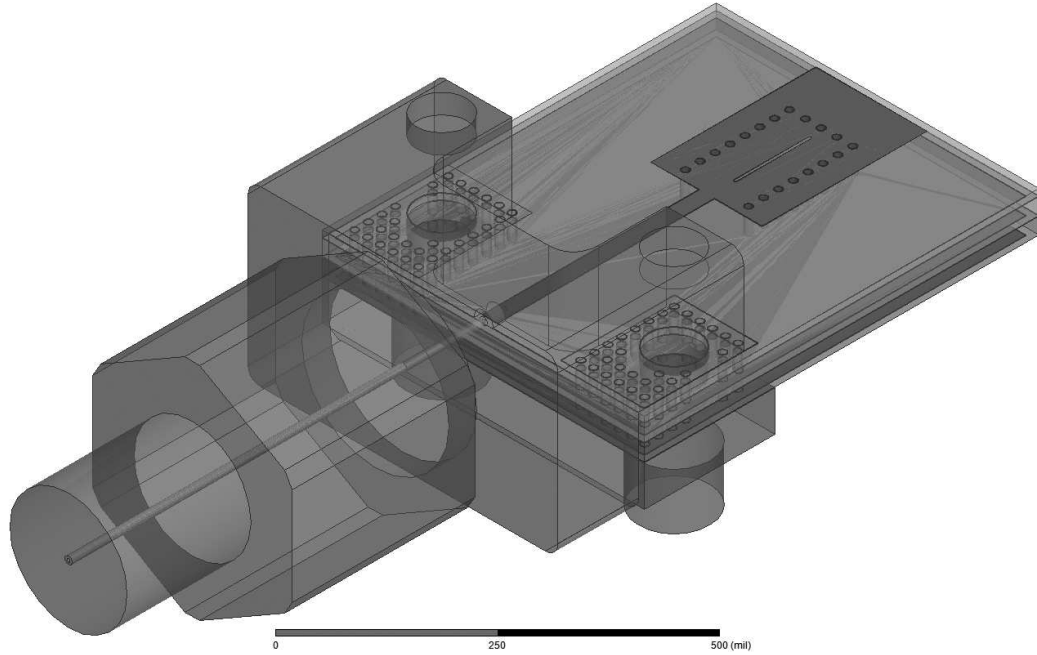
Figure 3.17: The antenna with a connector and a short piece of coax cable simulated in HFSS.

connector is expected to be close to the simulated results of only the antenna.

The antenna performance summary and comparison with other SIW antennas is given in Table 3.4.

3.6 Conclusion

The design and experimental results of the 46 GHz broadband high-gain SIW slot antenna are presented in this chapter. The antenna has a -10 dB S_{11} bandwidth of 4.80 GHz from HFSS simulation, which agrees with the measured bandwidth of 4.72 GHz. The simulated gain is 9.6 dBi and the simulated efficiency is 96% at 46.2 GHz. The measured gain is 7.8 dBi at 46.2 GHz. The measured antenna pattern agrees with the simulations. Comparing with other SIW slot antennas, this antenna has a larger bandwidth and a higher gain due to the optimized dimensions of top metal and the large ground metal. It was found that properly selected dimensions of the top and bottom metal are important to achieve high gain and large front-to-back ratio.

Table 3.3: Vias offset from original coordinates in the simulations.

Via #	Test 1 offset		Test 2 offset		Test 3 offset		Test 4 offset	
	x (mil)	y (mil)	x (mil)	y (mil)	x (mil)	y (mil)	x (mil)	y (mil)
Via1	0	3	-1	1	-1	2	3	3
Via2	0	-2	1	-2	-3	3	-1	-3.5
Via3	0	3	1.5	4	-5	0	2.5	-1
Via4	0	-3	3	-0.5	-1	3	-1	1.2
Via5	0	-2	-2	-2	3	0.5	0	-2
Via6	0	1	0	3	-1	-2	-0.5	0.5
Via7	0	3	-1.5	-1	1.5	-3	3	1.5
Via8	0	0	-3	0	1.5	4	1	-0.5
Via9	0	0	2	3	-1.5	-1	2	-0.5
Via10	0	0	0.5	1.5	-3.5	0	0.5	-2
Via11	0	0	3.5	1	-2	-1.5	4	1
Via12	0	0	-1	-2	-2	3	-3	4
Via13	0	2	4	-2	1	-3.5	2	-0.5
Via14	0	-3	0	0.5	2.5	-1.5	-1.5	4
Via15	0	3	-3	-2	-1	0	2.5	-1
Via16	0	-1	3	-1	1	-2	0	2
Via17	0	1	1.5	-4	-1	4	1	-1.5
Via18	0	-3	1.5	1	-3	-2	-2	2
Via19	0	2	-2	-3	1.5	2	-1	-3

Table 3.4: Performance summary and comparison of SIW antennas.

Reference	[59]	[60]	[63]	**This work**
Process	PCB	FPCB	PCB	**PCB**
Antenna Type	Horn	Slot	Dual-slot	**Slot**
Frequency	84 GHz	79 GHz	10 GHz	**46 GHz**
Bandwidth	1.2%	4.7%	8.5%	**10.3%**
Gain	9 dBi*	2.8 dBi	8.14 dBi	**7.8 dBi**
Efficiency	-	47%*	75%	**96%***

* Simulated

Chapter 4

460 GHz CMOS SIW Slot Antenna Design

In the previous chapter, a 46 GHz PCB SIW slot antenna was designed and tested to verify the design procedure. Since that design demonstrated good agreement between the simulated and measured results, it was concluded that the design concepts were proven. This chapter first describes the 65 nm CMOS process design-rule restrictions and the way to minimize the restrictions for the SIW slot antenna design in Section 4.1. Sections 4.2 and 4.3 present the 460 GHz SIW slot antenna design and the simulated results, respectively. At last, Section 4.4 analyzes the antenna efficiency and loss mechanisms with a simulation in which different loss mechanisms are implemented.

4.1 65 nm CMOS Process Design-Rule Restrictions

In order to facilitate integration with the entire receiver, the 460 GHz SIW slot antenna was designed in a TSMC (Taiwan Semiconductor Manufacturing Company) 65 nm CMOS process. Figure 4.1 shows the cross-section of the TSMC 65 nm process metalization and dielectric layers. There are 10 metal layers in 65 nm process: M1, M2,···, M10. M10 is an aluminum layer and all other layers are copper layers. Also, there are 9 different vias connecting the adjacent metal layers. For example, Via1 connects M1 and M2. In addition, there are 35 dielectric layers: D0, D1···, D34. Some layers are very thin, about several $10^{-2}\,\mu$m thick. Figure 4.1 shows 4 different gray colors for the dielectric layers, which stand for 4 different dielectric constants of the 35 dielectric layers. M1 and M10 are selected to be the top and bottom metals of the SIW respectively. The SIW via-walls comprise of the via stack from M1 to M10. The side view of vias model in HFSS is shown in Figure 4.2.

An SIW layed out in a CMOS process is somewhat different from other processes due to limitations imposed by the CMOS technology design rules. In particular, the CMOS

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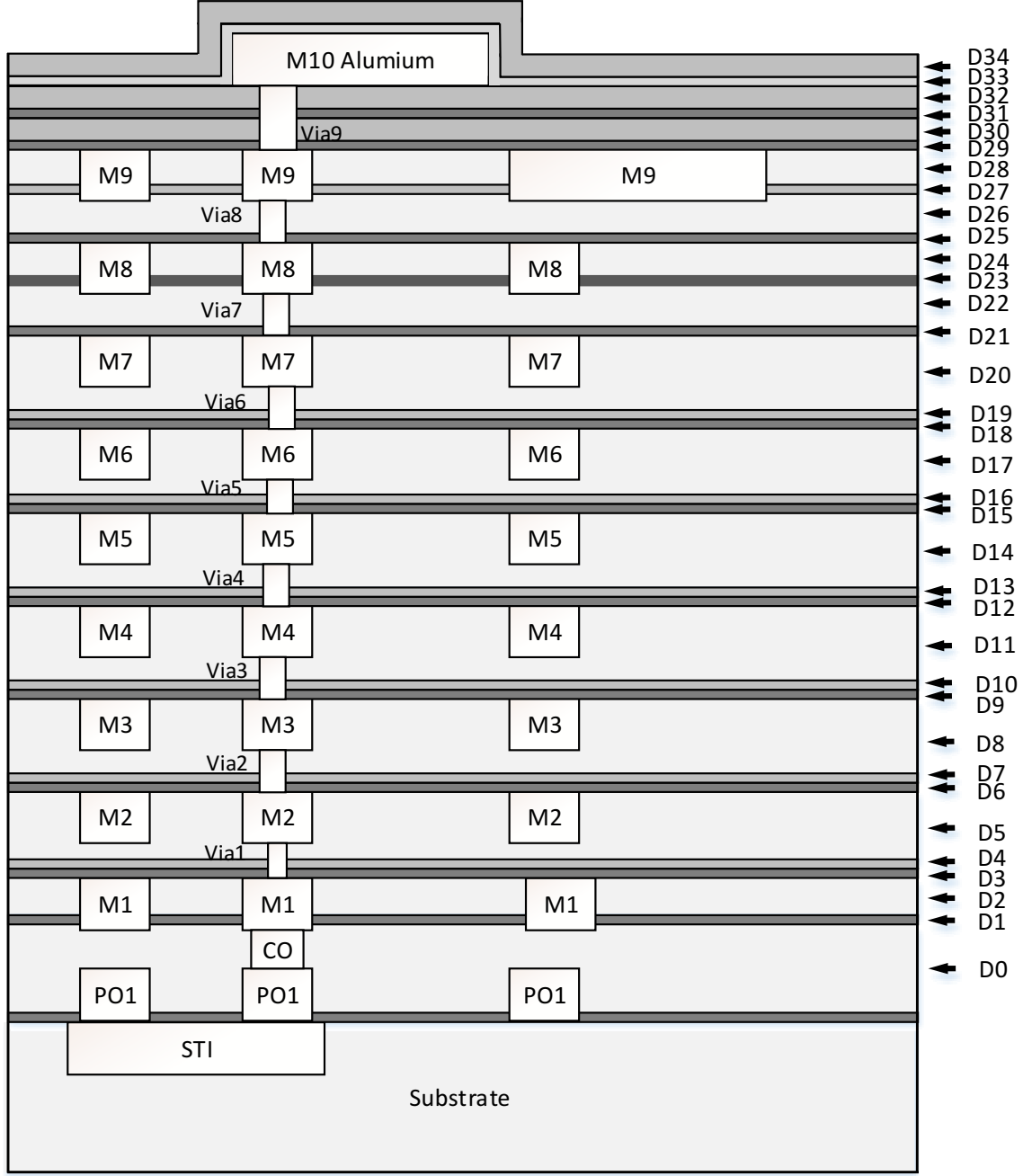
Figure 4.1: A schematic cross-section of TSMC 65 nm process. Different grayscale shows different dielectric constant for the dielectric layers (D0-D34).

metal density rules significantly impact the SIW design. The maximum metal density of M1 is 80% in each $100\,\mu m \times 100\,\mu m$ window, in steps of $50\,\mu m$. To satisfy the maximum metal density rules, square holes ($10\,\mu m \times 10\,\mu m$, spacing $10\,\mu m$) were created in the M1 as shown in Figure 4.3 (a). The reduced M1 density to 76.2% over the whole antenna area.
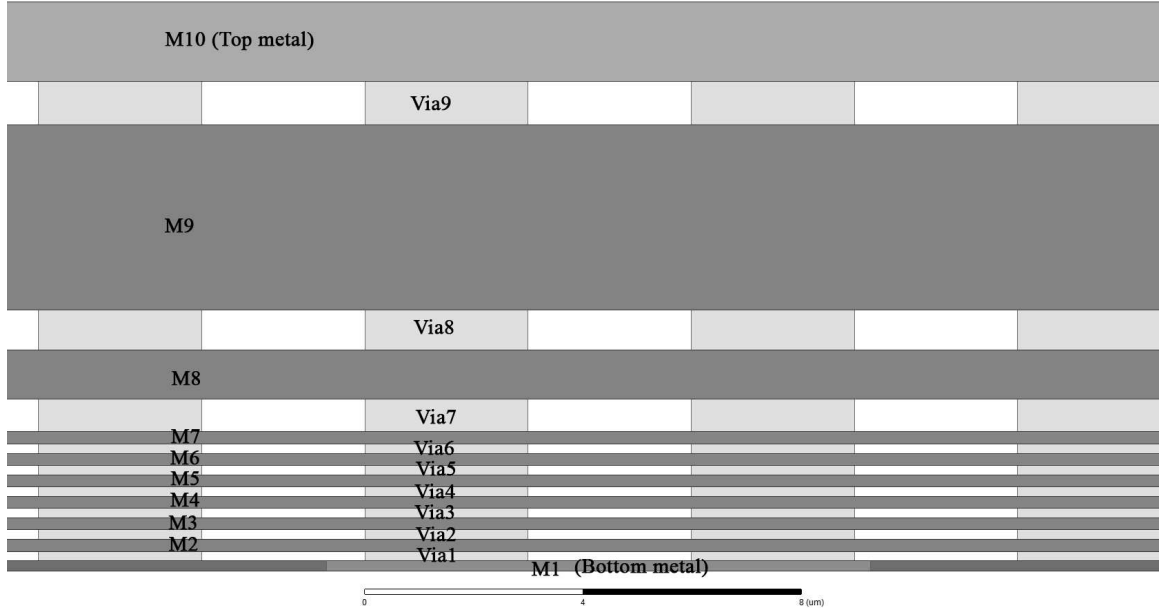
Figure 4.2: Side view of vias.

For the internal metal layers $(M2 - M9)$ a minimum metal density is 10% in each $75\,\mu\text{m} \times 75\,\mu\text{m}$ window, in steps of $37.5\,\mu\text{m}$. In this case when this rule is not satisfied with a given layout, some small "dummy" metals have to be placed on the M2 to M9 layers to increase the metal density and pass the minimum density requirements. Since inside of a SIW the metal density is ideally zero, some extra "dummy" metals have to be added in the final layout of the SIW antenna. The "dummy" metals in the SIW dielectric do not only change the SIW dielectric constant but also increase the complexity of the simulation model. To reduce the impact of the "dummy" metals, the antenna was identified as an inductor. This is done with a special identification layer that tells TSMC that some of the design rules can be relaxed. In most RF designs, inductor layouts are covered with such an identification layer to keep their self-resonance frequencies as high as possible by reducing the amount of metal under inductors. In this work also to reduce the internal metal $(M2 - M9)$ density requirements, most of the SIW slot antenna was defined as an inductor using the inductor identification layer as shown in Figure 4.3 (b). In the final design there

are 95 pieces of "dummy" metals ($3\,\mu$m $\times$ $3\,\mu$m, spacing $12\,\mu$m) placed on each of 8 metal layers M2 to M9 as shown in Figure 4.3 (b). In the antenna layout, displayed in Figure 4.4, this inductor identification layer is shown to cover most of the antenna area. With this, in the final antenna layout, the metal density for the internal layers including the "dummy" metals and vias is only 5.2%. More specifically, the density of "dummy" metals is only 0.7% in the SIW instead of the minimum requirement of 10%.

The slot is cut in the M10 layer, which is the top metal that does not have to follow strict metal density. However, there are two dielectric layers above M10 in the TSMC 65 nm CMOS process as shown in Figure 4.1. Although they can be removed above M10 by identifying the top layer as a bondpad, in the slot where M10 is removed the two dielectric layers remain. Figure 4.5 shows the cross-section of the SIW slot antenna. The two dielectric layers are thinner than metal M10, so the antenna slot is not completely filled by the dielectric. The slot antenna can be considered as a dielectric-covered antenna.
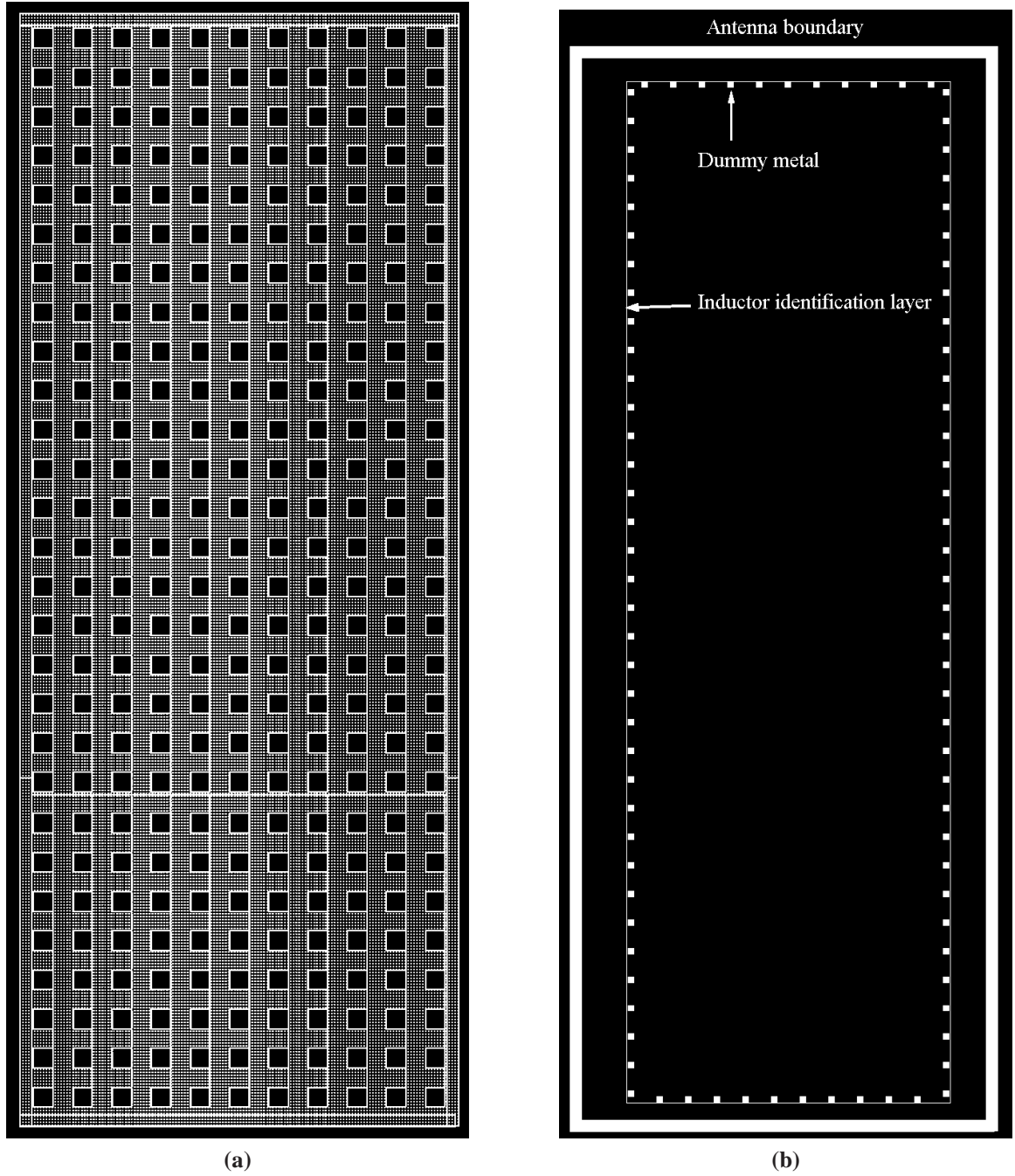
Figure 4.3: (a) Layout of M1 layer with 308 square holes. (b) The inductor identification layer and 95 pieces of square dummy metals ($3\,\mu$m $\times$ $3\,\mu$m, spacing $12\,\mu$m) filled in the antenna.
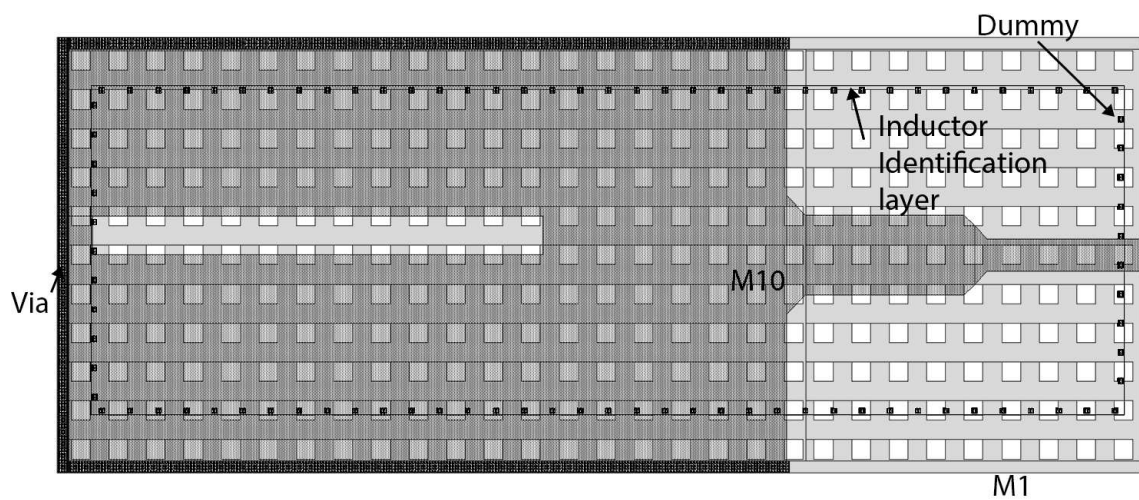
Figure 4.4: Top view of the antenna layout generated in Cadence.
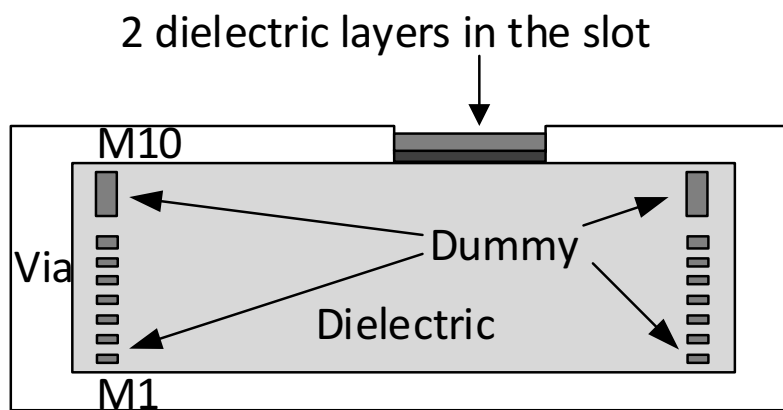
Figure 4.5: Cross-section of the SIW slot antenna.

Table 4.1: Cutoff frequencies of the rectangular waveguide.

Mode	Cutoff Frequency (GHz)
TE_{10}	351.7
TE_{20}	703.4
TE_{01}	8587
TE_{11}, TM_{11}	8595

4.2 Antenna Design

The TSMC CMOS process limits and sets some design parameters. One of them is the height of the SIW, which has to be the thickness between M1 and M10 metal layers. The maximum size of the via (Via9) is $3\,\mu m \times 3\,\mu m$. The minimum space ($3\,\mu m$) between Via9 is selected in the design of the SIW. With these, a SIW can be designed by using Equation 2.1, from which the width of the equivalent rectangular waveguide was calculated. The width (w) and height (h) of the SIW are $215\,\mu m$ and $8.805\,\mu m$, respectively. The dielectric of the SIW is so thin that the width of $215\,\mu m$ allows the SIW to support the presence of only a single mode (TE_{10}). The cutoff frequencies of different modes in the equivalent rectangular waveguide are given by Equation 4.1:

$$f_{c_{mn}} = \frac{c}{2\pi\sqrt{\varepsilon_r}}\sqrt{\left(\frac{m\pi}{w}\right)^2 + \left(\frac{n\pi}{h}\right)^2} \tag{4.1}$$

where c is the speed of light in free space, ε_r is the dielectric constant of the dielectric filled in the waveguide, w and h are the width and height of the rectangular waveguide, and $m,n = 0,1,2\cdots$. Table 4.1 demonstrates the cutoff frequencies of the TE and TM modes for the equivalent rectangular waveguide of the SIW. The simulated propagation constant (γ) for the first two modes are shown in Figure 4.6. The cutoff frequencies are $354.6\,GHz$ and $709.5\,GHz$ for TE_{10} mode and TE_{20} mode, respectively, which are very close to the

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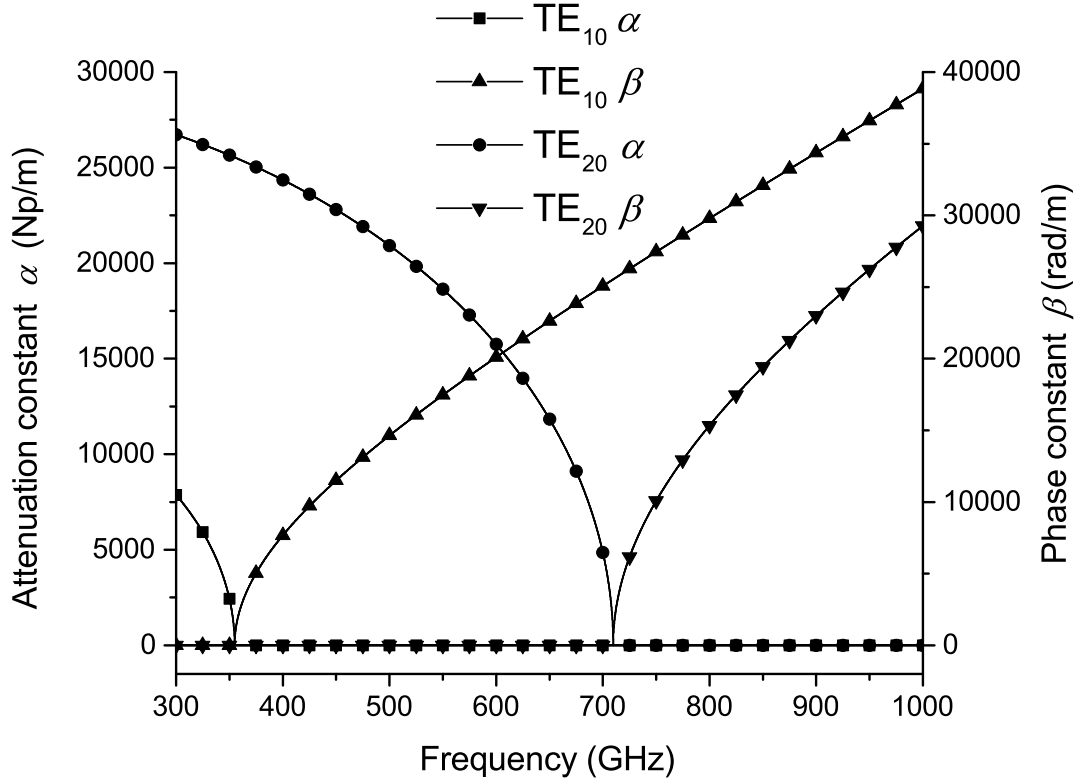
Figure 4.6: Simulated propagation constant (γ) of the TE_{10} and TE_{20} mode. The real parts (attenuation constant α) are the lines with squares (TE_{10}) and circles (TE_{20}), respectively. The imaginary parts (phase constant β) are the lines with up triangles (TE_{10}) and down triangles (TE_{20}), respectively.

theoretical value listed in Table 4.1.

To save space and reduce the cost of the IC, it is better to design a small on-chip antenna. A shorter slot results in a small area of the antenna not only because of the slot itself, but also because the distance between the slot center and the end of SIW needs to be a quarter of the guide wavelength as shown in Figure 4.7. If the slot was a half of the guide wavelength, the slot would interact with the end of the SIW perturbing the operation of the antenna.

For the SIW in the TSMC 65nm CMOS process, the guide wavelength of $501\,\mu$m was calculated from the equation in Table A.1 in Appendix A. For a dielectric-filled guide, the
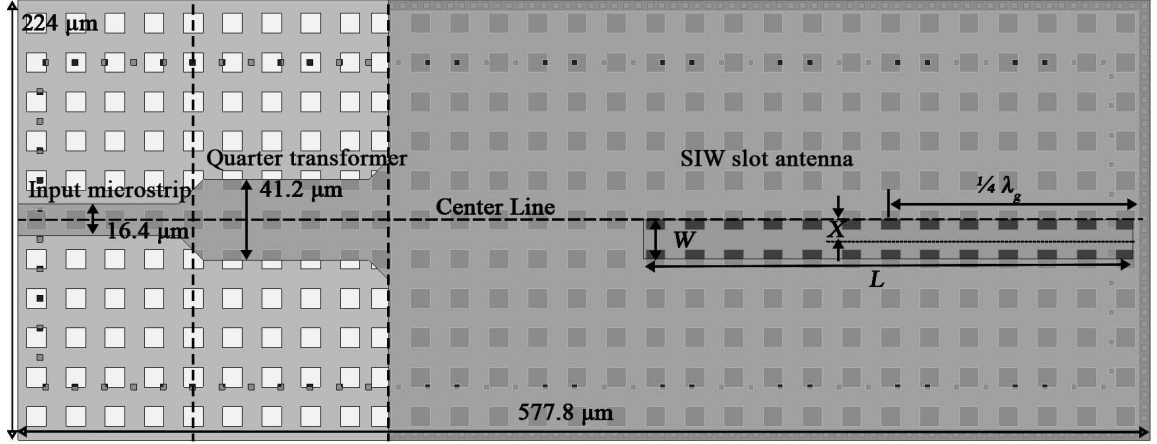
Figure 4.7: Top view of the SIW slot antenna.

slot length can be approximated by [68]:

$$L = \frac{\lambda_0}{\sqrt{2(\varepsilon_r + 1)}} \tag{4.2}$$

Although comprehensive theory has been developed for dielectric-covered antenna since 1960s [69, 70], this design is a little different as: the dielectric is inside the slot and does not cover the top of the slot as shown in Figure 4.5. Instead, a numerical method was used to analyze the antenna in this work. Figure 4.8 compares the S_{11} of the SIW slot antenna with and without dielectric in the slot. The figure demonstrates that the dielectric in the slot reduces the resonance frequency of the antenna. In addition, the comparison of radiation patterns are shown in Figure 4.9, which give the same conclusion as in [71]: in the E-plane patterns it is evident that the dielectric in the slot reduces the normal electric field component along the surface ($\theta = 90^{\circ}$ and 270°), and in the H-plane the presence of the dielectric has very small overall effect.

The top view of the antenna in HFSS is shown in Figure 4.7. The antenna model consists of 3 parts: a $50 - \Omega$ microstrip, a quarter-wave transformer, and the SIW slot antenna. The SIW slot antenna part was designed first. The distance between the center of the slot and the end of SIW is a quarter-guide wavelength. Three parameters: the length
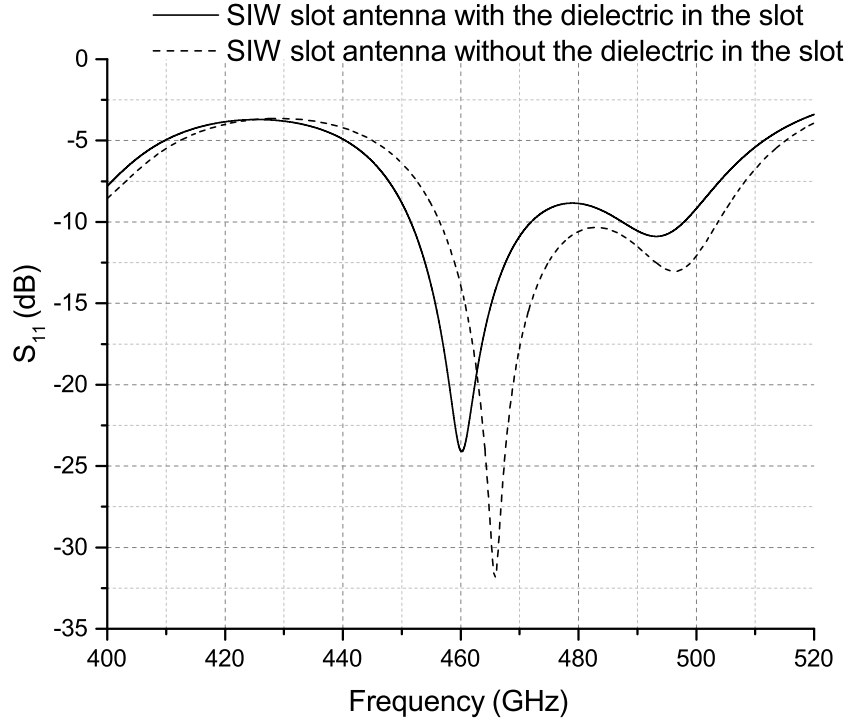
Figure 4.8: Comparison the S_{11} of the SIW slot antenna with and without dielectric in the slot.

of the slot L, the width of the slot W, and the displacement of the slot from the center line of the SIW X are important for the design. The comparison of S_{11}s for different sizes and positions of the slot are shown in Figures 4.10, 4.11, and 4.12. These three figures illustrate that the resonant frequency increases when the slot length gets shorter, the width gets wider, or the slot gets more offset from the center line. This conclusion is used to optimize the impedance matching for the SIW slot antenna.

The characteristic impedance of the SIW slot antenna is $15 + j0.14\,\Omega$ at $460\,\text{GHz}$ from HFSS simulation as shown in Figure 4.13. It agrees with the theoretical result of the characteristic impedance of the SIW

$$Z_{SIW} = \frac{h}{w} \frac{465}{\sqrt{\varepsilon_r - \left(\frac{\lambda_0}{2w}\right)^2}} \tag{4.3}$$

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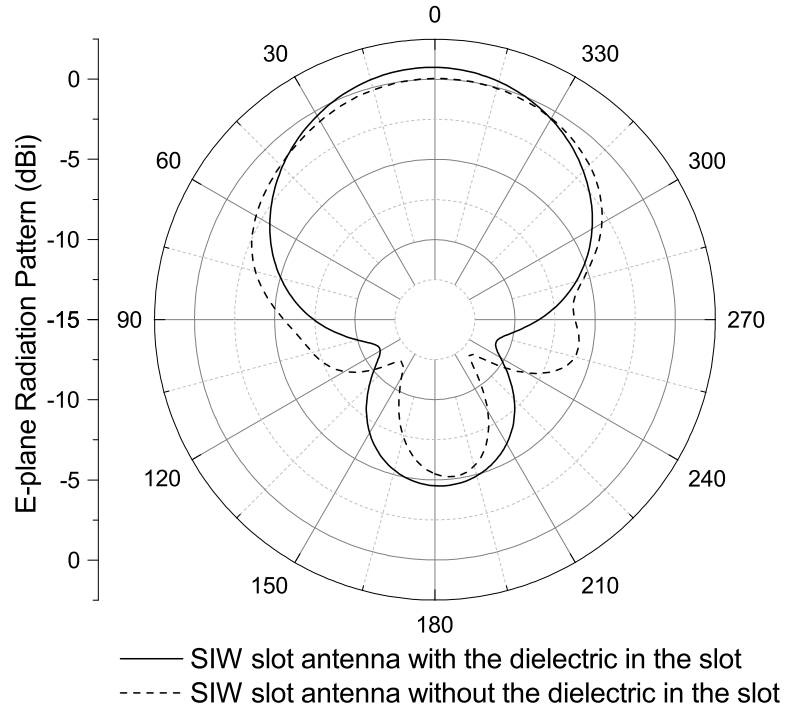
(a)
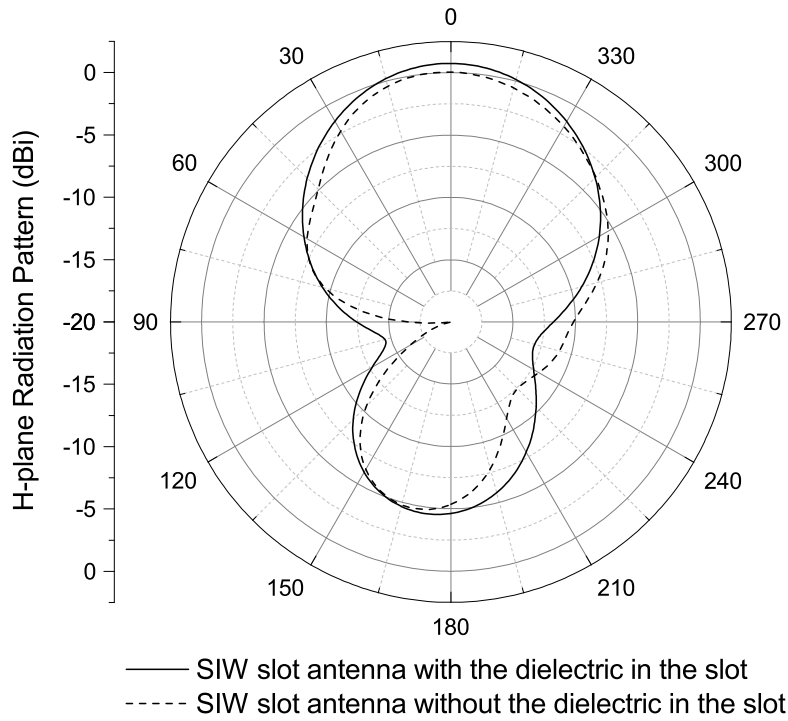
(b)

Figure 4.9: The comparison of radiation patterns for slot antenna with and without dielectric in the slot. (a) E-plane. (b) H-plane.
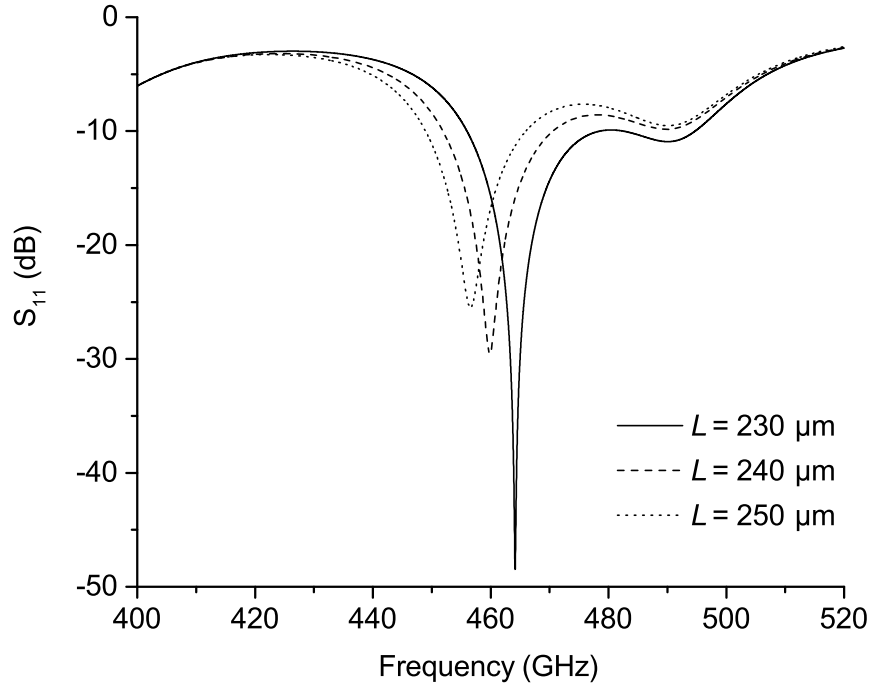
Figure 4.10: Simulated S_{11} of different slot lengths.

where h is the height of the SIW, w is the width of the SIW, and λ_0 is the wavelength in free space, which is derived from the characteristic impedance of the rectangular waveguide with the power-current definition [72]. The equations, which are used for the derivation of Equation 4.3, are presented in Appendix A. The characteristic impedance in HFSS was set to Z_{pi}, which is also based on the power-current definition as Equation 4.3. In Figure 4.13, the imaginary part of the propagation constant is close to zero at all frequencies. The small difference between simulated and theoretical values is due to the error of equivalent width of the rectangular waveguide.

The characteristic impedance and the effective dielectric constant of a microstrip are given approximately by [73]:

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\varepsilon_e}} \ln\left(\frac{8h}{w_m}\right) + \frac{w_m}{4h} & \text{for } w_m/h \leq 1 \\ \frac{120\pi}{\sqrt{\varepsilon_e}\left[w_m/h + 1.393 + 0.667\ln(w_m/h + 1.444)\right]} & \text{for } w_m/h \geq 1 \end{cases} \tag{4.4}$$

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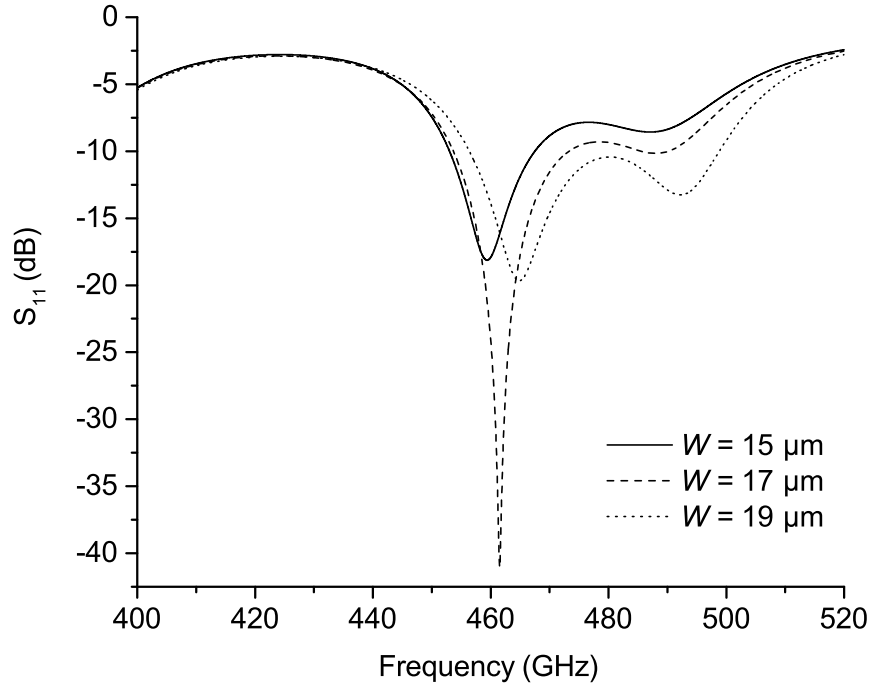
Figure 4.11: Simulated S_{11} of different slot widths.

$$\varepsilon_r = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12h/w_m}} \qquad (4.5)$$

where w_m is the width of the microstrip line, h is the thickness of the substrate, ε_e is the relative dielectric constant of the substrate.

Since the height of the SIW is only $8.805\,\mu$m, the width of microstrip line is larger than the height. Then $w_m/h \geq 1$ is used in the design of the microstrip. With the effective dielectric constant ε_r of 3, the width of the microstrip of $15\,\mu$m for a $50 - \Omega$ microstrip can be calculated from the Equations 4.4 and 4.5. The wavelength in the microstrip is $377\,\mu$m at 460 GHz. According to the impedance of quarter-wave transformer $Z_1 = \sqrt{Z_0 R_L}$, the quarter-wave transformer is implemented between the input microstrip and the SIW slot antenna. The antenna dimensions are listed in Table 4.2.

As mentioned in the Section 4.1, the "dummy" metal inside the dielectric change the dielectric constant of the SIW. By using the inductor identification layer the "dummy" metals
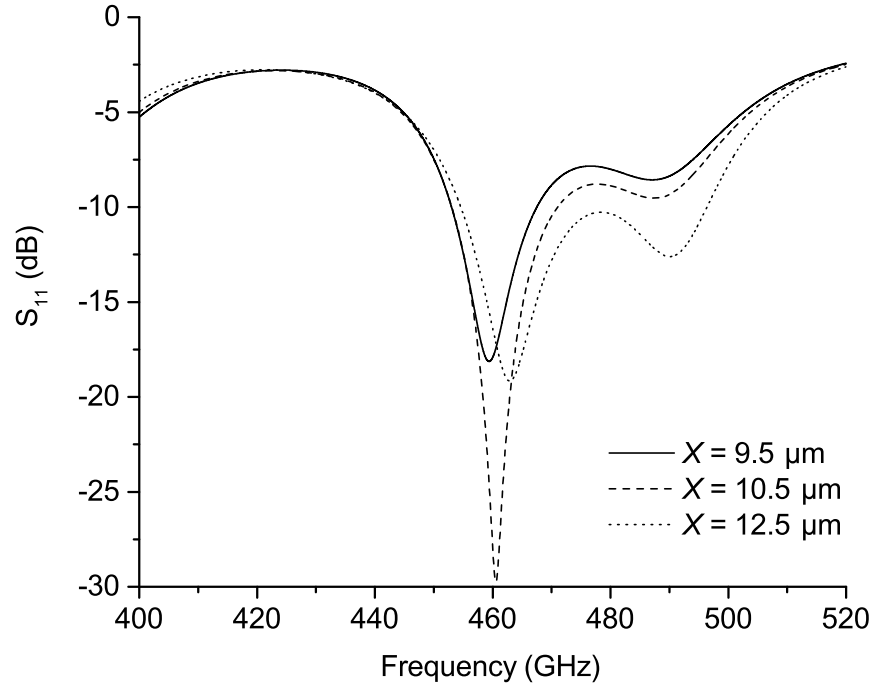
Figure 4.12: Simulated S_{11} of different slot offsets.

were significantly reduced in the SIW. Figure 4.14 compares the simulated S_{11} for the proposed antenna and the antenna without "dummy" metals. It is evident that the "dummy" metals in the SIW do not impact the impedance of the SIW. The inductor identification layer works well to minimize the impact of the "dummy" fill. In addition, the simulated S_{11} for the antenna without holes in M1 layer is also presented in Figure 4.14. The presence of the holes in M1 changes the impedance of the SIW, which makes the resonant frequency of the SIW slot antenna decrease 7 GHz from 467 GHz to 460 GHz. The dielectric layer D1 and D2 are at the same level as M1 as shown in Figure 4.1. Therefore, D1 and D2 fill in the holes after square holes are created in M1. This changes the equivalent dielectric constant of the SIW as demonstrated in the following section.
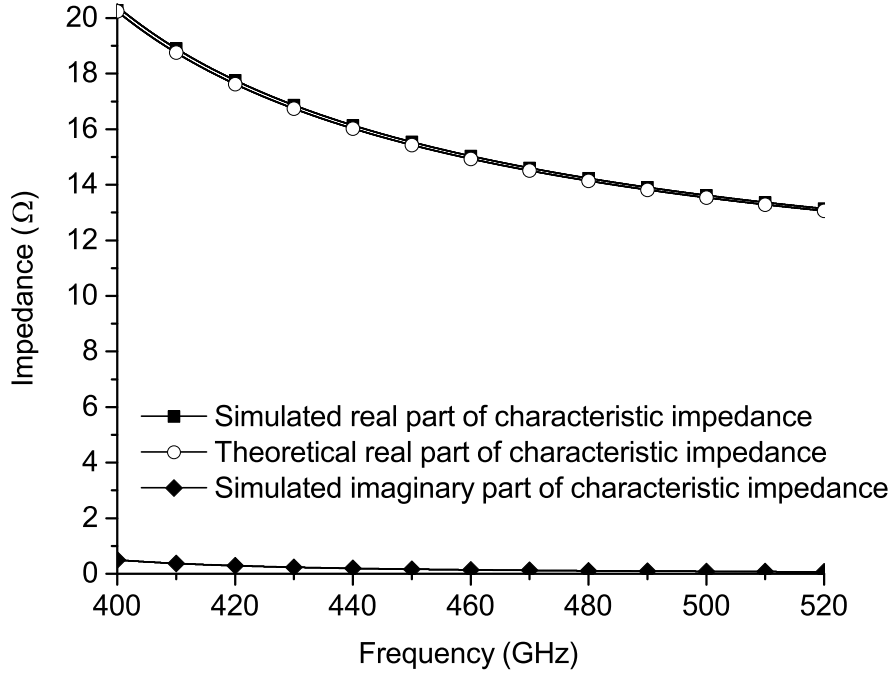
Figure 4.13: Simulated and theoretical impedance of the proposed SIW.

4.3 Simulation Results

Given the sheet resistance and the thickness of each metal layers from the TSMC 65 nm CMOS design rules, the conductivity of each metal layer is calculated from Equation 4.6,

$$\sigma = \frac{1}{\rho} = \frac{1}{R_s \cdot t} \tag{4.6}$$

where σ is the conductivity, ρ is the resistivity, R_s is the sheet resistance, and t is the sheet thickness. The bulk conductivity of M1, M2, $\cdots$, M7, M10 and Via9 are a little lower than that of aluminum. The bulk conductivity of M8 and M9 are a little lower than that of copper. With all dimensions, metal conductivity and dielectric constants, the design can be precisely modeled in HFSS.

However, the accurate model is not appropriate for all simulations. There are 30 di-

Table 4.2: Antenna dimensions of the 460 GHz SIW slot antenna.

Name	Dimension (μm)
Microstrip length	94.5
Quarter-wave transformer length	94.5
Microstrip width	16.4
Quarter-wave transformer width	41.2
Dummy square size	3
Dummy spacing	12
M1 square hole size	10
M1 square hole spacing	10
Via size	3
Via spacing	3
Slot length L	250
Slot width W	20
Slot offset X	10
Entire chip length	577.8
Entire chip width	224

electric layers between M1 and M10 in the 65 nm CMOS process. Some layers are only about several 10^{-2} μm thick. Electromagnetic 3D simulations of such a complex structure requires significant computational resources and a very long simulation time. Therefore, to make 3D EM simulations feasible, an equivalent model comprising of a single dielectric layer was investigated for simulations. By considering all 30 dielectric layers as a series combination of capacitors as shown in Figure 4.15, the total capacitance is calculated by

$$\frac{1}{C_t} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_n}. \tag{4.7}$$
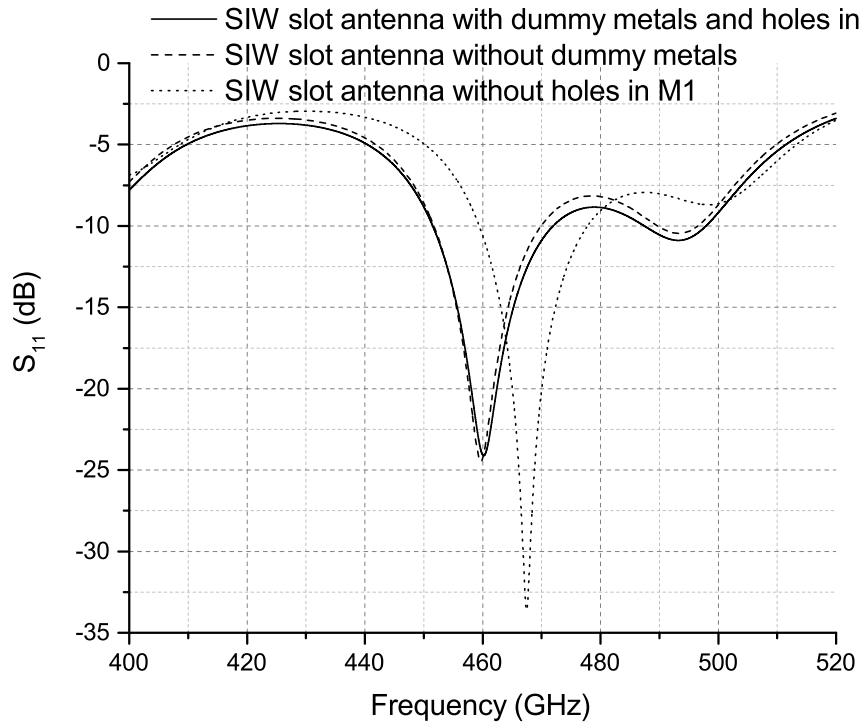
Figure 4.14: Comparison of S_{11} for the SIW slot antenna with and without "dummy" metals in the dielectric and holes in the M1.
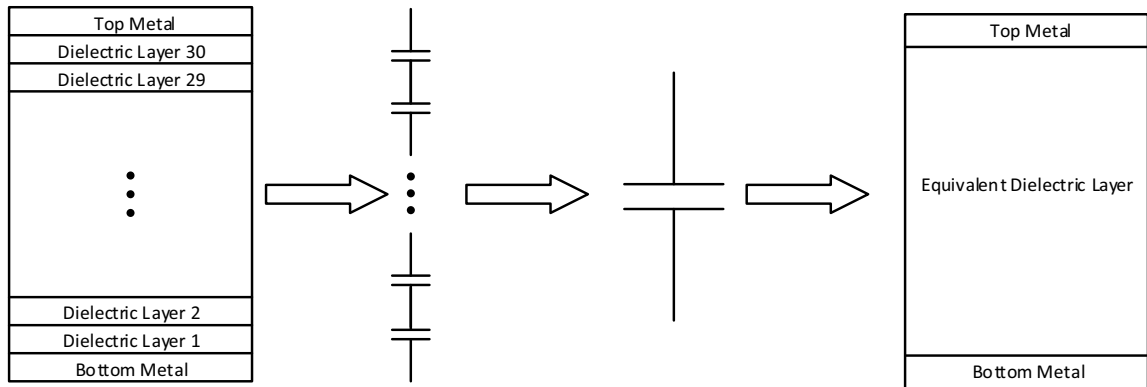
Figure 4.15: Multi-dielectric layers can be equivalent to a series combination of capacitors.

By calculating the dielectric constant, which makes the single capacitor formed between the top and bottom layers equal to total capacitance, the equivalent dielectric layer is found from

$$C = \frac{\varepsilon A}{d}, \tag{4.8}$$

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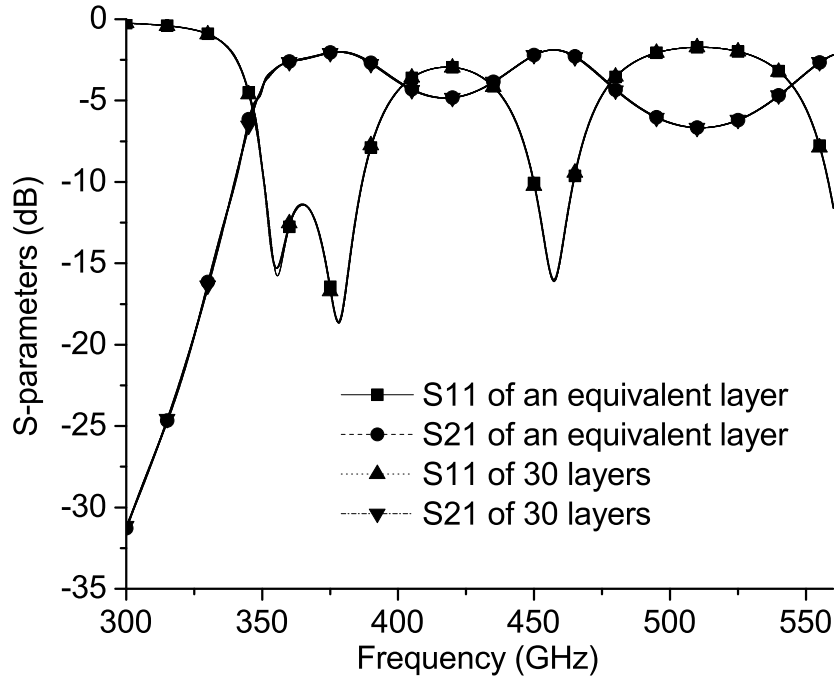
Figure 4.16: Simulated S-parameters of 30 layers and an equivalent dielectric layer.

where ε is the permitivity of the dielectric, A is the area of the parallel metallic plates, and d is the thickness of the dielectric. Then the equivalent dielectric constant of 3.93 can be calculated. A comparison of S-parameters between 30 dielectric layers SIW and an equivalent dielectric layer SIW is shown in Figure 4.16. The simulated S_{11} is almost identical for both 30 layers and equivalent single layer model. In addition, Figure 4.17 illustrates 3D HFSS simulations of S_{11} of a SIW slot antenna, which was modeled with an equivalent dielectric layer and with 30 dielectric layers. The simulations of the antenna modeled with the complete 30-dielectric-layer structure required 752 GB of RAM. However, only 21.5 GB of RAM was needed for the single equivalent-dielectric-layer-antenna model. It was concluded that the equivalent dielectric model reduces memory requirements significantly while keeping the simulation precision. This equivalent dielectric was used for all antenna simulations.

The simulated gain of the final antenna is 0.86 dBi at 460 GHz. The co-polarization
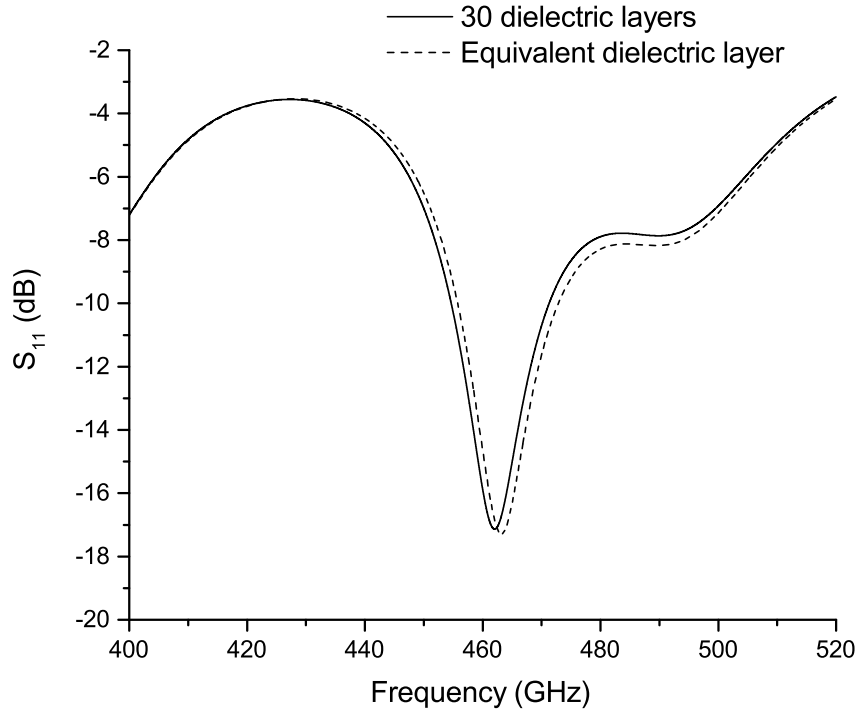
Figure 4.17: Simulated of S_{11} for antennas with both 30 dielectric layers and an equivalent dielectric layer.

and cross-polarization radiation patterns are shown in Figure 4.18 using Ludwig's third definition of cross polarization [74]. The HPBWs are $102°$ and $73°$ in E-plane and H-plane, respectively. The simulated peak gain for both co-polarization and cross-polarization and radiation efficiency are shown in Figure 4.19. The peak gain and radiation efficiency do not change much from 450 GHz to 470 GHz. The cross-polarization is $20 \sim 23$ dB below the co-polarization in the frequency range. The surface currents distribution of top metal is shown in Figure 4.20, which is similar distribution to that of the 46 GHz antenna. The currents are depicted as a grayscale map using white for maximum current intensity and traversing to black for minimum current intensity. The 3D radiation pattern with the antenna model from HFSS is presented in Figure 4.21 .

There is a ~ 0.5 mm dielectric substrate under the M1 in the 65 nm CMOS process. To determine the impact of the CMOS silicon substrate on the antenna performance, the

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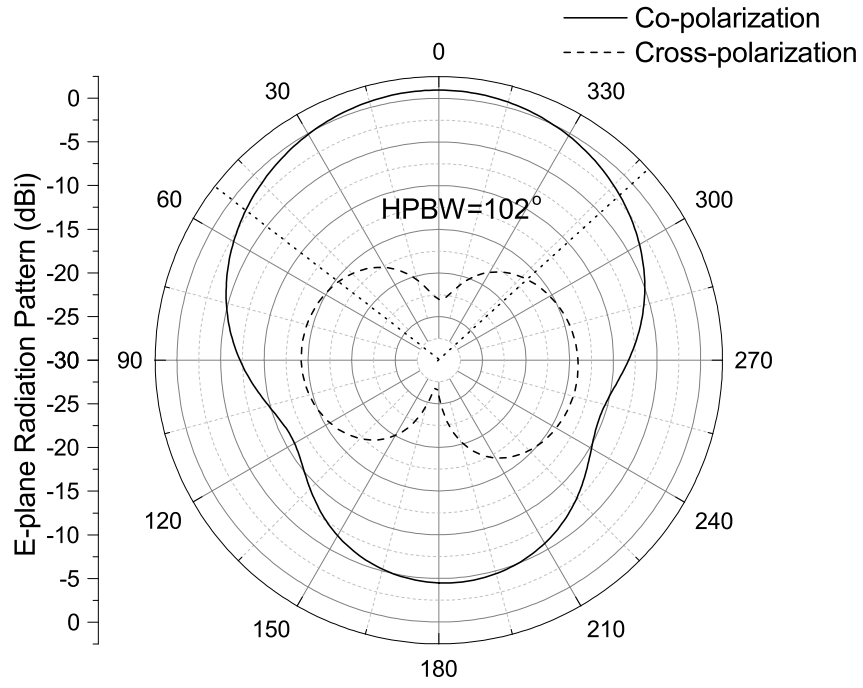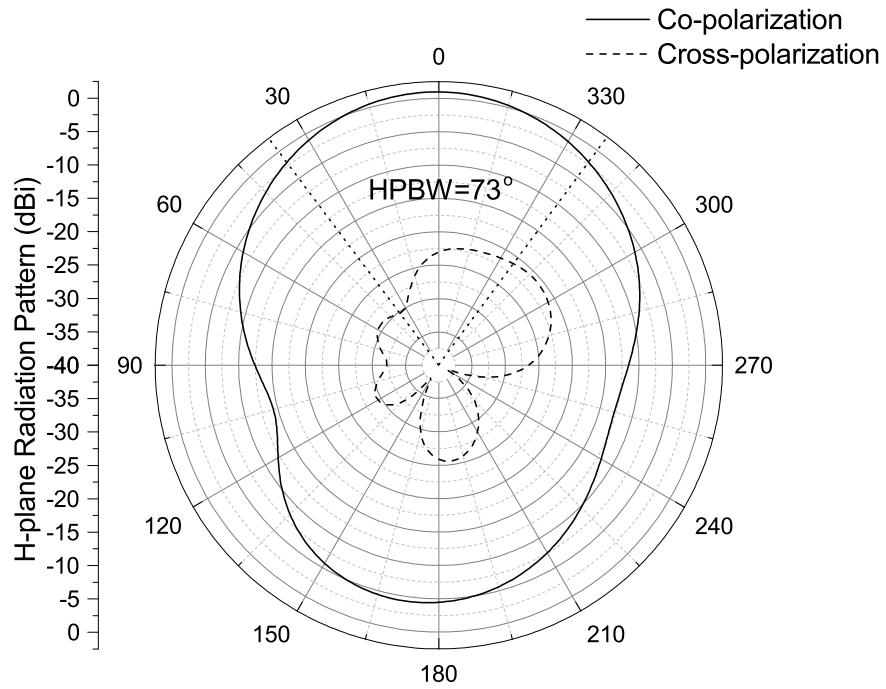
Figure 4.18: Radiation patterns of the proposed antenna at 460 GHz. (a) E-plane radiation pattern. (b) H-plane radiation pattern.
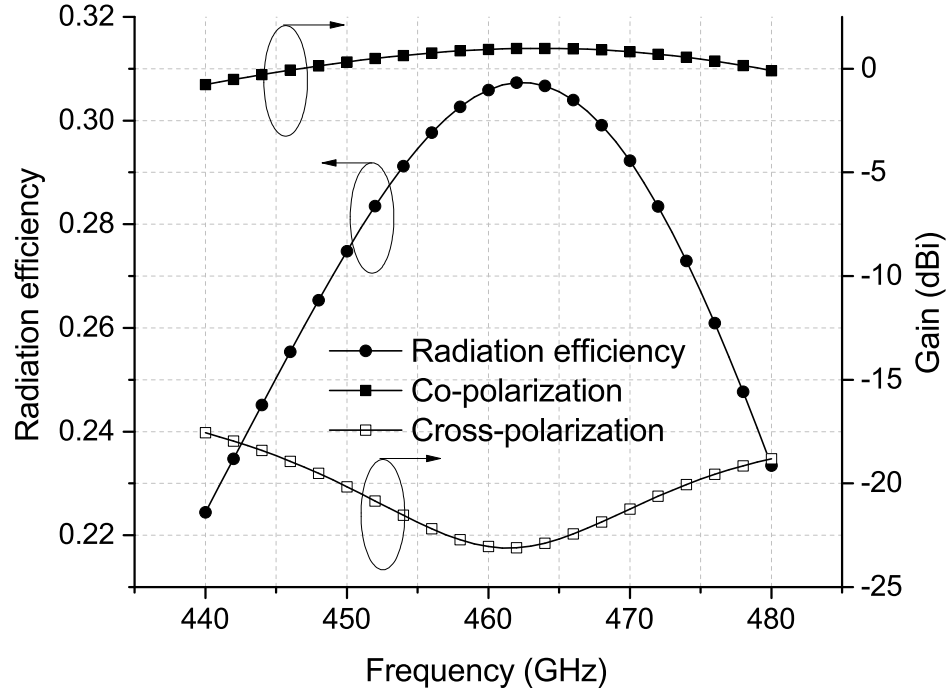
Figure 4.19: Simulated radiation efficiency and the peak gains of the proposed antenna for both co-polarization and cross-polarization.

simulated S_{11} of the proposed antenna with and without the silicon substrate is presented in Figure 4.22. With the substrate the resonant frequency shifts from 460.1 GHz to 457.6 GHz. The bandwidth of S_{11} below -10 dB increases from 20.4 GHz to 25.3 GHz. The gain and efficiency are listed in Table 4.3. Also, the simulated radiation patterns of the antenna with and without the silicon substrate are shown in Figure 4.23. As can be seen, with the substrate the gain drops from 0.86 dBi to 0.09 dBi. The radiation efficiency drops from 30.1% to 29.1%. In addition, Table 4.3 compares the proposed antenna with 4 other simulated terahertz on-chip CMOS antennas.

4.4 Loss Analysis

The antenna radiation efficiency is affected by two dissipation mechanisms: ohmic and dielectric loss. Ohmic losses are due to the finite conductivity and the roughness of the
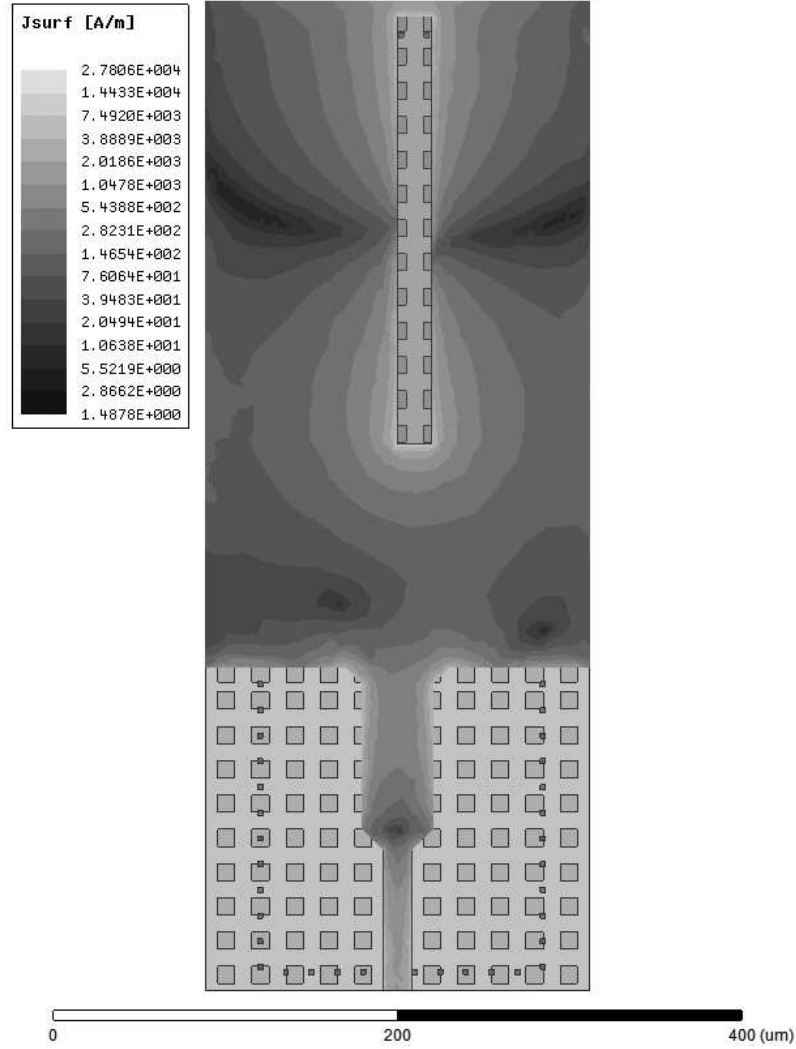
Figure 4.20: Surface currents distribution of the top metal.

metal layers and vias. Dielectric losses are due to the dissipation caused by the dielectric material (loss tangent). In the previous section the loss tangent was 0.001 for the dielectric and conductivity of metal layers were calculated from the design rules, which resulted in conductivity nearly that of aluminum and copper.

To find out the cause for reduced antenna efficiency and gain, two initial sets of simulations were performed: one was to check material losses and the other one was to check the "dummy" metals and holes influences. The first simulation in the first set investigated the effect of ohmic loss, by using perfect electric conductor (PEC) instead of the finite conductivity of the metals in the CMOS process. The second simulation investigated the loss
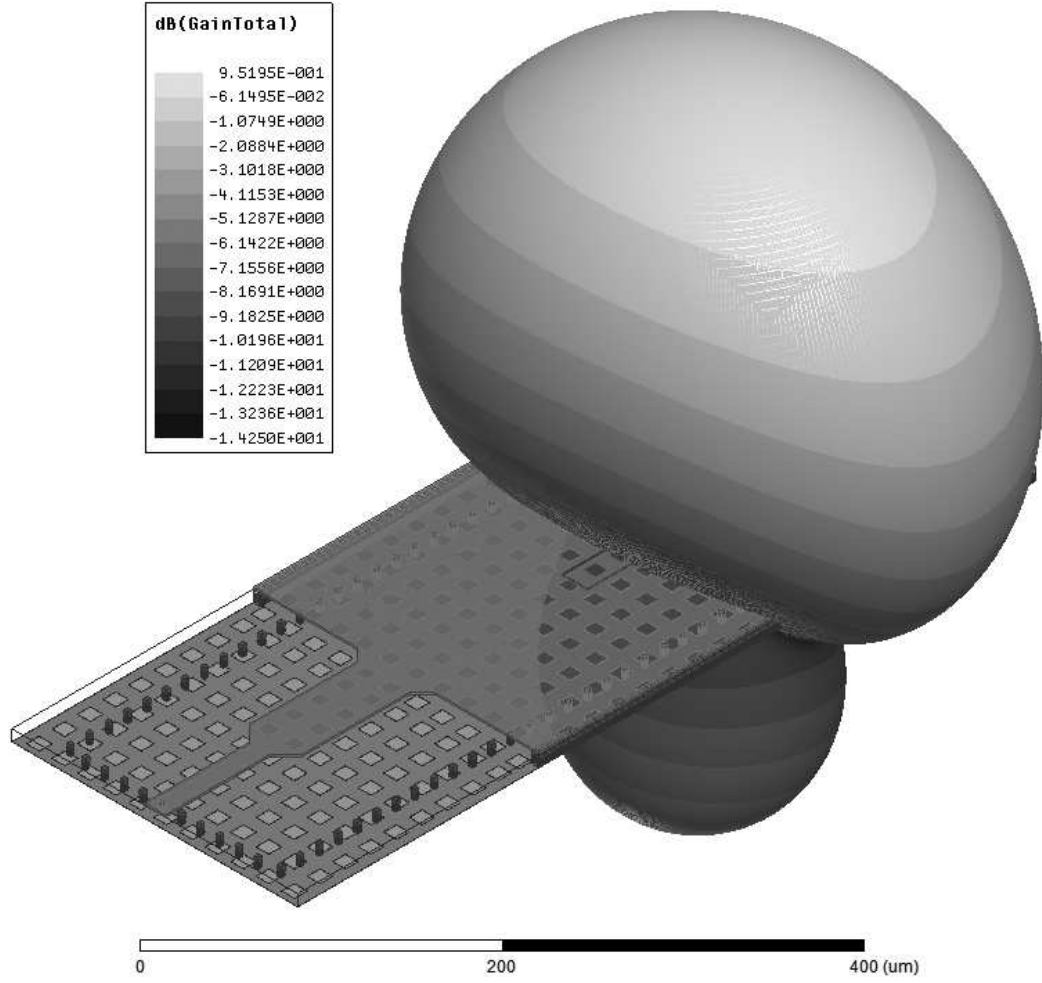
Figure 4.21: Antenna model and 3D radiation pattern from HFSS.

tangent of the dielectric material by setting loss tangent to zero for the no-dielectric-loss case. The results are shown in the first 4 rows of Table 4.4 where for comparison a lossless case (row 1) and the practical case (row 4) are also included. As can be seen most of loss is due to ohmic loss.

To investigate the effect of "dummy" metals and square holes in the bottom metal, in addition to the first two simulations another 3 simulations were conducted. In the first simulation of the second set all metal "dummies" were removed to investigate their affect on antenna performance. In the next simulation, all M1 holes were removed, which was followed by the last simulation where both "dummies" and holes were removed. The comparison of radiation efficiency and peak power gain resulted from the three additional
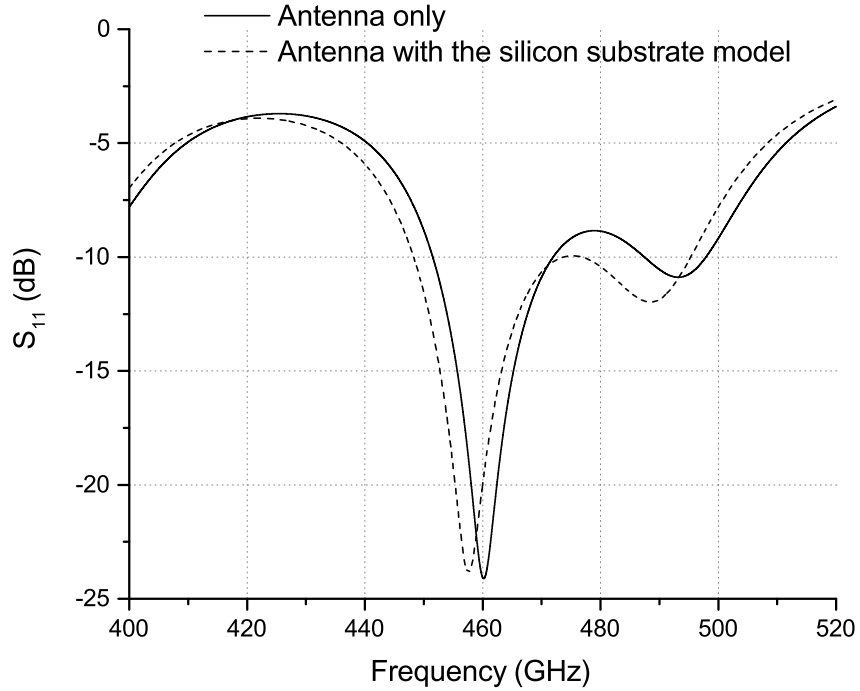
Figure 4.22: Simulated S_{11} of the SIW slot antenna with and without silicon substrate underneath.

simulations are shown in the fifth to seventh rows of Table 4.4.

At last another loss test was performed on bottom metal. Because there are many holes in the M1 layer, it was suspected that it may not be a good ground metal. Therefore, M2 was connected to M1. The same hole size ($10\,\mu$m $\times\,10\,\mu$m) was created on M2 as shown in Figure 4.24 (a) while keeping the holes in M1 and M2 non overlapping. The top view of M1 and M2 combined together is shown in Figure 4.24 (b). M1 and M2 are connected by Via1, which are in horizontal rows. The simulated gain and efficiency are listed in the last row of Table 4.4. As can be seen combining M1 and M2 improves the gain by $0.4\,$dB and efficiency by 3.5%. However, this model conflicts with the design rules and cannot be fabricated.

The loss analysis for the SIW shows the same result: a SIW with the same width and height of the proposed antenna was simulated in HFSS. PEC and loss tangent of 0.001

Table 4.3: Comparison of simulated on-chip antennas.

	This work[1]	[48]	[49][1]	[47]	[46] [1]
Antenna type	**SIW slot**	SIW slot	Planar dipole	Patch	SIW corner slots
Frequency	**460 GHz**	434 GHz	540 GHz	410 GHz	270 GHz
Gain	**0.86 dBi, 0.09 dBi** [2]	−0.55 dBi	1.33 dBi [2]	0.41 dBi [3]	−0.5 dBi
Radiation efficiency	**30.1%, 29.1%** [2]	49.8%	28% [2]	22% [2]	21.4%
Process	**65 nm CMOS**	0.13 μm SiGe BiCMOS	40 nm CMOS	45 nm CMOS	65 nm CMOS
Antenna area	**380 μm× 224 μm**	450 μm × 250 μm [4]	170 μm × 300 μm	200 μm × 200 μm	410 μm × 410 μm

[1] Satisfy the metal density rules
[2] With the silicon substrate
[3] Calculated from directivity and efficiency
[4] Estimated from the microphotograph of the chip-set

Table 4.4: Efficiency and gain for different loss set-up SIW slot antenna.

Antenna loss set-up	Efficiency	Peak Gain (dBi)
Lossless	100%	6.0
Only metal loss	31.5%	1.1
Only dielectric loss	95.4%	5.8
Both metal and dielectric loss	30.1%	0.86
Without "dummies"	33.6%	1.3
Without holes in M1	37.5%	2.0
Without "dummies" and holes	41.8%	2.3
Combining M1 and M2 as bottom metal	33.6%	1.25
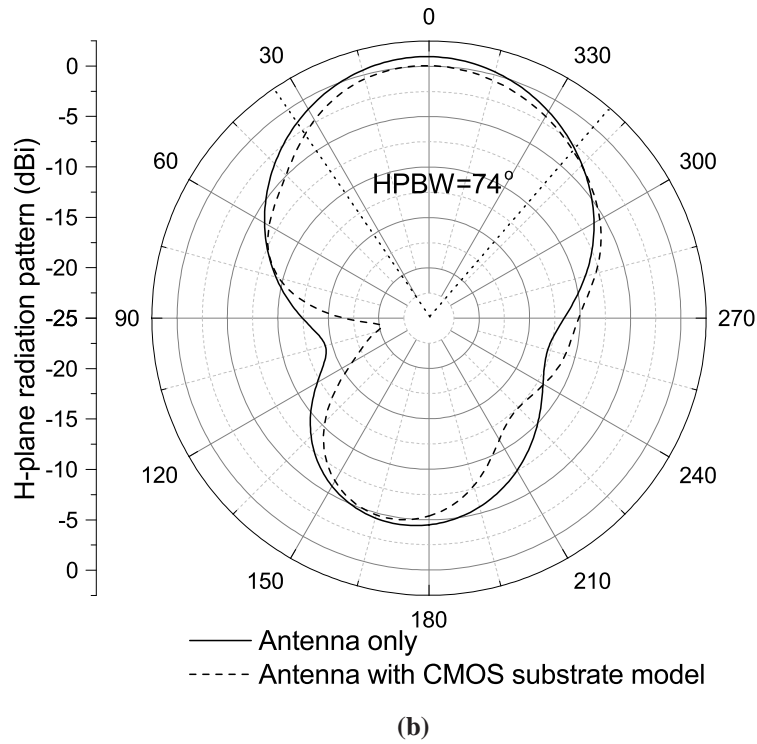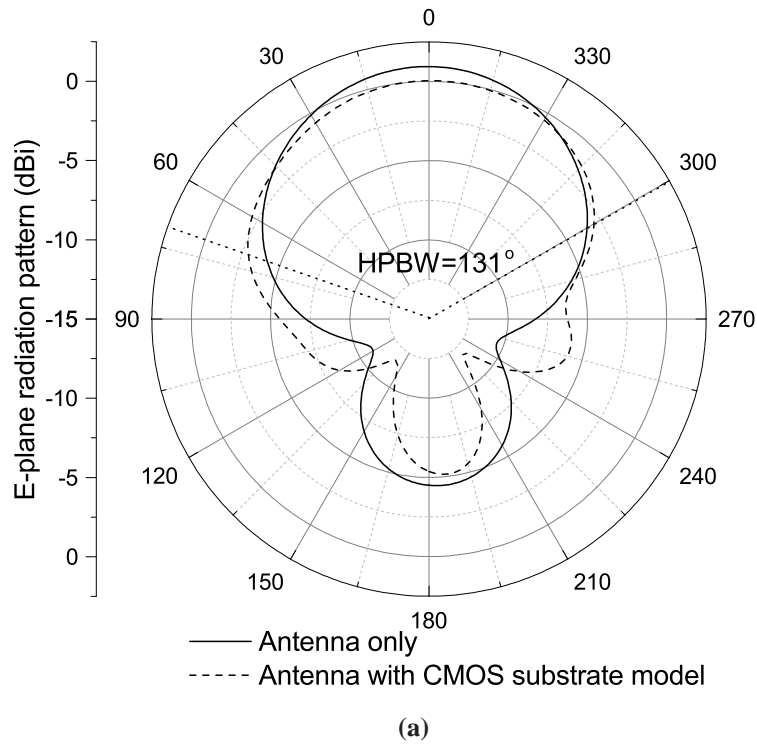
Figure 4.23: Comparison of simulated radiation patterns for antenna only and antenna with CMOS substrate model. (a) E-plane. (b) H-plane.

are set for metal and dielectric material respectively. The attenuation is 14.5 Np/m due to dielectric loss, which is identical to the result calculated for dielectric loss of a rectangular waveguide from [73]

$$\alpha_d = \frac{k^2 \tan\delta}{2\beta},\qquad(4.9)$$

where β is the propagation constant, k is wave number and $\tan\delta$ is the loss tangent of the dielectric.

To simulate the attenuation due to conductor loss, the loss tangent was set to 0 and the conductivity is calculated from data in the 65 nm CMOS design rule manual. The theoretical attenuation of 217.6 Np/m for a rectangular waveguide is obtained from [73]:

$$\alpha_c = \frac{R_s \left(2h\pi^2 + w^3 k^2 \right)}{w^3 h\beta k\eta},\qquad(4.10)$$

where R_s is the surface resistivity of the metal, μ_0 is the permeability of free space, and $\eta = \sqrt{\mu/\varepsilon}$ is the intrinsic impedance of the material filling the waveguide, w and h are the width and height of the rectangular waveguide, respectively. However the simulated attenuation due to metal loss was found to be 259 Np/m, which is higher than the theoretical value. The reason could be that M1 metal is too thin, is only 1.4 times the skin depth of M1 at 460 GHz, and some extra loss from the silicon substrate contributes to the attenuation.
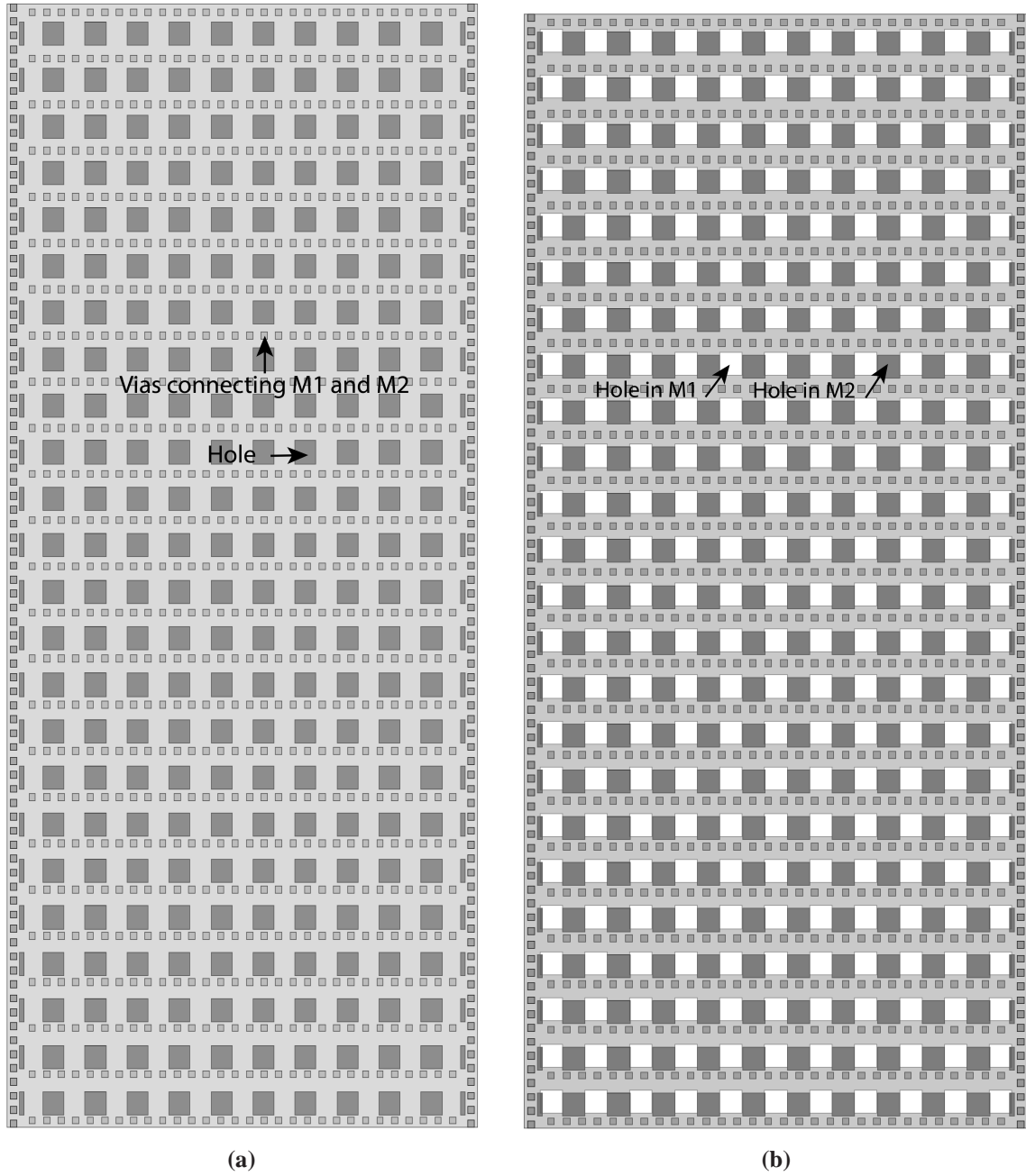
Figure 4.24: (a) M2 layer model from HFSS. The dark squares are holes in M2, which are $10\,\mu$m $\times$ $10\,\mu$m. Vias connecting M1 and M2 are in horizontal rows, which are $3\,\mu$m $\times$ $3\,\mu$m. (b) Both M1 and M2 layers model from HFSS. The white squares are holes in M1, and the dark squares are holes in M2. Both are also $10\,\mu$m $\times$ $10\,\mu$m.

4.5 Conclusion

A design of the $460\,\text{GHz}$ SIW slot antenna on $65\,\text{nm}$ CMOS process is proposed in this chapter. Some methods are developed to simplify the design and simulation: an inductor identification layer is introduced to reduce the metal density requirements from 10% to 0.7%, an equivalent dielectric layer that accurately models the effects of multiple dielectric layers is investigated to reduce the RAM needed from $752\,\text{GB}$ to $21.5\,\text{GB}$ for 3D EM simulations, and the top metal layer identified as a bondpad removed some dielectric covering the antenna top. When implemented on a $0.5\,\text{mm}$ Si substrate, the proposed antenna has a gain of $0.09\,\text{dBi}$ and efficiency of 29.1%. The impedance bandwidth $(\text{S}_{11} < -10\,\text{dB})$ is $25.3\,\text{GHz}$. The ohmic loss is the dominant loss contributor influencing the antenna gain and efficiency. Also, the "dummy" metals and holes in the bottom metal, which are needed to satisfy the design rule requirements, decrease efficiency by 11.7% and gain by $1.4\,\text{dB}$. In the simulation combining M1 and M2 as the bottom metal achieves higher gain and radiation efficiency than using M1 layer only. However, due to design-rule restrictions combining M1 and M2 is not fabricatable.

Chapter 5

Conclusions, Contributions and Future Work

5.1 Thesis Summary

The design of a 460 GHz CMOS SIW slot antenna inspired by the developments of CCAT CHAI is presented in this thesis. This work is not officially part of the CHAI development but may provide alternatives to implementation of CHAI. Chapter 1 introduced the infrared astronomy science, discussed the avalable electromagnetic spectrum for the science, and reviewed some ground-based observatories, such as CCAT CHAI.

Chapter 2 provided literature review and explained the selection of the substrate-integrated waveguide (SIW) slot antenna for this work. Chapter 2 also introduced SIW technology and its operation principles. In addition a brief introduction of slot antennas was given with discussions of the Babinet's Principle and the impedance of a longitudinal slot in the broad wall of a rectangular waveguide.

Chapter 3 presented the design of a 46 GHz SIW slot antenna, which is a down-scaled prototype of the 460 GHz SIW slot antenna. A 46 GHz SIW slot antenna was designed and tested to verify the design concepts, which are identical to that of the 460 GHz SIW slot antenna. The antenna fabricated on PCB was presented in Figure 3.12. The comparisons of the simulated and experimental S_{11}s and radiation patterns were given. There are strong agreements between simulated and measured results, which verified the design and simulations approaches and supported.

Chapter 4 demonstrated the design and simulations of a 65 nm CMOS 460 GHz SIW slot antenna. The chapter started with a discussion of the CMOS process design-rule restrictions, which make the design of SIW slot antenna more complicated than for its 46 GHz PCB counterpart. An inductor identification layer was introduced in the design to minimize the design-rule restrictions, which reduced the "dummy" metal requirements from 10% to 0.7%. The effect of the slot size and its placement on the SIW slot antenna S_{11} were

demonstrated. The final antenna dimensions are given in Table 4.2. The SIW slot antenna simulation results and comparison with other similar antennas are listed in Table 4.3. At the end of the chapter, the loss mechanisms were investigated. The final conclusion was that the metal loss was the most significant contributor to low antenna efficiency with the analysis results presented in Table 4.4.

5.2 Contributions

The 46 GHz SIW slot antenna presented in this thesis :

- Minimized the back lobe by oversizing the bottom ground

- Achieved large gain by properly selecting dimensions of the top metal

- Was published in [29]

The 460 GHz CMOS SIW slot antenna presented in the thesis:

- Introduced an inductor identification layer in the layout to reduce the internal metal density requirements significantly

- Found an equivalent dielectric layer that accurately models the effect of multiple dielectric layers is used to reduce the RAM needed significantly for the 3D EM simulations

- Ran HFSS from command mode remotely on the HPC (High Performance Computer) "Bigbyte" computer and provided the scripts for later user

- Had been submitted to *Microwave and Optical Technology Letters*

Other published contribution during the author's M.Sc. studies is a joint report [75] co-authored with three other graduate students and faculty members working on various aspects of CCAT CHAI.

5.3 Future Work

This thesis demonstrates the feasibility of using a CMOS technology to implement an antenna operating in the frequency range of the CCAT CHAI. While it is shown that the 460 GHz SIW slot antenna can be fabricated in a 65 nm CMOS process, there are several areas that need improvement and additional examination prior to finalizing the design of the SIW slot antenna.

The first major area relates to the feed of the SIW slot antenna. Currently in the simulation the feed network is a $50 - \Omega$ microstrip and the matching network is a quarter-wave transformer. When connecting the antenna with the CHAI receiver, the signal would come from transistors, which are connected to on M1 metal layer. In this case, the microstrip may not be an optimum choice. A pin in the SIW through a hole of M1 connecting to the transistor may be a better option to excite the antenna. In this case, the antenna will be a SIW cavity-backed slot antenna.

Another major area relates to fabrication and testing of this design. Although the design concept has been proved correctly with a 46 GHz SIW slot antenna, it is desirable to test the 460 GHz SIW slot antenna directly.

The gain of the proposed SIW slot antenna is not very high and the HPBW is not narrow enough to illuminate CCAT CHAI reflector. Slot arrays therefore should be investigated to increase the gain and narrow the beamwidth.

At last the CMOS design-rules restrictions limit the antenna performance. From the loss test it was determined that ohmic loss is the dominant loss contributor influencing the antenna gain and efficiency. Ways of reducing conductor losses should be investigated. Alternatively, dielectric resonator antennas (DRA) have lower conductor loss [76] and either DRAs or dielectric lens attached to the CMOS slot antenna may be a way of improving efficiency.

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Appendix A

Summary of Dominant Mode (TE$_{10}$) of the Rectangular Waveguide

The electric field and magnetic field lines of TE$_{10}$ mode for a rectangular waveguide with a width of w and height of h are shown in Figure A.1. In addition, Table A.1 lists summary of TE$_{10}$ mode results for a rectangular waveguide.

From equations listed in the Table A.1 and the relationship between the frequency and the wavelength, $\omega = 2\pi f = 2\pi \frac{c}{\lambda}$, Equation 4.3 can be obtained.

Table A.1: Summary of TE$_{10}$ mode for rectangular waveguide.

Quantity Name	Equation
z component of magnetic field	$H_z = A_{10}\cos\frac{\pi x}{w}e^{-j\beta z}$
x component of magnetic field	$H_x = \frac{j\beta w}{\pi}A_{10}\sin\frac{\pi x}{w}e^{-j\beta z}$
y component of electric field	$E_y = \frac{-j\omega\mu w}{\pi}A_{10}\sin\frac{\pi x}{w}e^{-j\beta z}$
Other components of E, H field	$E_x = E_z = H_y = 0$
Cutoff frequency	$f_{c10} = \frac{1}{2w\sqrt{\mu\varepsilon}}$
Guide wavelength	$\lambda_g = \frac{2\pi}{\beta}$
Propagation constant	$\beta = \sqrt{k^2 - k_c^2}$
Wave number	$k = \omega\sqrt{\mu\varepsilon}$
Cutoff wave number	$k_c = \frac{\pi}{w}$
Wave impedance	$Z_{TE} = \frac{k\eta}{\beta}$
Intrinsic impedance of the dielectric in the waveguide	$\eta = \sqrt{\frac{\mu}{\varepsilon}}$
Maximum power	$P_{max} = \frac{E_{max}^2 wh\sqrt{\varepsilon_r}}{480\pi}\sqrt{1 - \left(\frac{\lambda_0}{2w\sqrt{\varepsilon_r}}\right)^2}$
Attenuation (dB/m)*	$\alpha = \frac{8.686 R_s}{120\pi h}\frac{1 + \frac{2h}{w}\left(\frac{\lambda}{2w}\right)^2}{\sqrt{1 - \left(\frac{\lambda}{2w}\right)^2}}$
Characteristic impedance power-current definition	$Z_{pi} = 465\frac{h}{w}\sqrt{\frac{\mu_r}{\varepsilon_r}}\frac{\lambda_g}{\lambda}$
Characteristic impedance power-voltage definition	$Z_{pv} = 754\frac{h}{w}\sqrt{\frac{\mu_r}{\varepsilon_r}}\frac{\lambda_g}{\lambda}$
Characteristic impedance voltage-current definition	$Z_{vi} = 592\frac{h}{w}\sqrt{\frac{\mu_r}{\varepsilon_r}}\frac{\lambda_g}{\lambda}$

* R_s is the skin depth of the metal. $R_s = \sqrt{\frac{\omega\mu}{2\sigma}}$
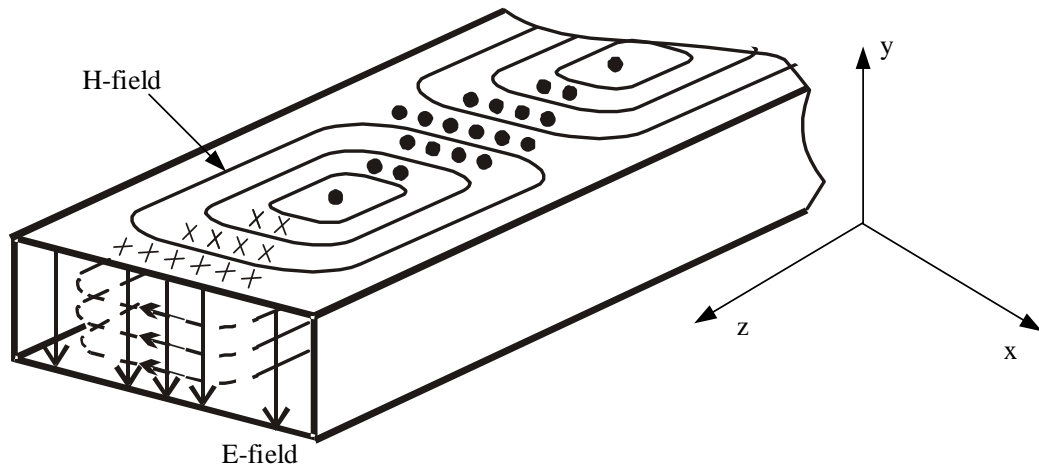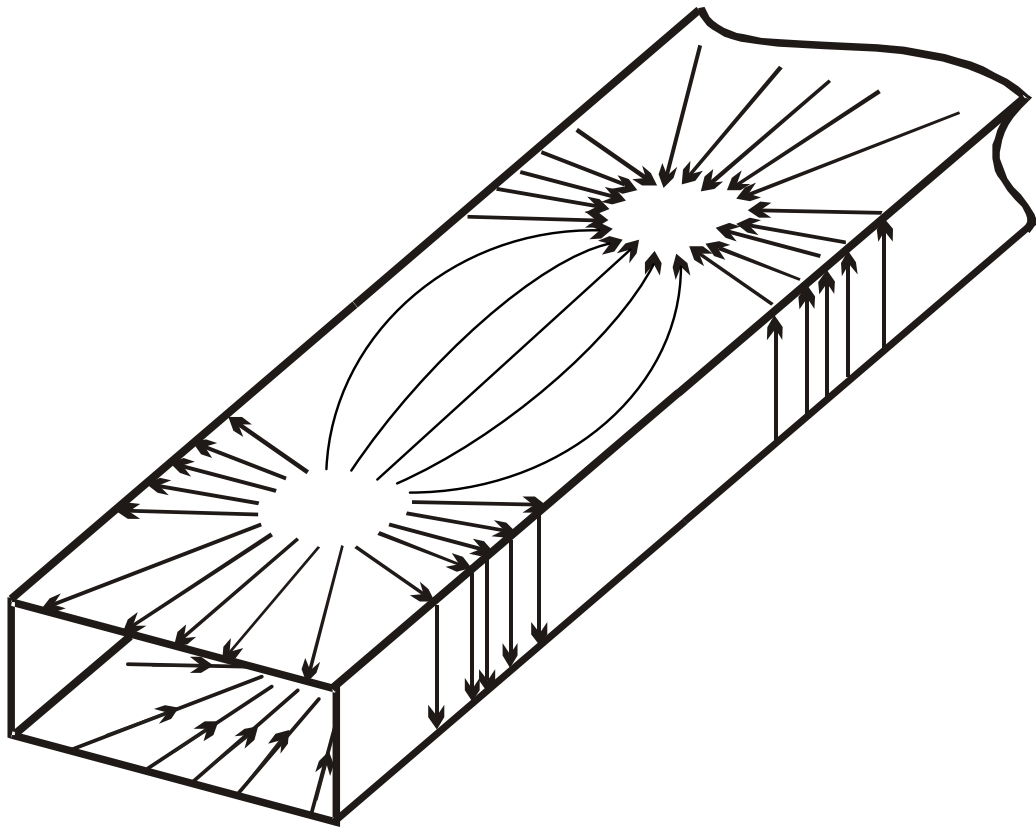
Figure A.1: (a) Field lines for TE_{10} mode of a rectangular waveguide. (b) Surface currents for TE_{10} mode of a rectangular waveguide.