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Characterization of Distortion Reduction for Single-Phase Multiple Inverter Operation

by

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Abstract

In photo-voltaic and other alternative energy systems, sine-wave pulse width modulation is often used to shift harmonics present in the inverter-bridge output to frequencies centered on the carrier frequency, which can be effectively attenuated by a passive filter, and thus result in a near sinusoidal AC voltage across the load. The inverter industry sometimes makes use of operating inverters in parallel to shift harmonics to even higher frequencies but this technique is not well understood. The harmonic performance of a naturally-sampled pulse width modulation strategy is investigated, in simulation and experimentally, with different modulation indices, inversion levels, and carrier-to-sine-wave frequency ratios, in the cases of two or three parallel inverters. Results indicate that the minimum total harmonic distortion occurs for an approximate inverter-to-inverter transistor gating delay of $T_c/N$ where $T_c$ is the carrier period and $N$ is the number of parallel transistor-gating-synchronized inverters.
Acknowledgements

Really, I am unable to derive suitable expressions to thank so many helpful people. Without their assistance, I could not complete this thesis.

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To my mother, who always sacrifices without expecting any returns from me, I thank you for your persistent prayers and patience. My mother, without doubt, I love you so much.

Special thanks to our God, first and last, for granting me the good fortune to meet all these kind people. Without them it would have been impossible to achieve what we have achieved.
Dedication

To: Fatima-El Zahra and Mary
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<td>AC</td>
<td>Alternating current</td>
</tr>
<tr>
<td>CSI</td>
<td>Current source inverter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct current</td>
</tr>
<tr>
<td>DG</td>
<td>Distributed generation</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital signal processor</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic compatibility</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier transform</td>
</tr>
<tr>
<td>NPC</td>
<td>Natural-point clamped</td>
</tr>
<tr>
<td>PCC</td>
<td>Point of common coupling</td>
</tr>
<tr>
<td>PIC</td>
<td>Programmable intelligent computer</td>
</tr>
<tr>
<td>PV</td>
<td>Photo voltaic</td>
</tr>
<tr>
<td>RMS</td>
<td>Root mean square</td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
</tr>
<tr>
<td>UPS</td>
<td>Uninterruptible power supply</td>
</tr>
<tr>
<td>VAR</td>
<td>Volt-ampere reactive</td>
</tr>
<tr>
<td>VSI</td>
<td>Voltage source inverter</td>
</tr>
<tr>
<td><strong>Modulation Methods</strong></td>
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<tr>
<td>PWM</td>
<td>Pulse width modulation</td>
</tr>
<tr>
<td>SPWM</td>
<td>Sinusoidal pulse width modulation</td>
</tr>
<tr>
<td>SHE</td>
<td>Selective harmonic elimination</td>
</tr>
<tr>
<td>TPWM</td>
<td>Trapezoidal pulse width modulation</td>
</tr>
<tr>
<td><strong>Semiconductor Power Switches</strong></td>
<td></td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar junction transistor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-oxide semiconductor field-effect transistor</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated gate bipolar transistor</td>
</tr>
<tr>
<td>GTO</td>
<td>Gate turn-off thyristor</td>
</tr>
<tr>
<td>SCR</td>
<td>Silicon controlled rectifier</td>
</tr>
<tr>
<td><strong>Mathematical Symbols</strong></td>
<td></td>
</tr>
<tr>
<td>Ac</td>
<td>Amplitude of carrier waveform</td>
</tr>
<tr>
<td>Am</td>
<td>Amplitude of sine waveform</td>
</tr>
<tr>
<td>C\textsubscript{1}</td>
<td>Magnitude of fundamental component</td>
</tr>
<tr>
<td>fc</td>
<td>Frequency of carrier waveform</td>
</tr>
<tr>
<td>fs</td>
<td>Frequency of modulating sine-wave</td>
</tr>
<tr>
<td>fh</td>
<td>Frequency of a harmonic component</td>
</tr>
<tr>
<td>M</td>
<td>Modulation index</td>
</tr>
<tr>
<td>N</td>
<td>Number of parallel inverters</td>
</tr>
<tr>
<td>N\textsubscript{T}</td>
<td>Number of terms used in THD calculation</td>
</tr>
<tr>
<td>Tc</td>
<td>Period of carrier waveform</td>
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<tr>
<td>Td</td>
<td>Range of phase shift delays</td>
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Chapter 1

Introduction

1.1 The Power Quality Concept

Modern civilization has become more dependent on electric energy in many fields such as commercial buildings, industrial applications, and residential facilities. With the development of electricity, the number of electrical and electronic devices and equipment connected to national and international grids has increased since a century ago, but also there has been a tremendous increase in the number of different types of electrical loads combined with rapid increase in electrical power consumption recently, particularly in newly industrialized areas such as China and India. At the same time, environmental concerns are having an impact on power system operation, including concern for CO₂ emissions from coal-fired and natural gas electrical plants.

In particular, power system operators (sometimes reluctantly) are incorporating alternative forms of electrical energy generation into the electrical grid, resulting in a new power system structure often referred to a distributed generation (DG). The most economic alternative electrical power generation is in the form of wind power. Wind farms are being installed worldwide, where, for systems presently being commissioned, each wind turbine in the farm has a rated power output typically of 1.8MW or 3MW. Another, less economic, form of alternative electrical power generation is based on the use of photo voltaic (PV) panels, also referred to as solar cells. There are locations where wind power is not viable and PV power generation is the logical choice of alternative energy. In the case of wind power, most wind power turbine systems employ a rotating electromagnetic generator (in concept not too different from the rotating generators used in existing coal, gas, and hydro generation plants). However, there are new rotating electric generators that cannot be connected directly to the electric grid and require power
conditioning in the form of an AC-to-AC, usually an AC-DC-AC, power converter. In the case of PV power, the electricity produced by the solar cells is DC electricity and thus a DC-to-AC power converter is required for the majority of PV generation applications. Note that a DC-to-AC converter is commonly referred to as an inverter since the DC input voltage is periodically reversed in polarity to produce the unfiltered AC waveform.

There are other forms of alternative energy, for example fuel cells, that also require an inverter. In general, the most desirable form of AC power is a fixed amplitude, fixed frequency, sinusoidal waveform. In the case of an off-grid application it is desirable that the inverter output voltage-waveform be sinusoidal. In the case of a grid-connected application it is desirable that the inverter output current-waveform be sinusoidal. Deviation, in amplitude, frequency or waveform shape, from the ideal is referred to as a loss of power quality.

The principle of power quality improvement is part of a very broad concept in grid-connected power generator systems (and also for loads on the grid), namely, electromagnetic compatibility (EMC). But the nonlinear current-voltage characteristics of the power electronic equipment (in a generator or a load) results in distortion of the current and/or voltage waveforms of the power system, ie, these waveforms deviate from the ideal (in North America 60 Hertz) sinusoidal waveform. Consequently the non-ideal waveform can be analyzed in terms of frequency components that are multiples of 60 Hertz, known as harmonics [1]. These harmonic components are sometimes referred to as being injected into the grid, or as polluting the power system.

1.2 Harmonic Distortion Phenomena

Recently electric power quality improvement and the power system harmonics mitigation in particular have become most important topics; for example, as presented regularly at each International Conference on Harmonics in Power Systems (ICHPS)
regularly, for three decades. The increasing use of power semiconductor devices such as diodes, transistors, thyristors as switching elements in power electronic circuits have gained much interest but their shortcoming is a nonlinear current-voltage characteristic. These nonlinear loads result in periodic but non-sinusoidal current. Using the Fourier series expansion, we can analyze these currents and the result is a sum of (in theory up to an infinite) number of sinusoidal currents of different frequencies. These frequencies are at integer multiples of the fundamental power frequency, where the fundamental frequency is 60 Hertz in North America, and is 50 Hertz in Europe. These current harmonic components will produce harmonic voltage components when flowing through the power system impedance and this leads to distortion of the utility voltage and "pollution" of the power system. This undesirable phenomenon affects the utility and its customers, sometimes adversely. With increasingly wider use of nonlinear devices in power system loads, a serious harmonic pollution is expected to continue and this has many negative effects [2, 3]:

- Worse power quality for the end users.
- More losses in transmission lines.
- Over-heating and thermal overloading of machines and other equipment.
- Malfunction of protective relays and circuit breakers in the power system.
- System disruption.
- Dielectric stressing.
- Harmonic resonance.
- System power factor reduction.
- Over-voltage and over-current on the network.
- Dielectric breakdown of insulated cables and kWh metering errors.

For the above reasons and the concerns over the negative effects of nonlinear power electronic devices, several standards organizations have or plan to issue distortion limits for these loads. The limits are based on the effects of these nonlinear loads and the cost of mitigation of these effects.
1.3 Mitigation of Harmonic Distortion

Since harmonic distortion has a multitude of negative impacts on loads and the power system as well, it is necessary to reduce the level of harmonics to acceptable limits. The Institute of Electrical and Electronics Engineers (IEEE) standard 519-1992 "Recommended practice and requirements for harmonic control in electrical power systems" provides specific constraints for current and voltage distortion at the point of common coupling (PCC), which is the point of interconnection between the customer and the utility supplier. To comply with the IEEE standard 519-1992, there are many techniques and strategies to mitigate harmonic distortion in electrical power systems, but not all strategies are adequate for a given problem. The first step in solving the harmonics problem is to analyze precisely the power system loads to define the nature, source and the characteristics of the problem. On the other hand, the design of cost-effective methods and solutions of distortion reduction will help alternative energy providers to meet the imposed limits. These strategies can be summarized as follows [4, 5].

- Introducing inductance in the form of a reactor or transformer in inductive drive circuits: This directly reduces a significant amount of the harmonic voltages or currents produced by this inductive load.
- Use of phase-shifting transformers: Delta-Wye connected transformers are classified as a second best way to reduce the harmonics of a system designed so that multiple 6-pulses AC drives operate simultaneously and at similar load levels.
- Passive filters: The output waveform of a grid-connected inverter contains harmonics which can be reduced to adequate levels (typically 5 percent total harmonic distortion) by passing the inverter output through a passive filter.
- AC line filters: These filters are used especially with large converters and reduce penetration of harmonics into the AC system. For this purpose harmonic filters can be connected to the neutral of each line.
- Active filters: This strategy uses a pulse width modulation (PWM) converter (e.g. a controlled rectifier type load) technique to convert distorted current into a sinusoidal current in phase with the line voltage.
1.4 Pulse Width Modulation Switching Technique

Power electronic converters are used to convert electrical energy from a certain level of voltage/current/frequency to another voltage/current/frequency using semiconductor device as switching elements. The important issue related to these converters is that the switches are operated only in one of two states, either fully on (or low impedance state) or fully off (or high impedance state). The process of changing the switching state of these semiconductor devices from fully on to fully off or vice versa is called gating. This topic is of a great importance and has gained considerable researcher interest. As a result, there are many strategies used to implement gating techniques such as square wave, modified square wave, and PWM techniques, where in each case it is very important to take into consideration many parameters such as carrier to modulating sine-wave frequency ratio, switching losses, harmonic distortion, and speed of response.

One of the most common approaches for controlling both frequency and amplitude of the AC output of power electronic converters is the strategy known as pulse width modulation (PWM). In this technique a microcontroller is used to vary the duty cycle (or mark-space ratio) of the switching device(s) at a relatively high switching frequency to attain the desired low frequency output voltage or current. Pulse width modulation as a theory and technique has been well developed and though no longer a major research area in power electronics PWM continues to be one of the most effective techniques used in modern power converters.

1.5 Motivation Behind the Thesis

PWM inverters have been used for many decades for controlling the amplitude of the output voltage and also as a modern and effective strategy for reducing its harmonic content [6, 7]. In general, the PWM technique “pushes” most of the harmonic energy into high frequency regions, which can then be more easily filtered out using frequency selective passive filters. This is a practical approach since harmonics at low frequencies are very difficult to filter out without removing some of the desired fundamental frequency. Although this technique is an extremely successful method, there have been a
number of strategies implemented in the development of PWM principles and schemes to suit different converter topologies. Several strategies have been suggested to mitigate harmonic distortion utilizing different PWM techniques, and are reviewed in Chapter 2. Some of these proposals aim at optimizing the position of gating pulses to achieve a high degree of harmonic cancellation.

The motivation underlying this thesis is to find an effective way to achieve a near-optimal reduction of total harmonic distortion (THD) of a single-phase inverter voltage output using multiple PWM inverters operated in parallel with synchronized transistor gating. Upon studying the other methods in this field, the author has found some harmonic reduction methods suffer from some kind of complexity and so he set out to find a straight-forward way to achieve harmonic cancellation. In order to develop this strategy, the following plan was adopted:

- Review different alternatives for determining the inverter switch on-times for fixed frequency modulation systems and examine the feasibility of each alternative for our case. To this end, we have chosen naturally sampled PWM.
- Investigate the implementation of operation of multiple parallel-connected PWM inverters and decide if the implementation is possible using the available equipment in the Power Electronic Lab at the University of Calgary (including programming firmware). MOSFET transistor modules (constructed by Jason Panel at the University of Calgary) and BJT devices were used to implement the inverters together with control and gating functions provided by a PICF877 microcontroller (designed by Richard Galambos at the University of Calgary).
- Investigate the theoretical principle of harmonic cancellation and determine the best algorithm (discussed in Chapter 3).
- Examine harmonic cancellation methods based on experimental results obtained in the laboratory. Then modify and improve our harmonic reduction technique.
- Simulate the system operation using MATLAB software, and return to the lab to implement the modifications.
- Examine the experimental results to check the degree of harmonic cancellation of the parallel inverters and compare with theory as developed in MATLAB.
1.6 Thesis Outline

This thesis is composed of six chapters which discuss the characterization of harmonic cancellation techniques to reduce the total harmonic distortion (THD) in general and in the particular case of parallel synchronously operated PWM inverters.

In Chapter 2 several PWM techniques are presented. The basic principles of single-phase inverter design are discussed, including, inverter topologies and gating strategies.

Presented in Chapter 3 is the concept of harmonic distortion including a mathematical analysis of the system, used to characterize the proposed harmonic cancellation strategy.

In Chapter 4, the simulation results (using MATLAB) are presented for several cases, ie, 2-level and 3-level PWM for different modulation index values and different carrier-to-sinusoid frequency ratios (fc/fs) for 1, 2, and 3 inverters. A Fourier analysis is presented for harmonics up to 200 times the fundamental frequency. The THD is also calculated using these harmonic components.

In Chapter 5 the experimental results corresponding directly to the cases examined in Chapter 4 are presented. As expected, the experimental cases have more THD than in the corresponding simulation cases. The difference between simulation and experimental results is discussed.

The conclusions of this thesis and some suggestions for future work are presented in Chapter 6.
Chapter 2

Single-Phase Inverter Topologies and Transistor Gating Methods

2.1 Introduction

A solid-state power electronic circuit that changes electric power from AC-to-DC or from DC-to-AC or from one level to another is known as a power processor or power conditioner. An older name is static converter (because it contains only stationary parts). In general it is called a power converter [8].

There are two classes of DC-to-AC converters (which are also called inverters): voltage source inverters (VSI) and current source inverters (CSI). Both types are presented in this chapter. It is important to note that the performance of these inverters is affected by the type of transistor control technique used. There are different techniques presented in this chapter including square-wave, modified square-wave, and pulse width modulation (PWM) techniques. In this thesis, the focus is on single-phase inverters employing sine-wave PWM techniques. A sine-wave PWM type inverter has the primary advantage of lower output voltage or current distortion, and in the case of grid-connected inverters, improved output power factor control. This implies a substantial reduction in filter requirements on both AC and DC sides. A brief review of single-phase PWM inverter topologies including half-bridge, full-bridge, and multilevel inverters is presented in this chapter.

The PWM process for inverters can be categorized as one of three types: sinusoidal pulse width modulation (SPWM), selective harmonics elimination (SHE), and trapezoidal PWM. We will describe all of these types of modulation methods later in this chapter.
2.2 Power Semiconductor Devices

The semiconductor switching device technology has significant impact on the size, type and performance of the overall power converter used in the power electronics field. In general, the semiconductor switch development has played a great role in industry in general and power electronics evolution in particular.

The ideal switching device would have a high current-rating in its on-state and a high voltage-rating in its off-state. When the ideal device is conducting current (on), it would have zero on-resistance and zero voltage drop, and in the off-state it would have zero leakage current. This ideal device would also have high temperature capability, instantaneous turn-on and turn-off characteristics, and a reasonable price.

The group of power semiconductor devices that are primarily used for power conversion includes: thyristor (SCR), gate turn-off thyristor (GTO), insulated gate bipolar transistor (IGBT), and the power metal-oxide semiconductor field effect transistor (MOSFET). Generally, the SCR and GTO are employed for high power (megawatt) applications and the IGBT and MOSFET are employed for kilowatt applications. Among these devices, both SCR and GTO are known as current controlled devices, while the MOSFET and IGBT are voltage-controlled devices. The MOSFET switch, which is illustrated in Fig. 2.1, possesses a fast switching response time with low switching losses even at high switching frequencies. It is usually limited to low power applications (at present, power levels below about 100kW). In the off-state the MOSFET has a dc gate to source impedance which is practically infinite \((10^9 \text{ - } 10^{11} \text{ Ohms})\). The on-resistance is relatively very low, so MOSFET devices are easy to drive. The drive voltage (gating voltage) which is the voltage applied between gate and source to switch the MOSFET on must exceed a threshold value, typically 4V to 6V. The voltages of 10 to 20V are actually necessary to ensure that the MOSFET is fully switched on. Reducing the driver voltage below the threshold voltage value will turn off the MOSFET [9].
Power MOSFETs handle low current (e.g. 1A) to medium current values (e.g. 50A). Switching losses are usually very low, even at high switching frequencies due to quick turn-on and turn-off (a typical turn-on time is 43 ns and turn-off time is 47 ns). There is no necessity to use external anti-parallel diodes in inverter design because a body diode inherently exists within the device. Due to their ruggedness, low cost and excellent performance, the power MOSFET is a relevant switch for inverters of low (e.g. 60Hz) or high (e.g. 1MHz) switching frequencies. Based upon these characteristics of the MOSFET in low output power applications; it is often the power switching device of choice for power levels from low power (1W) to medium power (10kW) levels. At low power levels (even less than 1W), the more conventional bipolar junction transistor (BJT) is sometimes used (being a low cost component for low power applications), while at medium power levels (5kW to 200kW), the insulated gate bipolar transistor (IGBT) is often used as it possesses the desirable switching characteristics of both the MOSFET and the BJT at these power levels. For low and medium power applications, the gate turn-off thyristor (GTO) is often used, as it has relatively the high power capabilities of a thyristor SCR device but can also be turned off like the lower power switching transistors discussed above.

2.3 Power Converter Classification

The most common classification of Power converters is AC-to-DC converters (also called rectifiers); DC-to-AC converters (also called inverters); DC to DC converters (e.g. choppers); and AC-to-AC converters. A practical power electronic system may utilize more than one of these of these types. In this section, we focus on common types of inverters. The most common types of single-phase inverters are now discussed.
Voltage Source Inverter (VSI)

This type of inverter is the most common type of power inverter, operating with a voltage source supply or with a capacitor on the input (DC) side of the inverter. The input DC voltage may be a battery, photo-voltaic source or, as is most commonly the case, obtained by rectifying and filtering the AC line voltage. Fig. 2.2 shows a typical circuit diagram of a single-phase full-bridge Voltage Source Inverter (VSI), where each switch represents a semiconductor power switching device (e.g. BJT). The main advantage of this type of inverter is that it has no difficulties to drive a single load or multiple loads in parallel since a VSI operates as a voltage source. The main topology of this inverter is the four semiconductor switches; each is shunted by a freewheeling diode (except for the MOSFET, which, as noted above contains an internal body diode). The diode prevents inductive current interruption and provides protection against transient over-voltage, which may cause reverse breakdown of the semiconductor switches. The switches in the inverter are controlled by gate pulses. The gate signal contains one or more pulses per half-cycle of the fundamental output voltage waveform.

![Fig. 2.2 Single-phase voltage source inverter (or H-bridge inverter)](image_url)
Another class of inverters is the Current Source Inverter (CSI) which uses a DC link inductor to smooth the DC link current. The inductor behaves as a current source. It is obvious that the current flows to the load through the semiconductor switches branches, so the load must clearly be non-inductive to avoid infinite voltage spikes across the switches (alternatively the CSI output can be capacitor filtered). As it is shown in Fig. 2.3, that a pair of switches is connected in series with one inductor for each voltage bus in order to create AC current in the load. It is important to recall that since a CSI operates as a current source, in almost all cases it is necessary to employ a single load. Current source GTO PWM devices have been used for many years, especially in high-voltage and high-power applications [10], therefore CSIs have limited applications and are mainly used for high power motor drive systems. We will focus only on the VSI class of inverter.

![Fig. 2.3 Single-phase current source inverter](image)

### 2.4 Basic Inverter Topologies

Generally speaking, there are three different single-phase inverter topologies: the half-bridge inverter, the full-bridge inverter, and the multi-level inverter. A brief description of each topology now follows.
**Half-Bridge Single-Phase Inverter Topology**

The half-bridge single-phase inverter in its simplest form is shown in Fig. 2.4 (a). It has two semiconductor switches, two diodes, and a DC input that is centre-tapped, having two identical DC supplies connected in series, in order to produce a symmetrical AC output voltage waveform. As noted above the diodes are needed to protect the switches when these switches have to carry currents in the reverse direction (particularly, in the case of inductive loads). Most single-phase loads are inductive in nature, as shown in Fig. 2.4.

It is useful to know that the centre-tap point of the DC voltage is not provided to many inverters, but may be synthesized by placing two relevant and equal electrolytic capacitors in series across the input DC source as shown in Fig. 2.4 (b). These capacitors behave as a voltage source when both are fully charged. It is obvious that there are two equal resistors in parallel with the capacitors to ensure that the voltages across the capacitors are equal and to provide the paths for the capacitors currents during discharge time once the half-bridge is switched off.

![Half-Bridge Inverter Diagrams](image-url)

Fig. 2.4: (a) Half-bridge inverter with dual supply and (b) with single supply
Full-Bridge Single-Phase Inverter Topology

The circuit diagram of a single-phase full-bridge inverter, also known as an H-bridge inverter, is shown in Fig. 2.5 (for convenience, we have simply re-drawn the circuit of Fig. 2.2). This circuit comprises four controlled switches, with an anti-parallel diode across each switch. The load is connected across the middle of the bridge thus forming the “H-shape” structure. As seen in Fig. 2.5, the full-bridge inverter topology consists of two inverter “legs”; devices 1 and 3 constitute one leg and devices 2 and 4 are the other leg in the single-inverter (a three-phase full-bridge inverter has three legs). Generally the full-bridge converter topology is preferred over the half-bridge topology, especially at higher power applications (ie, above 500W).

![Circuit Diagram](attachment:Fig_2_5.png)

Fig. 2.5 Single-phase full-bridge (H-bridge) inverter

It is obvious that with this configuration, the maximum output voltage is now twice than that of the half-bridge inverter of Fig. 2.4 (b) because the full input voltage can be applied across the load compared with one-half of this voltage for half-bridge circuit. This means that for the same output power and input voltage, the average switch current is one-half of that for half-bridge inverter. It is clear that at higher power and high voltage level there is less switching devices are required and consequently reduction in switching losses. At high voltage, the losses are reduced in the system for many types of the loads along with a reduction in wiring cost. Alternatively, for the same output power and output
voltage, each power device in the full-bridge configuration has half the peak reverse-voltage compared to the half-bridge inverter. This results in a much less costly device and offsets the cost of having more power devices in the full-bridge inverter.

Referring again to Fig. 2.5, current flows through switches T1 and T4 in series (they must be on simultaneously, while T2 and T3 are both off) for a positive output voltage, whereas current flows through switches T2 and T3 in series (also must be on simultaneously, while T1 and T4 are both off) for a negative output voltage. To obtain an output of zero voltage across the load there are two possible cases: either switches T1 and T2 are on (while T3, T4 are off) or switches T3 and T4 are on (while T1, T2 are off). This is discussed further in section 2.5.2. Note that it is necessary that the two switches in the same leg of the H-Bridge (ie, T1, T3) must not be simultaneously on (for more than a few microseconds). This would short circuit the DC voltage source. This condition is called a “shoot through” and normally the gating of the switching elements is programmed in a way to avoid this shoot through (as an extra precaution, a hardware circuit may be added to the transistor driver to avoid shoot through).

**Multilevel Inverter Topology**

In recent decades, because of tremendous development in industry, the demand on higher power converters at level of megawatts has enhanced. AC drive of such high power level is connected to the medium-voltage grid network. It is evident that the direct connection of a single power semiconductor switch to the medium voltage grids (North American electric utilities define medium-voltage as line-to-line voltages of 2.3, 3.3, 4.16, 6.9, 11.6, or 13.9 kV) is very difficult. For this reason, a new group of multilevel inverters has developed as one of possible alternatives for operating with higher voltage levels [11, 12, 13]. These inverters has high capability to provide the necessary power required for some applications using static VAR compensation, AC variable speed machines, active power filters. Multilevel voltage source inverters have outstanding ability to withstand the above mentioned grid voltages without the use of transformers or series connected synchronized switching devices with relatively low output harmonics. There are three main multilevel inverter topologies: diode-clamped (sometimes called
neutral-point clamped), capacitor-clamped, and cascaded multilevel inverters with separate DC sources. We only focus here on the first topology because of the simplicity of the circuit.

The multi-level inverters technique was first introduced as neutral-point clamped three-level inverters by A. Nabae in 1980 [14]. So, we will demonstrate the principle of three-level inverter operation, and then discuss how it can be generalized to a higher number of levels. The neutral-point clamped (NPC) three-level inverter, as shown in Fig. 2.6, has a zero DC voltage centre point (p refers to the positive source potential, z refers to the zero source potential, and n refers to the negative source potential). One can conceive of a more obvious multilevel inverter where only three semiconductor power switches are used, however, the main benefit of the NPC configuration shown in Fig. 2.6 is that each of the switches must block only one-half of the DC link voltage. This is also a benefit compared to the full-bridge inverter of Fig. 2.5. But the drawback of this system is the issue of the voltage balance across the two series-connected capacitors that are connected across the DC source. First method to solve this problem is to connect each of the capacitors to its own isolated DC supply and the second solution is to balance the capacitor voltage by feedback loop. By this feedback control system we can adjust the time that each inverter leg is connected to the centre point so as to reduce the average current flow to the centre point to zero [15, 16].

![Fig. 2.6 Single-phase three-level diode-clamped inverter topology](image)
In the case of three levels, the switches are controlled in away that only two of the four switches in each half circuit are turned on at any time. When switches $T_{a1}$ and $T_{a2}$ are turned on, the positive of supply voltage is applied to the phase-a terminal; when $T_{a2}$ and $T_{a3}$ are turned on, the centre point voltage (zero volts) is applied, and when $T_{a3}$ and $T_{a4}$ are turned on, the negative of the supply voltage is applied.

The variables $m_{x1}$, $m_{x2}$ ($x = a$, or $b$) is considered as a logical one when switch combinations $(T_{x1} - T_{x2})$, $(T_{x2} - T_{x3})$, $(T_{x3} - T_{x4})$ are conducting, respectively, and zero otherwise, the two terminal voltages can be written as:

$$V_{az} = V_{dc} (m_{a1} - m_{a3})$$  \hspace{1cm} (2.1)

$$V_{bz} = V_{dc} (m_{b1} - m_{b3})$$  \hspace{1cm} (2.2)

Hence the line-to-line voltage is $V_{ab} = V_{az} - V_{bz}$,

$$\therefore V_{ab} = V_{dc} (m_{a1} - m_{a3} - m_{b1} + m_{b3})$$  \hspace{1cm} (2.3)

From equation 2.1, we conclude that $V_{az} = +V_{dc}$ when $m_{a1} =$ logic 1 (ie, both switches $T_{a1} - T_{a2}$ are conducting, $V_{az} = -V_{dc}$ when $m_{a3} =$ logic 1 (ie, both switches $T_{a3} - T_{a4}$ are conducting) and $V_{az} = 0$ when only both switches $T_{a2} - T_{a3}$ are conducting.

So three levels of voltage will be generated for line to midpoint ($V_{az}$ or $V_{bz}$).

From equation 2.3, the line-to-line voltage $V_{ab}$ pattern is as follows:

1. $V_{ab} = +2V_{dc}$ when both $m_{a1}$ and $m_{b3}$ are logic 1 (ie, both switches $T_{a1} - T_{a2}$ in leg a and $T_{b3} - T_{b4}$ in leg b are conducting simultaneously).

2. $V_{ab} = +V_{dc}$ when $m_{a1} =$ logic 1 (ie, both $T_{a1} - T_{a2}$ in leg a and $T_{b2} - T_{b3}$ in leg b are conducting simultaneously).

3. $V_{ab} = 0$ volt when all terms $m_{a1}$, $m_{a3}$, $m_{b1}$, $m_{b3}$ are logic 0 (ie, this occurs when switches $T_{a2} - T_{a3}$ in leg a and $T_{b2} - T_{b3}$ in leg b are conducting simultaneously).

4. $V_{ab} = -V_{dc}$ when either $m_{a3} =$ logic 1 (ie, both switches $T_{a3} - T_{a4}$ in leg a and $T_{b2} - T_{b3}$ in leg b are conducting simultaneously) or $m_{b1} =$ logic 1 (ie, both switches $T_{b1} - T_{b2}$ in leg b and $T_{a2} - T_{a3}$ are conducting simultaneously).
5. \( V_{ab} = -2V_{dc} \) when both \( m_{a3} \) and \( m_{b1} \) are logic 1 (ie, both switches \( T_{a3} - T_{a4} \) in leg a and \( T_{b1} - T_{b2} \) in leg b are conducting simultaneously).

It is obvious that the line-to-line voltage created by this method consists of five levels and this leads to reduced harmonic distortion of the output voltage (note that each half-cycle of operation has only three levels, hence the name of the inverter).

The technique of diode-clamping to DC link voltages can be developed to the higher number of the voltage levels [17]. As the number of levels increases, the resultant output waveform, increasingly staircase like, approaches the desired target with a significant reduction in harmonic distortion, and approaching zero distortion as the number of levels increases [18, 19]. Fig. 2.7 shows a circuit implementation for a four-level inverter. It is worthy to mention again that the voltages across the semiconductor switches are limited by conduction of the diodes connected to the various DC levels. For the case of the four-level inverter, switches \( T_{a1}, T_{a2} \) and \( T_{a3} \) are turned on simultaneously, then \( T_{a2}, T_{a3} \) and \( T_{a4} \) and so forth to produce the required voltage levels.

Fig. 2.7 Single-phase four-level diode-clamped inverter topology
We can summarize the most outstanding characteristics of multilevel inverters technique as follows. They can generate desirable output voltages, which contains insignificant harmonic distortion, and lower $\text{dv/dt}$. These inverters can operate with a lower switching frequency. Note that these benefits over other topologies, are only limited for high power, medium voltages applications, so this topology is not useful for low voltage, low power applications which is the focus of this thesis.

2.5 Single-Phase Full-Bridge Transistor Gating Techniques

There are many switch-gating techniques for single-phase full-bridge inverters. We now consider the more commonly employed techniques.

2.5.1 Square-wave Gating Technique

This type of inverter gating, sometimes called two-level square-wave inversion, produces a square-wave output as shown in Fig. 2.8, and is the simplest way to provide transistor gating for an inverter. For single-phase applications, the circuit topology can be either a half-bridge or a full-bridge topology, but we will discuss this gating method in the context of the full-bridge inverter, ie, consisting of a DC source, four switches, and the load as shown in Fig. 2.5. The switches are power semiconductor devices that are turned on and off in the correct sequence, at a certain frequency. Each phase leg is operated with a 50% duty cycle. The actual gating sequence is discussed below.

\[
\begin{align*}
\text{Fig. 2.8} & \quad \text{Square-wave output voltage}
\end{align*}
\]
Although this type of inverter operation is the simplest approach, it is no longer commonly used. It produces the lowest quality of power because a square wave contains a large numbers of harmonics. It may also cause problems in some applications such as switching stress for solid-state equipment; excessive heating for high inductive loads; and noise in some devices (audio-video equipment).

The operating sequence of this inverter is as follows. Referring to Fig. 2.5, the current flows to the load in the first half cycle, through T1 and T4 (they must be on simultaneously) while T2, T3 are off. The current flows to the load in second half cycle through T2 and T3 (they must be on simultaneously) while T1, T4 are off.

The switched output voltage of this inverter can be analyzed by Fourier series as the sum of a series of harmonic frequencies. Inspection of the square-waveform shown in Fig. 2.8 indicates that there are no sine terms, no even harmonics, and that there is quarter-waveform symmetry. Quarter-wave symmetry permits us to calculate Fourier amplitude harmonic components by integrating over one quarter of the fundamental output voltage shown in Fig. 2.8:

\[
V_{ab(n)} = \frac{4}{\pi} \int_{0}^{\pi/2} V_{dc} \cos(n\theta) d\theta \quad \text{(for odd values of } n) \tag{2.4}
\]

\[
V_{ab(n)} = 4 \frac{V_{dc}}{n\pi} \quad \text{(for odd } n) \tag{2.5}
\]

\[
V_{ab(n)} = 0 \quad \text{(for even } n) \tag{2.6}
\]

where \( \theta = \omega t \), and \( \omega \) is the angular frequency of the fundamental.

If \( n=1 \), this is the amplitude (ie, the peak value) of the fundamental component:

\[
V_{ab(1)} = \frac{4}{\pi} V_{dc} = 1.2732 \ V_{dc} \tag{2.7}
\]

If \( n=3 \),

\[
V_{ab(3)} = \frac{4 \times V_{dc}}{3\pi} = 0.4244 \ V_{dc} \quad \text{and so forth for all the odd harmonics.} \tag{2.8}
\]
To calculate the total harmonic distortion (THD) of the square-wave inverter we can sum the squared values of the non-fundamental harmonic components, or alternatively:

\[ V_{1\text{rms}} = \frac{1}{\sqrt{2}} V_{ab(1)} \quad (\text{rms value of the fundamental voltage term}) \]  

\[ V_{ab(\text{rms})} = V_{dc} \quad (\text{rms value of the inverter output voltage waveform}) \]  

\[ \text{THD} = \sqrt{\frac{V_{ab(\text{rms})}^2 - V_{1\text{rms}}^2}{V_{1\text{rms}}^2}} = 48.4\% \]  

We conclude that the THD of a square-wave inverter is very high.

### 2.5.2 Modified Square-wave Gating Technique

The modified square-wave inversion method is similar to the simple square inversion method but reduced THD is possible by inserting zero-voltage intervals between the positive and negative output voltage levels. A typical waveform for this inversion technique is shown in Fig. 2.9. It is obvious that for both positive and negative half cycles, there is an equal angular period (\( \alpha \)) during which the output load voltage is zero. The root mean square (RMS) magnitude of the switched output voltage controlled and adjusted by changing the phase delay angle (\( \alpha \)). What is less obvious is how the harmonic spectrum changes as the phase-delay angle, \( \alpha \), changes. To obtain an approximate minimum THD with this inverter operation, typically (\( \alpha \)) is taken to be 45°.

![Fig. 2.9 Modified square-wave output voltage](image-url)
The gating sequence for modified square-wave operation is as follows (refer again to Fig. 2.5). In the first half cycle, T1, T4 are on (T2, T3 are off), thus producing a positive voltage across the load. Next, during the period $\alpha$, switches T3, T4 are on to produce zero volts across the load. In the second half cycle, T2, T3 are on (T1, T4 are off), thus producing a negative voltage across the load. To complete the cycle, and for a period $\alpha$, only T1, T2 are on to produce zero volts across the load.

The peak harmonic magnitude of the output voltage is:

$$V_{ab(n)} = \frac{4}{\pi} \int_{0}^{(\pi/2-\alpha/2)} V_{dc} \cos n\theta d\theta \quad \text{(for odd n, else } V_{ab(n)} \text{ is zero.)} \quad (2.12)$$

$$V_{ab(n)} = \frac{4V_{dc}}{\pi n} \frac{\cos n\alpha}{2} \quad \text{(Where n is odd, else } V_{ab(n)} \text{ is zero.)} \quad (2.13)$$

Following a similar procedure as we used for the square-wave technique to calculate THD, the modified square-wave output voltage harmonic components can be found taking $\alpha = 45^\circ$, then the THD of the modified square-waveform is calculated to be 30% which is much less than that of the square-wave inversion technique. Thus, due to the simplicity of the gating method, and the common practice of employing modified square-wave gating in an inverter without the need for an output filter, this type of inversion is very common in power inverters operating at lower power levels (less than about 3kW). The problems discussed for the square-wave inversion method are still present but to a lesser degree. However, in the near future, as sine-wave PWM gating methods become more economical, modified square-wave inverters may become less popular.

2.5.3 PWM Gating Techniques

In general, all modulation techniques aim to create a series of switched pulses. But these pulses contain unwanted harmonic frequencies which should be reduced to acceptable limit. There are two objectives behind any pulse width modulation (PWM) technique. The first purpose is to define the appropriate inverter switch ON times to
create desirable low frequency output voltage or current (e.g. at a frequency of 60Hz).
The second purpose is to arrange the switching instances in an optimum way to reduce
undesirable harmonics of the system, semi conductor devices losses, or to satisfy aspects
of system performance improvement.

For PWM inverters, the input DC voltage is essentially constant (aside from a
possible ripple). Therefore, the inverter gating method must control the magnitude and
frequency of the AC output voltage. Various PWM techniques include [20-26]:

- Sinusoidal Pulse Width Modulation (most common)
- Selective Harmonic Elimination PWM
- Trapezoidal PWM
- Space-Vector PWM
- Instantaneous Current Control PWM
- Hysteresis Band Current Control PWM
- Sigma-Delta Modulation

Despite the wealth of researches relating to PWM techniques, the first three methods
are the most popular and are now discussed in some detail.

**Sinusoidal Pulse Width Modulation (SPWM) Technique**

Sinusoidal pulse width modulation is used for both voltage and current source
inverters [27, 28, 29]. This technique is the oldest and most straightforward modulation
strategy in which a low-frequency target reference waveform (usually a sine-wave) is
compared to a high frequency carrier waveform. The advantage of pulse width
modulation over square-wave or modified square-wave operation is an improved
harmonic profile (ie, the harmonics are “pushed” to higher frequencies and are more
easily filtered out).
There are many SPWM techniques such as naturally sampled PWM, regular sampled PWM, and direct PWM. In each case the desired output voltage is achieved by comparing the desired low frequency reference waveform, which is called the modulating signal, with a high frequency triangular wave (called the carrier) as depicted in Fig. 2.10. Note that the inverter output is switched to the upper DC bus when the reference waveform is greater than the triangle wave carrier and the inverter output is switched to the lower DC bus when the carrier waveform is greater than the reference waveform. Note also that over one period of the triangle waveform; the average voltage applied to the load is proportional to the value of the modulating signal (assumed constant) during this period. The resulting square waveform contains desired low frequency components, with the higher frequency components close to the carrier frequency. It is obvious that the root mean square value of the AC voltage waveform is still equal to the DC input voltage, and therefore the THD is not affected by the PWM process. The harmonic components are only shifted into the higher frequency levels which can be easily filtered out by any adequate simple filter.

For sinusoidal modulating signal of amplitude $A_m$, and triangular carrier of amplitude of $A_c$, the ratio $M = A_m/A_c$ is known as the modulation index, as shown in Fig.2.10. Note that controlling the modulation index therefore controls the amplitude of the fundamental component of the output voltage. This is partially illustrated in Fig. 2.10 where the output current, $i_d(t)$, is shown as would be observed with inductive filtering (as was experimentally also done for the research underlying this thesis). Note that $i_d(t)$ contains very few of the switching harmonics present in the $v_{ab}(t)$ inverter voltage waveform. With a sufficiently high carrier frequency, a large number of switching instances per cycle will result in switching harmonics that are much higher than the fundamental sinusoidal frequency, which can be fairly easily filtered out. In Fig. 2.10 we illustrate sinusoidal PWM for a carrier frequency, $f_c$, to sinusoidal modulating frequency, $f_s$, ratio of 9. Note that if the switching frequency is too large, these results in an increased power loss (commonly called switching loss). Typically switching frequencies in the 1 to 15 kHz range are considered adequate for low power systems applications, without excessive switching losses.
Fig. 2.10 Illustration of the SPWM technique with M=0.9, 2-level, fc/fs=9

Note that the SPWM process works well for the region of M≤1. The fundamental components amplitude of the voltage waveform is linearly increased with M in this region. But this relation is not longer be linear for the region M>1. The region M>1 is called over-modulation region. As it is shown in Fig.2.11, that some switching cycles are skipped and the shape of the output voltage waveform is not fully under control. Consequently, the output voltage waveform becomes distorted and therefore contains low frequency harmonics which will contribute to increase the THD. Thus, in general, over-modulation is rarely used for the operation of power inverters and must be avoided in
UPS systems which require minimum distortion in the output voltage. An exception might be the case where the inverter DC input voltage drops sufficiently that the desired filtered output voltage would drop in rms value excessively unless over-modulation is employed.

![Diagram](image)

Fig. 2.11 Illustration of over-modulation: M=1.3, fc/fs=11, 2-level

*Selective Harmonic Elimination (SHE) Technique*

This technique is one of the first forms of PWM developed [30]. It is also called optimum PWM. The SHE technique has been researched since the four decades. This technique possesses several outstanding characteristics over the other traditional modulation methods. This strategy deals successfully with a low carrier frequency to fundamental frequency ratio (ie, low fc/fs) cases, and has advantage of reducing harmonic distortion via a direct control of output voltage waveform harmonics.
The shortcoming of the Sinusoidal PWM is having a large number of switching instances per cycle of the modulating waveform, and consequently high switching losses. So, SHE is the optimum solution if the switching frequency is not high because it can optimize PWM waveforms to reduce the total distortion of the system. With SHE only we can eliminate selected unwanted harmonics with the smallest number of switching instances. In practice, to implement this method a very organized set of look-up tables is required. This technique can be used with the VSI and CSI to remove unwanted harmonics. Fig. 2.12 shows the inverter unfiltered waveform produced using this technique. Usually, the lowest non-fundamental harmonics in this waveform have the priority to be eliminated.

![Fig. 2.12 Selective harmonic elimination technique](image)

The idea of this technique is to define a set of gating angles that is necessary to eliminate certain unwanted harmonics at different value of modulation index. Consequently, a group of non-linear equations is required to solve, and the results are stored in look-up tables for the gating controller (discussed in greater detail below). So, the SHE PWM based methods can provide the better quality of control compared to other PWM methods. However, the disadvantage of this method is that in the case of increasing number of required switching angles, a large memory space is required to store this amount of data.

Referring to Fig. 2.12, let us, for example, now illustrate the mathematical procedure of computing the required switching instances to eliminate the 3rd and 5th harmonics of a single-phase full-bridge inverter operating with a 2-level unfiltered inverter output waveform (ie, we are referring to Figs. 2.5 and 2.12).
Consider the Fourier series for the unfiltered inverter voltage waveform:

\[ f(\theta) = a_0 + a_1 \cos \theta + a_2 \cos 2\theta + a_3 \cos 3\theta + \ldots + a_n \cos n\theta + b_1 \sin \theta + b_2 \sin 2\theta + \ldots + b_n \sin n\theta \]

(Where \( \theta = \omega t, \omega = \text{fundamental angular frequency} \)).

A standard Fourier analysis yields the coefficients:

\[ a_0 = \frac{1}{2\pi} \int_{0}^{2\pi} f(\theta) d\theta \]  \hspace{1cm} (2.15)

\[ a_n = \frac{1}{\pi} \int_{0}^{\pi} f(\theta) \cos n\theta d\theta \quad \text{for } n \geq 1 \]  \hspace{1cm} (2.16)

\[ b_n = \frac{2}{\pi} \left( \int_{0}^{\pi} f(\theta) \sin n\theta d\theta \right) \quad \text{for } n \geq 1 \]  \hspace{1cm} (2.17)

Where \( a_0 \) is the DC value of the waveform, \( a_1 \) and \( b_1 \) are the amplitudes (ie, the peak values) of the fundamental cosine and sine terms respectively, and \( a_n \) and \( b_n \) are the amplitudes (ie, the peak values) of the harmonic cosine and sine terms respectively.

Since \( f(-\theta) = -f(\theta) \), then \( a_n = 0 \) for all \( n \), there are no cosine terms. Also, \( f(\theta + \pi) = -f(\theta) \), there are no even harmonics (ie, all \( b_n = 0 \) for even \( n \)). Utilizing quarter wave symmetry, the Fourier sine coefficients become:

\[ b_n = \frac{4}{\pi} \int_{0}^{\pi/2} f(\theta) \sin n\theta d\theta \quad \text{(for odd } n \text{, else } b_n = 0 \text{ for even } n. \text{)} \]  \hspace{1cm} (2.18)

If, for example, we eliminate the third and fifth harmonics from the waveform, the following procedure applies:

\[ b_1 = \frac{4E}{\pi} \left\{ \int_{0}^{\pi/4} \sin x dx + \int_{\pi/4}^{\pi/2} \sin x dx + \int_{\pi/2}^{\pi} \sin x dx + \ldots + \int_{\frac{\pi}{4}}^{\frac{\pi}{2}} \sin x dx \right\} \]

\[ b_1 = \frac{4E}{\pi} \left\{ 1 - 2\cos \alpha_1 + 2\cos \alpha_2 - 2\cos \alpha_3 \ldots 2\cos \alpha_n \right\} \]  \hspace{1cm} (2.19)

\[ b_3 = \frac{4E}{3\pi} \left\{ \int_{0}^{\pi/12} \sin 3x dx + \int_{\pi/12}^{\pi/6} \sin 3x dx + \int_{\pi/6}^{\pi/4} \sin 3x dx + \ldots + \int_{\frac{\pi}{12}}^{\frac{\pi}{6}} \sin 3x dx \right\} \]

\[ b_3 = \frac{4E}{3\pi} \left\{ 1 - 2\cos 3\alpha_1 + 2\cos 3\alpha_2 - 2\cos 3\alpha_3 \ldots 2\cos 3\alpha_n \right\} \]  \hspace{1cm} (2.20)

and similarly, \( b_5 = \frac{4E}{5\pi} \left\{ 1 - 2\cos 5\alpha_1 + 2\cos 5\alpha_2 - 2\cos 5\alpha_3 \ldots 2\cos 5\alpha_n \right\} \)  \hspace{1cm} (2.21)
where $E = V_{dc}$ is the inverter DC input voltage.

Now $b_1$ is the peak value of the fundamental waveform, but it is normal to specify the required rms value of the fundamental, $V_{1rms}$, so $b_1$ can be expressed as:

$$b_1 = \sqrt{2} \ V_{1rms}$$  \hspace{1cm} (2.22)

So the unknowns $\alpha_1, \alpha_2, \alpha_3$ can be obtained by solving a group of three nonlinear equations:

$$\sqrt{2} \ V_{1rms} = b_1 = \frac{4E}{\pi} \ {1 -2\cos \alpha_1 + 2\cos \alpha_2 -2\cos \alpha_3 \ldots 2\cos \alpha_n}$$ \hspace{1cm} (2.23)

$$0 = b_3 = \frac{4E}{3\pi} \ {1 -2\cos3 \alpha_1 + 2\cos3 \alpha_2 -2\cos3 \alpha_3 \ldots 2\cos3 \alpha_n}$$ \hspace{1cm} (2.24)

$$0 = b_5 = \frac{4E}{5\pi} \ {1 -2\cos5 \alpha_1 + 2\cos5 \alpha_2 -2\cos5 \alpha_3 \ldots 2\cos5 \alpha_n}$$ \hspace{1cm} (2.25)

Trapezoidal Pulse Width Modulation (TPWM)

This technique is another PWM control method that has the advantage of being simpler than selective harmonic elimination. The principle of this pulse width modulation technique is illustrated in Fig. 2.13. In this technique the triangular carrier waveform is compared with a reference trapezoidal waveform so that intersection points of the carrier waveform and modulating waveform determine the switching instances. It is obvious that the triangle wave is not appeared in the centre 60° interval of each half cycle so as to not allow any switching in this region [31, 32, 33]. This process is highly recommended for current source inverters operation. This technique is not applicable at low switching frequencies in contrast with selective harmonic elimination.
2.6 Chapter Summary

In this chapter, a review of single-phase inverter topologies is presented, with an emphasis on the full-bridge (ie, H-Bridge) inverter that is often used for power levels in the range of about 500W to 10kW. Also in this chapter, several gating methods are reviewed with an emphasis on commonly used sine-wave pulse width modulation (SPWM) inversion techniques. SPWM inversion is used for a wide range of applications because a high switching frequency can be effectively filtered out without costly filter components. A sinusoidal PWM inverter has flexibility in terms of fundamental frequency and phasing control (ie, the modulating waveform can be any reasonable frequency and can also be synchronized to some other waveform such as the utility voltage waveform) together with voltage amplitude control (which is generally not possible with square-wave and modified square-wave techniques). However, if the switching frequency is too high, switching losses become excessive, which limits the use of this technique to some high power applications where the lower switching frequencies of the trapezoidal PWM or better yet selective harmonic elimination gating methods become more attractive.
Chapter 3

Harmonic Analysis Background and Multiple Inverter Harmonic Cancellation

3.1 Introduction

In this chapter the Naturally Sampled Pulse Width Modulation (NSPWM) technique is reviewed, along with a mathematical analysis of both 2-level and 3-level NSPWM. The parallel operation of multiple inverters has been proposed by others as a means of reducing the total harmonic distortion in the output voltage or current waveform of a multi-inverter system. In this chapter we also present our version of multiple inverter harmonic reduction. Our approach makes use of a triggering signal that is fed to all of the multiple inverters. Each inverter employs an off-line computed NSPWM pattern that is delayed with respect to the triggering signal to produce a near-minimum total harmonic distortion in the load voltage waveform. This approach is discussed in some detail later in this chapter. In the following chapter we characterize the degree of harmonic distortion reduction with respect to parallel-inverter operating parameters.

3.2 Generation of Naturally Sampled PWM

As mentioned in Chapter 2 naturally sampled pulse width modulation NSPWM is the most popular and straightforward PWM strategy for single-phase inverters. The formation of gating (pulsing) logic for 3-level PWM with modulation index M=0.9 using double edge NSPWM is illustrated in Fig. 3.1 for a single-phase inverter. The intersection points of the carrier wave and modulating sine wave can be defined clearly via nonlinear equations. Fig. 3.1 shows a reference sine wave with a carrier wave whose frequency is six times that of the sine wave (i.e., $f_c/f_s=6$, where $f_c$ is the carrier frequency and $f_s$ is the frequency of the reference modulating sine waveform). Referring to Fig. 3.1,
we now derive an equation corresponding to the $i^{th}$ falling edge of the inverter output voltage waveform:

$$y_i = \frac{R(\alpha_i - (i-1)\frac{\pi}{R})}{\pi}, \quad i = 1, 3, 5, ..., R-1$$  \hspace{1cm} (3.1)$$

Where $y_i$ (for odd $i$) indicates that the output voltage changes from $V_{dc}$ to 0, $R = \frac{f_c}{f_s}$ which is the ratio of the carrier frequency to the modulating sine wave frequency, $\alpha_i$ is the angular value of horizontal-axis at the intersection point as identified in Fig.3.1. Also:

$$y_i = 1 - \frac{R(\alpha_i - (i-1)\frac{\pi}{R})}{\pi}, \quad i = 2, 4, 6, ..., R$$  \hspace{1cm} (3.2)$$

where $y_i$ (for even $i$) indicates that the output voltage changes from 0 to $V_{dc}$.

Now equating the carrier triangle wave and the modulating sine wave values at the intersection points between them yields:

$$M \sin \alpha_i = \frac{R(\alpha_i - (i-1)\frac{\pi}{R})}{\pi}, \quad i = 1, 3, 5, ..., R-1$$  \hspace{1cm} (3.3)$$

$$M \sin \alpha_i = 1 - \frac{R(\alpha_i - (i-1)\frac{\pi}{R})}{\pi}, \quad i = 2, 4, 6, ..., R$$  \hspace{1cm} (3.4)$$

Note that equations 3.1 to 3.4 correspond to the positive half cycle of inverter operation. Similarly for the negative half cycle we have:

$$M \sin(\alpha_i + \pi) = -\frac{R(\alpha_i - (i-1)\frac{\pi}{R})}{\pi}, \quad i = 1, 3, 5, ..., R-1$$  \hspace{1cm} (3.5)$$

$$M \sin(\alpha_i + \pi) = \frac{R(\alpha_i - (i-1)\frac{\pi}{R})}{\pi} - 1, \quad i = 2, 4, 6, ..., R$$  \hspace{1cm} (3.6)$$

For the positive fundamental half-cycle, equations 3.3 and 3.4 can be solved by Newton-Raphson iteration to compute the switching angles of the waveform for specific frequency ratio, $f_c/f_s$, and modulation index (M). Similarly, equations 3.5 and 3.6 can be solved for the negative fundamental half-cycle.
The Newton-Raphson iteration method would be impractical for an embedded system controller used to operate an inverter, given a large number of carrier wave ratios and/or different modulation indices. So, it is better to calculate the switching instances off-line, for example using the Newton-Raphson method and the appropriate program (e.g. MATLAB / Simulink, from The MathWorks, Inc. as shown in Appendix A). This data (switching angles) is converted to hexadecimal code and stored as a lookup table in random access memory (RAM) of the inverter microcontroller.

![Diagram of inverter switching instances](image)

**Fig. 3.1** Determination of inverter switching instances for 3-level inverter operation, with $M=0.9$, $f_c/f_s=6$, NSPWM. The lower waveform is the inverter output voltage.
3.3 Mathematical Analysis for Single-Phase Double Edge NSPWM Inverters

In this section we focus on double Fourier integral analysis of both 2-level and 3-level NSPWM.

*Harmonic Analysis for 2-level Inverter Operation, One Phase-Leg Only*

The basic circuit diagram of voltage source inverters, which can be utilized for 2-level PWM, is a one phase leg (half-bridge). This circuit consists of two semiconductor switches and their associated anti-parallel diodes as shown in Fig. 3.2 (a). The only way to provide a continuous path for the output load current is through conducting of always one of the two switches of the inverter (the switches are operating alternatively). From this circuit, the 2-level single-phase inverter as shown in Fig. 3.2 (b), as well as 3-level or multi-level inverters and three-phase inverters can be developed.

Fig. 3.2 (a) Half-bridge VSI (one phase-leg) and (b) full-bridge VSI (two phase-legs)
As discussed in section 3.2 above, a common method to obtain the gating (ie, pulsing) pattern for a 2-level pulse width modulated inverter system is to compare a low-frequency sinusoidal reference waveform with a high frequency carrier waveform, and the resultant output is used to gating the switches of the half-bridge (phase-leg) of the inverter. When the reference waveform is greater than the carrier waveform, the half-bridge output is switched to the upper (positive) DC bus. In contrast, if the reference waveform is less than the carrier waveform, the output is switched to the lower (negative) DC bus. So, the result is a train of pulses switched between the positive and negative voltage supply (c.f. Fig. 3.3 below) which contains the fundamental (sine reference) component and a series of undesirable harmonics generated as a result of the switching process. The analysis of these PWM switched phase-leg outputs is non-trivial and is often done using a Fourier analysis or the Fast Fourier Transform (FFT).

A large variety of PWM techniques has been developed [20-26]. These variations can be classified according to the following criteria: (a) the sampling strategy that can be used such as natural, symmetric regular sampled or asymmetrical regular sampled. (b) the type of the carrier waveform that can be used such as triangle, sawtooth, trapezoidal (c) type or value of the offset waveform that can be added to the reference waveform which can contribute to develop different types of modulation. Space vector modulation and discontinuous switching of NSPWM is some examples of this application. Each of these variations has its own particular harmonic profile benefits.

The analytical method of determining the harmonic components of a PWM switched half-bridge was first developed by Bowes and Bird [34], who applied an harmonic analysis technique to PWM converter that was developed previously for communication systems by Bennet [35] and Black [36].
In this PWM switched half-bridge technique, we have two time dependences, one is for the (usually sinusoidal) reference waveform \( x(t) = \omega_s t + \theta_s \), and the other is for the carrier waveform \( y(t) = \omega_c t + \theta_c \), where:

- \( \omega_s = 2\pi/T_s \) = sinusoidal fundamental angular frequency
- \( T_s \) = period of the sinusoidal fundamental waveform
- \( \theta_s \) = arbitrary phase angle for the sinusoidal fundamental waveform
- \( \omega_c = 2\pi/T_c \) = carrier (usually a triangular waveform) angular frequency
- \( T_c \) = period of the carrier waveform
- \( \theta_c \) = arbitrary phase angle for carrier waveform

From Fourier theory [37], a non-sinusoidal time-varying periodic function \( f(t) \) can be expressed as a summation of all harmonics:

\[
f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos n\omega_0 t + b_n \sin n\omega_0 t]
\]

where \( \omega_0 \) is the fundamental angular frequency, and the \( a, b \) coefficients are given by:

\[
a_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(t) \cos n\omega_0 t \, dt \quad n = 1, 2, \ldots, \infty
\]

\[
b_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(t) \sin n\omega_0 t \, dt \quad n = 1, 2, \ldots, \infty
\]

From reference [38], it is shown that the Fourier series for a double time controlled waveform \( f(x, y) \) is as follows:

\[
f(x, y) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n} \cos ny + B_{0n} \sin ny] + \sum_{m=1}^{\infty} [A_{m0} \cos mx + B_{m0} \sin mx] +
\]

\[
\sum_{m=1}^{\infty} \sum_{n=0}^{\infty} [A_{mn} \cos (mx + ny) + B_{mn} \sin (mx + ny)]
\]
where \( m \) = carrier index and \( n \) = base band index, and the coefficients are:

\[
A_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) \cos(mx + ny) \, dx \, dy
\]

(3.11)

\[
B_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) \sin(mx + ny) \, dx \, dy
\]

(3.12)

These coefficients can be re-written in complex form (where \( j = \sqrt{-1} \)):

\[
C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) e^{j(mx+ny)} \, dx \, dy
\]

(3.13)

Replacing \( x \) by \( \omega_c t + \theta_c \) and \( y \) by \( \omega_s t + \theta_s \), equation 3.10 can be expressed in time-varying form as:

\[
f(t) = f[x(t), y(t)] = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n} \cos(n[\omega_s t + \theta_s]) + B_{0n} \sin(n[\omega_s t + \theta_s])]
\]

\[
+ \sum_{m=1}^{\infty} [A_{m0} \cos(m[\omega_c t + \theta_c]) + B_{m0} \sin(m[\omega_c t + \theta_c])]
\]

\[
+ \sum_{m=1}^{\infty} \sum_{n=-\infty, n \neq 0}^{\infty} [A_{mn} \cos(m[\omega_c t + \theta_c] + n[\omega_s t + \theta_s]) + B_{mn} \sin(m[\omega_c t + \theta_c] + n[\omega_s t + \theta_s])]
\]

(3.14)

The first line of the equation 3.14 defines the DC component, the fundamental component is defined when \( n = 1 \) and baseband harmonic components which are integer multiples of the fundamental component. The second line of the equation defines carrier harmonic components as multiples of the modulating sine wave frequency. The third line defines sideband harmonic components displaced on either side of the main carrier harmonics by integer multiples of the fundamental frequency component.
The first term of equation 3.14 is $A_{00}/2$ represents the DC offset component of the output waveform (usually there is no DC offset). The second term is a summation term (contains no m terms) that defines the output fundamental low-frequency waveform and baseband harmonics around it. This baseband harmonics is undesirable low-order harmonics and should be minimized, eliminated or shifted to higher frequencies with an appropriate PWM technique. The third term is the summation term (contains no n-terms), that represents the carrier wave harmonics, which are relatively high frequency components if compared with the modulating carrier frequency. The forth term is a double summation term which contains both m and n terms, represents all groups of sideband harmonics around the carrier harmonic frequencies and formed as a result of the sum and differences between the modulating carrier waveform harmonics and the reference waveform combined with all baseband harmonics around it.

For the NSPWM technique of a triangular carrier and a simple sinusoidal fundamental reference, the procedure and solution described in equation 3.14 can be developed to equation 3.15 below [39]:

\[
V_{pm}(t) = V_{dc} \{ M \cos(\omega_c t + \theta_s) + \frac{4}{\pi} \sum_{m=\infty}^{m=\infty} \sum_{n=-\infty}^{n=\infty} \frac{1}{m} \sin[\pi(m+n)] \int \frac{\pi}{2} J_n(m \pi/2) \cos(m[\omega_c t + \theta_s] + n[\omega_c t + \theta_s]) \} \]

(3.15)

where $V_{pm}$ represents the output voltage of one phase-leg. This equation represents a more general harmonic form of the switched output waveform of a one phase-leg controlled by any carrier based PWM scheme.

It is obvious from equation 3.15 that by the presence of $\sin([m+n]\pi/2)$ terms in the equation, all odd sideband harmonic for each odd carrier multiple, and all even sideband harmonic for each even carrier multiple can be eliminated with NSPWM technique.

Equation 3.15 also refers to the sub-harmonics, which is described as carrier sideband harmonics. These sub-harmonics are of frequencies below the fundamental component and will be generated when the carrier/fundamental frequency ratio is low.
From equation 3.15 and evaluation of the \( J_n \) (Bessel function) values we identify the significant (>0.5%) lower frequency sideband harmonics for this sampling technique as:

\[
f_h = f_c \pm 2f_s, f_c \pm 4f_s, f_c \pm 6f_s, 2f_c \pm f_s, 2f_c \pm 3f_s, 2f_c \pm 5f_s
\]

These frequencies will be below the fundamental when \( f_c < 7f_s \). Therefore it is recommended that the inverter operate with \( f_c \geq 9f_s \) [39].

**Single-phase 2-level Double-edge NSPWM**

The 2-level modulation strategy makes the switching of one phase-leg exactly opposite to the other as shown in Fig.3.3, and that means the phase shift between the fundamental and the carrier waveforms is exactly 180°. This implies that the phase-leg and line-to-line voltages will be as shown in equations 3.16 and 3.17 [39]. So, it is clear that the odd carrier sideband harmonic is still present and this is valid for all modulation sampling techniques.

\[
V'_{p_h}(t) = V_{dc} \{ M \cos(\omega_c t + k\pi) \\
+ \frac{4}{\pi} \sum_{m=1}^{\infty} \sum_{n=\infty}^{m} \frac{1}{m} \{ \sin((m+n)\frac{\pi}{2})J_n(m \frac{\pi}{2} M) \cos(m[\omega_c t + k\pi] + n[\omega_c t + k\pi]) \} \} , k = 0,1
\]  \hspace{1cm} (3.16)

\[
V'_{l-l}(t) = V'_{p_h}(t) - V'_{p_h}(t) = V_{dc} \{ 2M \cos(\omega_c t) \\\n+ \frac{8}{\pi} \sum_{m=1}^{\infty} \sum_{n=\infty}^{m} \frac{1}{m} \{ \sin((m+n)( \frac{\pi}{2})J_n(m \frac{\pi}{2} M) \cos(m\omega_c t + n\omega_c t) \} \} 
\]  \hspace{1cm} (3.17)

However, upon comparison between 2-level double-edge modulation and 3-level double-edge modulation, we will find the latter has superior harmonic performance (c.f. Chapter 4) which is reviewed next.
Fig. 3.3  Single-phase inverter output voltage waveform determination for 2-level NSPWM operation with fc/fs = 9 and M=0.9

3-level double-edge NSPWM single-phase inverter

The 3-level modulation strategy is shown in Fig. 3.4. In a single-phase inverter with two phase-legs, a 3-level NSPWM can be achieved by modulating the two-legs with reference waveforms of phase shift 180°. Equation 3.15 can be analyzed and developed to express the unfiltered phase-leg waveforms and line-to-line output voltage waveform as shown in equation 3.18 and 3.19 [39].

\[
V_{\text{pm}}(t) = V_{\text{dc}} \{ M \cos(\omega t + k\pi) \\
+ \frac{4}{\pi} \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} \{ \sin([m+n] \frac{\pi}{2}) J_0(m \frac{\pi}{2} M) \cos(m[\omega t] + n[\omega t + k\pi]) \} \}, k = 0, 1
\] (3.18)

\[
V_{l-1}(t) = V_{\text{pm}}(t) - V_{\text{pml}}(t) = V_{\text{dc}} \{ 2M \cos(\omega t) \\
+ \frac{8}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} \{ \cos([m+n+1] \pi) J_{2n-1}(2m \frac{\pi}{2} M) \cos(2m[\omega t] + (2n-1)[\omega t]) \} \}
\] (3.19)
Fig. 3.4 Single-phase inverter output voltage waveform determination for 3-level NSPWM operation with $M=0.9$ and $fc/fs=6$

In equation 3.19, by virtue of the $\cos(2m[\omega_c t] + (2n-1)[\omega_s t])$ term, it is shown that complete cancellation occurs for all even sideband harmonics in the line-to-line output voltage for 3-level naturally sampled PWM single-phase inverters and all other single-phase PWM techniques for different carrier/fundamental frequency ratio. For the NSPWM technique in particular, this equation shows that the sideband harmonics associated with odd carrier frequency multiples are completely cancelled from the line-to-line output voltage. This mathematical analysis is confirming that the well known harmonic profile superior of 3-level modulation methods compared to 2-level modulation methods (which we have verified as shown in Chapter 4).
3.4 Implementation of Harmonic Cancellation for Parallel Full-Bridge Inverters

Fig. 3.5 shows the proposed implementation of three full-bridge inverters operated in parallel. It is worthwhile to note that inverter 2 in this schematic lags inverter 1 by Tc/3, and inverter 3 lags inverter 1 by 2Tc/3 where Tc is the period of one triangular carrier cycle. The key idea of the proposed operation is that once per cycle of the fundamental waveform, a triggering signal is sent to each inverter gating-controller to maintain this phase-shifted operation. Note that in Fig. 3.5, three load resistors are shown, but in practice one load (effectively resistive) is sufficient.
To understand the harmonic reduction effect of parallel synchronized inverter operation, consider the switching strategy for two phase-shifted full-bridge inverters as illustrated in Fig. 3.6. Fig 3.6 (a) shows the output pulses of each NSPWM 3-level operated inverter, with \( M = 0.9, \frac{f_c}{f_s} = 6 \) (as used in Fig.3.4). The second inverter is operated with the same set of pulses as the first inverter but delayed by time \( T_c/2 \) as shown in Fig.3.6 (b). Using current sharing filter inductors, the resultant effective unfiltered \( V_{re} \) (the imaginary unfiltered output voltage at the common point of all parallel inverters) can be expressed for the general case of \( N \) parallel inverters as:

\[
V_{re} = \left[ V_{ab(1)} + V_{ab(2)} + V_{ab(3)} + \ldots + V_{ab(N)} \right] / N
\]

(3.20)

For the case of two parallel inverters, the resultant effective load voltage waveform is shown in Fig.3.9 (c). Note that there are five voltage levels in the effective unfiltered load voltage waveform for each cycle of the fundamental (0V, 1/2 \( V_{dc} \), \( V_{dc} \), -1/2 \( V_{dc} \), -\( V_{dc} \), this is similar to “3-level” multilevel inverter operation having 3 voltage levels in each half-cycle of the fundamental as discussed in Chapter 2). In the case of three inverters synchronized for parallel operation (see Fig. 3.5), the effective unfiltered output voltage waveform will have seven voltage levels per cycle of the fundamental waveform (0V, 1/3 \( V_{dc} \), 2/3 \( V_{dc} \), \( V_{dc} \), -1/3 \( V_{dc} \), -2/3 \( V_{dc} \), -\( V_{dc} \)). As more inverters are employed, the effective unfiltered load voltage waveform becomes more sinusoidal-like with an effectively higher carrier frequency (ie, \( N \times f_c \)).

It is very important to realize that the filter inductors filter out the effective carrier frequency components with their side bands to produce the actual load voltage waveform that is even more sinusoidal-like than the effective unfiltered load voltage. The actual load voltage waveform will be presented in chapters 4 (theory) and 5 (experimental) for a wide variety of operating conditions so that we may characterize how the PWM operating parameters effect the harmonic content of the actual load voltage waveform.
As illustrated in Fig. 3.6, the choice of inverter-to-inverter phase delay of $T_c/N$ produces a pleasingly symmetrical appearing effective load voltage waveform, however we would like to provide some evidence that this produces a near-minimum total harmonic distortion (THD) in the effective (and actual) load voltage waveform.
In Chapter 4 we present a review of a THD calculation procedure, given a Fourier series of a given waveform. Applying this THD calculation technique for the proposed method of synchronous operation of two parallel inverters having \( \frac{f_c}{f_s} = 20 \), \( M=0.9 \), 3-level inversion, \( L=0.6\text{H} \), \( R(\text{load}) = 510\Omega \), with a range of phase delays, \( T_d \), from 0 to \( T_c \) (where \( T_c \) is the period of the carrier waveform) we obtain the THD curve shown in Fig. 3.7. As expected the minimum THD occurs near \( T_d = \frac{T_c}{2} \). Incidentally, the actual minimum occurs at \( 0.506T_c \). The deviation from \( T_c/2 \) is likely the result of the fact that we are using exactly the same gating train for each inverter rather than performing PWM with reference to a single (non-time-shifted) modulating sine wave. This explanation is consistent with the asymmetry of the curve plotted in Fig. 3.7.

![THD versus phase shift delay, Td/Tc, for two parallel synchronized inverters having fc/fs =20, M=0.9, 3-level NSPWM operation](image)
3.6 Chapter Summary

This chapter provides the theoretical background of Naturally Sampled PWM and Fourier analysis applied to NSPWM inverter operation, to assist the understanding of our version of harmonic reduction in the synchronized operation of multiple inverters. This background is useful for the simulation studies presented in Chapter 4. In section 3.4 we present our version of multiple inverter harmonic reduction. The key contribution of this thesis is not our inverter synchronization technique but rather the characterization of the technique presented in Chapter 4.

We also illustrate in this chapter how the effective carrier frequency (c.f. Fig. 3.6) is increased and the effective number of inversion levels is also increased when inverters are operated in parallel with synchronized transistor gating. This insight allows us to understand why synchronized parallel inverter operation using NSPWM may be a very attractive method of total harmonic distortion (THD) reduction. This is a key insight of this chapter.

The graph of THD versus different values of phase-shift between parallel inverters, as presented in section 3.5, shows that the minimum THD is in fact near $T_c/2$ (ie, one-half the carrier period) for two parallel inverters. This result can be generalized to the case of $N$ synchronized parallel inverters with the minimum THD occurring for an inverter-to-inverter phase-delay of approximately $T_c/N$, where $T_c$ is the carrier period. This is another worthwhile contribution of this chapter.
Chapter 4

Simulation Results

4.1 Introduction

Inverter designers are aware that inverters can be operated in parallel to reduce the total harmonic distortion of the load, but how to optimize such distortion reduction is not well known. Using the set-up presented in Chapter 3, we have simulated single and parallel inverter operation under a variety of conditions. The characterization of synchronized parallel-inverter operation, presented in this chapter, may be useful to inverter designers as new inverter applications are developed.

In this chapter, simulation results are presented including load voltage waveforms, and the calculated THD of the load voltage, in all cases for NSPWM gating. The inverter systems that were considered corresponded to 4 volt and 16 volt dc input supplies (as these were the voltage values employed in our experimental work, presented in the next chapter). In theory, the dc input voltage does not affect the load voltage THD, hence in this chapter, only the cases corresponding to a dc input of 4V are presented. However, the modulation index, M, carrier-to-sine-wave frequency ratio, fc/fs, and the number of inversion levels, does have a great effect on load voltage THD, hence it is these PWM operating parameters that are varied to perform our characterization. In all cases considered in this chapter, each inverter is operated with a filter inductance of 0.6H and a load resistance of 510Ω, as was the case in our experimental investigation (these values were chosen given the power limitation of the transistors in the H-bridge and to provide a reasonable range of THD values). The THD calculations were performed using the Fourier series coefficients for the output load voltage waveform, where the coefficients and THD calculations were obtained with our own MATLAB code. The NSPWM pulse widths required for these simulations were calculated using our own Simulink code (based on equations 3.1 to 3.6 of Chapter 3, c.f. Appendix A).
4.2 Output Voltage Waveform of Inductive Load in NSPWM Inverter Circuit

Referring to Fig. 3.5 of Chapter 3, we reproduce one inverter schematic in Fig. 4.1. It is a straightforward matter to set-up and solve the differential equation corresponding to this circuit for the period of time that $Vac$ is constant (ie, $Vac = 0$, $+V_{dc}$, $-V_{dc}$, depending on which set of switches is ON as discussed in section 2.5.2).

\[ L = 0.6 \text{ H} \]

\[ V_{dc} \]

\[ T1 \quad D1 \]

\[ T2 \quad D2 \]

\[ T3 \quad D3 \quad T4 \quad D4 \]

\[ i \]

\[ Vac \]

\[ VR \]

\[ 510 \text{ Ohm} \]

Fig. 4.1 Full-bridge inverter employed for simulation and experimental investigations

Assuming ideal switching devices (instantaneous and lossless switching), applying Kirchhoff's Voltage Law to the load resistance loop of Fig 4.1:

\[ Vac = L \frac{di}{dt} + Ri \]  \hspace{1cm} (4.1)

So, $R \times i = VR = Vac - L \frac{di}{dt}$  \hspace{1cm} (4.2)

Solving this differential equation:

\[ i(t) = i_f + (i_i - i_f) e^{-(R/L)t} \]  \hspace{1cm} (4.3)

where $i_i$ = initial current value and $i_f$ = final current value for $Vac$ = constant.

So, the output voltage $VR = R \times i$ will be given by:

\[ VR(t) = Vac + (Vri - Vac) e^{-(R/L)t} \]  \hspace{1cm} for $Vac$ = constant, \hspace{1cm} (4.4)

where $Vri$ is the initial value of $VR(t)$ at time $t=0$.

These equations are the basis of our MATLAB code that we employed to simulate the inverter system of Fig. 3.5. The details of this are presented in Appendix A.
4.3 Fourier Series Analysis of Periodic Waveforms

Generally, in power electronic circuits the current drawn from the grid network by the load is highly distorted and therefore the output waveform is a non-sinusoidal due to the nonlinear voltage-current characteristic inherently possessed by this load. In steady state, such waveforms repeat with a cycle period \( T \) and a frequency \( f = \omega / 2\pi = 1/T \). This frequency is called the fundamental frequency, which is (60Hz in North America) and it is usually designated by a subscript 1 in Fourier series analysis. In addition to the fundamental frequency, the waveforms contain frequencies that are integer multiples of the fundamental frequency (called harmonics). These components can be calculated by means of Fourier series analysis.

In general, a non-sinusoidal waveform, \( f(t) \), that is periodic with an angular frequency, \( \omega \), can be expressed using Fourier analysis as:

\[
f(t) = A_0 + \sum_{n=1}^{\infty} f_n(t) = \frac{1}{2} a_0 + \sum_{n=1}^{\infty} \{a_n \cos(n\omega t) + b_n \sin(n\omega t)\}
\]  

(4.5)

Where \( A_0 = \frac{1}{2} a_0 \) is the average (DC) component of the waveform, and:

\[
a_n = \frac{1}{\pi} \int_{0}^{2\pi} f(t) \cos(n\omega t) d(\omega t) \quad n=1, 2, \ldots, \infty
\]  

(4.6)

\[
b_n = \frac{1}{\pi} \int_{0}^{2\pi} f(t) \sin(n\omega t) d(\omega t) \quad n=1, 2, 3, \ldots, \infty
\]  

(4.7)

From equations 4.5 and 4.6 the DC value is:

\[
A_0 = \frac{1}{2} a_0 = \frac{1}{2\pi} \int_{0}^{2\pi} f(t) d(\omega t) = \frac{1}{T} \int_{0}^{T} f(t) d(t)
\]  

(4.8)
If \( f(t) \) represents a voltage waveform, then the rms value of the \( n \)th harmonic component is given by:

\[
R_n = \left[ (a_n^2 + b_n^2) \right]^{1/2} / \sqrt{2}
\]  \hspace{1cm} (4.9)

and the phase angle is expressed as:

\[
\phi_n = \arctan \frac{b_n}{a_n}
\]  \hspace{1cm} (4.10)

The rms value of the \( f(t) \) voltage waveform is given by:

\[
V_{\text{rms}} = \left( V_{1(\text{rms})}^2 + V_{2(\text{rms})}^2 + V_{3(\text{rms})}^2 + \ldots \right)^{1/2}
\]  \hspace{1cm} (4.11)

where \( V_{n(\text{rms})} = R_n / \sqrt{2} \) represents the rms value of the \( n \)th Fourier component, whereas, the total rms value of all the harmonic components is given by:

\[
V_{n\text{-\text{rms}}} = \left( V_{2(\text{rms})}^2 + V_{3(\text{rms})}^2 + V_{4(\text{rms})}^2 + \ldots \right)^{1/2}
\]  \hspace{1cm} (4.12)

In equations 4.11 and 4.12, it is common practice to employ a finite number of terms (we have generally used 200 terms).

Thus, the THD of the original function, \( f(t) \), may be expressed by definition as:

\[
\text{THD} = \frac{\left( V_{2(\text{rms})}^2 + V_{3(\text{rms})}^2 + V_{4(\text{rms})}^2 + \ldots + V_{N_T(\text{rms})}^2 \right)^{1/2}}{V_{1(\text{rms})}}
\]  \hspace{1cm} (4.13)

where \( N_T \) is a finite number above which the harmonic components are negligible (once again, we have generally used \( N_T = 200 \) in our simulation work).

As a point of interest, from equations 4.11 and 4.13, the exact THD of \( f(t) \) can also be expressed as:

\[
\text{THD} = \frac{\left( V_{\text{rms}}^2 - V_{1(\text{rms})}^2 \right)^{1/2}}{V_{1(\text{rms})}}
\]  \hspace{1cm} (4.14)

The above equations were employed in our MATLAB code to find the THD of the load voltage waveforms presented below (see Appendix A for details).
4.4 Sample Simulation Results

Simulations were carried out using MATLAB for one inverter, two parallel phase-shifted inverters, and three parallel phase-shifted inverters respectively (each inverter as shown in Fig. 4.1 and parallel system as shown in Fig. 3.5). Naturally sampled PWM was used. The simulation time step is 1 μs. Parameters are listed in Table 4.1. Note that even in the case of two or three parallel inverters, each inverter having a 0.6H filter inductor and local load of 510Ω, the effective L/R time constant remains constant at 1.176ms (other details are given in Appendix A).

Table 4.1 Simulation Parameters

<table>
<thead>
<tr>
<th>Parameters used</th>
<th>1 Inverter</th>
<th>2 Inverters</th>
<th>3 Inverters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdc</td>
<td>4 V</td>
<td>4 V</td>
<td>4 V</td>
</tr>
<tr>
<td>L (effective)</td>
<td>0.6 H</td>
<td>0.3 H</td>
<td>0.2 H</td>
</tr>
<tr>
<td>R (effective)</td>
<td>510 Ω</td>
<td>255 Ω</td>
<td>170 Ω</td>
</tr>
<tr>
<td>Modulation Index M</td>
<td>0.3, 0.6, 0.9, 1, 1.15</td>
<td>0.6, 0.9</td>
<td>0.6, 0.9</td>
</tr>
<tr>
<td>Frequency Ratio fc/fs</td>
<td>4, 6, 10, 14, 20, 21, 30, 31, 40</td>
<td>20, 21, 30, 31</td>
<td>20, 21, 30, 31</td>
</tr>
<tr>
<td>No. of Levels</td>
<td>2-level and 3-level</td>
<td>2-level and 3-level</td>
<td>2-level and 3-level</td>
</tr>
<tr>
<td>Phase-shift between Inverters</td>
<td>no phase-shift is required</td>
<td>Tc/2</td>
<td>Tc/3</td>
</tr>
</tbody>
</table>

Sample simulation results are presented in Figs. 4.2 to 4.11 (ie, not all the cases in Table 4.1 are presented in this section; more results are presented in tabular form below in section 4.5). In each of the Fourier coefficient plots, the C1 (ie, the fundamental) coefficient is not shown since C1 is quite large compared to the harmonics. The ratio of the harmonic frequency to the modulating sine wave frequency is fh/fs. Simulation results for one inverter operation (ie, these serve as reference cases for parallel inverter operation) are shown in Figs. 4.2 to 4.6. For two parallel inverters operating with a phase-shift of Tc/2 (where Tc is the carrier period), results are shown in Figs. 4.7 and 4.8, and results for three inverters operating in parallel with a phase-shift of Tc/3 are shown in Figs. 4.9 and 4.10. A discussion of these results is presented in section 4.6 below.
Fig. 4.2 One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=0.6$, $fc/fs=20$, $C_1=2.1919V$, THD = 11.21 %

Bottom: 3-level NSPWM, $M=0.9$, $fc/fs=20$, $C_1=3.290V$, THD = 6.34 %
Fig. 4.3 One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=1.0$, $fc/fs = 20$, $C_1 = 3.65 V$, THD = 6.00 %

Bottom: 3-level NSPWM, $M=1.15$, $fc/fs = 20$, $C_1 = 4.0 V$, THD = 5.34 %
Fig. 4.4 One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 2-level NSPWM, \( M = 0.6, \frac{f_c}{f_s} = 21, C_1 = 2.179V, \) THD = 21.85 %

Bottom: 2-level NSPWM, \( M = 0.9, \frac{f_c}{f_s} = 21, C_1 = 3.2818V, \) THD = 11.61 %
Fig. 4.5 One inverter only operation: voltage waveform and Fourier component magnitude

Top: 3-level NSPWM, $M=0.6$, $f_c/fs = 30$, $C_1 = 2.194V$, THD = 7.48 %
Bottom: 3-level NSPWM, $M=0.9$, $f_c/fs = 30$, $C_1 = 3.29V$, THD = 4.24 %
Fig.4.6 One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 2-level NSPWM, $M=0.6$, $fc/fs = 31$, $C_1=2.193V$, THD = 14.45%

Bottom: 2-level NSPWM, $M=0.9$, $fc/fs = 31$, $C_1=3.2824V$, THD = 7.73%
Fig. 4.7 Two inverters in parallel: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=0.6$, $f_c/f_s = 30$, $C_1 = 2.191V$, THD = 1.47%

Bottom: 3-level NSPWM, $M=0.9$, $f_c/f_s = 30$, $C_1 = 3.28V$, THD = 1.20%
Fig. 4.8 Two inverters in parallel: voltage waveform and Fourier component magnitude

Top: 2-level NSPWM, $M=0.6$, $f_c/fs=31$, $C_1=2.19V$, THD = 3.79 %

Bottom: 2-level NSPWM, $M=0.9$, $f_c/fs=31$, $C_1=3.2777V$, THD = 2.15 %
Fig. 4.9 Three inverters in parallel: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=0.6$, $f_c/f_s=30$, $C_1=2.185V$, THD = 0.86%

Bottom: 3-level NSPWM, $M=0.9$, $f_c/f_s=30$, $C_1=3.2716V$, THD = 0.60%
Fig. 4.10 Three inverters in parallel: voltage waveform and Fourier component magnitudes

Top: 2-level NSPWM, $M=0.6$, $f_c/f_s=31$, $C_1=2.1889V$, THD = 1.55%

Bottom: 2-level NSPWM, $M=0.9$, $f_c/f_s=31$, $C_1=3.2758V$, THD = 1.03%
It is of interest to also show the simulated output voltage and Fourier coefficient results in the case of a low carrier-to-sine-wave frequency ratio. This is done in Fig. 4.11. Note how the harmonics are now grouped very near the fundamental frequency, $f_s$. For this reason, it is advisable to keep the carrier-to-sine-wave frequency ratio above approximately 7.

Fig.4.11 One inverter only operation: voltage waveform and Fourier component magnitudes for 3-level NSPWM, $M=0.9$, $fc/fs =6$, $C_i= 3.753V$, THD = 21.27 %
4.5 Simulation Results Summary

The following tables summarize our theoretical THD results for one, two, and three parallel inverters, respectively (as obtained by MATLAB simulation, c.f. Appendix A).

Table 4.2 Load Voltage THD (simulation result) for One Inverter Only

<table>
<thead>
<tr>
<th>Carrier Frequency Ratio (fc/fs)</th>
<th>Modulation Index (M)</th>
<th>No. of inverter levels in one Cycle</th>
<th>THD (theoretical)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.9</td>
<td>3-level</td>
<td>39.92 %</td>
</tr>
<tr>
<td>6</td>
<td>0.9</td>
<td>3-level</td>
<td>21.27 %</td>
</tr>
<tr>
<td>10</td>
<td>0.9</td>
<td>3-level</td>
<td>12.68 %</td>
</tr>
<tr>
<td>14</td>
<td>0.9</td>
<td>3-level</td>
<td>9.23 %</td>
</tr>
<tr>
<td>18</td>
<td>0.9</td>
<td>3-level</td>
<td>7.28 %</td>
</tr>
<tr>
<td>20</td>
<td>0.3</td>
<td>3-level</td>
<td>16.64 %</td>
</tr>
<tr>
<td>20</td>
<td>0.6</td>
<td>3-level</td>
<td>11.21 %</td>
</tr>
<tr>
<td>20</td>
<td>0.9</td>
<td>3-level</td>
<td>6.34%</td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>3-level</td>
<td>6.00 %</td>
</tr>
<tr>
<td>20</td>
<td>1.15</td>
<td>3-level</td>
<td>5.34 %</td>
</tr>
<tr>
<td>21</td>
<td>0.6</td>
<td>2-level</td>
<td>21.85 %</td>
</tr>
<tr>
<td>21</td>
<td>0.9</td>
<td>2-level</td>
<td>11.61 %</td>
</tr>
<tr>
<td>30</td>
<td>0.6</td>
<td>3-level</td>
<td>7.48 %</td>
</tr>
<tr>
<td>30</td>
<td>0.9</td>
<td>3-level</td>
<td>4.24 %</td>
</tr>
<tr>
<td>31</td>
<td>0.6</td>
<td>2-level</td>
<td>14.45 %</td>
</tr>
<tr>
<td>31</td>
<td>0.9</td>
<td>2-level</td>
<td>7.73 %</td>
</tr>
<tr>
<td>40</td>
<td>0.9</td>
<td>3-level</td>
<td>3.28 %</td>
</tr>
</tbody>
</table>
Table 4.3 Load Voltage THD (simulation result) for Two Parallel Inverters

<table>
<thead>
<tr>
<th>fc/fs</th>
<th>M</th>
<th>No. of Levels</th>
<th>THD (theoretical)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.6</td>
<td>3-level</td>
<td>2.31%</td>
</tr>
<tr>
<td>20</td>
<td>0.9</td>
<td>3-level</td>
<td>1.90%</td>
</tr>
<tr>
<td>21</td>
<td>0.6</td>
<td>2-level</td>
<td>5.73%</td>
</tr>
<tr>
<td>21</td>
<td>0.9</td>
<td>2-level</td>
<td>3.47%</td>
</tr>
<tr>
<td>30</td>
<td>0.6</td>
<td>3-level</td>
<td>1.47%</td>
</tr>
<tr>
<td>30</td>
<td>0.9</td>
<td>3-level</td>
<td>1.20%</td>
</tr>
<tr>
<td>31</td>
<td>0.6</td>
<td>2-level</td>
<td>3.79%</td>
</tr>
<tr>
<td>31</td>
<td>0.9</td>
<td>2-level</td>
<td>2.15%</td>
</tr>
</tbody>
</table>

Table 4.4 Load Voltage THD (simulation result) for Three Parallel Inverters

<table>
<thead>
<tr>
<th>fc/fs</th>
<th>M</th>
<th>No. of levels</th>
<th>THD (theoretical)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.6</td>
<td>3-level</td>
<td>1.40%</td>
</tr>
<tr>
<td>20</td>
<td>0.9</td>
<td>3-level</td>
<td>1.06%</td>
</tr>
<tr>
<td>21</td>
<td>0.6</td>
<td>2-level</td>
<td>3.10%</td>
</tr>
<tr>
<td>21</td>
<td>0.9</td>
<td>2-level</td>
<td>1.68%</td>
</tr>
<tr>
<td>30</td>
<td>0.6</td>
<td>3-level</td>
<td>0.86%</td>
</tr>
<tr>
<td>30</td>
<td>0.9</td>
<td>3-level</td>
<td>0.60%</td>
</tr>
<tr>
<td>31</td>
<td>0.6</td>
<td>2-level</td>
<td>1.55%</td>
</tr>
<tr>
<td>31</td>
<td>0.9</td>
<td>2-level</td>
<td>1.03%</td>
</tr>
</tbody>
</table>
4.6 Discussion of Simulation Results

1. Shown in Fig. 4.2 (top) are the Fourier coefficients for double-edge naturally sampled PWM for the condition of a carrier-to-sine-wave frequency ratio of 20, 3-level inversion, and modulation index of 0.6. This plot shows the groups of the sideband harmonics arranged around the carrier, double carrier and triple carrier frequencies. As in all the single inverter cases of Figs. 4.2 to 4.6, the carrier frequency sidebands dominate the remaining harmonics.

2. We can identify from the Figs. 4.2 to 4.6, that for single inverter operation, in both 2-level and 3-level cases, there are only four essential harmonics which effectively contribute to the THD of the output voltage waveform, at frequencies of $\omega_c \pm \omega_s$ and $\omega_c \pm 3\omega_s$. So, the corresponding THD can be easily calculated from the following equation [38]:

$$\text{THD} = \frac{\sqrt{\frac{V(\omega_c-3\omega_s)}{(\omega_c-3\omega_s)}^2 + \frac{V(\omega_c-\omega_s)}{(\omega_c-\omega_s)}^2 + \frac{V(\omega_c+\omega_s)}{(\omega_c+\omega_s)}^2 + \frac{V(\omega_c+3\omega_s)}{(\omega_c+3\omega_s)}^2}}{V(\omega_c)}$$  \hspace{1cm} (4.15)

3. The reduction of THD with an increase in modulation index M (see for example Fig.4.2 (bottom), where for $M=0.9$ the THD is significantly lower than that of case where $M=0.6$) occurs primarily because the summed magnitude of the first carrier harmonics remains relatively constant, however, the fundamental coefficient $C_1$ increases as M increases. Thus, as seen from equation 4.13, THD will decrease as M increases (but remains below 1.15). Also the reduction of THD with an increasing carrier-to-sine-wave frequency ratio is essentially identified as the reduced influence of the carrier and sideband harmonics on the THD calculation as they move toward higher frequencies. It is shown in Figs. 4.2 to 4.6 and that as we increase $f_c/f_s$ from 20 to 30, the major harmonics (centered on $\omega_c$), which contribute to the THD, are shifted to higher frequencies which are more easily filtered out, ie, more attenuated, resulting in a lower THD.
4. For cases involving low carrier frequencies, as in Fig. 4.11, it is possible that PWM inverters operating with very low carrier frequency will generate sub-harmonics. Sub-harmonics could be produced if the carrier frequency is low resulting in lower sideband frequencies that are below the fundamental, that is, \( \omega_c - 4\omega_s < \omega_s \) or \( \omega_c < 5\omega_s \). Actually there is probably no practical NSPWM system that would operate with a very low carrier frequency, so it is recommended that the inverter designer set the minimum carrier-to-sine-wave frequency ratio to no less than 7. For this case, the lowest effective sideband occurs at \( 3\omega_s \).

5. Shown in Fig. 4.3 is an example of operation in the overmodulation region (ie, \( M > 1 \)). In the triangle intersection PWM technique, when the sinusoidal modulation wave magnitude becomes larger than the triangle carrier wave peak value, some switching cycles are skipped and this has the effect that the output voltage waveform does not linearly follow the modulation index (\( M \)). Consequently, the shape of the output voltage waveform is not fully under control and the output voltage of the inverter is nearly saturated. Therefore the output waveform becomes distorted and contains many low-frequency harmonics. It is clear that in the overmodulation region, the rms load voltage still increases as \( M \) increases. There are many strategies to increase the range of PWM control into the overmodulation region. Some of them extend the range of the SPWM modulation index, and others involve space vector PWM extensions [40-43].

6. For two parallel inverters, the resultant THD of the system decreases significantly as compared with single inverter operation. This is identified by Figs. 4.7 and 4.8 where the synchronization of two parallel inverters with the phase-shift of \( T_c/2 \) between them is used for different \( M \) and \( f_c/f_s \). It is seen in these figures that the major harmonics are shifted to the double carrier frequency (ie, harmonics centered on \( 2\omega_c \)) instead of being centered on the carrier frequency, \( \omega_c \), as in single inverter cases. The result of this shifting to higher frequencies is an increased attenuation by the LR filter. Referring to Tables 4.2 and 4.3 we see that for two parallel synchronized inverters, a reduction in the THD by a factor of about 0.3 compared to operation with only one inverter.
7. Even better harmonic reduction performance is achieved if three inverters are operated in parallel with a phase-shift of $T_c/3$ between them. Note that having three inverters operate in parallel, the major harmonics are arranged around the triple carrier frequency, $3\omega_c$, which can be very effectively attenuated by the LR filter. Moreover, as mentioned in Chapter 3 (c.f. Fig. 3.6), we are suggesting that three parallel inverters produce an effectively lower peak-to-peak voltage at the load resistance. Also, operation with 3-level inversion compared to 2-level inversion does produce a lower peak-to-peak voltage entering the LR filter and this will result in a significant reduction in THD. The minimum THD is obtained with $f_c/f_s = 30$, $M = 0.9$, 3-level PWM as shown in Fig.4.9. Referring to Tables 4.2 and 4.4 we see that for three parallel synchronized inverters, a reduction in the THD by a factor of about 0.15 compared to operation with only one inverter.

4.7 Chapter Summary

This chapter presents the simulation waveform and THD results for single-phase full-bridge NSPWM inverter operation in the case of one inverter only, two parallel inverters synchronized with a phase-shift of $T_c/2$, and three parallel inverters with phase-shift $T_c/3$. We use a 4 volt DC input supply and assume that the switching transistors are ideal. In this chapter, the concept of near-optimum harmonic cancellation using a phase-delay of $T_c/N$ (where $N =$ number of parallel inverters) between synchronized parallel inverters is applied. The parameters investigated in this chapter include modulation index $M$, the carrier frequency ratio, $f_c/f_s$, the number of PWM levels, and finally the number of parallel inverters used.

The simulation results confirm that the THD of the load voltage is decreased significantly if any one of the above mentioned parameters ($M$, $f_c/f_s$, and inversion levels) is increased in value. In particular, we see that three parallel synchronized inverters using a modulation index of 0.9, a carrier-to-sine-wave frequency ratio of 30, and 3-level inversion, gives the lowest THD of 0.60 % for a filter L/R time constant of 1.176ms.
Chapter 5

Experimental Results

5.1 Introduction

In the simulation study presented in the previous chapter, the inverter semiconductor switches are modeled as ideal (i.e., are lossless with instantaneous turn-on and turn-off), but in fact, they are not. In addition, the filter inductor in practice is lossy and the gating pulse-widths determined by the microcontroller have some imprecision (the pulse widths were represented by 8-bit integer numbers in our experimental set-up). Consequently, the THD levels obtained in the simulation study of Chapter 4 can never be obtained in practice. In this chapter, we present the experimentally obtained Fourier coefficients and the THD values corresponding to all the cases represented by Figs. 4.2 to 4.10. Once again, we calculate the THD using equation 4.13, with $N_T = 200$ (i.e., 199 harmonics are used in the THD calculation).

The experimental work presented in this chapter, in each case, is for a DC input voltage of 4V. In all cases considered in this chapter, each inverter is operated with a filter inductance of 0.6H and a load resistance of 510Ω (these values were chosen given the power limitation of the transistors in the H-bridge and to provide a reasonable range of THD values).

5.2 Experimental Set-up and Results

The synchronous operation of multiple parallel inverters was discussed in Chapter 3 (c.f. Fig. 3.5). Shown in Fig. 5.1 is our implementation that makes use of a function generator to provide a synchronizing pulse to each inverter. Hardware details and microcontroller coding are provided in Appendices B and C respectively.
Notice in Fig. 5.1 that a single load (indicated here as an equivalent resistance) is shown, as would be the case in practice. In order make a fair comparison between the cases of one inverter, two inverter, and three inverter operation (ie, each inverter is operated at the same power level for a given modulation index), the load resistance is composed of one, two, or three, parallel 510Ω resistors. Other experimental parameters are shown in Table 5.1. Experimental results are shown in Figs. 5.2 to 5.10. A discussion of these results (and other results not shown) is presented in section 5.4.

Table 5.1 Experimental Parameters (same as Table 4.1)

<table>
<thead>
<tr>
<th>Parameters used</th>
<th>1 Inverter</th>
<th>2 Inverters</th>
<th>3 Inverters</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}$</td>
<td>4 V</td>
<td>4 V</td>
<td>4 V</td>
</tr>
<tr>
<td>L(effective)</td>
<td>0.6 H</td>
<td>0.3 H</td>
<td>0.2 H</td>
</tr>
<tr>
<td>R(effective)</td>
<td>510 Ω</td>
<td>255 Ω</td>
<td>170 Ω</td>
</tr>
<tr>
<td>Modulation Index M</td>
<td>0.3, 0.6, 0.9, 1, 1.15</td>
<td>0.6, 0.9</td>
<td>0.6, 0.9</td>
</tr>
<tr>
<td>Frequency Ratio fc/fs</td>
<td>10, 14, 20, 21, 30, 31</td>
<td>20, 21 30, 31</td>
<td>20, 21 30, 31</td>
</tr>
<tr>
<td>No. of Levels</td>
<td>2-level and 3-level</td>
<td>2-level and 3-level</td>
<td>2-level and 3-level</td>
</tr>
<tr>
<td>Phase-shift between Inverters</td>
<td>no phase-shift is required</td>
<td>Tc/2</td>
<td>Tc/3</td>
</tr>
</tbody>
</table>
Fig. 5.2 One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, \( M=0.6, \frac{f_c}{f_s}=20, C_1=0.97V, \) THD = 15.6 %

Bottom: 3-level NSPWM, \( M=0.9, \frac{f_c}{f_s}=20, C_1=1.54V, \) THD = 8.4 %
Fig. 5.3 One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=1.0$, $f_C/f_s=20$, $C_I=1.78\,\text{V}$, THD = 8.3 %

Bottom: 3-level NSPWM, $M=1.15$, $f_C/f_s=20$, $C_I=2.08\,\text{V}$, THD = 7.4 %
Fig. 5.4 One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 2-level NSPWM, $M=0.6$, $f_c/f_s=21$, $C_1=0.97V$, THD = 28.5 %

Bottom: 2-level NSPWM, $M=0.9$, $f_c/f_s=21$, $C_1=1.41V$, THD = 15.4 %
Fig. 5.5 One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=0.6$, $f_{c}/f_s=30$, $C_1=0.96V$, THD = 11.0 %

Bottom: 3-level NSPWM, $M=0.9$, $f_{c}/f_s=30$, $C_1=1.42V$, THD = 6.2 %
Fig. 5.6 One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 2-level NSPWM, $M=0.6$, $f_c/fs=31$, $C_1=0.96V$, THD = 21.1 %
Bottom: 2-level NSPWM, $M=0.9$, $f_c/fs=31$, $C_1=1.4V$, THD = 10.9 %
Fig. 5.7  Two inverters in parallel: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=0.6$, $fc/fs=30$, $C_1=1.04V$, THD = 6.4 %

Bottom: 3-level NSPWM, $M=0.9$, $fc/fs=30$, $C_1=1.54V$, THD = 3.4 %
Fig. 5.8 Two inverters in parallel: voltage waveform and Fourier component magnitudes

Top: 2-level NSPWM, $M=0.6$, $f_c/f_s=31$, $C_1=1\, \text{V}$, THD = 13.1 \%
Bottom: 2-level NSPWM, $M=0.9$, $f_c/f_s=31$, $C_1=1.4\, \text{V}$, THD = 8.2 \%
Fig. 5.9  Three inverters in parallel: voltage waveform and Fourier component magnitudes

Top:  3-level NSPWM, $M=0.6$, $fc/fs = 30$, $C_1 = 1.03V$, THD = 4.2 %
Bottom: 3-level NSPWM, $M=0.9$, $fc/fs = 30$, $C_1 = 1.56V$, THD = 3.1 %
Fig. 5.10 Three inverters in parallel: voltage waveform and Fourier component magnitudes

Top: 2-level NSPWM, $M=0.6$, $f_c/f_s=31$, $C_1=1.13V$, THD = 10.5%

Bottom: 2-level NSPWM, $M=0.9$, $f_c/f_s=31$, $C_1=1.5V$, THD = 6.8%
5.3 Experimental Results Summary

Tables 5.2 to 5.4 provide more experimental THD results (with a comparison to the simulation results as presented in Chapter 4) than are given above in the figures of section 5.2. Results are presented in Figs. 5.2 to 5.4 for one inverter, two parallel inverters, and three parallel inverters respectively. As for the results presented above, the experimental work was conducted by the author in the Power Electronics Laboratory of the University of Calgary. A discussion follows in the next section.

Table 5.2  Load Voltage THD, Simulation and Experimental, for One Inverter Only

<table>
<thead>
<tr>
<th>Carrier Frequency Ratio( (f_c/f_s) )</th>
<th>Modulation Index (M)</th>
<th>No. of inverter levels</th>
<th>THD (theoretical)</th>
<th>THD (experimental)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.9</td>
<td>3-level</td>
<td>12.68 %</td>
<td>28.8 %</td>
</tr>
<tr>
<td>14</td>
<td>0.9</td>
<td>3-level</td>
<td>9.23 %</td>
<td>13.0 %</td>
</tr>
<tr>
<td>20</td>
<td>0.3</td>
<td>3-level</td>
<td>16.64 %</td>
<td>32.0 %</td>
</tr>
<tr>
<td>20</td>
<td>0.6</td>
<td>3-level</td>
<td>11.21 %</td>
<td>15.6 %</td>
</tr>
<tr>
<td>20</td>
<td>0.9</td>
<td>3-level</td>
<td>6.34 %</td>
<td>8.4 %</td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>3-level</td>
<td>6.00 %</td>
<td>8.3 %</td>
</tr>
<tr>
<td>20</td>
<td>1.15</td>
<td>3-level</td>
<td>5.34 %</td>
<td>7.4 %</td>
</tr>
<tr>
<td>21</td>
<td>0.6</td>
<td>2-level</td>
<td>21.85 %</td>
<td>28.5 %</td>
</tr>
<tr>
<td>21</td>
<td>0.9</td>
<td>2-level</td>
<td>11.61 %</td>
<td>15.4 %</td>
</tr>
<tr>
<td>30</td>
<td>0.6</td>
<td>3-level</td>
<td>7.48 %</td>
<td>11.0 %</td>
</tr>
<tr>
<td>30</td>
<td>0.9</td>
<td>3-level</td>
<td>4.24 %</td>
<td>6.2 %</td>
</tr>
<tr>
<td>31</td>
<td>0.6</td>
<td>2-level</td>
<td>14.45 %</td>
<td>21.1 %</td>
</tr>
<tr>
<td>31</td>
<td>0.9</td>
<td>2-level</td>
<td>7.73 %</td>
<td>10.9 %</td>
</tr>
</tbody>
</table>
Table 5.3  Load Voltage THD, Simulation and Experimental, for Two Parallel Inverters

<table>
<thead>
<tr>
<th>fc/fs</th>
<th>M</th>
<th>No. of Levels</th>
<th>THD(theoretical)</th>
<th>THD(experimental)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.6</td>
<td>3-level</td>
<td>2.31%</td>
<td>7.6 %</td>
</tr>
<tr>
<td>20</td>
<td>0.9</td>
<td>3-level</td>
<td>1.90 %</td>
<td>4.4 %</td>
</tr>
<tr>
<td>21</td>
<td>0.6</td>
<td>2-level</td>
<td>5.73 %</td>
<td>17.5 %</td>
</tr>
<tr>
<td>21</td>
<td>0.9</td>
<td>2-level</td>
<td>3.47 %</td>
<td>10.9 %</td>
</tr>
<tr>
<td>30</td>
<td>0.6</td>
<td>3-level</td>
<td>1.47 %</td>
<td>6.4 %</td>
</tr>
<tr>
<td>30</td>
<td>0.9</td>
<td>3-level</td>
<td>1.20 %</td>
<td>3.4 %</td>
</tr>
<tr>
<td>31</td>
<td>0.6</td>
<td>2-level</td>
<td>3.79 %</td>
<td>13.1 %</td>
</tr>
<tr>
<td>31</td>
<td>0.9</td>
<td>2-level</td>
<td>2.15 %</td>
<td>8.2 %</td>
</tr>
</tbody>
</table>

Table 5.4  Load Voltage THD, Simulation and Experimental, for Three Parallel Inverters

<table>
<thead>
<tr>
<th>fc/fs</th>
<th>M</th>
<th>No. of Levels</th>
<th>THD(theoretical)</th>
<th>THD(experimental)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.6</td>
<td>3-level</td>
<td>1.40 %</td>
<td>4.2 %</td>
</tr>
<tr>
<td>20</td>
<td>0.9</td>
<td>3-level</td>
<td>1.06 %</td>
<td>4.0 %</td>
</tr>
<tr>
<td>21</td>
<td>0.6</td>
<td>2-level</td>
<td>3.10 %</td>
<td>11.6 %</td>
</tr>
<tr>
<td>21</td>
<td>0.9</td>
<td>2-level</td>
<td>1.68 %</td>
<td>9.4 %</td>
</tr>
<tr>
<td>30</td>
<td>0.6</td>
<td>3-level</td>
<td>0.86 %</td>
<td>4.2 %</td>
</tr>
<tr>
<td>30</td>
<td>0.9</td>
<td>3-level</td>
<td>0.6 %</td>
<td>3.1 %</td>
</tr>
<tr>
<td>31</td>
<td>0.6</td>
<td>2-level</td>
<td>1.55 %</td>
<td>10.5 %</td>
</tr>
<tr>
<td>31</td>
<td>0.9</td>
<td>2-level</td>
<td>1.03 %</td>
<td>6.8 %</td>
</tr>
</tbody>
</table>
5.4 Discussion of Experimental Results

Figs. 5.2 to 5.6 show the output voltage waveforms and harmonic coefficients for one inverter operating with NSPWM, as experimentally obtained using a 4V DC input. It can be readily seen that as M increases for any fixed carrier-to-sine-wave frequency ratio, $f_c/f_s$, the THD decreases, as expected since the fundamental of the output voltage increases in direct proportion to M. Figs. 5.2 and 5.4 respectively demonstrate that as the number of PWM inversion levels increases, for fixed M, and fixed $f_c/f_s$, the THD decreases with no significant changes in the output voltage amplitude in both cases. Figs. 5.2 (top) and Fig 5.5 (top) show that as $f_c/f_s$ changes from 20 to 30 the THD decreases without significant change in output voltage amplitude in both cases. The best harmonic profile is achieved by using higher M, higher $f_c/f_s$ frequency ratio, and a higher number of inversion levels. All these cases are summarized in Table 5.2. It is evident that from the plot of harmonic coefficients for Figs.5.2 to 5.6, that the sideband harmonics are arranged around the carrier frequency and to a lesser extent around the double carrier frequency and an even lesser extent around the triple carrier frequency.

Figs. 5.7 and 5.8 show the output voltage waveforms and harmonic coefficients for two synchronized parallel inverters operating with NSPWM, as experimentally obtained using a 4V DC input. The transistor gating delay between the inverters is $T_c/2$, but the gating pattern is otherwise identical for the two inverters. As seen in these figures and in the comparison between Tables 5.2 and 5.3, for a higher carrier-to-sine-wave frequency ratio ($f_c/f_s=30$), the reduction in THD is less than for the lower $f_c/f_s$ of 20. This may imply that for higher carrier-to-sine-wave frequency ratios it becomes more difficult to obtain the same decrease in THD as theoretically possible due to overriding nonlinearities of experimental inverter operation.
We also see in Figs. 5.7 and 5.8 that the dominant harmonics are indeed shifted to twice the carrier frequency as expected from our simulation study in Chapter 4. However, the shift is not as significant as we expected. We also observe that the sideband grouping of harmonics is not as distinct as in the theoretical case. At the same time, we observe an increase in non-sideband harmonics corresponding to the noise that can be observed in the output voltage waveform itself.

Figs. 5.9 and 5.10 show the output voltage waveforms and harmonic coefficients for three synchronized parallel inverters operating with NSPWM, as experimentally obtained using a 4V DC input. The effect of noise observed experimentally becomes more significant for three inverters operating in parallel. Note, for example, that the THD for $f_c/f_s = 20$, $M=0.9$, 3-level, decreases from 4.4% for two parallel inverters to merely 4.0% for three parallel inverters. Similar results can be seen in Tables 5.3 and 5.4.

It is clear that our experimental results support our observations based on simulation as discussed in Chapter 4, however the experimental THD values are much larger than those obtained by simulation. Factors contributing to increase THD as experimentally observed include: The inductor is non-ideal having significant losses and a nonlinear B-H curve (the well know hysteresis curve). Also, the BJT switches employed (for a 4V DC input) and MOSFET switches employed (for a 16 V DC input, c.f. Appendix D) have conduction losses, switching losses, and non-zero response times (but we did observe lower experimental THD in the case of a MOSFET H-bridge, c.f. Appendix D). Our microcontroller, the PIC16F877 (from Microchip technologies Inc.) requires 21 instructions cycles when using the on-chip timers (one instruction takes 6 microseconds for system clock of 20MHz as we used); this timer inaccuracy together with 8-bit integer round-off used to represent gating pulse widths also contributes to an error in experimental delivery of the gating signals. Finally, any noise in the DC input voltage will contribute to harmonics of the output voltage waveform and contribute to an increase in the output voltage THD.
5.5 Chapter Summary

This chapter presents the experimental waveform and THD results for single-phase full-bridge NSPWM inverter operation in the case of one inverter only, two parallel inverters synchronized with a delay of Tc/2, and three parallel inverters with delay Tc/3; in all cases the DC input is 4V. The parameters investigated in this chapter include modulation index M, the carrier frequency ratio, fc/fs, the number of inversion levels, and finally the number of parallel inverters used. The experimental results confirm the observation of Chapter 4 that the THD of the load voltage is decreased significantly if any one of the above mentioned parameters (M, fc/fs, number of inversion levels) is increased in value.

An important observation in this chapter is that as the number of parallel inverters is increased, the sideband harmonics approach the level of harmonics introduced by various sources of system noise. Hence in practice there may be a limit to N, the number of synchronized parallel inverters. In our case, we did not observe a great improvement in the THD when the number of inverters is increased from two to three, but of course at higher voltage levels and higher power levels, we can expect the limit on N to increase.
Chapter 6

Conclusions and Future Work

6.1 Conclusions

This thesis presents a comprehensive characterization of synchronously operated multiple single-phase inverters using phase-shifted naturally sampled pulse width modulation (PWM) to reduce the total harmonic distortion of the voltage waveform across the load. This scheme can be used for low voltage, low power applications. Our target applications are photo-voltaic (PV) systems, fuel cell systems, and uninterruptible power supply (UPS) systems. Motor drive systems, wind energy systems are among the possible secondary applications of this thesis. The harmonic performance of the proposed fixed-frequency open-loop pulse width modulation strategy with different modulation indices, inversion levels, and carrier-to-sine-wave frequency ratios has been investigated, by simulation work and experimentally, in the cases of two or three parallel inverters with one inverter operation serving as a reference case. The thesis contributions are:

1. We have shown that synchronizing the operation of N parallel inverters with a delay of $T_c/N$ (where $T_c$ is the carrier period) between the transistor gating functions of successive inverters results in an effective increase in the carrier frequency (by a factor of N) \textit{as well as} an increase in the effective number of inversion levels per cycle of the fundamental (ie, from 3-level for one inverter operation to $2N+1$ levels).

2. A near-optimum THD is obtained by introducing a transistor-gating delay of $T_c/N$ (where N is the number of parallel inverters) between each two successive inverters. This is based on the generalization of our investigation showing that in the case of two synchronized inverters the minimum THD occurs if the delay is approximately $T_c/2$ (actual minimum occurs for a delay of $0.506T_c$). For example in the case of three parallel inverters, $T_c/3$ is the near-optimal delay between any two of the inverters, where $T_c$ is the
period of the carrier triangular wave. This technique is straightforward, requiring only that an external trigger be provided to maintain phase-lock between the multiple inverters. Problems with the technique are (a) the increased cost of building N inverters in place of just one inverter and (b) the diminished improvement in THD performance as N increases (ie, as the number of inverters increases, the harmonic sidebands approach the “noise floor”).

3. Our characterization of synchronous multiple parallel inverter operation shows that with first-order LR filtering, two inverter operation can produce a load total harmonic distortion that is acceptable to industry (ie, less than 5%) with a carrier-to-sine-wave frequency ratio as low as 20.

4. More generally, for two parallel synchronized inverters, we obtained a typical reduction in the THD (in simulation) by a factor of about 0.3 for operation at the same modulation index, for a given number of inversion levels.

5. For three parallel synchronized inverters, we obtained a typical reduction in the THD (in simulation) by a factor of about 0.15 for operation at the same modulation index, for a given number of inversion levels.

6. We selected naturally-sampled pulse width modulation for our PWM approach. In this technique, the switching instances is selected at the intersection of a reference waveform and a high-frequency carrier rather than at the intersection of a regularly sampled reference waveform and high frequency carrier which is called regular sampled PWM. We avoided also the other scheme of switching which is processed so that the volt-second average of the reference waveform over the high frequency carrier cycle is the same as that of the inverter output (called direct PWM). In our approach we used a triangular carrier waveform (which is called double-edged NSPWM) instead of a saw-tooth waveform (called single-edged NSPWM). The reason behind this is that the double-edged NSPWM technique produces an improved harmonic profile.
7. Our experimental study supported our numerical simulation study. We experimentally investigated single-phase voltage source inverter operation with BJTs and MOSFETs. We showed that our gating technique can be implemented with an inexpensive microcontroller. Experimental results indicated that the proposed algorithm is practically realizable. Although, there is some deviations from the simulation results, indicating that real switching devices with non-zero conduction and switching losses and inexact gating pulse-widths introduce unwanted harmonic components.

6.2 Suggested Future Work

The following research topics are recommended for future work.

1. The proposed technique deals with a constant resistive load condition. Although our research has partially addressed the question of operation at different load power levels by varying the modulation index, it may be worthwhile to characterize multiple inverter operation as a function of load level for a near-constant modulation index.

2. The proposed approach is of greatest value at low carrier-to-sine-wave frequency ratios. If this ratio is sufficiently small, there is the possibility that sub-harmonics can be introduced into the load voltage waveform. A characterization of sub-harmonic components would be a worthwhile continuation of our thesis research.

3. Closed-loop PWM techniques are becoming an attractive issue for inverter designers and researchers. In an effort to reduce output current distortion it is possible to insert a feed-back current control block within the inverter controller. Hysteresis current control is one of the options that could be used for this purpose, and suggests the possibility of grid-connected synchronous multiple inverter operation.

4. Also, it may be possible to apply selective harmonic elimination to synchronous parallel inverter operation to obtain even lower THD values than we obtained using naturally sampled PWM.
References


Appendix A

MATLAB Coding

A.1 Simulink Calculation of Gating Pulse Widths

The comparator (called here the relational operator) compares the reference sine-wave with a certain M (Modulation Index) and triangular carrier wave with certain frequency, and the result is a plotting of both waveforms with intersection between them as illustrated in Fig.3.1 (for example).

Fig.A.1 Simulink circuit to determine the intersection points of reference and carrier waveforms
A.2 MATLAB Code for Calculating and Plotting the Output Voltage Waveform of 3-Level PWM for One Inverter Only

```matlab
close all;
clear all;
load m4.m; % load pulse values as obtained from SimuLink
plot(m4); title('Pulse Values'); figure;
dt=1; % increment of time
yf=0;
tau=1176.47; % time constant R=510 ohm, L=0.6 H, tau = L/R
y1(1)=-0.2924; % initial value
N=0;
tt=0;
delay2=186; % delay for inverter2
delay3=370; % delay for inverter3
for p=1:29 % No. of pulses in first half cycle
    gate_short = m4(1:p); %
    N = m4(p);
    for t=1:dt:N
        y1(t+t+1) = yf + (y1(t+t) - yf) * expm(-1 * dt / tau);
    end
    tt=sum(gate_short); % total time
    c=1.33*1^(-1)^(+1); % value of voltage at the end of any pulse
    yf=yf+c; % final voltage value
    plot(yf); title('yfinal'); figure;
end
yf=0; % initial value of the Vfinal at the beginning of second cycle
for p=30:58 % No. of pulses in second half cycle
    gate_short = m4(1:p);
    N = m4(p);
    for t=1:dt:N
        y1(t+t+1) = yf + (y1(t+t) - yf) * expm(-1 * dt / tau);
    end
    tt=sum(gate_short);
    c=1.33*1^(-1)^(+1);
    yf=yf-c;
end
plot(y); title('y'); figure;
yf=0;
for p=59:68 % add some extra to the complete cycle
    gate_short = m4(1:p);
    N = m4(p);
    for t=1:dt:N
        y1(t+t+1) = yf + (y1(t+t) - yf) * expm(-1 * dt / tau);
    end
    tt=sum(gate_short);
    c=1.33*1^(-1)^(+1);
    yf=yf+c; % Value of inverter 1 output voltage
end
for t=1:dt:18500
    y2(delay2+t)=y1(t); % Value of inverter 2 output voltage
    y3(delay3+t)=y1(t); % Value of inverter 3 output voltage
    yt(t)=y1(t)+y2(t)+y3(t); % Resultant value of all parallel inverters voltage.
end
```

for t=1:dt:16667
  yl_one_cycle(t) = yl(t);
  ytf(t) = yt(t+1300);  % shift final waveform back by approx. five pulses
end

plot(yl); title('yl'); figure;
plot(y2); title('y2'); figure;
plot(y3); title('y3'); figure;
plot(yt); title('yt'); figure;
plot(yl_one_cycle); title('yl for one cycle'); figure;
plot(ytf); title('yt total for one cycle: yt shifted back'); figure;
save('C:\Program Files\matlab704\work\ms4.m', 'ytf', '-tabs', '-ASCII');

A.3 MATLAB Code for Calculating and Plotting the Output Voltage Waveform of 3-Level PWM for Two Parallel Synchronized Inverters

close all;
clear all;
load ml.m;
plot(ml); title('Gating Waveform'); figure;
dt=1;
yf=0;
tau=1176.47;
yl(1)=-0.63;
%yt(1)=y(1)+yl(1);
N=0;
tt=0;
delayl=417;  % delay for inverter2
for p=1:19
  gate_short = ml(1:p);
  N= ml(p);
  for t=1:dt:N
    yl(tt + t+1) = yf + ( yl(tt+t) - yf ) * expm( -1 * dt / tau );
  end
  tt=sum(gate_short);
c=2*(-1)^(p+1);
yf=yf+c;
%plot(yf); title('yfinal'); figure;
end
%plot(y); title('y at half way'); figure;
yf=0;
for p=20:38
  gate_short = ml(1:p);
  N= ml(p);
  for t=1:dt:N
    yl(tt + t+1) = yf + ( yl(tt+t) - yf ) * expm( -1 * dt / tau );
  end
  tt=sum(gate_short);
c=2*(-1)^(p);
yf=yf-c;
end
%plot(y); title('y'); figure;
yf=0;
for p=39:45
    gate_short = ml(1:p);
    N= ml(p);
for t=1:dt*N
    y1(tt + t+1) = yf + ( y1(tt+t) - yf ) * expm( -1 * dt / tau );
end
end

plot(y1); title('y1');figure;
plot(y2); title('y2');figure;
plot(yt); title('yt');figure;
plot(ytf); title('yt shifted back 5 pulses');figure;
save('C:\Program Files\matlab704\work\ms1.m','ytf','-tabs','-ASCII');

A.4 MATLAB Code for Calculating and Plotting the Output Voltage Waveform of 3-Level PWM for three parallel synchronized Inverters

close all;
clear all;
load ml.m;% load pulse values
plot(ml); title('Pulse Values');figure;
dt=1;% increment of time
yf=0;
tau=1176.47;% time constant R=510 ohm, L=0.6 H,tau = L/R
y1(1)=-0.42;% initial value
%y2(1)=-0.30;
%y3(1)=-0.30;
%yt(1)=y1(1)+y2(1)+y3(1);
N=0;
for t=1:dt:18500
    y2(delay1+t)=y1(t);
yt(t)=y1(t)+y2(t);
end
for t=1:dt:16667
    ytf(t)=yt(t+1300);%shift final waveform back by T/2
end

plot(y1); title('y1');figure;
plot(y2); title('y2');figure;
plot(yt); title('yt');figure;
plot(ytf); title('yt shifted back 5 pulses');figure;
save('C:\Program Files\matlab704\work\ms1.m','ytf','-tabs','-ASCII');

for p=1:19 % No. of pulses in first half cycle
    gate_short =ml(1:p);
    N= ml(p);
for t=1:dt:N
    y1(tt + t+1) = yf + ( y1(tt+t) - yf ) * expm( -1 * dt / tau );
end
end

plot(yf); title('yfinal');figure;
plot(y); title('y at half way');figure;
yf=0;% initial value of the Vfinal at the beginning of second cycle
for p=20:38 % No. of pulses in second half cycle
gate_short = ml(1:p);
    N= ml(p);
for t=1:dt:N
    y1(tt + t+1) = yf + ( y1(tt+t) - yf ) * expm( -1 * dt / tau );
end
tt=sum(gate_short);
c=1.33*(-1)^p;
yf=yf-c;
end
%plot(y); title('y');figure;
yf=0;
for p=39:45 % add some extra to the complete cycle
    gate_short =ml(1:p);
    N= ml(p);
for t=1:dt:N
    y1(tt + t+1) = yf + ( y1(tt+t) - yf ) * expm( -1 * dt / tau );
end
tt=sum(gate_short);
c=1.33*(-1)^p-1;
yf=yf+c; % Value of inverter 1 output voltage
end
for t=1:dt:18500
    y2(delay2+t)=y1(t); % Value of inverter 2 output voltage
    y3(delay3+t)=y1(t); % Value of inverter 3 output voltage
    y(t)=y1(t)+y2(t)+y3(t); % Resultant value of all parallel inverters voltage.
end
for t=1:dt:16667
    y1_one_cycle(t) = y1(t);
    ytf(t)=yt(t+1400); % shift final waveform back by appr. five pulses
end
plot(y1); title('y1');figure;
plot(y2); title('y2');figure;
plot(y3); title('y3');figure;
plot(yt); title('yt');figure;
plot(y1_one_cycle); title('y1 for one cycle');figure;
plot(ytf); title('y total for one cycle: yt shifted back');figure;
save('C:\Program Files\matlab704\work\msl.m','ytf','-tabs','-ASCII');
A.5 MATLAB Code for Calculating the Total Harmonic Distortion and Plotting of Fourier Coefficients up to $N_T = 200$

close all;
clear all;
load msl.m;% msl is the file(contains the output voltage waveform) to be loaded
N=16667;% number of points from which form the sine waveform
T= 0.01678;% the period of each points in the waveform
w=2*pi/T;
yos = msl(1:N);% row vector
figure;plot(yos,'color','k','linewidth',1.5);% plot the sine waveform with black color
xlabel('Time [\mu s]','Fontsize',14);% label x-axis with micro sec.
ylabel('Vout [V]','Fontsize',14);%label y-axis with Vout[volt],font 14
set(gca,'Fontsize',14,'linewidth',1.5)%;set the edges of both x,y axis with line thick 1.5,font 14
axis([0 18000 -4 4]);% set the x and y axis with the range in the bracket.
k= 1:N;
t=k*T/N;
for h=2:1:200 % No. of harmonic frequencies
ch = cos(h*w*t); % row vector
sh = sin(h*w*t); % row vector
voch= yos*ch'; % elementwise vector product -> vector result
vosh= yos*sh';
dt= T/N;
vochdt= voch * dt;
voshdt= vosh * dt;
integc= sum(vochdt);
integs= sum(voshdt);
ah= (w/pi) * integc;
bh= (w/pi) * integs;
rh=((ah)^2+(bh)^2)^0.5;
ahvec(h)=ah;
bhvec(h)=bh;
rhvec(h)=rh;
s(h)=(rh)^2;
qh=atan(bh/ah);
phase(h)=qh
end
figure; stem(rhvec,'marker','none','color','k','linewidth',1.5);% Set the harmonic number in bar type.
xlabel('fh / fs','Fontsize',14);% Set x-axis label with font size 14
ylabel('Harmonic Amplitude [V]','Fontsize',14);%set y-axis label with font size 14
set(gca,'Fontsize',14,'linewidth',1.5)% set x,y axis edge and line width.
axis([0 200 0 0.5]);% range of x,y axis respectively
s1=rhvec(1);
s2=(s1)^2
s4=sum(s);
s6=((s4-s2)^0.5)
s7=s6/s1
figure;plot (s7); %stem(s7);
Appendix B

Description of Experimental Hardware

There are many components used in the experimental part of this research:

B.1 Microcontroller PIC16F877

The PIC originally stood for Programmable Intelligent Computer. It is, in general, an inexpensive one-chip device designed and manufactured by microchip technology, Inc. In 1977, General Instruments developed the PIC 1650. The PIC 1650 which is considered now as a grand father of today’s PICs [B1].

Microchip Inc. purchased microcontroller business in the mid 1980s from the original manufacturer of PIC, General Instruments. Microchips produce about 200 different types of PIC Microcontrollers, which is the Microchips official name for the PIC. PIC Microcontroller operation is similar to microprocessors, but it is simpler, smaller in size and cheaper. Its outside world connections distinguish it from Microprocessor, so it is called Microcontroller. Microcontrollers can be adapted to control power electronic switching circuits, conventional relays, lamp circuits, measuring instruments. The main elements inside the PIC:

1. Central Processing Unit: The Central Processing Unit (CPU) is the microcontroller’s intelligence. It performs many functions including the logical and arithmetic functions of the PIC according to the instruction it reads from the program memory. It reads from and writes to the data memory and input/output module.

2. Program memory: this memory is feeding the instructions for the CPU. The CPU reads the all information in this memory.

3. Data memory: it contains all necessary data that is needed by programming. The CPU reads from and writes to data memory.

4. Input/output: These are the ports that the PIC communicates with the world outside the chip

5. Peripherals: these are some special functional elements built into the PIC, such as timers, analogue to digital converters, and pulse width modulators. Fig B.1 Shows the PIC elements and outer connections
After downloading of MPLAB Integrated Development Environment (IDE) program, which runs on a PC. An editor is used to write assembly code, build and assemble the project, and then the code is tested with the built-in simulator and debugger. The compiler or assembler is used to convert the source code to machine code. After debugging process is completed, the program is to be downloaded to the PIC by an appropriate programmer.

In our experiment we utilize the PIC16F877 which is from the PIC16F87X family of microchips. We use assembly language to write the program source files. This device with 40-pin 8-bit CMOS FLASH technology has the following features [B2]:

A. Core features including, but not limited to, the following:

- High-performance RISC CPU
- Required only 35 single word instructions to learn for programming.
- All single cycle instructions except for program branches which are two cycle.
- Operating speed: DC- 20 MHZ clock input; DC-200 ns instruction cycle.
- Up to 8K x 14 words of FLASH Program Memory, up to 368 x 8 bytes of Data Memory (RAM), and up to 256x8 bytes of EEPROM data memory
- Interrupt capacity up to 14 sources
- Eight level deep hardware stack
• Power-on Reset (POR)
• Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
• Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
• Programmable code-protection
• Power saving SLEEP mode
• Selectable oscillator options
• Low-power, high-speed CMOS FLASH/EEPROM technology
• Fully static design
• In-Circuit Serial Programming, In-Circuit Debugging and testing
• Processor read/write access to program memory
• Wide operating voltage range: 2.0V-5.5 V

B. Peripheral Features:
• Timer0: 8-bit timer/counter with 8-bit prescaler
• Timer1: 16-bit timer/counter with prescaler
• Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
• 10-bit multi-channel Analog-to-Digital converter
• Brown-out detection circuitry for Brown-out Reset (BOR)
• Synchronous Serial Port (SSP)
• Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
• Parallel Slave Port (PSP), with external read, write, etc, controls

The MPASM assembler from Microchip Technology (manufacturer of PIC family) is the PIC assembler that is used after the build-up of the assembly program. We use PICSTART Plus programmer which will program all PIC micro-controllers. So, a combination of the PIC16F877, MPASM assembler and low cost PIC16F877 programmer constitute competitive development system that is used to create microcontroller based project.

The output of this microcontroller is used to gating the inverter transistors. Fig.B.2 shows the connection of microcontroller to be connected to the function generator (synchronizer) and its associated inverter.
There are three types of memory in PIC16F877 central processing unit (CPU). The program memory, data memory. The data, which is of hexadecimal form, is stored in data memory. The data memory consists of different banks which contain the General Purpose Registers and the Special purpose registers. These registered are designed as static random access memory (RAM) to store the data. The assembly language Program is stored in FLASH Program Memory.

The PIC16F877 microcontroller has five I/O ports. Some pins for these I/O ports can be used also as inputs for some peripheral features of the PIC such as timers, or analogue signals. The pins of these ports can be configured as input or output through setting of the port data direction register.

B. 2 Oscilloscope

Tektronix TDS3032B two channel color Digital Phosphor Oscilloscope 300 MHz is used to display the synchronized output voltage waveform. By displaying the waveform on oscilloscope, we can adjust the synchronizer to get the optimum required signal. Also we use Tektronix P 5205, 100 MHz, and high voltage differential probes.
B.3 FLUKE 39 Power Meter

This device is used to measure both, frequency and total harmonic distortion (THD) of the synchronized output voltage waveform. By using this device we can get the desirable synchronized output signal of frequency (near 60 Hz) and of minimum THD. Then this signal (which is shown in oscilloscope) can be saved and analyzed, using MATLAB program, to find the exact and accurate voltage waveform THD.

B.4 Function Generator

WAVETEK P5205, 4MHz function generator model 182A is used to synchronize the parallel inverters. As mentioned earlier, there is a phase shift angle between parallel inverters, so the system has to be in synchronized state to produce the required minimum THD. The function generator is used as a master, it sends out a synchronization pulse during each cycle period of modulating signal, and this pulse is transmitted to PORT B of the PIC of each inverter (which is considered as a slave). Upon detection of the rising edge of this pulse, and through the software program (see Appendix C), is considered as external interrupt and is captured by all PICs at the same time. By adjusting the frequency of the function generator pulse, the synchronization is occurred. Fig. B.3 shows the detail connection of pulse-generator with all parallel inverters.

Fig.B.3. Pulse generator connected to 3-parallel inverters
B.5 MOSFET and Bi-polar Transistor Power Supply

Fig.B.4 shows the power supply designed for bi-polar transistor supply voltage and MOSFET supply source. It consists of a 120/30 V transformer and a full wave rectifier at the output. The rectified voltage is filtered out using capacitors. The voltage regulator LM 317 gives output of 0-30 V<sub>dc</sub>. The output voltage of the voltage regulator can be varied through 10 KΩ potentiometer. The capacitors at the regulator output improve the transient stability and contribute to fine control of the output voltage.

Fig.B.4. Schematic diagram of the MOSFET and bi-polar transistors power supply

B.6 MOSFET- Gate Drives

To turn on the MOSFET switching device, it is necessary to set the gate-source voltage higher than the threshold voltage, \( V_{GSth} \) (typically 2-4 V) for high voltage MOSFETs (larger than 100V) and 1-2 V for low-voltage MOSFETs (lower than 100V) [B3]. For turn off, it is required that \( V_{GS} \) must be set below \( V_{GSth} \). An off-state \( V_{GS} \) of zero voltage is sufficient.

Fig.3-14 shows the IR2110-MOSFET get drive block diagram. This driver is of high voltage and high speed power rating with separate high and low side referenced output channels. It can operate with logic voltage down to 3.3 V.
In this circuit the $V_{GS} = 15$ V. When the PIC high-side is in logic1 (5 V), the high-side MOSFET (upper-right side) will conduct and its source voltage will rise to HV Supply voltage (16 V in our experimental test), so the $V_{GS}$ will go down to -31 V. The driver main function is keep the $V_{GS} = 15$ V to keep the device conducting as long as the PIC high-side in logic1. Fig B.5 shows MOSFET circuit diagram with IR2110 gate driver (we did not use the IRF1830).

![MOSFET circuit diagram with IR2110 gate driver](image)

Fig.B.5. MOSFET circuit diagram with IR2110 gate driver

**B.7 Transistor Base Drive**

Transistor 2N3904, NPN type is used as switching device for all inverters in all 4V experiments in this thesis. The static characteristics of this type of transistors are: $V_{ce} = 30V_{dc}$, $V_{bc} = 0.5V_{dc}$, $I_{c} = 10mA$, $I_{b1} = 1.0$ mA. The base circuit of transistor is derived from 5 V$_{dc}$ from output of the microcontroller. Fig.B.6 shows the single-phase inverter utilizing these transistors as switching device. Note that each transistor is shunted by a back-connected diode to protect it from back electromotive force (emf) this is generated during transistor off-period because of inductance load.
B.8 Development Boards

Three PIC microcontroller development boards are utilized to gating three inverters (designed and built in-house by Richard Galambos).

B.9 Inductors

Three inductors (each for one inverter) of value 0.6 Henry and of current rating 750 mA.

B.10 PIC START Plus Development Programmer

This device is used to program the PIC with necessary instructions and data that is created by MP-LAB (assembly programming software from Microchip technology Inc.).

Appendix C

Assembly Code for the PIC16F877

C.1 Assembly Code Main Program For Two-inversion Level PWM

In designing assembly code for the PWM technique, two-inversion level, it is necessary to determine the PWM pulses output required to generate ideal sinusoidal waveform. The pulses is going to be positive supply voltage (+ V_{dc}) value if the reference sine wave value is higher than the triangle carrier value and going to be negative (- V_{dc}) if the reference value is less than carrier value. The pulses duration is then defined from these intersection points and convert to hexa-decimal values for implementation in the assembly code. Now the important point is how to select the transistors pattern to produce this train of PWM pulses. In Fig.2.5, for two-level PWM, the output voltage in the load will be negative if T2-T3 is going to logic 1 and the others in logic 0, so the pattern will be (0x06), and similarly the pattern will be (0x0c) for getting negative pulse. Recall that the PIC timer/counter generate an interrupt signal upon overflow at 0xFF, thus, it is a simple matter of setting the timer at a specific value and letting it count to interrupt where the pulse changes its state (from negative to positive or vice versa). These values are arranged as a lookup table in the PIC data memory. By using MPLAB Integrated Development Environment software (IDE) which is windows-based and allows the designer to write and debug the code.

; main program
bcf     intcon, 2 ; TMR0 did not overflow
bsf     intcon, 7 ; global interrupt enable bit
bsf     intcon, 5 ; TMR0 interrupt enable
bsf     status, 5 ; bank 01 selection
movlw   0xd4 ; prescaler divide by 16
begin
movwf   opt_reg ; copy the value d4 to option_reg register
        bsf     status, 5 ;
        bsf     opt_reg,6 ; interrupt on rising edge of RB0/INT pin
        bcf     status, 5 ; bank 00 selection
        bcf     intcon,1 ; RB0/INT external interrupt did not occur
        bcf     intcon,4 ; disable RB0/INT external interrupt
        btfss    intcon,1 ; RB0/INT external interrupt occurred
        goto    alpha ;
        bcf     intcon,2 ;
        bsf     intcon,7 ;
        bsf     intcon,5 ;
        movlw   0x06 ; copy (0000 0110) to Pat file
        movwf    pat
        movwf    porta ; copy (0000 0110) to port a
C.2 Assembly Code Main Program for Three-inversion Level PWM

In designing assembly code for the PWM technique, three-inversion level, it is necessary to determine the PWM pulses output required to generate ideal sinusoidal waveform. The same procedure of two-level PWM assembly code is applicable here except that the transistor pattern is different somewhat. For positive half cycle of the reference sine waveform, the pattern will be (0x0c) for zero pulses output and (0x09) for positive output pulses. For negative half cycle, the pattern for zero-output pulses will be (0x03) and (0x06) for negative output pulses.
; main program

bcf intcon,2 ; TMR0 did not overflow
bsf intcon,7 ; global interrupt enable bit
bsf intcon,5 ; TMR0 interrupt enable
bsf status,5 ; bank 01 selection
movlw 0xd4 ; prescaler divide by 16
movwf opt_reg ; copy the value d4 to option_reg
begin bsf status,5
bsf opt_reg,6 ; interrupt on rising edge of RB0/IN
bsf status,5 ; bank 00 selection
bcf intcon,1 ; RB0/INT external interrupt did not occur
bcf intcon,4 ; disable RB0/INT external interrupt
beta btfss intcon,1 ; RB0/INT external interrupt occurred
goto beta
bcf intcon,2
bsf intcon,7
bsf intcon,5
movlw 0x0c ; copy the value (0000 1010) to pat(file)
movwf pat
movlw 0x0c
movwf porta ; copy the value (0000 1010) to port a
movlw min_val ; copy min.value of to the W register
movwf fsr ; Set pointer to the min.value
movf indf,0 ; move the value to indirect file
movwf tmr0 ; copy the value to the TMR0
movf pat,0 ; copy the value to the W register
xorlw 0x05 ; exclusive of the current value
movwf pat ; no operation
circle nop
goto circle ; go to circle

; iser
bcf intcon,2
bsf intcon,7
bsf intcon,5
incf fsr
movf pat,0
movwf porta
movlw max_val
xorwf fsr,0
btfss status,2 ; check if it is the last pulse
goto gama ; yes, it is the last pulse
movlw 0x0c ; no, it is not the last pulse
movwf porta
goto begin
Here, we present the assembly flow chart for 2-level PWM only.

This flow chart illustrates the generation of 2-level PWM. After the calculation of pulses duration. The hexadecimal values are stored in lookout table in PIC data memory and used as input to the PIC. The Port B of the PIC is selected as input and port A as output. The program detects if there is an interrupt occurs in port B, this means that the Synchronization signal comes out from the function generator is detected and the program will start.

The timer TMRO is incremented by incoming pulses. When the count climbs through 0XFF. The timer has an interrupt on overflow from 0XFF to 0x00. Then the
program will take another pulse as input. This is evident from the Interrupt Service Routine (SIR) so that the program will select negative input pulse first time and then positive pulse second time alternately. When the program reaches the final value of the pulse, it will stop automatically.

**Main program**

```
<table>
<thead>
<tr>
<th>Port B inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port A Outputs</td>
</tr>
<tr>
<td>Port B All Lines High</td>
</tr>
<tr>
<td>Port A All Lines Low</td>
</tr>
<tr>
<td>Clear TMR0 Interrupt Flag</td>
</tr>
<tr>
<td>Enable Global Interrupt</td>
</tr>
<tr>
<td>Enable TMR0 Interrupt</td>
</tr>
<tr>
<td>Load Mode Register</td>
</tr>
<tr>
<td>Clear WDT, Assign Prescaler</td>
</tr>
<tr>
<td>Setup Option Register</td>
</tr>
</tbody>
</table>

No

RB0/INT external interrupt occurred

Yes

Start Count

Load /Start TMR0

Circle (generates interrupt)
```
Interrupt Service Routine (ISR) for 2 Level PWM

1. TMR0 Interrupt Flag at 0xFF
2. Clear TMR0 Interrupt Flag
3. Move Pulse Value To FSR
4. Move Contents of FSR to TMR0
5. Is Mode = 0?
   - No: Set Port A To Logic 1
   - Yes: Set Port A To Logic 0
6. Is FSR= Last Pulse Value?
   - No: Return From Interrupt
   - Yes: Return From Interrupt

Done
Appendix D

Experimental Results for a 16 V DC Single-Phase MOSFET Inverter

D.1 Experimental Output Voltage Waveforms and Fourier Coefficients for $V_{dc} = 16V$

![Waveform and Fourier coefficients](image)

**Fig.D.1.** One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=0.6$, $f_c/f_s = 20$, $c_1=4V$, THD = 14.6 %

Bottom: 3-level NSPWM, $M=0.9$, $f_c/f_s = 20$, $c_1=5.96 V$, THD = 7.8 %
Fig.D.2. One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=1.0$, $f_c/f_s=20$, $c_1=6.538\,\text{V}$, THD = 6.3 %

Bottom: 3-level NSPWM, $M=1.15$, $f_c/f_s=20$, $c_1=7.01\,\text{V}$, THD = 6.0 %
Fig. D.3. One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 2-level NSPWM, M=0.6, fc/fs =21, c1=3.95V, THD = 26.1 %
Bottom: 2-level NSPWM, M=0.9, fc/fs =21, c1=5.9 V, THD = 14.1 %
Fig. D.4. One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 3-level NSPWM, $M=0.6$, $f_c/f_s=30$, $c_1=4V$, THD = 10.8 
Bottom: 3-level NSPWM, $M=0.9$, $f_c/f_s=30$, $c_1=5.95V$, THD = 5.7 %
Fig. D.5. One inverter only operation: voltage waveform and Fourier component magnitudes

Top: 2-level NSPWM, $M=0.6$, $f_c/f_s =31$, $c_1=3.89V$, THD = 19.7 %

Bottom: 2-level NSPWM, $M=0.9$, $f_c/f_s =31$, $c_1=5.8V$, THD = 10.6 %
D.2 16V Experimental Results Summary

The following table illustrates the summary of experimental THD results for one inverter, (as obtained in the Power Electronics Laboratory of the University of Calgary) employing a 16 volt input supply and MOSFET switches in the H-bridge.

Table D.1 Experimental Load Voltage THD for Single-phase One Inverter Operation, where \( V_{dc} \) is 16V, using MOSFET Switches

<table>
<thead>
<tr>
<th>Carrier Frequency Ratio (fc/fs)</th>
<th>Modulation Index (M)</th>
<th>No. of inverter levels</th>
<th>THD (Theoretical)</th>
<th>THD (Experimental)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.9</td>
<td>3-level</td>
<td>12.68 %</td>
<td>22.4 %</td>
</tr>
<tr>
<td>14</td>
<td>0.9</td>
<td>3-level</td>
<td>9.23 %</td>
<td>10.2 %</td>
</tr>
<tr>
<td>20</td>
<td>0.3</td>
<td>3-level</td>
<td>16.64 %</td>
<td>20.4 %</td>
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