Advanced Doherty Power Amplifier Architectures for Broadband and Multistandard Wireless Transceivers

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Advanced Doherty Power Amplifier Architectures for Broadband and Multistandard Wireless Transceivers

by

Ramzi Darraji

A THESIS
SUBMITTED TO THE FACULTY OF GRADUATE STUDIES IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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Abstract

Power amplifiers (PAs) have always been a pivotal front-end building block in wireless communication transmitters. As signal modulation schemes become more spectrally efficient and cellular traffic increasingly intense, the radio frequency (RF) performance of PAs should be constantly improved. This can be achieved by improving the analog circuit design of the PA and by including additional software and system features to balance energy consumption and performance.

This thesis focuses on several aspects related to power efficiency enhancement and bandwidth extension of wireless Doherty PAs using baseband digital signal processing (DSP) techniques. A variety of digital signal conditioning algorithms are proposed to enable optimal Doherty PA operation at and beyond its nominal frequency bandwidth. An innovative dual-input Doherty PA architecture is also presented in this work to enable the implementation of these advanced DSP techniques.

Analog circuit design and optimization approaches are investigated and proposed for the enhancement of Doherty PA performance. Experimental implementation is carried out to validate the proposed techniques. Critical issues related to complex gain imbalance as well as energy waste within the RF building blocks of the Doherty PA are studied and mitigated. Two advanced methodologies, namely digital adaptive phase alignment and digital adaptive input power distribution, are developed to effectively address the above-mentioned problems.

The frequency response of Doherty PAs is analyzed; and, a novel digital domain based precompensation mechanism is derived to mitigate the bandwidth limitations of
Doherty PAs, resulting in substantial bandwidth extension. An original architecture of a digitally equalized Doherty PA based RF front-end is proposed to allow the use of Doherty PAs in the context of wide bandwidth and multistandard radios.
Preface

This thesis is submitted to the Faculty of Graduate Studies in partial fulfilment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering. It reports the work that I have conducted in University of Calgary’s Intelligent RF Radio Technology Laboratory (iRadio Lab) from September 2008 to December 2012. This thesis has been solely written by me and revised by my supervisor, Dr. Fadhel M. Ghannouchi. Most of the text in Chapters 3-7 is based on publications that have arisen from my research work.

A version of Chapter 3 has been published: R. Darraji, F. M. Ghannouchi, and O. Hammi, “Generic load-pull based design methodology for performance optimization of energy-efficient Doherty amplifiers,” IET Science Measurement & Technology, vol. 6, no. 3, pp. 132–138, May 2012. I conducted the tests and wrote the manuscript. Dr. Ghannouchi and Dr. Hammi have helped in editing the paper.

A version of Chapter 4 has been published: R. Darraji, F. M. Ghannouchi, and O. Hammi, “A dual-input digitally driven Doherty amplifier architecture for performance enhancement of Doherty transmitters,” IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 5, pp. 1284–1293, May 2011. I performed the measurements and drafted the manuscript. Dr. Ghannouchi and Dr. Hammi have provided technical advices and contributed in revising the paper.

A version of Chapter 5 has been published: R. Darraji and F. M. Ghannouchi, “Digital Doherty amplifier with enhanced efficiency and extended range,” IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 11, pp. 2898–2909,
Nov. 2011. I performed the practical tests and drafted the manuscript. In addition to his technical input, Dr. Ghannouchi has also helped in reviewing the paper.

A version of Chapter 6 has been published: R. Darraji, F. M. Ghannouchi, and M. Helaoui, “Mitigation of bandwidth limitation in wireless Doherty amplifiers with substantial bandwidth enhancement using digital techniques,” IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 9, pp. 2875–2885, Sep. 2012. I conducted the measurements and wrote the manuscript. Dr. Ghannouchi and Dr. Helaoui have contributed with technical suggestions. They have also helped in reviewing the paper.

A version of Chapter 7 has been submitted for peer review: R. Darraji, F. M. Ghannouchi, and M. Helaoui, “Digitally equalized Doherty RF front-end architecture for broadband and multistandard wireless transmitters,” IEEE Transactions on Industrial Electronics, Submitted, Aug. 2012. I conducted the tests and drafted the manuscript. Dr. Ghannouchi and Dr. Helaoui have provided technical advices. Dr. Ghannouchi has helped in revising the paper.
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I would like to acknowledge the Alberta Innovates Technology Futures (AITF) and the Department of Electrical and Computer Engineering at the University of Calgary for the financial support through their graduate student scholarship programs.

Finally, I would like to take this opportunity to express my sincere recognition to all instructors and professors who have taught me throughout my academic career.
To My Parents,
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<td>4G</td>
<td>Fourth generation</td>
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<tr>
<td>ACPR</td>
<td>Adjacent channel power ratio</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced design system</td>
</tr>
<tr>
<td>AM/PM</td>
<td>Amplitude-dependent phase distortion</td>
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<tr>
<td>AWG</td>
<td>Arbitrary waveform generator</td>
</tr>
<tr>
<td>BFOM</td>
<td>Baliga’s figure of merit</td>
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<tr>
<td>CDMA</td>
<td>Code division multiple access</td>
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<tr>
<td>CFR</td>
<td>Crest factor reduction</td>
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<tr>
<td>CW</td>
<td>Continuous wave</td>
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<tr>
<td>DC</td>
<td>Direct current</td>
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<tr>
<td>DPD</td>
<td>Digital predistortion</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital signal processing</td>
</tr>
<tr>
<td>EER</td>
<td>Envelope elimination and restoration</td>
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<tr>
<td>ET</td>
<td>Envelope tracking</td>
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<tr>
<td>FET</td>
<td>Field effect transistor</td>
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<tr>
<td>FIR</td>
<td>Finite impulse response</td>
</tr>
<tr>
<td>FLOP</td>
<td>Floating point operation</td>
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<tr>
<td>FPGA</td>
<td>Field programmable gate array</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium nitride</td>
</tr>
<tr>
<td>GMP</td>
<td>Generalized memory polynomial</td>
</tr>
<tr>
<td>GPIB</td>
<td>General-purpose interface</td>
</tr>
<tr>
<td>HEMT</td>
<td>High electron mobility transistors</td>
</tr>
<tr>
<td>HSPA</td>
<td>High speed packet access</td>
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<tr>
<td>IEEE</td>
<td>Institute of electrical and electronics engineers</td>
</tr>
<tr>
<td>I/Q</td>
<td>In-phase/quadrature</td>
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<tr>
<td>IMD3</td>
<td>Third order intermodulations</td>
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<tr>
<td>LDMOS</td>
<td>Laterally diffused metal oxide semiconductor</td>
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<tr>
<td>Acronym</td>
<td>Definition</td>
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<tr>
<td>LINC</td>
<td>Linear amplification with nonlinear components</td>
</tr>
<tr>
<td>LTE</td>
<td>Long term evolution</td>
</tr>
<tr>
<td>LUT</td>
<td>Look-up table</td>
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<tr>
<td>OFDM</td>
<td>Orthogonal frequency division multiplexing</td>
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<tr>
<td>OPBO</td>
<td>Output power back-off</td>
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<tr>
<td>PA</td>
<td>Power amplifier</td>
</tr>
<tr>
<td>PAE</td>
<td>Power-added efficiency</td>
</tr>
<tr>
<td>PAPR</td>
<td>Peak-to-average power ratio</td>
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<tr>
<td>PDF</td>
<td>Probability density function</td>
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<tr>
<td>PDPD</td>
<td>Phase digital predistortion</td>
</tr>
<tr>
<td>PSD</td>
<td>Power spectral density</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadratic amplitude modulation</td>
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<tr>
<td>RCE</td>
<td>Relative constellation error</td>
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<tr>
<td>RF</td>
<td>Radio frequency</td>
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<tr>
<td>SDR</td>
<td>Software defined radio</td>
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<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>SiC</td>
<td>Silicon carbide</td>
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<tr>
<td>SISO</td>
<td>Single-input single-output</td>
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<tr>
<td>SSG</td>
<td>Small signal gain</td>
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<tr>
<td>VSA</td>
<td>Vector signal analyzer</td>
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<tr>
<td>WCDMA</td>
<td>Wideband code division multiple access</td>
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<tr>
<td>WiMAX</td>
<td>Worldwide interoperability for microwave access</td>
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</table>
Chapter One: Introduction

1.1 Motivation

To cope with the shortage of spectrum resources and the ever-increasing demand for mobile connectivity with higher data throughput, modern wireless communication systems, including High Speed Packet Access (HSPA), Worldwide Interoperability for Microwave Access (WiMAX) and Long Term Evolution (LTE) standards, usually feature spectrum efficient modulation and access techniques. Orthogonal frequency division multiplexing (OFDM), code division multiple access (CDMA) and M-ary quadratic amplitude modulation (M-QAM, where M can be up to 256) are some of these methods.

Although the above-mentioned approaches permit efficient management of the overcrowded radio frequency (RF) spectrum, they also result in the creation of highly varying envelope communication signals that are characterized with high peak-to-average power ratios (PAPRs), which, in turn, present the challenge of energy efficient and linear (i.e., high fidelity) power amplification of amplitude-modulated signals. Indeed, to avoid signal clipping and loss of transmitted information in the form of undesirable distortion during power amplification, a wireless transmitter should be able to handle the peak values of the RF signal, although it mainly operates at significantly lower average power (typically 7 to 11 dB below the peak value). Accordingly, the power amplifier (PA) has to operate at a large back-off from its saturation power level, where its efficiency drops drastically [1, 2]. Therefore, high PAPRs not only stress the linearity of the PA, but also degrade the average transmission efficiency, due to the need for output power back-off (OPBO).
Benefiting from the advantages of the integration of analog circuits and digital signal processing (DSP) technologies, DSP based approaches have been increasingly investigated as a viable tool to improve the overall performance of RF PAs. Digital signal conditioning algorithms, such as crest factor reduction (CFR) for PAPR reduction and digital predistortion (DPD) for PA linearization, have been extensively implemented in cellular base station transmitters. While the CFR technique permits the reduction of the PAPR of the signal being transmitted and, thus, improves the power efficiency of the wireless transmitter [3, 4], DPD is essential for compliance with the linearity requirements imposed by spectrum emission regulations for the intended wireless communication standard [5, 6].

Analog PA circuits, on the other hand, have evolved from expensive feedforward linear and mildly nonlinear class AB types to more energy efficient PA architectures. For instance, Doherty PAs, which contain one carrier amplifier (always active) and one peaking amplifier (active only when signal peaks occurs), show maximum efficiency at power levels 6 to 12 dB below the saturation point, matching with the PAPR values of interest [7]. Likewise, transistor technology has progressed from moderately efficient laterally diffused metal oxide semiconductor (LDMOS) to highly reliable gallium nitride (GaN) devices, which can handle higher temperatures and higher voltages [8].

Due to the high demand on RF performance, base station PAs are mainly designed to operate within fixed and relatively narrow frequency bands. The continuous proliferation of wireless communication standards and the evolution of wireless communication technology towards the usage of nonfixed spectrum allocations have
brought new challenges in terms of reconfigurable operation, which also call for the use of mixed RF/DSP approaches to support the frequency band plurality.

Reconfigurability, as with software defined radio (SDR) systems, is essential to ensure the coexistence of current and forthcoming wireless communication standards. This implies that the PA should be able to operate not only within its nominal frequency band of design, but should also be capable to support further frequency bands without being constrained by hardware circuitry [9].

Cognitive radio, on the other hand, has been repeatedly confirmed as an enabling technology for forthcoming radio systems [10]. It uses the concept of opportunistic usage of the frequency bands that are not heavily occupied by licensed (primary) users to alleviate the problem of spectral congestion and enable new communication services. The dynamic nature of spectrum access within cognitive radio applications imposes additional requirements on the PA for efficient operation beyond its nominal frequency band, in order to make good use of the available opportunity in the spectrum.

Moreover, with the aim of achieving higher data rates, emerging fourth generation (4G) standards (e.g., LTE-Advanced) are supporting the use of aggregation of component carriers, which results in creating multicarrier signals with bandwidths up to 100 MHz [11]. Therefore, base station transmitters are expected to handle wider bandwidths and include multiple radios in one transmitter path, which requires broad bandwidth PAs.

It is clear that the emerging trends within wireless communication technologies are leading to an imminent need for producing more energy efficient, broadband and multistandard power amplification systems. This defines the framework of this thesis,
which proposes an advanced architecture of a digitally driven Doherty PA as a suitable power amplification topology for emerging wireless communication and SDR systems.

1.2 Objectives

The overall objectives of this thesis are related to the development of innovative methodologies for efficiency enhancement and bandwidth extension of wireless Doherty PAs. This work is particularly focused on Doherty PA architecture because, despite its popularity, it is often prone to several imperfections that degrade its efficiency and limit its convenience for broadband and multistandard applications, which leaves room for significant improvements.

The emphasis of the present work is on the development of DSP based techniques that are capable of effectively compensating for all hardware impairments compromising the RF performance of the Doherty PA and extending its optimal operation far beyond its original frequency band. Ultimately, the methodologies proposed in this research work will enable the implementation of efficiency enhanced and digitally driven Doherty PAs that are suitable for broadband and multistandard communication systems.

The specific objectives of the current work are classified into three phases:

1. Design of performance enhanced analog Doherty PAs. This topic consists of investigating potential hardware-based improvements and design approaches to get the best possible performance out of the analog circuit, prior to further improvement using software-based techniques. This phase targets the design of an optimized Doherty PA prototype to be used as a basis component to build an advanced digitally driven Doherty PA.
2. Development of digital compensation techniques for efficiency enhancement of analog Doherty PAs. This topic covers the study of critical issues impairing the operation of the Doherty PA and implementation of digital signal conditioning functions required to restore the optimal operation. This study will lead to the implementation of proof-of-concept prototypes demonstrating the benefits of DSP based approaches in boosting the performance of Doherty PAs.

3. Bandwidth enhancement of wireless Doherty PAs. This topic involves a comprehensive analysis of the frequency-dependent operation of the Doherty PA and mitigation of its bandwidth limitations using digital techniques. This research will lead to the implementation of a multistandard Doherty PA prototype having its optimal operation extended over a wide frequency bandwidth.

1.3 Contributions

The objectives of this work have been fully accomplished, and several contributions have been achieved. These are briefly described in this section, and more details are given throughout the thesis.

1. Design optimization of performance enhanced Doherty PAs. The effects of the series transmission lines, which are commonly used at the output of the carrier and peaking amplifiers, on the performance of the Doherty PA were studied; and, their usefulness in improving the efficiency, linearity and output power was thoroughly investigated. The main contribution is a systematic design methodology for performance optimization of Doherty
PAs. It has been shown that the output offset line of the carrier amplifier can be optimized to track the optimal impedance points that ensure the highest possible performance, in terms of efficiency, linearity and output power (or any possible combination of these). A noniterative load-pull based approach has also been proposed to accurately derive the electrical length of the optimal offset line of the carrier amplifier.

2. Efficiency enhancement of wireless Doherty PAs using digital techniques. Two digital compensation methodologies have been proposed: namely, adaptive phase alignment and adaptive power distribution. Also, dual-input Doherty PA architecture has been introduced to enable the implementation of the proposed techniques. The main contributions related to this objective are:

a. Digital adaptive phase alignment for performance enhancement of Doherty PAs. The difference in the operating conditions between the carrier and peaking amplifiers results in power-dependent phase variation throughout the output branches of the Doherty PA, especially for GaN based implementations, which greatly impact the overall performance of the PA. A new digital adaptive phase alignment mechanism has been proposed to entirely compensate for this problem.

b. Digital adaptive power distribution for enhanced efficiency. The difference in the modes of operation of the carrier and peaking amplifiers induces an amplitude imbalance throughout the output branches of the Doherty PA, as well as a significant waste of input
power when the peaking amplifier is not active. A new digital adaptive power distribution methodology has been proposed to efficiently distribute the available power between the input branches of the Doherty PA and correct for the amplitude imbalance problem.

c. Dual-input digitally driven Doherty amplifier architecture. This flexible architecture makes it possible to implement advanced signal processing algorithms that cannot be implemented in conventional single-input architectures. It was demonstrated that the dual-input digitally driven Doherty PA leads to substantial improvement in power efficiency compared to the conventional single-input fully analog Doherty PA architecture.

3. Bandwidth extension of wireless Doherty PAs using DSP based methods. The analysis of the frequency response of the Doherty PA pointed out that the bandwidth restrictions of the Doherty PA originate mainly from its output power combiner. A new frequency-selective compensation mechanism has been proposed to overcome this limitation. The main contributions related to this objective are:

a. Mitigation of bandwidth limitations using digital techniques. Digital control of the input power distribution and the phase variation between the carrier and peaking amplifiers prevent the efficiency degradation that naturally occurs as the frequency of operation deviates from the design frequency. An optimized frequency-dependent power
distribution scheme has been proposed, and its performance has been
experimentally assessed.

b. Digitally equalized Doherty PA architecture. This architecture
incorporates a baseband equalizer that has been implemented using
finite impulse response (FIR) filters to enable the implementation of
the optimal power distribution scheme at each frequency component of
wide bandwidth communication signals. The effectiveness of this
architecture for broadband and multistandard radios has been
experimentally verified. This demonstration was the first attempt of
the use of digital equalization within the Doherty structure.

1.4 Thesis Outline

The organization of this thesis is described in the following paragraphs.

In Chapter 2, a survey of the most important PA efficiency enhancement
techniques is presented. This covers Doherty, envelope tracking, linear amplification with
nonlinear components, and envelope elimination and restoration power amplification
systems. The operation principle of each of these techniques is discussed, along with its
main advantages and limitations. In particular, the Doherty PA topology is thoroughly
analyzed, since it is the core of this thesis work.

Chapter 3 presents the work performed on the design of enhanced Doherty PAs. A
generalized design methodology for the performance optimization of wireless Doherty
PAs is presented. A noniterative load-pull based technique is introduced and applied to
derive the optimal output matching elements of the carrier and peaking amplifiers for any
design criterion, in terms of efficiency, linearity and output power. For the experimental
validation, the implementation of a Doherty PA prototype using the proposed methodology for power efficiency is showcased.

Chapter 4 details the proposed dual-input digitally driven Doherty PA architecture. The problem of the power-dependent phase imbalance between the carrier and peaking branches is first studied. Second, the digital phase alignment mechanism introduced in this work is described. A dual-input Doherty PA running the proposed mechanism is then implemented; and, its ability to outperform its conventional counterpart is demonstrated.

In Chapter 5, a digital adaptive power distribution mechanism is proposed to jointly solve the problems of amplitude imbalance and input power waste in the peaking branch when the peaking amplifier is inactive. The efficiency enhancement capability of the proposed technique is first highlighted from a theoretical point of view based on a thorough analysis of its operational principle. It is then demonstrated practically within the dual-input architecture.

Chapter 6 is devoted to the proposed techniques for bandwidth extension of wireless Doherty PAs in the digital domain. In the first part, the optimal input power distribution profile between the carrier and peaking amplifiers is derived based on the analysis of the frequency response of the Doherty PA. The bandwidth extension potential of the proposed technique is then confirmed based on theoretical and practical results.

In Chapter 7, an adaptive baseband equalization methodology is proposed to enable the implementation of the optimal signal separation at each frequency component of the transmit signal. The effectiveness of the digitally equalized Doherty PA for high
efficiency power amplification of broadband and multistandard RF signals using Doherty PAs is then validated.

Chapter 8 presents the conclusions of this work and recommends related future research directions.
Chapter Two: Power Amplifier Efficiency Enhancement Techniques

2.1 Introduction

The challenge in wireless transmitters design is to achieve high power efficiency and high linearity. The linearity is required to meet the spectrum emission mask (i.e., reduce unwanted signals in the adjacent frequency channels) whereas efficiency is needed to minimize the energy waste (i.e., less direct current (DC) consumption and power dissipation) and to control the running costs of wireless communications infrastructures (i.e., lower energy cost and cooling requirements). However, these two key features are dominated by the performance of the power amplification block of the radio frequency (RF) front-end [1, 2]. Therefore, power amplifier (PA) topologies with efficiency enhancement and linearization techniques should be used to boost the efficiency and satisfy the linearity requirements of the intended wireless communication standard. As a linearization technique, the digital predistortion (DPD) is a robust and well-established solution for PA linearization [5, 6]. Therefore, the primary target of PA designers consists of developing PAs with the highest possible power efficiency, while maintaining their linearizability. Such a target can be achieved through the proper selection of the device technology, the PA’s class of operation and the power amplification architecture.

In this chapter, a brief overview of recent advances in semiconductor technologies is provided. An introduction to the various classes of PAs is then exposed. Afterwards, most important PA efficiency enhancement architectures are reviewed. The last section is dedicated to a detailed study of the Doherty PA topology.
2.2 Transistor Technology

The power efficiency of PAs, which is generally defined as the ratio of RF output power to DC power consumption, is primarily influenced by the device technology. An appropriate choice of the transistor technology should be considered during the design stage depending on type of application and the targeted performance.

Laterally diffused metal oxide semiconductor (LDMOS) based field effect transistors (FETs) have been widely considered as the indisputable technology for cellular base station and repeater PA systems, due to their value in terms of performance over cost ratio. Over the last decade, the performance of LDMOS transistors has been constantly improved, especially in terms of power efficiency and gain [12]. However, as the limits of operability of these devices are reached, the need for a semiconductor material that can fulfill the higher frequency and power requirements has recently emerged [12].

Meanwhile, gallium nitride (GaN) based high electron mobility transistors (HEMT) have begun to challenge LDMOS FETs and have gained a considerable interest for applications in wireless communications infrastructures [8]. As depicted in Table 2.1, this is mainly due to their superior material properties, in terms of current density, electron mobility, operating temperature, power capability, breakdown voltage, and frequency range, compared to the LDMOS technology. Moreover, the development costs of GaN devices have been considerably reduced over the last few years, making GaN technology presently considered as the technology of choice for high power PA implementations in cellular base stations. In fact, GaN HEMT technologies have already had a significant impact on various PA concepts, as outlined in Table 2.2 where a
A comparison is made between silicon (Si) LDMOS FETs and GaN on Silicon Carbide (SiC) HEMTs [8].

### Table 2.1 Material Properties of GaN HEMT and Si LDMOS Semiconductors

<table>
<thead>
<tr>
<th>Material</th>
<th>Current Density (mA/mm)</th>
<th>Electron Mobility (cm²/V.s)</th>
<th>Maximal Temperature (°C)</th>
<th>BFOM Ratio</th>
<th>Drain Voltage</th>
<th>Frequency Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si LDMOS</td>
<td>150</td>
<td>1300</td>
<td>300</td>
<td>1</td>
<td>28 V</td>
<td>&lt; 3GHz</td>
</tr>
<tr>
<td>GaN on SiC</td>
<td>1000</td>
<td>1500</td>
<td>700</td>
<td>24.6</td>
<td>48 V</td>
<td>&gt; 12 GHz</td>
</tr>
</tbody>
</table>

*BFOM: Baliga’s figure of merit for power transistor performance [8].

### Table 2.2 Impact of GaN on PA Architectures

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Si LDMOS</th>
<th>GaN on SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Mode</td>
<td>Low frequency, high parasitic capacitance</td>
<td>High frequency, low parasitic capacitance</td>
</tr>
<tr>
<td>Doherty</td>
<td>Low off-state impedance</td>
<td>High off-state impedance</td>
</tr>
<tr>
<td><em>LINC</em></td>
<td>Large nonlinear output capacitance</td>
<td>Small nonlinear output capacitance</td>
</tr>
<tr>
<td><strong>EER</strong></td>
<td>Poor amplitude-to-phase modulation conversion</td>
<td>Good amplitude-to-phase modulation conversion</td>
</tr>
</tbody>
</table>

*LinC: linear amplification with nonlinear components.

**EER: envelope elimination and restoration.
2.3 Power Amplifier Classes of Operation

The classes of operation of PAs form the foundation of the advanced power amplification architectures to be discussed in this chapter. Therefore, most significant aspects related to this topic are outlined in this section. The analysis performed herein assumes a FET; however, in principle, it is applicable to any other type of transistor with appropriate correspondence.

Figure 2.1 defines the parameters of the output current waveform to be used for the analysis. The conduction angle is denoted by $\alpha$, the quiescent current by $I_q$, the output drain current by $i_d$, and the amplitude of the maximal current by $I_{\text{max}}$ [2].

![Figure 2.1 Definition of the conduction angle of the PA](image-url)
In theory, the general expression of the output current illustrated in Figure 2.1 is given by [2]:

\[
i_d(\theta) = \begin{cases} 
  \frac{I_{\text{max}}}{1 - \cos(\alpha/2)} \cdot (\cos \theta - \cos(\theta/2)), & -\alpha/2 < \theta < \alpha/2 \\
  0, & -\pi < \theta \leq -\alpha/2; \alpha/2 \leq \theta \leq \pi 
\end{cases}
\]  

(2.1)

where \( \theta \) is the angular frequency.

Assuming a periodic wave shaping, the amplitude of the DC current \( I_{\text{dc}} \), of the fundamental \( I_1 \), and the harmonics \( I_n \) can be expressed based on Fourier decomposition as [13]:

\[
I_{\text{dc}} = \frac{I_{\text{max}}}{2\pi} \cdot \frac{2 \sin(\alpha/2) - \alpha \cos(\alpha/2)}{1 - \cos(\alpha/2)} 
\]  

(2.2)

\[
I_1 = \frac{I_{\text{max}}}{2\pi} \cdot \frac{\alpha - \sin \alpha}{1 - \cos(\alpha/2)} 
\]  

(2.3)

\[
I_n = \frac{I_{\text{max}}}{\pi(1 - \cos(\alpha/2))} \cdot \left[ \frac{\sin((n - 1) \cdot \alpha/2)}{n(n - 1)} - \frac{\sin((n + 1) \cdot \alpha/2)}{n(n + 1)} \right] 
\]  

(2.4)

Figure 2.2 illustrates the frequency components of the drain current as a function of the conduction angle \( \alpha \), which were calculated using (2.2), (2.3) and (2.4). It is noted that the reduction of \( \alpha \) leads to the creation of harmonic components in the output signal. The amplitude of these harmonics increases with the reduction of \( \alpha \), which degrades the linearity of the PA.
For a given $\alpha$, the maximal drain efficiency, $\eta_{\text{max}}$, has been demonstrated to be [2]:

$$
\eta_{\text{max}} = \frac{\alpha - \sin \alpha}{4 \sin(\alpha/2) - 2\alpha \cos(\alpha/2)}
$$

Figure 2.3 shows that the maximal drain efficiency $\eta_{\text{max}}$ increases with the reduction of $\alpha$. This trend is opposite to that observed in Figure 2.1 which infers that the linearity worsens when $\alpha$ decreases. These two opposite tendencies show that efficiency and linearity are two antagonists that cannot be achieved simultaneously.
Starting from the previously presented theory, four classes of operation have been established on the basis of the conduction angle [1, 2]:

- **Class A** \((\alpha = 2\pi, I_q = 0.5I_{\text{max}})\) is the most linear mode of operation. With a class A bias, a sine wave at the input results in a linearly amplified version at the output. However, there is a DC current constantly flowing through the transistor, even if there is no input signal, which limits the efficiency. Based on (2.4), the maximal drain efficiency of a class A PA is 50%.

- **Class B** \((\alpha = \pi, I_q = 0)\) allows for a significant efficiency increase given that the DC current consumption is 0 when no RF signal is driving the PA.
With a class B operation, the drain efficiency is improved to a theoretical maximum of 78.5% (the exact value is $\pi/4$ as inferred from (2.4)). However, with a class B bias, only half of the input waveform is amplified and the output waveform is distorted in a nonlinear way.

- Class AB ($\pi < \alpha < 2\pi, 0 < I_q < 0.5I_{\text{max}}$) is biased somewhere in-between class A and class B and represents a good trade-off between linearity and power efficiency.

- Class C ($0 < \alpha < \pi, I_q = 0$) is biased to be turned OFF more than half of the sine wave period. This gives rise to larger distortions than the class B PA but also to higher power efficiency (theoretically up to 100%). The gain of the amplifier, however, is lowered compared to the other classes of operation. Class C PAs are mainly used in advanced PA architectures (e.g., Doherty PA) and in power amplification of constant-envelope radios.

The previously described power amplification classes of operation refer to continuously driven (linear) PAs. This contrasts with switching mode PA classes for which the transistor operates as a switch with two discrete states (ON and OFF). Switching mode PAs encompass several classes including, class D, class E, class F and its inverse ($F^{-1}$) [14].

The operation of switching mode PAs is essentially based on terminating the device at the fundamental and harmonic frequencies, in order to produce voltage and current waveforms that do not overlap, resulting in no power dissipation in the device and a theoretical maximal efficiency of 100% [14]. Switching mode PAs are commonly used
within advanced power amplification architectures, especially in LINC and EER systems [1].

It is worth mentioning that, in addition to the semiconductor technology and the class of PA operation, the efficiency is greatly influenced by the power operating point. To consider this effect, the instantaneous drain efficiency, $\eta$ has been approximated by [1]:

$$\eta = \eta_{\text{max}} \cdot E = \eta_{\text{max}} \cdot \frac{\nu}{V_{\text{max}}}$$  (2.6)

where $E (0 \leq E \leq 1)$ is the normalized output voltage that is given by the ratio of the instantaneous RF voltage ($\nu$) to the maximal RF voltage ($V_{\text{max}}$) at the output of the PA. $E$ is equal to 1 at peak power level and 0 when no RF signal is driving the PA.

From (2.6), it is clear that the efficiency is maximal only at peak power drive; and, drops rapidly as soon as the instantaneous input power is decreased. Accordingly, all stand-alone PAs, regardless of their classes of operation, will fail to maintain satisfactory efficiency performance when driven with envelope-varying wireless communication signals, due to the high peak-to-average power ratio (PAPR) values of these signals. This stimulated the need for more appropriate alternatives.

### 2.4 Advanced Power Amplification Architectures

Many research efforts have been done to develop advanced power amplification architectures that are capable of providing high efficiency at large power back-off levels. These architectures can be categorized into two groups.

The first group consists of boosting the average efficiency of linear mode PAs, such as class AB PAs, by using drain modulation or load modulation techniques [15–19].
Envelope tracking (ET) systems and Doherty PAs are the most popular topologies that belong to this group.

In ET systems, the drain voltage of the RF PA is adapted to the instantaneous output power. For low output power, the supply voltage is reduced; and, for high power levels, it is increased through the action of a voltage modulator. In the ideal case, the RF PA is always driven near its maximum output power where it exhibits maximal efficiency [1, 2]. The critical component of the ET system is the voltage modulator which has to be very efficient and broadband [15, 16]. The delay adjustment between the envelope and RF signal paths is also crucial. A block diagram of ET based amplifier is depicted in Figure 2.4.

![Figure 2.4 Block diagram of ET based amplifier](image)

Load modulation techniques, on the other hand, are based on dynamically varying the load impedance presented to the PA according to the amplitude of the input signal to ensure the high efficiency operation [17–19]. In the case of Doherty PAs, the load presented to a class AB biased amplifier is dynamically changed through the impedance.
modulation triggered by the turn-on of a class C biased amplifier. This active load modulation mechanism allows both amplifiers to operate into optimal load impedance trajectories that maximize the efficiency according to the amplitude of the input signal [7, 17]. A block diagram of a Doherty PA is presented in Figure 2.5.

![Figure 2.5 Block diagram of a Doherty PA](image)

The second category of efficiency enhancement techniques consists of using highly nonlinear but energy efficient PAs, mainly switching mode types, within an appropriate system level architecture that restores the linearity. This category encompasses a number of topologies, including LINC and EER transmitters [20–24].

The LINC concept is based on the use of two switching mode based amplification branches, as presented in Figure 2.6. Its principle consists of dividing the highly varying envelope signal \( S(t) \) into two phase-modulated signals with a constant envelope, \( S_1(t) \) and \( S_2(t) \), as illustrated in Figure 2.7. The combination of these two signals after amplification ideally results in a linearly amplified version of the input signal along with high average efficiency operation [20–22]. The two signals, \( S_1(t) \) and \( S_2(t) \) are related to \( S(t) \) by [20]:

\[
S(t) = S_1(t) + S_2(t)
\]
\[
\begin{align*}
S(t) &= \cos(\phi(t)) \cdot \cos(\omega_0(t) + \theta(t)) \\
S_1(t) &= \frac{1}{2} \cos(\omega_0(t) + \theta(t) + \phi(t)) \\
S_2(t) &= \frac{1}{2} \cos(\omega_0(t) + \theta(t) - \phi(t))
\end{align*}
\] (2.7)

Figure 2.6 Block diagram of LINC based amplifier

Figure 2.7 Signal components separation in LINC technique
Maintaining high efficiency in the output combiner, however, is a challenging task for LINC systems, especially when an isolated output power combiner (e.g., Wilkinson type) is used. This is mainly due to the power dissipated in the isolation resistance when low power levels are generated from out-of-phase high power signals [21]. Conversely, the use of a nonisolated combiner (e.g., Chireix type) permits to improve the efficiency but at the cost of degraded linearity due to the interaction between the nonisolated branches [22].

In the EER technique, the amplitude- and phase modulated input signal is applied to highly efficient switching mode or saturated RF PA through the envelope and phase paths. A block diagram of an EER based PA is shown in Figure 2.8. The phase path incorporates a limiter that strips the signal from its amplitude, allowing the constant-amplitude phase modulated signal to be amplified efficiently by the RF PA [1, 2]. In the envelope path, the amplitude information is extracted using an envelope detector. This information is then used to modulate the supply voltage of the RF PA through a voltage modulator, which allows restoring the envelope to the amplified phase-modulated signal.

![Figure 2.8 Block diagram of EER based amplifier](image)

**Figure 2.8 Block diagram of EER based amplifier**
In theory, the efficiency of EER based PA is equal to the maximal efficiency of its RF PA over a wide dynamic range of power levels [1, 2]. The actual efficiency of EER PAs, however, is essentially impacted by the performance of the voltage modulator. In addition, it is essential to ensure a precise time alignment between envelope and phase paths to preserve the linearity [23, 24].

Figure 2.9 reports the theoretical drain efficiency, $\eta$, of ERR, LINC, Doherty and class B PAs as a function of the normalized output signal $E$. The theoretical expressions of $\eta$ for these PA topologies can be found in [1, 2, 7, 13, 22]. A typical probability density function (PDF) of an OFDM modulated signal is also included in Figure 2.9.

![Figure 2.9 Efficiency of EER, LINC, Doherty and class B PA versus normalized output voltage](image-url)
Based on Figure 2.9, it is clear that advanced PA architectures permit a significant increase in power efficiency at large back-off power levels where the probability of occurrences of the input signal is high, which justifies their convenience for power amplification in modern wireless communication systems. Among these topologies, Doherty PAs are extensively used in modern wireless communication infrastructures. Simple circuit configuration, low fabrication costs for mass production and proven linearizibility using DPD are the main reasons of the successful incursion of Doherty PAs in field-deployed cellular base stations [25–46].

In the next section, a comprehensive analysis of the operation of the Doherty PA is provided, a review of a number of critical challenges affecting its performance is reported, and a selection of state-of-the-art research advancements is exposed.

2.5 Doherty Amplifiers

2.5.1 Operation Principle of the Doherty PA

The circuit diagram of a Doherty PA is presented in Figure 2.10. It encompasses two parallel amplifiers, namely the carrier amplifier (operating in class AB) and the peaking amplifier (operating in class C), an input analog splitter, and a nonisolated output power combiner that consists of two transmission lines, with an electrical length of 90°. In Figure 2.10, the transmission line connected to the output load, \( Z_0 \), is commonly denominated as impedance transformer, whereas that having a characteristic impedance of \( Z_0 \) is designated as impedance transformer. Typically, the carrier and peaking amplifiers have identical device sizes and matching networks and are evenly driven. The gate bias of the peaking PA is chosen to control its turn ON region. This defines the
Doherty design parameter $\alpha$ ($0 \leq \alpha \leq 1$) that expresses the relative contribution, at full drive, of the carrier amplifier to the total output power of the Doherty PA.

![Figure 2.10 Circuit diagram of a Doherty PA](image)

The operation of the circuit can be analyzed in two modes: at low power mode where only the carrier amplifier is active; and, at high power mode where both carrier and peaking amplifiers are contributing to the output power of the Doherty PA.

At low input power levels, the peaking amplifier is turned OFF and its branch ideally presents an open circuit. As inferred from Figure 2.10, due to the action of the impedance inverter, the carrier amplifier will be operating into a load, $Z_C$, given by:

$$Z_C = \frac{(Z_0)^2}{\alpha Z_0} = \frac{1}{\alpha} \cdot Z_0$$

(2.7)

where $Z_0$ is the output load of the Doherty PA, which is usually equal to 50 $\Omega$.

The load impedance of the carrier amplifier remains unchanged as long as the peaking amplifier is still turned OFF. This causes the premature saturation of the carrier
amplifier at $20 \log_{10}(\alpha)$ dB back-off from the Doherty PA peak power level, which leads to an efficiency maximum at this power level [7].

As soon as the input power goes beyond the conduction threshold of the peaking amplifier, the latter starts contributing to the total output power of the Doherty PA. This creates an active load modulation mechanism; and, the load impedance of the carrier amplifier decreases gradually from its value given by (2.7) to $Z_0$, and that of the peaking amplifier, $Z_P$, drops rapidly from very large value (theoretically infinite, $\infty$) to $Z_0$. In this case, an efficiency maximum occurs at peak power drive [7].

The theoretical efficiency of a Doherty PA, the carrier and peaking amplifiers of which are operating in class B, is given by [7]:

$$
\eta = \begin{cases} 
\pi \cdot \frac{1}{\alpha} \cdot 10^{-20} \cdot \frac{\text{OPBO}}{\alpha}, & \text{OPBO} \leq 20 \log_{10}(\alpha) \\
\pi \cdot \left( \frac{10^{-10} \cdot \frac{\text{OPBO}}{1 + \alpha} \cdot 10^{-20}}{\alpha} \right), & 20 \log_{10}(\alpha) \leq \text{OPBO} \leq 0
\end{cases}
$$

(2.8)

where OPBO refers to the back-off of the actual output power of the Doherty PA from its saturation power.

Figure 2.11 depicts the simulated efficiency as function of OPBO for various values of $\alpha$. It is clear that the active load modulation mechanism allows to maintain relatively high efficiency over the power range spanning from $P_{\text{sat,dB}} = 20 \log_{10}(\alpha)$ to $P_{\text{sat,dB}}$, where $P_{\text{sat,dB}}$ is the output saturation power, expressed in dB, of the Doherty PA. Furthermore, it can be seen that the choice of $\alpha$ shapes the efficiency curve of the Doherty PA. A typical choice for the Doherty design parameter is $\alpha = 0.5$, which, by
definition, means that the carrier and peaking amplifiers should contribute equally to the peak output power. This specific type is commonly denoted by symmetrical Doherty PA.

![Theoretical efficiency of the Doherty PA](image)

**Figure 2.11 Theoretical efficiency of the Doherty PA**

From now on, all materials to be presented in this thesis will be focused on the symmetrical Doherty PA which will be oftentimes denoted simply by Doherty PA.

2.5.2 Critical Challenges and Review of Existing Methodologies

Actual implementations of Doherty PAs are often prone to several limitations that are related to nonideal behavior of the active devices and inherent imperfections in the analog building blocks of the PA, greatly impacting its performance [31–46].
2.5.2.1 Gain Imbalance between Carrier and Peaking Amplifiers

The difference in classes of operation of the carrier and peaking amplifiers results in gain imbalance between the two branches of the Doherty PA due to the lower gain of the class C biased peaking PA. As such, the maximal output power of the peaking amplifier is lower than that of the carrier amplifier, which translates into an imperfect load modulation mechanism and degraded efficiency at peak power [31–34].

Several solutions were proposed to tackle the problem of amplitude imbalance between the carrier and peaking amplifier. Uneven power drive where the peaking amplifier receives more input power compared to the carrier amplifier [32], asymmetrical Doherty PA design where the transistor used in the peaking amplifier is bigger than that of the carrier amplifier [33] and gate bias adaptation where the gate bias voltage of the peaking amplifier is modulated to upgrade it mode of operation from class C (at the turn-on point) to class AB (at peak power) [34] are the main used methods. While the first approach significantly decreases the gain and the average efficiency of the Doherty PA, the second is not always feasible especially for high output power devices, and the third needs external voltage control circuitries and precise time alignment between the envelope and RF paths, which increases the complexity of implementation.

2.5.2.2 Power-Dependent Phase Imbalance between Carrier and Peaking Amplifiers

The incursion of the highly efficient and increasingly affordable GaN devices has given rise to additional challenges for Doherty PA design, especially in terms of power-dependent phase variation through the output combining branches of GaN Doherty PAs. Indeed, the difference in bias conditions between the carrier and peaking amplifiers results in power-dependent phase misalignment between the output branches of GaN
Doherty PAs, which causes severe loss of RF output power and degraded power efficiency [35–38].

This problem has been partially tackled in an analog way by inserting a series transmission line at the input of the phase lagging path [35]. This suboptimal solution permits to align the phases of the output RF signals of carrier and peaking amplifiers but only at a single power level.

2.5.2.3 Output Power Leakage into the Peaking Branch

Due to the parasitic components of the device, the output impedance of the peaking path at low input power levels does not exhibit an ideal open circuit. As a result, a portion of the output power from the carrier amplifier leaks into the peaking branch when the peaking amplifier is still inactive, causing RF output power loss and average efficiency degradation. To solve this problem, a series transmission line is usually used in conjunction with the output matching network of the peaking amplifier to ensure the quasi open-circuit condition and, thus, alleviate the power leakage problem [39].

2.5.2.4 Input Power Waste into the Peaking Branch

Another problem related to power losses within the symmetrical Doherty PA is that a lot of input power drive is wasted into the peaking branch when the peaking amplifier is still turned OFF [31, 40].

A technique based on the use of a customized analog power divider, denoted by extended-resonance power divider, has been introduced in [41] to distribute the input power between the carrier and peaking amplifiers in an adaptive manner. The implementation of such a power divider, however, entirely relies on the nonlinear input impedance of the peaking amplifier, which greatly compromises its flexibility.
2.5.2.5 Narrow Bandwidth Limitations

A well-known weakness of the Doherty architecture is the narrow bandwidth performance, which compromises its convenience for multisandard and broadband applications. The fractional bandwidth of typical Doherty PA implementations is often lower than 10% [42]. This restriction is mainly attributed to the frequency response of the quarter-wavelength transmission lines of the output combiner and the frequency-dependent behaviour of the active devices [42–46].

In this context, a variety of solutions have been proposed in an effort to improve the bandwidth efficiency of wireless Doherty PAs in an analog way. Quasi-lumped transmission line impedance inverter [42], varactor based Doherty combiner [43], ladder-type multi-section based output Doherty network [44], stepped transmission line based Doherty combiner [45] and Doherty PA design via real frequency technique [46] are some of these methods.

Although effective in improving the bandwidth, these techniques have constrained capabilities as they are based on analog components and cannot entirely correct for frequency- and bias-dependant impairments that perturb the active load modulation mechanism.

2.6 Conclusions

In this chapter, a thorough review of power amplification systems that can be considered for base station applications was presented. An analysis spanning from device technology to single-ended PAs and advanced system-level power amplification architectures was carried out. According to this study, it appears that, for the short- and mid-terms, GaN based Doherty PAs are the most promising solution for PA systems in
wireless communication infrastructures. However, Doherty PAs are still facing several limitations that need to be addressed.

In the next chapter, a systematic methodology for Doherty PA design is proposed and applied to design a highly efficient Doherty PA for Worldwide Interoperability for Microwave Access (WiMAX) applications. This prototype will be used to develop the digitally driven Doherty PA proposed in this thesis work.
Chapter Three: Systematic Doherty Power Amplifier Design Methodology

3.1 Introduction

To achieve optimal performance when designing Doherty power amplifiers (PAs), special attention must be given to the output matching elements of the carrier and peaking amplifiers. The optimization procedure of the output matching components of the peaking amplifier is well known and requires the use of an offset line in series with the output matching network in order to prevent the loss of output power at back-off [25, 39]. The matching elements of the carrier amplifier, on the other hand, should be optimized to track the impedance points that guarantee the best possible performance at both low and high power regions [47, 48].

This chapter investigates the design considerations that allow for addressing this latter matter; and, proposes a new load-pull based procedure that permits the optimization of the output matching elements of the carrier amplifier for enhanced performance, in terms of efficiency, power gain and linearity [48]. The effectiveness of the proposed approach is then confirmed through simulation results and the practical implementation of a Doherty PA prototype that is optimized for power efficiency.

3.2 Systematic Design Methodology of Enhanced Doherty PAs

3.2.1 Doherty PA Design Considerations

The design of Doherty PAs for optimal performance should consider the operating conditions at high and low power regions.

At peak power condition, the carrier and peaking amplifiers are ideally operating into 50 Ω. The design of the single-ended carrier and peaking amplifiers consists of
determining the appropriate source and load impedances and designing the input and output matching networks that are required to achieve the targeted performance in terms of power efficiency or output power. The design procedure is well-established and a load-pull\(^1\) based approach is often adopted.

At the low power region, the design considerations of the carrier and peaking amplifiers are different. First, the peaking branch should present an open circuit to prevent the leak of output power from the carrier amplifier into the peaking path when the peaking amplifier is still turned OFF. As depicted in Figure 3.1, this problem can be surmounted by inserting an offset line (\(\theta_P\)) following the peaking amplifier to ensure the quasi open-circuit condition.

![Figure 3.1 Prevention of power leakage into the peaking path](image)

\(^1\) Load-pull is a comprehensive look at the device’s response to the variation of the load impedance, plotting the performance results with contour lines.
Second, the performance of the carrier amplifier at back-off (i.e., when the peaking amplifier is still inactive) should be optimized as it will dominate the overall performance of the Doherty PA when driven with modulated signals with high peak-to-average power ratios (PAPRs) [47, 48]. As graphically illustrated in Figure 3.2, this can be achieved by means of a series offset line ($\theta_C$) that converts the 100 $\Omega$ seen by the carrier amplifier at back-off to an optimal matching point, $Z_{Opt,BO}$, that gives the best possible performance around the turn-on point of the peaking device.

![Diagram of Carrier Output Path, Z_{Opt,BO}, 50 $\Omega$, 100 $\Omega$, Load-pull Reference Plane, Device Under Test](image)

**Figure 3.2 Definition of optimal back-off matching point and load-pull plane**

To determine $Z_{Opt,BO}$, load-pull is performed on the carrier device at the input power drive corresponding to the turn-on of the peaking device. The load-pull is performed purposely at this lower level to take into account the moving location of the load-pull contours depending on the input power and, thus, increase the design accuracy. Given that the impedance observed at the Doherty combiner plane is known (100 $\Omega$ before optimization), it is more appropriate to solve the optimization problem at this plane. Accordingly, the load-pull contours are de-embedded such that the previously designed output matching network is part of the device under test as shown in Figure 3.2.
Figure 3.3 presents the simulated load-pull contours for constant drain efficiency, output power and third order intermodulations (IMD3), which are de-embedded at the output matching network of a stand-alone carrier amplifier that is implemented using a 10-Watt gallium nitride (GaN) packaged transistor (CGH40010 from Cree Inc.). It can be seen that, depending on the location of the contours, the Smith chart can be mapped into three regions where the performance can be optimized separately. Although the traces reported in Figure 3.3 are device-dependent, the same trend is expected to take place for any other transistor given that maximal efficiency, best linearity, and peak output power are usually achieved with significantly different load impedances.

![Figure 3.3 Back-off load-pull contours of the carrier device for efficiency (red), output power (blue), and IMD3 (green)](image-url)
The optimal impedance \( Z_{\text{Opt,BO}} \) is then derived directly in accordance with the back-off load-pull contours. Indeed, \( Z_{\text{Opt,BO}} \) is given by the intersection point of the circular path starting from 100 \( \Omega \) and the contour having the highest performance, as graphically illustrated in Figure 3.3, where each star indicates the optimal impedance for a given design criterion.

Practically, \( Z_{\text{Opt,BO}} \) is reached by inserting an offset line (\( \theta_C \)) with a characteristic impedance of 50 \( \Omega \) at the output of the carrier amplifier. Considering that the latter ideally operates into 50 \( \Omega \) at peak power, it is possible to boost back-off performance as proposed without altering the matching conditions at peak power.

The analytical expression of \( Z_{\text{Opt,BO}} \) is given by [48]:

\[
Z_{\text{Opt,BO}} = 50 \cdot \frac{2 + j \cdot \tan \theta_C}{1 + 2j \cdot \tan \theta_C}
\]

where \( \theta_C \) refers to the electrical length of the offset line inserted at the output branch of the carrier amplifier.

The offset line of the carrier amplifier (\( \theta_C \)) is independent from that of the peaking amplifier (\( \theta_P \)). Since in most general case, the two lines may not be identical, the delay difference \( |\theta_C - \theta_P| \) needs to be added at the input of the lagging path to align the delay through the two branches of the Doherty PA. Figure 3.4 shows the circuit diagram of a Doherty PA, the performance of which is optimized using offset lines in the carrier and peaking branches.
3.2.2 Generic Doherty PA design Approach

The design steps are summarized in the flow chart depicted in Figure 3.5. The first two steps are devoted to circuit level design of the single-ended carrier and peaking amplifiers. The next three steps focus on the optimization of Doherty PA performance at back-off. First, the offset line at the output path of the peaking amplifier is adjusted to ensure the quasi-open circuit condition. The output offset line of the carrier amplifier is then optimized to maximize the efficiency, the gain or the linearity around the turn-on point of the peaking device. The final step is the delay alignment between the two branches of the Doherty PA. This is achieved by inserting the delay difference between the two branches at the input of the delay lagging path.
3.3 Simulation Results

To validate the proposed design methodology, three Doherty PAs were implemented in Advanced Design System (ADS) software. In the first circuit, the optimal load impedance $Z_{\text{opt,BO}}$ is selected to boost the efficiency. In the second configuration, $Z_{\text{opt,BO}}$ is optimized to increase the gain. In the third design, $Z_{\text{opt,BO}}$ is optimized to improve the linearity. The output matching networks of the single-ended carrier and peaking amplifiers are designed to maximize the efficiency at peak power drive. All
Doherty PAs are identical except for the length of the output offset line in the carrier path and the corresponding input offset line used for delay alignment between the two branches of the Doherty PA. The simulations are carried out using the large-signal nonlinear model of the CGH40010 device, which was provided by the device manufacturer, Cree Inc.

To obtain $Z_{\text{Opt,BO}}$ for each design criterion, load-pull is performed on the carrier device at an input power of 22 dBm, which corresponds to 6 dB back-off from the maximal input power of the CGH40010 device. The bias conditions for class AB operation are drain voltage, $V_{DS} = 28$ V and quiescent drain current, $I_{DQ} = 200$ mA. The simulated load-pull contours de-embedded at the output matching network plane of the carrier amplifier are those reported in Figure 3.3.

Figure 3.6 shows the simulated drain efficiency and gain of the three Doherty PA circuits driven with continuous wave (CW) signal at the center frequency of 2.425 GHz. The reported traces confirm that the optimization methodology allows for an improved design of Doherty PAs. Indeed, the design sought for efficiency permitted a significant improvement in drain efficiency at back-off. A drain efficiency of 53% is obtained around 7 dB output power back-off (OPBO), which presents an improvement of 9% compared to the other two Doherty PAs.

Besides, the Doherty PA that is designed for gain allowed for up to 2 dB improvement in gain, compared to the most efficient Doherty PA. However, the improvement in gain is limited to 0.2 dB relatively to the prototype optimized for linearity. Referring to Figure 3.3, this can be explained by the proximity of gain and linearity areas in the Smith chart.
The IMD3 characteristics of the designed Doherty PAs are reported in Figure 3.7. The results were obtained using two-tone signal with 1 MHz spacing around the center frequency. As expected, the Doherty PA, of which $Z_{\text{Opt,BO}}$ is optimized for linearity, exhibits the lowest intermodulation distortions with an improvement of 10 dB compared to the most efficient configuration. It is noteworthy, on the other hand, that the circuit optimized for gain has better performance in terms of linearity compared to the circuit sought for efficiency. This result is also due to the proximity of gain and linearity regions, as reported in Figure 3.3. Accordingly, it can be inferred that this design
methodology can be used to optimize the performance of Doherty PAs by trading-off two features in conformity with the location of their load-pull contours in the Smith chart.

![Graph showing IMD3 and OPBO for different optimizations](image)

**Figure 3.7** Simulated lower (L) and upper (U) IMD3s of the Doherty PAs using a two-tone signal

### 3.4 Design of Doherty PA Prototype Sought for Power Efficiency

In this section, the proposed design methodology is applied to the implementation of a Doherty PA prototype that is optimized for power efficiency.

At first, optimal source and load terminations required to maximize the efficiency at peak power are determined using load-pull setup. In addition, the second and third
harmonics at the load side were tuned with the purpose of reinjecting them with appropriate phases to boost the power efficiency [49]. The carrier and peaking amplifiers were designed using identical input and output matching networks and biased in class AB ($V_{DS} = 28$ V, $I_{DQ} = 200$ mA) and class C ($V_{DS} = 28$ V, $I_{DQ} = 0$) conditions, respectively. The measured gain and power-added efficiency (PAE) of the single-ended amplifiers are shown in Figure 3.8.

![Figure 3.8 Measured PAE and gain of the carrier and peaking amplifiers using a CW signal](image)

In the next step, the output reflection coefficient ($S_{22}$) of the peaking amplifier is measured under different class C bias conditions. The electrical length ($\theta_P$) of the offset
line of the peaking path is then adjusted to transform the complex output impedance of the peaking amplifier into highly resistive impedance as illustrated in Figure 3.9.

![Figure 3.9 Optimization of the offset line of the peaking amplifier for open circuit condition](image)

Afterwards, a second load-pull is performed in order to determine the optimal matching point for efficiency. Figure 3.10 presents the PAE contours transformed at the output of the load matching network of the carrier amplifier. Based on the proposed approach, $Z_{\text{Opt,BO}}$ is given by the clockwise circular motion starting from 100 $\Omega$ and
crossing the contour with the highest efficiency. As graphically illustrated in Figure 3.10, a maximal PAE of 53% can be obtained around the turn-on point by using an offset line in the carrier path having an electrical length equal to 21°.

Figure 3.10 Optimization of the offset line of the carrier amplifier for power efficiency

The Doherty PA is implemented on Rogers RT5870 laminate (dielectric constant, $\varepsilon_r = 2.33$; and, substrate height, $h = 20$ mil) using the CGH40010 GaN device. The prototype of the fabricated Doherty PA is shown in Figure 3.11.
Figure 3.11 Photograph of the fabricated Doherty PA sought for power efficiency

Figure 3.12 shows the measured gain and PAE of the Doherty PA when driven with a CW signal at the center frequency 2.425 GHz. The measured output saturation power and peak PAE of the PA are 43.6 dBm and 61%, respectively. At the output power of 36.8 dBm (i.e., 6.8 dB OPBO), a peak PAE of 52% is measured. Throughout an OPBO range of 8 dB, the Doherty PA demonstrated a PAE higher than 40%.

Looking into Figure 3.8, however, it can be noted that the maximal efficiency of the stand-alone carrier and peaking amplifiers is in excess of 70% whereas that of the Doherty PA is just above 60%. Moreover, the efficiency curve of the Doherty PA shows a drop at the medium power region. These results suggest that a deficient load modulation behavior has occurred.
Figure 3.12 Measured PAE and gain of the Doherty PA using a CW signal

The performance of the fabricated Doherty PA is also assessed based on a 5 MHz bandwidth one-carrier downlink Worldwide Interoperability for Microwave Access (WiMAX) signal with a PAPR of 7 dB. As depicted in Figure 3.13, a maximal average efficiency of 50% is measured at an average output power of 36.8 dBm. The corresponding adjacent channel power ratio (ACPR) at 5 MHz offset is $-23$ dBC.
In order to meet the linearity requirements of the WiMAX standard, the designed Doherty PA was linearized using digital predistortion (DPD). As shown in Figure 3.14, the spectrum emission conditions were successfully satisfied after DPD is applied.
Figure 3.14 Measured output spectra before and after DPD

3.5 Conclusion

In this chapter, a systematic performance optimization methodology for the design of enhanced Doherty PAs has been proposed. It was shown that the use of offset lines at the output branches of the carrier and peaking amplifiers is indispensable for optimizing the operation of Doherty PAs. In this approach, the offset lines at the output of the carrier and peaking amplifiers have been determined directly based on design criteria and independently of each other.

The proposed approach was applied to implement three Doherty PA circuits that were optimized for power efficiency, gain, and linearity. For each configuration,
simulation results demonstrated a considerable improvement in the targeted performance for each design. For the experimental validation, a GaN Doherty PA sought for power efficiency was experimentally implemented. Measurement results showed that the fabricated PA has excellent power efficiency, especially at back-off. The achieved efficiency at the high power region, however, was below the expectations due to impaired load modulation mechanism.

In the next chapter, the quasi-ideal load modulation behavior of the fabricated Doherty PA will be restored; and, its performance will be significantly improved through direct access to and digital preprocessing of the input signals of the carrier and peaking amplifiers.
Chapter Four: Dual-Input Digitally Driven Doherty Power Amplifier Architecture

4.1 Introduction

Several power amplification architectures have been proposed to improve the average efficiency of wireless radio frequency (RF) transmitters [1]. These architectures are either based on using Doherty and envelope tracking (ET) power amplifiers (PAs) along with a linearization technique (e.g., digital predistortion (DPD)); or, switching mode PAs within an appropriate system-level architecture, such as linear amplification using nonlinear components (LINC) and envelope elimination and restoration (EER).

Although the Doherty PA is commonly used in base station wireless transmitters, it suffers from some limitations that restrict the achievable power efficiency. One major problem is the power-dependent phase imbalance between the output branches of the carrier and peaking amplifiers, which is very prominent in gallium nitride (GaN) based implementations [35–38]. Due to its power- and bias-dependent nature, this problem cannot be completely surmounted using analog based approaches (e.g., offset lines [35]).

In this chapter, the amplitude-dependent phase distortion (AM/PM) response of GaN based PAs is examined. Second, the detrimental effects of the power-dependent phase variation through the carrier and peaking branches are analyzed. The dual-input digitally driven Doherty PA with adaptive phase alignment mechanism [50] is then proposed to compensate for the phase imbalance problem. Afterwards, the practical implementation of the proposed architecture is discussed and the measured performance of the dual-input digitally driven Doherty PA is benchmarked against that of the fully analog single-input Doherty PA.
4.2 Amplitude-Dependent Phase Distortion Response of Class AB and Class C GaN Biased PAs

In this section, the AM/PM responses of two GaN PA prototypes are examined. The aim is to characterize the AM/PM behaviour in class AB and class C modes and investigate its impacts on the performance of GaN Doherty PAs.

The first PA prototype was implemented using 10-Watt CGH40010 GaN device from Cree Inc. and operated at 2.425 GHz. This same PA has been used to design the carrier and peaking amplifiers of the Doherty PA prototype that has been implemented in the previous chapter. The class AB bias conditions are gate voltage, $V_{GS} = -3.1$ V, drain voltage, $V_{DS} = 28$ V, and drain quiescent current, $I_{DQ} = 200$ mA. The bias conditions for class C operation are $V_{GS} = -5.5$ V, $V_{DS} = 28$ V, and $I_{DQ} = 0$.

The second GaN PA prototype was designed to operate at 1 GHz using 10-Watt EGN010MK transistor from Eudyna Inc. For this PA, the class AB bias conditions are $V_{GS} = -0.85$ V, $V_{DS} = 41$ V, and $I_{DQ} = 200$ mA. The bias settings for the class C mode are $V_{GS} = -2.6$ V, $V_{DS} = 41$ V and $I_{DQ} = 0$.

The measurements are performed using a 5 MHz bandwidth one carrier worldwide interoperability for microwave access (WiMAX) signal having a peak-to-average-power-ratio (PAPR) of 7 dB. The AM/PM responses of the PA prototypes under test are shown in Figure 4.1. The phase variation under class AB bias is almost constant versus input power, whereas that under class C bias is highly sensitive to the input power drive. The nonlinear AM/PM response observed for the class C biased PAs can be attributed to a strong variation of the intrinsic capacitive elements of the device after the transition from the OFF state to the ON state.
Figure 4.1 AM/PM responses (a) Cree device based PA; (b) Eudyna device based PA
Since the carrier and peaking amplifiers operate in class AB and class C, respectively, a phase misalignment will occur at the Doherty combiner; and, their respective output signals will combine with a phase offset that varies as function of the input power.

4.3 Performance Analysis of GaN Doherty PAs Exhibiting Power-Dependent Phase Imbalance

This section presents the issues related to the efficiency performance of GaN Doherty PAs exhibiting power-dependent phase imbalance. The GaN Doherty PA that was optimized for power efficiency and implemented in Advanced Design System (ADS) software, in the previous chapter, is considered for the analysis. Furthermore, this circuit will be used as a design reference to benchmark the simulated performance of the dual-input digitally driven architecture introduced in the next section. The simulations are carried out using the large-signal nonlinear model of the CGH40010 device.

The simulated phase variations through the carrier and peaking paths as function of the input power \( P_{\text{in}} \) are reported in Figure 4.2. The AM/PM response of the carrier path with the class AB bias \( V_{\text{DS}} = 28 \text{ V}, I_{\text{DQ}} = 200 \text{ mA} \) is found to be quasi-constant versus input power. The phase fluctuation through the peaking path, on the other hand, is more prominent. The phase discrepancy varies between 100° at \( P_{\text{in}} = 24 \text{ dBm} \) (i.e., turn-on point of the peaking device) and 50° at \( P_{\text{in}} = 30 \text{ dBm} \) (i.e., peak input power). These trends are in good agreement with those observed in measurements, as inferred from Figure 4.1(a).

The phase misalignment introduces a dynamic phase offset between the output signal of the carrier amplifier and that of the peaking amplifier at the junction point of the
Doherty combining network, which translates into an improper load modulation mechanism and output power loss; consequently, degraded efficiency.

Figure 4.2 Simulated phase variation through the carrier and peaking amplifiers

In what follows, an analytical formulation is derived to quantify the performance degradation caused by the power-dependent phase misalignment through the output branches of the Doherty PA. The analysis is restricted to the medium and high power regions, since the peaking amplifier is turned OFF at low input power levels.

Figure 4.3(a) shows the equivalent circuit diagram that is commonly used to analyze the efficiency of and load modulation in Doherty PAs [25, 32, 33, 42, 44]. It is
assumed that the magnitude of each current source is linearly proportional to the input drive voltage ($v_{in}$) and terminated with ideal harmonic short circuits. As such, the efficiency and the output power can be assessed using only the fundamental and direct current (DC) components [32, 33, 42, 44]. Furthermore, in order to identify only the impacts of the phase misalignment problem on the overall performance, the analysis is carried out assuming that the maximum current level ($I_1$) of the carrier and peaking amplifiers is the same at the maximal input voltage ($V_{in,max}$), as shown in Figure 4.3(b).

![Figure 4.3 (a) Equivalent circuit diagram of the Doherty PA; (b) fundamental currents of carrier and peaking sources versus input voltage](image-url)
Based on Figure 4.3, the currents from the carrier and peaking amplifiers at the Doherty junction point, $L$, can be written as [50]:

\[ I_C(v_{in}) = \frac{v_{in}}{V_{in,max}} \cdot I_1 \cdot e^{j\phi_C(v_{in})} \]  \hspace{1cm} (4.1)

\[ I_P(v_{in}) = \left( \frac{2v_{in}}{V_{in,max}} - 1 \right) \cdot I_1 \cdot e^{j\phi_P(v_{in})} \]  \hspace{1cm} (4.2)

where $\phi_C(v_{in})$ and $\phi_P(v_{in})$ are the instantaneous phases of the carrier and peaking currents at the input drive voltage ($v_{in}$) between ($V_{in,max}/2$) and ($V_{in,max}$), respectively.

From Figure 4.3(a), the RF output power of the Doherty PA is given by:

\[ P_{RF}(v_{in}) = \frac{Z_0}{4} \cdot |I_L(v_{in})|^2 \]  \hspace{1cm} (4.3)

where $Z_0$ is the optimal load of the carrier and peaking amplifiers, which is typically equal to 50 $\Omega$. $I_L$ is the total current flowing through the common load at the junction point of the Doherty network.

For a given input drive voltage ($v_{in}$) between ($V_{in,max}/2$) and ($V_{in,max}$), let $\delta \phi(v_{in})$ denote the instantaneous phase difference between the peaking and carrier currents at the junction point, $L$. Using the geometrical method demonstrated in Figure 4.4, the total current flowing through the common load can be written as:

\[ |I_L(v_{in})|^2 = |I_C(v_{in})|^2 + |I_P(v_{in})|^2 + 2 \cdot |I_C(v_{in})| \cdot |I_P(v_{in})| \cdot \cos \delta \phi(v_{in}) \]  \hspace{1cm} (4.4)
Figure 4.4 Addition of two out-of-phase vectors

The instantaneous Doherty PA’s relative output power degradation, due to the phase misalignment between the carrier and peaking branches, can be defined as [50]:

$$\Delta_{P_{RF}}(v_{in}) = 1 - \frac{P_{RF}(v_{in})}{P_{RF}(v_{in})|_{\delta\phi(v_{in})=0^\circ}}$$  \hfill (4.5)

Using (4.1)–(4.4), the output power degradation defined in (4.5) can be expressed by:

$$\Delta_{P_{RF}}(v_{in}) = \frac{2v_{in}}{V_{in,\text{max}}} \cdot \left( \frac{2v_{in}}{V_{in,\text{max}}} - 1 \right) \cdot (1 - \cos \delta\phi(v_{in}))$$  \hfill (4.6)

Figure 4.5 shows the simulated results of the relative output power degradation due to phase imbalance through Doherty PA output branches, which is obtained using (4.6). One can deduce that, after the peaking amplifier is turned ON, the phase
misalignment between the two branches inevitably leads to a severe drop in the output power, due to the destructive summation of the out-of-phase current vectors.

Figure 4.5 Simulated output power degradation due to phase imbalance problem

Figure 4.6 shows the simulated results of the output power degradation for the phase imbalance conditions reported in Figure 4.2. This result confirms the detrimental effect of the phase discrepancy problem on the output RF power of the Doherty PA. The degradation can be as high as 40% after the peaking amplifier is turned ON. The degradation is less severe at peak power drive because the phase difference tends to reduce towards the saturation. Also, it is worth mentioning that it is assumed, in the simulation, that the peaking amplifier is still in turned OFF at the input drive voltage ($V_{in,max}/2$); consequently, there is no output power degradation at this power level.
Figure 4.6 Simulated output power degradation based on the phase imbalance conditions reported in Figure 4.2

Based on Figure 4.3(a), (4.1) and (4.2), the expression of the carrier impedance, \( Z_C \), and that of the peaking impedance, \( Z_P \), is derived as follows:

\[
I_C(v_{\text{in}}) = \frac{Z_0^2}{2} \cdot \left[ 1 + \frac{I_P(v_{\text{in}})}{I_C(v_{\text{in}})} \right] = \frac{2Z_0}{1 + \left( 2 - \frac{V_{\text{in,max}}}{v_{\text{in}}} \right) \cdot e^{j\phi(v_{\text{in}})}} \quad (4.7)
\]

\[
Z_P(v_{\text{in}}) = \frac{Z_0}{2} \left[ 1 + \frac{I_C(v_{\text{in}})}{I_P(v_{\text{in}})} \right] = \frac{Z_0}{2} \cdot \left[ 1 + \frac{1}{\left( 2 - \frac{V_{\text{in,max}}}{v_{\text{in}}} \right)} \cdot e^{-j\phi(v_{\text{in}})} \right] \quad (4.8)
\]
Figure 4.7 shows the simulation results of the variations of $Z_C$ and $Z_P$ versus input power with $Z_0 = 50 \, \Omega$, based on the phase imbalance conditions reported in Figure 4.2. These results reveal that, even though the amplitude of $I_P$ and $I_C$ are equal at peak power, the correct load modulation of $Z_C$ (from 100 to 50 $\Omega$) and that of $Z_P$ (from very high impedance to 50 $\Omega$) cannot take place. The values of $Z_C$ and $Z_P$ at peak power are complex and different from the optimal 50 $\Omega$ impedance. Accordingly, the carrier and peaking amplifiers cannot reach their full capabilities, in terms of efficiency and output power, which compromises the overall performance of the Doherty PA.

Figure 4.7 Active load modulation in presence of phase imbalance
4.4 Dual-Input Doherty PA with Digital Adaptive Phase Alignment Mechanism

To minimize the adverse effects of the dynamic phase misalignment problem, the dual-input digitally driven Doherty PA architecture is proposed [50]. In this architecture, the input digital signal \((I/Q)_\text{in}\) is digitally preprocessed to generate two separate RF signals \((RF_{\text{Carrier}})\) and \((RF_{\text{Peaking}})\) that are supplied to each branch of the Doherty PA in order to compensate for the phase misalignment at the Doherty junction point \((L)\). The block diagram of the dual-input Doherty PA with digital adaptive phase alignment mechanism is shown in Figure 4.8.

![Block Diagram of Dual-Input Doherty PA with Digital Adaptive Phase Alignment](image)

**Figure 4.8 Dual-input Doherty PA with digital adaptive phase alignment**

Starting from the reference circuit that has been implemented in ADS, the dynamic phase offset is adjusted using a power-indexed look-up table (LUT) to correct for the phase disparity at all power levels, where both the carrier and peaking devices are active. As a result, the phase difference between the branches of the Doherty PA (shown in Figure 4.2) is reduced to 0° over the input power range spanning from the turn-on of the peaking device until the saturation of the Doherty PA.
Figure 4.9 presents the simulated results of the load modulation of the Doherty PA. The active load modulation mechanism is significantly improved with the adaptive phase alignment. Indeed, load impedance $Z_C$ is modulated from 100 Ω to nearly 50 Ω as the input power increases. Likewise, load impedance $Z_P$ increases gradually from a very high value to about 50 Ω. Since the phase imbalance is canceled, $Z_C$ and $Z_P$ remain purely real while converging towards 50 Ω, which suggests a more appropriate Doherty behaviour. It is noteworthy that the ideal load modulation mechanism is not strictly fulfilled since $Z_C$ and $Z_P$ did not fully converge to 50 Ω. The reason is that the output amplitudes of the carrier and peaking amplifiers at full power drive are not equal due to the lower gain of the class C biased peaking amplifier.

![Load modulation of the Doherty PA, with and without adaptive phase alignment](image)
Figure 4.10 shows the simulated output power of the Doherty PA, with and without adaptive phase alignment. As expected, by enforcing the constructive phase summation of the output signals at all times, the power losses are considerably reduced, which manifestly results in an increased total output power. In addition, it can be seen that the relative improvement in output power is more pronounced at medium input drive levels. This result is in good agreement with that reported in Figure 4.6.
Figure 4.11 depicts the simulated power-added efficiency (PAE) of the dual-input Doherty PA with digital adaptive phase alignment. The superior efficiency performance of the proposed architecture, as compared to the conventional one, is the direct result of the improved active load modulation mechanism and the increased RF output power.

![Figure 4.11 Simulated PAE of the Doherty PA, with and without adaptive phase alignment](image)

4.5 Implementation and Experimental Results

Thus far, the superior load modulation and output power profiles of the Doherty PA when the phases of the carrier and peaking branches are adequately aligned have been demonstrated to be instrumental in increasing the overall efficiency of the PA. In this
section, the implementation procedure of the dual-input digital Doherty PA is described; and, measurement results are discussed.

In the experiments, the dual-input Doherty PA is implemented based on the single-input Doherty PA prototype that was presented in Chapter 3 by eliminating the input analog splitter. Isolators are inserted between the preamplification stage and the input branches of the dual-input Doherty PA in order to ensure that the carrier and peaking amplifiers are operating into 50 Ω source impedance at all times. The bias settings of the carrier and peaking amplifiers are those reported in Section 4.2 for the PA prototype that was implemented using the CGH40010 GaN device. The separate RF inputs of the carrier and peaking amplifiers are evenly driven by using two synchronized arbitrary waveform generators (AWGs), ESG–4438C from Agilent Technologies Inc.

To implement the adaptive phase alignment functionally for the continuous wave (CW) test, the phase offset of the peaking AWG is corrected by adaptively changing the starting phase of the in-phase/quadrature (I/Q) waveform. A photograph of the experimental set-up of dual-input digital Doherty PA is shown in Figure 4.12.

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**Figure 4.12 Experimental setup of the dual-input Doherty PA with digital adaptive phase alignment**

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The measured PAE results for the CW test are presented in Figure 4.13. The obtained results confirm the benefits of the digital Doherty PA. The maximal output power is increased from 43.6 to 44.5 dBm, which extends the operation of the Doherty PA by 0.9 dB. The adaptive phase alignment between the carrier and peaking amplifiers helped increasing the overall output power of the Doherty PA, which translated into higher efficiency performance. In fact, the PAE is significantly improved at medium and high power regions. In fact, the drop that has been observed in the efficiency curve of the previously designed Doherty PA is completely avoided; and, at peak power, the PAE is increased from 62 to nearly 71%.

Figure 4.13 Measured PAE of the Doherty PA, with and without adaptive phase alignment
For the modulated signal test, the digital adaptive phase alignment mechanism is implemented by applying phase digital predistortion (PDPD) at the input of the peaking path [36–38]. As illustrated in Figure 4.14, this process results in two quasi-steady AM/PM responses having a constant phase shift that is digitally aligned by adding a phase offset to the input signal of the carrier or the peaking amplifier.

![Figure 4.14 Execution of the digital adaptive phase alignment mechanism](image)

The measured output spectra of the two Doherty PAs driven with a 5 MHz bandwidth WiMAX signal having a PAPR of 7 dB are shown in Figure 4.15. It can be seen that the two Doherty PAs have comparable linearity performance. However, the
The dual-input digital Doherty PA delivered an average PAE of 57% at the average output power of 37.8 dBm. Under identical drive conditions, the average efficiency and the output power of the single-input fully analog Doherty PA were 50% and 36.8 dBm, respectively.

![Figure 4.15 Measured output spectra, with and without adaptive phase alignment](image)

The previously discussed results confirm the merits of the dual-input digitally driven Doherty architecture in boosting the RF performance of GaN Doherty PAs. The flexibility and performance enhancement achieved by this architecture justify the slightly increased complexity due to the need for an additional signal upconversion branch.
4.6 Conclusion

In this chapter, the dynamic phase imbalance between the carrier and peaking amplifiers of GaN Doherty PAs was investigated. It was found that this problem yields significant loss of output power, impaired load modulation and fast efficiency drop following the turn-on of the peaking amplifier.

To overcome these issues, the dual-input digitally driven Doherty PA architecture was proposed. In this architecture, direct access to the baseband signals of the carrier and peaking amplifiers enabled the implementation of a digital adaptive phase alignment mechanism that compensated for the phase discrepancy between the carrier and peaking amplifiers. Driven with a WiMAX modulated signal, the dual-input digital Doherty PA demonstrated an improvement of 7% in average efficiency and 1 dB in average output power with no linearity deterioration, as compared to the fully analog Doherty PA.

In the next chapter, the dual-input Doherty PA architecture will be demonstrated to be of major usefulness in jointly surmounting two other critical limitations that compromise the performance Doherty PAs, namely amplitude imbalance between the carrier and peaking amplifiers and input power waste into the peaking branch at back-off.

5.1 Introduction

In addition to the phase misalignment problem that was discussed in the previous chapter, the difference in classes of operation of the carrier and peaking amplifiers results in a gain imbalance between the two branches of the Doherty power amplifier (PA). As such, the maximal output power of the peaking amplifier is lower than that of the carrier amplifier, which yields a deficient load modulation mechanism and degraded power efficiency [31–34, 41].

Furthermore, due to its class C bias, the peaking amplifier is active only during short bursts when the instantaneous input power exceeds the conduction threshold of the peaking device. Accordingly, the share of input power that is supplied to the peaking amplifier is wasted when it is turned OFF [40].

In the present chapter, a dual-input Doherty PA employing digital adaptive input power distribution is introduced [51]. This digitally driven Doherty PA allows effectively overcoming the above-discussed problems. Furthermore, it helps extending the range of high back-off efficiency where the probability of occurrences of the input signal is relatively high. This is achieved by adaptively distributing the input power between the carrier and peaking amplifiers to reduce the power drive into the peaking branch when the peaking device is turned OFF; and, to ensure that the output amplitudes of the carrier and peaking amplifiers are aligned at peak power, as dictated by the ideal load modulation mechanism [51].
The merits of the digitally driven Doherty PA introduced in this chapter are highlighted from a theoretical point of view based on an in-depth study of its operational principle. In this context, new analytical models of the output currents and input power profiles of the carrier and peaking sources are also proposed.

Besides, by taking advantage of the high flexibility and the large potential of the dual-input Doherty PA architecture presented in the previous chapter, the dual-input configuration is adopted to enable the implementation of a digitally controlled adaptive power distribution scheme between the carrier and peaking amplifiers. This offers a superior degree of freedom to efficiently distribute the power between the two branches of the Doherty PA without relying on the nonlinear behavior of the devices [41].

5.2 Illustration of Amplitude Imbalance and Power Waste Problems

This section briefly presents the design specifications of a symmetrical Doherty PA and discusses its performance. This design will be used as a reference to benchmark the performance of the digitally driven Doherty PA that is introduced in the next Section.

The Doherty PA prototype under test was implemented using 10-Watt CGH40010 gallium nitride (GaN) transistor from Cree Inc. The PA was designed for downlink Wideband Code Division Multiple Access (WCDMA) applications and operated at the center frequency of 2.14 GHz [35]. The carrier amplifier and peaking amplifier are biased in class AB (gate voltage, $V_{GS} = -2.1$ V, drain voltage, $V_{DS} = 28$ V, and quiescent current, $I_{DQ} = 200$ mA) and class C ($V_{GS} = -4$ V, $V_{DS} = 28$ V, and $I_{DQ} = 0$), respectively. The input splitter was implemented using 3 dB quadrature branchline coupler providing equal input power division to the carrier and peaking amplifiers at all times. This second Doherty PA will be used as basis prototype for the remaining parts of the thesis.
Figure 5.1 depicts the measured gain and power-added efficiency (PAE) of the balanced class AB and Doherty PAs driven with a continuous wave (CW) signal. The two PAs are identical in all aspects except for the bias conditions of the second amplifier of the balanced class AB PA, which are set to $V_{GS} = -2.1 \, V$, $V_{DS} = 28$, and $I_{DQ} = 200 \, mA$.

Based on Figure 5.1, it is noticeable that the symmetrical Doherty PA has lower gain in comparison to the balanced class AB amplifier. Indeed, the small signal gain of the Doherty PA is nearly 3 dB lower than that of the balanced class AB amplifier. This is
due to the fact that half of the input drive power is wasted while the peaking amplifier is inactive. Therefore, it is crucial to minimize this waste in order to improve the performance at back-off.

Moreover, it can be seen that, as expected, the Doherty PA has higher efficiency at back-off. The peak power efficiency of the Doherty PA, however, is lower than that of the balanced class AB amplifier. The deviation from the ideal case where the peak power efficiency of the Doherty PA is comparable to that of the balanced class AB PA is mainly attributed to gain imbalance between the carrier and peaking amplifiers at peak power as well as dynamic phase imbalance between the carrier and peaking amplifiers [31–34, 50].

5.3 Theoretical Analysis of Doherty PA Operation with Adaptive Input Power Distribution

To overcome the issues related to gain and efficiency deterioration in symmetrical Doherty PAs, the digitally driven Doherty PA with adaptive input power distribution is proposed in this chapter [51]. In this section, a theoretical analysis explaining the operational principle of the proposed Doherty PA and demonstrating its usefulness in boosting the efficiency over a wide operational range is detailed.

Henceforth, the digitally driven Doherty PA with adaptive input power distribution will be denoted by digital Doherty PA.

5.3.1 Output Currents and Input Power Distribution Profiles

The analytical study is started by briefly recalling the operational principle of the symmetrical Doherty PA to be then generalized for the digital Doherty PA.

Assuming that the magnitude of each current source is linearly proportional to the input drive voltage \(v_{in}\) and that the conduction angle of each amplifier remains
unvarying and independent from \(v_{\text{in}}\), the fundamental current and direct current (DC) of the carrier and peaking sources of the symmetrical Doherty PA can be written as [51]:

\[ I_{\text{C,sym}}(v_{\text{in}}, \varphi_{C}) = \frac{v_{\text{in}}}{V_{\text{in,max}}} \cdot I_{1,C}(\varphi_{C}), \quad 0 \leq v_{\text{in}} \leq V_{\text{in,max}} \] (5.1)

\[ I_{\text{DC,C,sym}}(v_{\text{in}}, \varphi_{C}) = \frac{v_{\text{in}}}{V_{\text{in,max}}} \cdot I_{\text{dc,C}}(\varphi_{C}), \quad 0 \leq v_{\text{in}} \leq V_{\text{in,max}} \] (5.2)

\[ I_{\text{P,sym}}(v_{\text{in}}, \varphi_{P}) = \begin{cases} \frac{v_{\text{in}}}{V_{\text{in,max}}} - \frac{V_{\text{turn-on,sym}}}{V_{\text{in,max}}} \cdot I_{1,P}(\varphi_{P,\text{sym}}), & 0 \leq v_{\text{in}} \leq V_{\text{turn-on,sym}} \\ V_{\text{turn-on,sym}} \leq v_{\text{in}} \leq V_{\text{in,max}} \end{cases} \] (5.3)

\[ I_{\text{DC,P,sym}}(v_{\text{in}}, \varphi_{P}) = \begin{cases} \frac{v_{\text{in}}}{V_{\text{in,max}}} - \frac{V_{\text{turn-on,sym}}}{V_{\text{in,max}}} \cdot I_{\text{dc,P}}(\varphi_{P,\text{sym}}), & 0 \leq v_{\text{in}} \leq V_{\text{turn-on,sym}} \\ V_{\text{turn-on,sym}} \leq v_{\text{in}} \leq V_{\text{in,max}} \end{cases} \] (5.4)

where

\[ I_{1,C}(\varphi_{C}) = \frac{I_{\text{max}}}{2\pi} \cdot \frac{\varphi_{C} - \sin \varphi_{C}}{1 - \cos \left( \frac{\varphi_{C}}{2} \right)} \] (5.5)

\[ I_{\text{dc,C}}(\varphi_{C}) = \frac{I_{\text{max}}}{2\pi} \cdot \frac{2 \sin \left( \frac{\varphi_{C}}{2} \right) - \varphi_{C} \cdot \cos \left( \frac{\varphi_{C}}{2} \right)}{1 - \cos \left( \frac{\varphi_{C}}{2} \right)} \] (5.6)

\[ I_{1,P}(\varphi_{P,\text{sym}}) = \frac{I_{\text{max}}}{2\pi} \cdot \frac{\varphi_{P,\text{sym}} - \sin \varphi_{P,\text{sym}}}{1 - \cos \left( \frac{\varphi_{P,\text{sym}}}{2} \right)} \] (5.7)
\[ I_{\text{dc},p}(\phi_{\text{p, sym}}) = \frac{I_{\text{max}}}{2\pi} \cdot \frac{2 \sin \left( \frac{\phi_{\text{p, sym}}}{2} \right) - \phi_p \cdot \cos \left( \frac{\phi_{\text{p, sym}}}{2} \right)}{1 - \cos \left( \frac{\phi_{\text{p, sym}}}{2} \right)} \] (5.8)

\[ V_{\text{turn-on, sym}} = \frac{V_{\text{in, max}}}{2} \] (5.9)

and \( I_{\text{C, sym}}, I_{\text{P, sym}}, I_{\text{DC, C, sym}} \) and \( I_{\text{DC, P, sym}} \) denote the fundamental and DC current components of the carrier and peaking amplifiers of the symmetrical Doherty PA, respectively. \( \phi_C \) and \( \phi_{\text{p, sym}} \) designate the conduction angles of the carrier and peaking amplifiers of the symmetrical Doherty PA, respectively. \( V_{\text{in, max}} \) is the maximal input drive voltage, \( I_{\text{max}} \) is the maximal current level, and \( V_{\text{turn-on, sym}} \) is the input drive level corresponding to the turn-on point of the peaking device of the symmetrical Doherty amplifier.

Figure 5.2 shows the fundamental current profiles of the carrier and peaking amplifiers of the symmetrical Doherty PA. In operation, the back-off saturation point of the carrier amplifier occurs at the input voltage level of \( (V_{\text{in, max}}/2) \), when the output current reaches \( (I_{\text{1, C, } \phi_C}/2) \). It is also to be noted that, because of the lower conduction angle of the peaking device, the maximal output current of the peaking amplifier at full power drive is lower than that of the carrier amplifier, which yields an incomplete load modulation and reduced peak efficiency [31–34, 41, 51].
Figure 5.2 Fundamental currents of the carrier and peaking amplifiers of the digital and symmetrical Doherty PAs versus input voltage

To prevent the power loss and improve the load modulation, the proposed digital Doherty PA utilizes a dynamic input power distribution, providing more input power to the carrier amplifier at back-off; and, conveying more input power to the peaking amplifier at the high power region.

To investigate the effects of the adaptive input power distribution on the overall performance, a new fundamental current profile is modeled in Figure 5.2. In this model, the fundamental current of the carrier amplifier is increased by a multiplicative factor ($\delta$).
prior to the turn-on of the peaking device, while that of the peaking amplifier is increased by a multiplicative factor ($\sigma$) after the turn-on point.

As illustrated in Figure 5.2, once the peaking amplifier is turned ON, the operation of the digital Doherty PA is similar to that of the uneven Doherty PA that was reported in [32]; and thus, the currents of the carrier and peaking sources follow the tendency exhibited by the uneven Doherty PA. Accordingly, the current profiles of the digital Doherty PA are given by [51]:

\[
I_{C,\text{dig}}(v_{\text{in}}, \varphi_C) = \begin{cases} 
\delta \cdot \frac{v_{\text{in}}}{V_{\text{in,max}}} \cdot I_{1,C}(\varphi_C), & 0 \leq v_{\text{in}} < V_{\text{turn-on,dig}} \\
\sqrt{(2 - \sigma^2)} \cdot \frac{v_{\text{in}}}{V_{\text{in,max}}} \cdot I_{1,C}(\varphi_C), & V_{\text{turn-on,dig}} \leq v_{\text{in}} \leq V_{\text{in,max}} 
\end{cases}
\] (5.10)

\[
I_{\text{DC,C,dig}}(v_{\text{in}}, \varphi_C) = \begin{cases} 
\delta \cdot \frac{v_{\text{in}}}{V_{\text{in,max}}} \cdot I_{\text{dc,C}}(\varphi_C), & 0 \leq v_{\text{in}} < V_{\text{turn-on,dig}} \\
\sqrt{(2 - \sigma^2)} \cdot \frac{v_{\text{in}}}{V_{\text{in,max}}} \cdot I_{\text{dc,C}}(\varphi_C), & V_{\text{turn-on,dig}} \leq v_{\text{in}} \leq V_{\text{in,max}} 
\end{cases}
\] (5.11)

\[
I_{P,\text{dig}}(v_{\text{in}}, \varphi_{P,\text{dig}}) = \begin{cases} 
0, & 0 \leq v_{\text{in}} \leq V_{\text{turn-on,dig}} \\
\sigma \left( \frac{v_{\text{in}}}{V_{\text{in,max}}} - \frac{V_{\text{turn-on,dig}}}{V_{\text{in,max}}} \right) \cdot I_{1,P}(\varphi_{P,\text{dig}}), & V_{\text{turn-on,dig}} \leq v_{\text{in}} \leq V_{\text{in,max}} 
\end{cases}
\] (5.12)

\[
I_{\text{DC,P,dig}}(v_{\text{in}}, \varphi_{P,\text{dig}}) = \begin{cases} 
0, & 0 \leq v_{\text{in}} \leq V_{\text{turn-on,dig}} \\
\sigma \left( \frac{v_{\text{in}}}{V_{\text{in,max}}} - \frac{V_{\text{turn-on,dig}}}{V_{\text{in,max}}} \right) \cdot I_{\text{dc,P}}(\varphi_{P,\text{dig}}), & V_{\text{turn-on,dig}} \leq v_{\text{in}} \leq V_{\text{in,max}} 
\end{cases}
\] (5.13)

where
\[ I_{1,p}(\varphi_{P,\text{dig}}) = \frac{I_{\text{max}}}{2\pi} \cdot \varphi_{P,\text{dig}} - \sin \varphi_{P,\text{dig}} \cdot \frac{1 - \cos\left(\frac{\varphi_{P,\text{dig}}}{2}\right)}{1 - \cos\left(\frac{\varphi_{P,\text{dig}}}{2}\right)} \] \tag{5.14}

\[ I_{\text{dc},p}(\varphi_{P,\text{dig}}) = \frac{I_{\text{max}}}{2\pi} \cdot \frac{2 \sin\left(\frac{\varphi_{P,\text{dig}}}{2}\right) - \varphi_{C} \cdot \cos\left(\frac{\varphi_{P,\text{dig}}}{2}\right)}{1 - \cos\left(\frac{\varphi_{P,\text{dig}}}{2}\right)} \] \tag{5.15}

\[ \delta = \frac{I_{C,\text{dig}}(v_{\text{in}},\varphi_{C})}{I_{C,\text{sym}}(v_{\text{in}},\varphi_{C})}, \quad 0 \leq v_{\text{in}} < V_{\text{turn-on,dig}} \] \tag{5.16}

and \( I_{C,\text{dig}}, I_{P,\text{dig}}, I_{\text{DC,C,\text{dig}}} \) and \( I_{\text{DC,P,\text{dig}}} \) denote the fundamental and DC current components of the carrier and peaking amplifiers of the digital Doherty PA, respectively. \( \sigma \) is the enhanced current factor necessary to align the output currents of the carrier and peaking amplifiers at peak power. \( V_{\text{turn-on,dig}} \) and \( \varphi_{P,\text{dig}} \) designate the turn-on point and the conduction angle of the peaking amplifier of the digital Doherty PA, respectively.

Since the output current of the carrier amplifier in the digital Doherty PA is \( \delta \) times larger than that of the symmetrical Doherty PA at the back-off, the output current of the carrier amplifier reaches the saturation state \( (I_{1,C}(\varphi_{C})/2) \) earlier than \( (V_{\text{in,max}}/2) \), precisely at \( (V_{\text{in,max}}/2\delta) \). Therefore, the turn-on point of the peaking device of the digital Doherty PA, \( V_{\text{turn-on,dig}} \), is given by:

\[ V_{\text{turn-on,dig}} = \frac{V_{\text{in,max}}}{2\delta} \] \tag{5.17}

As a result of the early saturation of the carrier amplifier, an extended range of high efficiency at back-off is achieved; and, the additional efficiency range \( (\gamma) \) is expressed as:
\( \gamma [\text{dB}] = 10 \cdot \log_{10}(\delta^2) \) \hspace{1cm} (5.18)

and the total power back-off (PBO\textsubscript{dig}) following the saturation of the carrier amplifier is given by:

\[
P_{\text{BO\textsubscript{dig}}}[\text{dB}] = 6 + 10 \cdot \log_{10}(\delta^2) = 6 + \gamma \hspace{1cm} (5.19)
\]

Once PBO\textsubscript{dig} is known, the conduction angle of the peaking amplifier (\( \varphi_{P,\text{dig}} \)) of the digital Doherty PA is then chosen to ensure the turn-on condition at the input power level given by (\( P_{\text{in,max}} - \text{PBO}_{\text{dig}} \)), where \( P_{\text{in,max}} \) denotes the maximal input power (in dBm) of the Doherty PA. Practically, the gate bias point associated to (\( \varphi_{P,\text{dig}} \)) can be determined by satisfying the turn-on condition when the standalone peaking amplifier is driven with (\( P_{\text{in,max}} - \text{PBO}_{\text{dig}} - 3 \)) dBm.

Besides, it is noteworthy that, because of the uneven drive at the high power region, the maximal current of the carrier amplifier of the digital Doherty PA is actually lower than that of the symmetrical Doherty PA (\( I_{1,C}(\varphi_C) \)). Based on the mathematical demonstration exposed in the appendix, the peak power current of the carrier amplifier of the digital Doherty PA is expressed by:

\[
I_{C,\text{dig}}(V_{\text{in,max}},\varphi_C) = \sqrt{(2 - \sigma^2)} \cdot I_{1,C}(\varphi_C) \hspace{1cm} (5.20)
\]

Accordingly, by using (5.12) and (5.20), the enhanced current factor \( \sigma \) is solution of:

\[
\sqrt{(2 - \sigma^2)} \cdot I_{1,C}(\varphi_C) = \sigma \cdot \left(1 - \frac{1}{2\delta}\right) \cdot I_{1,P}(\varphi_{P,\text{dig}}) \hspace{1cm} (5.21)
\]

and it is given by:
\[ \sigma = \frac{2 \cdot \nu^2}{\sqrt{1 + \nu^2}} \]  

(5.22)

where \( \nu \) is expressed by:

\[ \nu = \frac{I_{1,C}(\phi_C)}{(1 - \frac{1}{2\delta}) \cdot I_{1,P}(\phi_{P,dig})} \]  

(5.23)

By using the theoretical formulations derived in the appendix, the following expressions arise:

\[ P_{in,C,dig} = \frac{\delta^2}{2} \cdot P_{in,DPA}, \quad 0 \leq \nu_{in} < \frac{V_{in,max}}{2\delta} \]  

(5.24)

\[ P_{in,P,dig} = \frac{\sigma^2}{2} \cdot P_{in,DPA}, \quad \frac{V_{in,max}}{2\delta} \leq \nu_{in} < V_{in,max} \]  

(5.25)

where \( (P_{in,C,dig}) \) and \( (P_{in,P,dig}) \) are the respective input powers supplied to the carrier branch and to the peaking branch of the digital Doherty PA. \( P_{in,DPA} \) is the total input power of the Doherty PA.

It is of note that it can be inferred from (5.24) and (5.25) that the enhanced current factors \( \delta \) and \( \sigma \) are both bounded by 1 (i.e. the input power is equally split between the carrier and peaking branches) and \( \sqrt{2} \) (i.e. the input power is completely supplied to either branch of the Doherty PA). It is also to be noted that, when \( \delta \) and \( \sigma \) are both equal to 1, the digital Doherty PA is reduced to the particular case of the symmetrical Doherty PA. This can be easily verified throughout all expressions that include \( \delta \) and \( \sigma \).

Based on (5.24) and (5.25), the input power distribution profile of the digital Doherty PA can be expressed by:
\[ P_{\text{in,C,\text{dig}}}[\text{dBm}] = \begin{cases} 10 \cdot \log_{10} \left( \frac{\delta^2}{2} \right) + P_{\text{in,DPA}} \left|_{\text{dBm}}, \right. & \text{if } P_{\text{in,DPA}} < P_{\text{in,max}} - (6 + \gamma) \\ 10 \cdot \log_{10} \left( 1 \right) + P_{\text{in,DPA}} \left|_{\text{dBm}}, \right. & \text{if } P_{\text{in,DPA}} \geq P_{\text{in,max}} - (6 + \gamma) \end{cases} \] (5.26)

\[ P_{\text{in,P,\text{dig}}}[\text{dBm}] = \begin{cases} 10 \cdot \log_{10} \left( 1 \right) + P_{\text{in,DPA}} \left|_{\text{dBm}}, \right. & \text{if } P_{\text{in,DPA}} < P_{\text{in,max}} - (6 + \gamma) \\ 10 \cdot \log_{10} \left( \frac{\delta^2}{2} \right) + P_{\text{in,DPA}} \left|_{\text{dBm}}, \right. & \text{if } P_{\text{in,DPA}} \geq P_{\text{in,max}} - (6 + \gamma) \end{cases} \] (5.27)

By using (5.26) and (5.27), the carrier-to-peaking power division ratio of the digital Doherty PA \((R_{\text{dig}})\) can be expressed by:

\[ R_{\text{dig}}[\text{dB}] = P_{\text{in,C,\text{dig}}}[\text{dBm}] - P_{\text{in,P,\text{dig}}}[\text{dBm}] \]

\[ = \begin{cases} 10 \cdot \log_{10} \left( \frac{\delta^2}{2 - \delta^2} \right), & \text{if } P_{\text{in,DPA}} < P_{\text{in,max}} - (6 + \gamma) \\ 10 \cdot \log_{10} \left( \frac{2 - \sigma^2}{\sigma^2} \right), & \text{if } P_{\text{in,DPA}} \geq P_{\text{in,max}} - (6 + \gamma) \end{cases} \] (5.28)

Figure 5.3 depicts the power division profiles for the symmetrical Doherty PA and the digital Doherty PA. At low power drive levels, the carrier amplifier of the digital Doherty PA receives \(10 \cdot \log_{10} \left( \frac{\delta^2}{2 - \delta^2} \right)\) dB higher input power compared to the peaking amplifier. Conversely, after the turn-on point, it gets \(10 \cdot \log_{10} \left( \frac{2 - \sigma^2}{\sigma^2} \right)\) dB lower input power compared to the peaking amplifier. As for the symmetrical Doherty PA \((\delta = 1, \sigma = 1)\), the carrier and peaking amplifiers receive the same input power at all times.
5.3.2 Performance Analysis

The efficiency of the Doherty PA is analyzed based on the equivalent circuit diagram that is presented in Figure 5.4. For simplicity, it is assumed that each current source is terminated with ideal harmonic short circuit so that the efficiency and the output power can be assessed using only the fundamental and DC components that are expressed in (5.1)–(5.8) and (5.10)–(5.15).
Referring to Figure 5.4, the load impedances of the carrier amplifier ($Z_C$) and that of peaking amplifier ($Z_P$) are determined by the current ratios as:

$$Z_{C,dig} = \begin{cases} \frac{Z_T^2}{Z_L}, & 0 \leq v_{in} < \frac{V_{in,max}}{2\delta} \\ \frac{Z_T^2}{Z_L \cdot \left(1 + \frac{I_{p,dig}(v_{in},\Phi_{P,dig})}{I_{C,dig}(v_{in},\Phi_C)}\right)}, & V_{in,max}/2\delta \leq v_{in} \leq V_{in,max} \end{cases}$$

(5.29)

$$Z_{P,dig} = \begin{cases} \frac{Z_L}{Z_T}, & 0 \leq v_{in} < \frac{V_{in,max}}{2\delta} \\ \frac{Z_L}{Z_T \cdot \left(1 + \frac{I_{C,dig}(v_{in},\Phi_C)}{I_{P,dig}(v_{in},\Phi_{P,dig})}\right)}, & V_{in,max}/2\delta \leq v_{in} \leq V_{in,max} \end{cases}$$

(5.30)

where

$$Z_T = Z_0$$

(5.31)

$$Z_L = \frac{Z_0}{2}$$

(5.32)

$$Z_0 = \frac{V_{DC}}{I_{1,C}(\Phi_C)} \approx \frac{V_{DC}}{I_{1,P}(\Phi_{P,sym})} \approx \frac{V_{DC}}{I_{1,P}(\Phi_{P,dig})}$$

(5.33)
and $Z_0$ is the optimal load impedance of the carrier and peaking amplifiers. $Z_T$ and $Z_L$ are the characteristic impedance of impedance inverter and the common load at the junction point of the Doherty network, respectively. $V_{DC}$ is the drain supply voltage.

At the low power region ($0 \leq v_{in} < V_{in,\text{max}}/2\delta$), only the carrier amplifier is active. Accordingly, by using (5.10), (5.11), (5.29) and (5.31)–(5.33), the output radio frequency (RF) power ($P_{RF,\text{dig}}$) and DC power ($P_{DC,\text{dig}}$) of the digital Doherty PA are demonstrated to be:

$$P_{RF,\text{dig}} = \frac{1}{2} I_{C,\text{dig}}^2(v_{in},\varphi_C) \cdot Z_{C,\text{dig}} = \delta^2 \cdot \left(\frac{v_{in}}{v_{in,\text{max}}}\right)^2 \cdot I_{1,C}(\varphi_C) \cdot V_{DC}$$ (5.34)

$$P_{DC,\text{dig}} = I_{DC,C,\text{dig}}(v_{in},\varphi_C) \cdot V_{DC} = \delta \cdot \frac{v_{in}}{V_{in,\text{max}}} \cdot I_{dc,C}(\varphi_C) \cdot V_{DC}$$ (5.35)

From (5.34) and (5.35), the efficiency of the digital Doherty PA ($\eta_{\text{dig}}$) can be calculated as:

$$\eta_{\text{dig}}(v_{in}) = \frac{P_{RF,\text{dig}}}{P_{DC,\text{dig}}} = \delta \cdot \left(\frac{v_{in}}{V_{in,\text{max}}} \cdot \frac{I_{1,C}(\varphi_C)}{I_{dc,C}(\varphi_C)}\right) = \delta \cdot \eta_{\text{sym}}(v_{in})$$ (5.36)

where ($\eta_{\text{sym}}$) is recognized as the efficiency of the symmetrical Doherty PA at the region ($0 \leq v_{in} < V_{in,\text{max}}/2\delta$); and, it is expressed based on (5.34) and (5.35) as:

$$\eta_{\text{sym}}(v_{in}) = \frac{P_{RF,\text{sym}}}{P_{DC,\text{sym}}} = \left.\frac{P_{RF,\text{dig}}}{P_{DC,\text{dig}}}\right|_{\delta=1} = \left(\frac{v_{in}}{V_{in,\text{max}}}\right)^2 \cdot \frac{I_{1,C}(\varphi_C) \cdot V_{DC}}{V_{in,\text{max}} \cdot I_{dc,C}(\varphi_C) \cdot V_{DC}}$$ (5.37)

$$= \frac{v_{in}}{V_{in,\text{max}}} \cdot \frac{I_{1,C}(\varphi_C)}{I_{dc,C}(\varphi_C)}$$
where \((P_{RF,sym})\) and \((P_{DC,sym})\) designate the output RF power and DC power of the symmetrical Doherty PA, respectively.

The result obtained in (5.35) is significant in that it demonstrates that the digital Doherty PA exhibits \(\delta\) times higher efficiency at back-off compared to its symmetrical counterpart.

Furthermore, by defining the enhanced power gain ratio \((\chi)\) as:

\[
\chi = \frac{P_{RF,dig}}{P_{RF,sym}} = \frac{\delta^2 \cdot \left(\frac{v_{in}}{V_{in,max}}\right)^2 \cdot I_{1,C}(\varphi_C) \cdot V_{DC}}{\left(\frac{v_{in}}{V_{in,max}}\right)^2 \cdot I_{1,C}(\varphi_C) \cdot V_{DC}} = \delta^2
\]

(5.38)

it can be deduced that the gain of the digital Doherty PA is \(\delta^2\) times higher than that of the conventional Doherty PA, at the low power region \((0 \leq v_{in} < V_{in,max} / 2\delta)\).

At the high power region \((V_{in,max} / 2\delta \leq v_{in} \leq V_{in,max})\), both amplifiers contribute to the output power of the Doherty PA. Accordingly, by using (5.10)–(5.14), (5.21) and (5.29)–(5.33), the output RF power \((P_{RF,dig})\) and DC power \((P_{DC,dig})\) of the digital Doherty PA are given by:

\[
P_{RF,dig} = \frac{1}{2} \cdot \left( I_{C,dig}(v_{in},\varphi_C) \cdot Z_{C,dig} + I_{P,dig}(v_{in},\varphi_P,dig) \cdot Z_{P,dig} \right)
\]

\[
= \sigma^2 \cdot \left\{ \left[ \left( \frac{1}{2\delta} \right)^3 \cdot V^3 + \frac{1}{4} \cdot \left( V - \frac{1}{2\delta} \right) \cdot \left[ \left( \frac{2}{2\delta} \right) \cdot V - \frac{1}{2\delta} \right] \right] \cdot I_{1,P}(\varphi_P,dig) \right\} \cdot V_{DC}
\]

(5.39)
\[ P_{DC,dig} = (I_{DC,C,dig}(v_{in}, \phi_c) + I_{DC,P,dig}(v_{in}, \phi_{P,dig})) \cdot V_{DC} \]

\[ = \left[ (2 - \sigma^2) \cdot V \cdot I_{dc,C}(\phi_c) + \sigma \cdot \left( V - \frac{1}{2\delta} \right) \cdot I_{dc,P}(\phi_{P,dig}) \right] \cdot V_{DC} \]

(5.40)

where

\[ V = \frac{v_{in}}{V_{in,max}} \]

(5.41)

Based on (5.39) and (5.40), the efficiency of the digital Doherty PA \( \eta_{dig} \) can be expressed as:

\[ \eta_{dig}(v_{in}) = \frac{P_{RF,dig}}{P_{DC,dig}} \]

\[ = \left\{ \frac{\sigma^2 \cdot \left( 1 - \frac{1}{2\delta} \right)^3 \cdot V^3}{\left( \left[ (2 - \frac{1}{2\delta}) \cdot V - \frac{1}{2\delta} \right] \cdot \left[ (2 - \frac{1}{2\delta}) \cdot V - \frac{1}{2\delta} \right] \right)} \right\} I_{1,p}(\phi_{P,ext}) \]

\[ + \left[ (2 - \sigma^2) \cdot V \cdot I_{dc,C}(\phi_c) + \sigma \cdot \left( V - \frac{1}{2\delta} \right) \cdot I_{dc,P}(\phi_{P,ext}) \right] \]

(5.42)

Assuming that the carrier and peaking amplifiers consume the same DC power at peak power drive (i.e., \( \sqrt{(2 - \sigma^2)} \cdot I_{dc,C}(\phi_c) \cdot V_{DC} = (1 - \frac{1}{2\delta}) \cdot I_{dc,P}(\phi_{P,dig}) \cdot V_{DC} \)), then by using (5.42), the power efficiency of the digital Doherty PA at peak voltage drive (i.e., \( V = 1 \)) can be demonstrated to be:

\[ \eta_{dig}(V_{in,max}) = \frac{1}{2} \cdot \frac{\sigma \cdot \left( 1 - \frac{1}{2\delta} \right) \cdot I_{1,p}(\phi_{P,dig})}{I_{dc,P}(\phi_{P,dig})} = \eta_P \]

(5.43)
where \( \eta_P \) is identified as the maximal power efficiency of the standalone peaking amplifier; and, it is expressed based on (5.12)–(5.15) and (5.30)–(5.33) as:

\[
\eta_P = \frac{P_{RF,P}}{P_{DC,P}} = \frac{1}{2} \left[ \frac{I_{P,\text{dig}}^2 (V_{\text{in,\text{max}},P} \cdot \phi_{P,\text{dig}}) \cdot Z_{P,\text{dig}}}{I_{DC,P,\text{dig}} (V_{\text{in,\text{max}},P} \cdot \phi_{P,\text{dig}}) \cdot V_{DC}} \right] = \frac{1}{2} \left[ \frac{\sigma \cdot \left( 1 - \frac{1}{2 \delta} \right) \cdot I_{1,P} (\phi_{P,\text{dig}})}{\sigma \cdot \left( 1 - \frac{1}{2 \delta} \right) \cdot I_{dc,P} (\phi_{P,\text{dig}}) \cdot V_{DC}} \right]^2 \cdot Z_0
\]

(5.44)

where \( (P_{RF,P}) \) and \( (P_{DC,P}) \) designate the maximal output RF power and DC power of the standalone peaking amplifier, respectively.

The result of (5.43) is also significant as it shows that the efficiency of the digital Doherty PA at peak power is maximal, which demonstrates its capability of boosting the efficiency at the high power region.

Based on the above-derived expressions, it can be concluded that the digital Doherty PA has a number of interesting features. Indeed, it is proven that it helps increasing the efficiency and gain performance at back-off. In addition, due to the dynamic input power distribution, the digital Doherty PA has an extended range of high efficiency at back-off as well as maximal efficiency performance at peak power. The main characteristics of the digital Doherty PA are summarized in Table 5.1 and compared side-by-side to those of the symmetrical Doherty PA.

In the next Sections, the operational analysis of the digital Doherty PA is validated through simulation and experimental results.
Table 5.1 Characteristics of the Symmetrical and Digital Doherty PAs

<table>
<thead>
<tr>
<th>Parameter/Performance</th>
<th>Symmetrical Doherty PA</th>
<th>Digital Doherty PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \delta )</td>
<td>1</td>
<td>( 1 \leq \delta \leq \sqrt{2} )</td>
</tr>
<tr>
<td>( \sigma )</td>
<td>1</td>
<td>( 1 \leq \sigma \leq \sqrt{2} )</td>
</tr>
<tr>
<td>( V_{\text{turn-on}} )</td>
<td>( V_{\text{in,max}}/2 )</td>
<td>( V_{\text{in,max}}/2\delta )</td>
</tr>
<tr>
<td>( \gamma )</td>
<td>0 dB</td>
<td>( 10 \cdot \log_{10}(\delta^2) )</td>
</tr>
<tr>
<td>( \text{PBO}_{\text{ext}} )</td>
<td>6 dB</td>
<td>( 6 + 10 \cdot \log_{10}(\delta^2) )</td>
</tr>
<tr>
<td>( \eta ) at Back-off</td>
<td>( \eta_{\text{sym}} )</td>
<td>( \delta \cdot \eta_{\text{sym}} )</td>
</tr>
<tr>
<td>Gain at Back-off</td>
<td>( g_{\text{sym}} )</td>
<td>( \delta^2 \cdot g_{\text{sym}} )</td>
</tr>
<tr>
<td>( \eta ) at Peak Power</td>
<td>( &lt; \eta_{\text{peaking}} )</td>
<td>( \eta_{\text{peaking}} )</td>
</tr>
</tbody>
</table>

5.4 Simulation Results

For the simulation analysis, the digital Doherty PA is implemented in Advanced Design System (ADS) software. Besides, by taking advantage of its superior flexibility, the dual-input Doherty PA architecture is adopted to implement the digital adaptive input power distribution between the carrier and peaking branches. For the comparative study, a symmetrical Doherty PA circuit is also implemented in ADS.

In simulations, the adaptive power distribution is realized based on the dual-input configuration by using power-indexed look-up tables (LUTs) to control the power level of the input signals that are separately driving the carrier and peaking amplifiers. The simulations are carried out using the large signal nonlinear model of the CGH40010 transistor. Both Doherty PAs are implemented using identical input and output matching.
networks. The class C bias conditions of the peaking amplifier of the symmetrical Doherty PA and that of the digital Doherty PA are \((V_{GS} = -4 \text{ V}, V_{DS} = 28 \text{ V}, \text{ and } I_{DQ} = 0)\) and \((V_{GS} = -3.4 \text{ V}, V_{DS} = 28 \text{ V}, \text{ and } I_{DQ} = 0)\), respectively. The carrier amplifier of each Doherty PA is operated in class AB with \(V_{GS} = -2 \text{ V}, I_{DQ} = 200 \text{ mA}, \text{ and } V_{DS} = 28 \text{ V}\). For the digital Doherty PA, the value of \(\delta\) is selected to be 1.3; and, its corresponding optimal value of \(\sigma\) necessary to align the output currents is found to be equal to 1.1.

The adaptive input power division scheme used in the digital Doherty PA is shown in Figure 5.5. This profile is similar to the one that can be generated using (5.28) with \(\delta = 1.3\) and \(\sigma = 1.1\) apart from a softer transition region that is incorporated to avoid the abrupt transition that might affect the quality of the input signal.

![Figure 5.5 Power distribution schemes of the digital and symmetrical Doherty PAs](image-url)
Figure 5.6 depicts the simulated fundamental currents of the symmetrical and the digital Doherty PAs. It can be seen that the carrier amplifier of the digital Doherty PA produces more output current at back-off. In addition, the output currents of the carrier and peaking amplifiers are aligned at peak power as targeted.

Figure 5.6 Simulated fundamental currents of the carrier and peaking amplifiers of the digital and symmetrical Doherty PAs

Figure 5.7 shows the load modulation results of \((Z_C)\) for the two Doherty PAs. The load impedance of the carrier amplifier of the digital Doherty PA is modulated from 100 to 50 Ω as the input power increased. However, this is not happening for the
symmetrical Doherty PA because the peaking amplifier needs more power drive at saturation.

![Graph showing load modulation of the carrier amplifier for digital and symmetrical Doherty PAs](image)

**Figure 5.7 Simulated load modulation of the carrier amplifier of the digital and symmetrical Doherty PAs**

Figure 5.8 shows the simulated gain of the symmetrical and digital Doherty PAs with a CW stimulus. As expected, by minimizing the amount of the drive power into the peaking branch for the input power levels below the turn-on point, the power waste is reduced; consequently, the gain is significantly increased, especially at back-off. The improvement due to the adaptive input power distribution is about 2.4 dB, which is similar to the numerical result that can be obtained from (5.38) with $\delta = 1.31$. 

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Figure 5.8 Simulated gain of the digital and symmetrical Doherty PAs

Figure 5.9 depicts the simulated PAE of the two Doherty PAs serving for this study. It is clear that the digital Doherty PA has superior efficiency performance over the entire range of operation. Furthermore, it is worth noting that the back-off efficiency maximum of the symmetrical Doherty PA and that of the digital Doherty PA occur at the input power levels of 23.3 dBm and 21 dBm, respectively. The 2.3 dB difference is comparable to the theoretical extension predicted by (5.18) with $\delta = 1.31$. 
Figure 5.9 Simulated PAE of the digital and symmetrical Doherty PAs

In order to estimate the average efficiency of each Doherty PA, a one carrier worldwide interoperability for microwave access (WiMAX) signal with 9 dB peak-to-average power ratio (PAPR) is used. The probability density function (PDF) of the signal versus input power is shown in Figure 5.9. The average efficiency can be estimated based on the PDF of the signal and the CW efficiency as [51]:

\[
\langle \text{PAE} \rangle = \int \text{PAE}(P_{\text{in}}) \cdot \text{prob}(P_{\text{in}}) \, dP_{\text{in}}
\]  

(5.45)

where \( \text{prob}(P_{\text{in}}) \) is the probability of occurrences of \( P_{\text{in}} \) for the modulated input signal.

The average PAE of each Doherty PA is calculated using (5.45) while considering the simulated PAE reported in Figure 5.9. The average PAE of the symmetrical Doherty...
PA and that of the digital Doherty PA are found to be 43% and 51%, respectively. This enhancement of 8% exemplifies the suitability of the digital Doherty PA for wireless communication signals with high PAPRs.

5.5 Measurement results

Figure 5.10 shows the proof-of-concept setup of the digital Doherty PA. The dual-input prototype used in this setup is built based on the symmetrical Doherty PA prototype that was tested in Section 5.2. The bias settings of the carrier and peaking amplifiers of the digital Doherty PA are \(V_{GS} = -2.1 \text{ V}, V_{DS} = 28 \text{ V}, \text{ and } I_DQ = 200\) and \(V_{GS} = -3.5 \text{ V}, V_{DS} = 28 \text{ V}, \text{ and } I_DQ = 0\), respectively.

![Figure 5.10 Experimental setup of the dual-input Doherty PA with digital adaptive input power distribution](image)

5.5.1 Continuous Wave Measurement Results

For the CW test, the separate RF inputs of the carrier and peaking amplifiers of the digital Doherty PA prototype are controlled using two synchronized arbitrary waveform generators (AWGs), ESG–4438C from Agilent Technologies Inc. The input power level for each branch is adaptively adjusted based on the power distribution profile
reported in Figure 5.5. Also, in order to compensate for the quadrature phase relationship of the 3 dB branchline splitter that is eliminated in the dual-input configuration, the phase of the input signal of the peaking amplifier is maintained at 90º lag behind that of the carrier amplifier at all times.

The measured gain and PAE results for the CW test are presented in Figure 5.11. These results confirm the benefits of the digital Doherty PA architecture. Indeed, the small signal gain is improved by 2.3 dB. The enhancement in gain is in good agreement with theoretical and simulation results. The efficient power distribution between the carrier and peaking branches helped increasing the overall output power of the system, which ultimately translates into higher efficiency performance. In fact, the PAE is improved over a wide operational range; and, an enhancement of no less than 5% is maintained at large back-off. At saturation, the PAE is enhanced from 59 to 66%.

The measured output power results are depicted in Figure 5.12. The higher output power performance of the digital Doherty PA compared to the symmetrical Doherty PA is the result of the efficient input power distribution between the carrier and peaking branches.
Figure 5.11 Measured PAE and gain of the digital and symmetrical Doherty PAs

Figure 5.12 Measured output power of the digital and symmetrical Doherty PAs
5.5.2 Modulated Signal Measurement Results

To assess the performance using modulated signals, the digital Doherty PA is driven with a WiMAX signal having a PAPR of 9 dB and a bandwidth of 10 MHz. The baseband in-phase/quadrature \((I/Q)_{\text{in}}\) waveform of the input signal is digitally split based on the power distribution profile reported in Figure 5.5. As such, the data streams \((I/Q)_{\text{Carrier}}\) and \((I/Q)_{\text{Peaking}}\), which represent the respective input baseband waveforms of the carrier and peaking branches, are generated.

As shown in table 5.2, the digital Doherty PA delivers an average drain efficiency of 50% at the average output power of 36.8 dBm. Under identical input drive conditions, the efficiency and output power enhancement are 7% and 1 dB, respectively, compared to the symmetrical Doherty PA. However, since the power distribution profile is optimized for efficiency, the digital Doherty PA has inferior linearity performance. Indeed, the relative constellation error (RCE) is measured to be −23 dB for the symmetrical Doherty PA and −18 dB for the digital Doherty PA.

<table>
<thead>
<tr>
<th>Performance</th>
<th>Symmetrical Doherty PA</th>
<th>Digital Doherty PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Output Power</td>
<td>35.8 dBm</td>
<td>36.6 dBm</td>
</tr>
<tr>
<td>Average Efficiency</td>
<td>43%</td>
<td>50%</td>
</tr>
<tr>
<td>RCE Before DPD</td>
<td>−23 dB</td>
<td>−18 dB</td>
</tr>
<tr>
<td>RCE After DPD</td>
<td>−44 dB</td>
<td>−38 dB</td>
</tr>
</tbody>
</table>

Table 5.2 Measured Performance of the Digital and Symmetrical Doherty PAs Using WiMAX Signal
5.5.3 Linearization of the Dual-Input Digitally Driven Doherty PA

To meet the linearity requirements of the WiMAX standard, digital predistortion (DPD) is needed to linearize the dual-input digitally driven Doherty PA. Although the Doherty PA has a dual-input single-output structure, the linearization problem can be reduced to the conventional case of a single-input single-output (SISO) system. Indeed, the DPD can be applied on the SISO system that consists of \{digital adaptive signal separation unit + dual-input Doherty PA\} as device under test (DUT). Therefore, the initial characterization and DPD model identification of the digital Doherty PA can be conducted using well-established SISO methodologies \[5, 6\].

As inferred from the measured results of output spectra reported in Figure 5.13(a), a substantial linearity improvement is observed for the digital Doherty PA, after the DPD is applied. The adjacent channel power ratio (ACPR) at the 10 MHz offset is linearized to \(-46\) dBC, which is an improvement of approximately 17 dB. After linearization, the RCE is enhanced to \(-38\) dB largely satisfying the specification of the WiMAX standard, which is specified to be \(-28.5\) dB for the 64 quadratic amplitude modulation (QAM) scheme.
Figure 5.13 (a) Output spectra of the digital Doherty PA using WiMAX signal; (b) constellation diagram before DPD (gray), after DPD (black), and ideal (white +)
5.6 Conclusion

In this chapter, a digital Doherty PA with an extended range of enhanced efficiency was introduced. The improved performance resulted from a digitally controlled dynamic input power distribution that was implemented to compensate for power loss and efficiency degradation due to the use of static even power division in symmetrical Doherty PAs.

The advantages of the digital Doherty PA were investigated through an in-depth study of its operational principles. The theoretical analysis demonstrated its capability in boosting the efficiency over a wide range of operation. For the experimental validation, the dual-input digital Doherty PA architecture was used to realize the digital adaptive power distribution between the input branches of the Doherty PA. In view of that, a practical methodology was also proposed to fully linearize the dual-branch Doherty PA.

In the next chapter, the adaptive input power distribution concept will be shown to be instrumental in improving the bandwidth of Doherty PAs.
6.1 Introduction

Compared to linear power amplification classes, such as class A and class B modes, the Doherty power amplifier (PA) is an established technique that has been proven to provide significant enhancement in average efficiency. The efficiency enhancement of the Doherty architecture, however, drops rapidly when the frequency of operation of the Doherty PA deviates from the nominal design frequency. Such a bandwidth restriction originates mainly from the quarter-wavelength transmission lines of the output combining network and the frequency-dependent behavior of the active devices, which greatly compromises the convenience of Doherty PAs for multistandard applications [41–46].

This chapter introduces a new technique for extending the bandwidth of Doherty PAs in the digital domain. The digitally driven Doherty PA presented in this chapter allows preventing the efficiency degradation that naturally occurs as the frequency of operation deviates from the center frequency. This is achieved by controlling the input power distribution and the phase variation between the carrier and peaking amplifiers [52].

At first, the bandwidth extension capability of the digitally driven Doherty PA is demonstrated from a theoretical perspective. In particular, a set of generic equations is derived to illustrate its operation and assess its bandwidth. The experimental validation is
then carried out based on the dual-input Doherty PA architecture, which is adopted to enable the bandwidth enhancement in digital domain.

Henceforth, the terms Doherty PA and analog Doherty PA will be used interchangeably to designate a symmetrical Doherty PA that employs an analog input splitter with equal power division at all times. The term digital Doherty PA, on the other hand, indicates a Doherty PA in which the input signal splitting is performed in the digital domain.

6.2 Bandwidth Extension Analysis

The digital Doherty PA presented in this chapter employs a precompensation mechanism that acts on the input power distribution and the phase variation between the carrier and peaking amplifiers in order to overcome the bandwidth restrictions imposed by the quarter-wavelength transformers of the Doherty combining network and the frequency-dependent load modulation behavior. This precompensation function will be defined based on the enhanced current factors $\delta(f)$ and $\sigma(f)$, which are used herein to model the variation of the output current of the carrier amplifier and that of the peaking amplifier, respectively, in response to a variation in the injected input power, at a given frequency $f$.

In what follows, the expressions of $\delta(f)$ and $\sigma(f)$ are derived based on the operation of the Doherty PA with frequency-dependent components; and, the effectiveness of the digital Doherty PA in recovering the bandwidth is theoretically demonstrated. The analysis is carried out considering the following assumptions:

1. The carrier and peaking amplifiers operate in class B and class C modes, respectively.
2. Each current source is linearly proportional to the input drive voltage \(v_{in}\), as shown in Figure 6.1, and terminated with ideal harmonic short circuits so that the efficiency and the output power can be assessed using only the fundamental and direct current (DC) components.

3. The carrier and peaking amplifiers exhibit ideal bandwidth behaviour, i.e., the current sources generate the same fundamental and DC components at any frequency; and, the turn-on point of the peaking amplifier remains equal to \((V_{in,max}/2)\) at all frequencies \((V_{in,max}\) is the maximal input drive voltage).

![Figure 6.1 Fundamental currents of carrier and peaking amplifiers of the Doherty PA versus input voltage](image)

Figure 6.1 Fundamental currents of carrier and peaking amplifiers of the Doherty PA versus input voltage
6.2.1 Frequency Response Analysis at the Low Power Region

At the low power region \((0 \leq v_{in} \leq V_{in,\text{max}}/2)\), only the carrier amplifier is active. As such, the equivalent circuit diagram of the Doherty amplifier reduces to the carrier source operating into the impedance \(Z_C\), as shown in Figure 6.2. \(Z_C\) is resulting from the impedance transformation of the output load \(Z_0\) by means of two transmission lines having an electrical length of \(90^\circ\) at the center frequency \(f_0\) and characteristic impedances of \(Z_T/\sqrt{2} \approx 0.707Z_T\) and \(Z_T\), respectively.

![Figure 6.2 Equivalent circuit diagram of the Doherty PA at low power region](image)

Based on Figure 6.2, the output impedance of the carrier amplifier, \(Z_C\), at the low power region is given by:

\[
Z_C(f) = Z_T \cdot \frac{Z_L(f) + jZ_T \cdot \tan(\pi/2 \cdot f/f_0)}{Z_T + jZ_L(f) \cdot \tan(\pi/2 \cdot f/f_0)} 
\]  

(6.1)

where
and $Z_0$ is the optimal load of the carrier and peaking amplifiers. $Z_L$ is the impedance seen at the input of the transmission line that is connected to $Z_0$.

Figure 6.3 shows the variation of the real part of $Z_C$ versus $f$. It can be seen that $\text{real}\{Z_C(f)\}$ decreases rapidly from the optimal value of $2Z_0$ (at $f_0$) as the deviation from $f_0$ increases.

![Figure 6.3 Real part of $Z_C$ at low power region versus frequency](image)

$$Z_L(f) = \frac{Z_T}{\sqrt{2}} \cdot \left[ \frac{Z_0 + j \frac{Z_T}{\sqrt{2}} \cdot \tan(\pi/2 \cdot f/f_0)}{\frac{Z_T}{\sqrt{2}} + jZ_0 \cdot \tan(\pi/2 \cdot f/f_0)} \right]$$

(6.2)

$$Z_T = Z_0$$

(6.3)
The delivered radio frequency (RF) power of the Doherty PA ($P_{RF}$) at the low power region is related to $Z_C$ by:

$$P_{RF}(f) = \frac{1}{2} I_C^2 \cdot \text{real}(Z_C(f))$$  \hspace{1cm} (6.4)

where $I_C$ is the output RF current of the carrier amplifier at the low power region.

From (6.4), it is clear that the drop of $\text{real}(Z_C(f))$ induces a significant loss of output RF power; consequently, restricted efficiency improvement at back-off for $f \neq f_0$.

Figure 6.4, on the other hand, shows that $P_{RF}$ degrades by 14%, 26%, and 38% (with respect to the maximal level at the center frequency $f_0$) when $f$ deviates by $\pm 0.10 f_0$, $\pm 0.15 f_0$, and $\pm 0.20 f_0$, respectively. The normalized output power reported in Figure 6.4 is obtained based on the ratio $(P_{RF}(f)/P_{RF}(f_0))$, which is evaluated using (6.1)–(6.4) and found to be equal to $(\text{real}(Z_C(f))/2Z_0)$. 

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Ideally, a perfect Doherty combining network transforms $Z_0$ to $2Z_0$ at all frequencies. In this case, $P_{RF}(f)$ is identically equal to $P_{RF}(f_0)$. Introducing the enhanced current factor of the digital Doherty PA ($\delta$) as [52]:

$$\delta(f) = \frac{P_{RF}(f_0)}{\sqrt{P_{RF}(f)}} = \frac{2Z_0}{\sqrt{\text{real}[Z_C(f)]}}$$  \hspace{1cm} (6.5)$$

and expressing the fundamental RF current of the carrier amplifier of the digital Doherty PA ($I_{C,dig}$) as [52]:

---

The figure shows the normalized output power of the Doherty PA at low power region versus frequency. The graph illustrates how the output power changes with normalized frequency, $f/f_0$, and highlights the efficiency and performance characteristics of the Doherty PA in this low power regime.
\[ I_{C,\text{dig}}(f) = \delta(f) \cdot I_C \]  \hspace{1cm} (6.6)

Then, using (6.5) and (6.6), the delivered RF power of the digital Doherty PA \( P_{RF,\text{dig}} \) is given by:

\[
P_{RF,\text{dig}}(f) = \frac{1}{2} I_{C,\text{dig}}^2(f) \cdot \text{real}\{Z_C(f)\} = \frac{1}{2} \delta(f)^2 \cdot I_C^2 \cdot \text{real}\{Z_C(f)\}
\]

\[
= \frac{1}{2} \cdot \frac{2Z_0}{\text{real}\{Z_C(f)\}} \cdot I_C^2 \cdot \text{real}\{Z_C(f)\} = I_C^2 \cdot Z_0 = P_{RF}(f_0)
\]  \hspace{1cm} (6.7)

Therefore, in theory, the digital Doherty PA with non-ideal quarter-wavelength transformers can mimic the operation of a Doherty PA with an ideal output combining network as it can deliver \( P_{RF}(f_0) \) for \( f \neq f_0 \). Referring to (5.26) and (5.27) in Chapter Five, such a performance is achieved provided that the available input power of the Doherty PA \( P_{in} \) is distributed as follows:

\[
P_{in,C}(f) = \frac{\delta(f)^2}{2} \cdot P_{in}
\]  \hspace{1cm} (6.8)

\[
P_{in,P}(f) = \left(1 - \frac{\delta(f)^2}{2}\right) \cdot P_{in}
\]  \hspace{1cm} (6.9)

Where \( P_{in,C} \) and \( P_{in,P} \) denote the input powers injected into the carrier and peaking branches, respectively.

Figure 6.5 depicts the variation of \( \delta \) versus \( f \). It is noted that \( \delta(f) \) increases from 1 at \( f_0 \) (i.e., \( \text{real}\{Z_C\} = 2Z_0 \)) to \( \sqrt{2} \) at \( f = f_0 \pm 0.27f_0 \) (i.e., \( \text{real}\{Z_C\} = Z_0 \)). Likewise, Figure 6.6 shows that \( P_{in,C}(f) \) increases from \( (P_{in}/2) \) at \( f_0 \) (i.e., \( \delta = 1 \)) to \( (P_{in}) \) at \( f = f_0 \pm 0.27f_0 \) (i.e., \( \delta = \sqrt{2} \)).
Figure 6.5 Variation of $\delta$ versus frequency

Figure 6.6 Input power distribution between carrier and peaking branches versus frequency
The uneven drive splitting with higher power into the carrier branch allows compensating for the loss of RF output power due to the drop of real\(\{Z_C(f)\}\), which results in improving the efficiency of the Doherty PA for \(f \neq f_0\).

By using (6.4), the efficiency of the analog Doherty PA (\(\eta\)) at back-off can be calculated as:

\[
\eta(f) = \frac{P_{RF}(f)}{P_{DC}} = \frac{\frac{1}{2}I_C^2 \cdot \text{real}\{Z_C(f)\}}{I_{DC,C} \cdot V_{DC}} \tag{6.10}
\]

where \(P_{DC}\) is the dissipated DC power of the Doherty PA at the low power region, which is given by the product of the DC current of the carrier amplifier \(I_{DC,C}\) and the drain supply voltage \(V_{DC}\).

Similarly, by using (6.7) and (6.10), the efficiency of the digital Doherty PA (\(\eta_{\text{dig}}\)) at back-off is demonstrated to be:

\[
\eta_{\text{dig}}(f) = \frac{P_{RF,\text{dig}}(f)}{P_{DC,\text{dig}}(f)} = \frac{\frac{1}{2} \delta(f)^2 \cdot I_C^2 \cdot \text{real}\{Z_C(f)\}}{\delta(f) \cdot I_{DC,C} \cdot V_{DC}} = \frac{\frac{1}{2} I_C^2 \cdot \text{real}\{Z_C(f)\}}{I_{DC,C} \cdot V_{DC}} = \delta(f) \cdot \eta(f) \tag{6.11}
\]

where \(P_{DC,\text{dig}}\) is the dissipated DC power of the digital Doherty PA at the low power region, which is given by the product of \(\delta(f)\), \(I_{DC,C}\) and \(V_{DC}\).

From (6.11), the normalized efficiency of the digital Doherty PA (\(\xi_{\text{dig}}\)) at back-off can be written as:

\[
\xi_{\text{dig}}(f) = \frac{\eta_{\text{dig}}(f)}{\eta_{\text{dig}}(f_0)} = \frac{\delta(f) \cdot \eta(f)}{\delta(f_0) \cdot \eta(f_0)} = \frac{\eta(f)}{\eta(f_0)} = \frac{\eta(f)}{f_0} \cdot \xi(f) \tag{6.12}
\]
where \( \xi \) is recognized as the normalized efficiency of the analog Doherty PA, which can be evaluated from (6.1)–(6.3), and (6.10) as:

\[
\xi(f) = \frac{\eta(f)}{\eta(f_0)} = \frac{\text{real}[Z_C(f)]}{2Z_0}.
\] (6.13)

Figure 6.6 depicts the variations of \( \xi \) and \( \xi_{\text{dig}} \) versus \( f \), which are computed using (6.12) and (6.13), respectively. In theory, the analog Doherty PA can achieve a fractional bandwidth of 16\% at the cost of 10\% efficiency degradation. The digital Doherty PA, on the other hand, achieves a 24\% bandwidth for the same efficiency degradation, which corresponds to a relative improvement of 50\%.

![Figure 6.7 Normalized efficiency of the analog and digital Doherty PAs at low power region versus frequency](image-url)
6.2.2 Frequency Response Analysis at the High Power Region

At the high power region \((V_{in,max}/2 \leq v_{in} \leq V_{in,max})\), the carrier and peaking amplifiers are both active. As depicted in Figure 6.8, the equivalent circuit diagram of the Doherty PA consists of the carrier and peaking sources, which are operating into the common load \((Z_L)\).

![Equivalent circuit diagram of the Doherty PA at high power region](image)

**Figure 6.8 Equivalent circuit diagram of the Doherty PA at high power region**

The fundamental RF currents of the carrier and peaking amplifiers of the Doherty PA at peak power are given by [52]:

\[
I_C = I_{C,max} \quad \text{(6.14)}
\]

\[
I_P = I_{P,max} \cdot e^{-j(\pi/2)/f_0} \quad \text{(6.15)}
\]

where \(I_{C,max}\) and \(I_{P,max}\) \((I_{P,max} \leq I_{C,max})\) designate the output RF currents of the carrier and peaking amplifiers at peak power, respectively.
The lower fundamental RF current of the peaking amplifier and the frequency-selective behavior of the Doherty combining network impair the load modulation mechanism and degrades the efficiency of the Doherty PA [52].

Introducing the enhanced current factor ($\sigma$) required to ensure the ideal load modulation behavior in the digital Doherty PA as [52]:

$$\sigma(f) = \frac{I_{P,\text{dig}}(f)}{I_P}$$

(6.16)

where $I_{P,\text{dig}}$ is the fundamental RF current of the peaking amplifier of the digital Doherty PA, then the purpose of the following is to derive an explicit expression of $\sigma$ versus $f$, in order to evaluate the performance of the digital Doherty PA and compare it with that of the analog Doherty PA.

Starting from the ABCD matrix of the quarter-wavelength transformer with the characteristic impedance $Z_T$ and referring to Figure 6.8, one can write [52]:

$$V_C = \cos(\pi/2 \cdot f/f_0) \cdot V_{C,T}(f) + jZ_T \cdot \sin(\pi/2 \cdot f/f_0) \cdot I_{C,T}(f)$$

(6.17)

$$I_C = j \frac{1}{Z_T} \cdot \sin(\pi/2 \cdot f/f_0) \cdot V_{C,T}(f) + \cos(\pi/2 \cdot f/f_0) \cdot I_{C,T}(f)$$

(6.18)

Also, based on Figure 6.8, the following expressions arise:

$$V_{C,T}(f) = Z_{C,T}(f) \cdot I_{C,T}(f)$$

(6.19)

$$Z_{C,T}(f) = Z_L(f) \cdot \left[ 1 + \frac{I_P}{I_{C,T}(f)} \right]$$

(6.20)
Substituting $Z_{C,T}$ in (6.19) with its expression (6.20) results in:

$$V_{C,T}(f) = Z_L(f) \cdot (I_{C,T}(f) + I_P)$$ \hspace{1cm} (6.21)

where $Z_L$ is given by (6.2).

Rearranging (6.18) for an expression of $I_{C,T}$ while accounting for (6.21) gives:

$$I_{C,T}(f) = \frac{I_C - j \frac{Z_L(f)}{Z_T} \cdot \sin(\pi/2 \cdot f/f_0) \cdot I_P}{\cos(\pi/2 \cdot f/f_0) + j \frac{Z_L(f)}{Z_T} \cdot \sin(\pi/2 \cdot f/f_0)}$$ \hspace{1cm} (6.22)

To guarantee the ideal load modulation behavior in the digital Doherty PA, the peak power impedance seen by the carrier amplifier ($Z_C$) and that seen by the peaking amplifier ($Z_P$) should be equal to $Z_0$ at all frequencies. This intent is achieved by satisfying the necessary and sufficient condition given by:

$$Z_L(f) \cdot \left[1 + \frac{I_{P,dig}(f)}{I_{C,T,dig}(f)}\right] \equiv Z_L(f) \cdot \left[1 + \frac{\sigma(f) \cdot I_P}{I_{C,T,dig}(f)}\right] = Z_0$$ \hspace{1cm} (6.23)

where $I_{C,T,dig}$ is deduced from (6.22) as:

$$I_{C,T,dig}(f) = \frac{I_C - j \frac{Z_L(f)}{Z_T} \cdot \sin(\pi/2 \cdot f/f_0) \cdot \sigma(f) \cdot I_P}{\cos(\pi/2 \cdot f/f_0) + j \frac{Z_L(f)}{Z_T} \cdot \sin(\pi/2 \cdot f/f_0)}.$$ \hspace{1cm} (6.24)

Thus, using (6.14), (6.15) and (6.24), the enhanced current factor of the digital Doherty PA ($\sigma$) is explicitly obtained from (6.23) as:

$$\sigma(f) = \frac{I_C}{I_P} \cdot e^{j(\pi/2 \cdot f/f_0)} \cdot \frac{Z_0 - Z_L(f)}{Z_L(f)} = \frac{I_{C,max}}{I_{P,max}} \cdot \frac{Z_0 - Z_L(f)}{Z_L(f)} = \sigma_0 \cdot \frac{Z_0 - Z_L(f)}{Z_L(f)}$$ \hspace{1cm} (6.25)
where \( \sigma_0 (\sigma_0 \geq 1) \) is recognized as the enhanced current ratio of the uneven and the asymmetrical Doherty PAs [32, 33], which is given by the ratio of the peak power RF current of the carrier amplifier \((I_{C,\text{max}})\) to the peak power RF current of the peaking amplifier \((I_{P,\text{max}})\) at \( f_0 \).

It is noteworthy that the design parameter \( \sigma_0 \) indicates the bias point of the peaking device. Indeed, the higher \( \sigma_0 \), the deeper the class C bias of the peaking amplifier. Conversely, operating the peaking amplifier at class B mode results in \( \sigma_0 \) equal to 1.

Figure 6.9 shows the variation of the magnitude and phase of \( \sigma \) versus \( f \). It can be noted that \(|\sigma(f)|\) decreases from \( \sigma_0 \) at \( f_0 \) to \( 0.84\sigma_0 \) at \( f = f_0 \pm 0.27f_0 \). Therefore, the uneven drive power into the peaking path is relaxed as \( f \) deviates from \( f_0 \). In addition, the phase response of the peaking amplifier should be adjusted for \( f \neq f_0 \), in order to ensure that (6.23) is strictly fulfilled at any frequency.
Figure 6.9 Variation of $\sigma$ versus frequency: (a) magnitude; (b) phase
Based on Figure 6.8, the real RF power of the digital Doherty PA \( P_{RF,dig} \) at full drive can be expressed as:

\[
P_{RF,dig}(f) = \frac{1}{2} \left| I_{C,T,dig}(f) + I_{P,dig}(f) \right|^2 \cdot \text{real}\{Z_L(f)\}
\]

\[
= \frac{1}{2} \left| I_{C,T,dig}(f) + \sigma(f) \cdot I_P \right|^2 \cdot \text{real}\{Z_L(f)\}
\]

By using (6.24) and (6.25), \( P_{RF,dig} \) can be written as:

\[
P_{RF,dig}(f) = \frac{1}{2} |\Lambda(f)|^2 \cdot |I_C|^2 \cdot \text{real}\{Z_L(f)\}
\]

where

\[
\Lambda(f) = \frac{1 - \frac{Z_0 - Z_L(f)}{Z_L(f)} \cdot e^{-j(\pi/2)} \cdot \sin(\pi/2 \cdot f/f_0)}{\cos(\pi/2 \cdot f/f_0) + \frac{Z_L(f)}{Z_T} \cdot \sin(\pi/2 \cdot f/f_0)} + \frac{Z_0 - Z_L(f)}{Z_L(f)} \cdot e^{-j(\pi/2)}
\]

From (6.27) and (6.28), the normalized output power of the digital Doherty PA \( P_{dig} \) can be explicitly expressed as:

\[
P_{dig}(f) = \frac{P_{RF,dig}(f)}{P_{RF,dig}(f_0)} = \frac{1}{4} \left| \Lambda(f) \right|^2 \cdot |I_C|^2 \cdot \text{real}\{Z_L(f)\} = \frac{\text{real}\{Z_L(f)\}}{2Z_0} \cdot |\Lambda(f)|^2
\]

Besides, the real RF power of the Doherty PA \( P_{RF} \) at peak power is given by:

\[
P_{RF}(f) = \frac{1}{2} \left| I_{C,T}(f) + I_P \right|^2 \cdot \text{real}\{Z_L(f)\}
\]

Considering that, \( I_C \) and \( I_P \) can be related by using (6.14), (6.15) and (6.25) as:
\[
I_p = \frac{I_c \cdot e^{-j(\pi/2)\cdot f/f_0}}{\sigma_0} \quad (6.31)
\]

then, based on (6.22) (6.30) and (6.31), \( P_{RF} \) can be expressed as:

\[
P_{RF}(f) = \frac{1}{2} |Y(f)|^2 \cdot |I_c|^2 \cdot \text{real}\{Z_L(f)\} \quad (6.32)
\]

where

\[
Y(f) = \frac{1 + \frac{1}{\sigma_0} \cdot \cos(\pi/2 \cdot f/f_0) \cdot e^{-j(\pi/2)\cdot f/f_0}}{\cos(\pi/2 \cdot f/f_0) + j \frac{Z_L(f)}{Z_T} \cdot \sin(\pi/2 \cdot f/f_0)} \quad (6.33)
\]

From (6.32) and (6.33), the normalized output power of the Doherty PA \( (P) \) can be explicitly expressed as:

\[
P(f) = \frac{P_{RF}(f)}{P_{RF}(f_0)} = \frac{1}{2} |Y(f)|^2 \cdot |I_c|^2 \cdot \text{real}\{Z_L(f)\} = \frac{\text{real}\{Z_L(f)\}}{2Z_0} \cdot |Y(f)|^2 \quad (6.34)
\]

Figure 6.10 depicts the variations of \( P_{\text{dig}} \) and \( P \) versus \( f \), which are calculated based on (6.29) and (6.34), respectively. The results confirm that the digital Doherty PA permits significant boost of output RF power for \( f \neq f_0 \). In addition, it can be noted that the output power degradation in the analog Doherty PA is more severe for deep class C operation of its peaking amplifier.
By using (6.27), the efficiency of the digital Doherty PA ($\eta_{\text{dig}}$) at peak power can be written as:

$$
\eta_{\text{dig}}(f) = \frac{P_{\text{RF,dig}}(f)}{P_{\text{DC,dig}}(f)} = \frac{1}{2} |\Lambda(f)|^2 \cdot |I_C|^2 \cdot \text{real}[Z_L(f)]}{\left( I_{\text{DC,C}} + \text{real}[\sigma(f)] \cdot I_{\text{DC,P}} \right) \cdot V_{\text{DC}}}
$$

(6.35)

where $I_{\text{DC,C}}$ and $I_{\text{DC,P}}$ are the peak power DC currents of the carrier and peaking amplifiers, respectively. $P_{\text{DC,dig}}$ is the dissipated DC power of the digital Doherty PA at peak power, which is given by the product, \((I_{\text{DC,C}} + \text{real}[\sigma(f)] \cdot I_{\text{DC,P}}) \times V_{\text{DC}}\).
Assuming that $I_{DC,P}$ at peak power can be approximated by:

$$I_{DC,P} \approx \frac{I_{DC,C}}{\sigma_0}$$  \hspace{1cm} (6.36)

then, by using (6.25), (6.35) and (6.36), $\eta_{\text{dig}}$ can be expressed as:

$$\eta_{\text{dig}}(f) = \frac{1}{2} |\Lambda(f)|^2 \cdot |I_C|^2 \cdot \text{real}[Z_L(f)]}{\left(1 + \text{real}\left\{\frac{Z_0 - Z_L(f)}{Z_L(f)}\right\}\right) \cdot I_{DC,C} \cdot V_{DC}}$$  \hspace{1cm} (6.37)

From (6.28) and (6.37), the normalized peak power efficiency of the digital Doherty PA ($\xi_{\text{dig}}$) is explicitly given by:

$$\xi_{\text{dig}}(f) = \frac{\eta_{\text{dig}}(f)}{\eta_{\text{dig}}(f_0)} = \frac{|\Lambda(f)|^2 \cdot \text{real}[Z_L(f)]}{\left(1 + \text{real}\left\{\frac{Z_0 - Z_L(f)}{Z_L(f)}\right\}\right) \cdot Z_0}$$  \hspace{1cm} (6.38)

Besides, from (6.32), the efficiency of the analog Doherty PA ($\eta$) at peak power can be expressed as:

$$\eta(f) = \frac{P_{RF}(f)}{P_{DC}(f)} = \frac{1}{2} |Y(f)|^2 \cdot |I_C|^2 \cdot \text{real}[Z_L(f)]}{(I_{DC,C} + I_{DC,P}) \cdot V_{DC}}$$  \hspace{1cm} (6.39)

where $P_{DC}$ is the dissipated DC power of the analog Doherty PA at peak power, which is given by the product, $(I_{DC,C} + I_{DC,P}) \times V_{DC}$.

By using (6.33) and (6.39), the normalized peak power efficiency of the analog Doherty PA ($\xi$) is expressed as:

$$\xi(f) = \frac{\eta(f)}{\eta(f_0)} = \frac{\text{real}[Z_L(f)]}{2Z_0} \cdot |Y(f)|^2$$  \hspace{1cm} (6.40)
Figure 6.11 shows the variations of $\xi_{\text{dig}}$ and $\xi$ versus $f$, which are obtained from (6.38) and (6.40), respectively. The results show that, regardless of the bias condition of the peaking device, the digital Doherty PA is capable of maintaining the maximal efficiency $\eta(f_0)$ for $f \neq f_0$. This result is not surprising because the digital amplifier is designed to ensure that the carrier and peaking amplifiers are operating into the optimal impedance, $Z_0$, at all frequencies.

Figure 6.11 Normalized efficiency of the analog and digital Doherty PAs at peak power versus frequency
6.3 Experimental Validation

In the previous section, it was theoretically demonstrated that the digital Doherty PA allows for significantly improved bandwidth compared to the analog Doherty PA. In this section, the bandwidth extension capability of the digital Doherty PA is experimentally established.

The experiments are carried out based on the analog Doherty PA prototype that was presented in the previous chapter. This PA prototype was nominally designed to operate at 2.14 GHz for downlink Wideband Code Division Multiple Access (WCDMA) band and implemented using 10-Watt CGH40010 gallium nitride (GaN) transistor from Cree Inc. The carrier amplifier and peaking amplifier are biased in class AB (gate voltage, $V_{GS} = -2.1$ V, drain voltage, $V_{DS} = 28$ V, and quiescent current, $I_{DQ} = 200$ mA) and class C ($V_{GS} = -4$ V, $V_{DS} = 28$ V, and $I_{DQ} = 0$) modes, respectively. The implementation procedure of the dual-input digital Doherty PA based on the single-input analog PA is performed by eliminating input analog splitter and isolating the input paths of the dual-input PA.

The block diagram of the proof-of-concept setup of the digital Doherty PA is reported in Figure 6.12. The baseband streams ($I/Q)_{\text{Carrier}}$ and ($I/Q)_{\text{Peaking}}$ are tailored in digital domain according to the carrier frequency ($f_c$) of the input signal ($I/Q)_{\text{In}}$ and downloaded into two synchronized arbitrary waveform generators (AWGs), ESG-4438C from Agilent Technologies Inc. The experimental validation is conducted over a frequency range of 500 MHz (1.96 GHz $\leq f \leq$ 2.46 GHz) where the analog Doherty PA prototype has acceptable suboptimal performance in terms of efficiency, output power and gain.
Figure 6.12 Experimental setup of the digital Doherty PA with frequency-dependent signal separation

6.3.1 Continuous Wave Measurement Results

Figure 6.12 depicts the variations of the enhanced current factors $\delta$ and $\sigma$ as function of the frequency. It can be noted that $\delta$ follows the theoretical tendency that is reported in Figure 6.5. Indeed, the overdrive power into the carrier path at back-off is increased gradually when the deviation from the design frequency, 2.14 GHz, increases in order to compensate for the RF power loss due to the frequency response of the carrier branch.

However, due to the nonideal bandwidth behavior of the carrier and peaking amplifiers of the prototype under test, the analytically derived response of $\sigma$ cannot be applied as is. The phase disparity (related to the phase of $\sigma$ through (6.25)) between the carrier and peaking paths and the overdrive power into the peaking branch at high power region (related to the magnitude of $\sigma$ through (6.25)) were derived experimentally at each frequency using continuous wave (CW) measurements to maximize the peak power performance. For instance, referring to Figure 6.13, the optimal value of $\sigma$ at 2.04 GHz is found to be equal to $1.03 \angle -10^\circ$. This means that the best performance at peak power is
achieved by ensuring that 1) the input signal of the peaking amplifier is lagging behind that of the carrier amplifier by $-10 + 90 \times (2.04/2.14) = -75.8^\circ$, as inferred from (6.16); and, 2) the peaking amplifier is driven with $10 \log_{10} [1.03^2/(2 - 1.03^2)] = 0.53$ dB higher power compared to the carrier amplifier, as inferred from (5.28) in Chapter 5.

Figure 6.13 Variation of $\delta$ and $\sigma$ versus frequency for the digital Doherty PA prototype
Figure 6.14 shows the measured drain efficiency of the analog Doherty PA and that of the digital Doherty PA at 6~7 dB output power back-off (OPBO) and at peak power. It can be seen that the digital Doherty amplifier enables important bandwidth improvement. Indeed, its measured drain efficiency at 6~7 dB OPBO is higher than 40% throughout the frequency range spanning from 1.96 to 2.46 GHz. Such performance is achievable only from 2.04 to 2.22 GHz using the fully analog Doherty PA. Hence, the bandwidth is enhanced from 180 to 500 MHz, which corresponds to an increase by a factor of 2.8.

Figure 6.14 Measured efficiency of the analog and digital Doherty PAs versus frequency
The performance in terms of small signal gain (SSG) and saturated output power \( (P_{\text{sat}}) \) of the analog and digital Doherty PAs is reported in Figure 6.15. The digital Doherty PA has higher SSG and \( P_{\text{sat}} \), due to the digital control of input power and phase variation between the carrier and peaking branches.

![Figure 6.15 Measured SSG and \( P_{\text{sat}} \) of the analog and digital Doherty PAs versus frequency](image)

To further explore the performance of the Doherty PAs under test, Figure 6.16 depicts the measured gain and efficiency characteristics of analog and digital Doherty PAs at several frequencies within the operation band.
Figure 6.16 Measured gain and drain efficiency of analog and digital Doherty PAs
6.3.2 Modulated Signal Measurement Results

To verify the suitability of the digital Doherty amplifier for multistandard wireless communications, three modulated signals of WCDMA, Long Term Evolution (LTE), and Worldwide Interoperability for Microwave Access (WiMAX) standards are employed. The peak-to-average power ratios (PAPRs) of the signals are 7.04, 7.18 and 7.31 dB, respectively.

When driven with the WCDMA signal at 1.98 GHz, the digital Doherty PA achieved a drain efficiency of 40.1% at 7 dB OPBO versus 37% for the analog Doherty PA. Besides, using the 2.22 GHz LTE signal, a drain efficiency of 44.2% is measured for the digital Doherty PA against 37.3% for the analog Doherty PA. At 2.34 GHz, the digital Doherty PA exhibited an efficiency of 41.4% at 7 dB OPBO using the WiMAX signal. The efficiency of the analog Doherty PA, on the other hand, is limited to 35.2% under identical drive conditions. The measurement results for the modulated signal tests are summarized in Table I.

The measured output spectra of the analog and digital Doherty PAs for the modulated signal tests at 1.98, 2.22 and 2.34 GHz are reported in Figure 6.17. It can be deduced that the digital Doherty PA has an acceptable linearity that can be enhanced to meet the spectrum mask specifications of each standard by using the digital predistortion (DPD) technique based on the linearization procedure that was reported in the previous chapter.
Table 6.1 Measured Performance of the Symmetrical and Digital Doherty PAs Using Modulated Signals

<table>
<thead>
<tr>
<th>5 MHz Bandwidth 7.04 dB PAPR WCDMA Signal at 1.98 GHz</th>
<th>Gain</th>
<th>Output Power</th>
<th>Drain efficiency</th>
<th>*ACPR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Doherty PA</td>
<td>12 dB</td>
<td>35.88 dBm</td>
<td>37.02%</td>
<td>−35 dBc</td>
</tr>
<tr>
<td>Digital Doherty PA</td>
<td>12.4 dB</td>
<td>36.28 dBm</td>
<td>40.13%</td>
<td>−30 dBc</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>5 MHz Bandwidth 7.18 dB PAPR LTE Signal at 2.22 GHz</th>
<th>Gain</th>
<th>Output Power</th>
<th>Drain efficiency</th>
<th>*ACPR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Doherty PA</td>
<td>13.32 dB</td>
<td>37.14 dBm</td>
<td>37.29%</td>
<td>−30 dBc</td>
</tr>
<tr>
<td>Digital Doherty PA</td>
<td>14.02 dB</td>
<td>37.84 dBm</td>
<td>44.17%</td>
<td>−27 dBc</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>5 MHz Bandwidth 7.36 dB PAPR WiMAX Signal at 2.34 GHz</th>
<th>Gain</th>
<th>Output Power</th>
<th>Drain efficiency</th>
<th>*ACPR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Doherty PA</td>
<td>13.41 dB</td>
<td>37.07 dBm</td>
<td>35.20%</td>
<td>−24 dBc</td>
</tr>
<tr>
<td>Digital Doherty PA</td>
<td>13.64 dB</td>
<td>37.3 dBm</td>
<td>41.38%</td>
<td>−24 dBc</td>
</tr>
</tbody>
</table>

*ACPR: adjacent channel power ratio measured at 5 MHz offset.
Figure 6.17 Measured output spectra of the analog and digital Doherty PAs
6.4 Conclusion

This chapter presented a new method for extending the bandwidth of Doherty PAs in the digital domain. The bandwidth enhancement is achieved through a frequency-selective precompensation mechanism that was implemented to prevent the efficiency degradation that occurs as the frequency of operation deviates from the nominal design frequency of the Doherty PA, enforcing the RF front-end to operate efficiently throughout a wide frequency range that is significantly larger than its nominal bandwidth. Precisely, the bandwidth restrictions imposed by the analog building blocks of the Doherty PA were mitigated by digitally controlling the input power distribution and the phase variation between the carrier and peaking amplifiers.

By applying the proposed methodology, a Doherty PA that was originally designed at 2.14 GHz for downlink WCDMA has became operative at 1.98 GHz uplink WCDMA, 2.22 GHz LTE, and 2.34 GHz WiMAX bands. The nominal bandwidth of this Doherty PA was extended from 180 to 500 MHz, which represents an increase of approximately 180% in bandwidth.

In the next chapter, the proposed bandwidth extension methodology will be shown to be crucial to the implementation of an advanced digitally equalized Doherty PA that is suitable for power amplification of very wide bandwidth (≥ 20 MHz) RF signals.
Chapter Seven: Digitally Equalized Doherty Power Amplifier Architecture

7.1 Introduction

This chapter presents a new architecture of digitally equalized Doherty power amplifier (PA). This architecture incorporates a digital baseband equalizer that is implemented to enable high efficiency power amplification of broadband and multichannel radio frequency (RF) signals using Doherty PAs. Furthermore, the baseband equalizer makes it possible to efficiently operate the Doherty PA beyond its nominal frequency band, which is suitable for cognitive and software defined radio applications [53].

In principle, the specifications of such an equalizer are determined by the frequency response of the Doherty PA and the strategy of mitigation of its bandwidth limitations. These two aspects were thoroughly studied in the previous chapter, where it was established that a substantial extension in bandwidth is achievable provided that the input power is adaptively distributed between the carrier and peaking amplifiers according to an optimal frequency-dependent power distribution scheme.

In this perspective, the main role of the equalization system introduced in this chapter is the execution of the optimal signal separation at each frequency component of the transmit signal. As such, the digitally equalized Doherty PA should enable the RF front-end to support wider bandwidth signals as well as multiple radios within its extended bandwidth. This expands upon the methodology reported in the previous chapter, where the appropriate signal distribution was implemented selectively at discrete points depending on the RF frequency of the carrier signal.
In the next section, the functional blocks and the frequency domain specifications of the proposed baseband equalizer are presented. Then, the efficiency performance of the digitally-equalized Doherty PA is analyzed. Afterwards, the computation burden of the baseband equalizer is evaluated and its digital signal processing (DSP) resource utilization is benchmarked against that of a state-of-the-art digital predistorter. After that, the practical implementation of the digitally equalized Doherty PA architecture is described and its measured performance is discussed.

7.2 Adaptive Baseband Equalization Methodology

Figure 7.1 shows the system diagram of the digitally equalized Doherty PA [53]. It encompasses a baseband equalizer, a signal up-conversion block and a dual-input Doherty PA. In operation, the baseband equalizer takes the input baseband waveform \( x(n) \) and generates the baseband waveforms \( x_c(n) \) and \( x_p(n) \) that are feeding the carrier branch and the peaking branch, respectively.

Figure 7.1 Block diagram of the digitally equalized Doherty PA
In what follows, the functional blocks of the baseband equalizer are presented and its frequency domain specifications are derived. For simplicity sake, the classical assumption of class B operation of the carrier and peaking amplifiers is considered in this study [7, 3, 44].

7.2.1 Optimal Input Power Distribution Profile

As discussed in the previous chapter, due to the frequency-dependent behaviour of the analog building blocks of the Doherty PA, the power efficiency drops significantly as the frequency of operation \( f \) shifts away from the nominal design frequency \( f_0 \). Referring to (6.8), (6.9), and (6.25) in Chapter Six, this limitation can be mitigated on condition that the available input power of the Doherty PA (\( P_{in} \)) is distributed between the carrier and peaking branches according to the optimal scheme given by [53]:

\[
P_{in,C}(f, P_{in}) = \begin{cases} \frac{Z_0}{\text{real}\{Z_C(f)\}} \cdot P_{in}, & P_{in} < P_{in,max}/4 \\ \left(1 - \frac{1}{2} \cdot \left[\frac{Z_0 - Z_L(f)}{Z_L(f)}\right]^2\right) \cdot P_{in}, & P_{in} \geq P_{in,max}/4 \end{cases} \quad (7.1)
\]

\[
P_{in,P}(f, P_{in}) = \begin{cases} \left(1 - \frac{Z_0}{\text{real}\{Z_C(f)\}}\right) \cdot P_{in}, & P_{in} < P_{in,max}/4 \\ \frac{1}{2} \cdot \left[\frac{Z_0 - Z_L(f)}{Z_L(f)}\right]^2 \cdot P_{in}, & P_{in} \geq P_{in,max}/4 \end{cases} \quad (7.2)
\]

where

\[
Z_C(f) = Z_T \cdot \frac{Z_L(f) + jZ_T \cdot \tan(\pi/2 \cdot f/f_0)}{Z_T + jZ_L(f) \cdot \tan(\pi/2 \cdot f/f_0)} \quad (7.3)
\]
and $P_{in,C}$ and $P_{in,P}$ denote the input powers delivered to the carrier and peaking amplifiers, respectively. $P_{in,max}$ is the maximal power level of the input signal and $(P_{in,max}/4)$ is the input power level corresponding to the turn-on point of the peaking amplifier of the symmetrical Doherty PA. As depicted in Figure 7.1, $Z_C$ is the impedance of the carrier amplifier and $Z_L$ is the impedance seen at the input of the quarter-wavelength transmission line that is connected to the output load $Z_0$.

The variations of $P_{in,C}$ and $P_{in,P}$ versus $f$ and $P_{in}$ are reported in Figure 7.2. Based on Figure 7.2(a), it can be seen that the power supplied to the carrier amplifier should be increased rapidly from $(P_{in}/2)$ at $f_0$ to $P_{in}$ at $f = f_0 \pm 0.27f_0$, for $P_{in} < P_{in,max}/4$. Conversely, for $P_{in} \geq P_{in,max}/4$, the power supplied to the carrier amplifier has to be gradually increased from $(P_{in}/2)$ at $f_0$ to slightly higher than $(P_{in}/2)$ at $f = f_0 \pm 0.27f_0$.

Figure 7.2(b), on the other hand, shows that the power supplied to the peaking amplifier should be decreased from $(P_{in}/2)$ at $f_0$ to zero at $f = f_0 \pm 0.27f_0$, for $P_{in} < P_{in,max}/4$. Subsequently, when $P_{in} \geq P_{in,max}/4$, the power supplied to the input branch of the peaking amplifier has to be gradually decreased from $(P_{in}/2)$ at $f_0$ to slightly lower than $(P_{in}/2)$ at $f = f_0 \pm 0.27f_0$. 

\[ Z_L(f) = \frac{Z_T}{\sqrt{2}} \left[ \frac{Z_0 + j \frac{Z_T}{\sqrt{2}} \cdot \tan(\pi/2 \cdot f/f_0)}{Z_0 + j Z_0 \cdot \tan(\pi/2 \cdot f/f_0)} \right] \]  

(7.4)
Figure 7.2 Optimal input power distribution profile: (a) carrier path; (b) peaking path
### 7.2.2 Specifications of the Digital Baseband Equalizer

In theory, for a given input RF signal having a bandwidth (BW) and centered on a carrier frequency $f_{RF}$, the optimal power distribution expressed in (7.1) and (7.2) can be performed through two analog bandpass filters $A_C(f, P_{in})$ (for the carrier branch) and $A_P(f, P_{in})$ (for the peaking branch), the frequency responses of which are derived from (7.1) and (7.2) according to [53]:

$$A_C(f, P_{in}) = \begin{cases} 
A_C^{1}(f), & P_{in} < P_{in,max}/4 \\
A_C^{2}(f), & P_{in} \geq P_{in,max}/4 
\end{cases} \quad (7.5)$$

$$A_P(f, P_{in}) = \begin{cases} 
A_P^{1}(f), & P_{in} < P_{in,max}/4 \\
A_P^{2}(f), & P_{in} \geq P_{in,max}/4 
\end{cases} \quad (7.6)$$

where

$$A_C^{1}(f) = \begin{cases} 
0, & f < f_{RF} - BW/2 \\
\frac{Z_0}{\text{real}[Z_C(f)]}, & f_{RF} - BW/2 \leq f \leq f_{RF} + BW/2 \\
0, & f > f_{RF} + BW/2 
\end{cases} \quad (7.7)$$

$$A_C^{2}(f) = \begin{cases} 
0, & f < f_{RF} - BW/2 \\
1 - \frac{1}{2} \left( \frac{Z_0 - Z_L(f)}{Z_L(f)} \right)^2, & f_{RF} - BW/2 \leq f \leq f_{RF} + BW/2 \\
0, & f > f_{RF} + BW/2 
\end{cases} \quad (7.8)$$

$$A_P^{1}(f) = \begin{cases} 
0, & f < f_{RF} - BW/2 \\
\frac{Z_0}{\text{real}[Z_C(f)]}, & f_{RF} - BW/2 \leq f \leq f_{RF} + BW/2 \\
0, & f > f_{RF} + BW/2 
\end{cases} \quad (7.9)$$

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$$A_{P_2}(f) = \begin{cases} 
0, & f < f_{RF} - BW/2 \\
\frac{1}{2} \cdot \left| \frac{Z_0 - Z_L(f)}{Z_L(f)} \right|^2, & f_{RF} - BW/2 \leq f \leq f_{RF} + BW/2 \\
0, & f > f_{RF} + BW/2
\end{cases} \tag{7.10}$$

However, as inferred from (7.5) and (7.6), the filters should be adaptive to the input power, which is not practically feasible in the analog domain. To surmount this problem, the digital adaptive equalization system shown in Figure 7.3 is proposed to enable the power-dependent filtering in baseband.

![Figure 7.3 Block diagram of the baseband equalizer](image-url)
The operation of the proposed digital equalizer is illustrated in Figure 7.3. At first, the instantaneous power of the complex baseband waveform $x(n)$, $|x(n)|$, is evaluated and compared to the threshold level, $P_{\text{in,max}}/4$. If $P_{\text{in,max}}/4 > |x(n)|$, then $x(n)$ is filtered through the finite impulse response (FIR) digital filters, FIR1 and FIR3, to obtain the baseband waveforms $x_C(n)$ and $x_P(n)$ feeding the carrier branch and the peaking paths, respectively. Otherwise (i.e., $|x(n)| \geq P_{\text{in,max}}/4$), $x_C(n)$ and $x_P(n)$ are collected at the output of the digital filters FIR2 and FIR4, respectively. The frequency responses of FIR1, FIR2, FIR3 and FIR4, denoted by $D_{C1}(f)$, $D_{C2}(f)$, $D_{P1}(f)$ and $D_{P2}(f)$, respectively, are obtained from the analog-to-digital filter conversion of (7.7)–(7.10) according to [53]:

\[
D_{C1}(f) = \begin{cases} 
0, & -F_S/2 < f < -BW/2 \\
\frac{Z_0}{\text{real}\{Z_C(f+f_{RF})\}}, & -BW/2 \leq f \leq BW/2 \\
0, & BW/2 < f < F_S/2 
\end{cases} \tag{7.11}
\]

\[
D_{C2}(f) = \begin{cases} 
0, & -F_S/2 < f < -BW/2 \\
1 - \frac{1}{2} \cdot \left(\frac{Z_0 - Z_L(f+f_{RF})}{Z_L(f+f_{RF})}\right)^2, & -BW/2 \leq f \leq BW/2 \\
0, & BW/2 < f < F_S/2 
\end{cases} \tag{7.12}
\]

\[
D_{P1}(f) = \begin{cases} 
0, & -F_S/2 < f < -BW/2 \\
\frac{Z_0}{\text{real}\{Z_C(f+f_{RF})\}}, & -BW/2 \leq f \leq BW/2 \\
0, & BW/2 < f < F_S/2 
\end{cases} \tag{7.13}
\]
where $F_s$ is the sampling rate of the input baseband waveform, which is assumed to satisfy the condition, $F_s > BW$.

Figure 7.4 illustrates the magnitude responses of FIR1, FIR2, FIR3 and FIR 4. The filters are implemented in MATLAB to fit the responses expressed in (7.11)–(7.14) for the design example of $f_{RF} = 1.15 f_0$, $BW = 0.1 f_0$ and $F_s = 2 \times BW$.

Due to the nonsymmetrical frequency responses with respect to the y-axis, all FIR filters of the baseband equalizer are bandpass and have complex-valued coefficients. The MATLAB method used for linear phase FIR filter design employs the Remez exchange technique to approximate the desired frequency response [54]. The inputs of the function include the normalized frequency bands, the value of the magnitude in each band, and the filter order $N$. Using this method, the optimal magnitude responses were approximated using $N = 64$ taps; and, the resulting group delay is found to be equal to $N/2 = 32$ samples in each design.
Figure 7.4 Magnitude responses of the FIR filters of the equalizer for $f_{RF} = 1.15f_0$, $BW = 0.1f_0$, $F_S = 2BW$, and $N = 64$: (a) FIR 1 and FIR 2; (b) FIR 3 and FIR 4
7.3 Power Efficiency Analysis

To assess the efficiency performance of the Doherty PA when driven with modulated signals with large bandwidth around a given carrier frequency $f_{RF}$, the modulated efficiency across the signal bandwidth, $\eta_{DPA}^{BW}$, is introduced as criteria to estimate the average efficiency of the PA; and, it is defined by [53]:

$$\eta_{DPA}^{BW} = \frac{\int_{f_{RF}-BW/2}^{f_{RF}+BW/2} PSD(f) \cdot \eta_{DPA}^{CW, back-off}(f) df}{\int_{f_{RF}-BW/2}^{f_{RF}+BW/2} PSD(f) df}$$  (7.15)

where $\eta_{DPA}^{CW, back-off}$ is the continuous wave (CW) efficiency of the Doherty PA calculated at an input power level corresponding to the turn-on of the peaking amplifier, which corresponds to 6 dB back-off from the maximal power of the input signal. PSD is the power spectral density of the modulated signal. In (7.15), $\eta_{DPA}^{BW}$ is expressed as a function of the back-off efficiency because, generally, the average efficiency of Doherty PAs is mainly dominated by the peak efficiency point that occurs at back-off, especially when the latter matches with the peak-to-average power ratio (PAPR) of the input signal [55, 62].

Referring to (6.12) and (6.13) in Chapter Six, the back-off efficiency of the Doherty PA with baseband equalizer, $\eta_{DPA, EQ}^{CW, back-off}$, and with no baseband equalizer, $\eta_{DPA}^{CW, back-off}$, are given by [53]:

$$\eta_{DPA, EQ}^{CW, back-off}(f) = \eta_{DPA, EQ}^{CW, Back-off}(f_0) \cdot \sqrt{\frac{\text{real}\{Z_C(f)\}}{2Z_0}} = \frac{\pi}{4} \cdot \sqrt{\frac{\text{real}\{Z_C(f)\}}{2Z_0}}$$  (7.16)
\[
\eta_{\text{DPA, back-off}}^\text{CW}(f) = \eta_{\text{DPA, Back-off}}^\text{CW}(f_0) \cdot \frac{\text{real}\{Z_C(f)\}}{2Z_0} = \frac{\pi}{4} \cdot \frac{\text{real}\{Z_C(f)\}}{2Z_0}
\]  

(7.17)

where the \((\pi/4)\) term represents the theoretical efficiency value of the Doherty PA at 6 dB power back-off [7, 33, 44].

Figure 7.5 depicts the variation of the average efficiency versus BW of the digitally driven Doherty PA (baseband equalizer ON) and that of the conventional Doherty PA (baseband equalizer OFF). For the latter, the input power is evenly distributed between the two branches at all times. The average efficiency is estimated using (7.3), (7.4), and (7.15)–(7.17) assuming that PSD\((f)\) is constant through all possible frequency bands centered on \(f_0 \pm 0.25f_0, f_0 \pm 0.20f_0, f_0 \pm 0.15f_0, f_0 \pm 0.10f_0, f_0 \pm 0.05f_0\) and \(f_0\).

As inferred from Figure 7.5, when the input signals are centered on a carrier frequency that is distant from the nominal design frequency \(f_0\), the baseband equalizer yields significant improvement in power efficiency for both narrow and wide bandwidth signals. Besides, when the input RF signals are located at the vicinity of \(f_0\), the efficiency enhancement due to the equalizer is more visible for very wide bandwidth inputs.
Figure 7.5 Average efficiency versus bandwidth
7.4 Computation Burden

In this section, the computation complexity of the baseband equalization block is investigated. In the proposed equalizer, nearly all computational effort is spent on complex FIR filtering which involves additions, subtractions, and multiplications. Since the number of floating point operations (FLOPs) is a well-established criterion for measuring the number of additions, subtractions and multiplications [56], it is adopted as the complexity measure in this work. A typical operation-FLOP conversion is shown in Table 7.1 [56].

<table>
<thead>
<tr>
<th>Operation</th>
<th>Number of FLOPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>0</td>
</tr>
<tr>
<td>Conjugate</td>
<td>0</td>
</tr>
<tr>
<td>2-to-1 Multiplexing</td>
<td>0</td>
</tr>
<tr>
<td>Real Addition</td>
<td>1</td>
</tr>
<tr>
<td>Real Substation</td>
<td>1</td>
</tr>
<tr>
<td>Complex Addition</td>
<td>2</td>
</tr>
<tr>
<td>Complex-real Multiplication</td>
<td>2</td>
</tr>
<tr>
<td>$</td>
<td>.</td>
</tr>
<tr>
<td>Complex-complex Multiplication</td>
<td>6</td>
</tr>
</tbody>
</table>
Figure 7.6 depicts the block diagram for the synthesis and implementation in the field-programmable gate array (FPGA) of the baseband equalizer. At each time instance, the input complex sample is being filtered only by two complex FIR filters (i.e., either by FIR1 and FIR3 or by FIR2 and FIR4). Based on Figure 7.6 and Table 7.1, and recalling that the implementation of a complex $N$-tap FIR filter requires $N$ complex-complex multiplications and $(N-1)$ complex additions, the running complexity ($C$) can be written as:

$$C = 3 + 1 + 2[6N + 2(N - 1)] = 16N$$  \hspace{1cm} (7.18)

FLOPs, where the first term, 3, is for the squared magnitude construction and the second term, 1, is for the subtraction.

Figure 7.6 Block diagram of the baseband equalizer implemented in FPGA
Equation (7.18) shows that the running complexity of the baseband equalizer grows linearly with $N$. It is therefore important to optimize the design of the FIR filters while minimizing their order. This can be achieved by tolerating soft transition bands as graphically illustrated in Figure 7.7. Given that the useful signal exists only within the passband $[-BW/2, BW/2]$, this method helps reducing the running complexity without compromising the efficiency of the Doherty PA.

Figure 7.7 Magnitude responses of FIR1 for $f_{RF} = 1.15f_0$, $BW = 0.1f_0$, $F_S = 2BW$, and $N = 64$ (black) and 32 (gray)

To further analyze the computation burden, the complexity of the baseband equalizer is benchmarked against that of a digital predistorter. The generalized memory
polynomial (GMP) based model is considered for the comparison since it is widely recognized as the state-of-the-art technique for PA linearization [6, 57, 58].

As reported in [58], excellent linearization performance of a typical Doherty PA is achievable based on the GMP model with nearly 100 coefficients. In this case, the running complexity of the predistorter is estimated to be approximately 1000 FLOPs [56]. Based on (7.18), on the other hand, the implementation of the baseband equalizer for the design case with relaxed transition bands (i.e., \( N = 32 \)) would require \( 16 \times 32 = 512 \) FLOPs. Accordingly, one can deduce that the running complexity of the baseband equalizer is lower than that of the digital predistorter; and thus, it can be implemented along with the linearizer in the same DSP unit of the wireless transmitter with no detrimental effects on the linearity.

### 7.5 Experimental Results

For the practical implementation, the digitally equalized Doherty PA is implemented based on the experimental set-up shown in Figure 7.8. The system consists of two arbitrary waveform generators (AWGs) from Agilent Technologies Inc. (4438C with maximum clock rate of 100 MHz), a dual-input Doherty PA, a vector signal analyzer (VSA) from Agilent Technologies Inc. (E4440A with the maximum analysis bandwidth of 80 MHz) and a computer with MATLAB and Agilent’s VSA software for baseband signal processing.

The baseband signals \( x_c(n) \) and \( x_p(n) \) are generated in the computer and downloaded to the AWGs which modulate the baseband data to an RF carrier \( (f_{RF}) \). The RF signals of the carrier and peaking paths are then amplified by the preamplifiers and fed to the dual-input Doherty PA, which is the device under test (DUT). Next, the RF
output of the DUT is captured by the VSA and stored in the computer using Agilent’s VSA software for signal processing and analysis. All devices are connected by a general-purpose interface bus (GPIB) and triggered in synch.

The DUT is originally designed for downlink wideband code division multiple access (WCDMA) band and implemented using 10-Watt CGH40010 gallium nitride (GaN) transistor from Cree Inc. The carrier and peaking amplifiers are built using identical matching networks and operated in class AB (quiescent current, \( I_{DQ} = 200 \text{ mA} \), drain voltage \( V_{DS} = 28\text{V} \)) and class C (\( I_{DQ} = 0 \), \( V_{DS} = 28\text{V} \)) modes, respectively. Lastly, to maintain the proper phase offset between the input branches of the Doherty PA, the phase of the baseband signal of the peaking branch is adjusted in digital domain to be at \((-90 \times f_{RF} / f_0)\) degrees lag behind that of the carrier branch. The design frequency \( f_0 \) is equal to 2.14 GHz.

Figure 7.8 Experimental setup of the digitally equalized Doherty PA
To experimentally validate the simulation results reported in Section 7.3 and confirm the usefulness of the digitally equalized Doherty PA for broadband and multistandard applications, the following test scenarios are conducted in the experiments.

- Scenario 1: 60 MHz bandwidth Long Term Evolution (LTE)-Advanced signal (3×20 MHz carrier components) with 7.6 dB PAPR, centered at 2.36 GHz.
- Scenario 2: 20 MHz bandwidth LTE-Advanced signal with 7.5 dB PAPR, centered at 2.36 GHz.
- Scenario 3: 60 MHz bandwidth LTE-Advanced signal (3×20 MHz carrier components) with 7.6 dB PAPR and centered at 2.14 GHz.
- Scenario 4: 20 MHz bandwidth LTE-Advanced signal with 7.5 dB PAPR, centered at 2.14 GHz.

The measurement results are summarized in Table 7.2 and Figure 7.9.

When driven with the 60 MHz LTE signal at 2.36 GHz, the average drain efficiency of the digitally equalized Doherty PA is 42.4% whereas that of the conventional Doherty PA is 37%. At the same frequency, the baseband equalizer enabled an average efficiency enhancement of nearly 5% (from 38.4 to 43.1%) when the Doherty PA is driven with the 20-MHz LTE signal.

At the nominal design frequency, 2.14 GHz, the digitally equalized Doherty PA driven with the 60 MHz LTE signal exhibited an average drain efficiency of 46.5% versus 44.5% for its conventional counterpart. On the other hand, the efficiency enhancement is limited to 0.3% with the 20 MHz LTE signal. These results are in accordance with those reported in Figure 7.5.
<table>
<thead>
<tr>
<th>Scenario</th>
<th>Output Power</th>
<th>DC Current</th>
<th>Drain efficiency</th>
<th>ACPR Low/High</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Scenario 1</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equalizer OFF</td>
<td>36.6 dBm</td>
<td>442 mA</td>
<td>36.9%</td>
<td>−26/−27 dBc</td>
</tr>
<tr>
<td>Equalizer ON</td>
<td>36.4 dBm</td>
<td>367 mA</td>
<td>42.5%</td>
<td>−26/−28 dBc</td>
</tr>
<tr>
<td><strong>Scenario 2</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equalizer OFF</td>
<td>36.6 dBm</td>
<td>425 mA</td>
<td>38.4%</td>
<td>−24/−26 dBc</td>
</tr>
<tr>
<td>Equalizer ON</td>
<td>36.5 dBm</td>
<td>369 mA</td>
<td>43.2%</td>
<td>−25/−25.5 dBc</td>
</tr>
<tr>
<td><strong>Scenario 3</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equalizer OFF</td>
<td>36.7 dBm</td>
<td>375 mA</td>
<td>44.5%</td>
<td>−31/−28 dBc</td>
</tr>
<tr>
<td>Equalizer ON</td>
<td>36.8 dBm</td>
<td>368 mA</td>
<td>46.45%</td>
<td>−30/−29 dBc</td>
</tr>
<tr>
<td><strong>Scenario 4</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equalizer OFF</td>
<td>36.7 dBm</td>
<td>363 mA</td>
<td>46%</td>
<td>−34/−31 dBc</td>
</tr>
<tr>
<td>Equalizer ON</td>
<td>36.7 dBm</td>
<td>361 mA</td>
<td>64.3%</td>
<td>−34/−31 dBc</td>
</tr>
</tbody>
</table>

*a* Adjacent channel power ratio (ACPR) measured at 40 MHz offset.

*b* ACPR measured at 20 MHz offset.
Figure 7.9 Output spectra of the Doherty PAs: (a) scenario 1; (b) scenario 2; (c) scenario 3; (d) scenario 4
To verify the digital predistortion (DPD) performance of the digitally equalized Doherty PA, the 20 MHz bandwidth LTE signal centered at 2.36 GHz is considered for the test (scenario 2). As illustrated in Figure 7.9(b), the ACPR is significantly reduced after linearization.

Due to the limitations of instrument’s bandwidth and sampling rate, the bandwidth of the modulated signals was restricted to a maximum of 60 MHz for the efficiency tests and 20 MHz for DPD linearization. However, the reported results demonstrate the potential of the proposed Doherty PA for high efficient operation with wider signal bandwidths when using an experimental platform with higher sampling rate and wider analysis bandwidth.

7.6 Conclusion

In this chapter, a new architecture of digitally equalized Doherty PA was introduced. The baseband equalization system of this architecture is implemented to mitigate the frequency limitations of wireless Doherty PAs. Experimental results performed on a Doherty PA driven by 20 and 60 MHz bandwidth LTE-Advanced signals demonstrated the usefulness of the proposed architecture in the context of broadband and multistandard applications. The applicability of the proposed architecture can be further demonstrated for multiband applications on condition that test equipments with sufficiently high sampling rate and analysis bandwidth are available.
Chapter Eight: Conclusions

8.1 Summary of the Main Contributions

This thesis has addressed some of the critical challenges that restrain the power efficiency and bandwidth of wireless Doherty power amplifiers (PAs). An advanced dual-input Doherty PA architecture and a variety of digital signal processing (DSP) techniques have been proposed, in order to compensate for most of the analog impairments and restore the quasi-perfect load modulation behaviour. All aspects have been covered, from Doherty PA design to hardware/software integration and performance assessment.

As a first step in the realization of these advanced architectures, a systematic approach for enhanced Doherty PA design has been reported in the first part of the thesis. This approach employs load-pull data to synthesize the circuit elements (i.e., output matching networks and offset lines) of the carrier and peaking amplifiers. A step-by-step design methodology has been presented to ensure best achievable performance.

In contrast to previously reported approaches [27–30], the proposed methodology can be adopted to optimize the operation of the Doherty PA at the design stage for any criterion, in terms of efficiency, linearity, gain or any possible combination of these, without relying on the knowledge of the intrinsic elements of the device, as in [27, 28] or on the use of post-tuning circuitries for optimizing the output matching elements of the carrier and peaking amplifiers, as reported in [29, 30]. A gallium nitride (GaN) based Doherty PA was then designed for power efficiency. This PA delivered a power-added efficiency (PAE) of 52% at an output power back-off (OPBO) of nearly 7 dB from saturation power. The peak PAE was just above 60%.
The problem of the power- and bias-dependent phase imbalance that is generally observed through the output branches of GaN Doherty PAs was addressed. A digital adaptive phase alignment mechanism based on phase digital predistortion (DPD) was introduced and experimentally validated within the dual-input architecture. This method was applied to the previously designed GaN Doherty PA, showing significant improvement in power efficiency. Indeed, the PAE at full power drive exceeded the barrier of 70%; and, the efficiency drop that was observed in the response of the previously designed Doherty PA was completely avoided. As depicted in Table 8.1, the PAE performance of this digitally driven Doherty PA is among the best reported results.

### Table 8.1 Performance Comparison with State-of-the-Art GaN based Doherty PAs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Drain Efficiency / PAE</th>
<th>Design Frequency</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>at 6 dB OPBO</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>at Peak Power</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[35]</td>
<td>47.9% / 46%</td>
<td>2.14 GHz</td>
<td>2009</td>
</tr>
<tr>
<td>[59]</td>
<td>55% / N.A.</td>
<td>2.60 GHz</td>
<td>2009</td>
</tr>
<tr>
<td>[60]</td>
<td>74% / N.A.</td>
<td>2.655 GHz</td>
<td>2010</td>
</tr>
<tr>
<td>[61]</td>
<td>46% / 43%</td>
<td>1.90 GHz</td>
<td>2010</td>
</tr>
<tr>
<td>[46]</td>
<td>50% / N.A.</td>
<td>2.60 GHz</td>
<td>2012</td>
</tr>
<tr>
<td>[63]</td>
<td>60% / N.A.</td>
<td>2.00 GHz</td>
<td>2012</td>
</tr>
<tr>
<td>[64]</td>
<td>N.A. / 60%</td>
<td>1.80 GHz</td>
<td>2012</td>
</tr>
<tr>
<td>This Work [50]</td>
<td>60% / 57%</td>
<td>2.425 GHz</td>
<td>2011</td>
</tr>
</tbody>
</table>

N.A.: Not indicated.
The problems of gain imbalance between the carrier and peaking paths and input power waste into the peaking branch at back-off were studied. While the first problem affects the efficiency in the high power region, the second compromises the gain of the Doherty PA. The use of digital adaptive power distribution within the dual-input Doherty PA architecture has been proposed to tackle these two problems. It was demonstrated that this architecture is effective in improving the performance of the Doherty PA over a wide range of operation. The main original contributions of this research can be summarized as follows:

1. New models of carrier and peaking current profiles have been proposed to allow for the analysis of Doherty PA operation under adaptive input power drive.
2. Generalized and explicit expressions for performance assessment of Doherty PAs under adaptive input power drive have been derived and validated.
3. A practical methodology for DPD based linearization of dual-input Doherty PAs has been reported.

It is worth stating that the use of adaptive input power distribution in Doherty PAs was previously introduced in [41]. In that contribution, the adaptive power distribution functionally was performed in the analog domain based on customized analog splitters designated by extended-resonance power dividers. The operation of such power dividers, however, is entirely based on the nonlinear behaviour of the input impedance of the peaking amplifier, which greatly compromises the flexibility and limits the implementation to a restricted number of power distribution schemes. Furthermore, no
theoretical analysis illustrating the operation of the Doherty PA under adaptive power drive was reported. Instead, the results were discussed in a qualitative manner.

The next part of this thesis has dealt with the major limitation of Doherty PAs, namely the narrow bandwidth. The response of the Doherty PA with frequency-dependent components was thoroughly analyzed; and, it was theoretically confirmed that the quarter-wavelength transmission lines of the output combiner induce significant output power drop at back-off and an impaired load modulation mechanism after the turn-on of the peaking amplifier.

To tackle these critical issues, a frequency-dependent precompensation mechanism has been derived and applied within the dual-input Doherty PA architecture. Simulations and measurements demonstrated a substantial bandwidth extension following the adoption of the proposed technique. The original contributions related to this topic are:

1. An analytical examination of the power efficiency, output power, and bandwidth of the Doherty PA with frequency-dependent components and class C biased peaking amplifier has been developed.

2. An optimal power distribution scheme has been derived and was applied to restore the bandwidth of the Doherty PA. Analytical expressions of Doherty PA performance under the optimized power drive conditions were deduced and compared. It was concluded that the quasi-ideal operation could be reproduced over a fractional bandwidth of 54%.
The last phase of this work proposed a digitally equalized Doherty PA that is suitable for broadband and multistandard wireless radios. This original architecture incorporates a digital baseband equalizer, the frequency response of which fits the optimal power distribution scheme that has previously been derived. The baseband equalizer enabled the Doherty PA to operate at several frequency bands and efficiently amplify wide bandwidth radio signals within the extended frequency bandwidth. The main contributions in this field are:

1. A new baseband equalization methodology has been proposed and implemented within the dual-input Doherty PA architecture. The operation of Doherty PA with wide bandwidth (up to 60 MHz) modulated signals was experimentally demonstrated.

2. An implementation approach that alleviates the constraints on DSP resources in the baseband equalizer has been proposed.

The major research contributions of this work were disseminated in refereed journal and conference papers. These include three papers in *IEEE Transactions on Microwave Theory and Techniques* [50–52], one paper in *IEEE Transactions on Circuits and Systems* [47], one paper submitted to *IEEE Transactions on Industrial Electronics* [53], one manuscript in *IET Science, Measurement & Technology* [48], and five IEEE conferences papers, including two invited [31, 36–38, 49]. Furthermore, some of the inventive contributions achieved in this work are the subject of one U.S. Patent application [65].
8.2 Significance of the Current Work

The innovative power amplification architecture proposed in this thesis is significant in that it allowed for the adoption of advanced signal processing algorithms that cannot be implemented in conventional single-input architectures, resulting in substantial improvements in power efficiency and frequency bandwidth of wireless Doherty PAs.

The outcomes of this work have already pointed to new research directions in a number of research groups worldwide. For instance, Cao et al. [66] from Chalmers University of Technology, Gothenburg, Sweden, and Delft Institute of Microsystems and Nanoelectronics, Delft University of Technology, Delft, Netherlands, have investigated behavioural modeling and DPD techniques for dual-input Doherty PAs. Hone et al. [67] from the Centre for Communications Research, University of Bristol, Bristol, U K, proposed a dual-input digitally driven inverse load modulated Doherty PA. Moreover, the generic methodology for Doherty PA design and optimization reported in this thesis has been extended to support the design of dual-band Doherty PAs [68].

It is worth mentioning that the manuscript in which we presented the dual-input operation of Doherty amplifier for the first time [50] has already generated 10 citations in well-known IEEE publications [63, 66–74] since its publication in May 2011. This also exemplifies the significance of the present work.

Although one may argue that it increases the complexity of the overall transmitter, the dual-input architecture has been proven to overcome the major hurdles that analog Doherty PAs must overcome. The superior flexibility and achieved enhancement certainly justify the added complexity and the extra power consumption in
the digital signal processor. This point is better elucidated in the following paragraphs, where a breakdown of power consumption in cellular base stations is analyzed.

The power consumption of a typical second generation / third generation (2G/3G) base station has been evaluated to be 1,400 watts per annum with resulting energy costs in the range of $3,200 per annum and a carbon dioxide (CO$_2$) footprint of 11 tons [75]. Within a base station, it has been estimated that the PA consumes about 65% of the total energy requirement, which corresponds to 910 watts per annum. The power consumption share of the baseband/DSP, on the other hand, has been estimated to be approximately 8%, of which the DPD can be reasonably assumed to consume one fourth (i.e., 2% of the total power consumption of a base station, which corresponds to 28 watts per annum) [75].

In a realistic case, where a digitally driven Doherty PA enables an increase of 6% in power efficiency, nearly 56 watts per annum can be saved in each base station. Moreover, recalling the results of Section 7.4 in Chapter Seven, where it is shown that the power consumption of the digital baseband equalizer is estimated to be half of that of the DPD (i.e., nearly 14 watts), then the net reduction in power consumption is equal to 42 (56 – 14) watts per annum per base station. Taking into account that a medium-sized cellular network is typically equipped with approximately 10,000 2G/3G base stations, the digitally driven Doherty PA would permit a total saving in energy costs of $960,000 (i.e., nearly $1 million) per annum along with a reduction of 3,300 tons of CO$_2$. 

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8.3 Recommendations for Future Work

The research activities performed within this project have led to a number of topics that can be considered for future work. These are summarized in the following paragraphs.

First, an immediate continuation of this work will involve associating the proposed bandwidth extension approach with a well-designed broadband dual-input Doherty PA. In this paradigm, a bandwidth in the order of GHz may be anticipated, provided that we start with hardware that has an initial bandwidth of 400 to 500 MHz, which is feasible using state-of-the-art analog techniques [44, 46].

Second, it would be interesting to investigate the application of the digitally driven Doherty PA in the context of concurrent multistandard and software defined radio applications. The processing speed requirements for very wide signal bandwidths within these applications, however, will be quite challenging. Sub-band processing techniques can be adopted to alleviate the processing requirements [76].

Another interesting research work would be the integration of the proposed technology with newly introduced radio frequency digital-to-analog converters (RF DACs) [77] in order to develop an integrated fully digital PA/transmitter.

Finally, one may consider implementation of the proposed digital techniques in the field-programmable gate array (FPGA) and DSP units of a rapid prototyping platform, towards the evolution of a standalone digitally driven Doherty PA based transmitter. This will require refining the algorithms that have been developed in MATLAB for proof-of-concept validations to make them more computationally efficient.
Appendix

In what follows, the expressions of (5.24), (5.25), and (5.20) are demonstrated consecutively.

By rearranging (5.16) to:

\[ I_{C,dig}(v_{in},\varphi_C) = \delta \cdot I_{C,sym}(v_{in},\varphi_C), \ 0 \leq v_{in} < V_{in,max} / 2\delta \]  \hfill (A.1)

it can be deduced that:

\[ P_{out,C,dig} = \delta^2 \cdot P_{out,P,sym}, \ 0 \leq v_{in} < V_{in,max} / 2\delta \]  \hfill (A.2)

where \((P_{out,C,ext})\) and \((P_{out,C,sym})\) designate the output power of the carrier amplifier of the digital and symmetrical Doherty power amplifiers (PAs), respectively.

Assuming that the gain of the carrier amplifier is constant, (A.2) gives:

\[ P_{in,C,dig} = \delta^2 \cdot P_{in,P,sym}, \ 0 \leq v_{in} < V_{in,max} / 2\delta \]  \hfill (A.3)

In view of the fact that the carrier amplifier of the symmetrical Doherty PA gets half of the available input power \((P_{in,DPA})\), the (A.3) becomes:

\[ P_{in,C,dig} = \frac{\delta^2}{2} \cdot P_{in,DPA}, \ 0 \leq v_{in} < V_{in,max} / 2\delta \]  \hfill (A.4)

and thus, (5.24) is demonstrated.

Besides, once can write:

\[ I_{P,dig}(v_{in},\varphi_C) = \sigma \cdot I_{P,sym}(v_{in},\varphi_{P,dig}), \ 0 \leq v_{in} < V_{in,max} / 2\delta \]  \hfill (A.5)
where $I_{P,sym}(v_{in},\varphi_{P,dig})$ designates the output current from the peaking amplifier of a symmetrical Doherty PA, the peaking device of which is biased at $\varphi_{P,dig}$. Based on Figure 5.2, $I_{P,sym}(v_{in},\varphi_{P,dig})$ is given by:

$$I_{P,sym}(v_{in},\varphi_{P,dig}) = \left( \frac{v_{in}}{V_{in,max}} - \frac{1}{2\delta} \right) \cdot I_{1,P}(\varphi_{P,dig}), \quad V_{in,max}/2\delta \leq v_{in} < V_{in,max} \quad (A.6)$$

By applying the procedure used through (A.1)–(A.4), it can be shown that:

$$P_{in,P,dig} = \frac{\sigma^2}{2} \cdot P_{in,DPA}, \quad V_{in,max}/2\delta \leq v_{in} < V_{in,max} \quad (A.7)$$

which demonstrates (5.25).

Now, starting from (A.7), one can write:

$$P_{in,C,dig} = \left( 1 - \frac{\sigma^2}{2} \right) \cdot P_{in,DPA}, \quad V_{in,max}/2\delta \leq v_{in} < V_{in,max} \quad (A.8)$$

Then, by following the reverse way of the procedure used through (A.1)–(A.4), it can be shown that:

$$I_{C,dig}(V_{in,max},\varphi_{C}) = \sqrt{(2 - \sigma^2)} \cdot I_{C,sym}(v_{in},\varphi_{C}), \quad V_{in,max}/2\delta \leq v_{in} < V_{in,max} \quad (A.9)$$

Afterwards, by evaluating (40) for $v_{in} = V_{in,max}$, it can be deduced that:

$$I_{C,dig}(V_{in,max},\varphi_{C}) = \sqrt{(2 - \sigma^2)} \cdot I_{1,C}(\varphi_{C}) \quad (A.10)$$

and this demonstrates (5.20).

Last of all, it is worth mentioning that (A.10) also explains the expressions of the fundamental and direct current (DC) components of the carrier amplifier of the digital Doherty PA, which are given in (5.10) and (5.11), respectively.
References


[12] O. Hammi and F. M. Ghannouchi, “Comparative study of recent advances in power amplification devices and circuits for wireless communication infrastructure,” in *IEEE International Conference on Electronics, Circuits, and


I. Kim, Y-Y. Woo, J. Kim, J. Moon, J. Kim, and B. Kim, “High-efficiency hybrid EER transmitter using optimized power amplifier,” IEEE Transactions on


