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Design and Implementation of Single Transistor Active Filters

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Design and Implementation of Single Transistor Active Filters

by

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A THESIS

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Abstract

This thesis investigates the design of single transistor second order active filters. Four general topologies are presented, each with a two port network surrounded by three impedances that form a T-network. From the topologies, four transfer functions are derived which are further simplified by replacing the two port transmission matrix parameters with those of an ideal MOS. An exhaustive MAPLE search code is used to generate all possible second order filters. The search is carried out on the four general transfer functions, considering all possible impedance combinations. Design procedures of selected filters are shown and verified by Cadence Spectre simulations and experimental measurements. Based on the single transistor second order filters, active realizations of higher order filters are explored. A fourth order bandpass Chebyshev filter and a fourth order Comb filter are presented. Simulation and experimental results of the designed filters are shown and compared with the theoretical ones.

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Table of Contents

Abstract	ii
Acknowledgements	iii
Table of Contents	iv
List of Tables	vi
List of Figures	vi
1 Introduction	1
1.1 Analog Filters	1
1.2 Filter Classification	2
1.3 Allpass Filter	4
1.4 Bandpass Filter	5
1.5 Bandstop or Notch Filter	6
1.6 Higher Order Filter Design	7
1.7 Research Objectives	8
1.8 Thesis Overview	9
2 Single Transistor Active Filter	11
2.1 Proposed General Three Impedance Filter Topologies	11
2.2 Variation of Type-3 Filter Structure	16
2.3 All possible filter types	17
2.4 Discussion of Selected Filters	18
2.4.1 Bandpass Filter	19
2.4.1.1 Input and Output impedance of Bandpass Filter	22
2.4.2 Bandstop or Notch Filter	25
2.4.2.1 Input and Output Impedance of the Bandstop Filter	25
2.4.3 Allpass Filter	27

2.4.3.1	Input and Output Impedance of the Allpass Filter	28
2.4.4	Effect of g_m	29
2.4.5	Biasing Details	30
2.4.6	Non-ideal Effects	32
2.4.6.1	Effect of r_o	32
2.4.6.2	Effect of parasitic capacitances	35
3	Simulation and Experimental Results	37
3.1	Bandpass Filter	37
3.2	Bandstop Filter	40
3.3	Allpass Filter	42
4	A Fourth Order Chebyshev Filter	50
4.1	Classical Chebyshev Filter Design Approach	50
4.2	Proposed Fourth Order Chebyshev Filter	51
4.3	Simulated Results	54
4.4	Two stage operational amplifier	54
4.4.1	Slew Rate	57
4.4.2	Compensation of the two stage operational amplifier	58
4.5	Chebyshev filter cascaded with two stage operational amplifier	59
4.6	Experimental Results	60
5	A Novel Active Comb Filter	65
5.1	Proposed Comb Filter Structure	65
5.2	Simulation Results	67
5.3	Experimental Results	69
6	Conclusions and Future Work	75
6.1	Conclusion	75
6.2	Trade-offs	76
6.3	Contribution	76
6.4	Future Work	77
	Bibliography	79

List of Tables

2.1	Type-1, Type-2 and Type-3 transfer functions using an ideal transistor	16
2.2	All possible second order filters for Type-1 filter configuration	19
2.3	All possible second order filters for Type-2 filter structure	20
2.4	All possible second order filters for Type-3 filter structure	21
2.5	All possible filters of an altered Type-3 filter topology of Figure 2.4.	21
4.1	Chebyshev filter design equations for two stages	52
4.2	Deviation in experimental and PSPICE simulation results for Chebyshev filter	61
5.1	Comb filter design equations for the two stages	66
5.2	Deviation in experimental and PSPICE simulation results for Comb filter .	70

List of Figures

1.1	Ideal brick wall magnitude response of (a) lowpass (b) highpass filters . . .	3
1.2	Ideal brick wall magnitude response of (a) bandpass (b) bandstop filters . . .	3
2.1	Type-1 filter topology with terminal A at AC ground	12
2.2	Type-2 filter structure with terminal C at AC ground	14
2.3	Type-3 filter topology with terminal B at AC ground	15
2.4	Altered Type-3 filter structure with R_s as an external resistor	16
2.5	Second order bandpass filter using a single transistor	22
2.6	General bandpass filter transfer function plotted in MATLAB at $f_o = 16.3$ MHz, $K = 0.99$ and $Q = 2.5$	22
2.7	Small signal diagram to find Z_{out} at very high and low frequencies	24
2.8	Small signal diagram to find Z_{out} at pole frequency	24
2.9	Second order bandstop filter topology	25
2.10	General bandstop filter transfer function plotted in MATLAB for $f_o = 16.3$ MHz, $K = 0.99$ and $Q = 2$	26
2.11	Small signal diagram to find Z_{in} of the notch circuit at very high frequencies	26
2.12	Second order AP filter structure	28
2.13	General allpass filter transfer function plotted in MATLAB for $f_o = 16.3$ MHz, $K = 1$ and $Q = Q_z = 1$	29
2.14	Allpass filter equivalent small signal diagram to find input impedance Z_{in} at very high frequencies	30
2.15	Allpass filter equivalent small signal diagram to find output impedance Z_{out} at high frequencies	30
2.16	Allpass filter #1 from Table 2.5 implemented with an additional DC biasing current source	31
2.17	Simulated magnitude and phase responses of allpass filter of Figure 2.16 . . .	32
2.18	Simulated input and output waveforms of allpass filter of Figure 2.16 at pole frequency of 4.6 MHz	33

3.1	Magnitude response of proposed bandpass filter simulated in Cadence to values of $L_1 = 50 \mu\text{H}$, $C_1 = 1.9 \text{ pF}$, $R_2 = 1.2 \text{ k}\Omega$, $R_3 = 100 \Omega$, and $R_s = 900 \Omega$.	38
3.2	Cadence simulated transient responses of input and output signals of bandpass filter at pole frequency of 16.3 MHz to values $L_1 = 50 \mu\text{H}$, $C_1 = 1.9 \text{ pF}$, $R_2 = 1.2 \text{ k}\Omega$, $R_3 = 100 \Omega$ and $R_s = 900 \Omega$.	39
3.3	Measured magnitude response of bandpass filter to values of $C_1 = 680 \text{ pF}$, $L_1 = 10 \text{ mH}$, $R_s = 900 \Omega$, $R_2 = 1.2 \text{ k}\Omega$ and $R_3 = 100 \Omega$.	40
3.4	Magnitude response of bandpass filter simulated in PSPICE to values of $C_1 = 680 \text{ pF}$, $L_1 = 10 \text{ mH}$, $R_s = 900 \Omega$, $R_2 = 1.2 \text{ k}\Omega$ and $R_3 = 100 \Omega$.	41
3.5	Bandstop filter magnitude response simulated in Cadence to values of $L_1 = 10 \mu\text{H}$, $C_1 = 9.52 \text{ pF}$, $R_2 = 600 \Omega$, $R_3 = 110 \Omega$, and $R_s = 1.2 \text{ k}\Omega$.	42
3.6	Cadence simulated input and output waveforms of bandstop filter at the pole frequency of 16.2 MHz to values $L_1 = 10 \mu\text{H}$, $C_1 = 9.52 \text{ pF}$, $R_2 = 600 \Omega$, $R_3 = 110 \Omega$, and $R_s = 1.2 \text{ k}\Omega$.	43
3.7	Measured magnitude response of bandstop filter to values of $C_1 = 68 \text{ pF}$, $L_1 = 2 \text{ mH}$, $R_s = 1.2 \text{ k}\Omega$, $R_2 = 500 \Omega$ and $R_3 = 100 \Omega$ with a vertical scale of 5 dB/ division and a logarithmic horizontal scale where each cycle represents a factor of 10.	44
3.8	Magnitude response of bandstop filter simulated in PSPICE to values of $C_1 = 68 \text{ pF}$, $L_1 = 2 \text{ mH}$, $R_s = 1.2 \text{ k}\Omega$, $R_2 = 500 \Omega$ and $R_3 = 100 \Omega$.	45
3.9	Allpass filter magnitude and phase response simulated in Cadence to values $L_2 = 24 \mu\text{H}$, $C_2 = 50 \text{ pF}$, $R_1 = 50 \Omega$, $R_3 = 930 \Omega$ and $R_s = 500 \Omega$.	46
3.10	Cadence simulated input and output waveforms of allpass filter at pole frequency to values $L_2 = 24 \mu\text{H}$, $C_2 = 50 \text{ pF}$, $R_1 = 50 \Omega$, $R_3 = 930 \Omega$ and $R_s = 500 \Omega$.	47
3.11	Measured magnitude and phase response of allpass filter to values $C_1 = 68 \text{ pF}$, $L_1 = 2 \text{ mH}$, $R_1 = 1 \text{ k}\Omega$, $R_3 = 1.2 \text{ k}\Omega$ and $R_s = 3.3 \text{ k}\Omega$.	48
3.12	Magnitude response of allpass filter simulated in PSPICE to values of $C_1 = 68 \text{ pF}$, $L_1 = 2 \text{ mH}$, $R_1 = 1 \text{ k}\Omega$, $R_3 = 1.2 \text{ k}\Omega$ and $R_s = 3.3 \text{ k}\Omega$.	49
4.1	Proposed Chebyshev fourth order bandpass filter	51
4.2	Passive fourth order bandpass filter	52
4.3	Source follower used as a voltage buffer	53
4.4	Comparison between ideal (dashed line) and simulated (solid line) magnitude and phase responses of Chebyshev filter	55
4.5	Two stage operational amplifier [33,34]	56

4.6	Small signal diagram of a common source amplifier	57
4.7	Small signal model of two stage operational amplifier	59
4.8	Magnitude and phase response of two stage operational amplifier simulated in Cadence	60
4.9	Two stage opamp cascaded with fourth order Chebyshev filter of Figure 4.1 to improve overall gain of the filter	61
4.10	Magnitude response of the proposed Chebyshev filter after cascading with a two stage opamp	62
4.11	Measured magnitude response of the fourth order Chebyshev filter for component values $C_1 = 6.8$ nF, $L_1 = 1$ mH, $C_2 = 2.2$ nF, $L_2 = 2$ mH, $R_s = 900$ Ω , $R_2 = R_4 = 1$ k Ω and $R_3 = R_5 = 100$ Ω with a vertical scale of 3dB/ division and horizontal scale of 20 kHz/ division.	63
4.12	Magnitude response of fourth order Chebyshev filter simulated in PSPICE for component values $C_1 = 6.8$ nF, $L_1 = 1$ mH, $C_2 = 2.2$ nF, $L_2 = 2$ mH, $R_s = 900$ Ω , $R_2 = R_4 = 1$ k Ω and $R_3 = R_5 = 100$ Ω	64
5.1	Proposed active fourth order comb filter	66
5.2	Passive fourth order Comb filter	66
5.3	Magnitude and phase responses of a general comb filter transfer function given by equation (5.1) plotted in MATLAB for $f_{o1} = 16.3$ MHz, $f_{o2} = 163$ MHz, $Q = 3$ and $K_1 = K_2 = 0.99$	68
5.4	Cadence simulated magnitude response of fourth order comb filter for values $C_1 = 9.5$ pF, $L_1 = 10$ μ H, $C_2 = 0.95$ pF, $L_2 = 1$ μ H, $R_s = 1.2$ k Ω , $R_2 = R_4 = 600$ Ω and $R_3 = R_5 = 110$ Ω	69
5.5	Input (V_{in}) and output (V_o) waveforms of Comb filter in Figure 5.1 at $f_{o1} = 16.2$ MHz simulated in Cadence	70
5.6	Input (V_{in}) and output (V_o) waveforms of Comb filter in Figure 5.1 at $f_{o2} = 162$ MHz simulated in Cadence	71
5.7	Cadence simulated response of comb filter designed to remove power line interferences at 50 Hz and 150 Hz	72
5.8	Measured magnitude response of comb filter implemented using discrete components of values $C_1 = 2.2$ nF, $L_1 = 10$ mH, $C_2 = 33$ pF, $L_2 = 2$ mH, $R_s = 1.2$ k Ω , $R_2 = R_4 = 500$ Ω and $R_3 = R_5 = 100$ Ω with a vertical scale of 5dB/ division and a logarithmic horizontal scale where each cycle represents a factor of 10.	73

5.9	Magnitude response of fourth order Comb filter simulated in PSPICE for component values $C_1 = 2.2 \text{ nF}$, $L_1 = 10 \text{ mH}$, $C_2 = 33 \text{ pF}$, $L_2 = 2 \text{ mH}$, $R_s = 1.2 \text{ k}\Omega$, $R_2 = R_4 = 500 \text{ }\Omega$ and $R_3 = R_5 = 100 \text{ }\Omega$	74
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CHAPTER 1

Introduction

1.1 Analog Filters

Analog filters are circuits that process signals in a frequency dependent manner, that is, they pass signals of a certain frequency range while blocking other frequencies. The range of frequencies that is allowed to pass is known as the passband, while the range of frequencies that is attenuated is the stopband. Filters can be passive or active. Passive filters are based on combinations of resistors, capacitors and inductors. They do not require external power supply and do not use any active elements such as transistors or operational amplifiers. Whereas, active filters are implemented by a combination of passive and active components (transistors, op-amps) and operate off an external power supply. The basic set of specifications that define a filter's response are its passband frequency, stopband frequency and gain characteristics at its passband and stopband. A filter's gain is the ratio of its output signal V_2 to its input signal V_1 and is usually expressed in decibels. Gain G_{dB} is defined as

$$G_{dB} = 20\log |T(\omega)| dB \quad (1.1)$$

where

$$|T(\omega)| = \left| \frac{V_2(\omega)}{V_1(\omega)} \right| \quad (1.2)$$

The term attenuation is also used instead of gain. It is simply the inverse of gain and can be defined as

$$\alpha(\omega) = -20\log|T(\omega)|dB, |T(\omega)| \leq 1 \quad (1.3)$$

Real world signals have both wanted and unwanted components. Therefore, to view signals at the desired frequency range it is essential to remove signals at other frequencies by means of filtering. Filters are used widely in almost every electronic equipments, from everyday electronics such as computers, radios, televisions, and stereo systems to equipments such as spectrum analyzers and signal generators. Analog to digital converters also require analog filters to prevent aliasing [1].

1.2 Filter Classification

The frequency selective characteristic of filter circuits can be used to differentiate between the types of filters. A filter can have a lowpass, highpass, bandpass, bandstop and allpass response where each name indicates the shape of the output waveform. For example, a lowpass filter will pass signals of frequencies lower than a certain cutoff frequency while attenuate the frequencies higher than the cutoff frequency. The ideal responses of lowpass and highpass filters are shown in Figure 1.1. An ideal filter, also called a brick wall filter transmits frequency in its passband completely unattenuated and without phase shift, while providing full attenuation of signal components in the stopband. Figure 1.2 shows the ideal responses of bandpass and bandstop filters. In practice, it is impossible to realise ideal or brick wall filters. Realistic filter responses are referred to as approximations to the original. There are different ways to approximate the characteristics of an ideal filter based on the specifications. Some approximation methods used in analog filter design are Butterworth, Chebyshev, Inverse Chebyshev, Elliptic or Cauer. In the following sections, some selected filter types are discussed whose implementations are presented in Chapters 2 and 3.

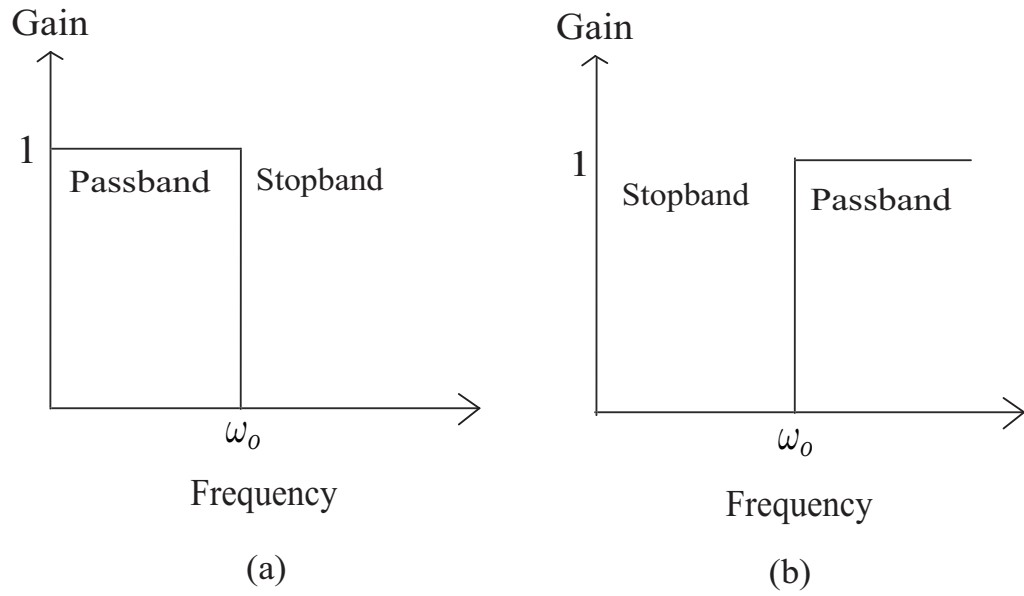


Figure 1.1: Ideal brick wall magnitude response of (a) lowpass (b) highpass filters

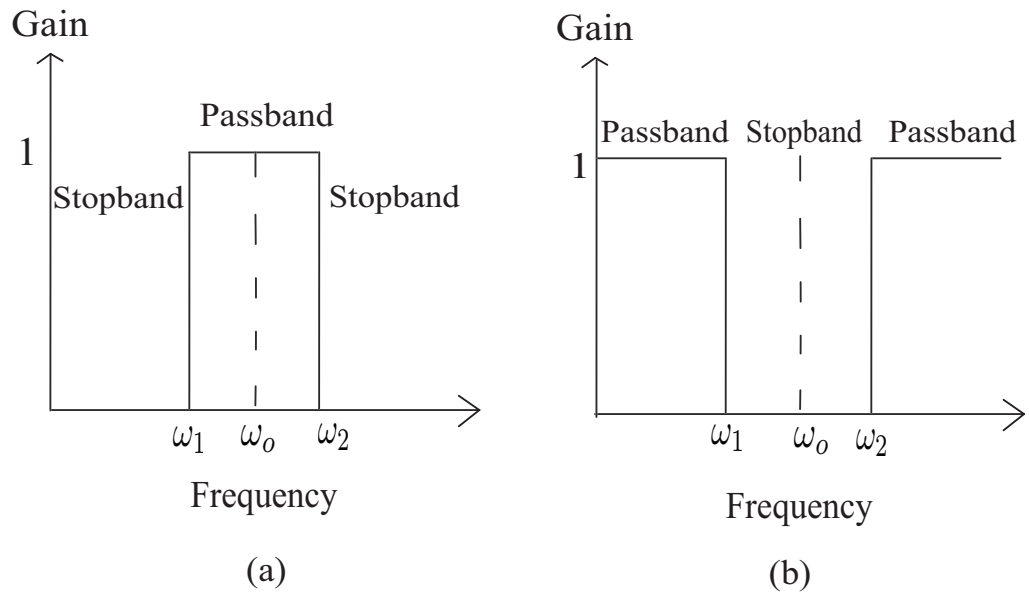


Figure 1.2: Ideal brick wall magnitude response of (a) bandpass (b) bandstop filters

1.3 Allpass Filter

Allpass filters are used to change phase of an input signal from 0° to 180° or from 180° to 0° , while keeping the amplitude constant over the desired range of frequencies. Allpass functions can be used to correct the delay characteristics of a circuit by connecting it in cascade with an allpass circuit so that the total delay of the cascaded circuit is the sum of the delay functions of the two circuits. Thus, allpass functions are chosen to yield a desired delay response and in such cases, are referred to as delay equalizers [2].

Several current mode and voltage mode allpass filters can be found in literature. Most of the circuits, however, use multiple passive elements and various active elements such as opamps [3,4], operational transconductance amplifiers (OTRA) [5,6], current differencing buffered amplifiers (CDBA) [7], current conveyors [8–10], and four-terminal floating nullors (FTFN) [11]. Different applications of allpass filters have been reported such as, fiber dispersion compensation [12], current-mode bandpass circuit designed with CDBA [7], and four phase oscillator build using a differential difference current conveyor (DDCC) as the building block [13]. MOS or bipolar realizations of the active building blocks found in literature tend to be complex and use several passive and active elements. For example, the first order allpass filter presented in [14] used two second generation current conveyors (CCIIIs) as active elements. Recently, the use of a single transistor as an active element to design second order filters was first explored in [15], with minimum number of passive components. Different second order filter types were presented and verified. In [16] a single transistor bandpass filter first reported in [15] was used to derive an allpass filter that employed only one transistor and four passive elements. The fabricated chip of the allpass filter was found to occupy an area of $380\mu m \times 165\mu m$. A comparison of the results with other published allpass filters showed the area of the filter to be lower than that of other implementations except for the filter in [17] where no inductors were used.

1.4 Bandpass Filter

A bandpass filter is a circuit that passes signals between two specific frequencies and rejects the signals outside the specified frequency range. Figure 1.2 (a) shows the ideal brick wall response of a bandpass filter. The bandwidth of a bandpass filter refers to the range of frequencies that are passed and is measured as the difference between the two 3 dB cutoff frequencies. If ω_1 and ω_2 as shown in Figure 1.2 (a) are the passband edges, the bandwidth is given as

$$B = \omega_2 - \omega_1 \quad (1.4)$$

The center frequency ω_o of the passband is the geometric mean of the cutoff frequencies given as

$$\omega_o = \sqrt{\omega_1 \omega_2} \quad (1.5)$$

The characteristic transfer function of a second order bandpass filter is

$$T(s) = K \frac{Bs}{s^2 + Bs + \omega_o^2} \quad (1.6)$$

where K is the center frequency gain and the bandwidth $\left(B = \frac{\omega_o}{Q}\right)$ is expressed as the ratio of center frequency ω_o and quality factor Q .

Bandpass filters have wide applications in transmitters and receivers. For RF front end applications, high selectivity bandpass filters are required to block out-of-band signals. Several active bandpass filters can be found in literature based on active inductors [18–20], active capacitance [21], and other techniques such as second generation current controlled conveyors (CCCIIs) [22]. The use of active inductors for building RF bandpass filters has also received a lot of attention. Even though passive monolithic integrated inductors can be used in CMOS processes, they are considered to be a poor choice due to the substrate

resistive losses, large chip area and low inductor quality factors [20]. In [19] first and second order active bandpass filters were derived by replacing a passive inductor with an active one realized using negative resistance circuits. In [18] an active inductor was used to produce high Q bandpass filter at RF frequencies. However, the use of active inductors can lead to complex circuit realizations, performance degradation due to high frequency parasitic effects, higher sensitivity and poor noise performance. Alternatively, researchers also tend to opt for off-chip inductors to avoid large parasitic capacitance and improve gain and noise performance [23]. Another realization of a bandpass filter was reported in [22] which operated in current mode employing two CCCIs and two capacitors, where implementation of each CCCIs required several MOS or bipolar transistors.

1.5 Bandstop or Notch Filter

As the name indicates, the property of a bandstop filter is to reject a particular band of frequencies. Like the bandpass filter, bandstop filter has two cutoff frequencies. It passes the signals below and above a certain range of frequencies, while attenuating signals between the two cutoff frequencies. Figure 1.2 (b) shows the ideal brick wall response of a bandstop filter. Conversely to a bandpass filter, the bandwidth of a bandstop filter refers to the range of frequencies that is blocked and is measured as the difference between the two 3 dB cutoff frequencies at the stopband. If ω_1 and ω_2 as shown in Figure 1.2 (b) are stopband edges, the bandwidth is given as

$$B = \omega_2 - \omega_1 \quad (1.7)$$

The center frequency ω_o of the stopband is the geometric mean of the cutoff frequencies defined as

$$\omega_o = \sqrt{\omega_1 \omega_2} \quad (1.8)$$

The characteristic transfer function of a second order notch filter is

$$T(s) = K \frac{s^2 + \omega_o^2}{s^2 + Bs + \omega_o^2} \quad (1.9)$$

where K is the DC and high frequency gain and the bandwidth $\left(B = \frac{\omega_o}{Q}\right)$ is expressed as the ratio of center frequency ω_o and quality factor Q .

Different realizations of notch filters can be found in literature. A gyrator¹ based active notch tunable filter [24, 25], a monolithic CMOS notch filter for RF image rejection applications [26], and a current mode bandstop circuit using a single current differencing buffered amplifier (CDBA) are among others. Bandstop filters find applications in signal processing and communication systems to reject certain bands of frequencies. For example, narrow band bandstop filters are extensively used in communication electronics to suppress spurious emissions or harmonics. In such cases where a very small band of frequencies are to be eliminated, the filter should have high selectivity or high quality factor Q .

1.6 Higher Order Filter Design

Real circuit elements usually deviate from their ideal behavior. Hence when we build a circuit using real components it is imperative to check their tolerances and know how they will affect the performance of the circuit. Monte Carlo simulations can be carried out to evaluate how the individual component tolerances affect the circuit performance. It is known that if the sensitivity is high, even small tolerances can produce significant performance variations. Hence circuits having small sensitivities to individual components are preferred. In [27], it was demonstrated that a direct realization of a higher order filter as a single block is not desirable as it makes the circuit very sensitive to component tolerances and hence unsuitable for practical applications. Another disadvantage of direct implemen-

¹A gyrator is a two-port component with a property of impedance inversion, that is, if the output port is terminated with a capacitor, the input port behaves like an inductor. They are mainly used to design inductorless filters.

tation is the use of several passive components. It was shown that cascading first or second order sections to realize higher order filters reduces sensitivities to circuit elements and is more beneficial than a direct implementation. Hence, higher order filters are generally designed using identical cascaded blocks. Thus the main goal will be to test the feasibility of the primary stage of the circuit, its equivalent transfer function and the resulting response in comparison to those in the specifications. It is also necessary to check the stability of these structures, which can be found from the pole and zero locations. All poles of a system should lie in the left half plane for a circuit to be stable. An advantage of the cascade design method is that it is easy to tune as it has only one pole pair per stage. However, we may need to use a buffer circuit between two stages to prevent loading. Also, higher order filters are known to have sharper rolloff and can achieve better out-of-band signal rejection. They are used in various areas such as to improve the dynamic range in analog fibre optic links by minimizing distortion [28], to achieve wideband tuning range [29] and in wireless data applications [30]. Classical active higher order filter realizations have at least one opamp as active element (implemented using at least seven or eight transistors) and some passive elements for each stage. In this work, second order topologies are introduced that use only one transistor as an active element and can be used to build higher order filters using a minimum number of circuit components.

1.7 Research Objectives

Higher order active filter realizations found in literature are complex and comprise the use of multiple active and passive elements. Some circuits are not suitable for integrated circuit implementations or tend to consume a large chip area. High power dissipation and cost is also a concern in such cases. The primary focus of this research was to develop topologies that have reduced element count, and can be easily implemented in integrated circuit (IC) form. To achieve this, new circuit topologies are proposed that will use only one transistor and a few passive components to design second order filter structures. The

previous work on single transistor filters presented in [15] demonstrated the feasibility of this type of circuits in generating different filters that can be operated from a low power supply and enable IC realization resulting in smaller chip area shown in [16]. In this work, novel single transistor topologies are presented and explored further to build higher order filters. The circuits were verified using Cadence Spectre simulations and experimental measurements.

1.8 Thesis Overview

In this thesis, different second and higher order filter circuits are presented, based on single transistor filter configurations. Chapter 2 introduces four general topologies where each of the single transistors are represented as two port networks. Simplified transfer functions of each topology are derived using two port transmission matrix equations considering an ideal MOS transistor. All possible second order filters generated from each of the general transfer functions are tabulated, along with their design parameters such as pole frequency ω_o , quality factor Q and gain K . Details of design procedures, biasing circuits, and non-ideal effects² of selected filter types are presented. Also, input and output impedances of the filters are derived for different frequencies. Chapter 3 shows the simulated and experimental results of the circuits designed in Chapter 2. The simulations were carried out using Cadence Spectre tool and the experimental measurements were done using discrete circuit elements. Chapter 4 introduces an active realization of a fourth order bandpass Chebyshev filter based on the second order bandpass filter. The complete design procedure and equations are presented. A comparison plot of the simulated and theoretical results are shown. Also, a two stage operational amplifier have been designed and connected in cascade to the Chebyshev filter to improve the overall gain of the filter. The simulation results showing the improvement in gain of the Chebyshev filter is presented. Experimental results of the designed filter is presented and compared with the theoretical ones. In Chapter 5, a fourth

²Non-ideal effects are considered by taking into account high frequency parasitic effects of transistors.

order Comb filter is presented and its design equations are tabulated. The simulation and experimental results of the designed filter are shown and compared with the theoretical ones. Finally, Chapter 6 gives the conclusion of the thesis and includes areas of further research based on this work.

CHAPTER 2

Single Transistor Active Filter

In the work of [15] single transistor active filters were first explored where the transistor was considered as a two port network surrounded by a minimum number of impedances that formed a Π -network. Six different configurations were introduced and an exhaustive search for all possible filters were performed using a MAPLE code. All valid second order filters of lowpass, highpass, bandpass and bandstop variety were reported.

In this chapter, new general configurations to realize single transistor second order filters are presented. Each of the proposed general circuits contain a single transistor as a two port network and three impedances that form a T-network. All possible second order filters are generated for each general transfer function using MAPLE search codes.

2.1 Proposed General Three Impedance Filter Topologies

Consider the circuit structure shown in Figure 2.1. It consists of a two port network surrounded by three impedances $Z_{1,2,3}$ that form a T-network. Terminal A is at AC ground, while the input and output are at terminals B and C, respectively. The circuit in Figure 2.1 is referred to as a Type-1 filter structure.

It is known that a two port network can be represented by the following transmission parameters

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} = [T] \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (2.1)$$

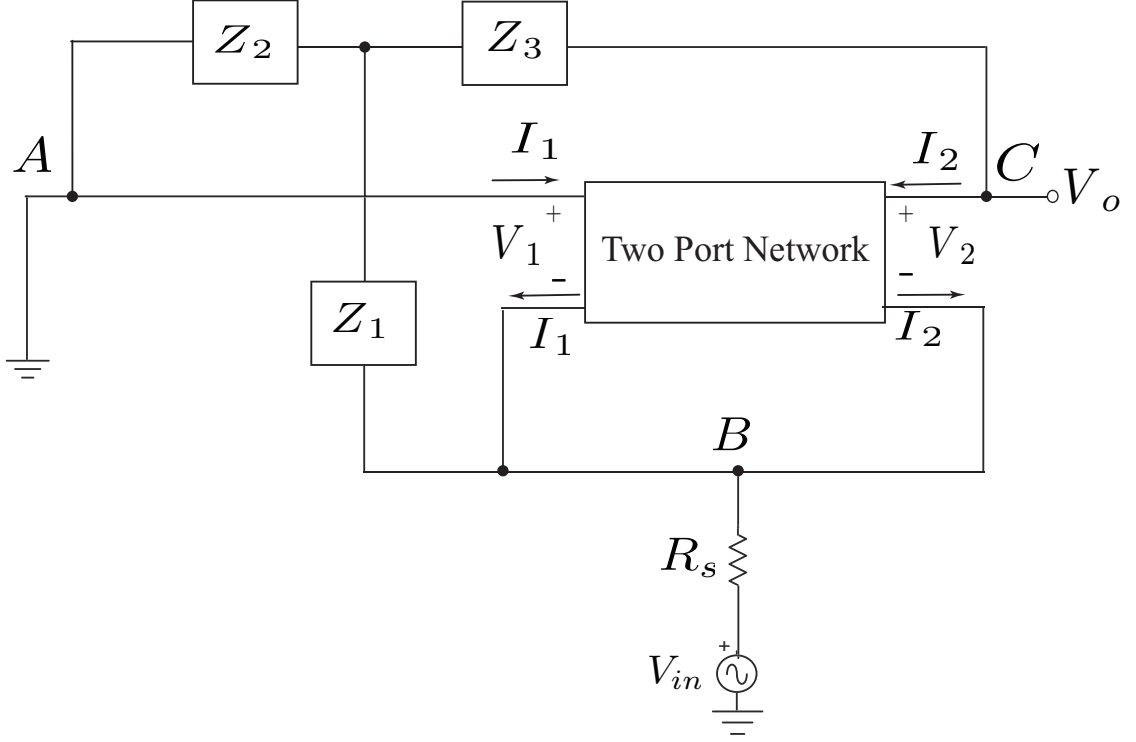


Figure 2.1: Type-1 filter topology with terminal A at AC ground

where V_1, I_1 are the voltage and current at the input port, whereas V_2, I_2 are the voltage and current at the output port. The coefficients $(a_{11}, a_{12}, a_{21}, a_{22})$ form the characteristic 2×2 transmission matrix that identifies the type of active element used as the two port. The coefficients a_{11} and a_{22} are dimensionless and represent the network's voltage and current gains respectively, whereas, a_{12} is the impedance and a_{21} is the admittance. Using nodal equations and two port transmission matrix equations, the transfer function of the Type-1 filter is obtained as

$$H_1(s) = \frac{V_o}{V_{in}} = \frac{a_{11}(Z_1Z_2 + Z_1Z_3 + Z_2Z_3) - Z_1Z_2 - Z_1Z_3 - Z_2Z_3 + a_{12}Z_2}{\Delta_{11}a_{11} + \Delta_{21}a_{21} + \Delta_{31}a_{22} + a_{12}(R_s + Z_1 + Z_2) - R_sZ_1} \quad (2.2)$$

where

$$\Delta_{11} = R_s(Z_1 - Z_1 a_{22} + Z_3) + Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 \quad (2.3)$$

$$\Delta_{21} = R_s(Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 + Z_1 a_{12}) \quad (2.4)$$

and

$$\Delta_{31} = R_s(Z_1 + Z_2) \quad (2.5)$$

Next consider the circuit shown in Figure 2.2 where the AC ground is at terminal C and the input and output are at terminals A and B, respectively. This circuit is denoted as the Type-2 filter. Once again, by circuit analysis the Type-2 transfer function is found to be

$$H_2(s) = \frac{V_o}{V_{in}} = \frac{a_{22}(Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3) - Z_1 Z_2 - Z_1 Z_3 - Z_2 Z_3 + a_{12} Z_3}{\Delta_{12} a_{11} + \Delta_{22} a_{21} + \Delta_{32} a_{22} + a_{12}(R_s + Z_2 + Z_3) - R_s Z_1 - Z_1 Z_2 - Z_1 Z_3 - Z_2 Z_3} \quad (2.6)$$

where

$$\Delta_{12} = R_s(Z_1 + Z_3) + Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 - a_{22}(R_s Z_1 + Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3) \quad (2.7)$$

$$\Delta_{22} = R_s(Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 + Z_1 a_{12}) + (Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3) a_{12} \quad (2.8)$$

and

$$\Delta_{32} = R_s(Z_1 + Z_2) + Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 \quad (2.9)$$

Finally, consider the Type-3 filter topology shown in Figure 2.3. This time, the input and output are at terminals A and C, while terminal B is grounded. Nodal analysis of the

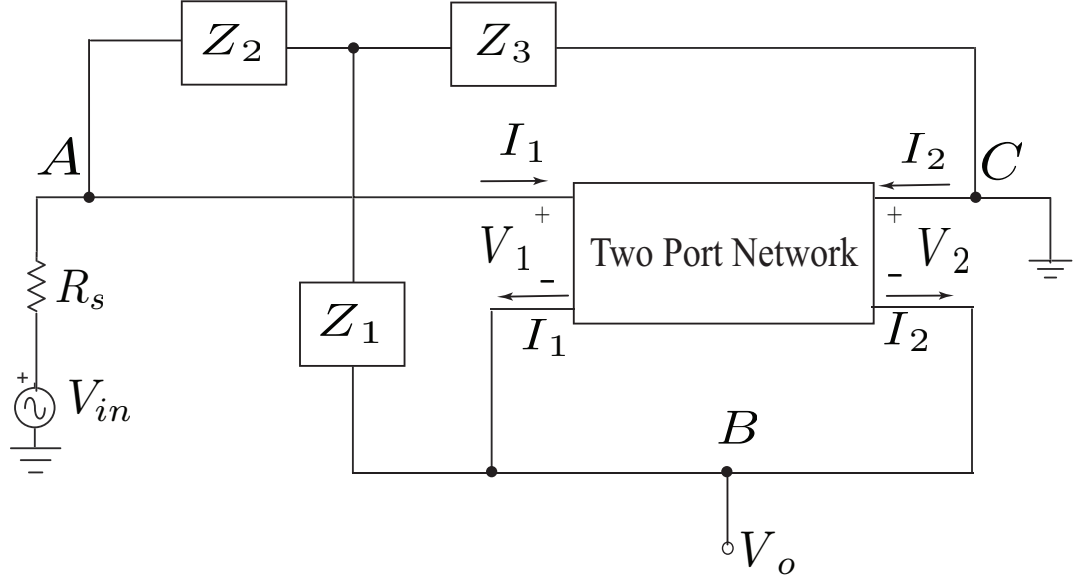


Figure 2.2: Type-2 filter structure with terminal C at AC ground

structure yields the following transfer function

$$H_3(s) = \frac{V_o}{V_{in}} = \frac{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 + a_{12} Z_1}{\Delta_{13} a_{11} + \Delta_{23} a_{21} + \Delta_{33} a_{22} + a_{12} (R_s + Z_1 + Z_2) - R_s Z_1} \quad (2.10)$$

where

$$\Delta_{13} = R_s (Z_1 - Z a_{22} + Z_3) + Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 \quad (2.11)$$

$$\Delta_{23} = R_s (Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 + Z_1 a_{12}) \quad (2.12)$$

and

$$\Delta_{33} = R_s (Z_1 + Z_2) \quad (2.13)$$

Since a single transistor active filter design is targeted, the two port network can be

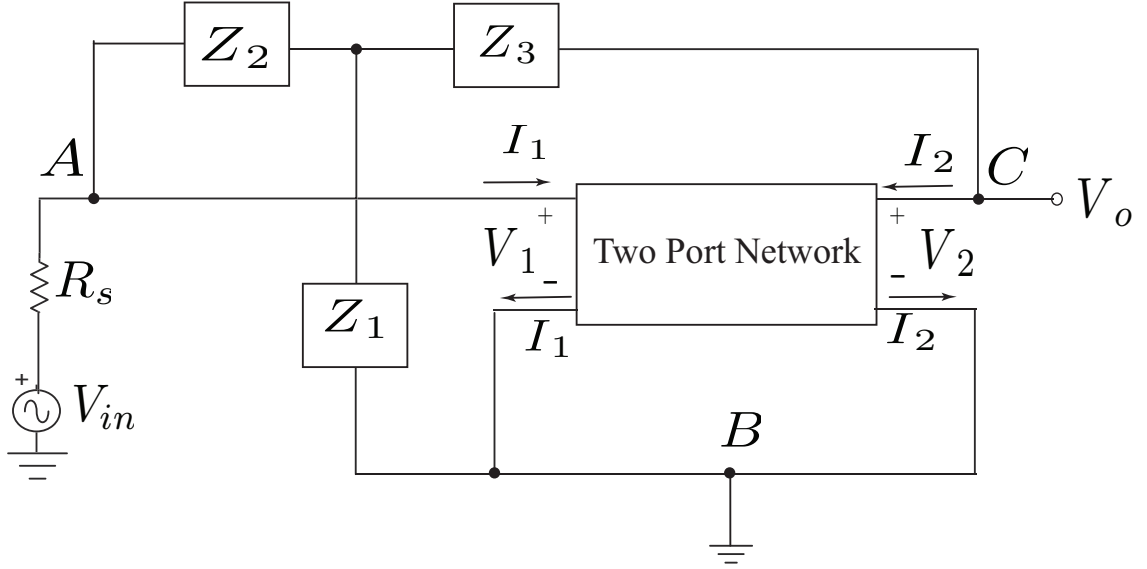


Figure 2.3: Type-3 filter topology with terminal B at AC ground

modeled as a Bipolar Junction Transistor (BJT) or a Metal-Oxide-Semiconductor (MOS) transistor. In this thesis, an ideal MOS transistor is used in the two port network and it is characterized by the transmission matrix given as

$$[T] = \begin{bmatrix} 0 & -\frac{1}{g_m} \\ 0 & 0 \end{bmatrix} \quad (2.14)$$

where $a_{11} = a_{21} = a_{22} = 0$, and $a_{12} = -\frac{1}{g_m}$ where g_m is the small signal transconductance. The two port network parameters for a MOS transistor can be described as $V_1 = V_{gs}$, $I_1 = I_g$, $V_2 = V_{ds}$ and $I_2 = I_{ds}$. More complex transistor models that show the effects of drain to source resistance r_o , and high frequency parasitic capacitances such as gate to source capacitance, C_{gs} and gate to drain capacitance C_{gd} can also be used, as shown in Section 2.4.6. However, in this work the ideal transistor model is used to design single transistor filters and to determine the filter type. Substituting the ideal transistor matrix parameters in the Type-1, Type-2 and Type-3 transfer functions given by equations (2.2), (2.6) and (2.10) yields simplified transfer functions listed in Table 2.1.

Topology	Transfer Function
Type-1	$H_1(s) = \frac{(Z_1 g_m + Z_3 g_m + 1)Z_2 + Z_1 Z_3 g_m}{(Z_1 g_m + 1)R_s + Z_1 + Z_2}$
Type-2	$H_2(s) = \frac{(Z_1 g_m + Z_3 g_m)Z_2 + (Z_1 g_m + 1)Z_3}{(Z_1 g_m + 1)R_s + (Z_1 g_m + Z_3 g_m + 1)Z_2 + (Z_1 g_m + 1)Z_3}$
Type-3	$H_3(s) = \frac{Z_1 - (Z_1 g_m + Z_3 g_m)Z_2 - Z_1 Z_3 g_m}{(Z_1 g_m + 1)R_s + Z_1 + Z_2}$

Table 2.1: Type-1, Type-2 and Type-3 transfer functions using an ideal transistor

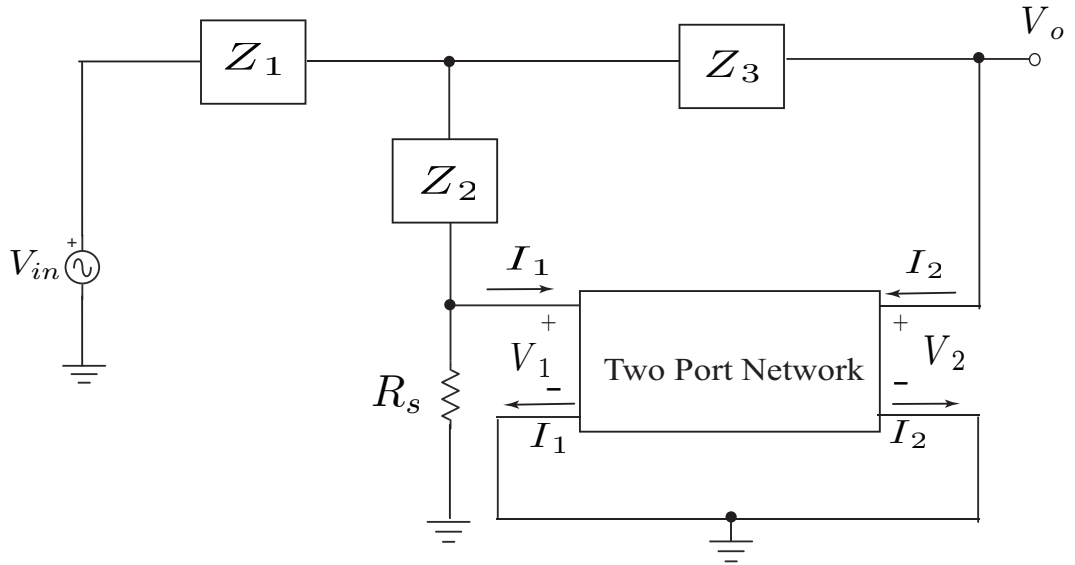


Figure 2.4: Altered Type-3 filter structure with R_s as an external resistor

2.2 Variation of Type-3 Filter Structure¹

Consider the filter topology shown in Figure 2.4. It is a variation of the general Type-3 filter structure given in Figure 2.3, obtained by exchanging the grounded terminal of Z_1 and V_{in} . In this case, R_s is used as an external resistor rather than as an internal source resistance and is connected to Z_2 and the input terminal of the two port network. Once again by circuit analysis, we find the transfer function of the new Type-3 filter topology to be

¹Variations of Type-1 and Type-2 filter structures were attempted but did not yield any valid second order filters.

$$\hat{H}_3(s) = \frac{V_o}{V_{in}} = \frac{R_s Z_2 a_{22} + R_s Z_3 + a_{12}(R_s + Z_2)}{\hat{\Delta}_1 a_{11} + \hat{\Delta}_2 a_{21} + \hat{\Delta}_3 a_{22} + a_{12}(R_s + Z_1 + Z_2) - R_s Z_1} \quad (2.15)$$

where

$$\hat{\Delta}_{13} = R_s (Z_1 - Z a_{22} + Z_3) + Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 \quad (2.16)$$

$$\hat{\Delta}_{23} = R_s (Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 + Z_1 a_{12}) \quad (2.17)$$

$$\hat{\Delta}_{33} = R_s (Z_1 + Z_2) \quad (2.18)$$

Substituting the ideal transistor matrix parameters ($a_{11} = a_{21} = a_{22} = 0, a_{12} = -\frac{1}{g_m}$) in the transfer function given by equation (2.15) yields a simplified expression

$$\hat{H}_3(s) = \frac{V_o}{V_{in}} = \frac{Z_2 - (Z_3 g_m - 1) R_s}{(Z_1 g_m + 1) R_s + Z_1 + Z_2} \quad (2.19)$$

2.3 All possible filter types

An exhaustive search for all possible three impedance single transistor second order filters was performed in MAPLE for different impedance combinations of each filter topology. The combinations of $Z_{1,2,3}$ in the search code consist of no more than two resistors (excluding resistor R_s) and two storage elements (capacitors and inductors). The results of this search was then compared to the second order transfer function

$$H(s) = K \frac{N(s)}{s^2 + Bs + \omega_o^2} \quad (2.20)$$

to determine the type of filter. For example, $N(s) = \omega_o^2$ gives a lowpass filter, $N(s) = Bs$ gives a bandpass filter, $N(s) = s^2$ gives a highpass filter, $N(s) = s^2 + \omega_o^2$ gives a bandstop

filter, $N(s) = s^2 - Bs + \omega_o^2$ gives an allpass filter and $N(s) = s^2 + B_1s + \omega_o^2$, where $B_1 \neq B$ gives a gain equalizer (GE). Gain K , pole frequency ω_o , and quality factor Q expressions are also found from MAPLE. All possible impedance combinations were considered and the valid second order filters obtained from MAPLE for each filter topology are presented in Tables 2.2, 2.3 , 2.4 and 2.5.

Note it is possible to obtain allpass filters from selected gain equalizer filters if they fulfill the condition $Q = -Q_z$, where Q_z is the zero quality factor. For example, for the gain equalizer filters #1 and #3 in Table 2.4, solving for R_s under the condition $Q = -Q_z$ yielded

$$R_s = \frac{R_2(1 - g_m(R_2 + 2R_3))}{R_2g_m(R_3g_m + 1) + R_3g_m - 1}$$

which shows that the circuits work as allpass filters as long as $g_m(R_2 + 2R_3) < 1$. Similarly, R_s for the gain equalizer filter #2 of Table 2.4 was obtained as

$$R_s = \frac{R_1(1 - g_m(R_1 + 2R_3))}{g_m(R_1 + R_3)(R_1g_m + 1)} \quad (2.21)$$

and the filter works as an allpass if $g_m(R_1 + 2R_3) < 1$. The gain equalizer filters #1 and #3 in Table 2.5 was found to work as allpass filters and the expression of R_3 under the condition $Q = -Q_z$ was found to be

$$R_3 = \frac{R_1(R_sg_m + 1) + 2R_s}{R_sg_m} \quad (2.22)$$

2.4 Discussion of Selected Filters

In this section, full circuit implementations, biasing requirements² and non-ideal effects of selected filters are presented. Designs of different filter types such as bandpass, bandstop, and allpass filters from Table 2.5 are shown. Input and output impedances of each circuit

²For most of the filters one DC current source suffice to bias the transistor. However, it was found that some filters require an extra biasing network, as discussed in Section 2.4.5.

Topology	$Z_{1,2,3}$	Pole Frequency: ω_o Gain, K	Quality Factor, Q Zero Quality Factor, Q_z	Extra Biasing
	Filter			
Type-1	$R_1, L_2 + C_2, R_3$ GE (#1)	$\frac{1}{\sqrt{C_2 L_2}}$ $R_1 g_m + R_3 g_m + 1$	$\left(\sqrt{\frac{L_2}{C_2}}\right) \frac{1}{R_1 R_s g_m + R_1 + R_s}$ $\left(\sqrt{\frac{L_2}{C_2}}\right) \frac{R_1 g_m + R_3 g_m + 1}{R_1 R_3 g_m}$	Yes
	$L_1 + C_1, R_2, R_3$ GE (#2)	$\frac{1}{\sqrt{C_1 L_1}}$ $\frac{g_m(R_2 + R_3)}{R_s g_m + 1}$	$\left(\sqrt{\frac{L_1}{C_1}}\right) \frac{R_s g_m + 1}{R_2 + R_s}$ $\left(\sqrt{\frac{L_1}{C_1}}\right) \frac{g_m(R_2 + R_3)}{R_2(R_3 g_m + 1)}$	No
	$R_1, L_2 \parallel C_2, R_3$ GE (#3)	$\frac{1}{\sqrt{C_2 L_2}}$ $\frac{R_1 R_3 g_m}{R_1 R_s g_m + R_1 + R_s}$	$\left(\sqrt{\frac{C_2}{L_2}}\right) R_1 R_s g_m + R_1 + R_s$ $\left(\sqrt{\frac{C_2}{L_2}}\right) \frac{R_1 R_3 g_m}{R_1 g_m + R_3 g_m + 1}$	No
	$L_1 \parallel C_1, R_2, R_3$ GE (#4)	$\frac{1}{\sqrt{C_1 L_1}}$ $\frac{R_2(R_3 g_m + 1)}{(R_2 + R_3)}$	$\left(\sqrt{\frac{C_1}{L_1}}\right) \frac{(R_2 + R_s)}{(R_s g_m + 1)}$ $\left(\sqrt{\frac{C_1}{L_1}}\right) \frac{R_2(R_3 g_m + 1)}{g_m(R_2 + R_3)}$	No

Table 2.2: All possible second order filters for Type-1 filter configuration

are also derived.

2.4.1 Bandpass Filter

The Type-3 bandpass filter #2 from Table 2.5 is designed as shown in Figure 2.5. One of the three impedances is a series LC network and the other two impedances are resistors. This can also be called a LC resonance based filter where the capacitor and inductor values control the center or pole frequency. A DC current source I_b is connected from the drain of the MOS transistor to the supply voltage V_{dd} to ensure proper biasing. The expressions of the design parameters Q , K and ω_o are given in Table 2.5.

Since the bandpass filter is a resonance based filter it will have quality factor, $Q > \frac{1}{2}$ which requires $L_1 > \frac{R_2 + R_s}{2(R_s g_m + 1)\omega_o}$, resulting in complex poles. To obtain a characteristic response of a second order bandpass filter, the general transfer function given by equation

Topology	$Z_{1,2,3}$	Pole Frequency: ω_o Gain, K	Quality Factor, Q Zero Quality Factor, Q_z	Extra Biasing
	Filter			
Type-2	$R_1, R_2, L_3 + C_3$ GE (#1)	$\frac{1}{\sqrt{C_3 L_3}}$ 1	$\left(\sqrt{\frac{L_3}{C_3}}\right) \frac{g_m(R_1+R_2)+1}{(R_2+R_s)(R_1 g_m+1)}$ $\left(\sqrt{\frac{L_3}{C_3}}\right) \frac{g_m(R_1+R_2)+1}{R_1 R_2 g_m}$	No
	$R_1, L_2 + C_2, R_3$ GE (#2)	$\frac{1}{\sqrt{C_2 L_2}}$ $\frac{g_m(R_1+R_3)}{g_m(R_1+R_3)+1}$	$\left(\sqrt{\frac{L_2}{C_2}}\right) \frac{g_m(R_1+R_3)+1}{(R_3+R_s)(R_1 g_m+1)}$ $\left(\sqrt{\frac{L_2}{C_2}}\right) \frac{g_m(R_1+R_3)}{R_3(R_1 g_m+1)}$	No
	$L_1 + C_1, R_2, R_3$ GE (#3)	$\frac{1}{\sqrt{C_1 L_1}}$ $\frac{R_2+R_3}{R_2+R_s+R_3}$	$\left(\sqrt{\frac{L_1}{C_1}}\right) \frac{g_m(R_2+R_s+R_3)}{R_2+R_s+R_3(R_2 g_m+1)}$ $\left(\sqrt{\frac{L_1}{C_1}}\right) \frac{g_m(R_2+R_3)}{R_3(R_2 g_m+1)}$	No
	$R_2, R_3, L_3 \parallel C_3$ GE (#4)	$\frac{1}{\sqrt{C_3 L_3}}$ $\frac{R_1 R_2 g_m}{(R_2+R_s)(R_1 g_m+1)}$	$\left(\sqrt{\frac{C_3}{L_3}}\right) \frac{(R_2+R_s)(R_1 g_m+1)}{g_m(R_1+R_2)+1}$ $\left(\sqrt{\frac{C_3}{L_3}}\right) \frac{R_1 R_2 g_m}{g_m(R_1+R_2)+1}$	No
	$R_1, L_2 \parallel C_2, R_3$ GE (#5)	$\frac{1}{\sqrt{C_2 L_2}}$ $\frac{R_3}{R_s+R_3}$	$\left(\sqrt{\frac{C_2}{L_2}}\right) \frac{(R_3+R_s)(R_1 g_m+1)}{g_m(R_1+R_3)+1}$ $\left(\sqrt{\frac{C_2}{L_2}}\right) \frac{R_3(R_1 g_m+1)}{g_m(R_1+R_3)}$	No
	$L_1 \parallel C_1, R_2, R_3$ GE (#6)	$\frac{1}{\sqrt{C_1 L_1}}$ $\frac{R_3(R_2 g_m+1)}{R_2+R_s+R_3(R_2 g_m+1)}$	$\left(\sqrt{\frac{C_1}{L_1}}\right) \frac{R_2+R_s+R_3(R_2 g_m+1)}{g_m(R_2+R_s+R_3)}$ $\left(\sqrt{\frac{C_1}{L_1}}\right) \frac{R_3(R_2 g_m+1)}{g_m(R_2+R_3)}$	No

Table 2.3: All possible second order filters for Type-2 filter structure

(1.6) is plotted in MATLAB for a Q of 2.5, pole frequency, $f_o = 16.3$ MHz and center frequency gain $K = 0.99$. The magnitude and phase responses are shown in Figure 2.6. The expression for the center frequency gain K given in Table 2.5 (filter #2) show that the gain cannot be greater than 1 as it will lead to one of the resistors or g_m becoming negative which is not possible.

Topology	$Z_{1,2,3}$	Pole Frequency: ω_o Gain, K	Quality Factor, Q Zero Quality Factor, Q_z	Extra Biasing
	Filter			
Type-3	$L_1 + C_1, R_2, R_3$ GE or AP (#1)	$\frac{1}{\sqrt{C_1 L_1}}$ $\frac{1 - g_m(R_2 + R_3)}{(R_s g_m + 1)}$	$\left(\sqrt{\frac{L_1}{C_1}}\right) \frac{(R_s g_m + 1)}{R_2 + R_s}$ $\left(\sqrt{\frac{L_1}{C_1}}\right) \frac{g_m(R_2 + R_3) - 1}{R_3 R_2 g_m}$	No
	$R_1, L_2 \parallel C_2, R_3$ GE or AP (#2)	$\frac{1}{\sqrt{C_2 L_2}}$ $\frac{R_1(1 - R_3 g_m)}{R_s(g_m R_1 + 1) + R_1}$	$\left(\sqrt{\frac{C_2}{L_2}}\right) (R_s(g_m R_1 + 1) + R_1)$ $\left(\sqrt{\frac{C_2}{L_2}}\right) \frac{R_1(R_3 g_m - 1)}{g_m(R_1 + R_3)}$	No
	$L_1 \parallel C_1, R_2, R_3$ GE or AP (#3)	$\frac{1}{\sqrt{C_1 L_1}}$ $-\frac{R_2 R_3 g_m}{R_2 + R_s}$	$\left(\sqrt{\frac{C_1}{L_1}}\right) \frac{R_2 + R_s}{(R_s g_m + 1)}$ $\left(\sqrt{\frac{C_1}{L_1}}\right) \frac{R_2 R_3 g_m}{g_m(R_2 + R_3) - 1}$	No

Table 2.4: All possible second order filters for Type-3 filter structure

Topology	$Z_{1,2,3}$	Pole Frequency: ω_o Gain, K	Quality Factor, Q Zero Quality Factor, Q_z	Extra Biasing
	Filter			
Alternate Type-3 Filter	$R_1, L_2 + C_2, R_3$ GE or AP (#1)	$\frac{1}{\sqrt{C_2 L_2}}$ 1	$\left(\sqrt{\frac{L_2}{C_2}}\right) \frac{1}{R_1 R_s g_m + R_1 + R_s}$ $\left(\sqrt{\frac{L_2}{C_2}}\right) \frac{1}{R_s(1 - R_3 g_m)}$	Yes
	$L_1 + C_1, R_2, R_3$ Bandpass (#2)	$\frac{1}{\sqrt{C_1 L_1}}$ $1 - \frac{R_3 R_s g_m}{R_2 + R_3}$	$\left(\sqrt{\frac{L_1}{C_1}}\right) \frac{R_s g_m + 1}{R_2 + R_s}$ -	No
	$R_1, L_2 \parallel C_2, R_3$ GE or AP (#3)	$\frac{1}{\sqrt{C_2 L_2}}$ $\frac{R_s(R_3 g_m - 1)}{R_1 R_s g_m + R_1 + R_s}$	$\left(\sqrt{\frac{C_2}{L_2}}\right) R_1 R_s g_m + R_1 + R_s$ $\left(\sqrt{\frac{C_2}{L_2}}\right) R_s(1 - R_3 g_m)$	No
	$L_1 \parallel C_1, R_2, R_3$ Bandstop (#4)	$\frac{1}{\sqrt{C_1 L_1}}$ $1 - \frac{R_3 R_s g_m}{R_2 + R_3}$	$\left(\sqrt{\frac{C_1}{L_1}}\right) \frac{(R_2 + R_s)}{(R_s g_m + 1)}$ -	No

Table 2.5: All possible filters of an altered Type-3 filter topology of Figure 2.4.

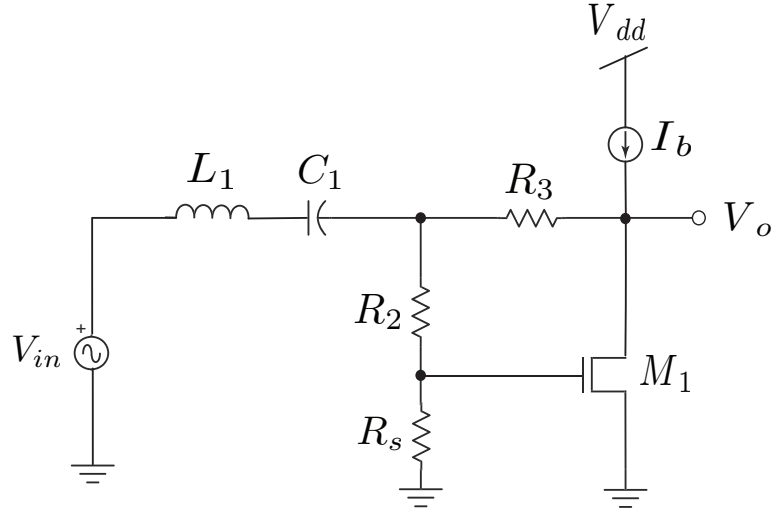


Figure 2.5: Second order bandpass filter using a single transistor

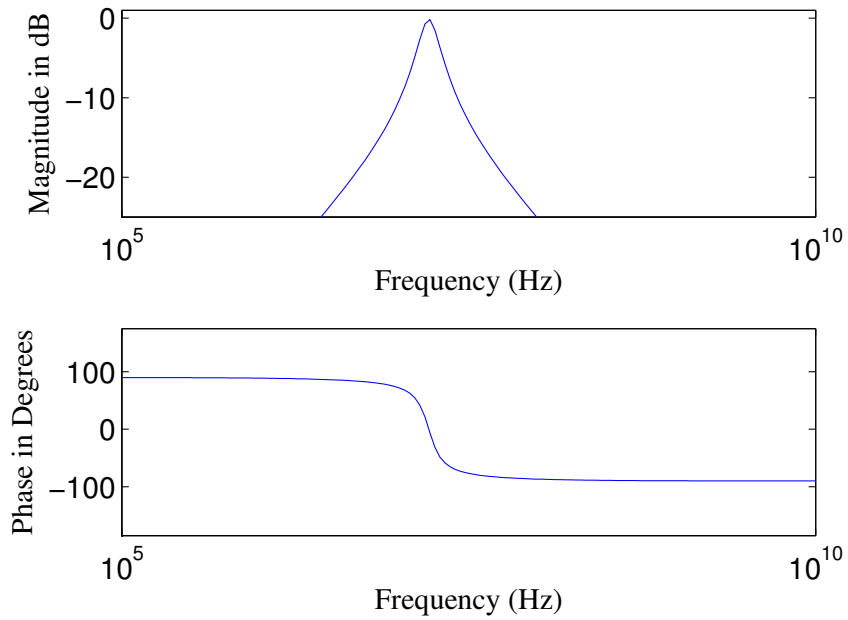


Figure 2.6: General bandpass filter transfer function plotted in MATLAB at $f_o = 16.3$ MHz, $K = 0.99$ and $Q = 2.5$

2.4.1.1 Input and Output impedance of Bandpass Filter

The expression of input impedance Z_{in} of the second order bandpass filter found looking into the circuit from the right of the source is given as

$$Z_{in}(s) = \frac{s^2 C_1 L_1 (R_s g_m + 1) + s C_1 (R_2 + R_s) + (R_s g_m + 1)}{s C_1 (R_s g_m + 1)} \quad (2.23)$$

From the bandpass circuit in Figure 2.5 it is observed that the input impedance is very high due to the series LC component used as Z_1 , where either the inductor or the capacitor will simulate an open circuit at very high and low frequencies, respectively. At low frequencies, Z_{in} is reduced to $1/sC_1$ and at very high frequencies, it becomes sL_1 . Hence this circuit will not be suitable for cascading multiple stages or adding a load stage without the use of a unity gain buffer between them to prevent loading. At the resonance or pole frequency the reactive components cancel each other, that is, Z_1 gets shorted and the input impedance is obtained as

$$Z_{in} = \frac{R_2 + R_s}{R_s g_m + 1} \quad (2.24)$$

The output impedance of the bandpass circuit is obtained as

$$Z_{out}(s) = \frac{s^2 C_1 L_1 (R_2 + R_3 + R_s) + s C_1 R_3 (R_2 + R_s) + (R_2 + R_3 + R_s)}{s^2 C_1 L_1 (R_s g_m + 1) + s C_1 (R_2 + R_s) + (R_s g_m + 1)} \quad (2.25)$$

At very high and low frequencies, Z_1 acts as an open circuit and the equivalent circuit diagram is shown in Figure 2.7. From straightforward circuit analysis, it can be shown that $Z_{out} = \frac{(R_2 + R_3 + R_s)}{(R_s g_m + 1)}$. Whereas, at pole frequency, Z_1 is shorted to ground due to the reactances canceling each other and resulting in the circuit seeing an output impedance of $Z_{out} = R_3$. The equivalent circuit diagram to find output impedance at the pole frequency is shown in Figure 2.8.

In the initial circuit analysis of the alternate Type-3 filters, R_s was treated as an external resistor and the internal resistance (R_{in}) of the source generator was ignored. To consider any possible effect of R_{in} , the nodal equations and transfer function are adjusted. This gives rise to altered Q and K expressions, which show the additional terms introduced by

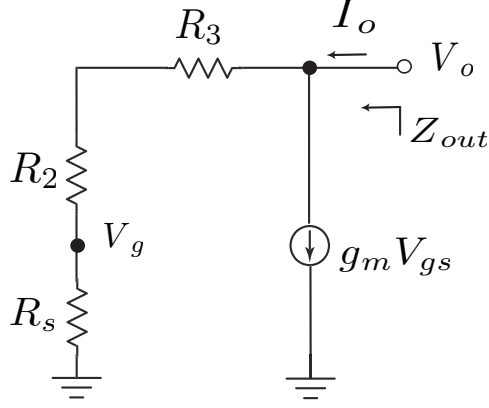


Figure 2.7: Small signal diagram to find Z_{out} at very high and low frequencies

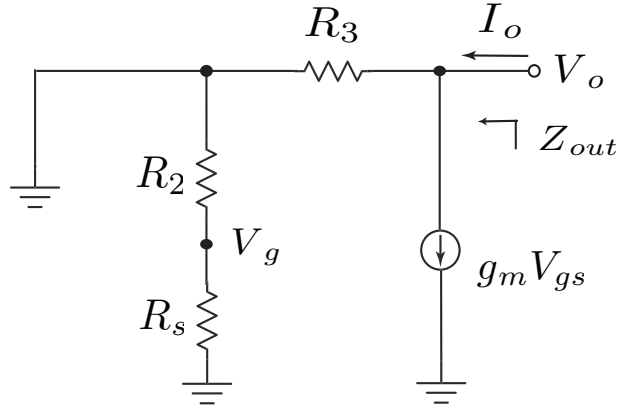


Figure 2.8: Small signal diagram to find Z_{out} at pole frequency

R_{in} in the denominator that will adversely affect the quality factor and DC gain. The pole frequency, however, remains unchanged. Hence ideally R_{in} should be as small as possible as it reduces Q and K as shown in equations 2.26 and 2.27, respectively,

$$Q = \frac{L_1 (R_s g_m + 1) \sqrt{\frac{1}{C_1 L_1}}}{R_2 + R_s + R_{in} (R_s g_m + 1)} \quad (2.26)$$

$$K = \frac{R_2 + R_s - R_3 R_s g_m}{R_2 + R_s + R_{in} (R_s g_m + 1)} \quad (2.27)$$

As can be observed from circuit analysis, the input impedance at the pole frequency due to R_{in} is $Z_{in} = R_{in} + \frac{R_2 + R_s}{R_s g_m + 1}$ and the output impedance at the pole frequency becomes $Z_{out} = \frac{R_{in} (R_2 + R_3 + R_s) + R_3 (R_2 + R_s)}{R_{in} (R_s g_m + 1) + (R_2 + R_s)}$.

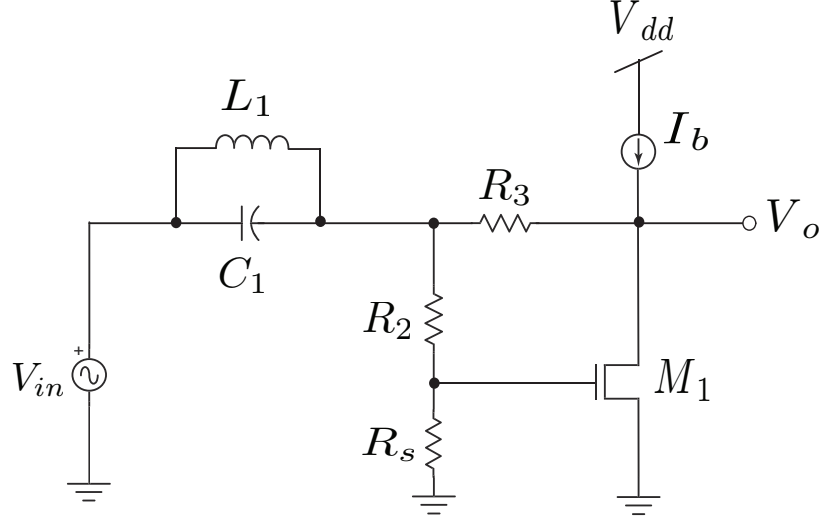


Figure 2.9: Second order bandstop filter topology

2.4.2 Bandstop or Notch Filter

The Type-3 active bandstop filter #4 from Table 2.5 was designed as shown in Figure 2.9, where one of the three impedances is a parallel LC network and the other two impedances are resistors. Again the resonance frequency of the LC parallel network coincides with the pole frequency of the notch filter. A current source I_b is used for biasing the transistor.

The expressions of the design parameters Q , K and ω_o are given in Table 2.5. To obtain a characteristic notch circuit response the second order notch transfer function given by equation (1.9) is plotted in MATLAB. The magnitude and phase responses for $Q = 2$, $K = 0.99$ and pole frequency $f_o = 16.3$ MHz are shown in Figure 2.10. Similar to the bandpass filter case, the DC gain K of the notch filter cannot be greater than unity, as either the resistors or g_m will become negative.

2.4.2.1 Input and Output Impedance of the Bandstop Filter

By circuit analysis, the expression of input impedance Z_{in} of the second order notch filter was found to be

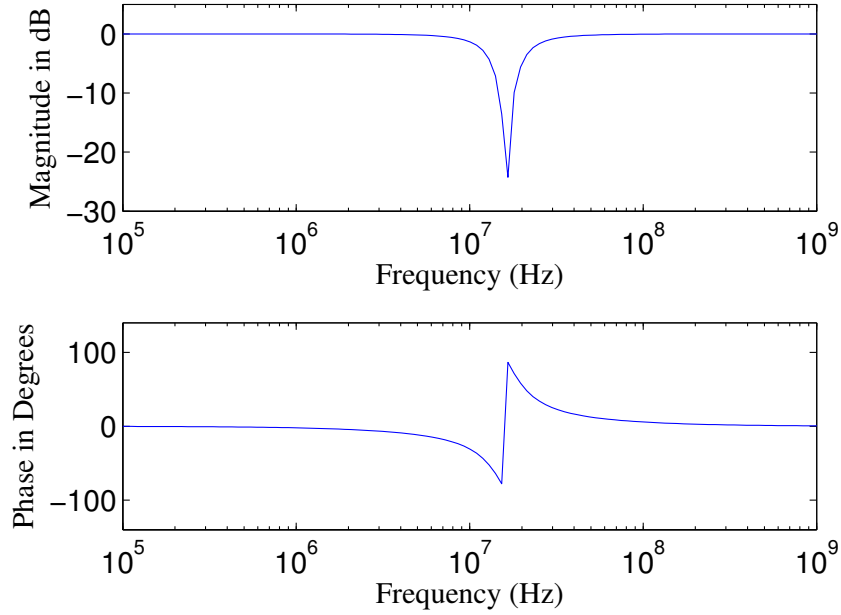


Figure 2.10: General bandstop filter transfer function plotted in MATLAB for $f_o = 16.3$ MHz, $K = 0.99$ and $Q = 2$

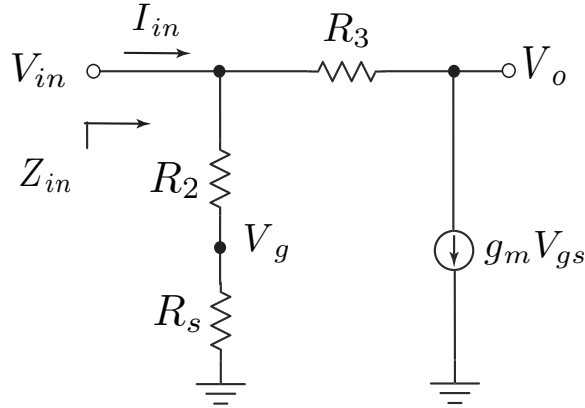


Figure 2.11: Small signal diagram to find Z_{in} of the notch circuit at very high frequencies

$$Z_{in}(s) = \frac{s^2 C_1 L_1 (R_2 + R_s) + s L_1 (R_s g_m + 1) + (R_2 + R_s)}{(s^2 C_1 L_1 + 1)(R_s g_m + 1)} \quad (2.28)$$

To find the input impedance at very high frequencies, Z_1 can be replaced by a short circuit as the inductor acts as an open circuit and the capacitor gets shorted. The equivalent bandstop filter is shown in Figure 2.11. By analyzing the circuit it is found that Z_{in} at high frequencies is expressed as $Z_{in} = \frac{R_2 + R_s}{R_s g_m + 1}$. This is also true for low frequencies where the

inductor is shorted and capacitor acts as an open circuit. At resonance frequency, however, the input impedance approaches infinity because the inductive and capacitive reactances equal each other and the LC tank circuit is replaced by an open circuit, thus presenting a high impedance to a narrow range of frequencies.

Output impedance is found to be $Z_{out} = R_3$ at low and high frequencies, where the signal source is set to zero ($V_{in}=0$) and Z_1 is connected to ground. The equivalent circuit diagram is the same as the one shown in Figure 2.8 but in this case for high frequencies. Consider the circuit in Figure 2.7 to find output impedance of the notch filter at resonance frequency. The output impedance expression is found to be $Z_{out} = \frac{(R_2+R_3+R_s)}{(R_s g_m + 1)}$ at resonance frequency, where the Z_1 branch is replaced with an open circuit.

To consider the effect of signal source resistance R_{in} for the notch circuit the nodal equations are adjusted to include R_{in} resulting in new expression for transfer function. New expressions of Q and K due to R_{in} are found to be

$$Q = C_1 \sqrt{\frac{1}{C_1 L_1}} \frac{R_{in} (R_s g_m + 1) + R_s + R_2}{R_s g_m + 1} \quad (2.29)$$

$$K = \frac{R_2 + R_s - R_3 R_s g_m}{R_2 + R_s + R_{in} (R_s g_m + 1)} \quad (2.30)$$

Input impedance due to R_{in} is $Z_{in} = R_{in} + \frac{R_2 + R_s}{R_s g_m + 1}$ at low and high frequencies and output impedance is $Z_{out} = \frac{R_{in} (R_2 + R_3 + R_s) + R_3 (R_2 + R_s)}{R_{in} (R_s g_m + 1) + (R_2 + R_s)}$. As expected output impedance at resonance frequency is not affected by R_{in} as the entire branch with Z_1 becomes an open circuit.

2.4.3 Allpass Filter

The Type-3 allpass filter #3 from Table 2.5 is designed as shown in Figure 2.12, which employs a parallel LC network as Z_2 and two resistors as Z_1 and Z_3 . This can also be called a LC resonance based filter where the capacitor and inductor values control the resonance or pole frequency. The expressions of design parameters ω_o , Q , Q_z (zero quality factor)

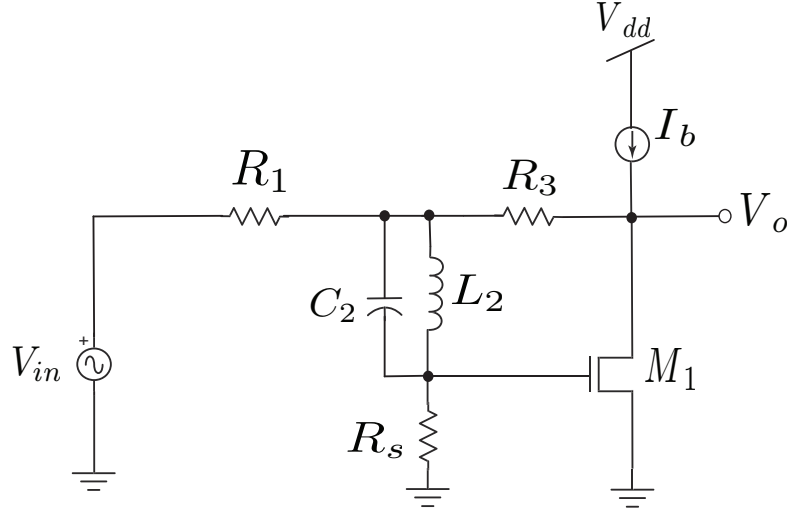


Figure 2.12: Second order AP filter structure

and K are given in Table 2.5.

A general transfer function of an allpass filter given as

$$H(s) = \frac{V_o}{V_{in}}(s) = K \frac{\left(s^2 - \frac{\omega_o}{Q_z}s + \omega_z^2\right)}{\left(s^2 + \frac{\omega_o}{Q}s + \omega_o^2\right)} \quad (2.31)$$

was plotted in MATLAB. The magnitude and phase responses for $Q = |Q_z| = 1$, $K = 1$, and $f_o = 16.3$ MHz are shown in Figure 2.13.

2.4.3.1 Input and Output Impedance of the Allpass Filter

At high frequencies C_2 gets shorted and L_2 becomes an open circuit, whereas, the opposite is true for low frequencies, where the capacitor is open and the inductor is shorted. In both cases, Z_2 can be replaced as a short circuit. The equivalent circuit diagram to find input impedance is shown in Figure 2.14. By circuit analysis, it can be shown that at low and high

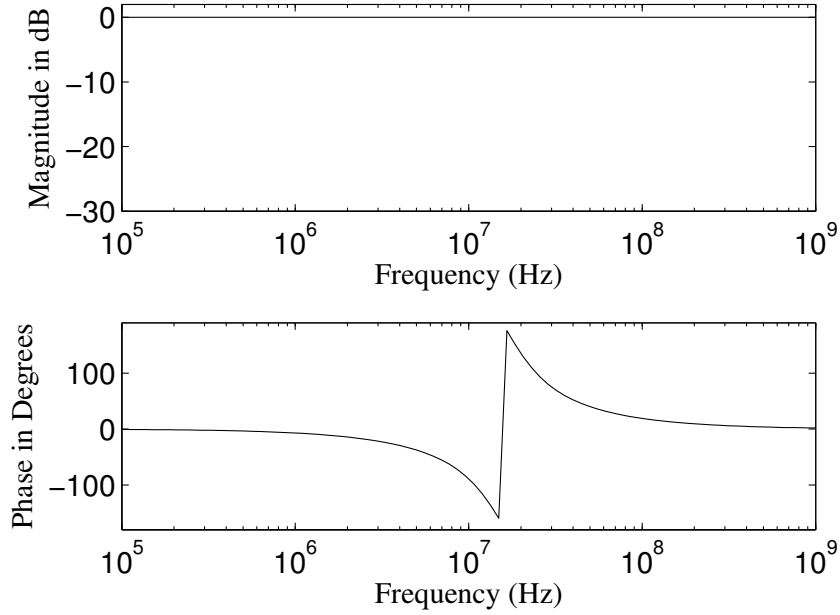


Figure 2.13: General allpass filter transfer function plotted in MATLAB for $f_o = 16.3$ MHz, $K = 1$ and $Q = |Q_z| = 1$

frequencies, $Z_{in} = \frac{R_1(R_s g_m + 1) + R_s}{(R_s g_m + 1)}$. At pole frequency, input impedance approaches infinity as L_2 and C_2 resonate with each other and is replaced by an open circuit. To find the output impedance, the input voltage is set to zero that connects R_1 to ground. From circuit analysis the output impedance is found to be $Z_{out} = R_1 + R_3$ at the pole frequency where Z_2 is an open circuit. At very high and low frequencies, it becomes $Z_{out} = \frac{R_3^2}{R_3 + (R_1 \parallel R_s \parallel R_3)(g_m R_3 - 1)}$ where Z_2 is shorted as illustrated in Figure 2.15.

2.4.4 Effect of g_m

From the expressions of design parameters K , Q and ω_o of the Type-3 filters shown in Table 2.5, it can be noted that g_m has no effect on the pole frequency but will affect the DC gain and quality factor. The component g_m can be controlled using the biasing current source or to a less extent by the W/L ratio of the transistor. For the bandpass filter #2, raising g_m will improve Q but will lower center frequency gain K . For the notch filter #4, the design equations show that increase in g_m will lower both Q and DC gain K . These aspects have

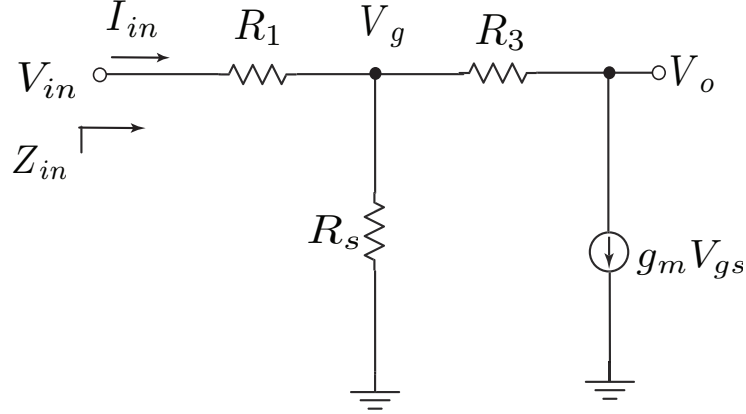


Figure 2.14: Allpass filter equivalent small signal diagram to find input impedance Z_{in} at very high frequencies

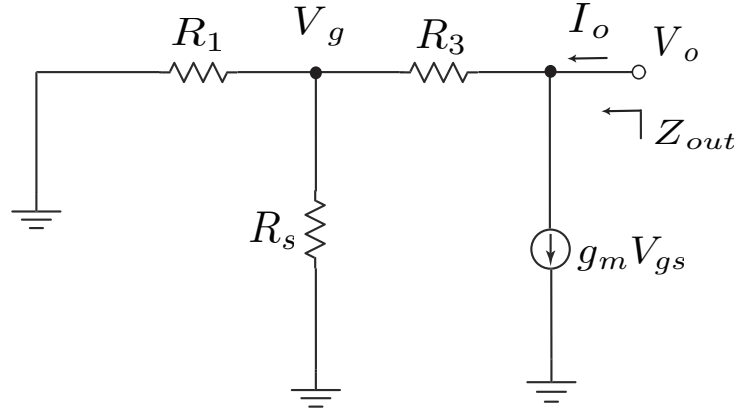


Figure 2.15: Allpass filter equivalent small signal diagram to find output impedance Z_{out} at high frequencies

to be carefully considered while carrying out simulations or experimental measurements and component values need to be chosen accordingly to obtain results that are close to the theoretical ones.

2.4.5 Biasing Details

For accurate implementation of single MOS transistor filters, care should be taken to maintain the transistors at saturation mode of operation, for which the conditions $V_{gs} > V_{th}$ and $V_{ds} > V_{gs} - V_{th}$ have to be met. Some impedance combinations can lead to the MOS transistor going out of saturation mode. For example, the Type-3 allpass filter #1 shown in Table 2.5 uses a series LC network for Z_2 that puts the transistor at improper operation mode as

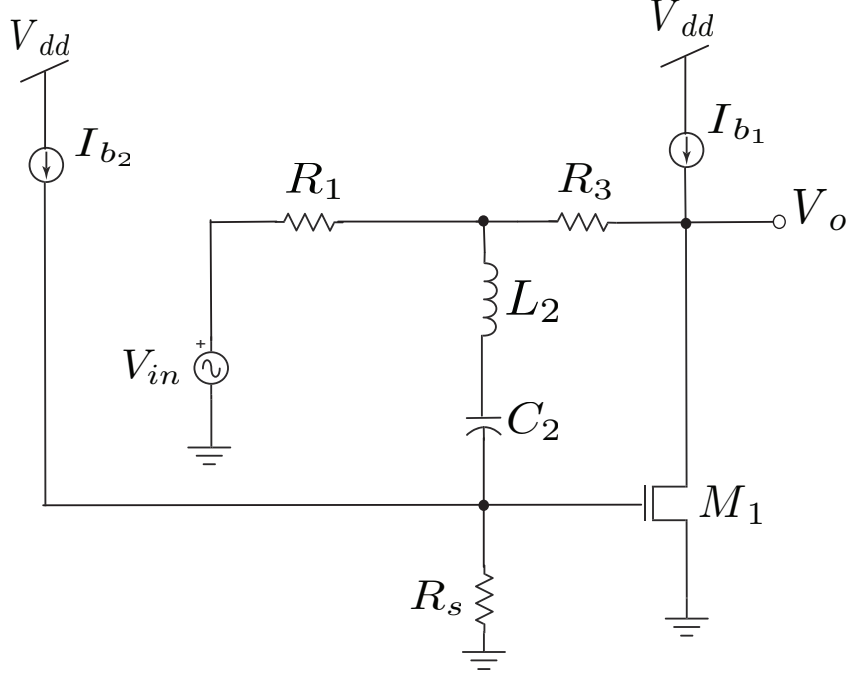


Figure 2.16: Allpass filter #1 from Table 2.5 implemented with an additional DC biasing current source

the capacitor blocks DC voltage to the gate terminal of the transistor. Similarly, the Type-1 gain equalizer filter #1 given in Table 2.2 also puts the transistor out of saturation mode due to the use of series LC network as Z_2 . However, these circuits can be made to operate by use of extra biasing. For example, Figure 2.16 shows the Type-3 allpass filter #1 from Table 2.5 with an extra DC current source I_{b2} connected to the gate terminal of the MOS transistor. To check the validity of the circuit it was simulated in Cadence Spectre using a single transistor with aspect ratio $W/L = 6\mu m/0.2\mu m$ and operated from a supply of 1.5 V in IBM 0.13 μm CMOS process. The allpass filter was designed to operate at $f_o = 4.6$ MHz with component values set to $L_2 = 24 \mu H$, $C_2 = 50$ pF, $R_1 = 50 \Omega$, $R_3 = 930 \Omega$ and $R_s = 500 \Omega$. The simulated magnitude and phase responses are shown in Figure 2.17. It is observed that the simulated DC gain is -0.69 dB which is close to the theoretical -0.1 dB gain. The transient waveforms of the input and output signals at pole frequency 4.6 MHz is shown in Figure 2.18.

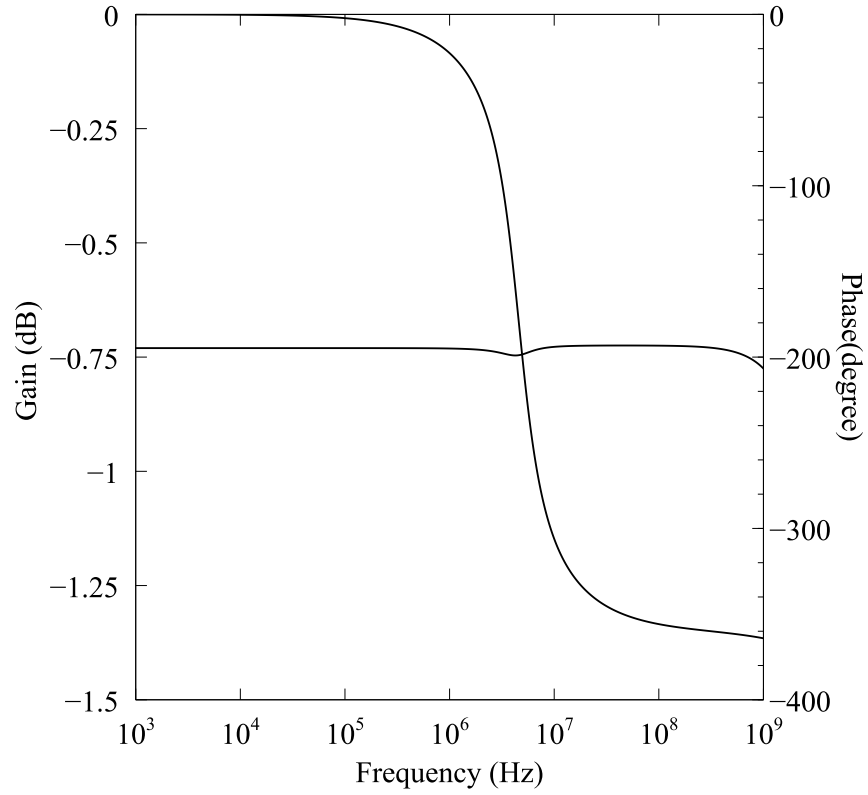


Figure 2.17: Simulated magnitude and phase responses of allpass filter of Figure 2.16

2.4.6 Non-ideal Effects

2.4.6.1 Effect of r_o

So far the MOS transistor was assumed to be ideal, by neglecting the drain to source resistance r_o and intrinsic parasitic capacitances of the transistor. In this section, the non-idealities of the proposed general circuit are discussed. To analyze the effects of r_o , the transistor can be modeled by an alternate transmission matrix given by

$$[T] = \begin{bmatrix} -\frac{1}{g_m r_o} & -\frac{1}{g_m} \\ 0 & 0 \end{bmatrix} \quad (2.32)$$

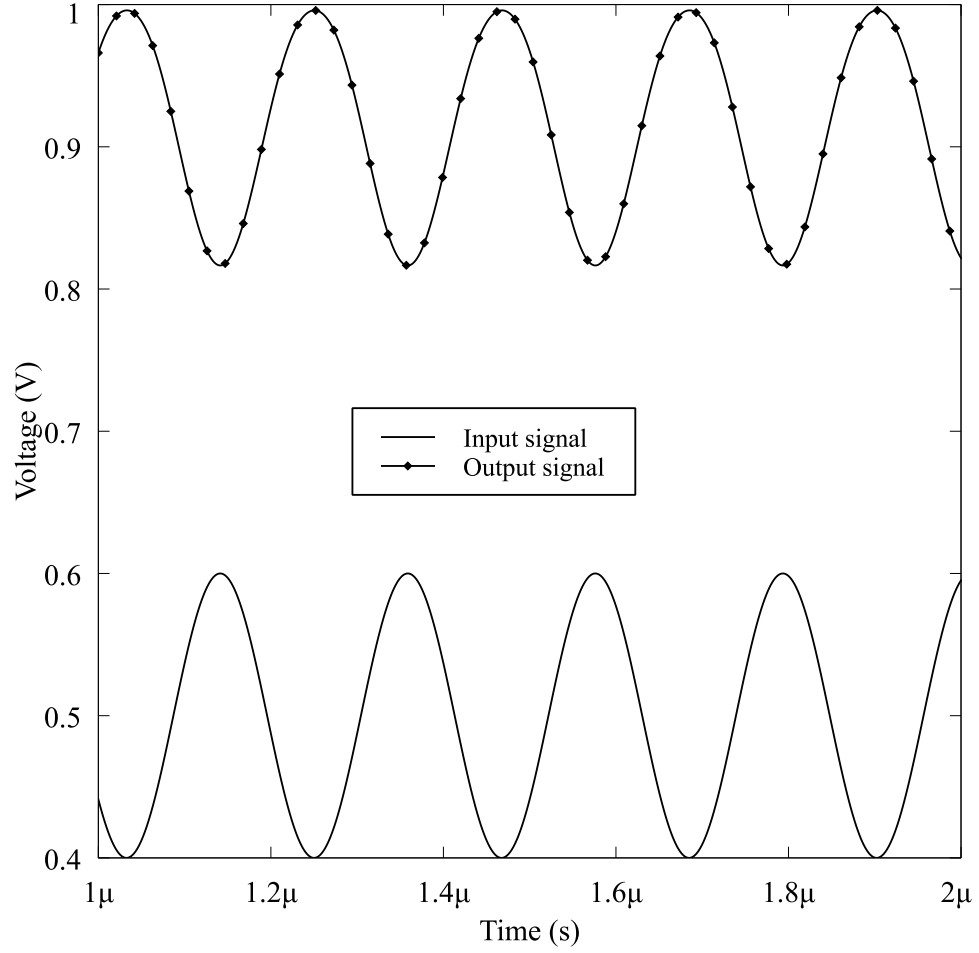


Figure 2.18: Simulated input and output waveforms of allpass filter of Figure 2.16 at pole frequency of 4.6 MHz

Bandpass filter (Table 2.5, #2)

The matrix given by equation (2.32) changes the transfer function of the bandpass filter and yields new expressions for Q and K . The pole frequency expression and order of the bandpass filter remains same. That is,

$$Q = \sqrt{\frac{L_1}{C_1}} \frac{r_o(R_s g_m + 1) + R_2 + R_3 + R_s}{r_o(R_2 + R_s) + R_3(R_2 + R_s)} \quad (2.33)$$

and

$$K = \frac{r_o(R_2 + R_s - R_3 R_s g_m)}{r_o(R_2 + R_s) + R_3(R_2 + R_s)} \quad (2.34)$$

The input and output impedance of the circuit due to r_o can also be considered. The input impedance at pole frequency becomes $Z_{in} = \frac{(R_2 + R_s)r_o + R_2 R_3 + R_3 R_s}{(R_s g_m + 1)r_o + R_2 + R_3 + R_s}$, while at very high and low frequencies the circuit sees sL_1 and $1/sC_1$ respectively, as can be observed from the circuit diagram in Figure 2.5. As expected, the effective output impedance seen looking into the drain terminal of the transistor is $Z_{out} = r_o \parallel R_3$ at the pole frequency, whereas, at low and high frequencies $Z_{out} = \frac{r_o(R_2 + R_3 + R_s)}{r_o(R_s g_m + 1) + R_2 + R_3 + R_s}$, when Z_1 is replaced by an open circuit.

Bandstop filter (Table 2.5, #4)

For the bandstop circuit, r_o alters the transfer function and hence the Q and K expressions become

$$Q = \sqrt{\frac{C_1}{L_1}} \frac{r_o(R_2 + R_s) + R_3(R_2 + R_s)}{r_o(R_s g_m + 1) + R_2 + R_3 + R_s} \quad (2.35)$$

$$K = \frac{r_o(R_2 + R_s - R_3 R_s g_m)}{r_o(R_2 + R_s) + R_3(R_2 + R_s)} \quad (2.36)$$

Input and output impedance of the bandstop filter considering the affect of r_o is found to be $Z_{in} = \frac{(R_2 + R_s)r_o + R_2 R_3 + R_3 R_s}{(R_s g_m + 1)r_o + R_2 + R_3 + R_s}$ and $Z_{out} = r_o \parallel R_3$ at low and high frequencies where Z_1 acts as a short circuit. At resonance frequency, $Z_{out} = \frac{r_o(R_2 + R_3 + R_s)}{r_o(R_s g_m + 1) + R_2 + R_3 + R_s}$, where Z_1 is an open circuit. As expected, r_o has no effect on the pole location and the filter order remains same. In the next section, however, it is shown that parasitic capacitances change the order of the filter by adding extra poles and zeroes.

2.4.6.2 Effect of parasitic capacitances

At very high frequencies the effects of parasitics are prominent which affects the expected performance of a filter. To consider the effects of high frequency parasitic capacitances, more complex transistor models are used.

First, to analyze the effect of C_{gs} , the transistor model given by

$$[T] = \begin{bmatrix} -\frac{1}{r_o g_m} & -\frac{1}{g_m} \\ -\frac{s C_{gs}}{r_o g_m} & -\frac{s C_{gs}}{g_m} \end{bmatrix} \quad (2.37)$$

is used to derive the transfer function and the pole and zero locations. C_{gs} is connected between the gate and source terminal of the transistor and hence shorts the gate to source path at very high frequencies. Another effect of C_{gs} is that it adds an extra real pole and zero which converts the second order bandpass filter to a third order filter. The additional pole and zero due to C_{gs} is given by

$$\omega_{z_1} = \frac{R_s R_3 g_m - R_2 - R_s}{C_{gs} R_2 R_s} \quad (2.38)$$

$$\omega_{p_1} = \sqrt{\frac{r_o (R_s g_m + 1) + R_2 + R_3 + R_s}{C_{gs} R_s (R_2 + R_3 + r_o)}} \quad (2.39)$$

A similar effect is observed for the bandstop filter where the extra pole and zero due to C_{gs} is found to be

$$\omega_{z_1} = \frac{R_s R_3 g_m - R_2 - R_s}{C_{gs} R_2 R_s} \quad (2.40)$$

$$\omega_{p_1} = \sqrt{\frac{R_2 + R_s}{C_{gs} R_2 R_s}} \quad (2.41)$$

Next we consider the effect of the parasitic capacitor C_{gd} on the bandpass circuit. It is connected across the gate and drain terminals of the transistor and will get shorted at very

high frequencies, reducing the output impedance of the bandpass filter to R_s . It also adds another pole and zero to the bandpass transfer function which are given by

$$\omega_{z_2} = \frac{R_s R_3 g_m - R_2 - R_s}{C_{gd} R_s (R_2 + R_3)} \quad (2.42)$$

$$\omega_{p_2} = \sqrt{\frac{r_o (R_s g_m + 1) + R_2 + R_3 + R_s}{C_{gd} (R_2 + R_3) (R_s g_m r_o + r_o + R_s)}} \quad (2.43)$$

In the case of bandstop filter the additional pole and zero due to C_{gd} are

$$\omega_{z_2} = \frac{R_s R_3 g_m - R_2 - R_s}{C_{gd} R_s (R_2 + R_3)} \quad (2.44)$$

$$\omega_{p_2} = \sqrt{\frac{(R_2 + R_s) (R_3 + r_o)}{C_{gd} (R_2 R_3 R_s (g_m r_o + 1) + r_o (R_2 R_3 + R_2 R_s + R_3 R_s))}} \quad (2.45)$$

It is observed that both C_{gs} and C_{gd} add an extra real pole and zero converting the filter from second to fourth order. This can be shown by using a more complex transmission matrix (2.46) that yields a transfer function of the fourth order.

$$[T] = \begin{bmatrix} \frac{sC_{gd} + 1/r_o}{sC_{gd} - g_m} & \frac{1}{sC_{gd} - g_m} \\ \frac{s(sC_{gd}C_{gs}r_o + C_{gd}g_m r_o + C_{gd} + C_{gs})}{r_o(sC_{gd} - g_m)} & \frac{s(C_{gd} + C_{gs})}{sC_{gd} - g_m} \end{bmatrix} \quad (2.46)$$

Hence, the filters do not work as expected beyond a certain frequency due to the high frequency effects of the transistors. The frequencies at which these additional poles/ zeroes occur can be found from the derived frequency expressions.

CHAPTER 3

Simulation and Experimental Results

To validate the theoretical study, simulation and experimental results of selected filters are presented. The circuits were simulated in an IBM 0.13 μm CMOS process using the Spectre simulation tool in Cadence design environment. Note that for Cadence simulations, the filters were designed to operate at high frequencies (in the tens of MHz) as we intended to implement one of the proposed filters in IC form. However, it was not possible to present an IC chip in this work due to time constraints. The filters were verified experimentally using standard discrete components connected on a breadboard and the measured responses were observed from Network Analyzer HP4395A. For experimental testing the operating frequency of the filters was lowered to the kHz range.

3.1 Bandpass Filter

The bandpass filter shown in Figure 2.5 was simulated using a single transistor with an aspect ratio of $W/L = 0.48 \mu\text{m}/0.18 \mu\text{m}$ and operated from a supply of 1.5 V. The component values were found using the equations of Q , ω_o , and K to be $L_1 = 50 \mu\text{H}$, $C_1 = 1.9 \text{ pF}$, $R_2 = 1.2 \text{ k}\Omega$, $R_3 = 100 \Omega$ and $R_s = 900 \Omega$. A bias current source of $400 \mu\text{A}$ yielded a center frequency gain of -0.042 dB at 16.3 MHz for a Q of 2.5. The simulated results are shown in Figure 3.1, which is similar to the calculated gain of -0.08 dB at center frequency of 16.3 MHz. Transient analysis of the bandpass filter was carried out at the center frequency of 16.3 MHz. The input signal and its corresponding output are shown in Figure 3.2, which shows that the waveforms have equal amplitude at the pole frequency. This is expected because

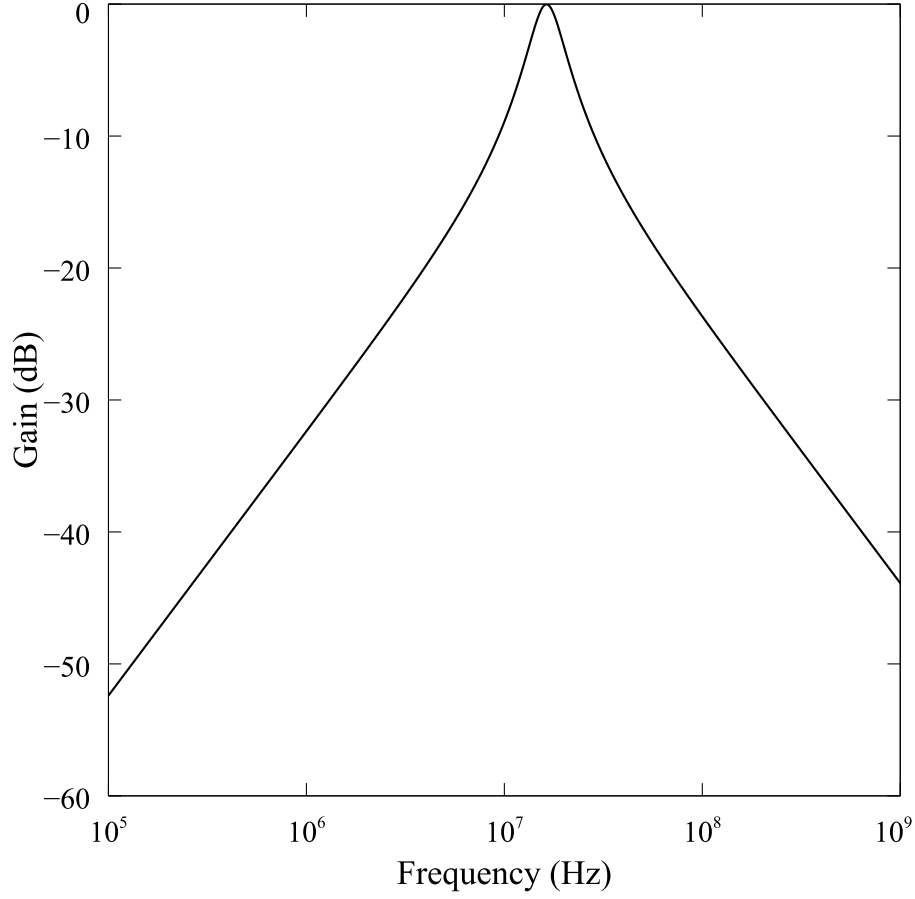


Figure 3.1: Magnitude response of proposed bandpass filter simulated in Cadence to values of $L_1 = 50 \mu\text{H}$, $C_1 = 1.9 \text{ pF}$, $R_2 = 1.2 \text{ k}\Omega$, $R_3 = 100 \Omega$, and $R_s = 900 \Omega$.

the simulated magnitude response in Figure 3.1 shows that the center frequency gain is around 0 dB, that is, input and output signals have the same amplitude.

The bandpass filter was also tested experimentally using discrete components and CD4007 transistor arrays that operated from a 5 V supply. Component values used were $C_1 = 680 \text{ pF}$, $L_1 = 10 \text{ mH}$, $R_s = 900 \Omega$, $R_2 = 1.2 \text{ k}\Omega$ and $R_3 = 100 \Omega$ that resulted in a calculated pole frequency of 61 kHz with a gain of -0.91 dB and $Q = 7$. The measured response shown in Figure 3.3 had a pole frequency of 63.4 kHz where the gain is -1.286 dB and $Q = 7.86$. To verify the experimental results, we tested the bandpass filter in PSPICE using CD4007 transistor model that operated from a 5 V supply. Component values of resistors, capacitor and inductor were kept same as the experimental setup which resulted in a pole frequency

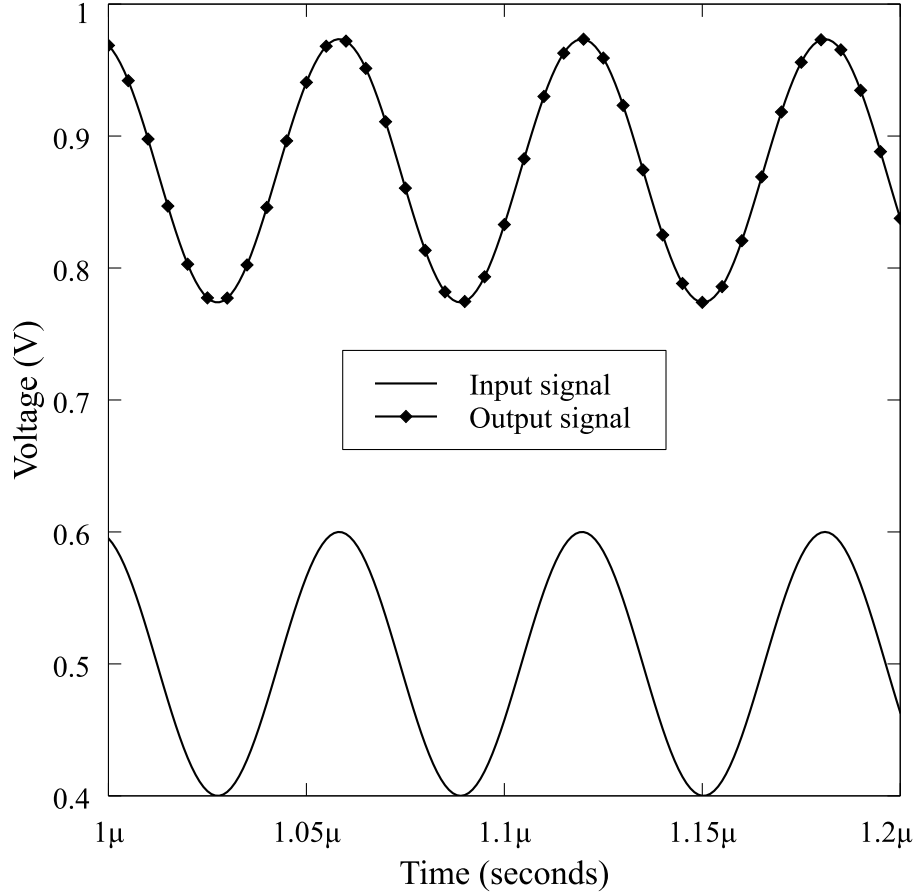


Figure 3.2: Cadence simulated transient responses of input and output signals of bandpass filter at pole frequency of 16.3 MHz to values $L_1 = 50 \mu\text{H}$, $C_1 = 1.9 \text{ pF}$, $R_2 = 1.2 \text{ k}\Omega$, $R_3 = 100 \Omega$ and $R_s = 900 \Omega$.

of 61.19 kHz with a gain of -1.30 dB and $Q = 8.2$. The simulated results from PSPICE are shown in Figure 3.4. It is observed that the values of the design parameters (gain, quality factor and pole frequency) obtained from experimental measurements are very close to those of the PSPICE simulations and the minor differences are due to the tolerances of the discrete components used. Note that the center frequency gain K of the bandpass filter can be made to move closer to unity gain (0 dB) but at the expense of quality factor Q . This is because of some common terms that appear in both K and Q expressions (Table 2.5). For example, raising the value of R_2 will improve K but lower Q .

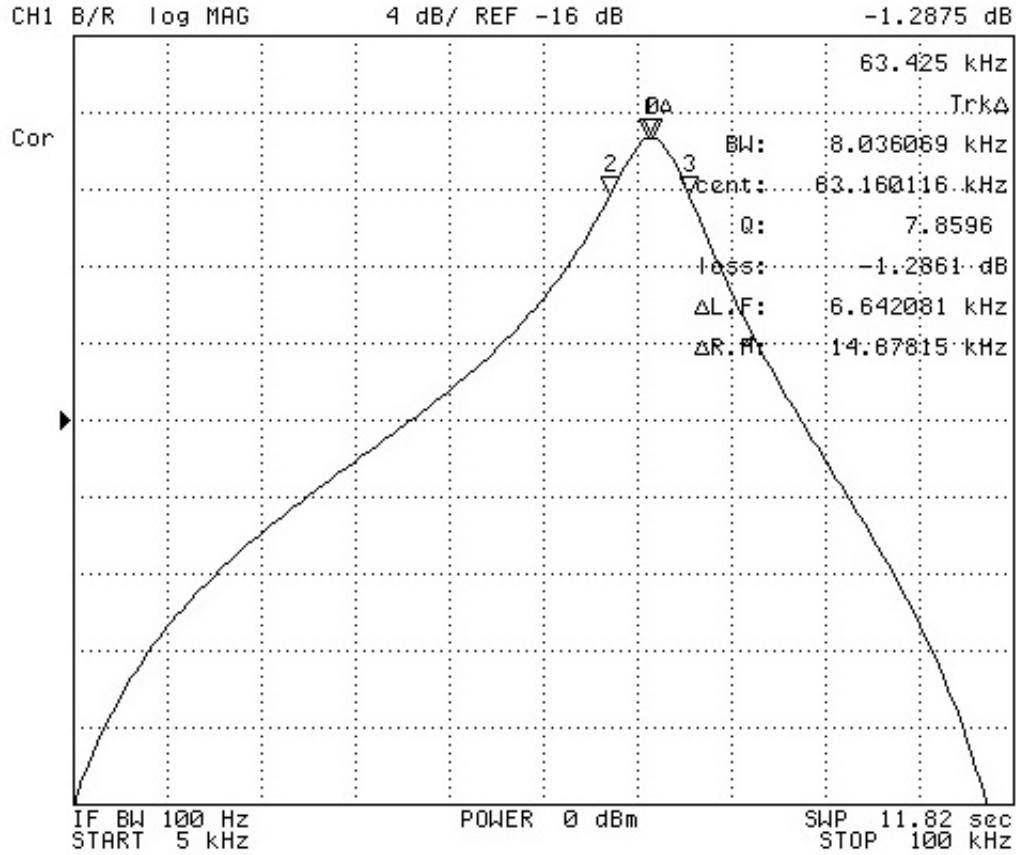


Figure 3.3: Measured magnitude response of bandpass filter to values of $C_1 = 680$ pF, $L_1 = 10$ mH, $R_s = 900 \Omega$, $R_2 = 1.2$ k Ω and $R_3 = 100 \Omega$.

3.2 Bandstop Filter

The bandstop circuit shown in Figure 2.9 was simulated in Cadence. It employed a single transistor with an aspect ratio of $W/L = 0.48 \mu m / 0.18 \mu m$ and operated from a supply of 1.5 V. The parallel LC network used component values $L_1 = 10 \mu H$, $C_1 = 9.52$ pF. The values of the resistors used were $R_2 = 600 \Omega$, $R_3 = 110 \Omega$, and $R_s = 1.2$ k Ω . A bias current source of 700 μA and $g_m = 73.8 \mu A/V$ yielded a simulated DC gain of -0.05 dB and a notch frequency of 16.2 MHz which is in good agreement to the calculated notch frequency of 16.3 MHz and DC gain of -0.06 dB. The notch depth at the center frequency 16.2 MHz was observed to be -34.69 dB. Figure 3.5 shows the simulated magnitude response for the circuit. The transient waveforms of the input and output signals at pole frequency 16.2 MHz are given in Figure

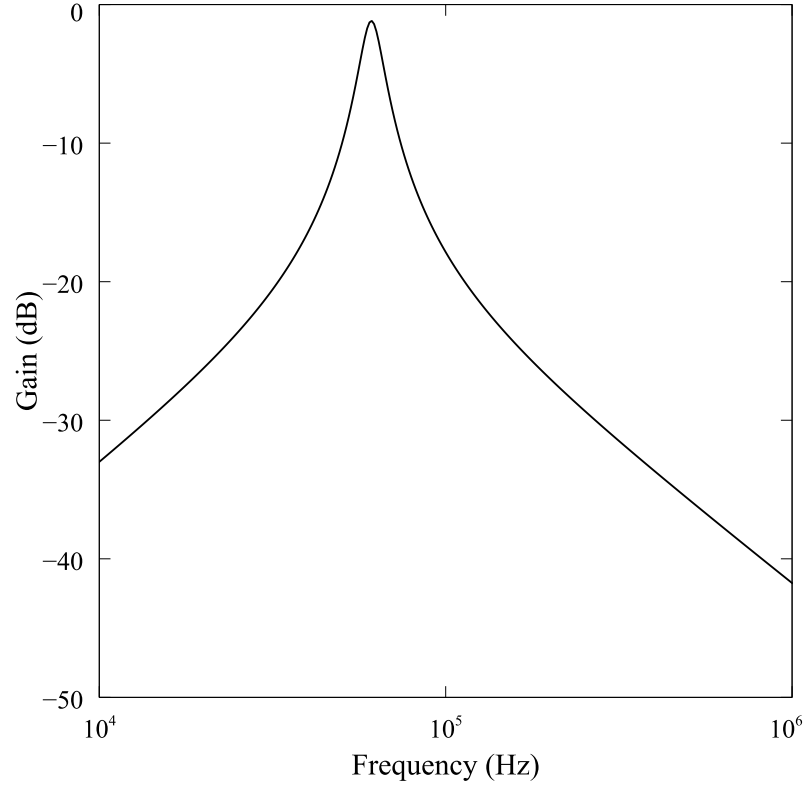


Figure 3.4: Magnitude response of bandpass filter simulated in PSPICE to values of $C_1 = 680 \text{ pF}$, $L_1 = 10 \text{ mH}$, $R_s = 900 \Omega$, $R_2 = 1.2 \text{ k}\Omega$ and $R_3 = 100 \Omega$.

3.6. It is observed that at the notch frequency the output signal is much smaller compared to the input signal. This is because the notch frequency magnitude of the bandstop filter was found to be -34.68 dB as shown in Figure 3.5.

To validate the bandstop filter, it was also tested experimentally using discrete components and CD4007 transistor arrays. The circuit operated from a 5 V supply with component values set to $C_1 = 68 \text{ pF}$, $L_1 = 2 \text{ mH}$, $R_s = 1.2 \text{ k}\Omega$, $R_2 = 500 \Omega$ and $R_3 = 100 \Omega$ that yielded a calculated pole frequency of 432 kHz with a DC gain of -0.1 dB. The measured magnitude response shown in Figure 3.7 has a notch at measured pole frequency of 425 kHz with a notch depth of -36.4 dB, while the DC gain is 0 dB. To check the accuracy of the measured results, the bandstop filter was simulated in PSPICE using CD4007 transistor and passive components that operated from a 5 V supply. Component values of resistors, capacitor and inductor were kept same as the experimental setup. The simulated results are

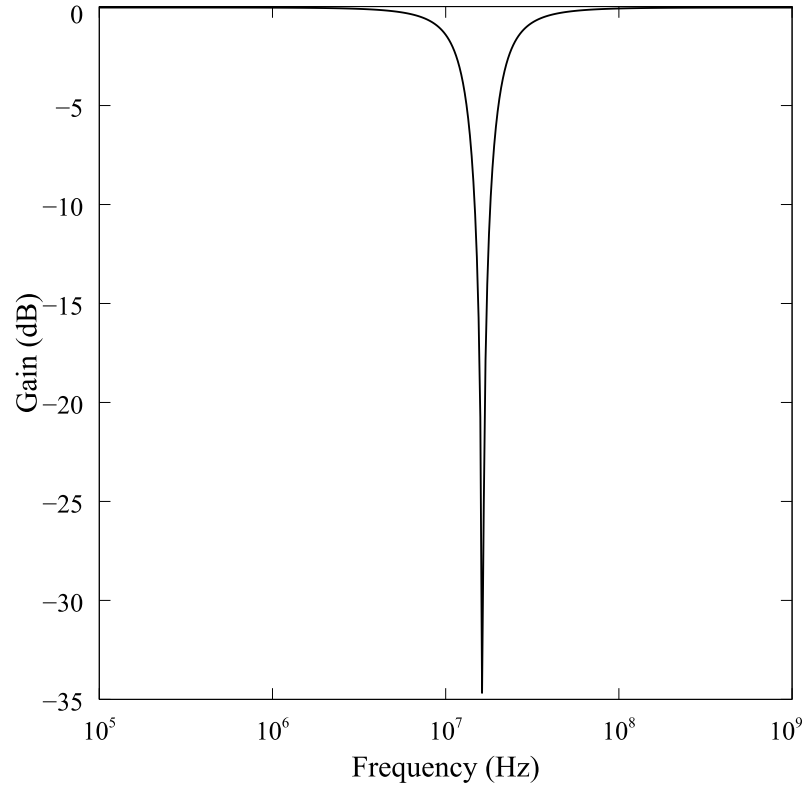


Figure 3.5: Bandstop filter magnitude response simulated in Cadence to values of $L_1 = 10 \mu\text{H}$, $C_1 = 9.52 \text{ pF}$, $R_2 = 600 \Omega$, $R_3 = 110 \Omega$, and $R_s = 1.2 \text{ k}\Omega$.

shown in Figure 3.8. It can be observed that the simulation results are in good agreement with the experimental ones. The DC gain is around 0 dB for both cases and the measured notch frequency of 425 kHz is close to the simulated value of 430 kHz. The measured quality factor $Q = 5.3$ is close to simulated $Q = 5.9$. The slight discrepancies are attributed to the tolerances and quality factors of the real components.

3.3 Allpass Filter

The allpass circuit shown in Figure 2.12 was simulated in Cadence. The filter was designed to operate at 4.6 MHz with $L_2 = 24 \mu\text{H}$, $C_2 = 50 \text{ pF}$, $R_1 = 50 \Omega$, $R_3 = 930 \Omega$ and $R_s = 500 \Omega$ from a 1.5 V supply voltage. A bias current source of $600 \mu\text{A}$ yielded a DC gain of -0.7 dB, quite close to the theoretical DC gain of -0.1 dB at a calculated pole frequency of 4.6 MHz. Figure 3.9 shows the simulated magnitude and phase responses while Figure 3.10

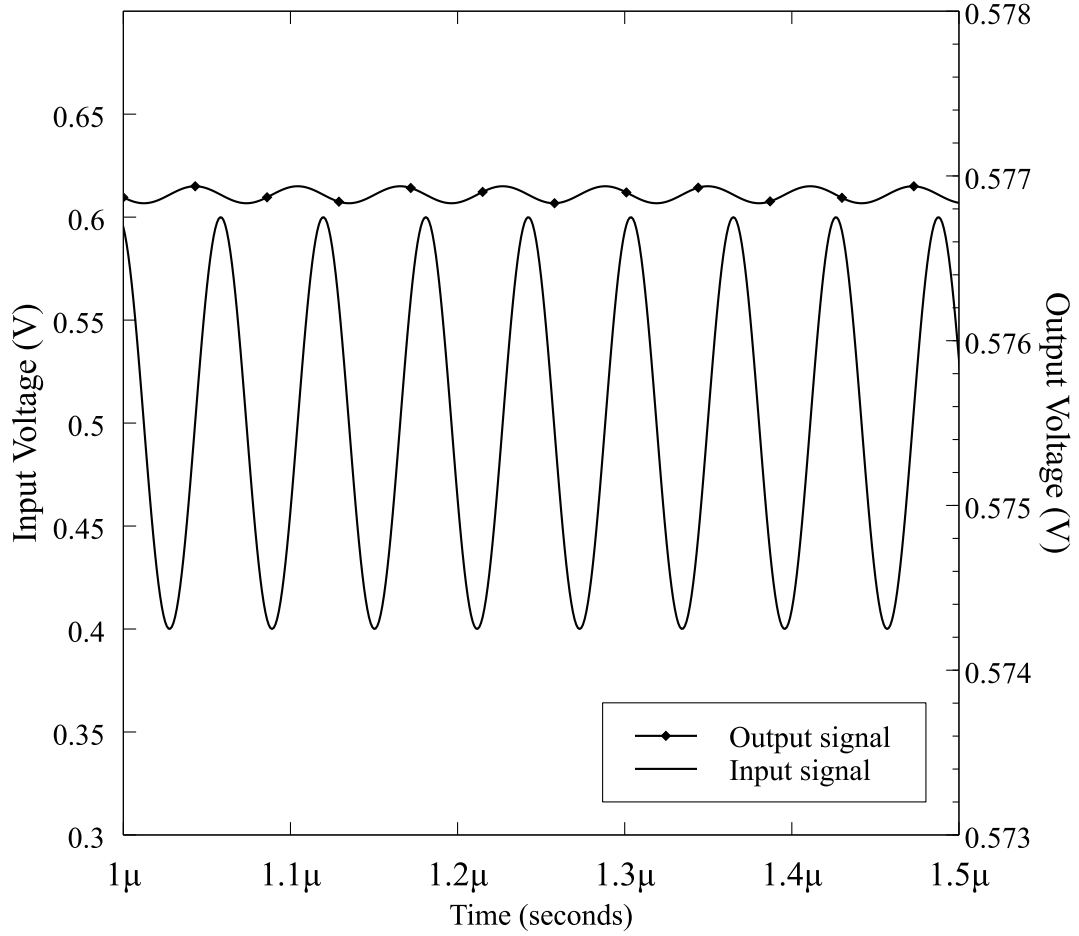


Figure 3.6: Cadence simulated input and output waveforms of bandstop filter at the pole frequency of 16.2 MHz to values $L_1 = 10 \mu\text{H}$, $C_1 = 9.52 \text{ pF}$, $R_2 = 600 \Omega$, $R_3 = 110 \Omega$, and $R_s = 1.2 \text{ k}\Omega$.

shows the transient waveforms at 4.6 MHz.

The allpass filter was also tested experimentally. The circuit operated from a 5 V supply with component values set to $C_1 = 68 \text{ pF}$, $L_1 = 2 \text{ mH}$, $R_1 = 1 \text{ k}\Omega$, $R_3 = 1.2 \text{ k}\Omega$ and $R_s = 3.3 \text{ k}\Omega$, designed to operate at 400 kHz. The measured magnitude and phase responses are shown in Figure 3.11. To verify the measured results, the allpass filter was simulated in PSPICE using CD4007 transistor and passive components of same values that operated from a 5 V supply. The simulated results are shown in Figure 3.12. It can be observed that the simulation results are close to the experimental ones.

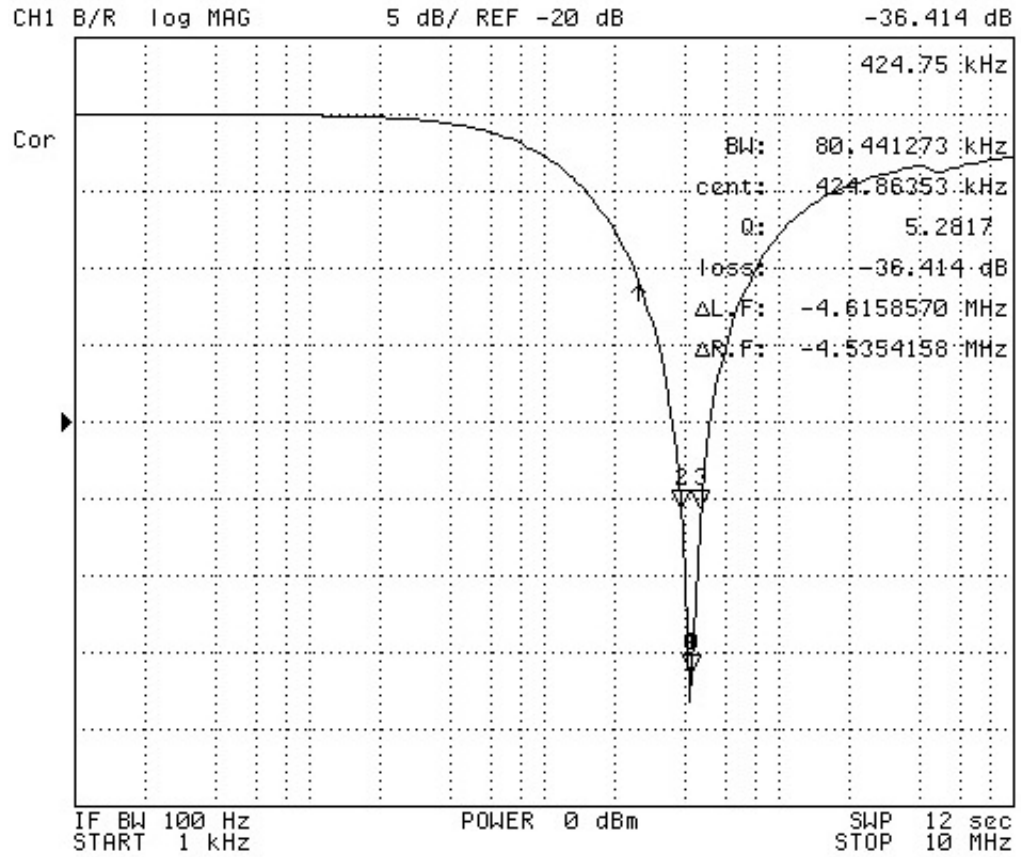


Figure 3.7: Measured magnitude response of bandstop filter to values of $C_1 = 68$ pF, $L_1 = 2$ mH, $R_s = 1.2$ k Ω , $R_2 = 500$ Ω and $R_3 = 100$ Ω with a vertical scale of 5 dB/division and a logarithmic horizontal scale where each cycle represents a factor of 10.

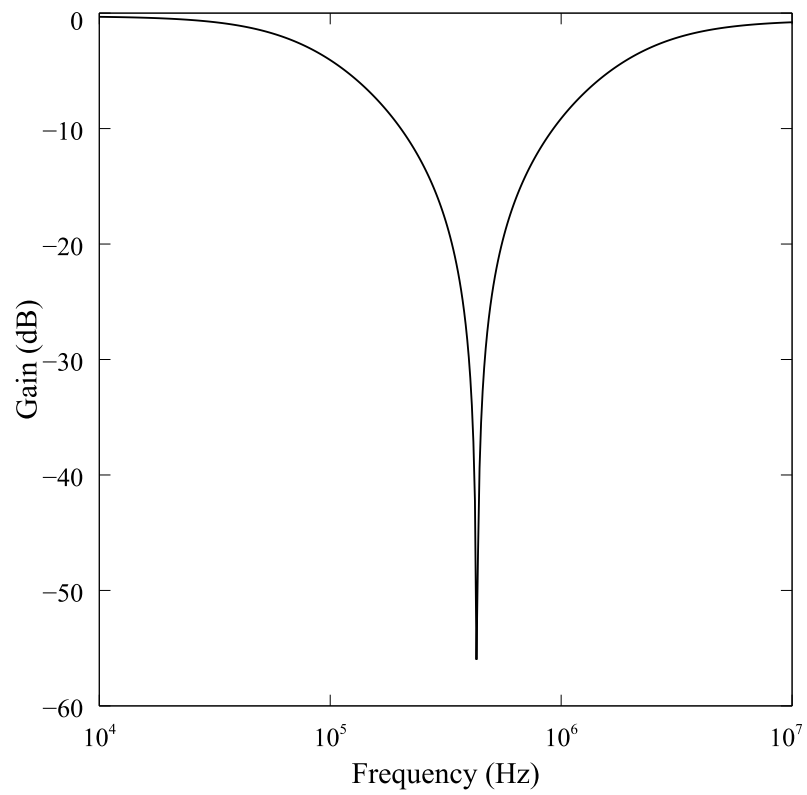


Figure 3.8: Magnitude response of bandstop filter simulated in PSPICE to values of $C_1 = 68$ pF, $L_1 = 2$ mH, $R_s = 1.2$ k Ω , $R_2 = 500$ Ω and $R_3 = 100$ Ω .

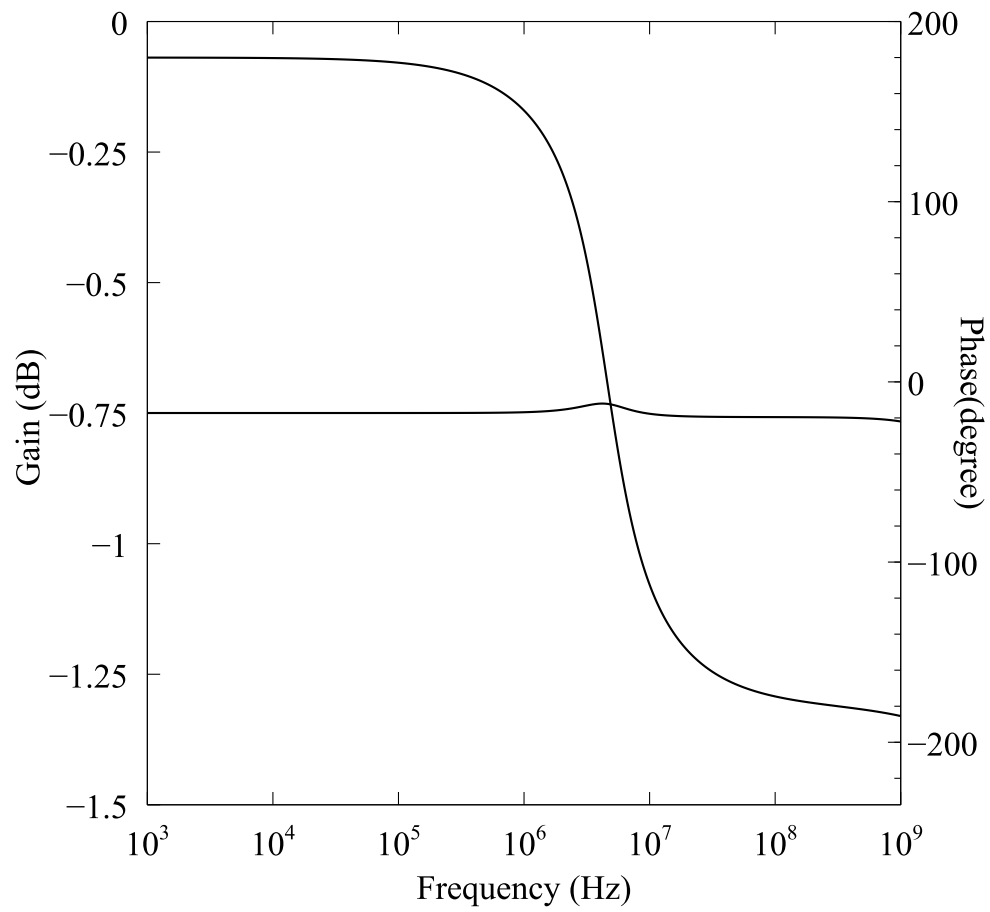


Figure 3.9: Allpass filter magnitude and phase response simulated in Cadence to values $L_2= 24 \mu\text{H}$, $C_2= 50 \text{ pF}$, $R_1= 50 \Omega$, $R_3=930 \Omega$ and $R_s= 500 \Omega$.

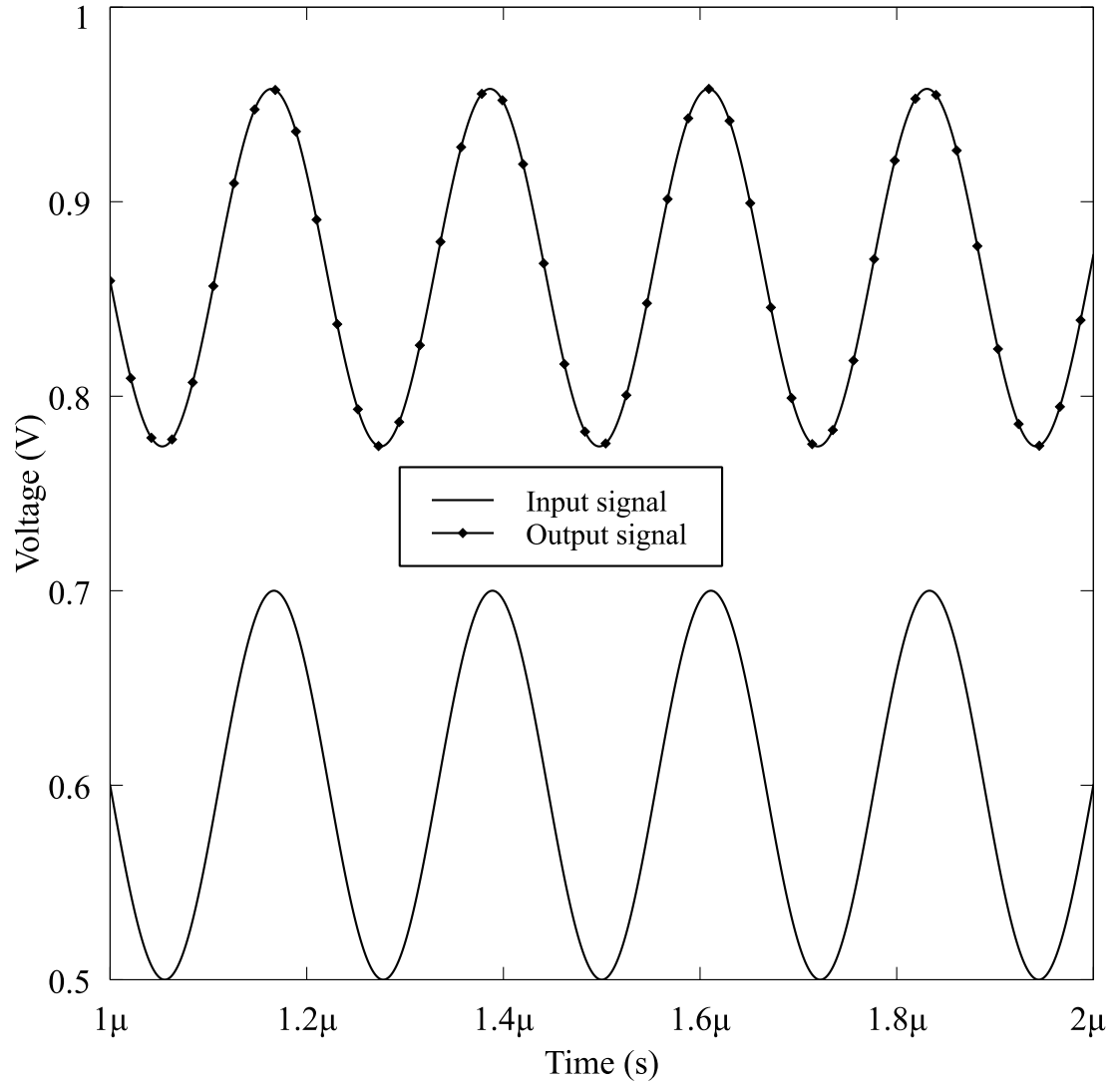


Figure 3.10: Cadence simulated input and output waveforms of allpass filter at pole frequency to values $L_2= 24\ \mu\text{H}$, $C_2= 50\ \text{pF}$, $R_1= 50\ \Omega$, $R_3=930\ \Omega$ and $R_s= 500\ \Omega$.

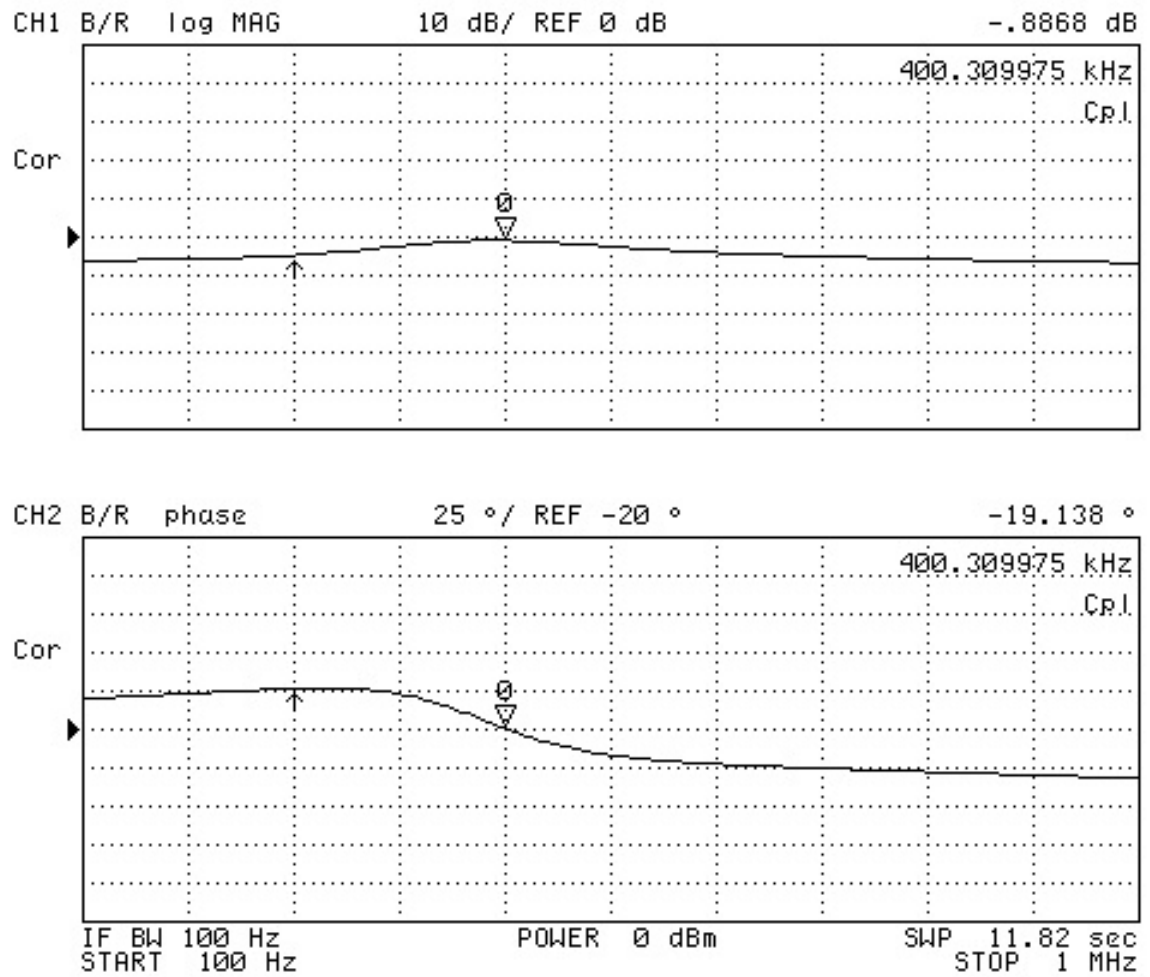


Figure 3.11: Measured magnitude and phase response of allpass filter to values $C_1 = 68$ pF, $L_1 = 2$ mH, $R_1 = 1$ k Ω , $R_3 = 1.2$ k Ω and $R_s = 3.3$ k Ω .

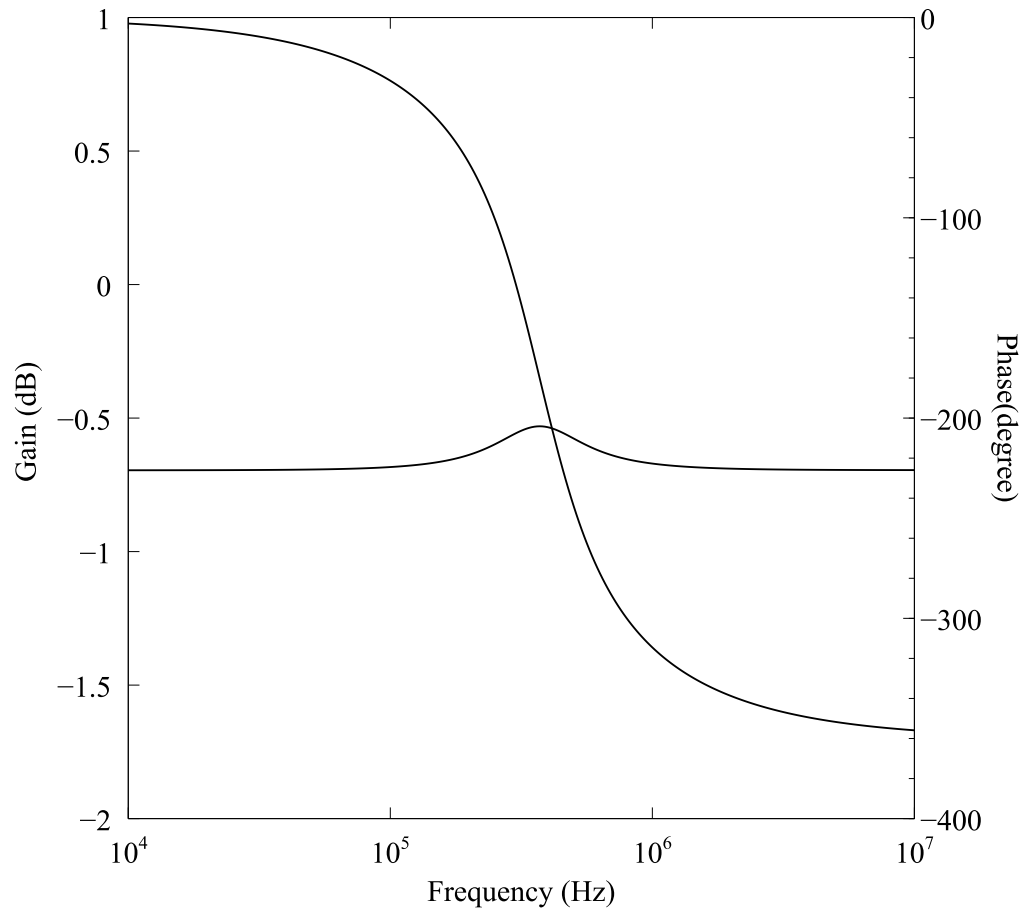


Figure 3.12: Magnitude response of allpass filter simulated in PSPICE to values of $C_1 = 68$ pF, $L_1 = 2$ mH, $R_1 = 1$ k Ω , $R_3 = 1.2$ k Ω and $R_s = 3.3$ k Ω .

CHAPTER 4

A Fourth Order Chebyshev Filter

4.1 Classical Chebyshev Filter Design Approach

It is known that ideal analog brick wall filters are not practically realizable. Different methods of approximations are used to design a filter that will satisfy certain desirable conditions. Several filter approximations have been proposed in the past, such as Butterworth, Chebyshev, Inverse Chebyshev, Elliptic and Bessel-Thompson, each having a different output response. The choice of the approximation method to be used depends on the filter specifications. The Butterworth, also referred to as a maximally flat magnitude filter has a flat response in the passband and an adequate roll-off. The Chebyshev implementation has a steeper roll-off but has ripples in the passband. It is sometimes known as the Type I Chebyshev filter. Inverse Chebyshev or Type II Chebyshev filters have ripples in the stopband.

In classical filter methods, design of Chebyshev and other filter approximations is based on equations and tables of theoretical values. For a given set of specifications, a lowpass Chebyshev filter is normalized at a passband edge frequency of $\omega_c = 1$ rad/s and the order of the filter is found from a given formula. Next, a set of formula or tabulated values are used to find the poles and zeroes. Other types of filters such as bandpass, bandstop, highpass filters can be obtained by use of frequency transformations. For example, to design a highpass Chebyshev filter, a lowpass prototype (LPP) is obtained by means of highpass to lowpass frequency transformation. Then, the order, poles and zeroes and transfer function of the LPP is found. Next, denormalization of the LPP transfer function and application of

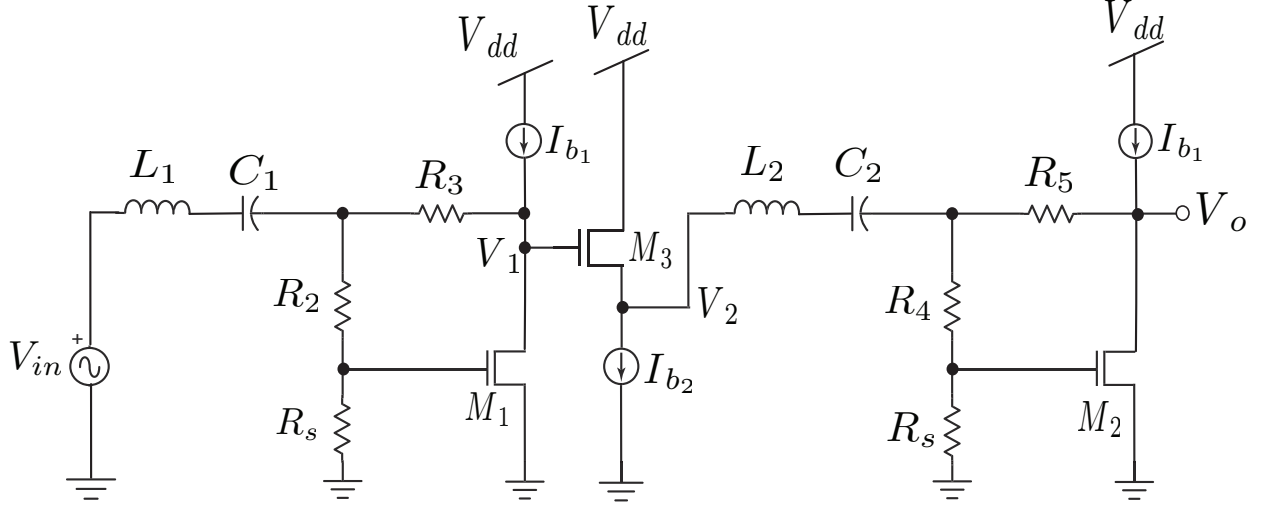


Figure 4.1: Proposed Chebyshev fourth order bandpass filter

the lowpass to highpass inverse transformation is performed to obtain the high pass transfer function that meets the given specifications. The final realization of the active filters can be implemented using multiple operational amplifiers, OTAs or CCIIs, especially for higher order filter structures where several passive and active elements are required. An application of a Chebyshev filter was found in [31]. It used a passive bandpass Chebyshev filter to achieve a wideband input match from 3.1 to 10 GHz for a low noise amplifier.

4.2 Proposed Fourth Order Chebyshev Filter

In this section, a fourth order active Chebyshev bandpass filter topology is introduced that is based on the single transistor bandpass filter. The core of the circuit is shown in Figure 4.1. It can be observed that the classical fourth order passive Chebyshev bandpass filter shown in Figure 4.2 is simpler compared to the proposed topology. However, classical active higher order filters use at least one opamp and some passive elements. For example, the third order active Chebyshev filter designed in [32] used two opamps and a couple of passive elements. The proposed topology implementing a fourth order Chebyshev filter using three transistors and several passive elements is shown in Figure 4.1.

The proposed circuit can be easily tuned as each stage controls only one pole which

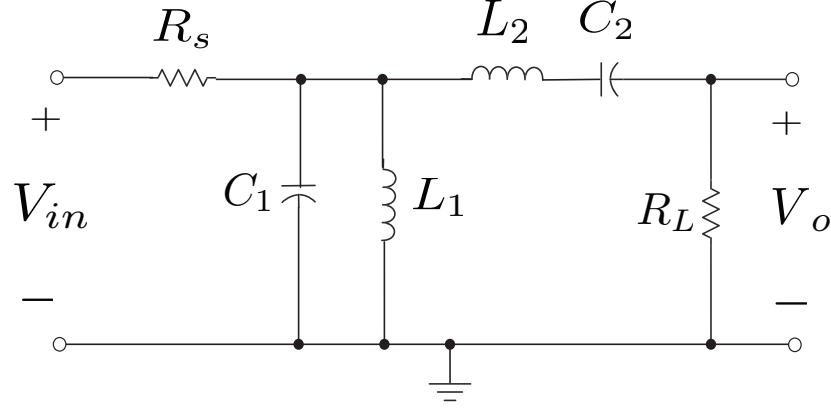


Figure 4.2: Passive fourth order bandpass filter

Design Parameters	Stage 1	Stage 2
Pole frequency	$\omega_{o1} = \sqrt{\frac{1}{C_1 L_1}}$	$\omega_{o2} = \sqrt{\frac{1}{C_2 L_2}}$
Quality factor	$Q_1 = \frac{(R_s g_{m1} + 1) \sqrt{\frac{L_1}{C_1}}}{R_2 + R_s}$	$Q_2 = \frac{(R_s g_{m2} + 1) \sqrt{\frac{L_2}{C_2}}}{R_4 + R_s}$
Gain	$K_1 = \frac{R_2 + R_s - R_3 R_s g_{m1}}{R_2 + R_s}$	$K_2 = \frac{R_4 + R_s - R_5 R_s g_{m2}}{R_4 + R_s}$

Table 4.1: Chebyshev filter design equations for two stages

depends solely on the series LC network of that stage. The design parameters of each stage of the Chebyshev filter is shown in Table 4.1. A Chebyshev filter with maximum passband loss (ripple magnitude) of 2 dB and minimum stopband loss of 20 dB with pole frequencies at 17 MHz and 29 MHz and a center frequency of 22.5 MHz at a Q of 3.6 was targeted. The general transfer function of the fourth order Chebyshev filter is given by

$$\frac{V_o}{V_{in}} = K_1 K_2 \frac{\left(\frac{\omega_{o1}}{Q}\right)s \times \left(\frac{\omega_{o2}}{Q}\right)s}{\left(s^2 + \frac{\omega_{o1}}{Q}s + \omega_{o1}^2\right) \left(s^2 + \frac{\omega_{o2}}{Q}s + \omega_{o2}^2\right)} \quad (4.1)$$

where K_1 , K_2 are the gains and ω_{o1} , ω_{o2} represent the pole frequencies of the first and second stages, respectively. In order to achieve a Type I Chebyshev filter response with ripples in the passband, the first and second stages were designed such that they have the same gain ($K_1 = K_2$) and quality factor Q but at different pole frequencies. The bandpass filter design equations were used to calculate component values for each stage for a Q of 3.6 and unity gain at two different pole frequencies, which is solely controlled by L and

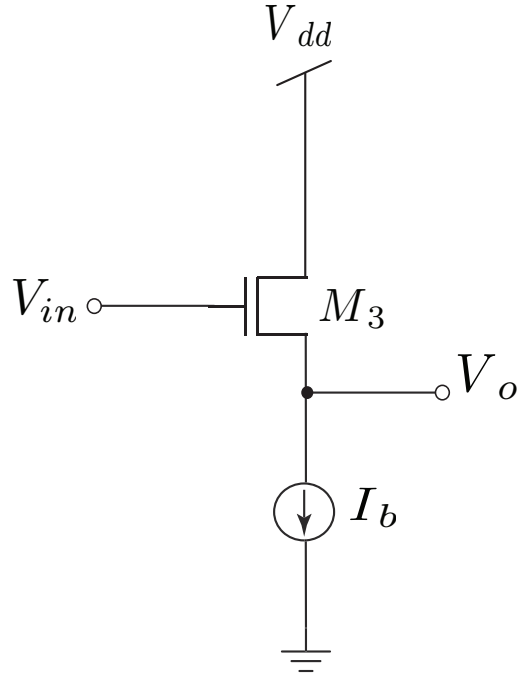


Figure 4.3: Source follower used as a voltage buffer

C. A unity gain voltage buffer was used between the two stages to prevent loading due to impedance mismatch. The buffer circuit was implemented using a source follower.

Figure 4.3 shows a source follower structure, which was realized using a CMOS transistor M_3 . This is also referred to as a common drain amplifier as the input and output signals are at the gate and source terminals, respectively while the drain terminal is at AC ground. A current source I_b is used as the active load at the source terminal to provide biasing to the MOS transistor. An alternative way of realizing the source follower is to use a current mirror as an active load [33]. The primary purpose of using a buffer between the two stages is to provide isolation between the two stages and prevent the second stage from loading the first stage of the circuit due to impedance differences between the output node of the first stage and input node of the second stage. Ideally, a source follower should have very high input impedance so that the input node draws minimum current from the source and does not load it. Also it must have very low output impedance so that it can drive the

load as if it were a perfect voltage source. Hence, in the ideal case the source follower has a voltage gain of 1. However, in practice it is usually less than unity, due to the body effect of M_3 .

4.3 Simulated Results

The proposed filter in Figure 4.1 was simulated in Cadence with the component values set to $L_1 = 50 \mu\text{H}$, $C_1 = 1.8 \text{ pF}$, $L_2 = 29 \mu\text{H}$, $C_2 = 1 \text{ pF}$, $R_2 = R_4 = 1.2 \text{ k}\Omega$, $R_3 = R_5 = 90 \Omega$ and $R_s = 900 \Omega$ that created poles at 17 MHz and 29 MHz where the gain was -14.1 dB and a center frequency of 23 MHz. Both the transistors had equal W/L ratios of $0.48\mu\text{m}/0.18\mu\text{m}$ and bias currents of $400 \mu\text{m}$ resulting in $g_{m1} = g_{m2} = 38.29\mu\text{A/V}$. To compare the theoretical and simulated responses, the transfer function of the Chebyshev filter given by equation (4.1) was plotted in MATLAB for a $Q_1 = Q_2 = 3.6$, $K_1 = K_2 = 0.99$, $f_{o1} = 17 \text{ MHz}$ and $f_{o2} = 29 \text{ MHz}$. The magnitude and phase responses are shown in Figure 4.4. It is observed from Figure 4.4 that the theoretical and simulated responses are very similar to each other. The theoretical Chebyshev response obtained by plotting the general transfer function in MATLAB had a gain of around -13 dB, while the simulated response from Cadence gave a gain of -14.1 dB. In the next section we attempted to improve the gain of the Chebyshev filter targeting unity gain using a two stage operational amplifier connected in cascade with the filter circuit.

4.4 Two stage operational amplifier

A two stage operational amplifier [33,34] is a commonly used analog building block, where the differential input stage and the common source amplifier form the two gain stages. A unity gain stage realized using a source follower form the output buffer that is used to provide low output impedance to drive the load connected to the opamp. A complete two stage opamp is shown in Figure 4.5. The differential amplifier is a popular input stage for opamps and is realized using n-channel CMOS transistors M_1 and M_2 with one input at the

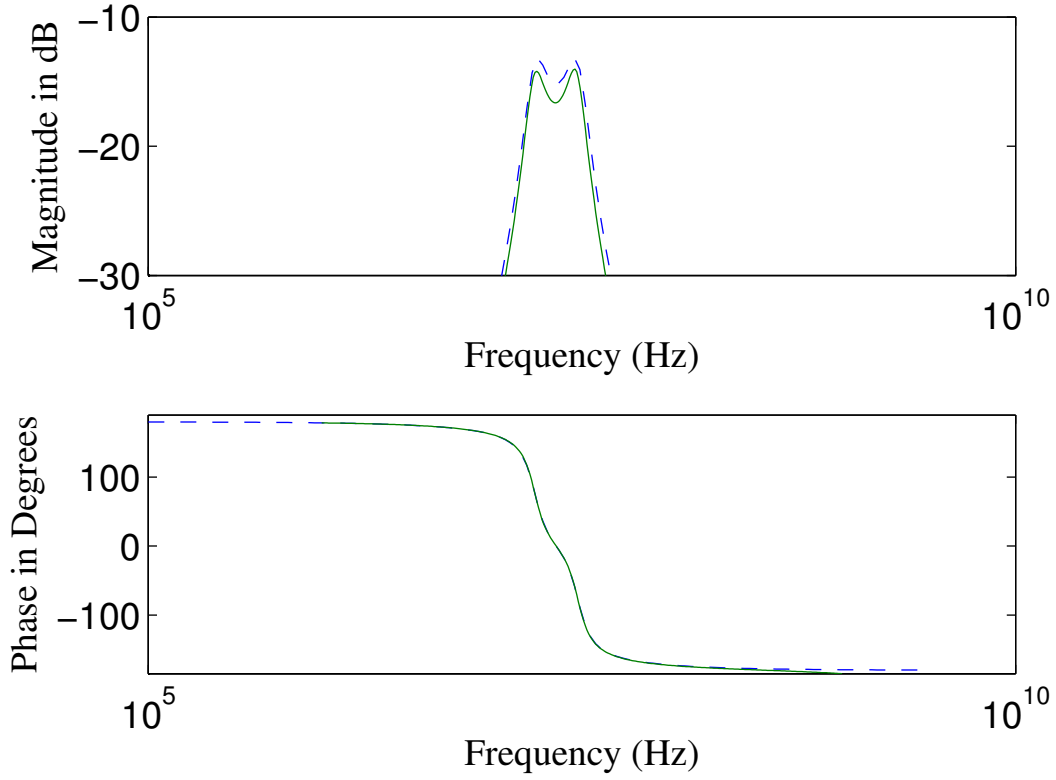


Figure 4.4: Comparison between ideal (dashed line) and simulated (solid line) magnitude and phase responses of Chebyshev filter

non-inverting and the second input at the inverting terminal. The transistors have identical sizes and are biased at the same DC voltage. The output voltage of a differential amplifier can be expressed as

$$v_{out} = A_{DM}(v_1 - v_2) \pm A_{CM} \left(\frac{v_1 + v_2}{2} \right) \quad (4.2)$$

where A_{DM} and A_{CM} are the differential and common mode voltage gains, respectively. The purpose of the differential amplifier is to amplify the difference between the two input signals and suppress the common voltage at the inputs. Thus, an ideal differential amplifier should have zero common mode voltage gain or infinite common mode rejection ratio (CMRR), which is the ratio of differential to common mode gain. The biasing circuitry consists of a current source I_b and a diode connected transistor M_8 which forms current mirror

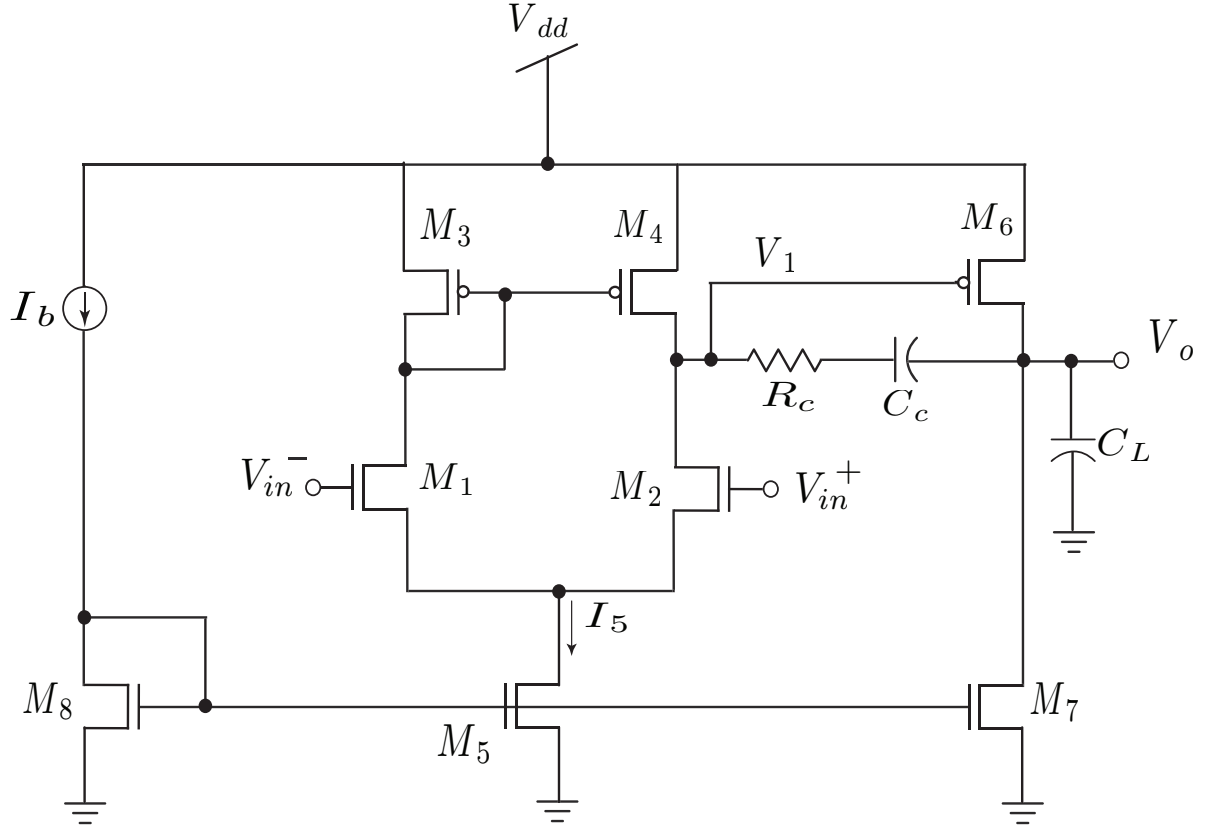


Figure 4.5: Two stage operational amplifier [33, 34]

with n-channel transistors M_5 and M_7 . The transistor M_5 acts as a tail current source. I_b provides a DC gate voltage to M_5 generating a current sink I_5 that biases M_1 and M_2 . The gate terminal of M_5 is at ac ground and the resistance of the tail current source is the resistance seen into the drain of M_5 , which is r_{ds5} . Ideally a tail current source should have infinite resistance so that common mode rejection ratio (CMRR) is infinite. The higher the resistance of the tail current source, the lower will be the common mode gain, resulting in better common mode rejection ratio for the differential amplifier. Transistors M_3 and M_4 of p-channel type form a current mirror active load connected between the drains of M_1 and M_2 and the power supply V_{dd} . Therefore, the current flowing through M_3 is mirrored onto transistor M_4 by virtue of the transistors having matched properties and the gate terminals tied together resulting in same gate to source voltage (V_{gs}). This guarantees the same drain

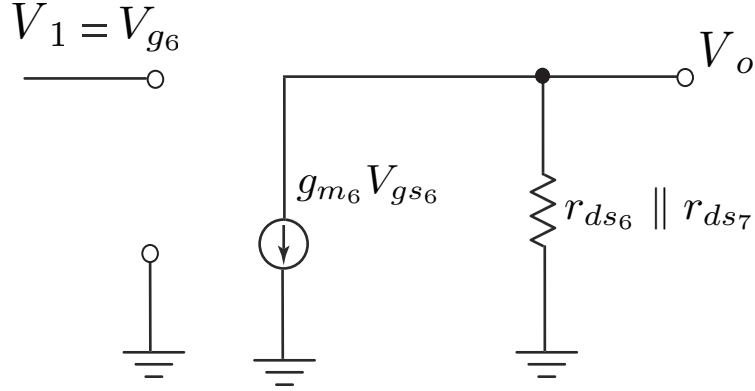


Figure 4.6: Small signal diagram of a common source amplifier

currents $I_5/2$ flowing through the two branches, that adds up to I_5 , the current in the tail current sink M_5 . The current mirror topology converts the differential input signal to a single ended output signal. Since the input and output signals are currents, an ideal current mirror will have zero input resistance and infinite output resistance. However, for real current mirrors, the input resistance is determined by the diode connected transistor M_3 and can be shown to be $(1/g_{m3}) \parallel r_{ds3} \approx (1/g_{m3})$ for $r_{ds3} \gg 1/g_{m3}$. The output resistance of the current mirror seen looking into the drain terminal of M_4 is r_{ds4} , which is large enough to provide a good voltage gain. The gain of the first stage is derived to be $A_{v1} = g_{m1} (r_{ds2} \parallel r_{ds4})$.

The second stage is a common source gain stage that is included to provide additional gain. Here, transistor M_6 serves as the p-channel common source amplifier along with M_7 as the active load. The gain of the second stage is given by $A_{v2} = g_{m6} (r_{ds6} \parallel r_{ds7})$ which is obtained from the small signal model of the common source amplifier as shown in Figure 4.6.

4.4.1 Slew Rate

The slew rate (SR) is the maximum rate of change of opamp output voltage. In the case of a differential amplifier when there is a large input signal, SR is determined by the current flowing through compensation capacitance C_C . When input voltage at the non-inverting terminal is maximum such that M_1 is off, M_2 is on and the current mirror pair M_3, M_4 is

off, the bias current I_5 will flow from C_C . Conversely, when input voltage at the inverting terminal is maximum, M_2 is off and the bias current I_5 flows through M_1 and the current mirror pair M_3, M_4 into the compensation capacitor C_C . In both cases, the maximum current entering or leaving C_C is I_5 yielding $SR = \frac{I_5}{C_C}$.

4.4.2 Compensation of the two stage operational amplifier

It is known that the stability of an amplifier can be checked from the frequency and phase responses of the amplifier. A minimum phase margin of 45° is required to ensure stability, while 60° is usually preferred to avoid ringing effect of output signals [33, 34]. First order systems have one pole and hence is unconditionally stable with a phase margin close to 90° . However, second order systems have two poles that cause a negative phase shift of 90° for each pole and can lead to a poor phase margin depending on the positions of the poles and unity gain frequency. Hence, the Miller compensation technique is used to modify the phase margin to a desired value to keep the second order system stable. In this method, a compensation capacitor C_C is connected from the output of first stage to the input of the second stage.

The differential stage has a pole located at $\omega_{p1} = \frac{1}{R_1 C_1}$, where $R_1 = r_{ds2} \parallel r_{ds4}$ is the resistance seen from the output of the differential stage and C_1 is the capacitance seen from the output of the differential stage. Due to Miller effect, the effective capacitance connected in parallel to R_1 increases to $C_C (1 + A)$ where A is the gain from V_1 to V_{out} , causing the first pole to move to a much lower frequency. Also, the compensation capacitor causes the second pole shift to a higher frequency, preferably more than the unity gain frequency. The overall objective of the Miller compensation is to reduce the frequency of one dominant pole to make it much lower relative to the other poles and zeroes, causing the second order system frequency response to be similar to that of a first order system. From the transfer function [33] of the two stage opamp, it is seen that in addition to two poles, there is also a zero present in the right half plane that produces a negative phase shift, degrading the

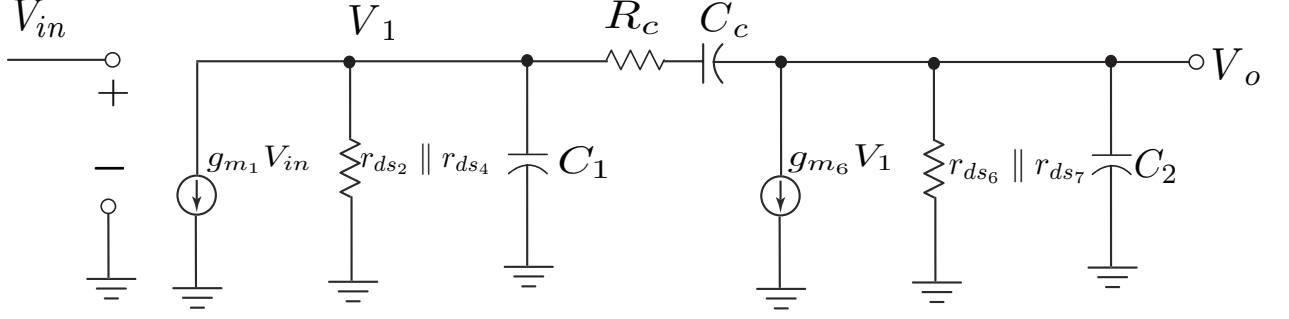


Figure 4.7: Small signal model of two stage operational amplifier

stability of the system. Hence to remedy the situation a nulling resistor R_C is introduced. Different methods of controlling RHP zero using R_C is mentioned in [33,34]. For this case, R_C is chosen such that it cancels out the zero. The small signal diagram of the two stage opamp is shown in Figure 4.7. The poles and zeroes found from the transfer function are as follows

$$\omega_{p1} = \frac{1}{g_{m6} R_1 R_2 C_C} \quad (4.3)$$

$$\omega_{p2} = \frac{g_{m6}}{C_2} \quad (4.4)$$

$$\omega_z = -\frac{1}{C_C (1/g_{m6} - R_C)} \quad (4.5)$$

where $R_2 = r_{ds6} \parallel r_{ds7}$ is the output resistance of the second stage and C_2 is the output capacitance of the second stage.

4.5 Chebyshev filter cascaded with two stage operational amplifier

Since the pole frequencies of the Chebyshev filter are at 17 MHz and 29 MHz, the gain bandwidth product of the opamp was designed to be at 530 MHz, as beyond the unity gain bandwidth the Chebyshev gain gets even lower than the original. The designed opamp had a gain of 31 dB and phase margin of 56°. Note that it is possible to improve the gain of

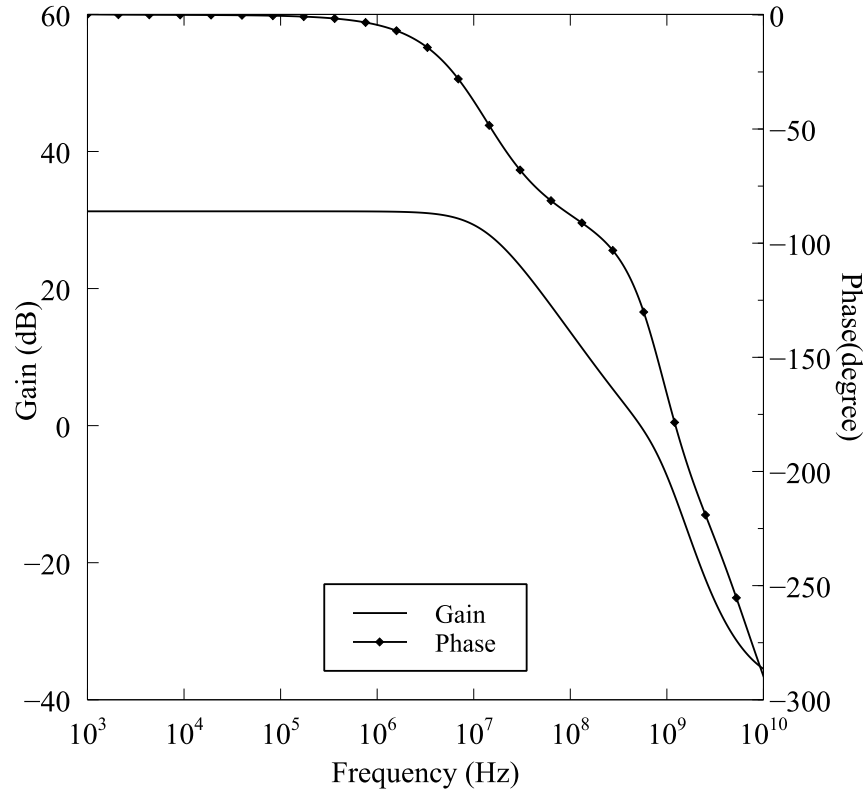


Figure 4.8: Magnitude and phase response of two stage operational amplifier simulated in Cadence

the opamp further by adding a cascode gain stage. Design procedures of such opamps are discussed extensively in [33, 34] and other research papers. However, in this work, the objective was to design an amplifier that will raise the gain of the Chebyshev filter to unity. The simulated magnitude and phase responses of the two stage opamp is shown in Figure 4.8. The designed opamp was cascaded with the fourth order Chebyshev filter as shown in Figure 4.9 which yielded a magnitude response that is close to unity gain at the pole frequencies as illustrated in Figure 4.10.

4.6 Experimental Results

The proposed Chebyshev filter in Figure 4.1 was validated experimentally using discrete components and CD4007 transistor arrays that operated from a 5 V supply. Component

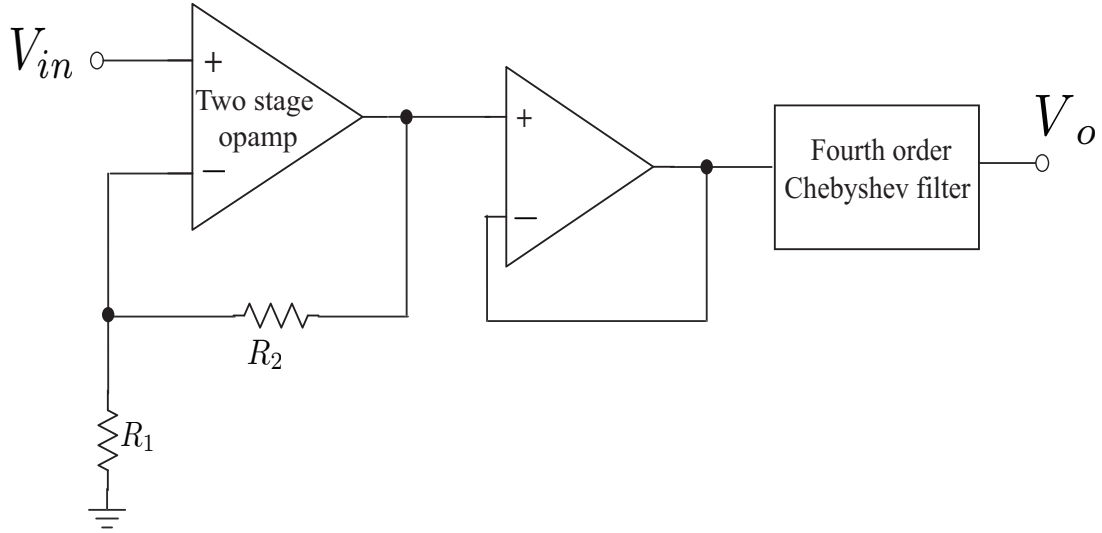


Figure 4.9: Two stage opamp cascaded with fourth order Chebyshev filter of Figure 4.1 to improve overall gain of the filter

Type	Pole frequency f_{o1} (kHz)	Pole frequency f_{o2} (kHz)	Gain ($K_1 = K_2$) (dB)	Ripple Magnitude (dB)
Experimental	57	78	-17.7	2.38
PSPICE Simulation	60	76.5	-15.5	2.2

Table 4.2: Deviation in experimental and PSPICE simulation results for Chebyshev filter

values used were $C_1 = 6.8$ nF, $L_1 = 1$ mH, $C_2 = 2.2$ nF, $L_2 = 2$ mH, $R_s = 900$ Ω , $R_2 = R_4 = 1$ k Ω and $R_3 = R_5 = 100$ Ω . The measured response is shown in Figure 4.11.

To check the accuracy of the experimental results, we also simulated the Chebyshev filter in PSPICE using CD4007 transistor and passive components of same values that operated from a 5 V supply. The simulated magnitude response is shown in Figure 4.12. The deviation between the experimental and the PSPICE results is given by Table 4.2. It is observed that the experimental results are close to the simulated ones. The minor differences are due to the tolerances of the discrete components and the quality factors of real inductors used.

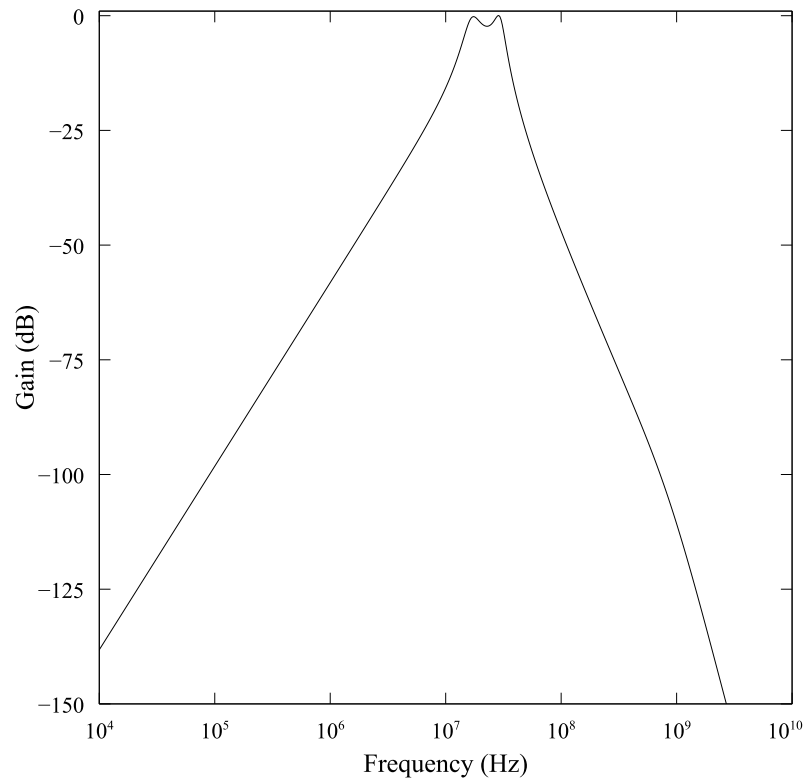


Figure 4.10: Magnitude response of the proposed Chebyshev filter after cascading with a two stage opamp

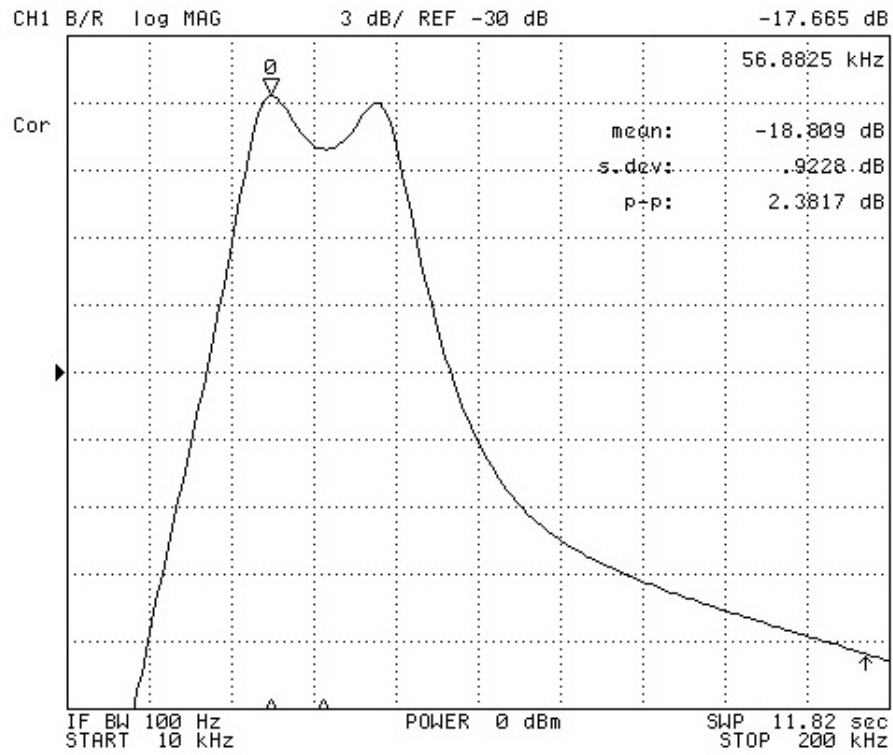


Figure 4.11: Measured magnitude response of the fourth order Chebyshev filter for component values $C_1 = 6.8$ nF, $L_1 = 1$ mH, $C_2 = 2.2$ nF, $L_2 = 2$ mH, $R_s = 900 \Omega$, $R_2 = R_4 = 1$ k Ω and $R_3 = R_5 = 100 \Omega$ with a vertical scale of 3dB/ division and horizontal scale of 20 kHz/ division.

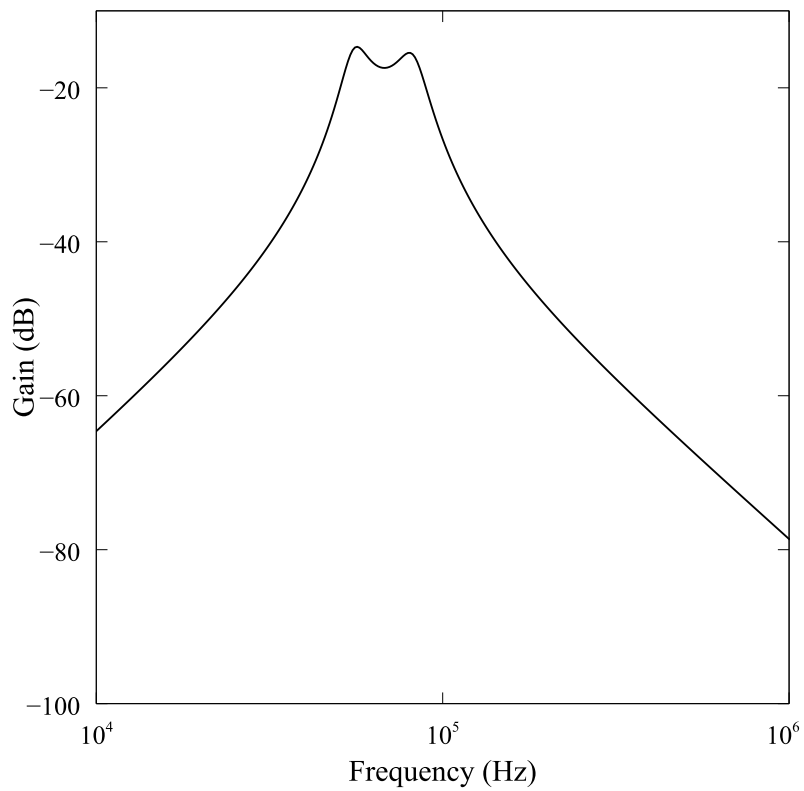


Figure 4.12: Magnitude response of fourth order Chebyshev filter simulated in PSPICE for component values $C_1 = 6.8 \text{ nF}$, $L_1 = 1 \text{ mH}$, $C_2 = 2.2 \text{ nF}$, $L_2 = 2 \text{ mH}$, $R_s = 900 \text{ } \Omega$, $R_2 = R_4 = 1 \text{ k}\Omega$ and $R_3 = R_5 = 100 \text{ } \Omega$.

CHAPTER 5

A Novel Active Comb Filter

A comb filter is a filter with a series of notches at regular spacing in its frequency response which creates the appearance of a comb. Comb filters can be used to eliminate harmonics of frequency components in biomedical instruments. Measurement signals of biomedical instruments operating on AC power line can suffer from harmonic interference which significantly affects correct interpretation of signals. Thus, some form of filtering technique is required to remove the interference. A notch filter or multiple notch filters can be useful for this purpose. In [35–37] higher order digital notch or comb filters are used to remove powerline interference at different frequencies. Different analog comb filter realizations are also found in literature. In [38], an active comb filter implemented using bandpass filter is presented that blocked four signal frequencies. A OTA-C comb filter realization is given in [39] where the notch filter was cascaded four times to eliminate harmonic components at four different frequencies. The filters found in the literature are shown to block low frequency signals (up to 500Hz) and tend to use several active and passive components. For example, [39] used two OTAs to replace every inductor and resistor for each of the four stages.

5.1 Proposed Comb Filter Structure

The single transistor bandstop filter #4 presented in Table 2.5 is used to implement a fourth order comb filter. The core of the circuit is shown in Figure 5.1. Each of the two stages of the circuit is a second order notch filter with design equations shown in Table 5.1. It

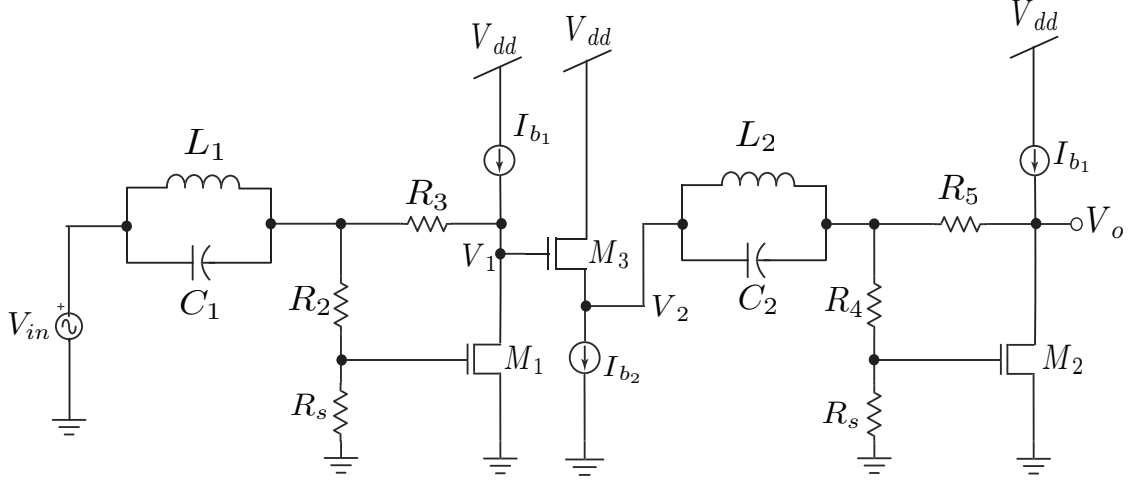


Figure 5.1: Proposed active fourth order comb filter

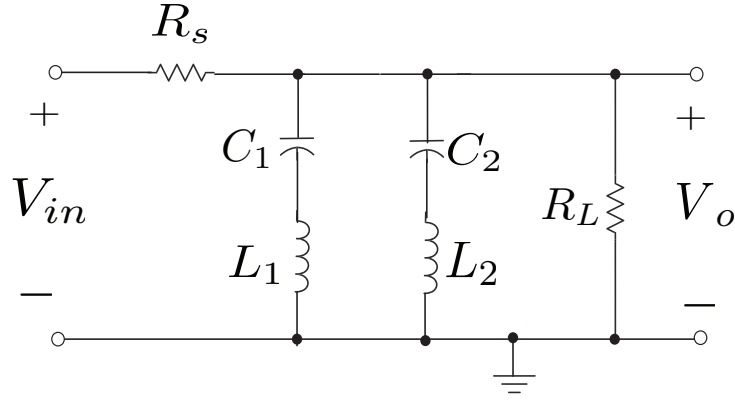


Figure 5.2: Passive fourth order Comb filter

Design Parameters	Stage 1	Stage 2
Pole frequency	$\omega_{o1} = \sqrt{\frac{1}{C_1 L_1}}$	$\omega_{o2} = \sqrt{\frac{1}{C_2 L_2}}$
Quality factor	$Q_1 = \frac{(R_2 + R_s) \sqrt{\frac{C_1}{L_1}}}{R_s g_{m1} + 1}$	$Q_2 = \frac{(R_4 + R_s) \sqrt{\frac{C_2}{L_2}}}{R_s g_{m2} + 1}$
DC Gain	$K_1 = \frac{R_2 + R_s - R_3 R_s g_{m1}}{R_2 + R_s}$	$K_2 = \frac{R_4 + R_s - R_5 R_s g_{m2}}{R_4 + R_s}$

Table 5.1: Comb filter design equations for the two stages

is observed that the classical passive fourth order bandstop filter given in Figure 5.2 is simpler compared to the proposed topology. However, active implementations of higher order comb filters usually used several opamps/ OTRAs and passive elements, as shown in [39]. The proposed implementation of a fourth order comb filter using three transistors and a minimum number of passive components is shown in Figure 5.1.

A comb filter with notch frequencies at 16.3 MHz and 163 MHz for a Q of 3 and a DC gain close to unity was designed. The general transfer function of a two stage notch filter is

$$\frac{V_o}{V_{in}} = K_1 K_2 \frac{(s^2 + \omega_{o1}^2)(s^2 + \omega_{o2}^2)}{\left(s^2 + \frac{\omega_{o1}}{Q}s + \omega_{o1}^2\right)\left(s^2 + \frac{\omega_{o2}}{Q}s + \omega_{o2}^2\right)} \quad (5.1)$$

where K_1, K_2 are the gains and ω_{o1}, ω_{o2} represent the pole frequencies of the first and second stages, respectively. The first and second stages are designed such that they have the same DC gain of unity ($K_1 = K_2$) and same quality factor Q at different pole frequencies. To obtain a characteristic response of a fourth order comb filter, the general transfer function given by equation (5.1) was plotted in MATLAB for $f_{o1} = 16.3$ MHz, $f_{o2} = 163$ MHz, $Q = 3$ and $K_1 = K_2 = 0.99$. The magnitude and phase responses are shown in Figure 5.3.

The notch circuit design equations were used to calculate component values in MAPLE for each stage. A unity gain buffer or an isolation buffer was placed in between the two filter stages due to the difference in impedances between the two circuit stages which can cause the second stage to load the first stage of the circuit. The voltage buffer was implemented using a source follower as shown in Figure 4.3.

5.2 Simulation Results

The validity of the proposed comb filter structure was tested using Cadence with the component values set to $C_1 = 9.5$ pF, $L_1 = 10$ μ H, $C_2 = 0.95$ pF, $L_2 = 1$ μ H, $R_s = 1.2$ k Ω , $R_2 = R_4 = 600$ Ω and $R_3 = R_5 = 110$ Ω , which produced notches at 16.2 MHz and 162 MHz. The simulated filter consumed 2.1mW from a power supply of 1.5 V. The two MOS transistors had aspect ratios $W/L = 0.48\mu m / 0.18\mu m$ and cutoff-frequencies $f_T = 10$ GHz. The simulated response of the comb filter is shown in Figure 5.4. At the rejection frequencies 16.2 MHz and 162 MHz, the notch depths were at -34.77 dB and -34.55 dB, respectively. A bias current source of 700 μ A was used for both the stages and $g_{m1} = 73.8$

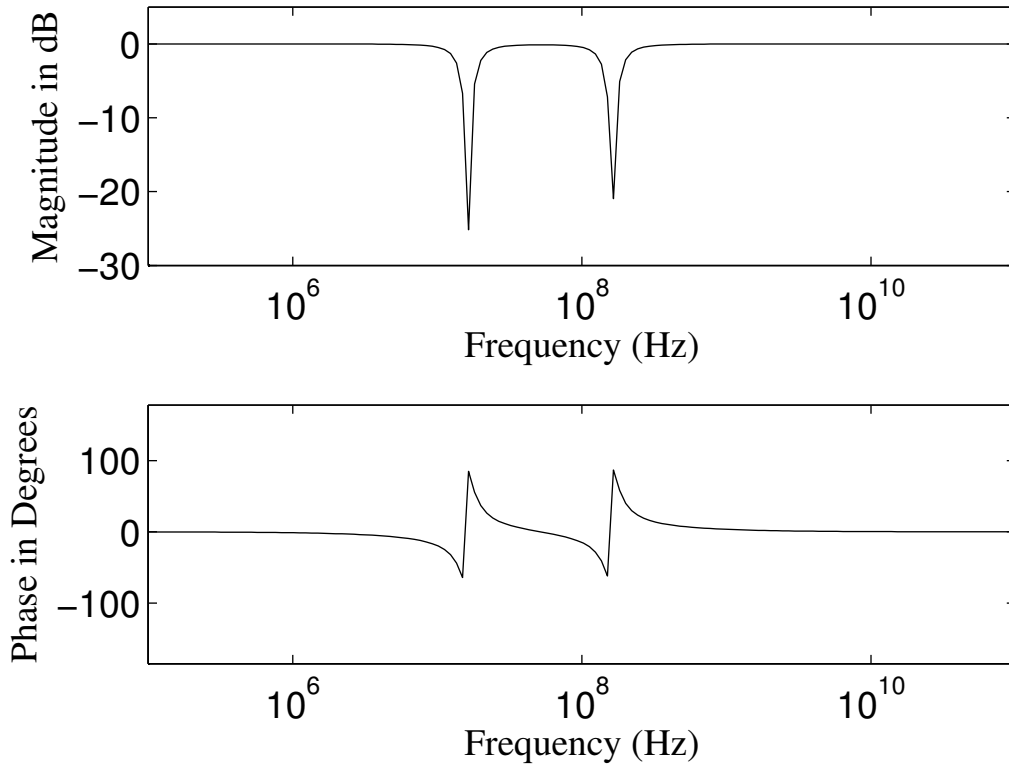


Figure 5.3: Magnitude and phase responses of a general comb filter transfer function given by equation (5.1) plotted in MATLAB for $f_{o1} = 16.3$ MHz, $f_{o2} = 163$ MHz, $Q = 3$ and $K_1 = K_2 = 0.99$.

$\mu A/V$, $g_{m2} = 99.46 \mu A/V$ for a Q of 3 yielded a DC gain of -0.111 dB which is very close to the theoretical -0.1 dB DC gain. The input signals at rejection frequencies 16.2 MHz and 162 MHz and their corresponding outputs are shown in Figures 5.5 and 5.6. It is observed that the amplitude of the output signals is much smaller than that of the input signals at the two notch frequencies as the magnitudes are very low at those frequencies.

It is known that biomedical signals such as ECG signals contain power line harmonics that affect the original signals [38] [39]. The proposed comb filter can be used to remove unwanted power line signals at fundamental frequency of 50 Hz and its odd harmonics. We designed the comb filter in Figure 5.1 to remove two frequencies 50 Hz and 150Hz as shown in Figure 5.7.

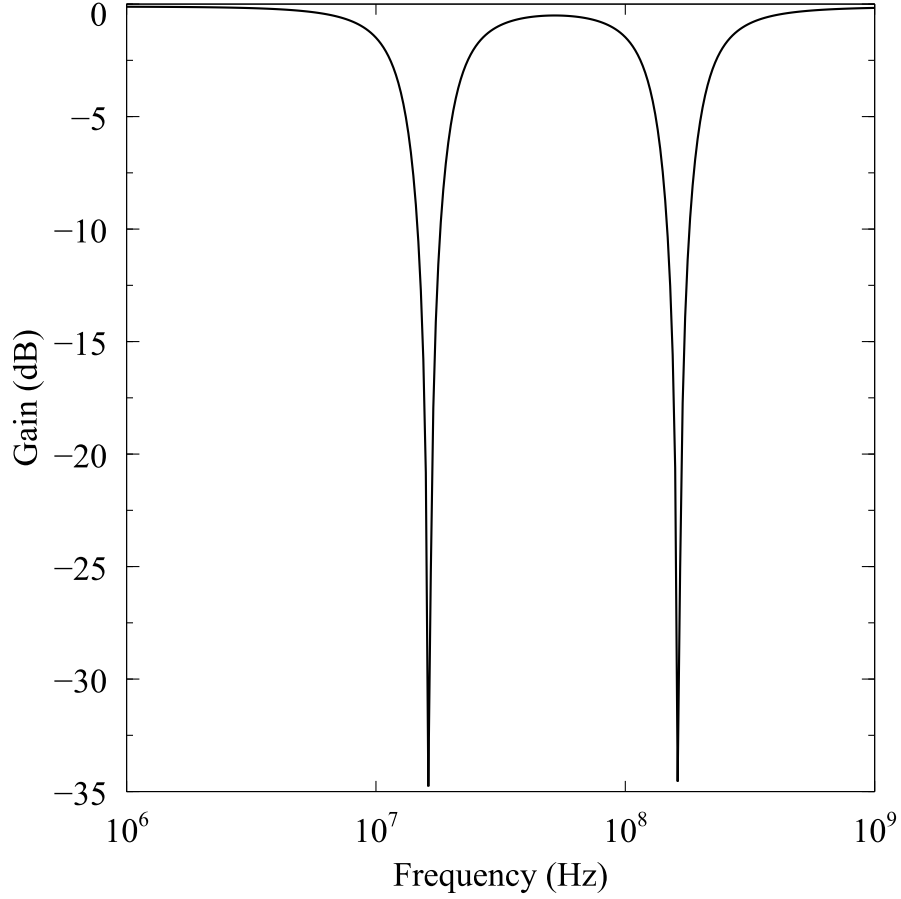


Figure 5.4: Cadence simulated magnitude response of fourth order comb filter for values $C_1 = 9.5 \text{ pF}$, $L_1 = 10 \text{ } \mu\text{H}$, $C_2 = 0.95 \text{ pF}$, $L_2 = 1 \text{ } \mu\text{H}$, $R_s = 1.2 \text{ k}\Omega$, $R_2 = R_4 = 600 \text{ } \Omega$ and $R_3 = R_5 = 110 \text{ } \Omega$.

5.3 Experimental Results

To validate the proposed comb filter and to test its practical use, experimental measurements were carried out using CD4007 transistor arrays and other discrete circuit elements. The circuit operated from a single 5 V power supply while component values used were $C_1 = 2.2 \text{ nF}$, $L_1 = 10 \text{ mH}$, $C_2 = 33 \text{ pF}$, $L_2 = 2 \text{ mH}$, $R_s = 1.2 \text{ k}\Omega$, $R_2 = R_4 = 500 \text{ } \Omega$ and $R_3 = R_5 = 100 \text{ } \Omega$ that resulted in pole frequencies at 34 kHz and 620 kHz with a measured DC gain of -0.3054 dB which is close to calculated pole frequencies of 33 kHz and 619 kHz with a calculated DC gain of -0.1 dB. Also the measured response shown in Figure 5.8 is similar to the characteristic fourth order comb filter response shown in Figure 5.3.

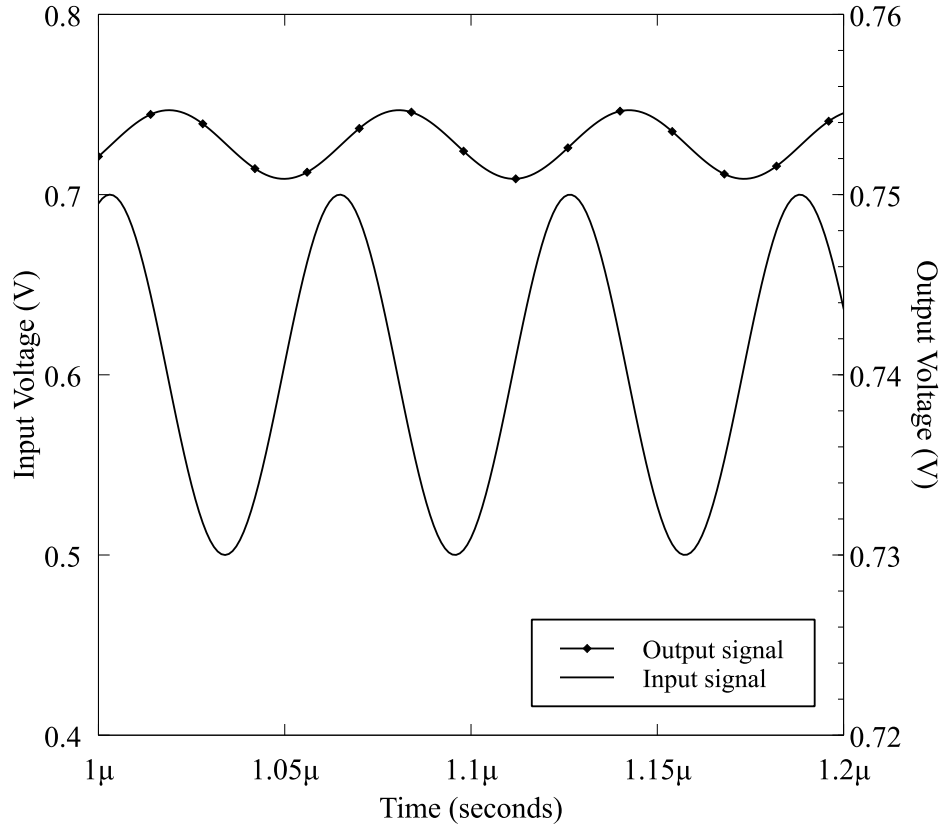


Figure 5.5: Input (V_{in}) and output (V_o) waveforms of Comb filter in Figure 5.1 at $f_{o1} = 16.2$ MHz simulated in Cadence

Type	Pole frequency f_{o1} (kHz)	Pole frequency f_{o2} (kHz)	DC Gain (dB)
Experimental	34	620	-0.3
PSpice Simulation	33.8	618	-0.4

Table 5.2: Deviation in experimental and PSpice simulation results for Comb filter

To verify the experimental results, we also simulated the comb filter in PSpice using CD4007 transistors and passive components of same values that operated from a 5 V supply. The simulated magnitude response is shown in Figure 5.9. The deviation between the experimental and the PSpice results is given by Table 5.2. It is observed that the experimental results are very close to the simulated ones. The minor differences are attributed to the tolerances of the discrete components.

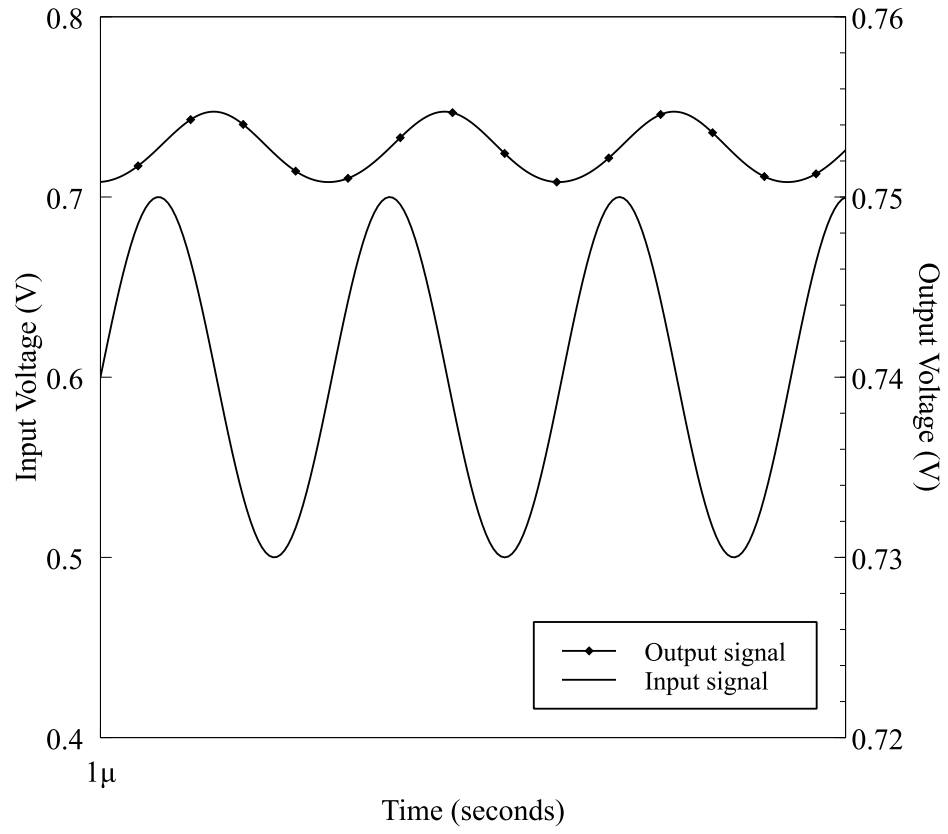


Figure 5.6: Input (V_{in}) and output (V_o) waveforms of Comb filter in Figure 5.1 at $f_{o2} = 162$ MHz simulated in Cadence

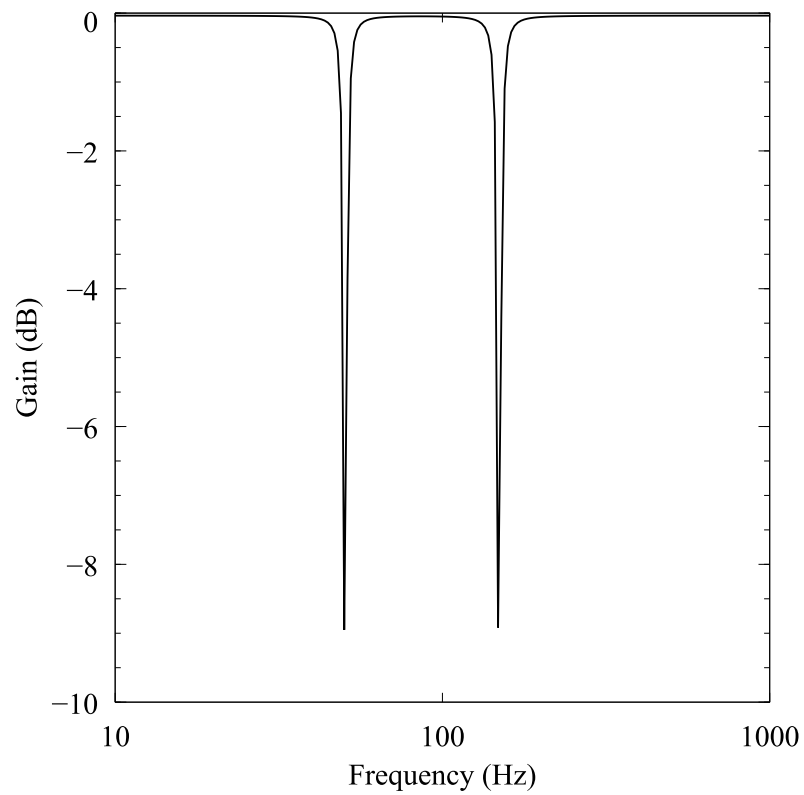


Figure 5.7: Cadence simulated response of comb filter designed to remove power line interferences at 50 Hz and 150 Hz

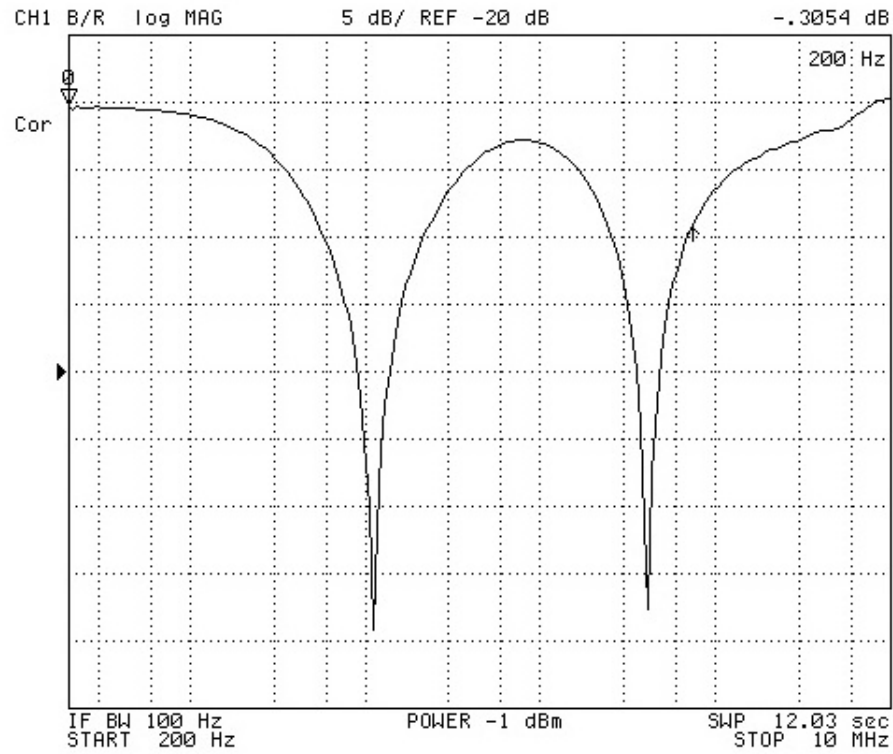


Figure 5.8: Measured magnitude response of comb filter implemented using discrete components of values $C_1 = 2.2 \text{ nF}$, $L_1 = 10 \text{ mH}$, $C_2 = 33 \text{ pF}$, $L_2 = 2 \text{ mH}$, $R_s = 1.2 \text{ k}\Omega$, $R_2 = R_4 = 500 \text{ }\Omega$ and $R_3 = R_5 = 100 \text{ }\Omega$ with a vertical scale of 5dB/ division and a logarithmic horizontal scale where each cycle represents a factor of 10.

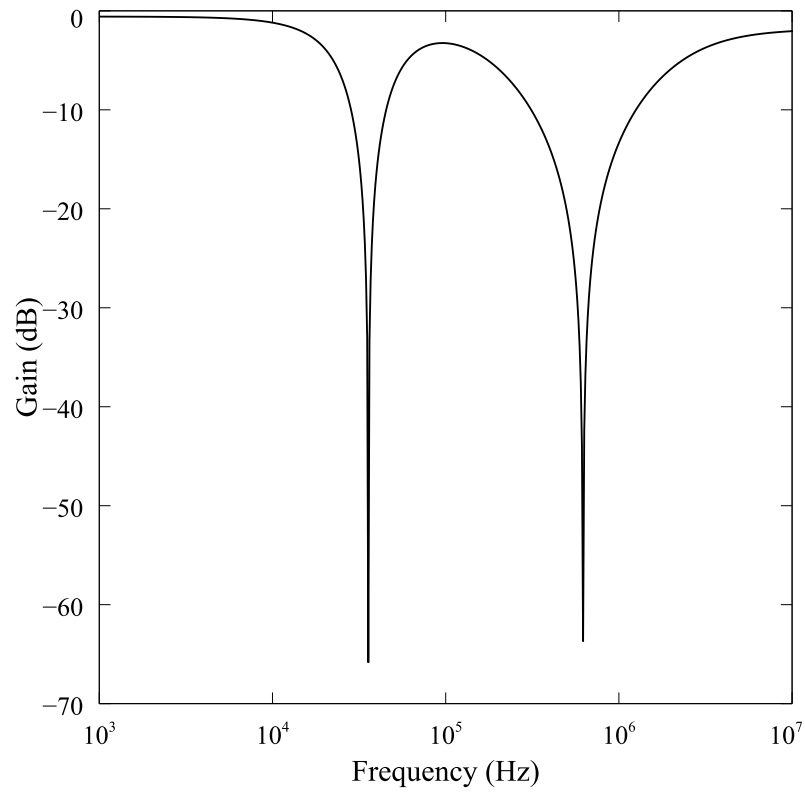


Figure 5.9: Magnitude response of fourth order Comb filter simulated in PSPICE for component values $C_1 = 2.2$ nF, $L_1 = 10$ mH, $C_2 = 33$ pF, $L_2 = 2$ mH, $R_s = 1.2$ k Ω , $R_2 = R_4 = 500$ Ω and $R_3 = R_5 = 100$ Ω .

CHAPTER 6

Conclusions and Future Work

6.1 Conclusion

In this work new implementations of different second and higher order active filter topologies are presented. Four different configurations were introduced where a single transistor was considered as a two port network surrounded by a minimum number of impedances that formed a T-network. The transfer functions of the proposed general topologies were found by means of nodal analysis and an exhaustive search for all possible second order filters was performed in MAPLE for different impedance combinations. The results of the search was then compared with a general second order transfer function to determine the filter type. The transfer function and expressions of design parameters such as quality factor Q , gain K and pole frequency ω_o for each filter were presented. Input and output impedances of the second order filters were derived for different frequencies. The filters were designed using an ideal transistor model but possible effects of more complex transmission matrices on transfer function, poles/zeros and order of the filters were explored and presented. The effects of high frequency parasitic capacitances were investigated and expressions of extra poles and zeros due to the parasitics were derived for some examples. Higher order filters such as a fourth order Chebyshev and a fourth order Comb filters were designed based on the single transistor active filter topologies. Each filter was simulated using Cadence Spectre and the results were compared with theoretical values and with ideal responses obtained by plotting characteristic transfer functions of the filters in MATLAB. The proposed filters were validated by experimental measurements using real

circuit components.

6.2 Trade-offs

All active filters are expected to have some trade-offs in their designs. In this work the trade-offs are as follows:

1. The gain of the proposed filters cannot exceed unity as it will cause one of the terms to become negative. Only Type-1 gain equalizer filters #1 and #3 (Table 2.2) have $K > 1$, while Type-3 gain equalizer filter #3 (Table 2.4) have negative gain.
2. Some of the filters require an extra biasing network such as Type-1 gain equalizer filter #1 (Table 2.2) and alternate Type-3 allpass filter #1 (Table 2.5) as discussed in Section 2.4.5.
3. The four general topologies did not yield any lowpass and highpass filter types.
4. The topologies are not directly cascadable and a buffer circuit has to be used between two stages to prevent loading.

6.3 Contribution

There are three main contributions of this thesis. The first contribution is that it adds to the work on single transistor active filters that was first presented in [15] and further explores and applies the design procedures to introduce additional circuit topologies. This work introduced four general topologies from which several second order filters have been derived. Complete design procedures, biasing details and non-ideal effects of selected filter types have been discussed in details and the circuits have been validated using Cadence simulations and experimental measurements. All the second order filter circuits are concise with only one transistor as an active element and four impedances. The filters can be implemented in discrete and integrated circuit form.

The second contribution is that this work has presented several gain equalizer and all-pass filters. To the best of our knowledge there is no single transistor implementation of gain equalizer filters found in literature. While active implementations of such filters were reported, they consisted of opamps, OTRAs or other complex building blocks [3, 5, 7]. The proposed active realizations of gain equalizer filters have used one transistor and four impedances. To date, single transistor allpass filter was presented in [15], [16]. This work presented an alternative realization of allpass filters using a single transistor and four impedances. A possible comparison between the two realizations can be a future topic of study.

Another contribution of this work is that it has presented two higher order active filters based on the designed second order filters. Novel implementations of a fourth order bandpass Chebyshev filter and a fourth order Comb filter have been presented. Compared to active realizations of higher order filters reported in literature that used two or more opamps, the proposed implementations of higher order filters have used three transistors and some passive elements. All the designed filters have been shown to operate from a low supply voltage of 1.5 V.

6.4 Future Work

There are several areas related to this work that can be further explored. Recently, integrated circuit realization of a single transistor filter based on the work of [15] was presented in [16] with promising results. This demonstrates that single transistor second order filters are suitable for IC implementations. This idea can be extended to the IC implementations of proposed higher order filters. In this work, the second order filters have used passive inductors. It is known that passive monolithic integrated inductors used in CMOS processes occupy large chip area. Hence, different active realizations of the inductors can be explored and its possible effects on the designed circuits can be investigated.

This work focused on the magnitude, phase and transient responses of the designed

filters. Future work on noise figure analysis of the circuits can be done. Also, it has been found that the second order filters are not suitable at very high frequencies due to the effects of parasitic capacitances that change the order of the filter. Further work can be done to develop ways to operate the circuits at very high frequencies.

In this work, a fourth order Chebyshev filter has been designed based on the single transistor filter. This can be extended to the realizations of other filter approximations such as Butterworth and Elliptic filters.

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